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CSE 3666

4/6/17

Architecture Assignment 7

Instructions:

add $t0, $t1, $t2

lw $t1, 8 ($sp)

sw $ra, 4 ($sp)

addi $sp, $sp, 4

sub $t0, $t0, $t1

Cycle 1

Instruction 1, stage 1: add $t0, $t1, $t2

IF/ID

PC+4: 0x0040C004

Instruction: 0x012A4020

Cycle 2

Instruction 1, stage 2: add $t0, $t1, $t2

ID/EX

Function code: 0x20

Data 1: 40

Data 2: 5

Immediate: 0x00001021

Destination Register: $t0

RS: $t1

RT: $t2

ALU Src: 0

Mem Read: 0

Mem Write: 0

Mem to Reg: 0

RegWrite: 1

Instruction 2, stage 1: lw $t1, 8 ($sp)

IF/ID

PC+4: 0x0040C008

Instruction: 0x8FA90008

Cycle 3

Instruction 1, stage 3: add $t0, $t1, $t2

EX/Mem

Zero?: 0

ALU result: 45

Data 2: 5

Destination Register: $t0

Mem Read: 0

Mem Write: 0

Mem to Reg: 0

RegWrite: 1

Instruction 2, stage 2: lw $t1, 8 ($sp)

ID/EX

Function Code: 0x3C

Data 1: 0xFFFF F000

Data 2: 40

Immediate: 8

Destination Register: $t1

RS: $sp

RT: $tq

ALU Src: 1

Mem Read: 1

Mem Write: 0

Mem to Reg: 1

RegWrtie: 1

Instruction 3, stage 1: sw $ra, 4 ($sp)

IF/ID

PC+4: 0x0040C00C

Instruction: 0xAFBF0004

Cycle 4

Instruction 1, stage 4: add $t0, $t1, $t2

Mem/WB

Read Data: 0

ALU Result: 45

Destination Register: $t0

Mem to Reg: 0

Reg Write: 1

Instruction 2, stage 3: lw $t1, 8 ($sp)

EX/Mem

Zero?: 0

ALU result: 125

Data 2: 40

Destination Register: $t1

Mem Read: 1

Mem Write: 0

Mem to Reg: 1

Reg Write: 1

Instruction 3, stage 2: sw $ra, 4 ($sp)

ID/EX

Function Code: 0x2B

Data 1: 0xFFFF F000

Data 2: 0x0400 BA12

Immediate: 4

Destination Register: $ra

RS: $sp

RT: $ra

ALU Src: 1

Mem Read: 0

Mem Write: 1

Mem to Reg: X

RegWrite: 0

Instruction 4, stage 1: addi $sp, $sp, 4

IF/ID

PC+4: 0x0040C010

Instruction: 0x23BD0004

Cycle 5

Instruction 2, stage 4: lw $t1, 8 ($sp)

Mem/WB

Read Data: 0

ALU Result: 125

Destination Register: $t1

Mem to Reg: 1

RegWrite: 1

Instruction 3, stage 3: sw $ra, 4 ($sp)

EX/Mem

Zero?: 0

ALU Result: 0xFFFF F004

Data 2: 0x0400 BA12

Destination Register: $ra

Mem Read: 0

Mem Write: 1

Mem to Reg: X

RegWrite: 0

Instruction 4, stage 2: addi $sp, $sp, 4

ID/EX

Function Code: 0x04

Data 1: 0xFFFF F000

Data 2: 0xFFFF F000

Immediate: 4

Destination Register: $sp

RS: $sp

RT: $sp

ALU Src: 1

Mem Read: 0

Mem Write: 0

Mem to Reg: 0

RegWrite: 1

Instruction 5, stage 1: sub $t0, $t0, $t1

IF/ID

PC+4: 0x0040C014

Instruction: 0x01094022

Cycle 6

Instruction 3, stage 4: sw $ra, 4 ($sp)

Mem/WB

Read Data: 0

ALU Result: 0xFFFF F004

Destination Register: $ra

Mem to Reg: X

RegWrite: 0

Instruction 4, stage 3: addi $sp, $sp, 4

EX/Mem

Zero?: 0

ALU Result: 0xFFFF F004

Data 2: 4

Destination Register: $sp

Mem Read: 0

Mem Write: 0

Mem to Reg: 0

RegWrite: 1

Instruction 5, stage 2: sub $t0, $t0, $t1

ID/EX

Function Code: 0x22

Data 1: 45

Data 2: 125

Immediate: 0x x00001022

Destination Register: $t0

RS: $t0

RT: $t1

ALU Src: 0

Mem Read: 0

Mem Write: 0

Mem to Reg: 0

RegWrite: 1

Cycle 7

Instruction 4, stage 4: addi $sp, $sp, 4

Mem/WB

Read Data: 0

ALU Result: 0xFFFF F004

Destination Register: $sp

Mem to Reg: 0

RegWrite: 1

Instruction 5, stage 3: sub $t0, $t0, $t1

EX/Mem

Zero?: 0

ALU Result: -80

Data 2: 125

Destination Register: $t0

Mem Read: 0

Mem Write: 0

Mem to Reg: 0

RegWrite: 1

Cycle 8

Instruction 5, stage 4: sub $t0, $t0, $t1

Mem/WB

Read Data: 0

ALU Result: -80

Destination Register: $t0

Mem to Reg: 0

RegWrite: 1

Cycle 9

Final Register Values (that are relevant):

$t0 = -80

$t1 = 125

$t2 = 5

$sp = 0xFFFFF004

$ra = 0x0400BA12

$sp+8 = 125

($sp+4 = 0x0400BA12)