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CSE 3666

Extra Assignment: Synchronous Bus Protocol

1. If the addressed device does not respond during a read operation, the protocol process will still be carried out, but the results of the process will be wrong. This is since the device cannot detect whether a malfunction has occurred during the operation. A possible remedy for this issue would be giving a response sequence from the device for a bus operation. Although this isn't necessary, it will enable the bus to stop if there is a failure to read or a lack of response. Once this error signal is detected, the device should stop and throw an error.

2. As the distance between the processor and I/O devices increases, a longer delay time between the processor and I/O devices will develop. As for the timing diagram, this can produce a skew. This skew would cause the diagram intervals to be more distended to cover worst case variation during the delay propagation. The clock speed will increase as well to have maximum propagation delay. So, the timing diagram will become more skewed, the intervals distended, and the clock timing increased.

3. The slave can only send data in the second phase of a clock, because it needs the master first to send a clock frequency for the slave to understand. Without this signal, the slave doesn't necessarily know where to put data or how much data to put. This can lead to incorrect results as well as unreliable processing, so the slave must go after the master to ensure these don't happen.

4. To create an interface that will allow all states of the 8 switches to be read simultaneously as 1 byte, each switch needs to be assigned to 2 bits. These bits will be one after the next, and they will reset they're positions (on/off) at the top when the cycle is over. The following table describes the signals/bits that each switch will have (the leftmost column is the switch number; the reset occurs in the top left corner):

	sensor 1	sensor 2	sensor 3	sensor 4	sensor5	sensor 6	sensor 7	sensor 8
1	1	0	0	0	0	0	1	1
2	1	1	0	0	0	0	0	1
3	0	1	1	0	0	0	0	0
4	0	0	1	1	0	0	0	0
5	0	0	0	1	1	0	0	0
6	0	0	0	0	1	1	0	0
7	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	1	0