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CSE 3666

Extra Assignment: Multi-Cycle Protocol

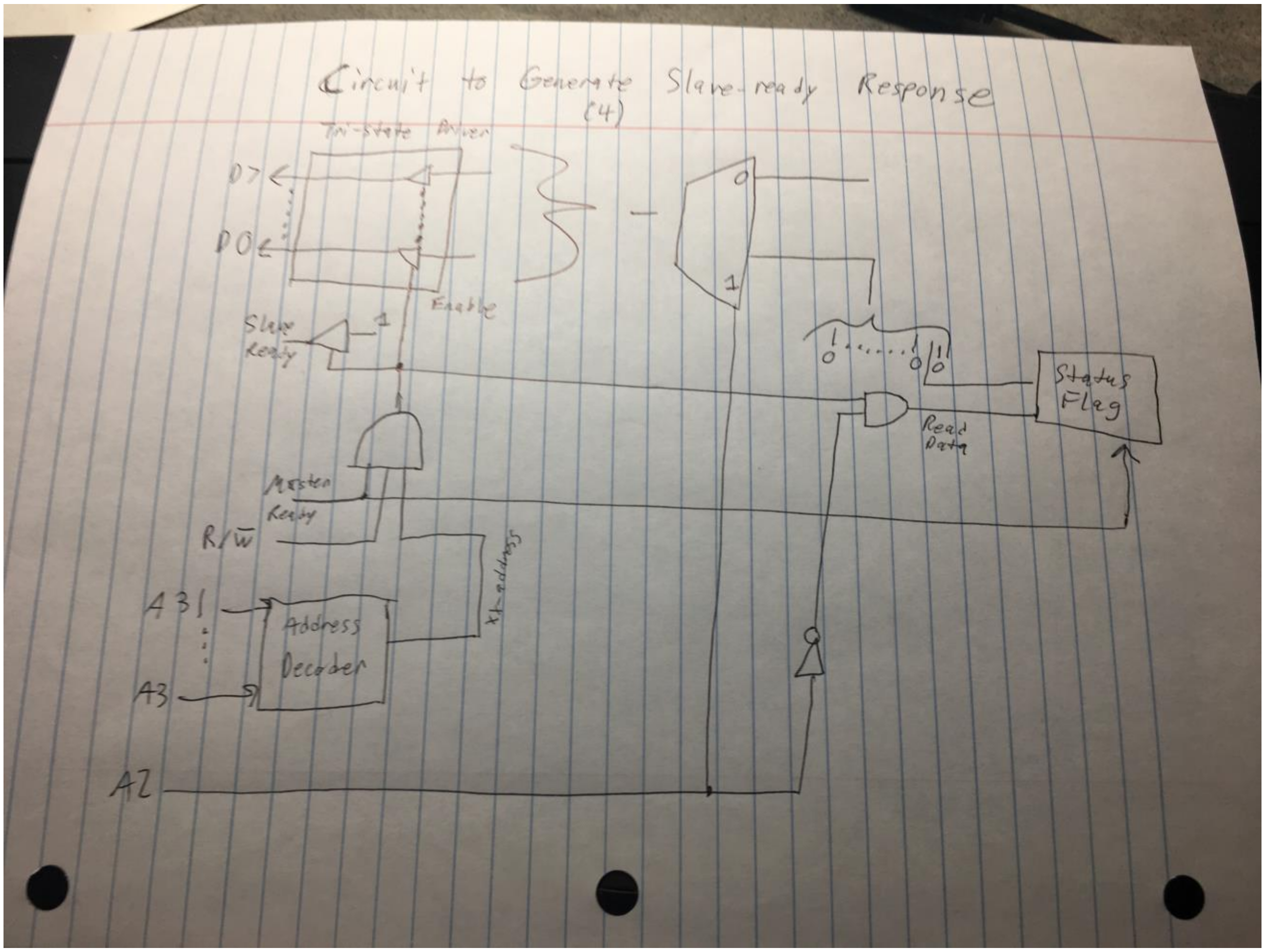
1. During a read malfunction, the processor does not know if the device doesn't respond. The processor assumes that the data from the read operation was already received after a given clock cycle. No error notification will be sent out during this malfunction, causing the device to not respond and the processor being unaware something is wrong. This can be solved by adding a control signal that responds from the devices. This control signal will display whether the data is ready to be transferred and the devices can also alter the clock cycles to act accordingly to any delay in processing the read operation.

2. The address on the bus must be maintained until some sort of response is received. This is since it is needed to remember the address on the data bus for getting data. These addresses on the data bus must also be remembered for the next cycles. Another thing that is required for the device is a buffer to store the address when it requires more time to receive the data. When this happens, the address can be removed from the bus after the very first instruction cycle.

3. a) The maximum clock speed at which the bus can operate is the maximum times and delays of all the parameters. So, it would be: Bus driver delay + maximum time for the propagation delay on the bus + address code delay + maximum time to fetch requested data + setup time = maximum clock cycle time. This translates to 3 ns + 15 ns + 6 ns + 25 ns + 2 ns = 51 ns. Maximum clock cycle time = 51 ns.

   b) Since it takes 51 ns, 4 clock cycles are needed.

4. (next page)


Circuit to Generate Slave-ready Response
(4)
Tri-state Driver
D7
D0
Enable
Slave Ready
1
0
1
Status Flag
Read Data
Master Ready
R/W
A31
Address Decoder
A3
A2