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CSE 3666

Architecture Assignment 4

Which existing blocks (if any) can be used for this instruction?

a) Instruction memory, registers, ALU, branch hardware, control, PC, and PC adder.
b) Instruction memory, registers, ALU, control, PC, and PC adder.
c) Instruction memory, registers, ALU, jump hardware, PC, and PC adder.
d) Instruction memory, control, registers, ALU, PC, and PC adder.

How will the existing blocks be used to support this instruction?

a) The registers are needed to compare data to 0. To do this comparison we need an ALU, which handles this, while the instruction memory allows for a target address to be determined as well as the register to compare to 0 (the immediate). A PC will allow to find the branch instructions in memory, while the adder adds 4 to get the next instruction. The branch hardware multiplexor allows selection between multiple PC adders to determine equivalence while the PCs in the hardware act as the control to branch hardware.
b) Registers are needed to store the values somewhere to be subtracted and the ALU does the subtraction. The instruction memory allows to get the location of the registers and where/what to do with the values in them. Control is determined by ALU register connection, but a control can be added. A PC will act as the index instruction in the memory to get the subtraction instruction, and PC adder will increment the PC for further subtraction instructions.
c) The instruction memory holds the target address of the jump while the registers hold certain values in them and a place for the instruction to carry out actions. The ALU allows for jumping along with the jump hardware, and the PC and PC adder do the same as in the subtraction instruction discussed in b).
d) Registers are needed to store the values somewhere to be subtracted and the ALU does the shift. The instruction memory allows to get the location of the registers and where/what to do with the values in them. Control is determined by ALU register connection, but a control can be added. A PC will act as the index instruction in the memory to get the shift instruction, and PC adder will increment the PC for further shift instructions.

What new or modified hardware (if any) do we need for this instruction?

a) Logic gates to control the branch multiplexor based on the result of the comparison of the value and 0.
b) None

c) A bus to pass the PC+4 to the registers and a fixed value of 31 for the write register. This would require more multiplexors.
d) None

What new signals (if any) do we need from the control unit to support this instruction?

a) A bgez signal to allow the branch multiplexor to be toggled when the value in the register is greater than or equal to 0.
b) None
c) New signals to control the additional RegDst and MemtoReg multiplexors.
d) None