Board 2 Hex Inverter (Good Layout vs Bad Layout)

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Oct 24th, 2025

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1) Objective:

To understand how switching noise and board layout affect the circuit's performance. It focuses on measuring noise levels, checking the behaviour of switching signals, and seeing how design choices impact power stability and overall board operation.

2) Bill of Materials:

I. NE555DR
II. LDO-AMS1117
III. Hex Inverter – SN7AHC14DR
IV. Resistors – 47ohm x 6
1k ohm x 4
10k ohm x 2
V. LED – 8 Nos.
VI. Power Adapter
VII. Header pins and shorting flags – 4
VIII. Capacitor – 1uF – 1
22uF – 5
IX. Mini Slide Switch - 2

3) Plan of Record:

- The board has power Jack where an AC to 5V DC adaptor can be plugged in, which supplies the main power source for the board.
- A 3.3V LDO provides power for the hex inverters. also, a filter capacitor is added to the output line with a switch, allowing observation of performance differences when the capacitor is connected or disconnected.
- A switch is included to select between 5V and 3.3V supply for the hex inverters.
- A 555-timer circuit generates a 5Vp-p square wave at 500Hz with a 60% duty cycle, serving as the clock signal for the hex inverters.
- Two hex inverter circuits are connected through the 5V/3.3V switch.
- Each inverter IC drives three LEDs to create switching activity (di/dt) synchronized with the 555-timer output.
- A 10kΩ pull-up resistor prevents floating state which causes unnecessary output trigger 555 output is idle. (due to the high input impedance of the inverter).
- Quiet High and Quiet Low Outputs from both hex inverters are monitored to evaluate rail stability and identify any voltage variations during operation.
- Resistors are added in the series of LED to limit the current passing to LED
- Test points are provided for the 5V and 3.3V power rails, 555-timer output, Quiet High, Quiet Low, and inverter trigger signals. These allow easy measurement of voltage drops and signal behaviour during testing.

4) Napkin Sketch:

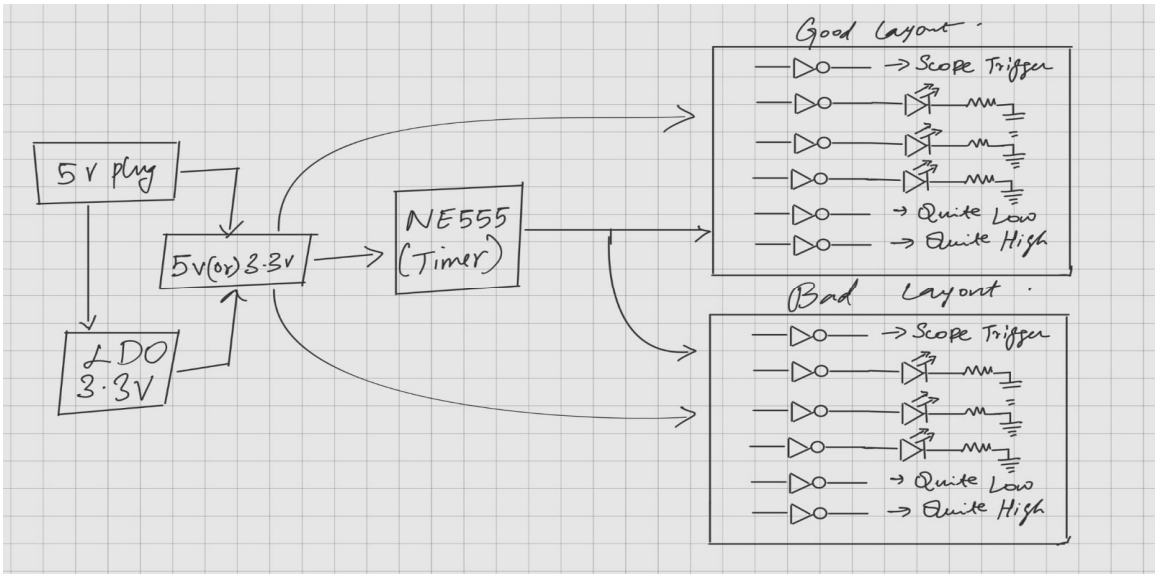

Figure 4.1 - This sketch shows the plan

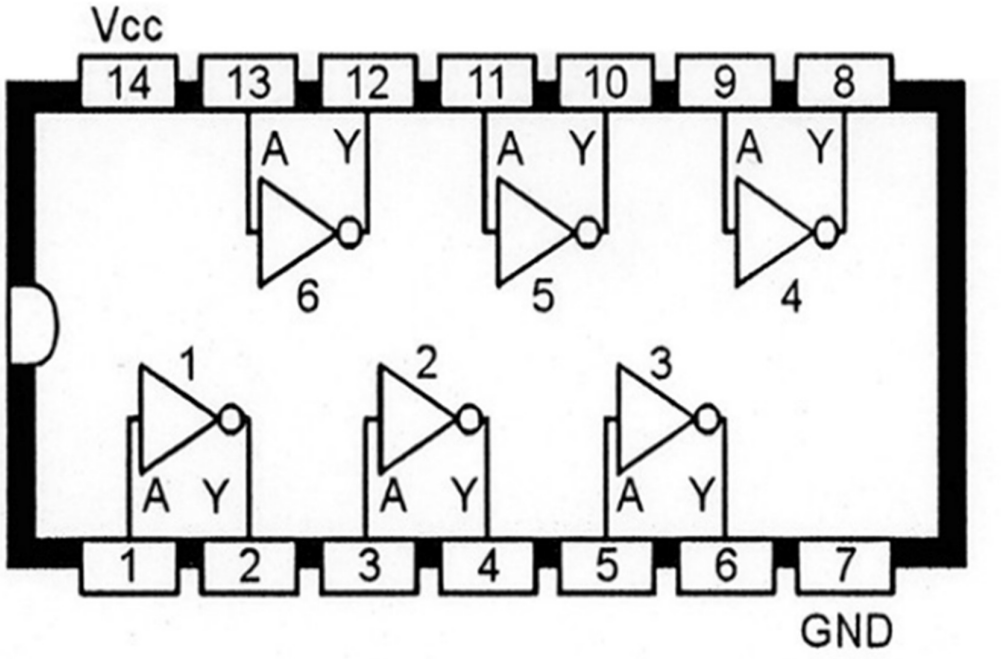

Figure 4.2 – Hex Inverter Internal working

5) Calculations:

The 555 Timer must drive 2 Hex Inverters and the NE555DR have the capabilities for sourcing and sinking are up to 200mA and the output rise time is 80ns, min input supply 4.7V

$$T_{ON} = 0.693\ (R_1 + R_2)C$$

= 0.693 (1000 +1000)(1x10^{-6})

= 1.386 ms

$$T_{OFF} = 0.693\ (R_2)C$$

= 0.693(1000)(1x10^{-6})

= 0.693 ms

$$Total\ Time(T) = T_{ON} + T_{OFF}$$

$$On\ Duty\ Cycle = \frac{R_1 + R_2}{R_1 + 2R_2}$$

On Time Duty Cycle $= \frac{2000}{3000}\ x\ 100$

= 66.66%

$$Off\ Duty\ Cycle = \frac{R_2}{R_1 + 2R_2}$$

On Time Duty Cycle $= \frac{1000}{3000}\ x\ 100$

= 33.33%

Frequency

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)C}$$

$$= \frac{1}{3000\ x10^{-6}}$$

= 480 Hz

6) Schematic & Layout:

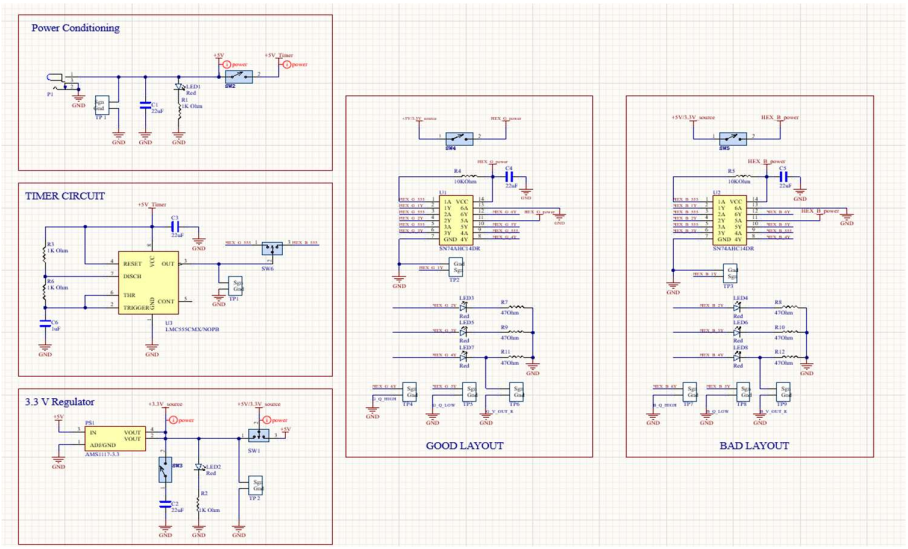

Figure 6.0 - Schematics

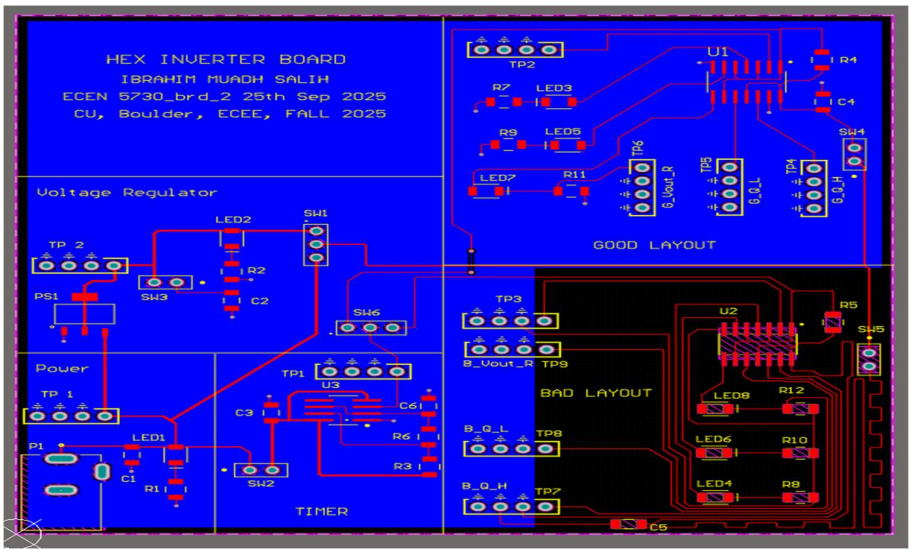

Figure 6.1 - Layout in Altium for 555 Timer

The bottom right section (Bad layout) is black in to indicate that it has no bottom return plane. In that same section, all the returns are interconnected, and decoupling capacitor is far from IC. Whereas, On the top right (Good layout), it has continuous return plane on its bottom layer, and the decoupling capacitor is near the IC.

7) Before & After Assembling

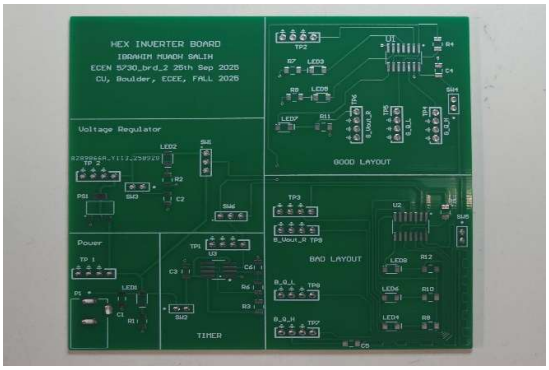

Figure 6.2 - Before assembling

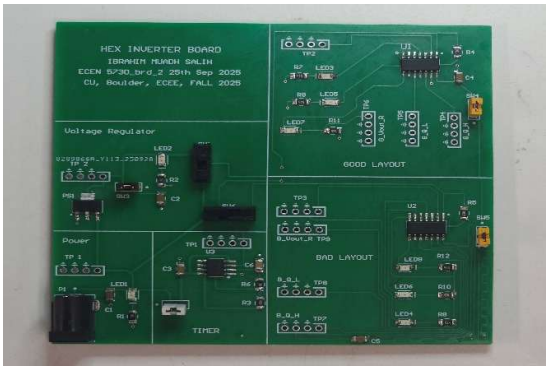

Figure 6.3 After assembling

Figure 6.4 – Working of the Board

8) What it means to work

1. When the power is on, indicator LEDs (5V and 3.3V) should turn ON.
2. Board is powered with a 5 V AC to DC adapter which can be measured Test Point of Adapter and 3.3V of LDO at its Test Point.
3. When SW6 ON, the 555 timer outputs a square wave signal with a frequency and duty cycle of about 500Hz and 66% and rise time are around 80 ns. This can be measured at the respective test point.
4. SW6 drives Bad Layout on and off.
5. SW1 switches the 3.3v and 5V.
6. SW4 switches the power of Good Layout Hex.
7. SW5 drives the power of Bad Layout Hex
8. 3 LEDs of each inverter should work on both 3.3V and 5V power supply switched by mini slide switch
9. Quiet low, Quiet high and Triger signals can be measured for each inverter in respective Test points

9) After Bring-up:

There were no errors. The indicator LED of 5V, 3.3v supply, output LEDs turned ON, and all the test points can be measured.

10) What did not work and debugged

Everything worked well because good soldering practices were followed during assembly.

11) Scope Analysis

a) 5V (Yellow) and 3.3V (Green) rail measured at TP2 and TP1 respectively.

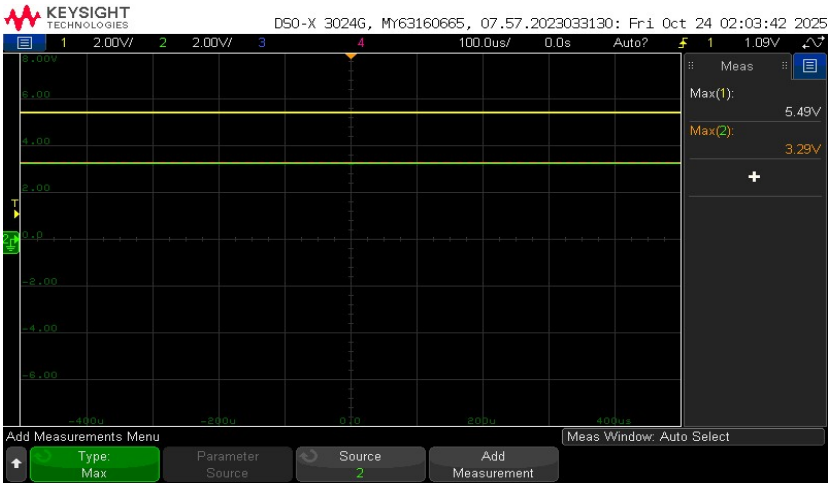

Figure 10.1 Power Rails (5V and 3.3V)

b) 555 output and triggers of hex inverters:

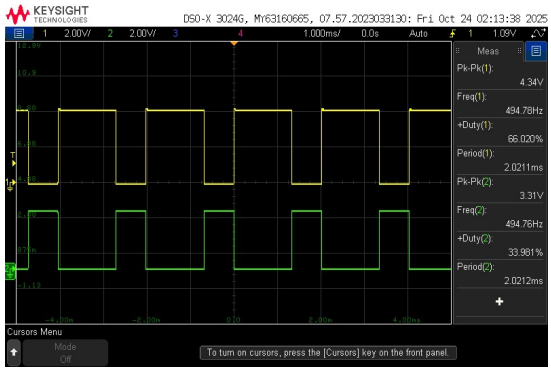

Figure 10.2 – Good Layout Hex and 555 Timer

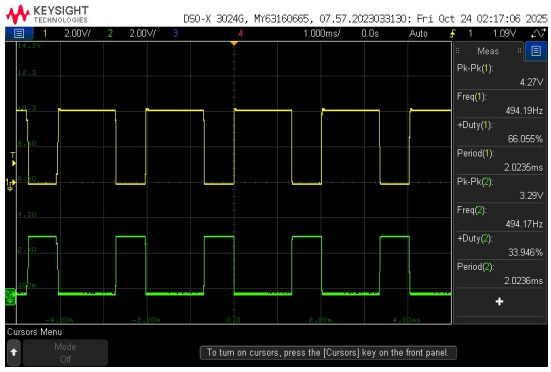

Figure 10.3 – Bad Layout Hex and 555 Timer

Description	555 Output	Good Layout	Bad Layout
Peak - Peak	4.34V	3.31V	3.29V
Period	2.021ms	2.021ms	2.023ms
Frequency	494.78Hz	494.76Hz	494.17Hz
Duty Cycle	66.02%	33.98%	33.94%

The outputs of the 555 timer and the hex inverter were measured for both the good and bad layouts, with the circuit powered at 3.3 V. The 555-timer output was connected to one NOT gate of each hex inverter, and the inverter output served as the trigger. In both layouts, the measured frequency, period, and peak-to-peak voltage (Vp-p) were nearly identical. This confirms that the circuit performed consistently in both cases, as expected.

c) LDO oscillations with/ without filter capacitor:

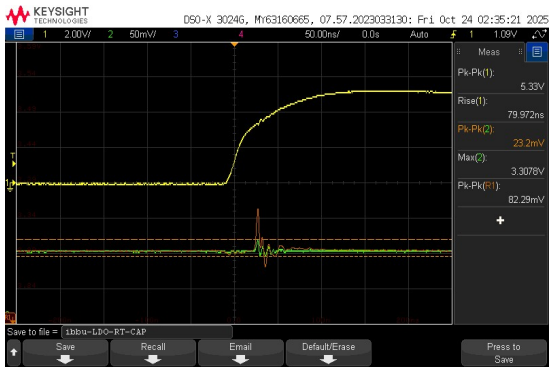

Figure 10.4 – Rise Edge during LDO oscillations

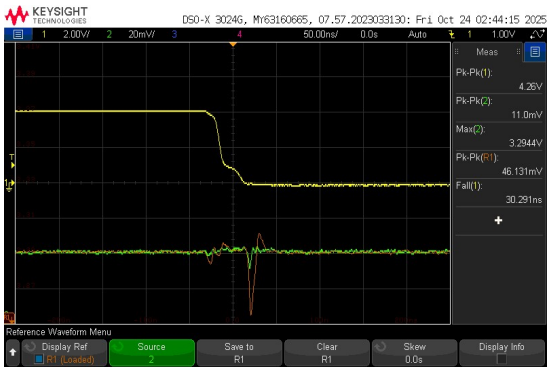

Figure 10.5 - Falling Edge during LDO oscillations

Figures 7.1 and 7.2 show the behaviour of the 3.3 V rail during the rising and falling edges of the 555-timer output.
Channel 1 (yellow) measures the 555 outputs, which exhibits a rise time of 79.97 ns and a fall time of 30.29 ns.
Channel 2 (green) captures the 3.3 V rail when capacitor C2 is connected through switch SW3, while the reference trace (orange) represents the 3.3 V rail without the capacitor in the LDO filter.
From the waveforms, it is observed that the 3.3 V rail experiences oscillations during both rising and falling edges of the 555 outputs. However, the configuration with the capacitor shows roughly half the noise amplitude compared to the case without the capacitor, confirming the capacitor's effectiveness in reducing LDO-induced oscillations.

d) Rising edge -Quiet low and Quiet High (3.3v):

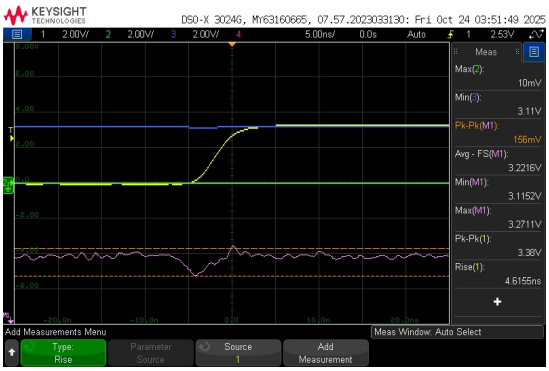

Figure10.6 – Good Layout (3.3v) Rise Time Rail Collapse

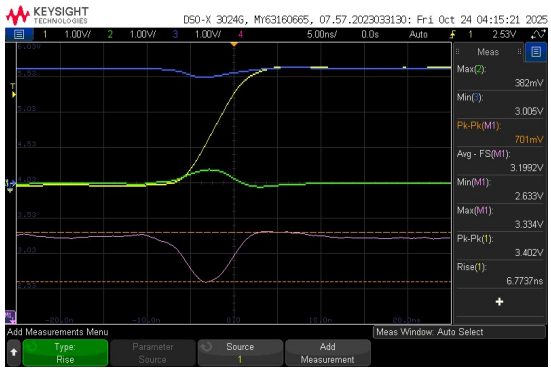

Figure10.7 – Bad Layout (3.3) Rise Time Rail Collapse

Metrics	Good Layout	Bad Layout
Rise Time	4.6155ns	6.773ns
Rail Voltage Min	3.115v	2.663v
Rail Voltage Max	3.271v	3.334v
Rail Compression Pk-Pk	156mv	701mv

e) Rising edge -Quiet low and Quiet High(5V):

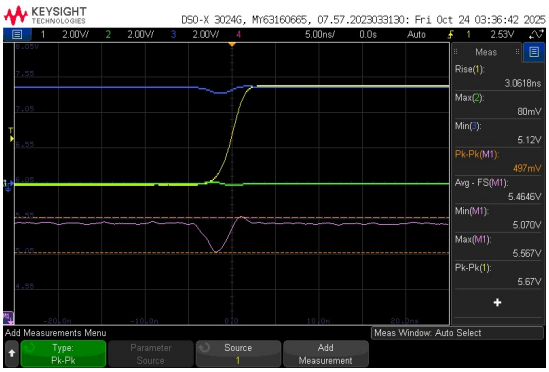

Figure 10.8 – Good Layout (5v) Rise Time Rail Collapse

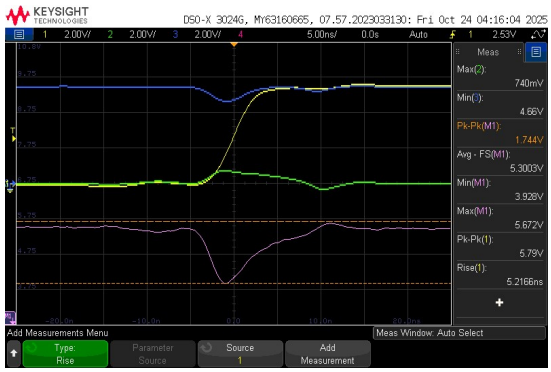

Figure10.9 – Bad Layout (5v) Rise Time Rail Collapse

Metrics	Good Layout	Bad Layout
Rise Time	3.061ns	5.216ns
Rail Voltage Min	5.070v	3.928v
Rail Voltage Max	5.567v	5.672v
Rail Compression Pk-Pk	497mV	1.744mV

In the figures, yellow represents the Hex inverter trigger output, green corresponds to the Quiet Low (QL) signal, and blue indicates the Quiet High (QH) signal. The pink waveform shows the rail-compression trace, which represents the effective supply voltage (VCC –GND) seen by the inverter.
During **steady-state (non-transient)** conditions, the pink trace remains stable near the nominal supply voltage, indicating minimal rail compression. However, during **signal transitions (rising or falling edges)**, a noticeable **voltage droop** occurs on the VCC rail and **ground bounce** occurs on the GND rail, momentarily compressing the power rail. This rail compression is more pronounced in the **bad layout**, where the combined effects of poor decoupling and longer trace inductance result in higher noise coupling.
Inference

The comparison between good and bad layouts of Rise Time at both 3.3 V and 5 V supplies clearly shows that the bad layout significantly degrades signal integrity and rail stability.

At 3.3 V:

- Rise time increases from 4.615 ns to 6.773 ns — approximately 1.47× slower.
- Rail voltage minimum drops from 3.115 V to 2.663 V, a 14.5% decrease, showing poor transient hold.
- Rail compression (noise) rises from 156 mV to 701 mV, nearly 4.5× higher, indicating severe power rail collapse.

At 5 V:

- Rise time increases from 3.061 ns to 5.216 ns, about 1.7× slower.
- Rail voltage minimum decreases from 5.070 V to 3.928 V, a 22.5% reduction in voltage stability.
- Rail compression grows from 497 mV to 1.744 V, around 3.5× higher, signifying strong noise coupling into the power rail.

Overall Observation:
Across both voltage levels, the bad layout shows 1.5–1.7× slower edge transitions and 3–5× higher rail compression, confirming that poor PCB layout design leads to greater rail disturbance, slower switching, and degraded signal integrity.

f) Falling edge -Quiet low and Quiet High (3.3v):

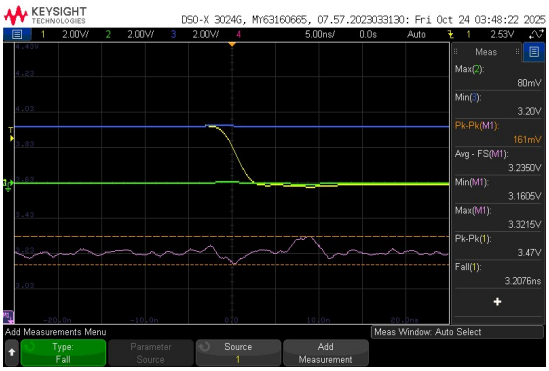

Figure 10.10 - Good Layout (3.3v) Fall Time Rail Collapse

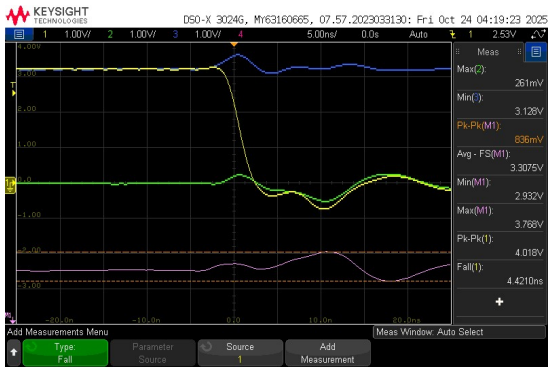

Figure 10.11 - Bad Layout (3.3v) Fall Time Rail Collapse

Metrics	Good Layout	Bad Layout
Fall Time	3.207ns	4.421ns
Rail Voltage Min	3.160v	2.932v
Rail Voltage Max	3.321	3.766v
Rail Compression Pk-Pk	161mV	836mV

g) Falling edge -Quiet low and Quiet High (5V):

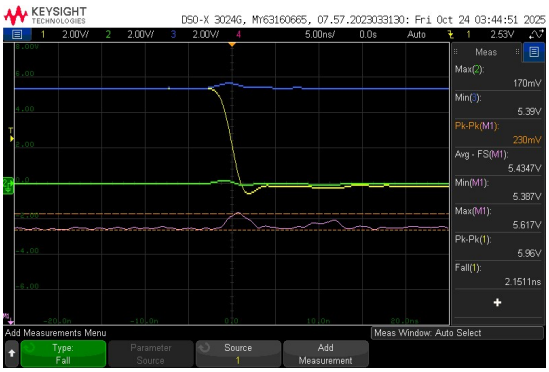

Figure 10.12 - Good Layout (5v) Fall Time Rail Collapse

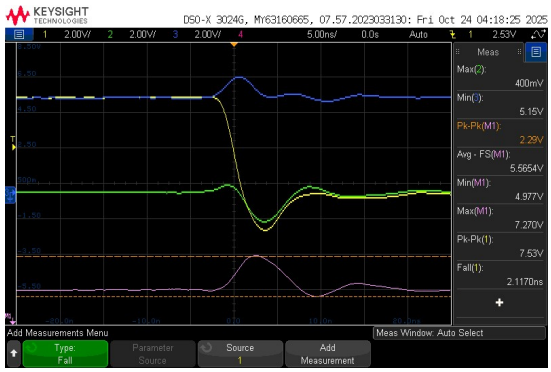

Figure 10.13 - Good Layout (5v) Fall Time Rail Collapse

Metrics	Good Layout	Bad Layout
Fall Time	2.151ns	2.117ns
Rail Voltage Min	5.387v	4.977v
Rail Voltage Max	5.617v	7.270v
Rail Compression Pk-Pk	230mV	2.29mV

In the figures, yellow represents the Hex inverter trigger output, green corresponds to the Quiet Low (QL) signal, and blue indicates the Quiet High (QH) signal. The pink waveform shows the rail-compression trace, which represents the effective supply voltage (VCC-GND) seen by the inverter.

During steady-state (non-transient) conditions, the pink trace remains stable near the nominal supply voltage, indicating minimal rail compression. However, during falling transitions, a noticeable voltage droop occurs on the VCC rail and ground bounce occurs on the GND rail, momentarily compressing the power rail. This compression is more pronounced in the bad layout, where poor decoupling and higher trace inductance lead to greater noise coupling.

Inference

The comparison between good and bad layouts during falling edges at both 3.3 V and 5 V clearly shows that the bad layout significantly worsens rail compression and transient response.

At 3.3 V:

- Fall time increases from 3.207 ns to 4.421 ns, approximately 1.38× slower.
- Rail voltage minimum drops from 3.160 V to 2.932 V, showing 7.2% lower voltage stability.
- Rail compression increases from 161 mV to 836 mV, roughly 5.2× higher, indicating strong rail collapse.

At 5 V:

- Fall time remains nearly similar (2.151 ns vs 2.117 ns), showing minimal timing difference.
- Rail voltage minimum decreases from 5.387 V to 4.977 V, a 7.6% reduction in voltage hold.
- Rail compression rises sharply from 230 mV to 2.29 V, about 9.96× higher, showing significant rail disturbance.

Overall Observation

Across both voltage levels, the bad layout exhibits slower or unstable transitions and 5–10× higher rail compression, confirming that poor PCB layout design severely impacts power rail stability, increases noise coupling, and degrades signal integrity.

12) Thevenin's Resistance

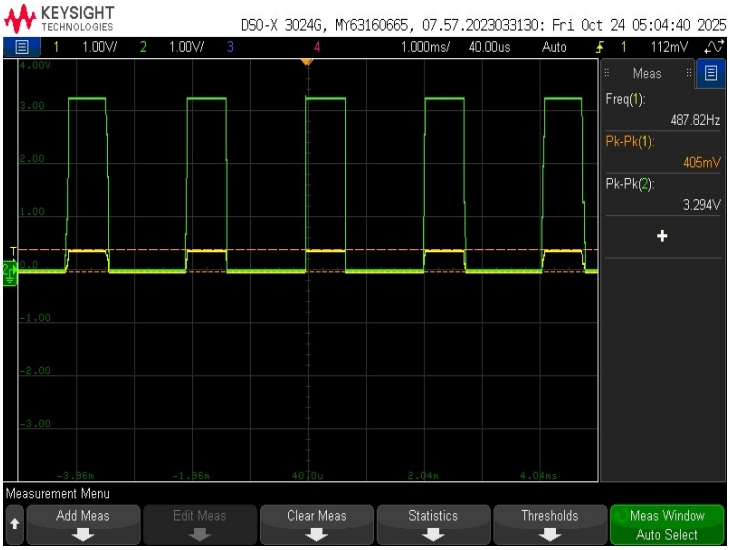

Figure 10 .14 – Voltage across 47 ohms Resistor

Channel 2 (Green) shows the Hex Output measured at TP 2 without load and Channel 1 (Yellow) shows Voltage across the 47-Ohms resistor when LED is powered On.

Parameter	Description	Value
V_{th}	The inverter output voltage without any connected load is measured as	V_{th} = 3.3
V_{load}	When the LED is connected, the inverter output voltage drops	V_{load} = 2.405
I_{Load}	The Current through the resistor	$\frac{Resistor\ Voltage}{Resistor\ Value} = \frac{0.40}{47} = 8.5mA$

$$\boldsymbol{Rth = \frac{Vth - Vload}{Iload} = \frac{3.3 - 2.40}{0.0085} = 105.75\ ohms}$$

13) Best Design Practices Followed

1. The number of unique components was minimized to simplify the Bill of Materials and make the assembly and procurement processes easy.

2. Decoupling capacitors were positioned as close as possible to the IC power pins (except in the bad layout section) to minimize loop inductance and enhance power rail stability.

3. All test points were clearly labelled to help accurate signal probing and reduce to avoid mistakes or errors during testing and measurements.

4. Indicator LEDs and isolation switches were incorporated to enable quick identification of circuit status and to simplify troubleshooting during testing.

5. Power traces were routed with a 20-mil width to ensure adequate current-carrying capability, while 6 mil widths were used for signal traces to achieve high routing density within fabrication constraints.

6. 1206-sized passive components were chosen to allow for easy manual soldering and rework, ensuring reliability during prototyping and testing.

14) Improvements to be Implemented

1. Extra hands-on practice is needed to make the connections cleaner and more reliable.

2. Shorter paths in the layout can be used later to keep signals steady and reduce disturbance.

3. Must try reducing the cross under.

15) Conclusion:

Through this board study, it was observed that placing decoupling capacitors close to IC power pins and maintaining a continuous return plane beneath signal traces significantly improve power rail and signal performance. Additionally, the board helped in practically measuring and studying the on-chip power rail noise, giving a better understanding of how the design performs in real conditions. Thevenin's Internal resistance was also calculated and was around 105.75 ohms.