# Board 1 - 555 Timer in Astable Configuration
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# Table of Contents


**1) Objective:** **1**
**2) Bill of Materials:** **1**
Table 2.0 Explains all the Bill of Materials **1**
**3) Plan of Record:** **2**
**4) Napkin Sketch:** **2**
Figure 4.1 - This sketch shows the overall plan **2**
**5) Hardware Setup & Schematic:** **3**
Figure 5.0 - Schematics 3
Figure 5.1 - Layout in Altium for 555 Timer 3
Figure 5.2 - Before assembling 4
Figure 5.3 After assembling 4
**6) Calculations:** **4**
**7) Scope Analysis** **5**
**a) Load Time vs Without Load:** **5**
Figure 7.1 - 555 Timer with Load 6
Figure 7.2 - 555 Timer without Load 6
**8) Switching Noise on Power Rail:** **6**
a) Rise and Fall Time without Load: 6
Figure 8.1 - Rise time without load 6
Figure 8.2 - Fall time without load 6
b) Rise and Fall Time With Load 7
Figure 8.3 - Rise time with Load 7
Figure 8.4 - Fall time with Load 7
**9) Current Calculations across 1K and 300 Ohm Resistor** **7**
FIgure 9.1 - Voltage across 1K 7
Figure 9.2 - Voltage across 300 ohms 7
**10) Best Design Practices Followed** 8
**11) Improvements to be Implemented** 8
**12) Conclusion:** **8**

## 1) Objective:

The objective of this work is to gain hands-on experience with the full PCB design and development process, including part selection, circuit drafting, layout preparation, manual soldering, and testing. A 555 timer configured in astable mode is used to drive multiple LEDs, and its behavior is studied by measuring output resistance, observing supply line variations during switching, and verifying the overall performance of the board.

## 2) Bill of Materials:

| Comment | Designator | Footprint | LibRef | Quantity |
|---|---|---|---|---|
| | | | | |
| 22uF | C1, C2 | 1206_Passive_Capacitor | C_22uF_1206 | 2 |
| 1uF | C3 | 1206_Passive_Capacitor | C_1uF_1206 | 1 |
| Red | LED1, LED2, LED3, LED4, LED5 | LED_1206 | LED_RED_1206 | 5 |
| Power Jack | P1 | Power_Jack | P_Power Jack | 1 |
| 1k | R1, R2, R3, R7 | 1206_Passive_Resitor | R_1K_1206 | 4 |
| 300 Ohm | R4 | 1206_Passive_Resitor | R_300Ohm_1206 | 1 |
| 100Ohm | R5 | 1206_Passive_Resitor | R_100Ohm_1206 | 1 |
| 10k | R6 | 1206_Passive_Resitor | R_10KOhm_1206 | 1 |
| SW_2Pin_100mil_Switch | SW1, SW2 | 2Pin-Header-Conn | SW_2Pin_100mil_Switch | 2 |
| 10x Probe TP | TP1, TP2, TP3, TP 5V | TP10x_Probe | TP_10x_Probe | 4 |
| NE555DR | U1 | NE555DR | U_555 | 1 |

Table 2.0 Explains all the Bill of Materials

## 3) Plan of Record:

- The board should include:
- An input jack to connect a 5 V DC adapter derived from main power.
- An astable 555 timer configured to deliver a 5 V peak-to-peak square waveform at roughly 500 Hz with a 60% duty cycle.
- Four LEDs arranged in parallel, driven directly by the 555 timer signal.
- A four different current limiting resistors for the LEDs, with values of 47 Ω, 300 Ω, 1 kΩ, and 10 kΩ.
- A main LED that indicates the supply voltage.
- Dedicated Test points to check the 5 V line, the timer's output, and the voltage across a 1 kΩ resistor for current evaluation.
- Removable header pins placed in series with the supply line and the timer output for troubleshooting and signal isolation.

## 4) Napkin Sketch:

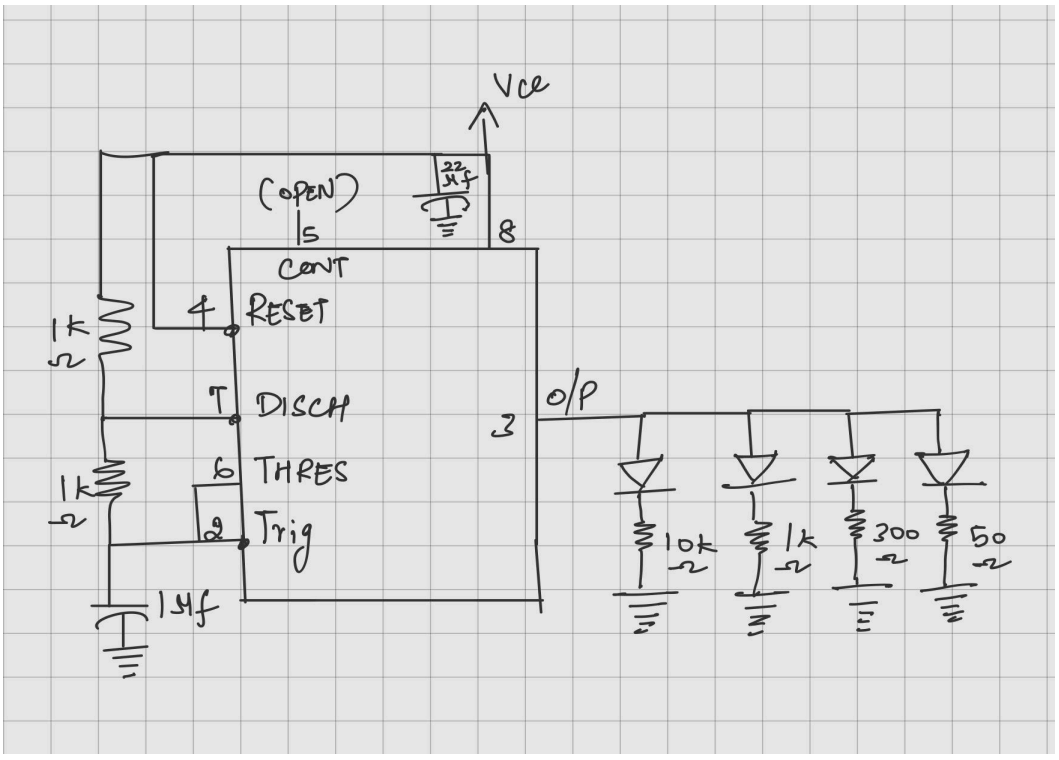


Figure 4.1 - This sketch shows the overall plan

A 5 V supply feeds a 555 timer in astable mode. RA = 1 kΩ, RB = 1 kΩ, C = 1 µF with pins 2 & 6 tied. RESET is tied high. A small decoupling capacitor is placed from VCC to GND. The OUT (pin 3) node drives several LEDs, each with a different series resistor.

# 5) Hardware Setup & Schematic:

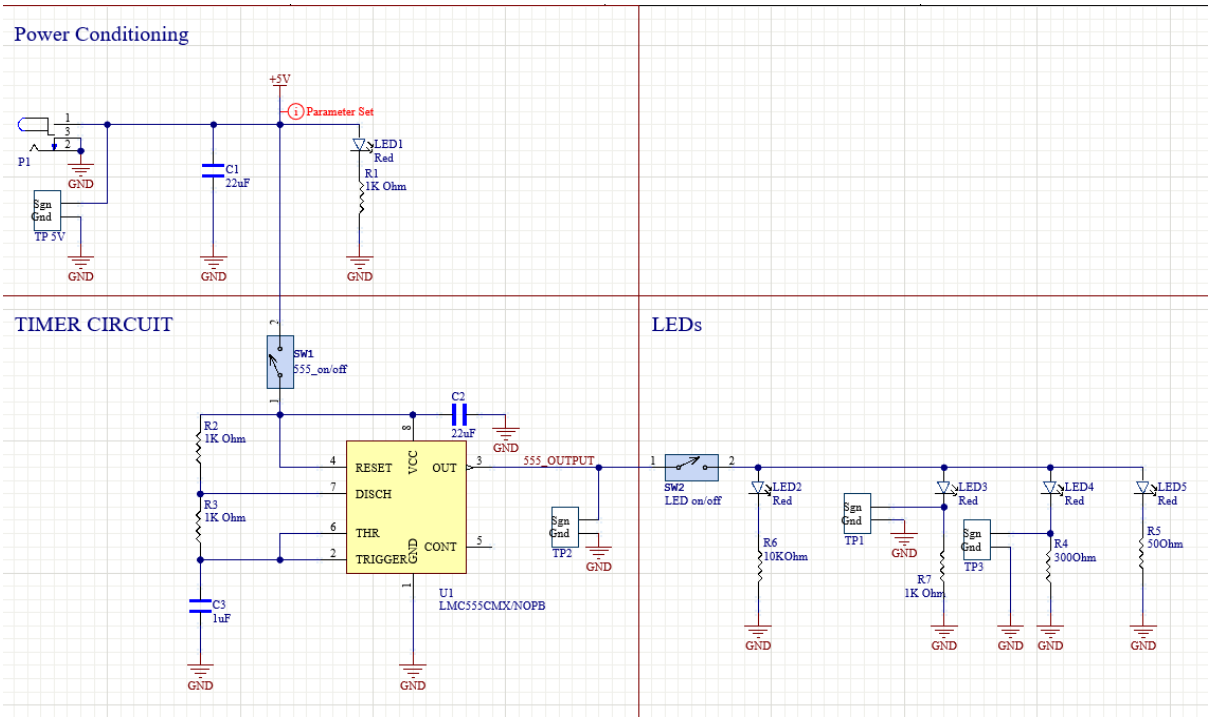


***Figure 5.0 - Schematics***

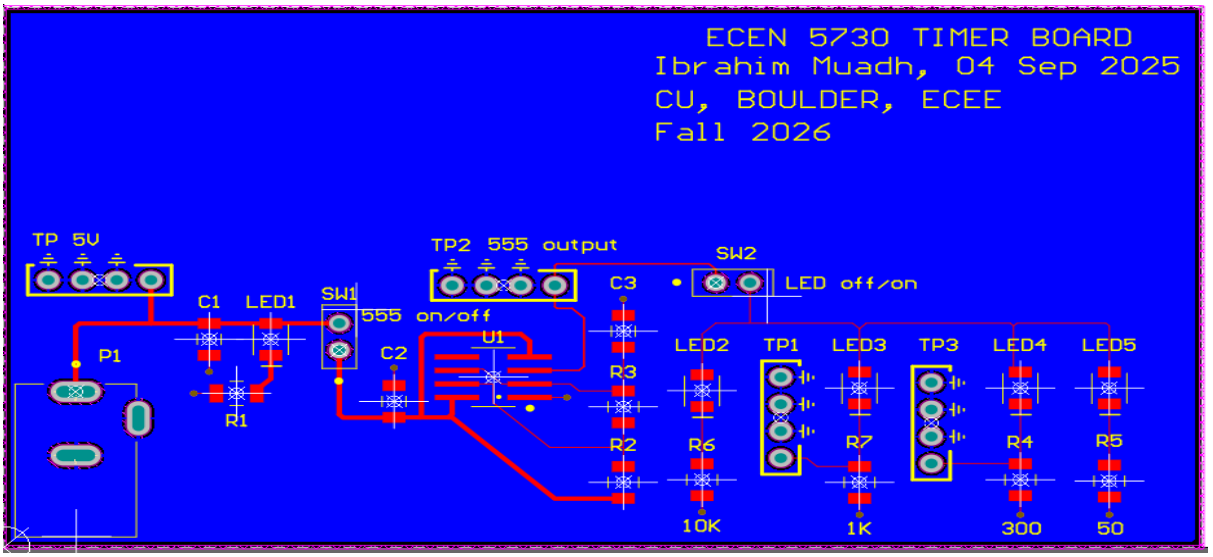


*Figure 5.1 - Layout in Altium for 555 Timer*

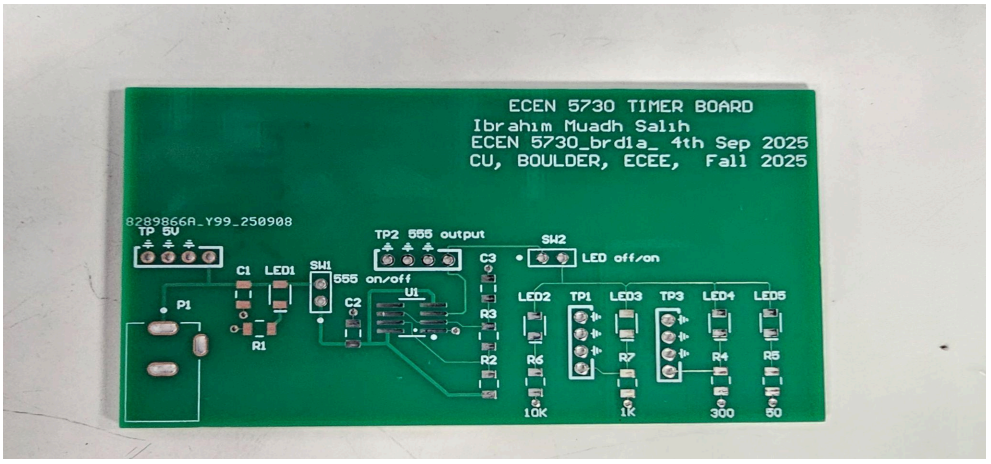


*Figure 5.2 - Before assembling*

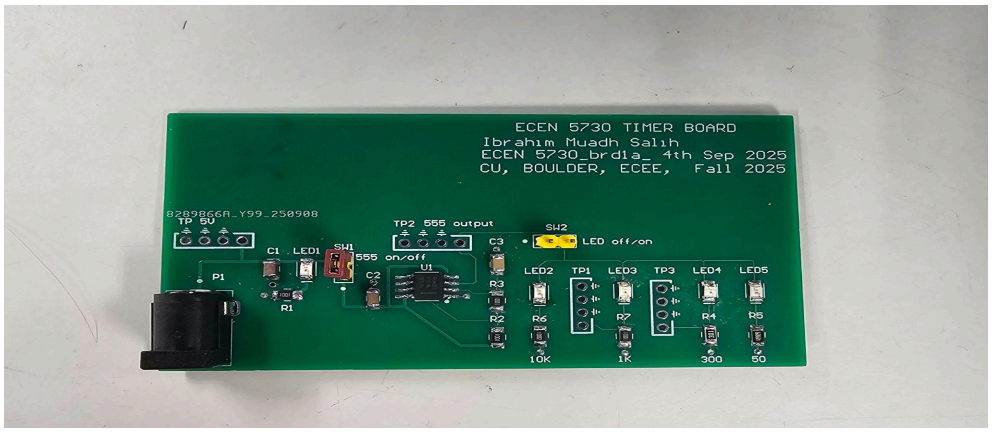


*Figure 5.3 After assembling*

## 6) Calculations:

The duty cycle will be determined using the formula provided in the datasheet to establish expected values

$$T_{ON} = 0.693\,(R_1 + R_2)C$$

$$= 0.693\ (1000 + 1000)(1\text{x}10^{-6})$$

$$\mathbf{= 1.386\ ms}$$

$$T_{OFF} = 0.693\,(R_2)C$$

$= 0.693(1000)(1x10^{-6})$

**= 0.693 ms**

$$Total\,Time(T) = T_{ON} + T_{OFF}$$

$$Duty\ Cycle = \frac{R_1 + R_2}{R_1 + 2R_2}$$

$$= \frac{2000}{3000}\ x\ 100$$

**= 66.66%**

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)C}$$

$$= \frac{1}{3000\ x10^{-6}}$$

**= 480 Hz**

# 7) Scope Analysis

## a) Load Time vs Without Load:

**Calculating Thevenin's Resistance**

- No load attached, the measured peak is **4.82 V**.
- The measured peak drops to **3.9 V** with the load.
- The Resistance = 1 / [(1/47) + (1/300) + (1/1000) + (1/10000)] 38.895 ohms ($R_{LOAD}$)
- Rth = 38.89 (4.82 - 3.9 / 3.9) = 9.17 Ohms

Hence the 555 Timer has an internal resistance of **9.17 Ohms,** so 555 timer voltage is not an ideal voltage source.

| Description | With Load | Without Load |
|---|---|---|
| Peak - Peak | 3.90V | 4.82V |
| Period | 1.9568ms | 1.9840ms |
| Frequency | 511.03Hz | 504.03Hz |
| Duty Cycle | 65.93% | 65.814% |

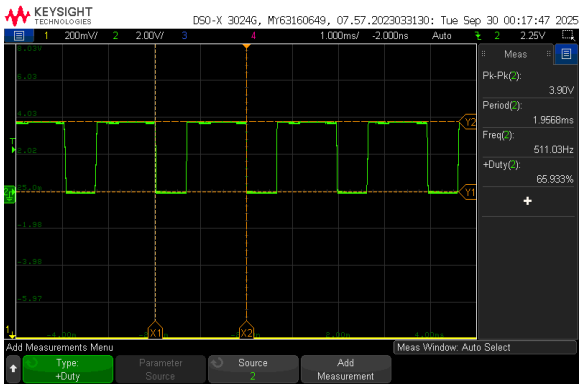


Figure 7.1 - 555 Timer with Load

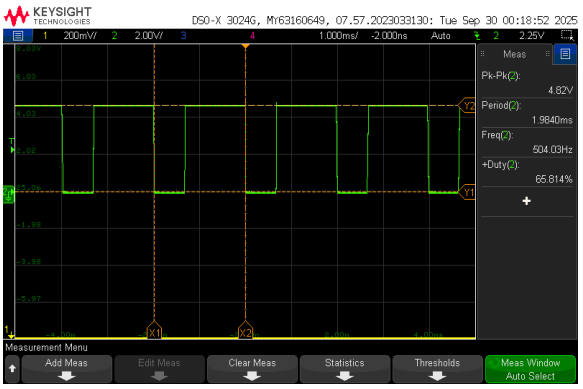


Figure 7.2 - 555 Timer without Load

# 8) Switching Noise on Power Rail:

## a) Rise and Fall Time without Load:

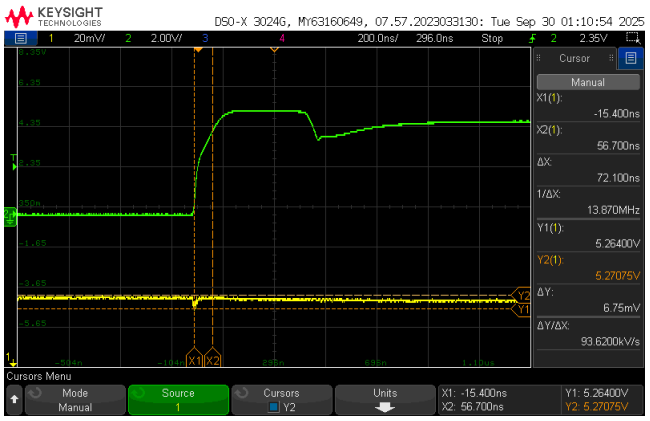


Figure 8.1 - Rise time without load

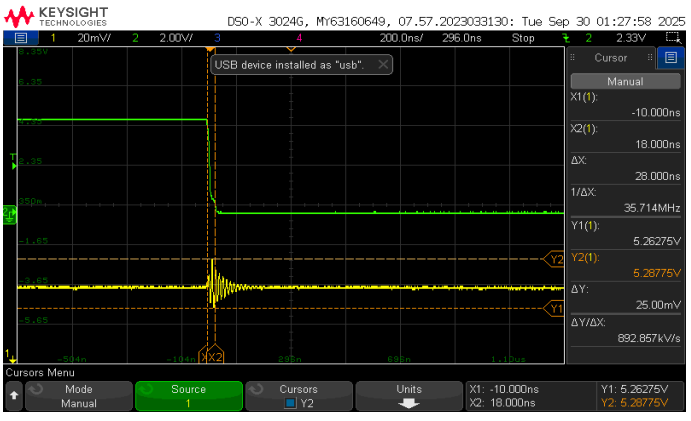


Figure 8.2 - Fall time without load

From the captured waveforms, the **rise transition** (Figure 8.1) occurs in about **72.100 ns**, and the **fall transition** (Figure 8.2) takes around **28 ns**. During these transitions, small disturbances are visible on the 5 V rail roughly **6.75 mV** for the rising edge and **25 mV** for the falling edge. These disturbances appear because of the voltage drop across the power rail's loop inductance when current changes rapidly (dI/dt) as the 555 switches.

## b) Rise and Fall Time With Load

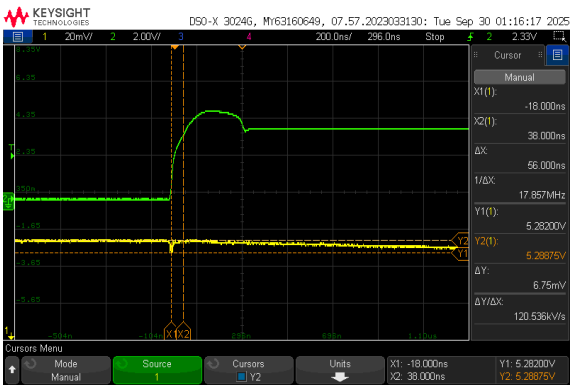


Figure 8.3 - Rise time with Load

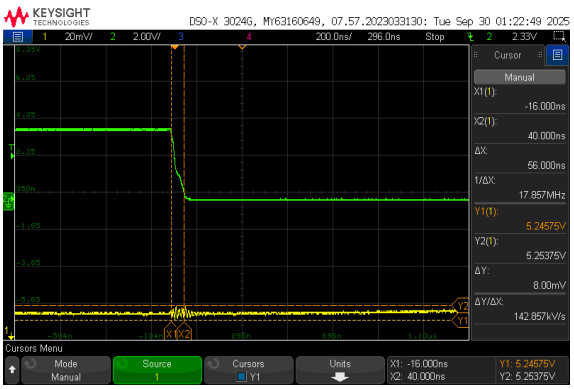


Figure 8.4 - Fall time with Load

In the captured traces, the **rising edge** measures around **56 ns**, showing a disturbance of about **6.75 mV** on the supply path. The **falling edge** measures close to **56 ns**, with a disturbance level of roughly **8 mV**. This is mainly because a decoupling capacitor placed near the 555 helps stabilize the supply, preventing any significant increase in noise.

# 9) Current Calculations across 1K and 300 Ohm Resistor

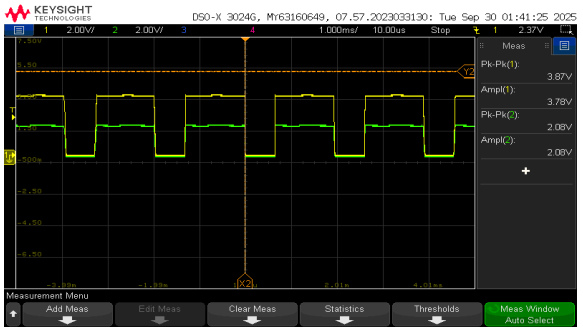


FIgure 9.1 - Voltage across 1K

Voltage across 1K ohms Resistor = 2.08V
Current = 2.08/1000 = 2.08mA

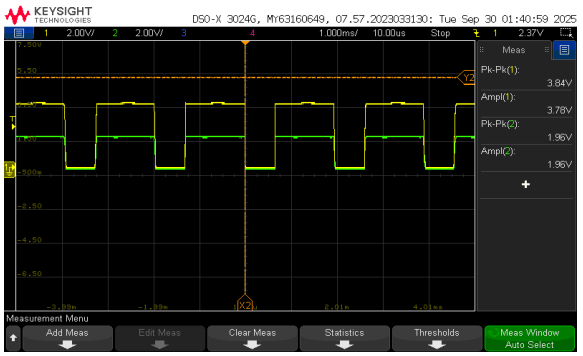


Figure 9.2 - Voltage across 300 ohms

Voltage across 300 ohms Resistor = 1.96V
Current = 1.96/300 = 6.53mA

In these captures, Channel 1 (yellow) shows the 555 output waveform, while Channel 2 (green) indicates the voltage drop across the external resistor. The current through the resistor is obtained using Ohm's law.

For a **1 kΩ resistor**, the measured drop is **2.08 V**, which corresponds to **2.08 mA**.
For a **300 Ω resistor**, the drop is **1.96 V**, giving a current of **6.53 mA**.

## 10) Best Design Practices Followed

1. A **decoupling capacitor** was placed close to the 555 timer to suppress voltage fluctuations caused by the loop inductance of the supply line, reducing noise during fast switching.

2. **Clear labeling** was applied to test points and connections to avoid mistakes during measurement and make debugging easier.

3. **Indicator LEDs and isolation switches** were included to simplify testing, allowing faster identification of signals and easy separation of circuit sections when required.

4. A **continuous ground plane** was maintained in the layout to ensure a proper return path and minimize cross-talk, avoiding unwanted disturbances on the supply.

5. **Optimized trace widths** were used: wider tracks for power lines to handle higher current, and narrower tracks for signals to achieve higher routing density while keeping costs low

## 11) Improvements to be Implemented

1. Extra hands-on practice is needed to make the connections cleaner and more reliable.

2. Shorter paths in the layout can be used later to keep signals steady and reduce disturbance.

## 12) Conclusion:

The circuit built with the 555 timer performed as expected and met the intended goals. The output delivered the required waveform to drive LEDs, and the internal resistance was found to be around 9.5 Ω. Noise on the supply line remained small because of proper capacitor placement near the IC. The step-by-step design process, from circuit drafting to PCB assembly and testing, was successfully carried out. Overall, the project gave clear practical learning on design flow, good layout practice, and proper testing methods.