Ibraheem Moin

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EDUCATION

The University of Texas at Austin, Cockrell School of Engineering **May 2027**
Bachelor of Science, Electrical and Computer Engineering **GPA: 3.8 / 4.0**

- **Relevant Coursework:** Computer Architecture, Embedded Systems Design Lab, Digital System Design (HDL), Digital Logic Design, Data Structures & Algorithms, Software Design I/II (+Lab), Linear Systems and Signals

SKILLS

Programming Languages: C, C++, Python, Java, Verilog, Assembly (ARM)
Embedded Systems: RTOS (FreeRTOS), JTAG, I2C, SPI, UART, USB, GPIO, EXTI, DMA, Timers, PWM
Hardware & Tools: STM32 (F4), TI MSPM0/TM4C, Arduino, Basys3, Oscilloscopes, Git/GitHub, KiCad, Vivado

EXPERIENCE

Burns & McDonnell – Controls Engineering Intern | Houston, TX **May 2025 – August 2025**

- Validated and reviewed over 650 control loops and safety instrumented system (SIS) logic on P&IDs with cause-and-effect matrices, confirming setpoints and fail-safe actions to ensure alignment with design standards.
- Interpreted technical documentation (P&IDs/PFDs) to input and verify 6,000+ instruments data records in SmartPlant Instrumentation, supporting the development of accurate instrument index databases for large scale oil and gas projects.
- Evaluated field instrumentation and control devices by analyzing technical specifications, vendor datasheets, and process data to ensure compatibility with client and operational standards.

NexTek Services – Embedded Engineer Intern | Houston, TX **May 2024 – August 2024**

- Developed C/C++ firmware on Arduino Uno microcontroller, integrating an RFID reader, matrix keypad, LCD display, electronic solenoid lock and relay with error handling and user feedback to create a home security system.
- Implemented a state machine with non-blocking timing to cut input latency to less than 5 ms while managing user authentication, device control, and timeout handling with UART serial communication for debugging.
- Built a simple HMI using an I2C LCD to display status/error codes and prompts, plus a buzzer for alerts.

MZX Superior Car Wash – Operations Manager | Houston, TX **May 2021 – Present**

- Optimized chemical usage by adjusting relay timing, improving water mixing accuracy, and removing leaks which reduced chemical usage by 12%, leading to more cost-effective and eco-friendly operations.
- Managed inventory of chemicals, parts, and supplies by tracking usage and reorder points and coordinating vendor orders, which ensured stock availability during peak periods and minimized downtime.
- Performed maintenance and repairs on car wash/lube equipment ensuring business remained operational and efficient.

PROJECTS

RTOS Embedded Sensor & LED System – *C, FreeRTOS, STM32, I2C/SPI*

- Engineered an RTOS-based system on STM32 integrating a BMP280 and PIR, updating an I2C LCD, and driving WS2812B LEDs by synthesizing the 800 kHz waveform via the SPI peripheral to visualize temperature in real time.
- Implemented C drivers and FreeRTOS tasks for hardware with mutex synchronization and used EXTI interrupt to keep motion, display, and LED updates responsive.

Embedded Systems Pac-Man Game – *C, C++, ARM Cortex-M, PCB Design, ADC/DAC*

- Recreated Pac-Man on an ARM Cortex microcontroller with a custom PCB by interfacing an ST7735 LCD over SPI, buttons via GPIO, a slide potentiometer via ADC for input, and a speaker via DAC for audio.
- Developed game architecture in C++ using finite state machine design to manage game flow and implemented tile-based rendering engine with collision detection, path-finding algorithms, and graphic animations.

LC-3b Architecture Simulator – *C, Computer Architecture, RTL, Pipelining, Python*

- Built a cycle-accurate LC-3b CPU simulator in C with a microcoded control store and a 5-stage pipeline, implementing per-cycle latching, state transitions, while also designing RTL logic to handle exceptions and virtual memory.
- Engineered the pipeline control path with hazard detection, branch prediction and data forwarding to model instruction parallelism, and validated edge cases with Python scripts.

FPGA Stopwatch/Timer – *Verilog, RTL, FSM/HLSM, FPGA (Basys3), Vivado*

- Designed and built a Verilog stopwatch/timer on a Basys3 FPGA, featuring a BCD counter data path and an FSM controller with mode control, range checks, and reset/enable logic, driving a multiplexed 4-digit 7-segment display.
- Developed Verilog code involving clock division, input synchronization, delivered a bitstream within XDC constraints.