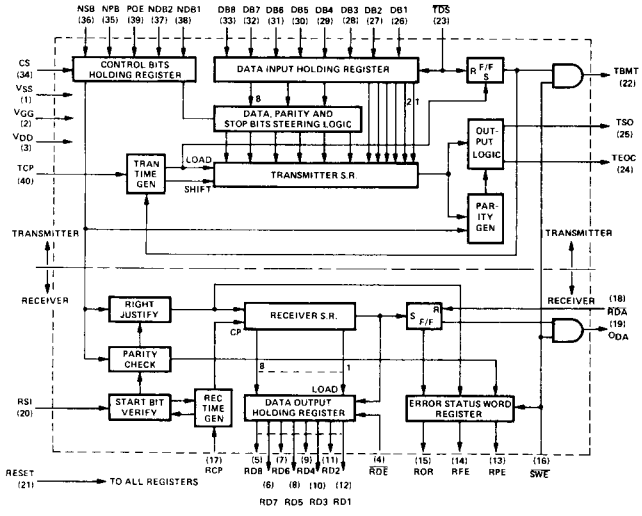
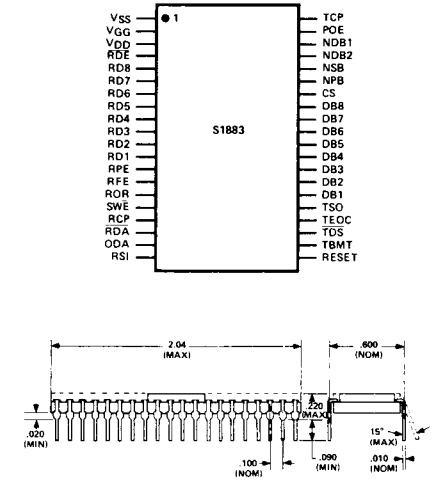


S1883 BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

(Available in Pkgs. 3M, 1T - see Sec. 1)

FEATURES

- 12.5 K Baud Data Rates
- 5-8 Bit Word Length
- Parity Generation/Checking Odd, Even, None
- Framing and Overflow Error Detection
- 1, 1.5, or 2 Stop Bits
- Double Buffered Input/Output
- Independent Transmit/Receive Rates
- Start and Stop Bits Generated and Detected
- Interchangeable with TMS6011, COM2017, TR1602, AY-5-1013
- Tri-State Outputs

FUNCTIONAL DESCRIPTION

The S1883 Universal Asynchronous Receiver Transmitter (UART) is a single chip MOS/LSI device that totally replaces the asynchronous parallel to serial and serial to parallel conversion logic required to interface a word parallel controller or data terminal to a bit serial communication network.

For asynchronous data transmission with a non-contiguous data bit stream, the UART automatically inserts a START bit preceding each character and under program control 1, 1.5, or 2 stop bits at the end of each character. To detect incoming characters in a noisy environment the UART employs a START bit detection network and allows errorless recovery of data with up to 42% distortion.

The UART will transmit or receive data characters of 5, 6, 7, or 8 bit length. Options allow the generation and checking of odd, even parity or no parity. The odd or even parity bit is automatically added to the character length for transmission.