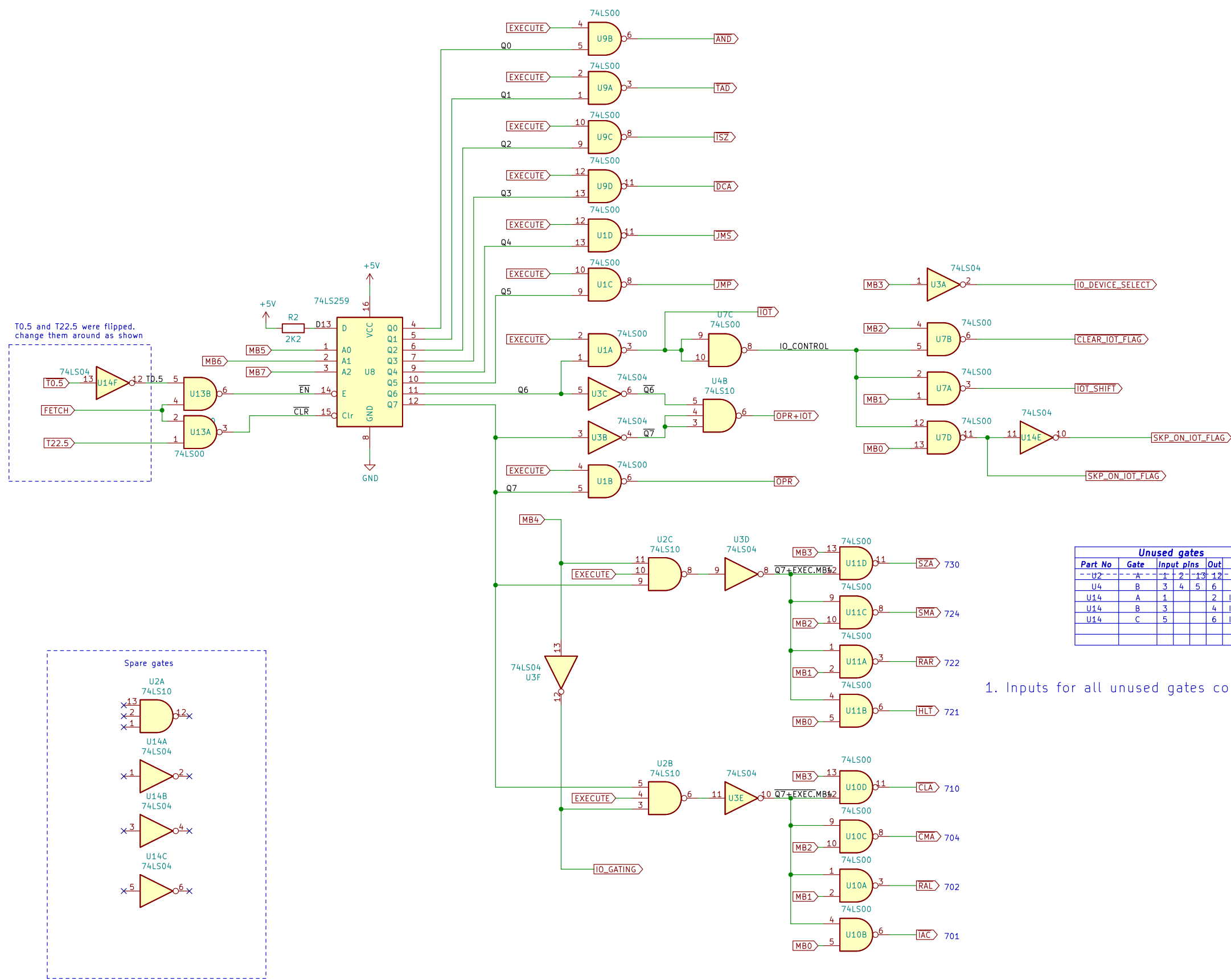
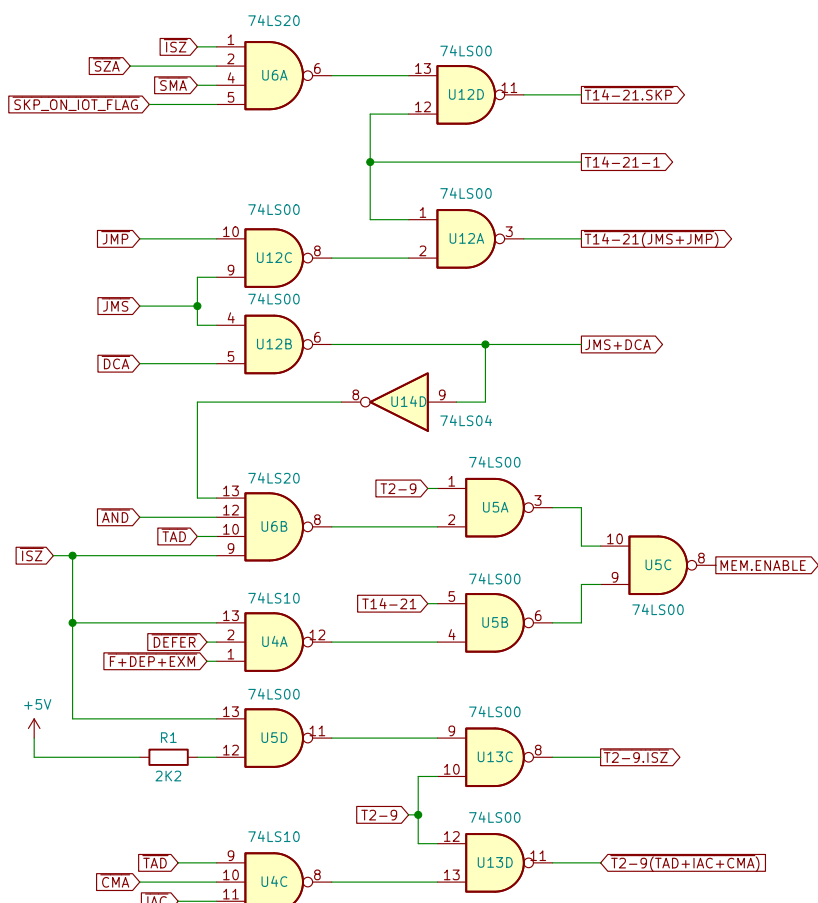
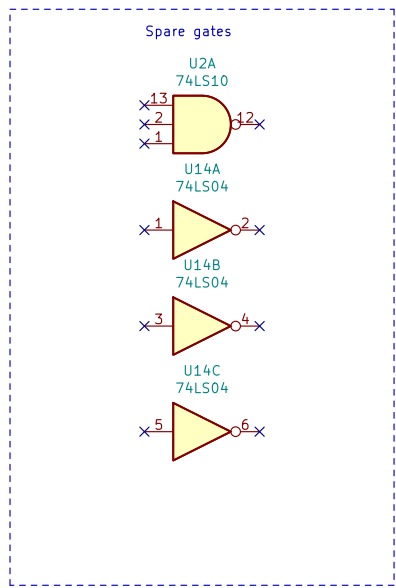


Every track and pad checked against the original artwork



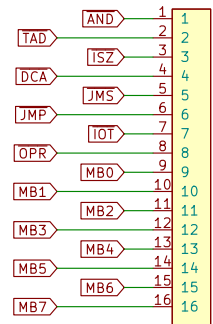
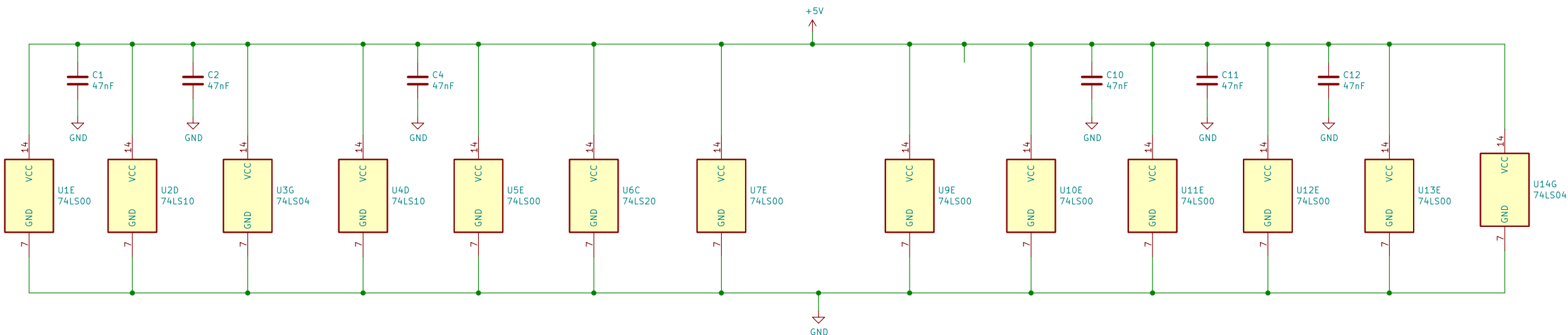
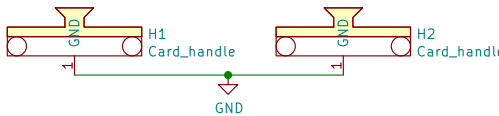
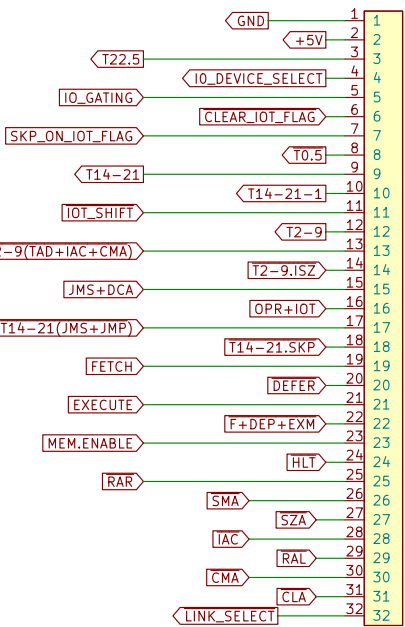
Unused gates				
Part No	Gate	Input pins	Out	
U2	A	1 2 12 12	NAND	
U4	B	3 4 5 6	NAND	
U14	A	1 2	INVERTER	
U14	B	3 4	INVERTER	
U14	C	5 6	INVERTER	

1. Inputs for all unused gates connected to GND



CONNECTION TABLE		
CARD EDGE 1		
Pin No	Function	Pin No
C1	47nF	1
C2	47nF	2
C4	47nF	3
C10	47nF	4
C11	47nF	5
C12	47nF	6
H1	Card_handle	7
H2	Card_handle	8
J1	32-way-pcb-edge-connector	9
J2	16-way-pcb-edge-connector	10
R1	2K2	11
R2	2K2	12
U1	74LS00	13
U2	74LS10	14
U3	74LS04	15
U4	74LS10	16
U5	74LS00	17
U6	74LS20	18
U7	74LS00	19
U8	74LS259	20
U9	74LS00	21
U10	74LS00	22
U11	74LS00	23
U12	74LS00	24
U13	74LS00	25
U14	74LS04	26

CONNECTION TABLE		
CARD EDGE 1		
Pin No	Function	Pin No
C1	47nF	1
C2	47nF	2
C4	47nF	3
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C12	47nF	6
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R1	2K2	11
R2	2K2	12
U1	74LS00	13
U2	74LS10	14
U3	74LS04	15
U4	74LS10	16
U5	74LS00	17
U6	74LS20	18
U7	74LS00	19
U8	74LS259	20
U9	74LS00	21
U10	74LS00	22
U11	74LS00	23
U12	74LS00	24
U13	74LS00	25
U14	74LS04	26



INSTRUCTION DECODER

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