Electronic Circuits I

Problems to be solved in Class

For the E2204 course

Spring 2021

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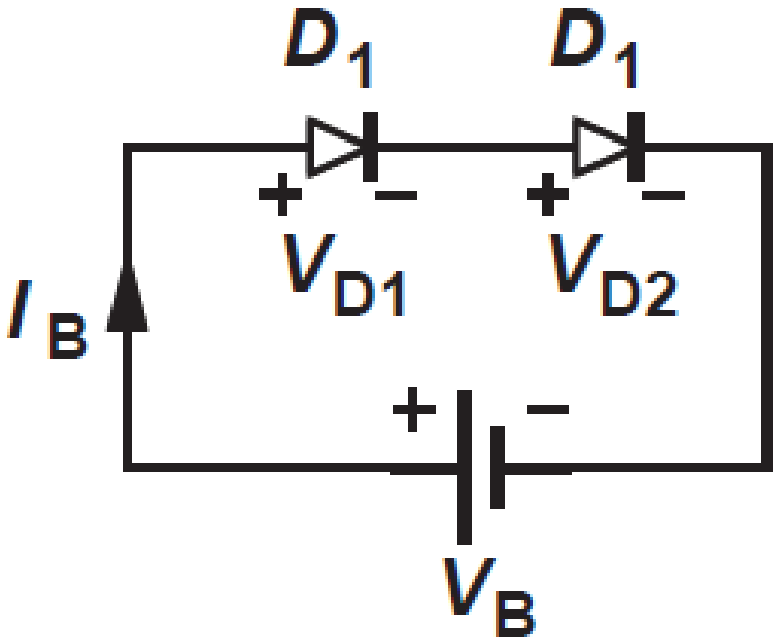
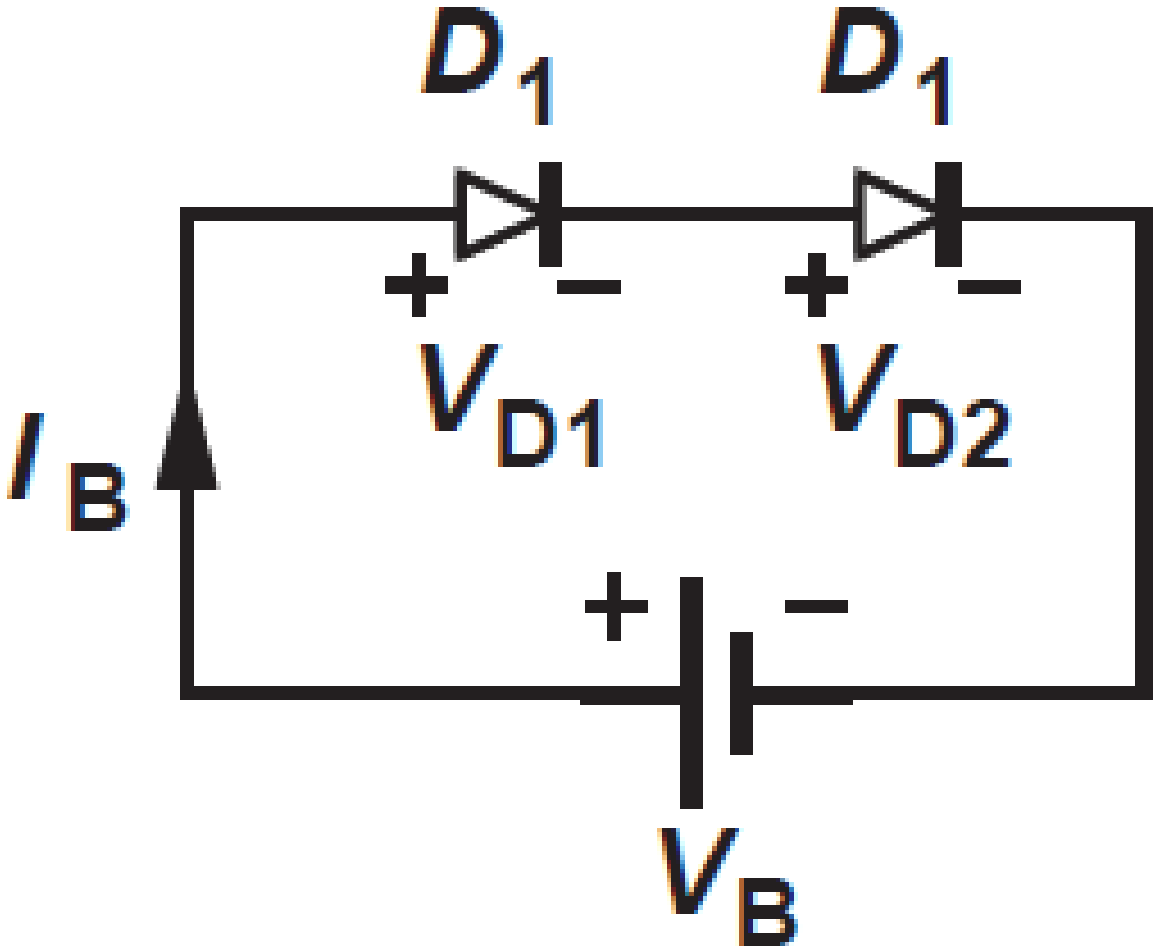
CHAPTER 2

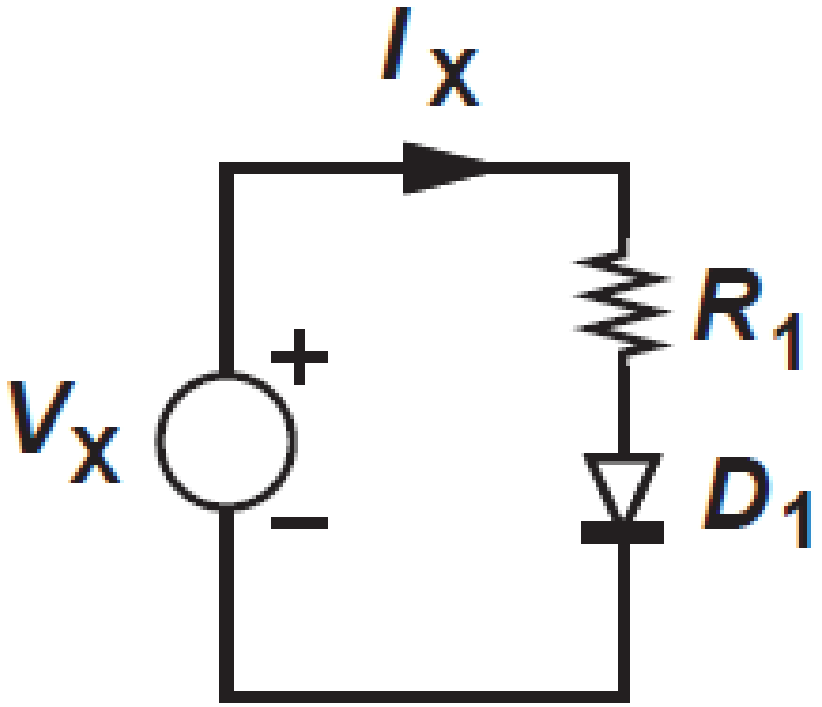
2.17. Figure 2.41 shows two diodes with reverse saturation currents of I_{S1} and I_{S2} placed in series. Calculate I_B, V_{D1}, and V_{D2} in terms of V_B, I_{S1}, and I_{S2}.



2.18. In the circuit of Problem 2.17, we wish to increase I_B by a factor of 10. What is the required change in V_B?



2.23. We have received the circuit shown in Fig. 2.43 and wish to determine R_1 and I_S. We note that $V_X = 1\,\text{V} \rightarrow I_X = 0.2\,\text{mA}$ and $V_X = 2\,\text{V} \rightarrow I_X = 0.5\,\text{mA}$. Calculate R_1 and I_S.



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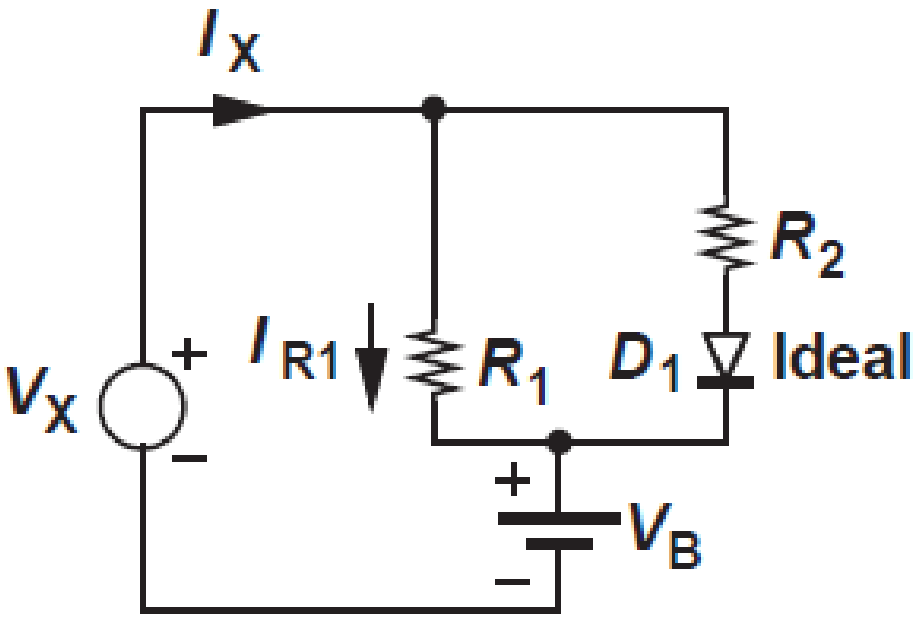
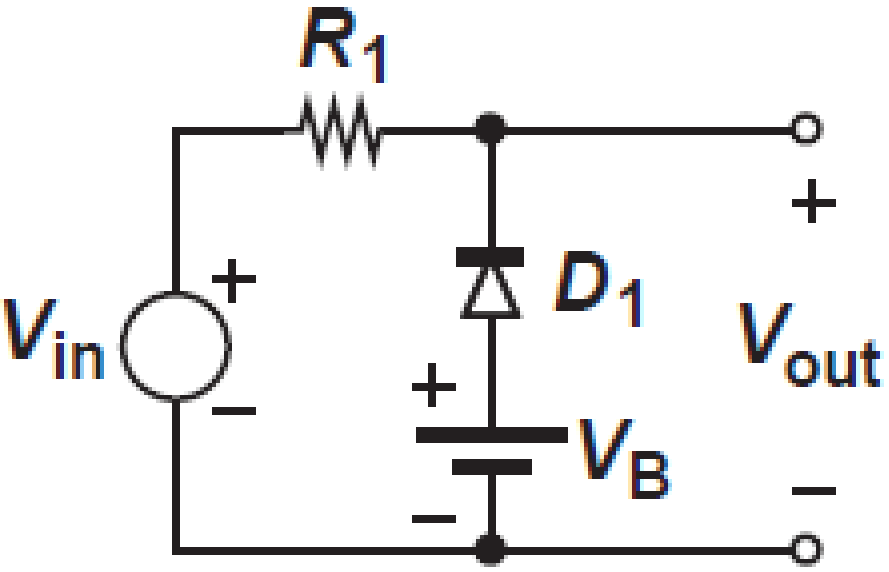
Chapter 3

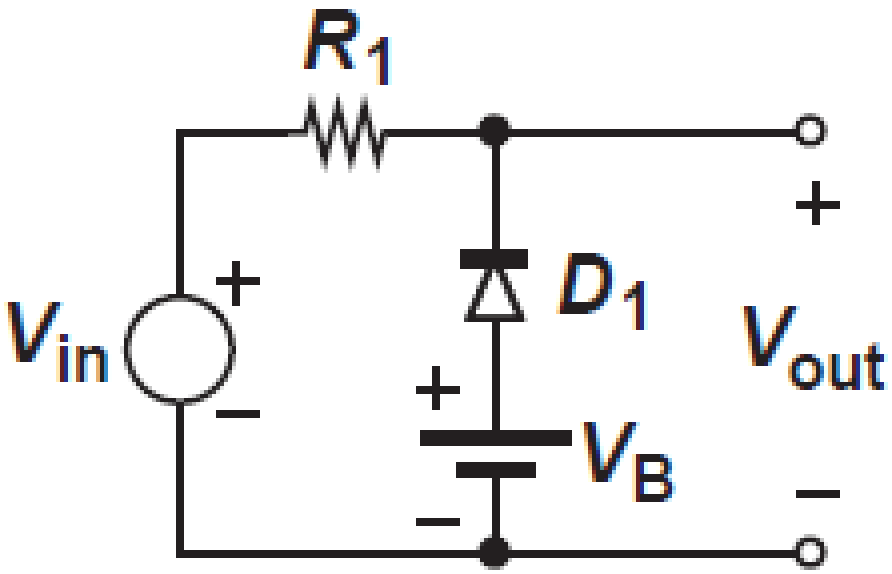
3.8. For the circuit depicted in Fig. 3.68, plot I_X and I_{R1} as a function of V_X for two cases: $V_B = -1$ V and $V_B = +1$ V.



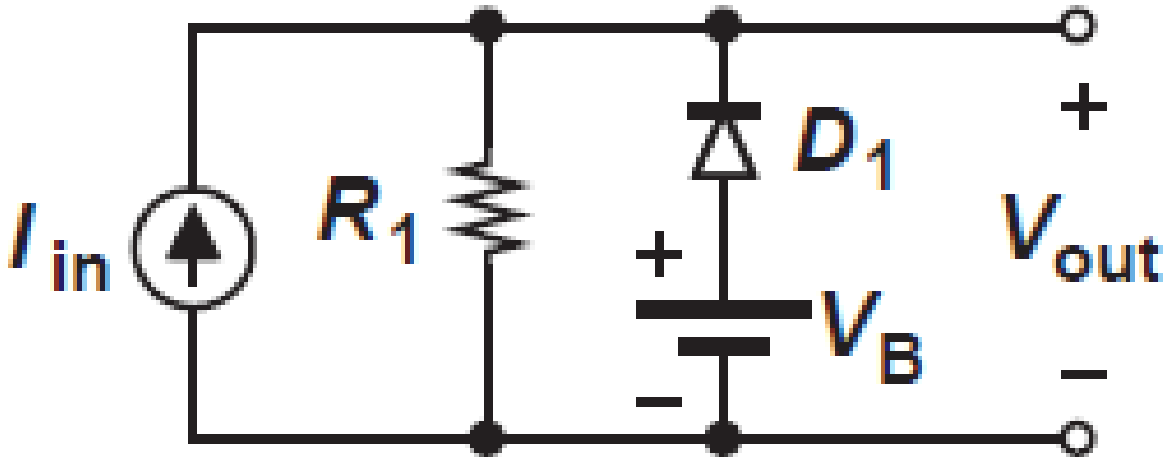
3.12. Plot the input/output characteristics of the circuits shown in Fig. 3.70 using an ideal model for the diodes.



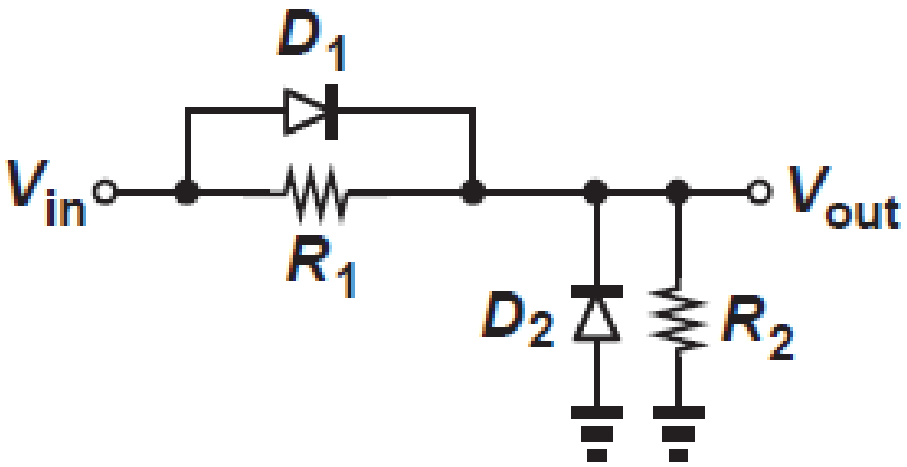
3.13. Repeat Problem 3.12 with a constant-voltage diode model.



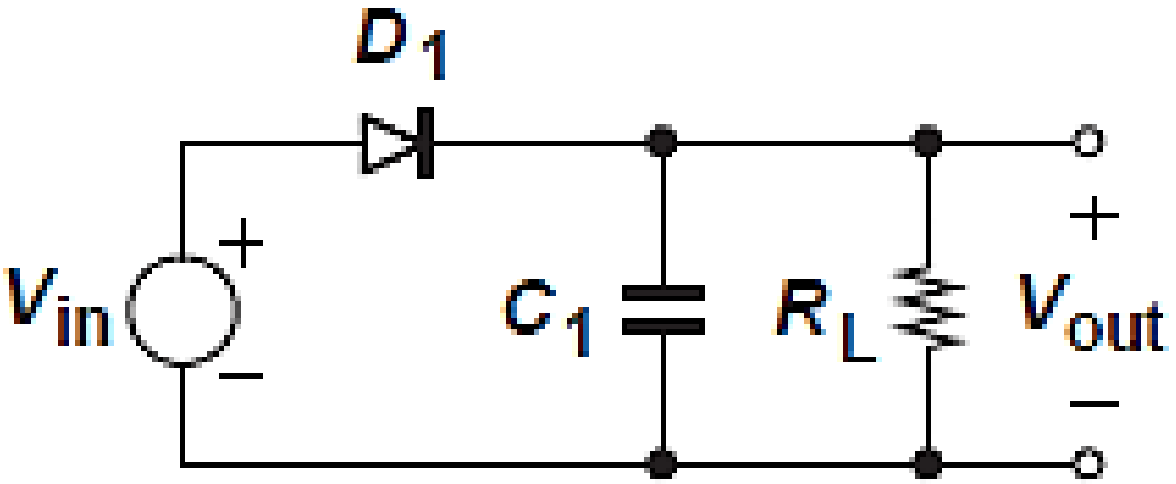
3.18. Plot V_{out} as a function of I_{in} for the circuits shown in Fig. 3.72. Assume a constant-voltage diode model.



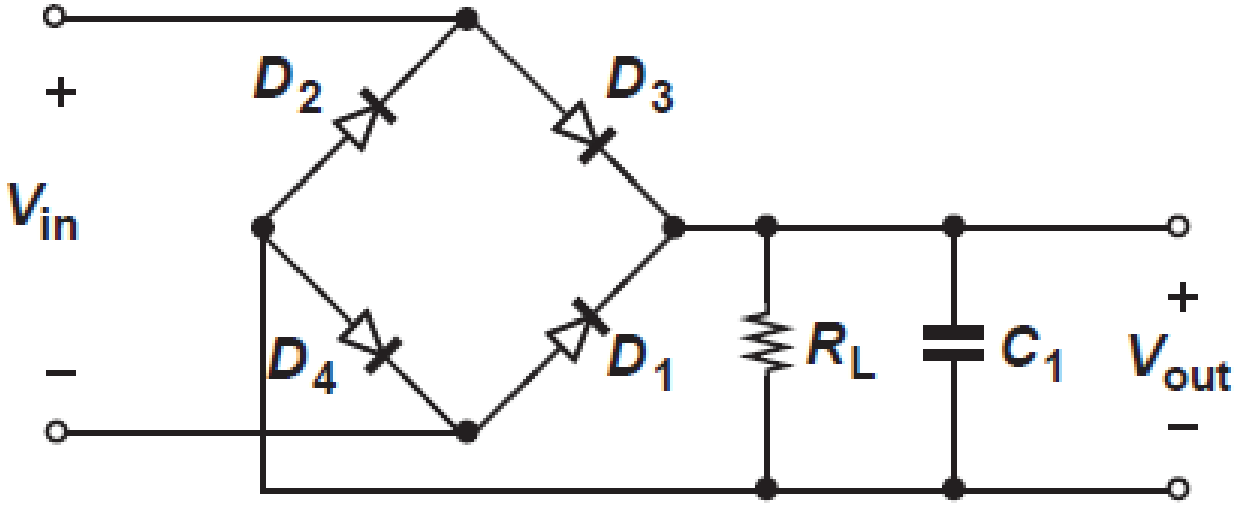
3.30. Plot the currents flowing through R_1 and D_1 as a function of V_{in} for the circuits of Fig. 3.77. Assume constant-voltage diode model.



3.37. A 3-V adaptor using a half-wave rectifier must supply a current of 0.5 A with a maximum ripple of 300 mV. For a frequency of 60 Hz, compute the minimum required smoothing capacitor.



3.41. A full-wave rectifier is driven by a sinusoidal input $V_{in} = V_0 \cos \omega t$, where $V_0 = 3$ V and $\omega = 2\pi(60\text{ Hz})$. Assuming $V_{D,on} = 800$ mV, determine the ripple amplitude with a 1000-μF smoothing capacitor and a load resistance of 30 Ω.



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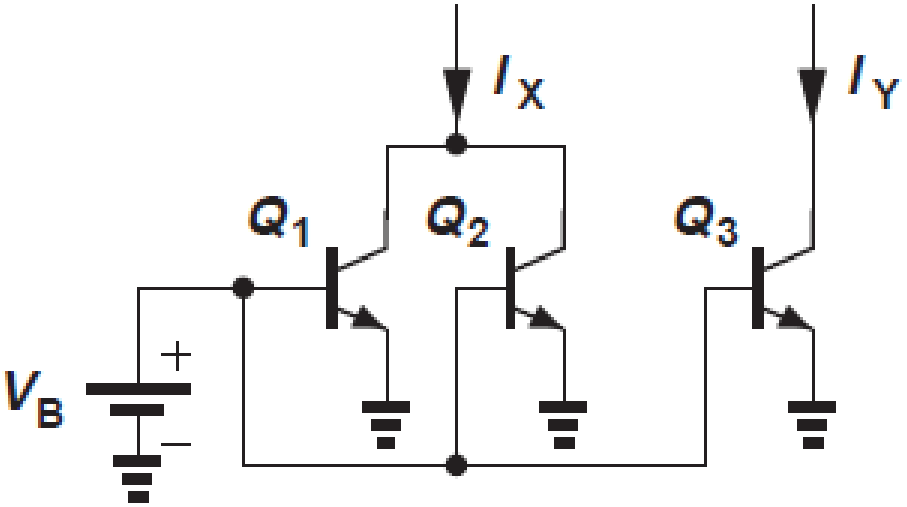
Chapter 4

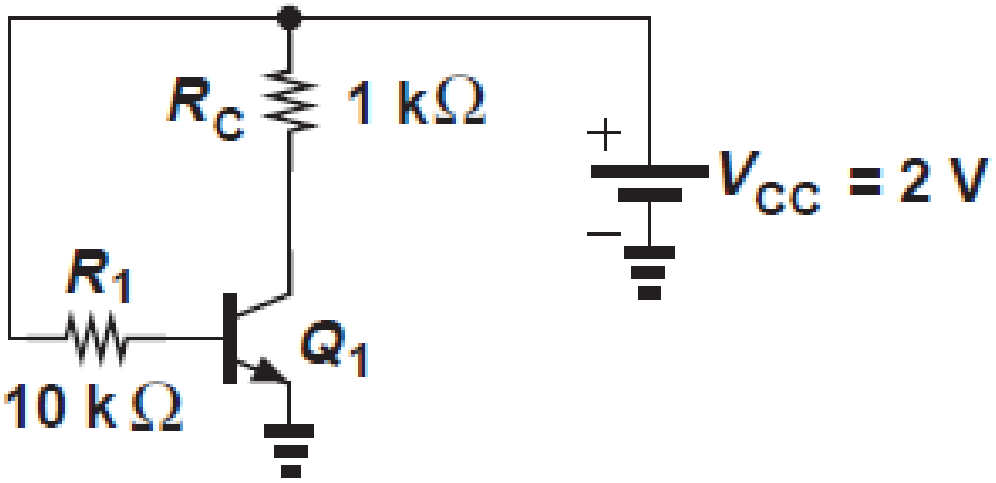
4.5. In the circuit of Fig. 4.48, $I_{S1} = I_{S2} = 3 \times 10^{-16}$ A.

(a) Calculate V_B such that $I_X = 1$ mA.

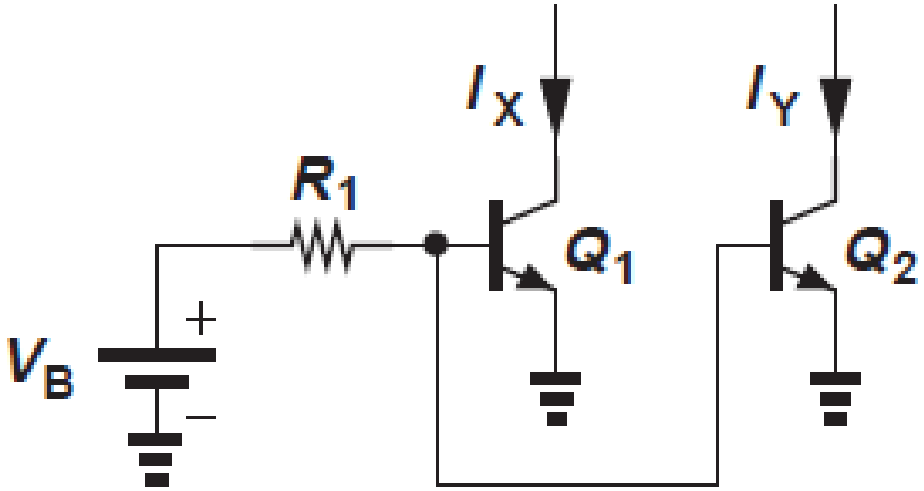
(b) With the value of V_B found in (a), choose I_{S3} such that $I_Y = 2.5$ mA.



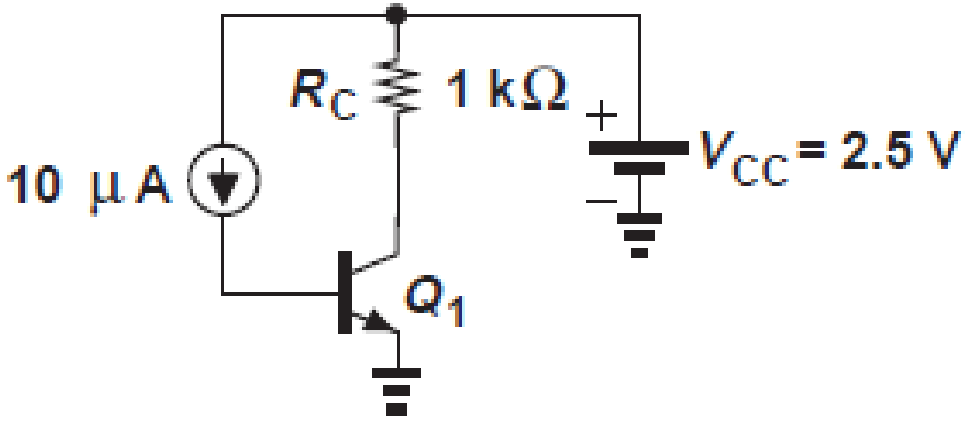
4.10. In the circuit of Fig. 4.52, determine the maximum value of V_{CC} that places Q_1 at the edge of saturation. Assume $I_S = 3 \times 10^{-16}$ A.



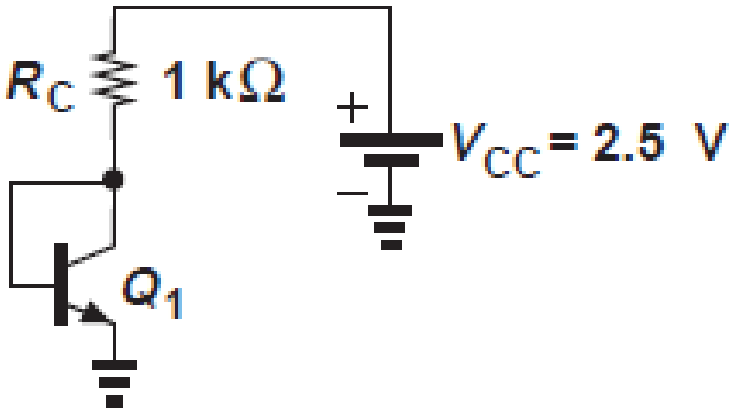
4.16. In the circuit depicted in Fig. 4.56, $I_{S1} = 2I_{S2} = 4 \times 10^{-16}$ A. If $\beta_1 = \beta_2 = 100$ and $R_1 = 5\,\text{k}\Omega$, compute V_B such that $I_X = 1\,\text{mA}$.



4.21. Determine the operating point and the small-signal model of Q_1 for each of the circuits shown in Fig. 4.57. Assume $I_S = 8 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

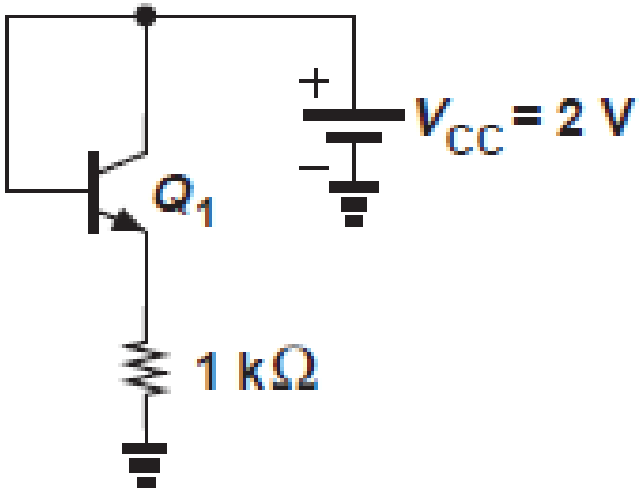


(b)

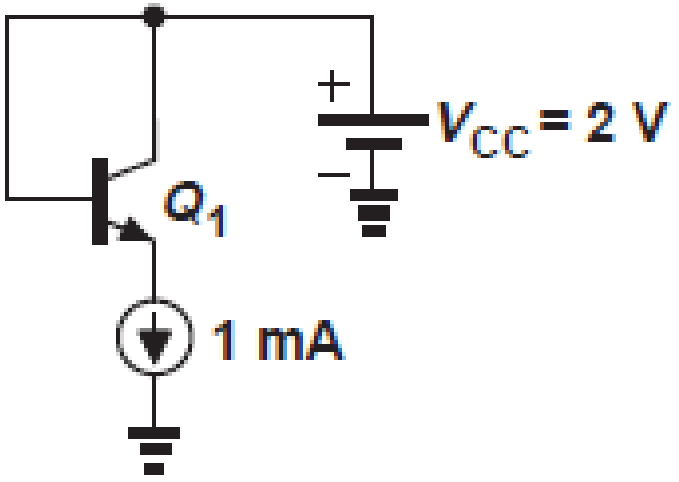


(c)

4.22. Determine the operating point and the small-signal model of Q_1 for each of the circuits shown in Fig. 4.58. Assume $I_S = 8 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

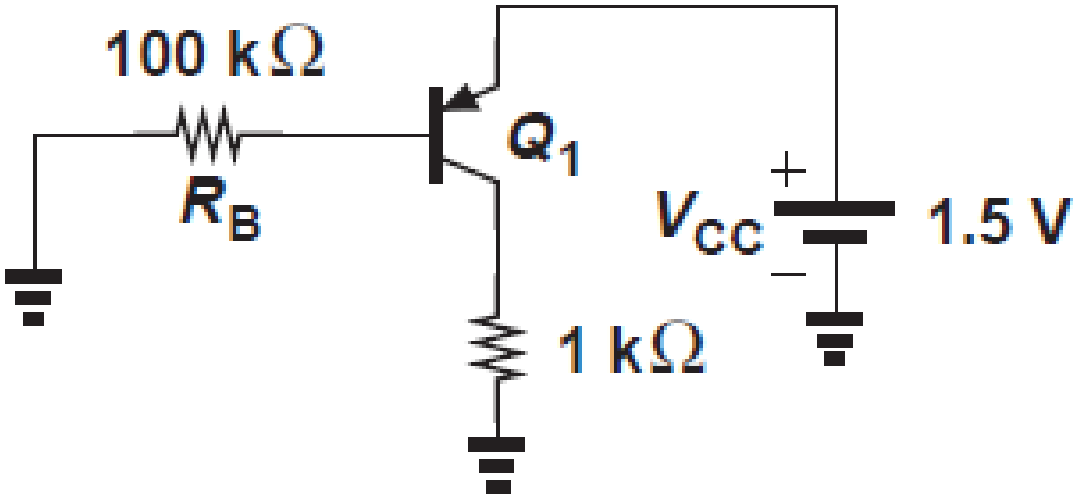


(b)

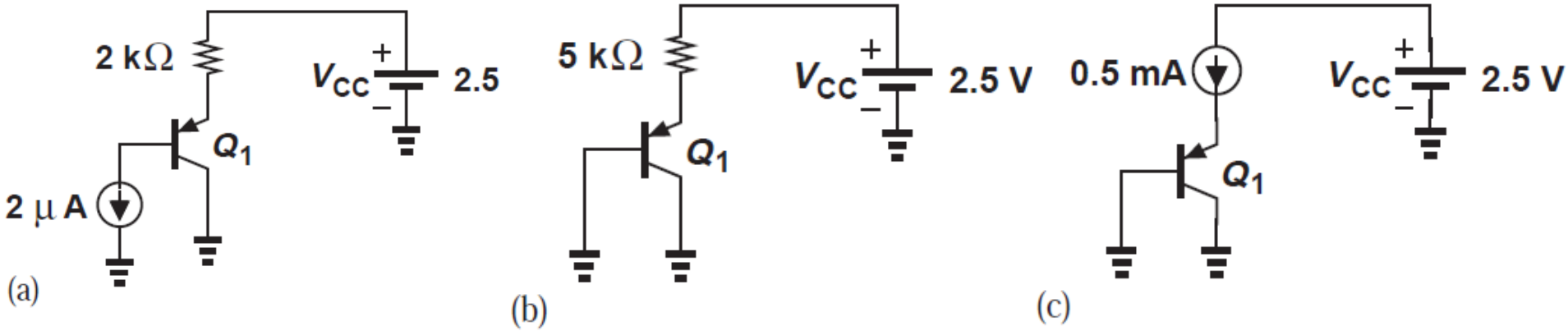


(c)

4.41. What is the value of β that places Q_1 at the edge of the active mode in Fig. 4.72? Assume $I_S = 8 \times 10^{-16}$ A.



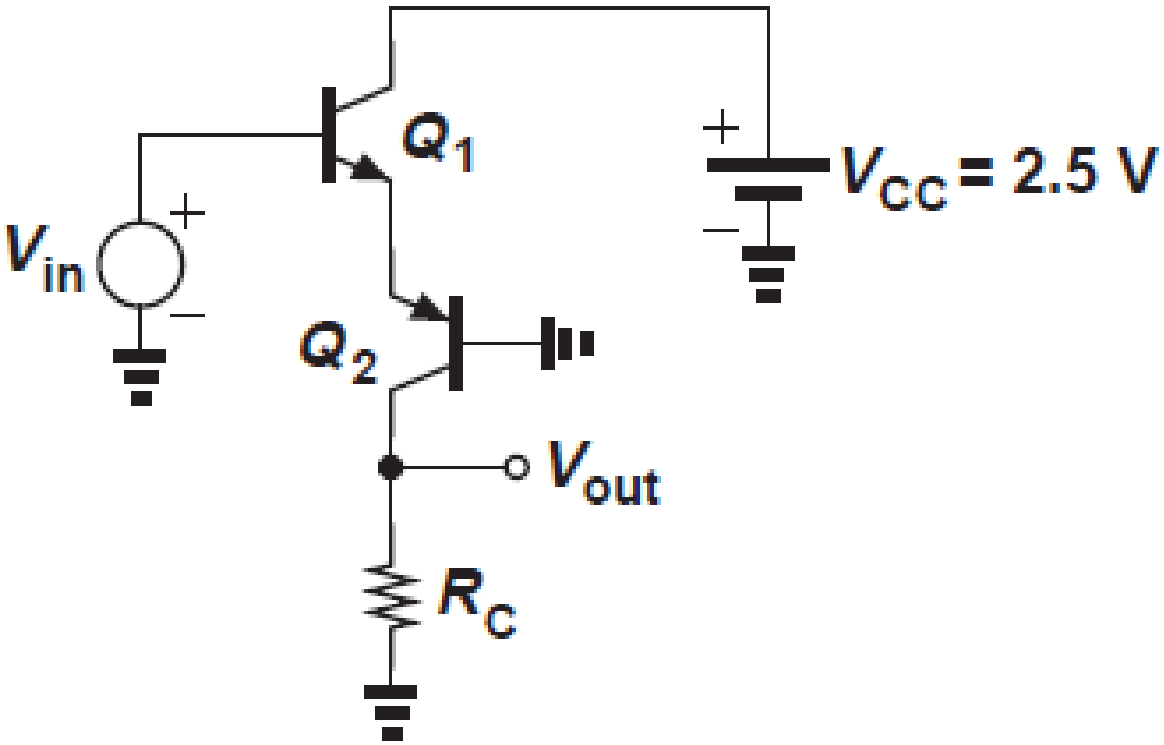
*4.45. Determine the operating point and the small-signal model of Q_1 for each of the circuits shown in Fig. 4.76. Assume $I_S = 3 \times 10^{-17}$ A, $\beta = 100$, and $V_A = \infty$.



**4.53. Consider the circuit shown in Fig. 4.81, where $I_{S1} = 3I_{S2} = 5 \times 10^{-16}$ A, $\beta_1 = 100$, $\beta_2 = 50$, $V_A = \infty$, and $R_C = 500\,\Omega$.

(a) We wish to forward-bias the collector-base junction of Q_2 by no more than 200 mV. What is the maximum allowable value of V_{in}?

(b) With the value found in (a), calculate the small-signal parameters of Q_1 and Q_2 and construct the equivalent circuit.



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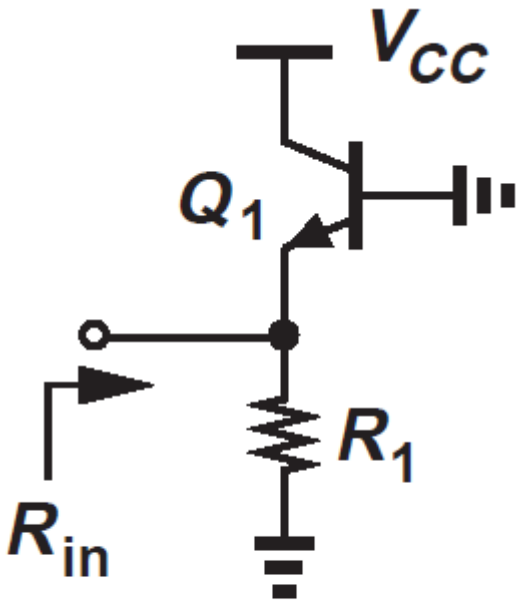
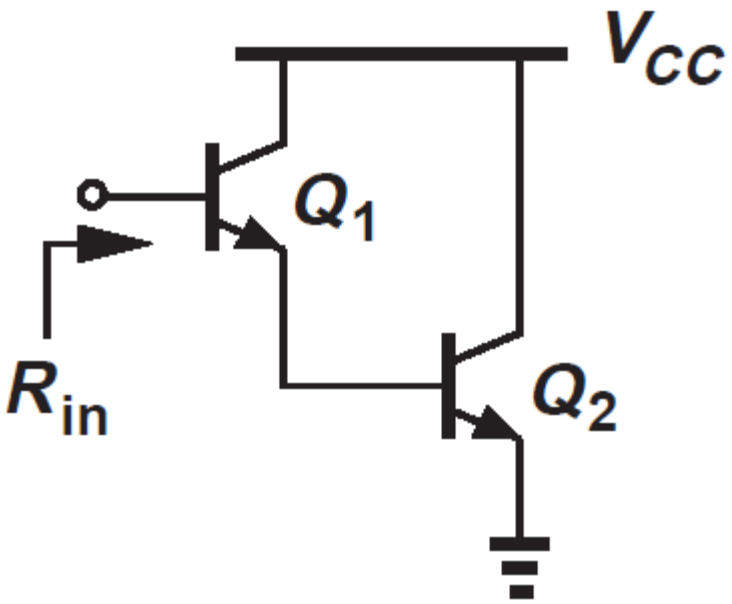
Chapter 5

5.3. Compute the input resistance of the circuits depicted in Fig. 5.105. Assume $V_A = \infty$.

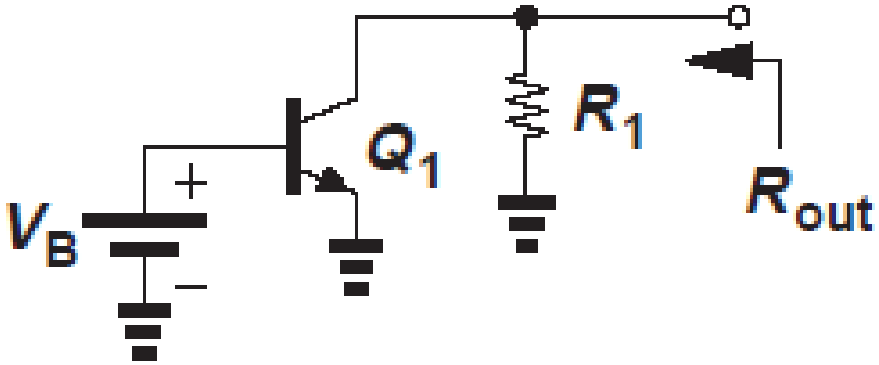


(b)

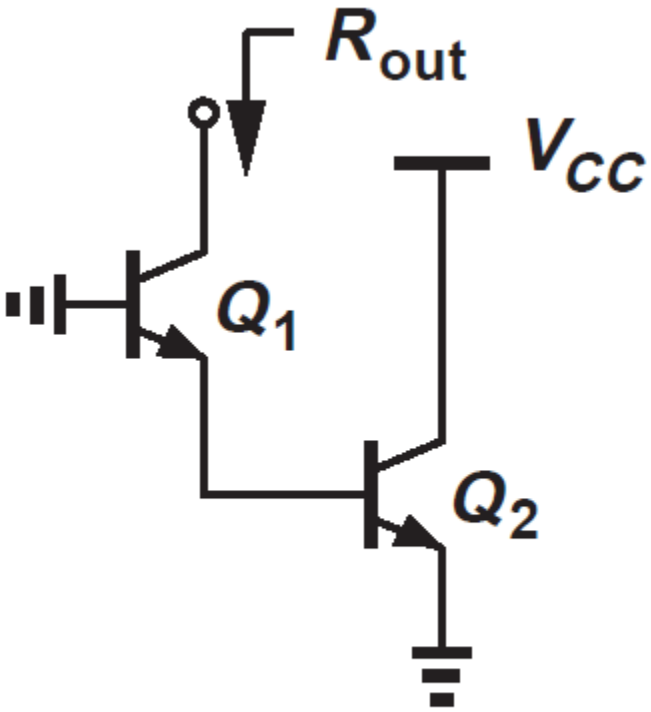


(d)

5.4. Compute the output resistance of the circuits depicted in Fig. 5.106.

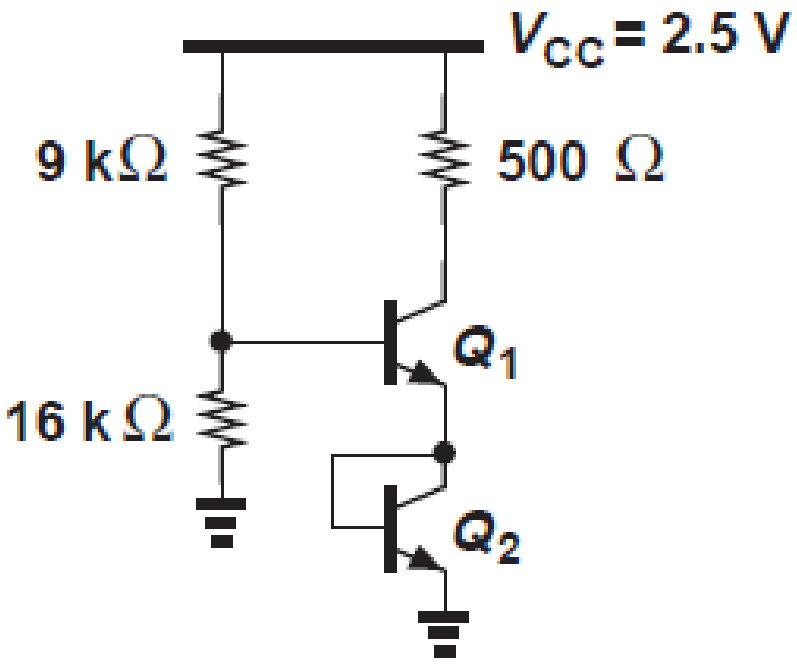


(a)



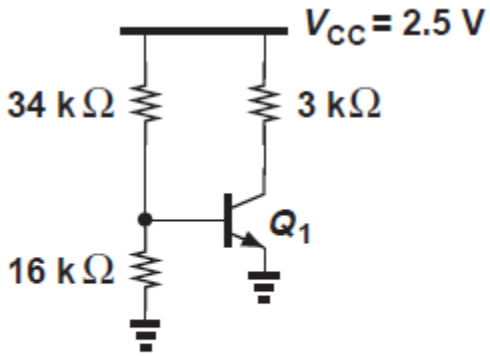
(d)

*5.9. Calculate the bias point of the circuits shown in Fig. 5.110. Assume $\beta = 100$, $I_S = 5 \times 10^{-16}$ A, and $V_A = \infty$.

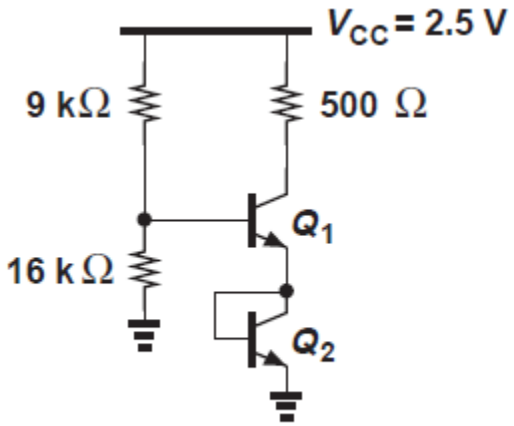


(b)

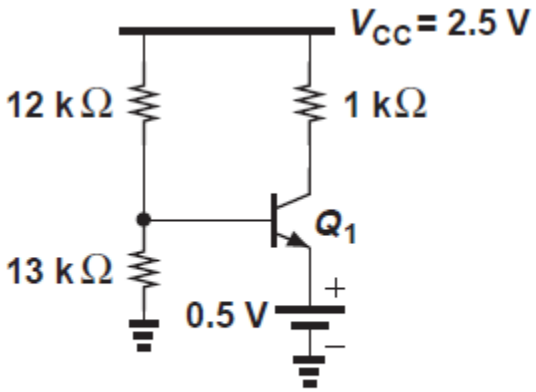
5.10. Construct the small-signal equivalent of each of the circuits in Problem 5.9.



(a)



(b)

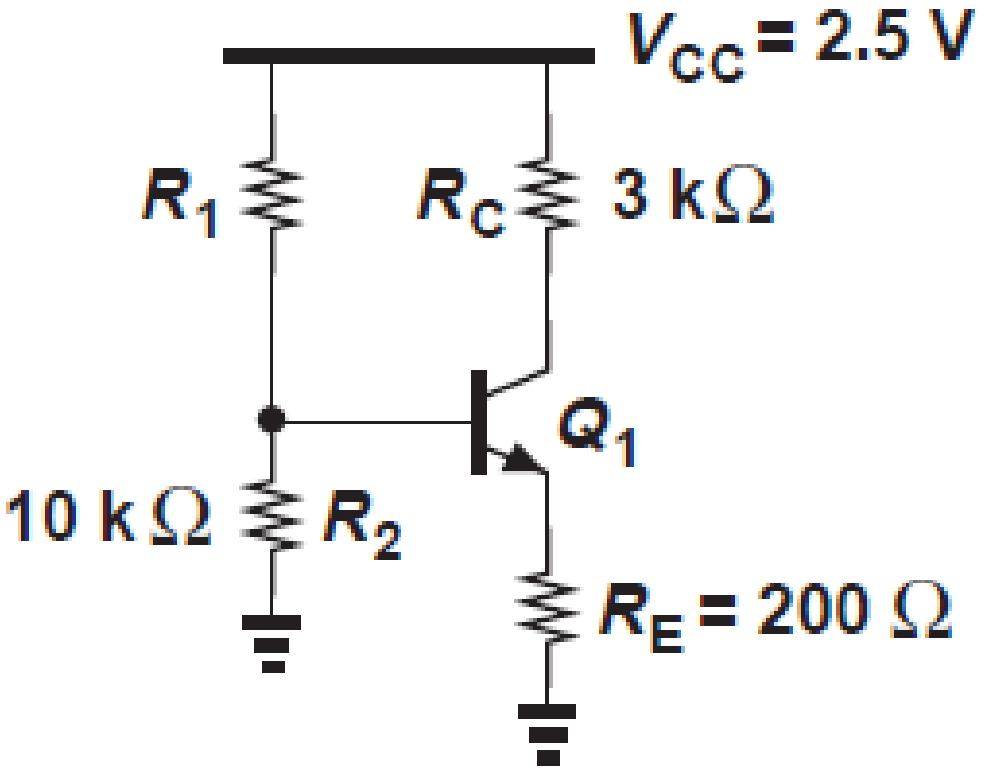


(c)

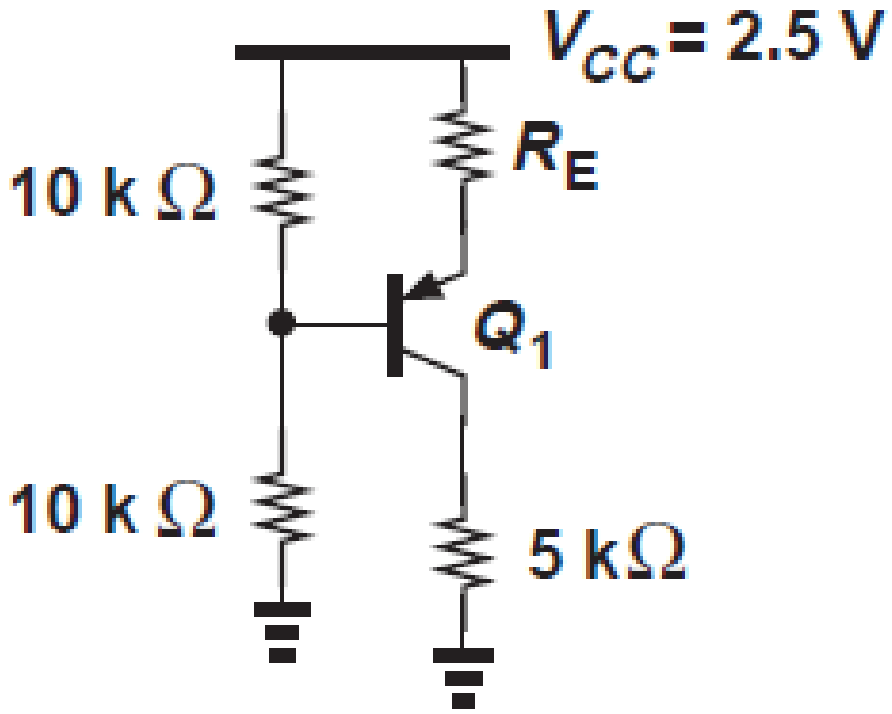
5.16. The circuit of Fig. 5.115 is designed for a collector current of 0.25 mA. Assume $I_S = 6 \times 10^{-16}$ A, $\beta = 100$, and $V_A = \infty$.

(a) Determine the required value of R_1.

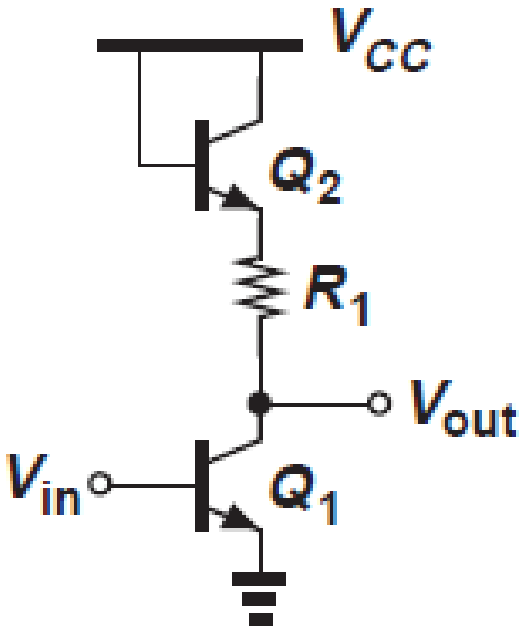
(b) What is the error in I_C if R_E deviates from its nominal value by 5%?



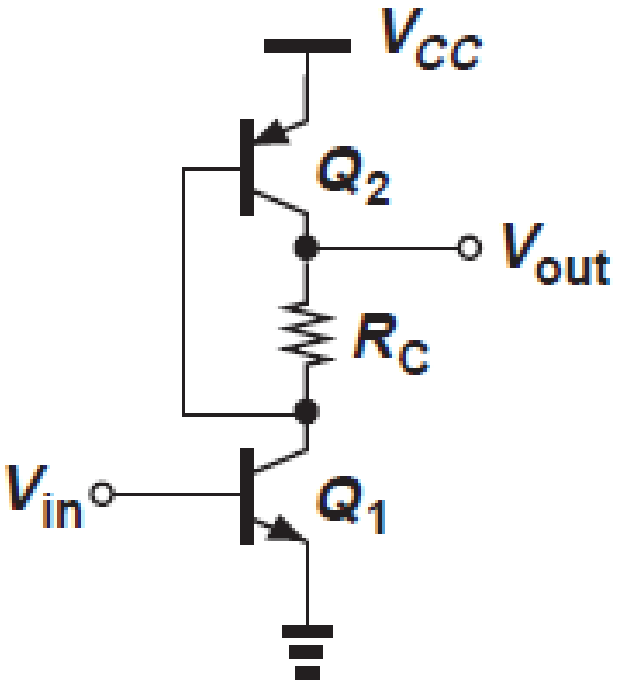
5.30. Calculate the value of R_E in Fig. 5.127 such that Q_1 sustains a reverse bias of 300 mV across its base-collector junction. Assume $\beta = 50$, $I_S = 8 \times 10^{-16}$ A, and $V_A = \infty$. What happens if the value of R_E is halved?



**5.38. Determine the voltage gain and I/O impedances of the circuits shown in Fig. 5.135. Assume $V_A = \infty$. Transistor Q_2 in Figs. 5.135(d) and (e) operates in soft saturation.

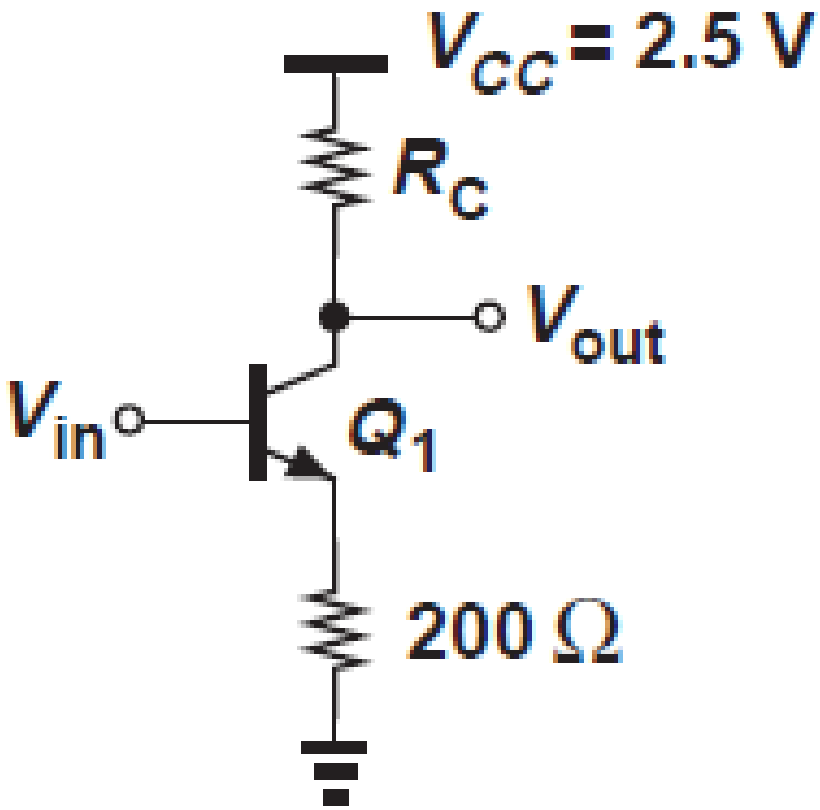


(b)

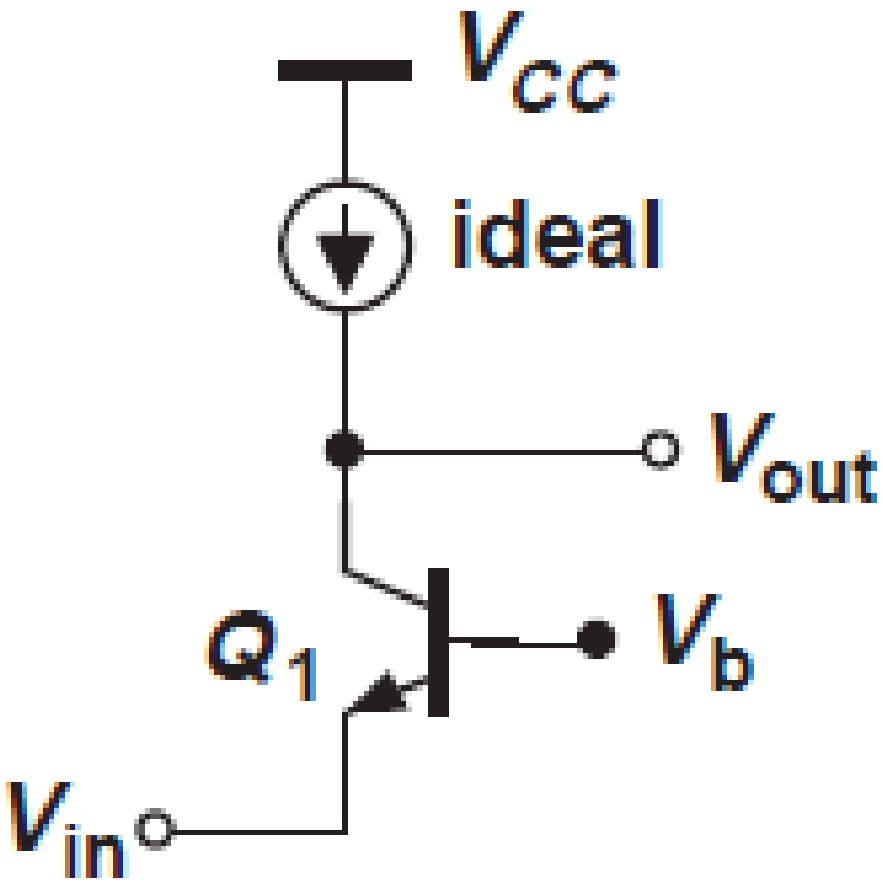


(e)

5.42. We wish to design the degenerated stage of Fig. 5.137 for a voltage gain of 10 with Q_1 operating at the edge of saturation. Calculate the bias current and the value of R_C if $\beta = 100$, $I_S = 5 \times 10^{-16}$ A, and $V_A = \infty$. Calculate the input impedance of the circuit.



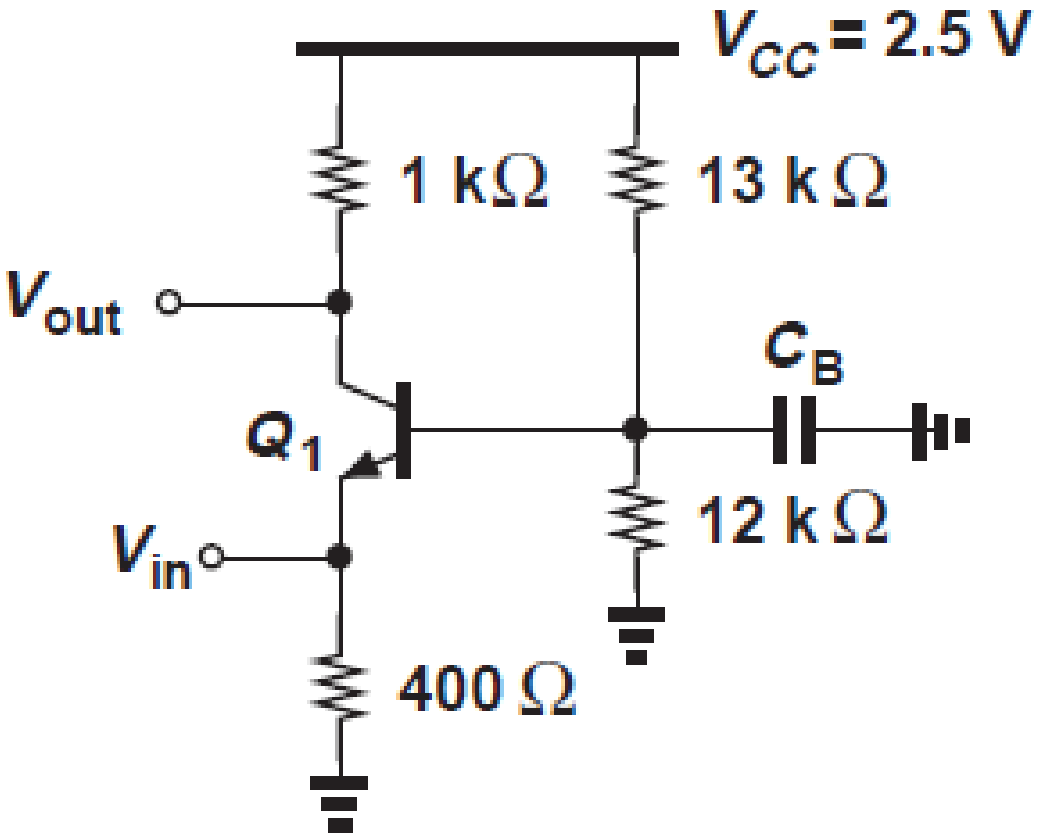
5.57. Calculate the voltage gain and I/O impedances of the CB stage shown in Fig. 5.146. Assume $V_A < \infty$.



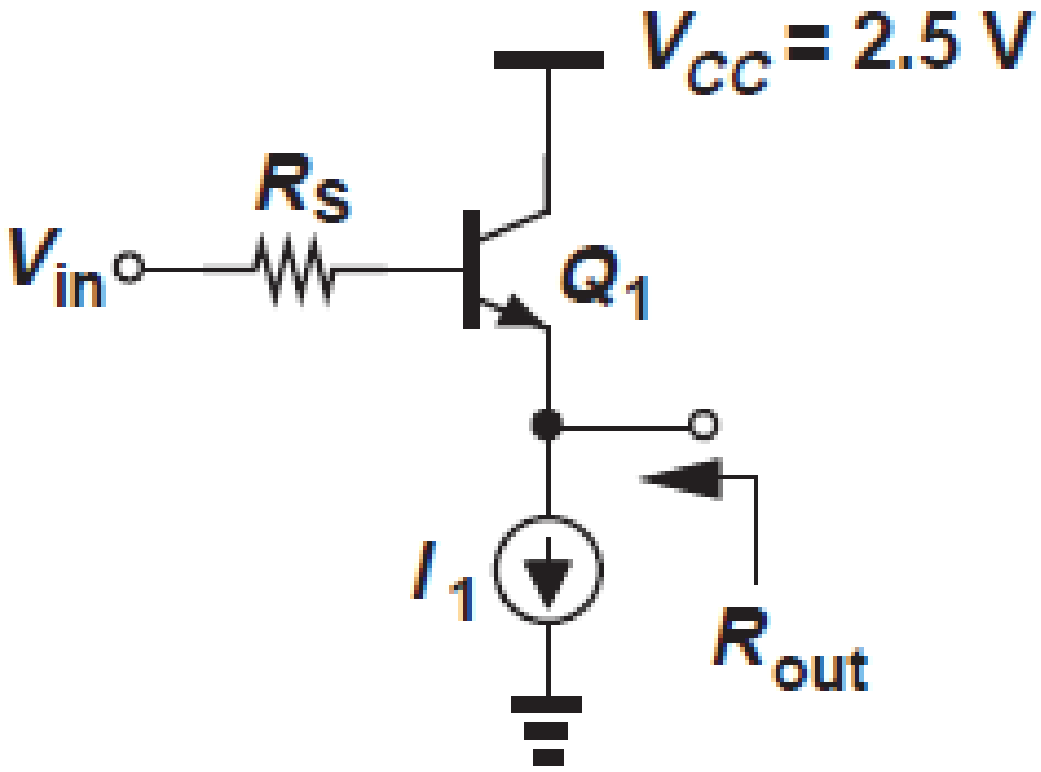
5.58. Consider the CB stage depicted in Fig. 5.147, where $\beta = 100$, $I_S = 8 \times 10^{-16}$ A, $V_A = \infty$, and C_B is very large.

(a) Determine the operating point of Q_1.

(b) Calculate the voltage gain and I/O impedances of the circuit.



5.67. A microphone having an output impedance $R_S = 200\,\Omega$ drives an emitter follower as shown in Fig. 5.153. Determine the bias current such that the output impedance does not exceed 5 Ω. Assume $\beta = 100$ and $V_A = \infty$.

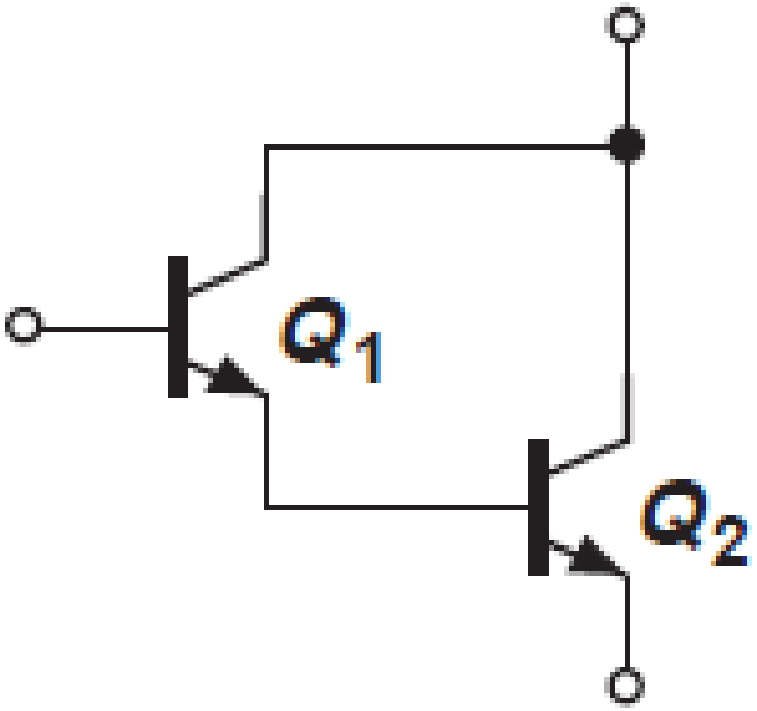


*5.69. Figure 5.155 depicts a "Darlington pair," where Q_1 plays a role somewhat similar to an emitter follower driving Q_2. Assume $V_A = \infty$ and the collectors of Q_1 and Q_2 are tied to V_{CC}. Note that $I_{E1}(\approx I_{C1}) = I_{B2} = I_{C2}/\beta$.

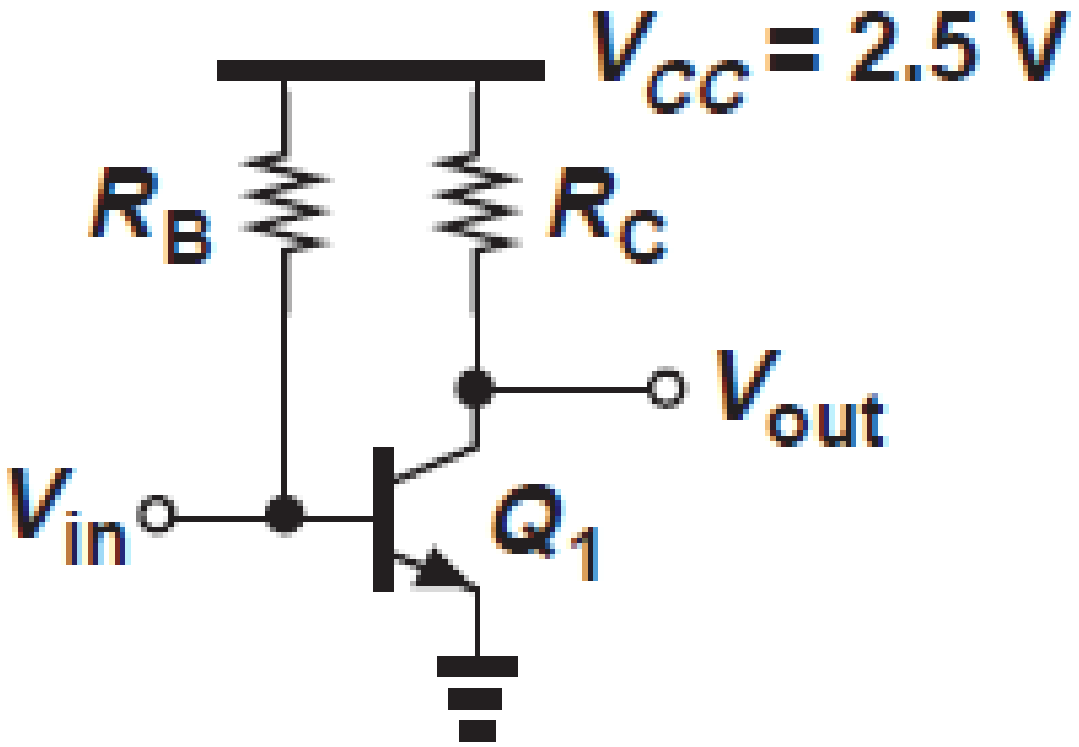
(a) If the emitter of Q_2 is grounded, determine the impedance seen at the base of Q_1.

(b) If the base of Q_1 is grounded, calculate the impedance seen at the emitter of Q_2.

(c) Compute the current gain of the pair, defined as $(I_{C1} + I_{C2})/I_{B1}$.



5.77. The CE stage of Fig. 5.161 must be designed for minimum supply voltage but with a voltage gain of 15 and an output impedance of 2 kΩ. If the transistor is allowed to sustain a base-collector forward bias of 400 mV, design the stage and calculate the required supply voltage.



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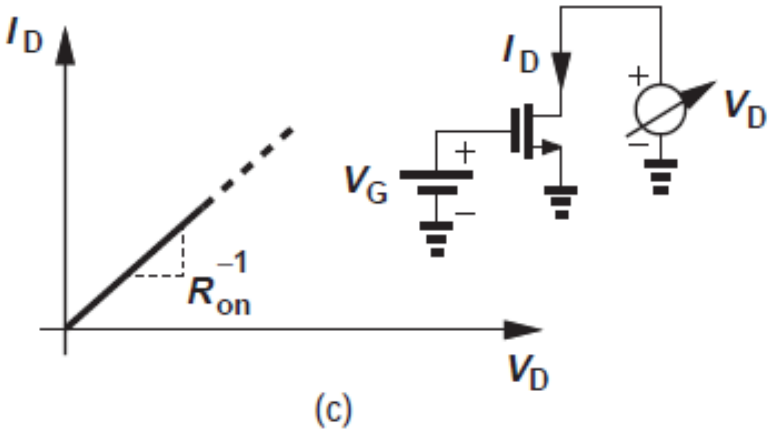
Chapter 6

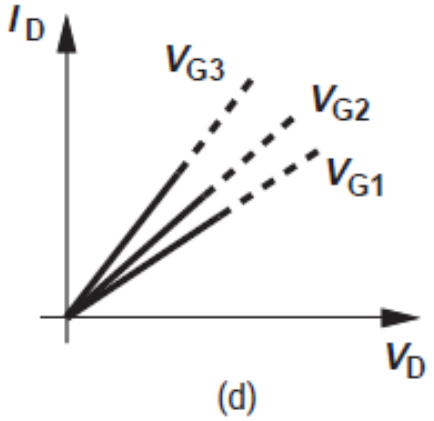
6.9. For a MOS transistor biased in the triode region, we can define an incremental drain-source resistance as

$$r_{DS,tri} = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1}. \qquad (6.78)$$

Derive an expression for this quantity.

In the following problems, unless otherwise stated, assume $\mu_n C_{ox} = 200\,\mu\text{A/V}^2$, $\mu_p C_{ox} = 100\,\mu\text{A/V}^2$, and $V_{TH} = 0.4\,\text{V}$ for NMOS devices and $-0.4\,\text{V}$ for PMOS devices.

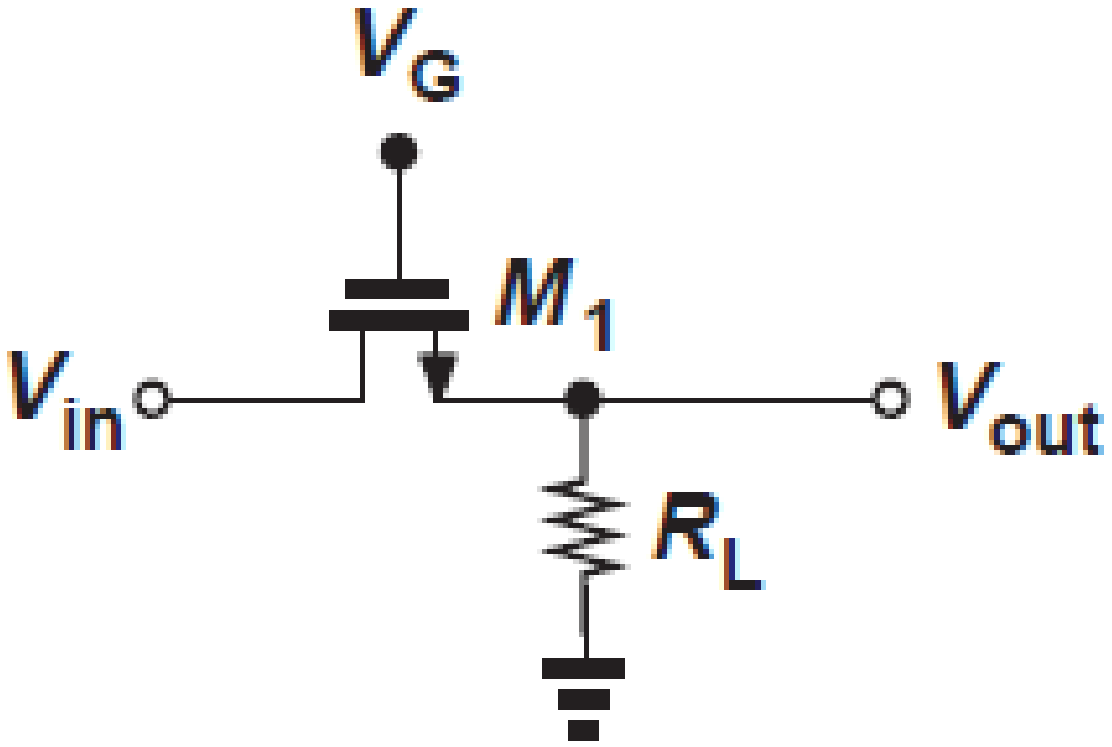




6.14. In the circuit of Fig. 6.37, the input is a small sinusoid superimposed on a dc level: $V_{in} = V_0 \cos \omega t + V_1$, where V_0 is on the order of a few millivolts.

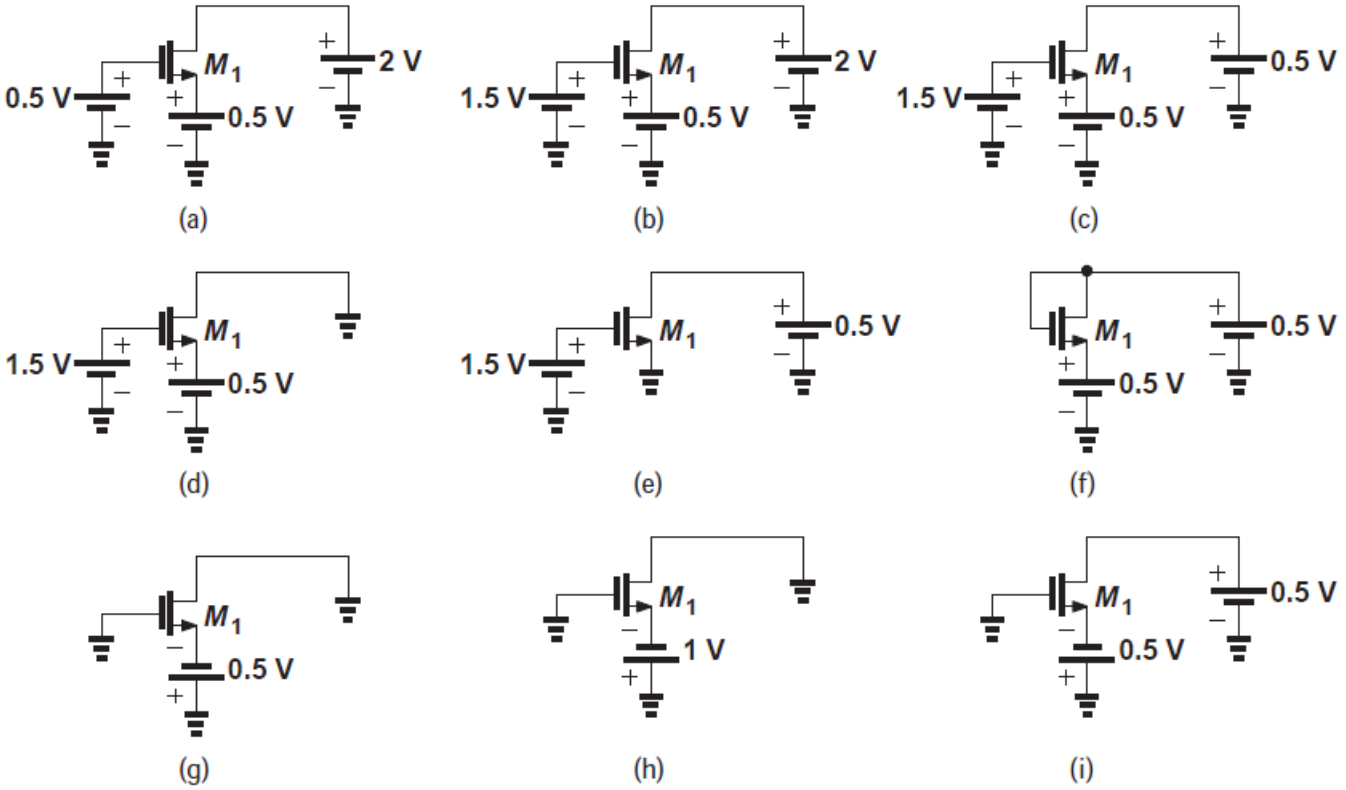
(a) For $V_1 = 0$, obtain W/L in terms of R_L and other parameters so that $V_{out} = 0.95 V_{in}$.

(b) Repeat part (a) for $V_1 = 0.5$ V. Compare the results.



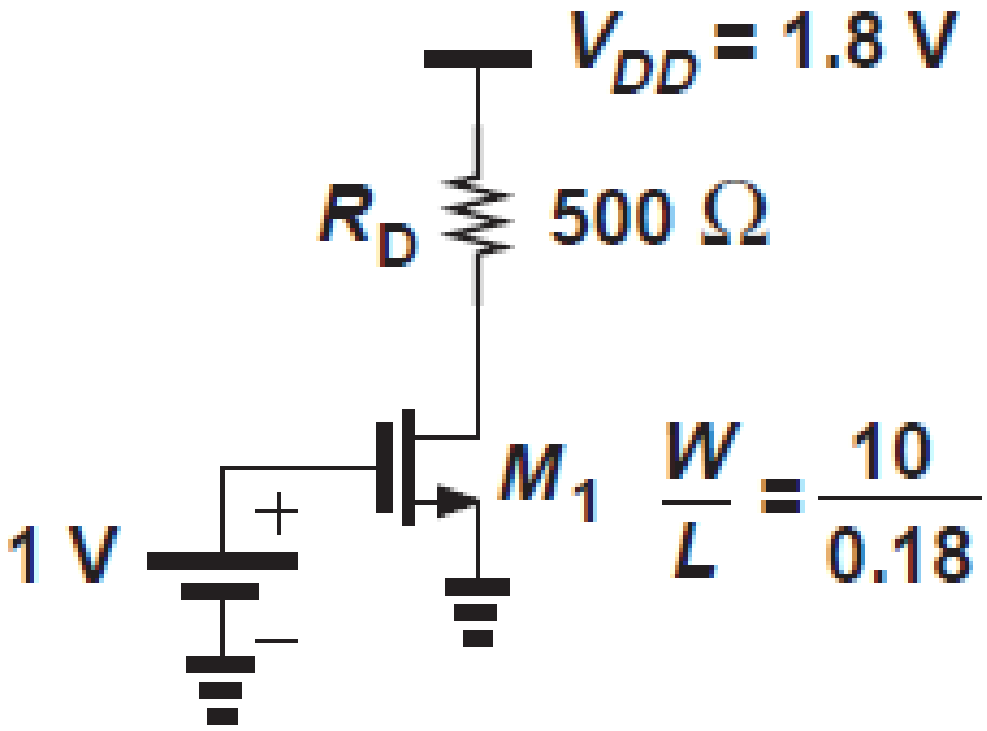
*6.20. Determine the region of operation of M_1 in each of the circuits shown in Fig. 6.39.

$V_{TH} = 0.4\ V\ for\ NMOS\ devices$

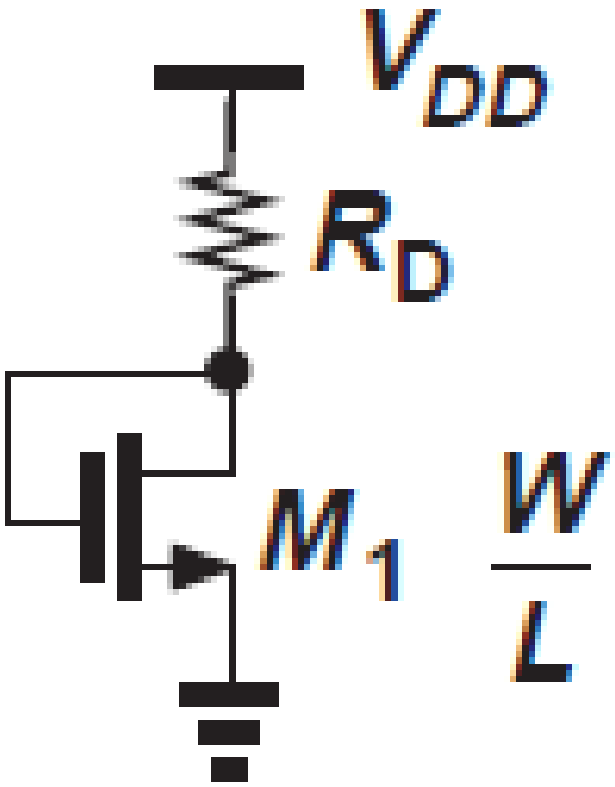


	A	B	C	D	E	F	G	H	i
V_{GS}									
$V_{GS}-V_{TH}=V_{OV}$									
V_{DS}									
V_{GD}									
Region									

6.24. In the Fig. 6.42 ,what is the minimum allowable value of V_{DD} if M_1 must not enter the triode region? Assume $\lambda = 0$.



6.25. Calculate the bias current of M_1 in Fig. 6.43 if $\lambda = 0$.



6.26. Compute the value of W/L for M_1 in Fig. 6.44 for a bias current of I_1. Assume $\lambda = 0$.

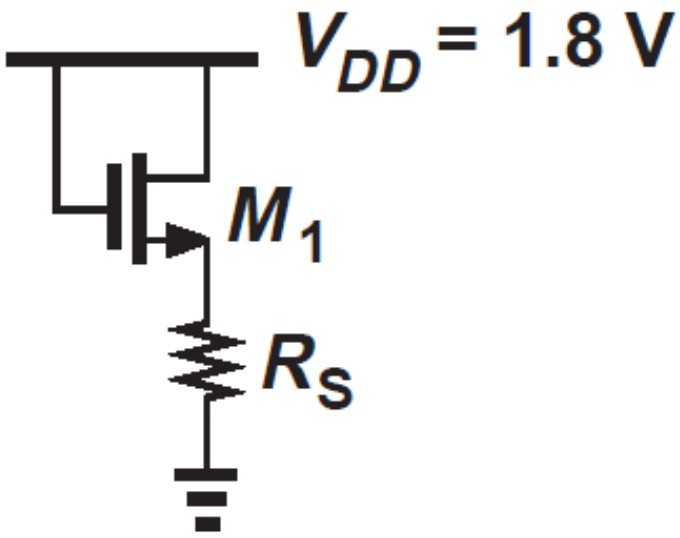
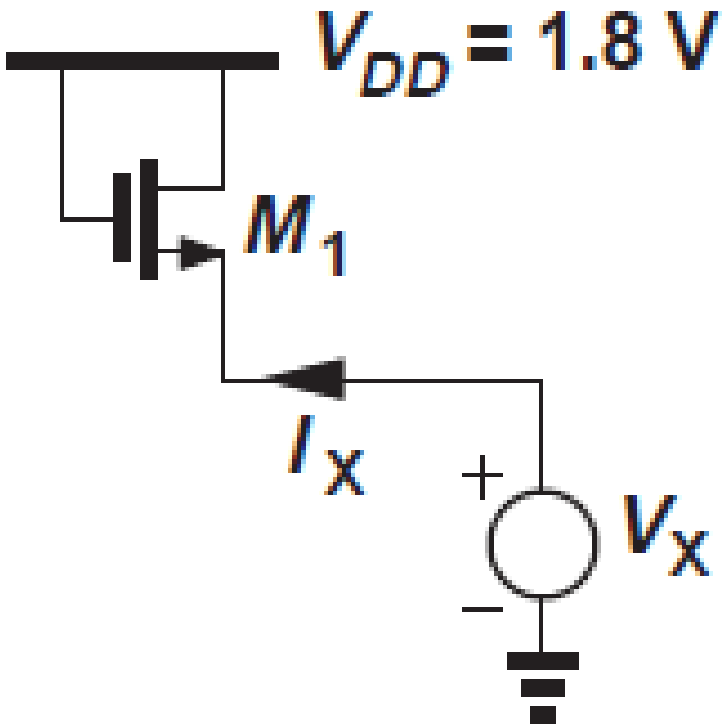
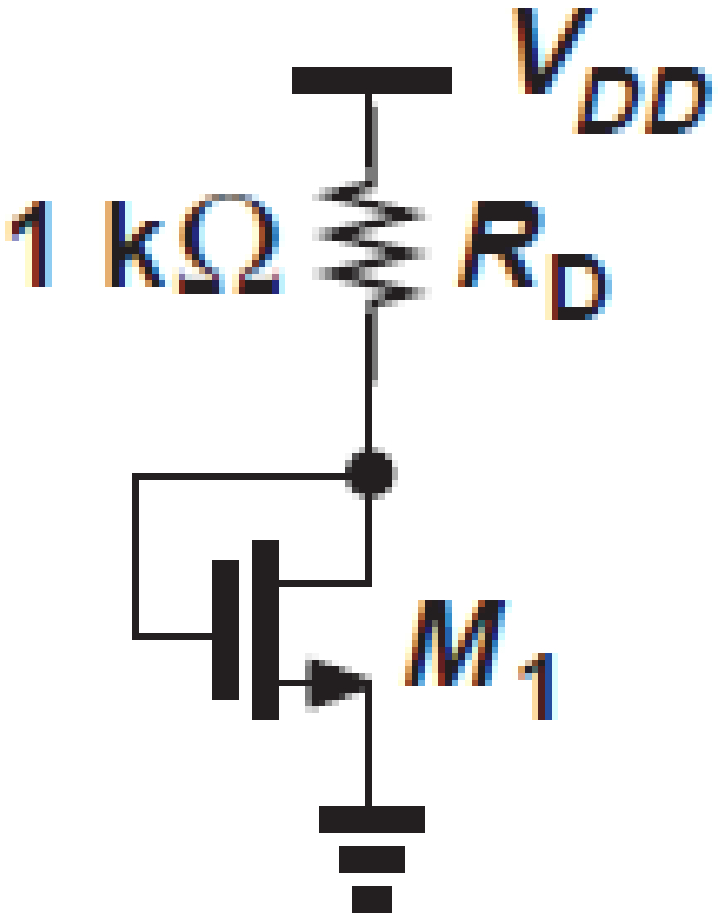


Figure 6.44

**6.28. Sketch I_X as a function of V_X for the circuits shown in Fig. 6.46. Assume V_X goes from 0 to $V_{DD} = 1.8$ V. Also, $\lambda = 0$. Determine at what value of V_X the device changes its region of operation.

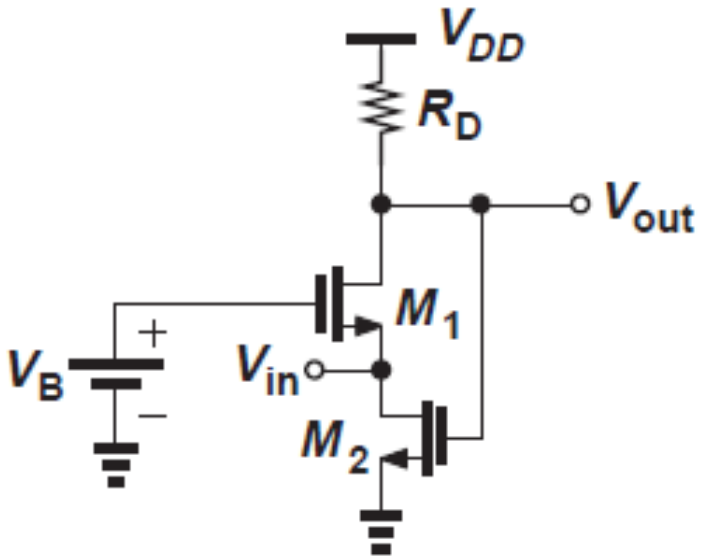


6.29. Assuming $W/L = 10/0.18$ $\lambda = 0.1\ \mathrm{V}^{-1}$, and $V_{DD} = 1.8$ V, calculate the drain current of M_1 in Fig. 6.47.



6.33. The "intrinsic gain" of a MOSFET operating in saturation is defined as $g_m r_O$. Derive an expression for $g_m r_O$ and plot the result as a function of I_D. Assume V_{DS} is constant.

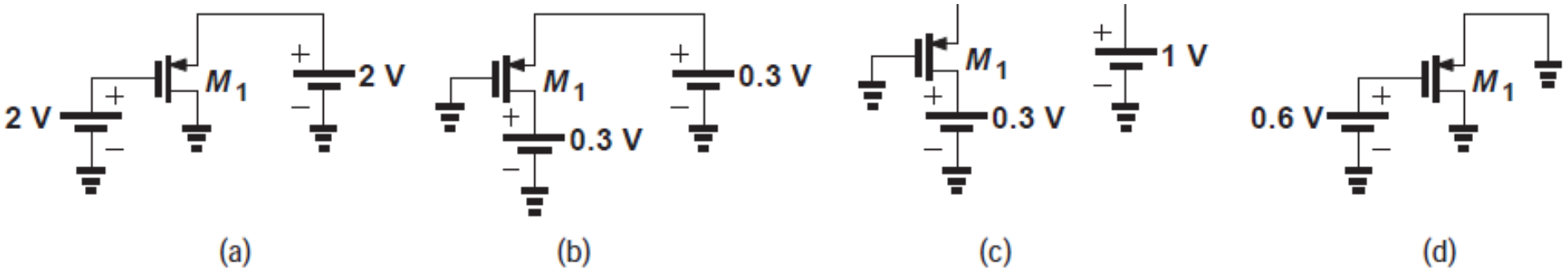
6.38. Construct the small-signal model of the circuits depicted in Fig. 6.50. Assume all transistors operate in saturation and $\lambda \neq 0$.



(e)

*6.39. Determine the region of operation of M_1 in each circuit shown in Fig. 6.51.

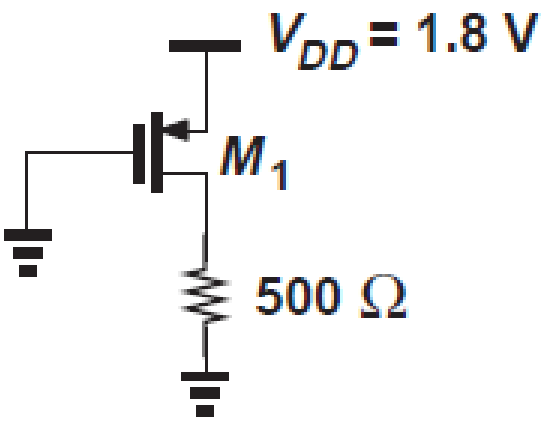
$V_{TH} = -0.4\,V\ for\ PMOS\ devices$



(a) (b) (c) (d)

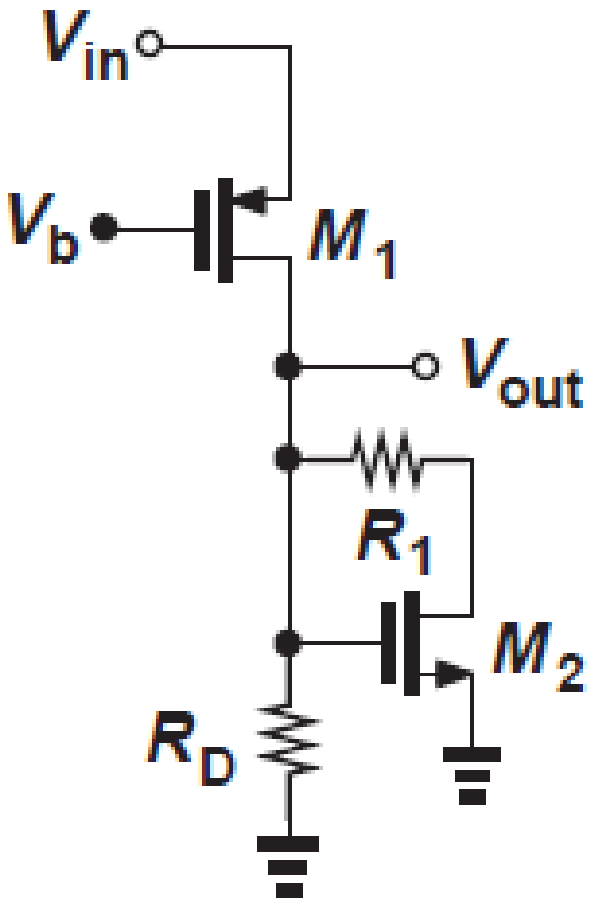
	A	B	C	D
V_{GS}				
$V_{GS}-V_{TH}=V_{OV}$				
V_{DS}				
V_{GD}				
Region				

6.43. If $W/L = 10/0.18$ and $\lambda = 0$, determine the operating point of M_1 in each circuit depicted in Fig. 6.54.



(a)

6.45. Construct the small-signal model of each circuit shown in Fig. 6.56 if all of the transistors operate in saturation and $\lambda \neq 0$.



(c)

EENG 350 Electronic Circuits I

Problems to be solved in Class

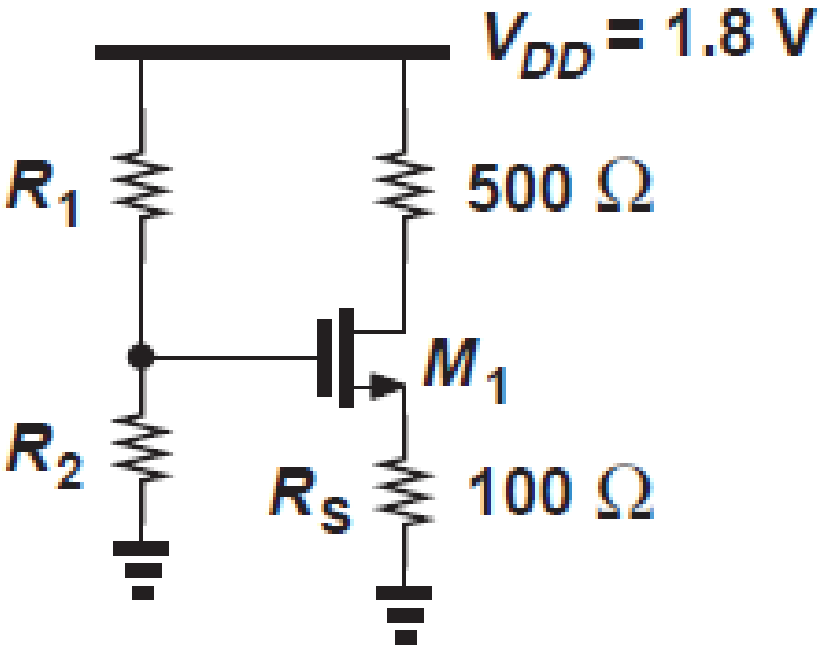
Chapter 7

7.4. The circuit of Fig. 7.42 must be designed for a voltage drop of 200 mV across R_S.

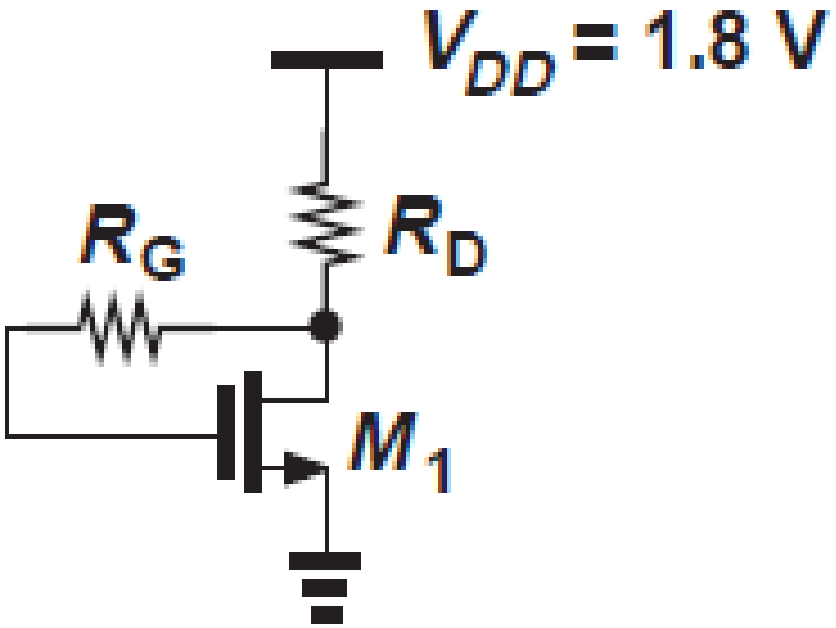
(a) Calculate the minimum allowable value of W/L if M_1 must remain in saturation.

(b) What are the required values of R_1 and R_2 if the input impedance must be at least 30 kΩ?

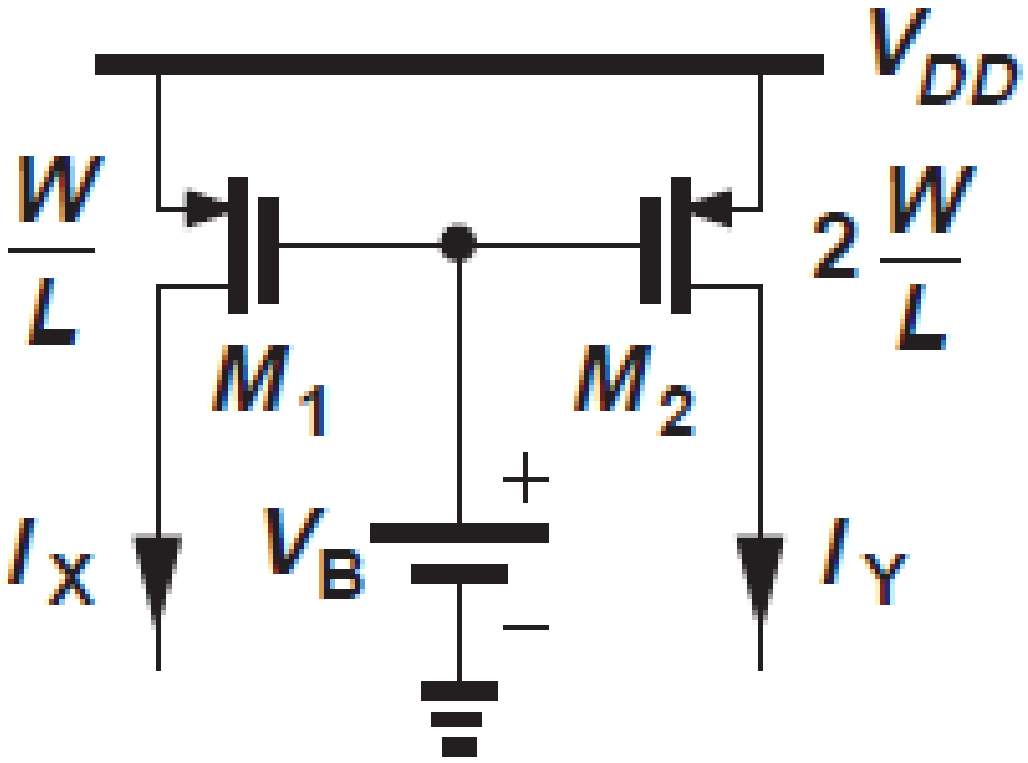
In the following problems, unless otherwise stated, assume $\mu_n C_{ox} = 200\,\mu\text{A/V}^2$, $\mu_p C_{ox} = 100\,\mu\text{A/V}^2$, and $V_{TH} = 0.4\,\text{V}$ for NMOS devices and $-0.4\,\text{V}$ for PMOS devices.



7.6. The self-biased stage of Fig. 7.44 must be designed for a drain current of 1 mA. If M_1 is to provide a transconductance of $1/(100\ \Omega)$, calculate the required value of R_D.



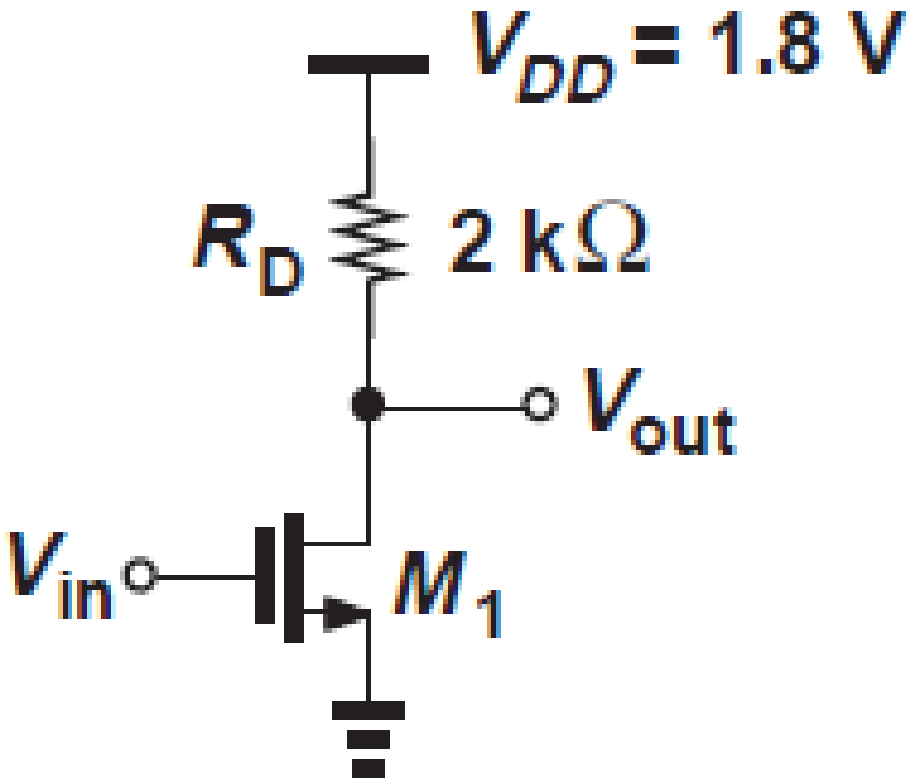
7.14. In the circuit of Fig. 7.51, M_1 and M_2 serve as current sources. Calculate I_X and I_Y if $V_B = 1\,\text{V}$ and $W/L = 20/0.25$. How are the output resistances of M_1 and M_2 related?



7.18. The circuit of Fig. 7.54 is designed with $W/L = 20/0.18, \lambda = 0$, and $I_D = 0.25\,\text{mA}$.

(a) Compute the required gate bias voltage.

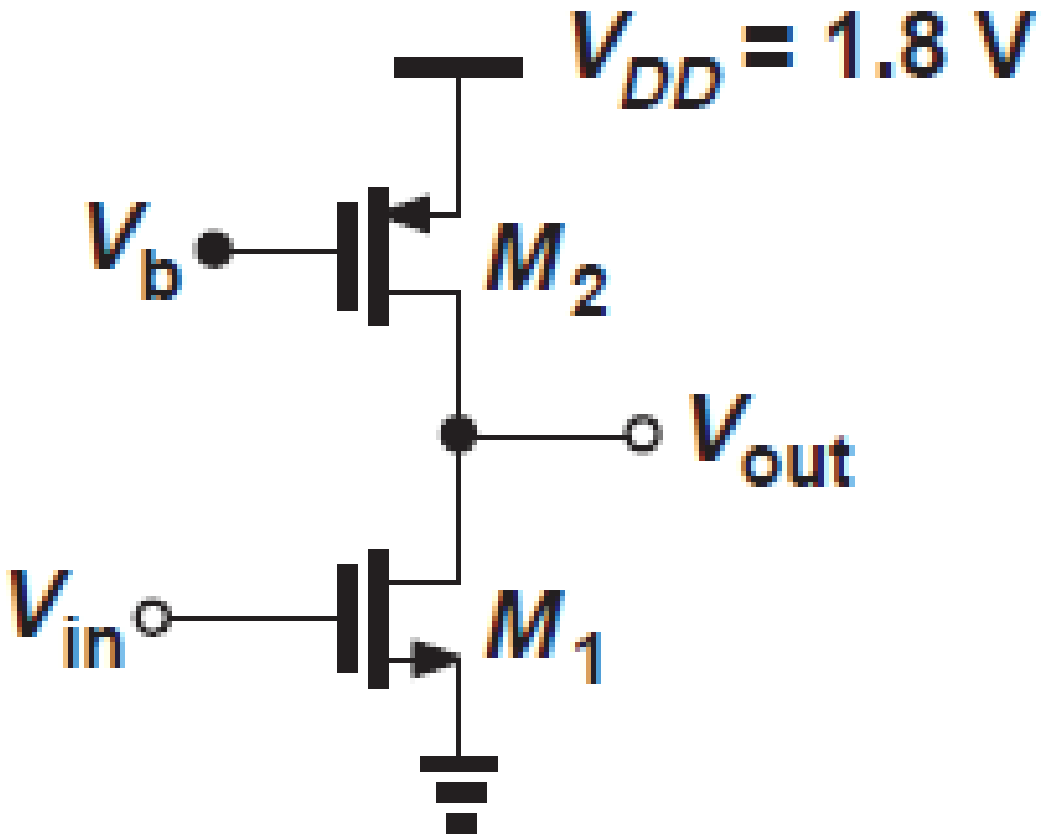
(b) With such a gate voltage, how much can W/L be increased while M_1 remains in saturation? What is the maximum voltage gain that can be achieved as W/L increases?



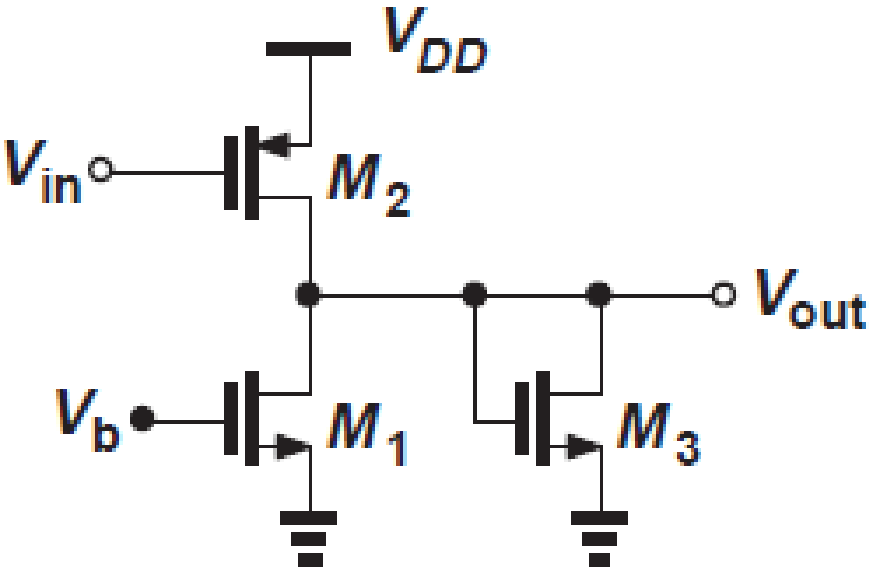
7.20. The CS stage of Fig. 7.56 must provide a voltage gain of 10 with a bias current of 0.5 mA. Assume $\lambda_1 = 0.1\,\text{V}^{-1}$, and $\lambda_2 = 0.15\,\text{V}^{-1}$.

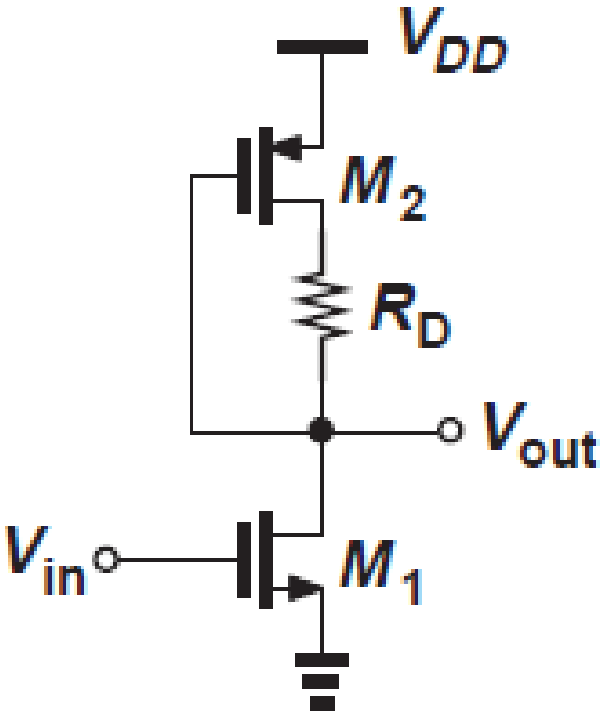
(a) Compute the required value of $(W/L)_1$.

(b) If $(W/L)_2 = 20/0.18$, calculate the required value of V_B.

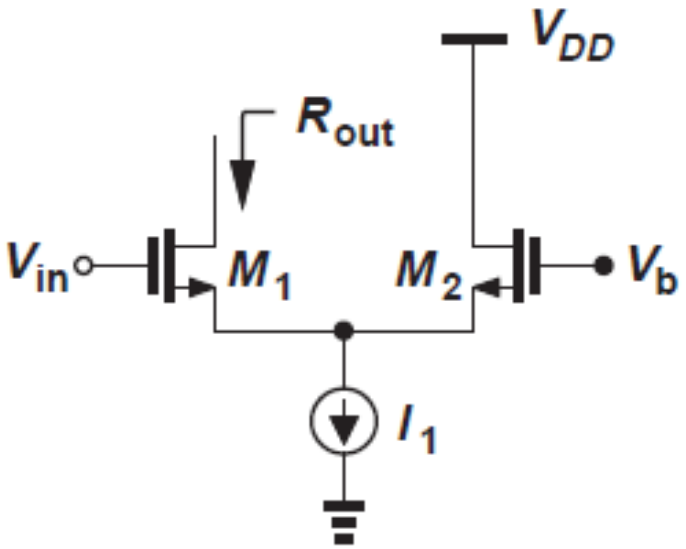


**7.28. If $\lambda \neq 0$, determine the voltage gain of the stages shown in Fig. 7.60.

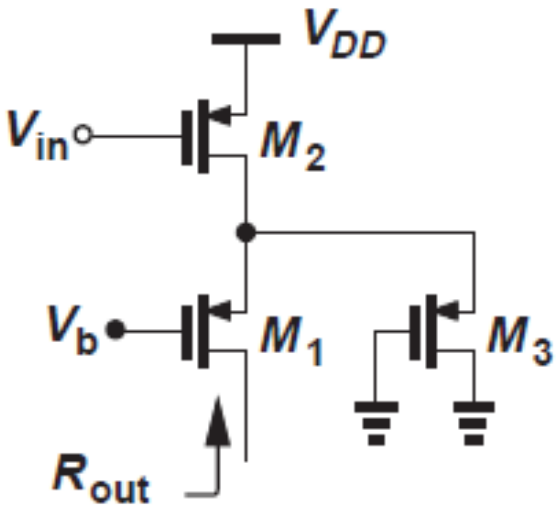




*7.33. Determine the output impedance of each circuit shown in Fig. 7.63. Assume $\lambda \neq 0$.



(b)



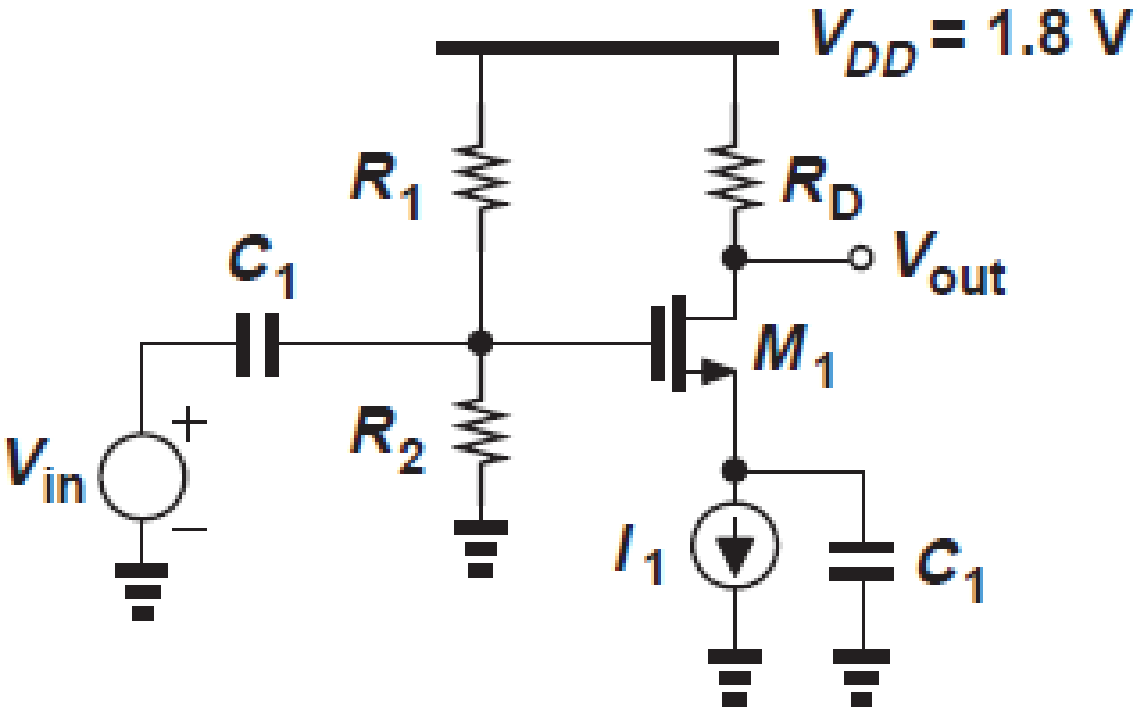
(d)

7.37. In the common-source stage depicted in Fig. 7.66, the drain current of M_1 is defined by the ideal current source I_1 and remains independent of R_1 and R_2 (why?). Suppose $I_1 = 1$ mA, $R_D = 500\,\Omega$, $\lambda = 0$, and C_1 is very large.

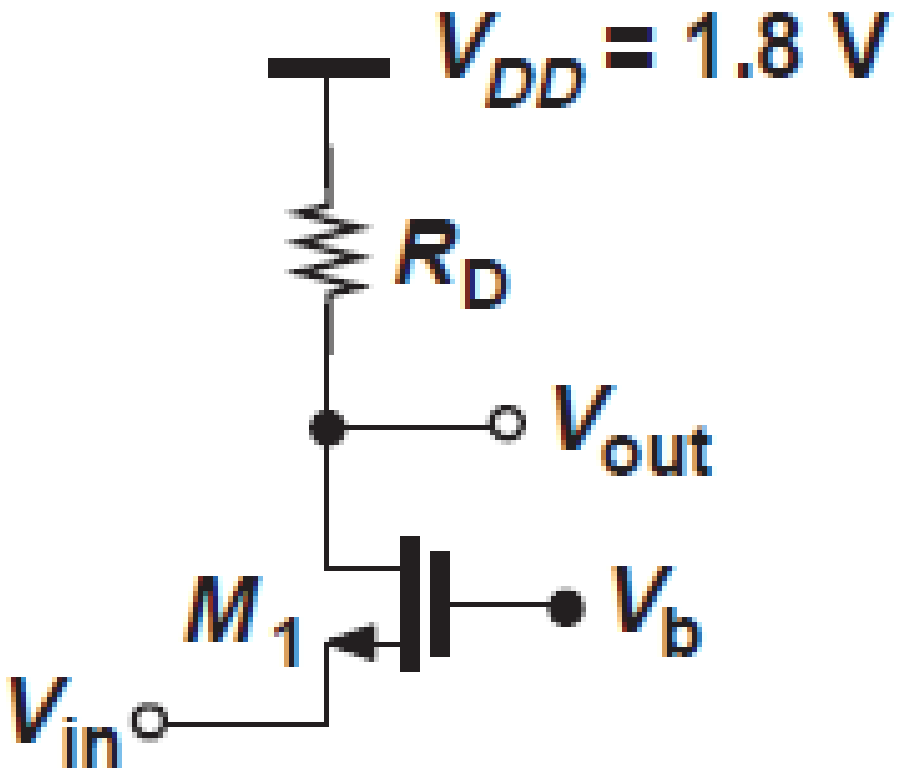
(a) Compute the value of W/L to obtain a voltage gain of 5.

(b) Choose the values of R_1 and R_2 to place the transistor 200 mV away from the triode region while $R_1 + R_2$ draws no more than 0.1 mA from the supply.

(c) With the values found in (b), what happens if W/L is twice that found in (a)? Consider both the bias conditions (e.g., whether M_1 comes closer to the triode region) and the voltage gain.



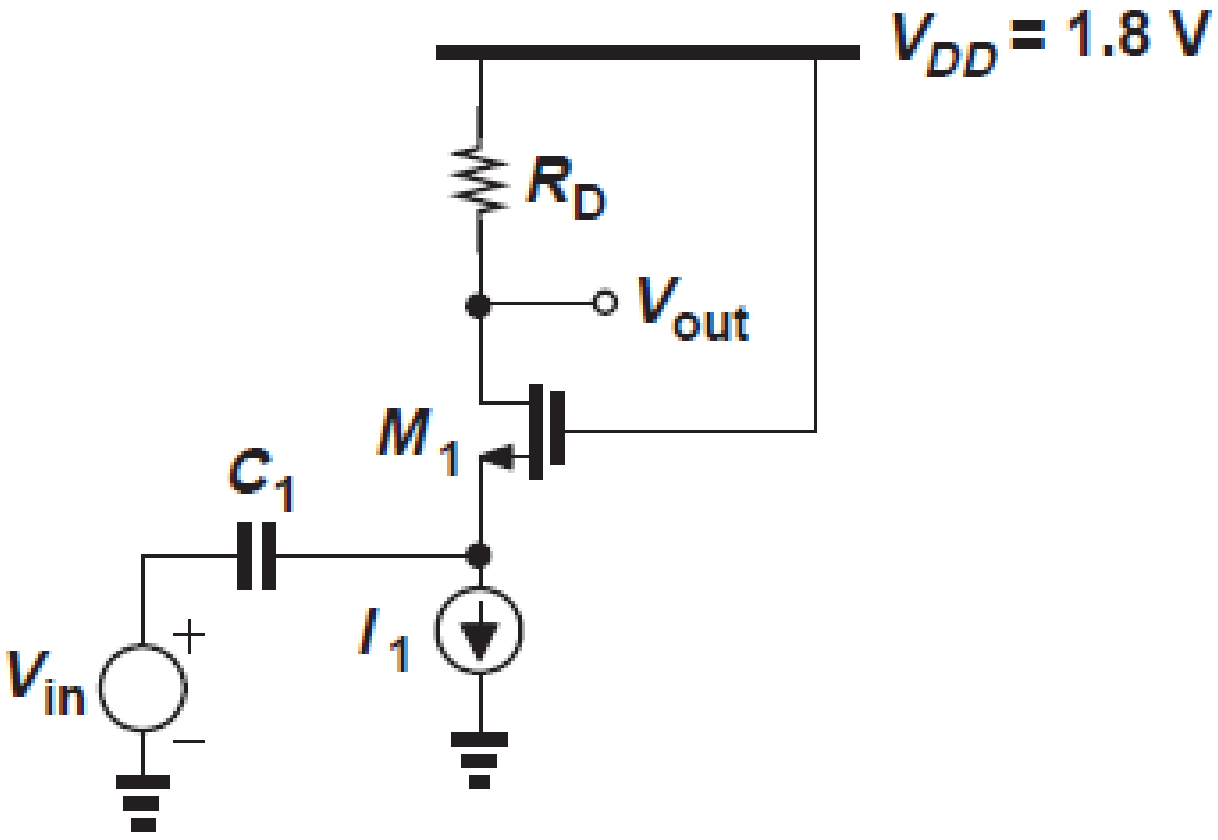
7.40. Suppose in Fig. 7.68, $I_D = 0.5\,\text{mA}$, $\lambda = 0$, and $V_b = 1\,\text{V}$. Determine the values of W/L and R_D for an input impedance of 50 Ω and maximum voltage gain (while M_1 remains in saturation).



7.43. The CG amplifier shown in Fig. 7.70 is biased by means of $I_1 = 1$ mA. Assume $\lambda = 0$ and C_1 is very large.

(a) What value of R_D places the transistor M_1 100 mV away from the triode region?

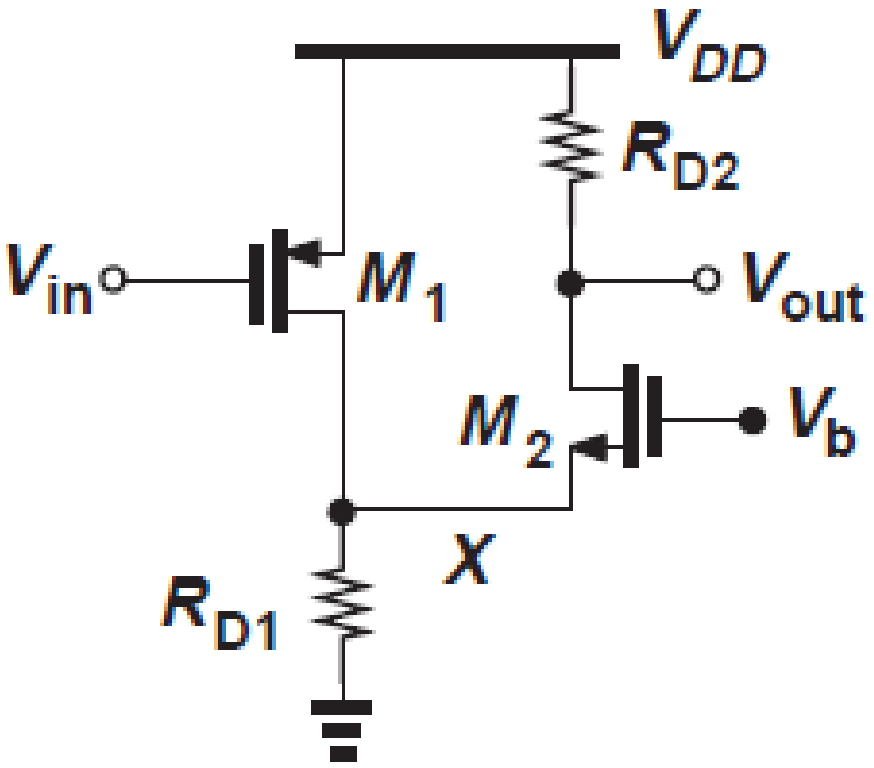
(b) What is the required W/L if the circuit must provide a voltage gain of 5 with the value of R_D obtained in (a)?



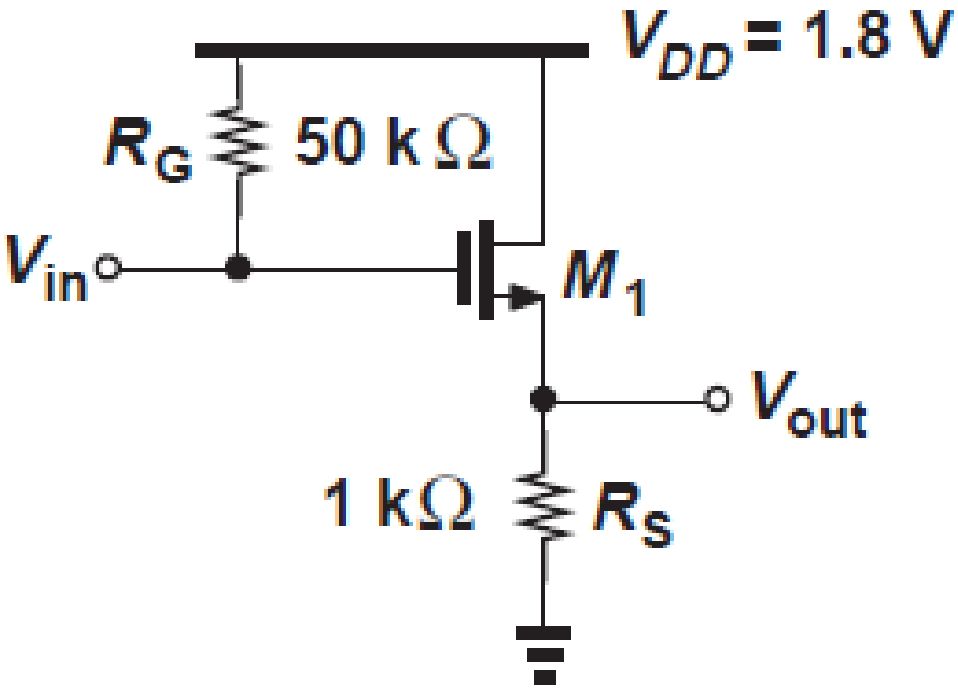
7.46. Consider the circuit of Fig. 7.73., where a common-source stage (M_1 and R_{D1}) is followed by a common-gate stage (M_2 and R_{D2}).

(a) Writing $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$ and assuming $\lambda = 0$, compute the overall voltage gain.

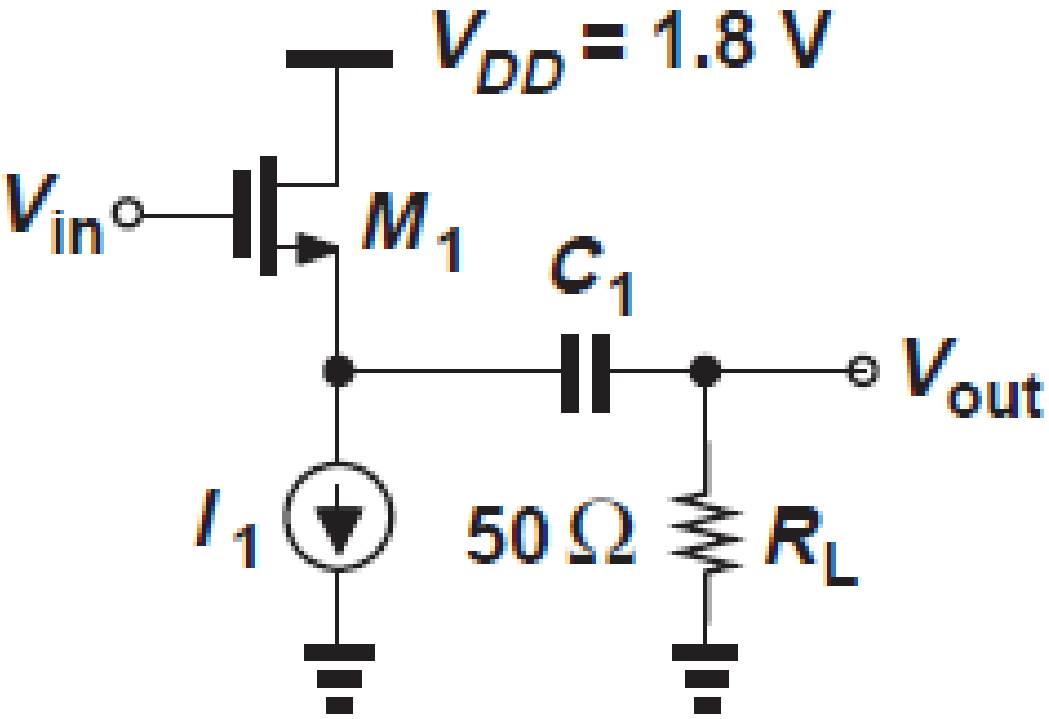
(b) Simplify the result obtained in (a) if $R_{D1} \to \infty$. Explain why this result is to be expected.



7.49. The source follower shown in Fig. 7.76 is biased through R_G. Calculate the voltage gain if $W/L = 20/0.18$ and $\lambda = 0.1\ \text{V}^{-1}$.



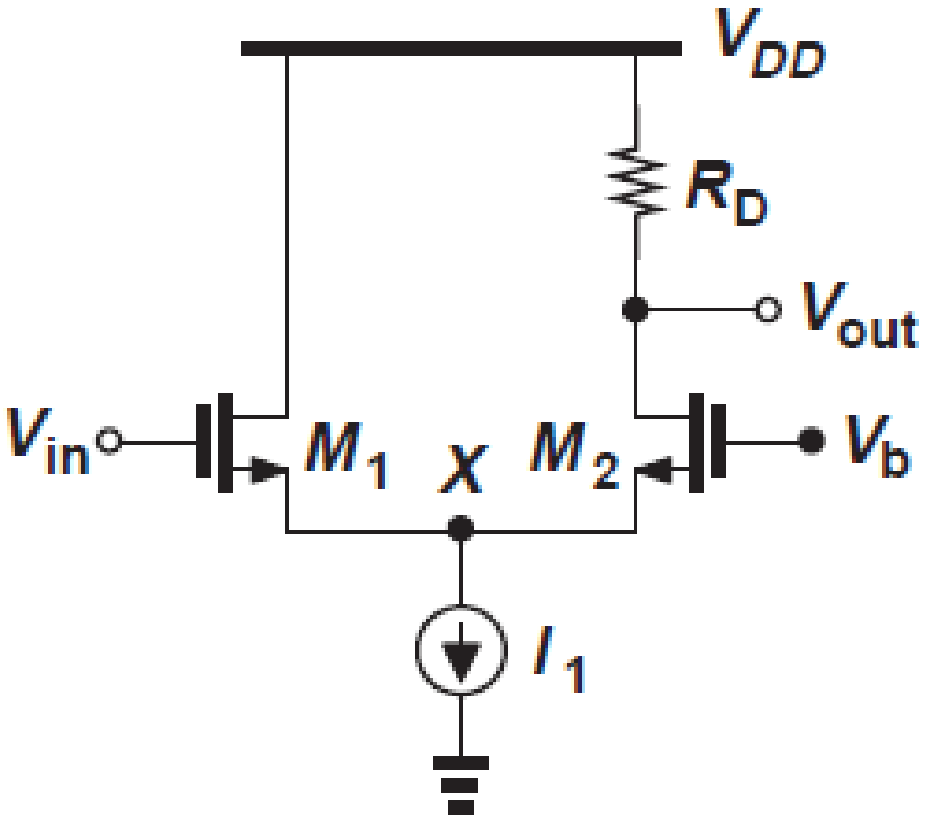
7.54. We wish to design the source follower of Fig. 7.79 for a voltage gain of 0.8 with a power budget of 3 mW. Compute the required value of W/L. Assume C_1 is very large and $\lambda = 0$.



*7.56. Consider the circuit shown in Fig. 7.81, where a source follower (M_1 and I_1) precedes a common-gate stage (M_2 and R_D).

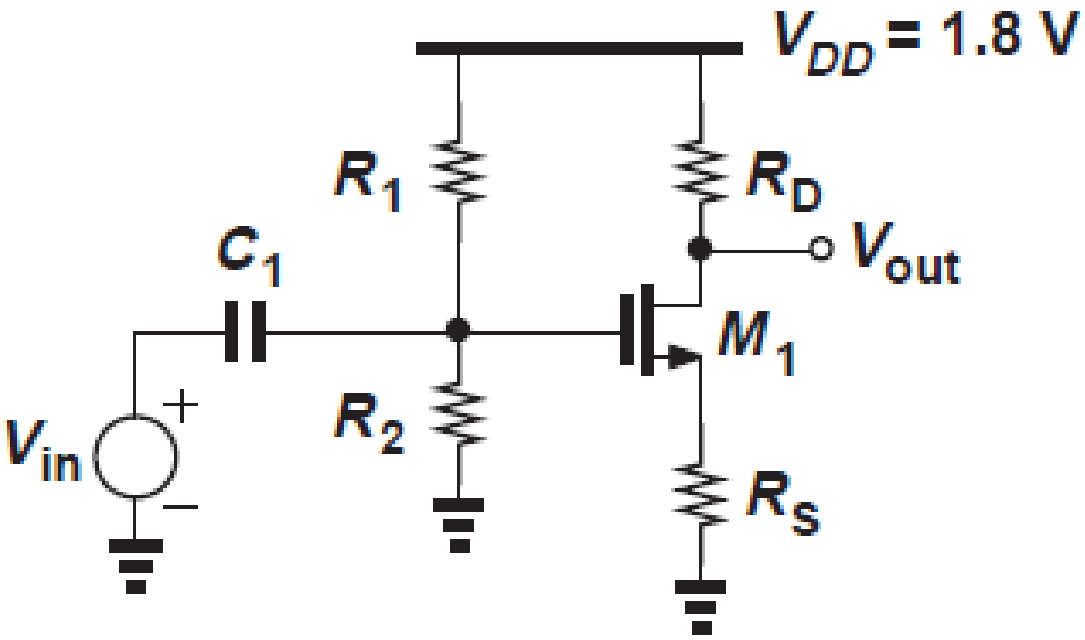
(a) Writing $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$, compute the overall voltage gain.

(b) Simplify the result obtained in (a) if $g_{m1} = g_{m2}$.



7.60. The degenerated stage depicted in Fig. 7.83 must provide a voltage gain of 4 with a power budget of 2 mW while the voltage drop across R_S is equal to 200 mV. If the overdrive voltage of the transistor must not exceed 300 mV and $R_1 + R_2$ must consume less than than 5% of the allocated power, design the circuit. Make the same assumptions as those in Problem 7.57.

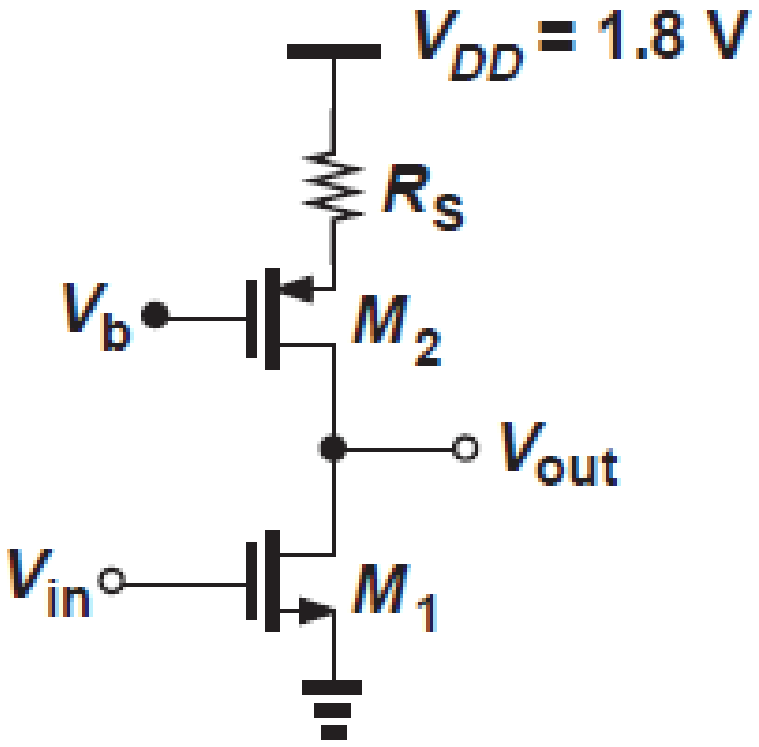
Assume the capacitors are very large and $R_D = 10\,\text{k}\Omega$.



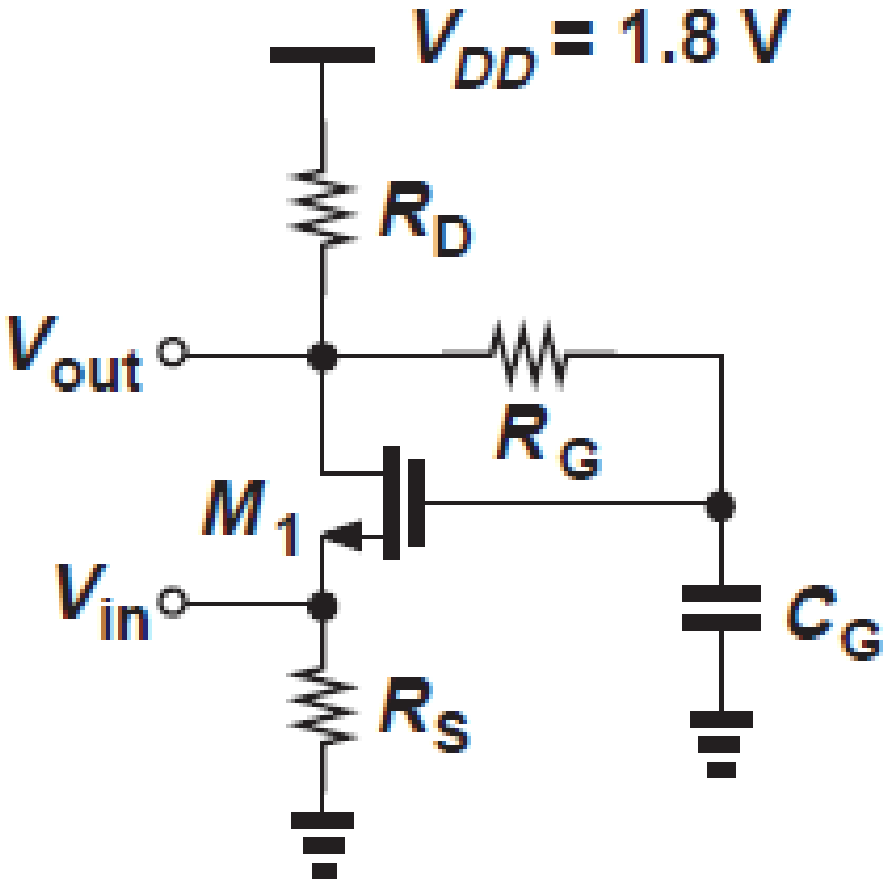
7.65. The CS stage of Fig. 7.87 incorporates a degenerated PMOS current source. The degeneration must raise the output impedance of the current source to about $10r_{O1}$ such that the voltage gain remains nearly equal to the intrinsic gain of M_1. Assume $\lambda = 0.1\ \text{V}^{-1}$ for both transistors and a power budget of 2 mW.

(a) If $V_B = 1\ \text{V}$, determine the values of $(W/L)_2$ and R_S so that the impedance seen looking into the drain of M_2 is equal to $10r_{O1}$.

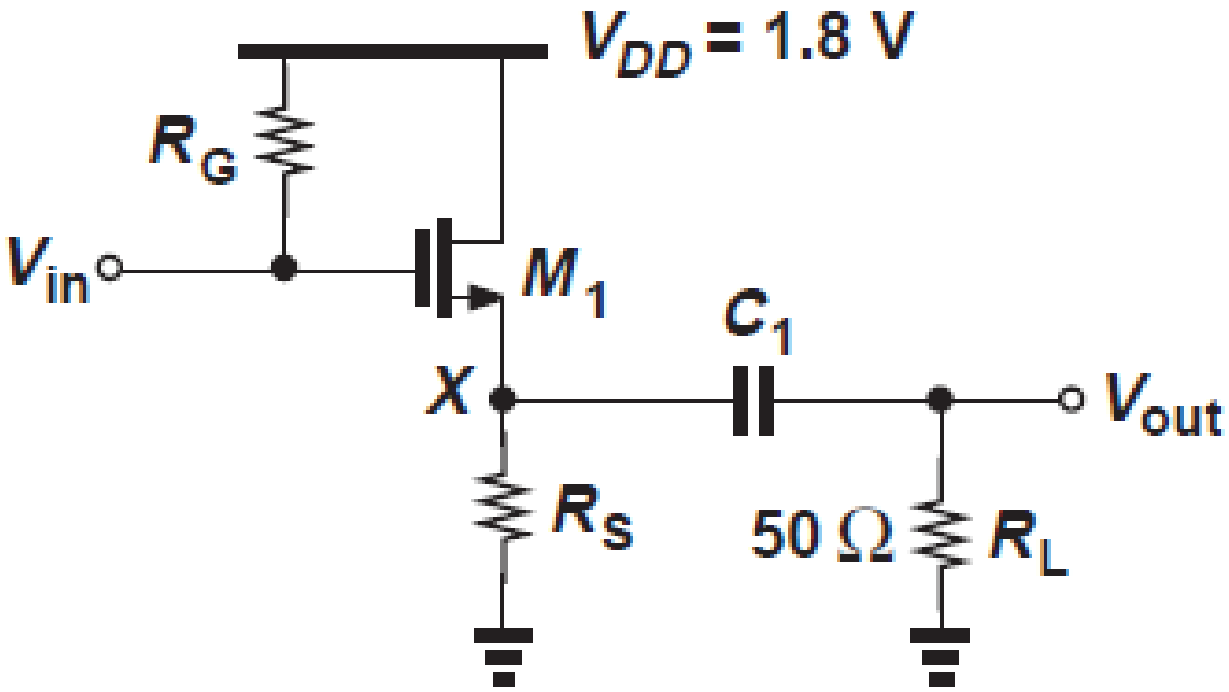
(b) Determine $(W/L)_1$ to achieve a voltage gain of 30.



7.69. Figure 7.91 shows a self-biased common-gate stage, where $R_G \approx 10R_D$ and C_G serves as a low impedance so that the voltage gain is still given by $g_m R_D$. Design the circuit for a power budget of 5 mW and a voltage gain of 5. Assume $R_S \approx 10/g_m$ so that the input impedance remains approximately equal to $1/g_m$.

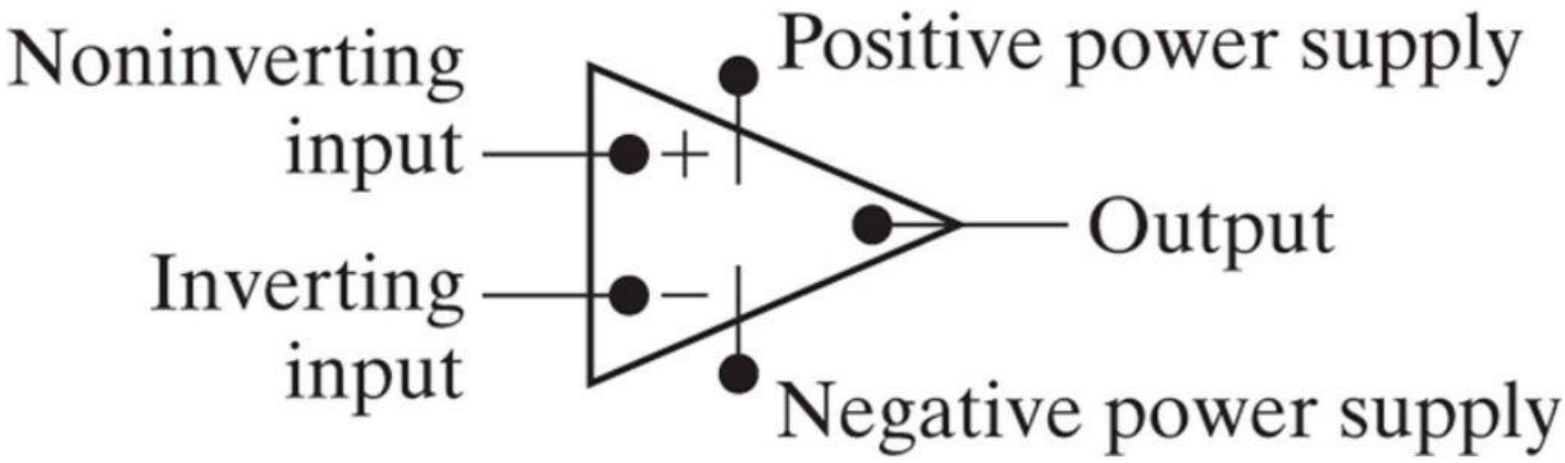


7.72. Consider the source follower shown in Fig. 7.94. The circuit must provide a voltage gain of 0.6 at 100 MHz. Design the circuit such that the dc voltage at node X is equal to $V_{DD}/2$. Assume the input impedance exceeds 20 kΩ.

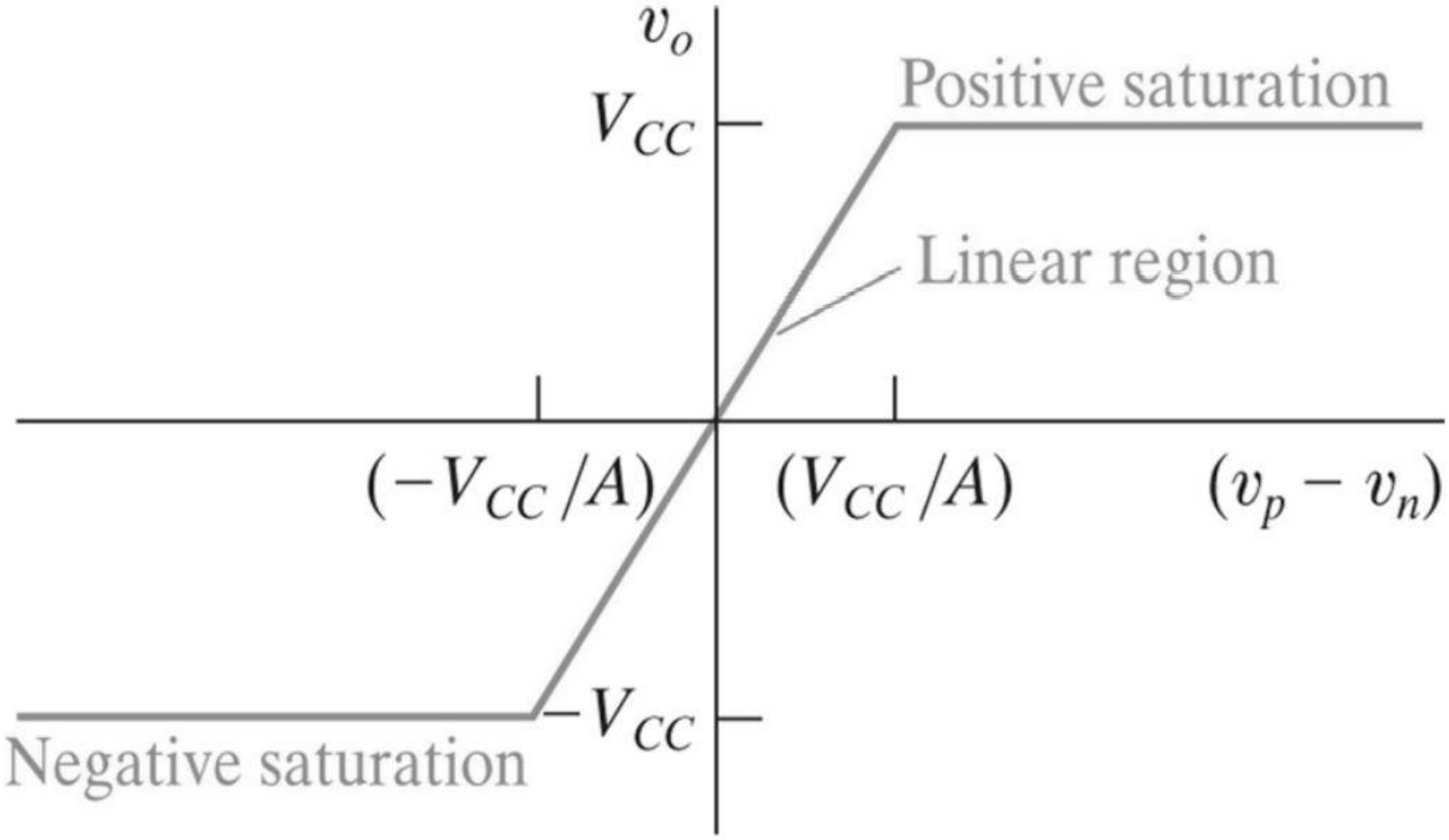


Chapter 8: Operational amplifier: Ideal configurations

Recall:


Noninverting input
Inverting input
Positive power supply
Output
Negative power supply
+
–

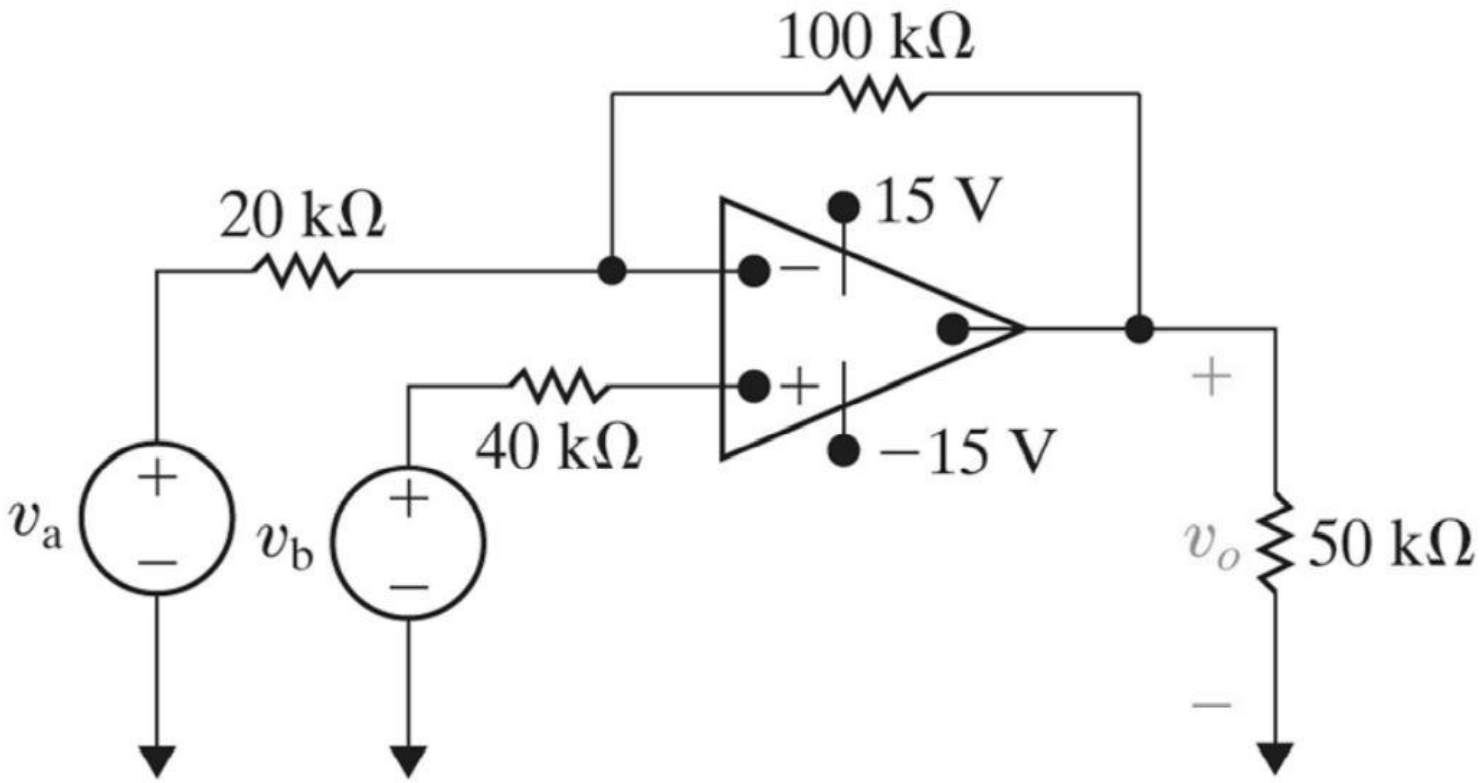
Recall:


v_o
V_{CC}
Positive saturation
Linear region
$(-V_{CC}/A)$
(V_{CC}/A)
$(v_p - v_n)$
$-V_{CC}$
Negative saturation

Problem 1:

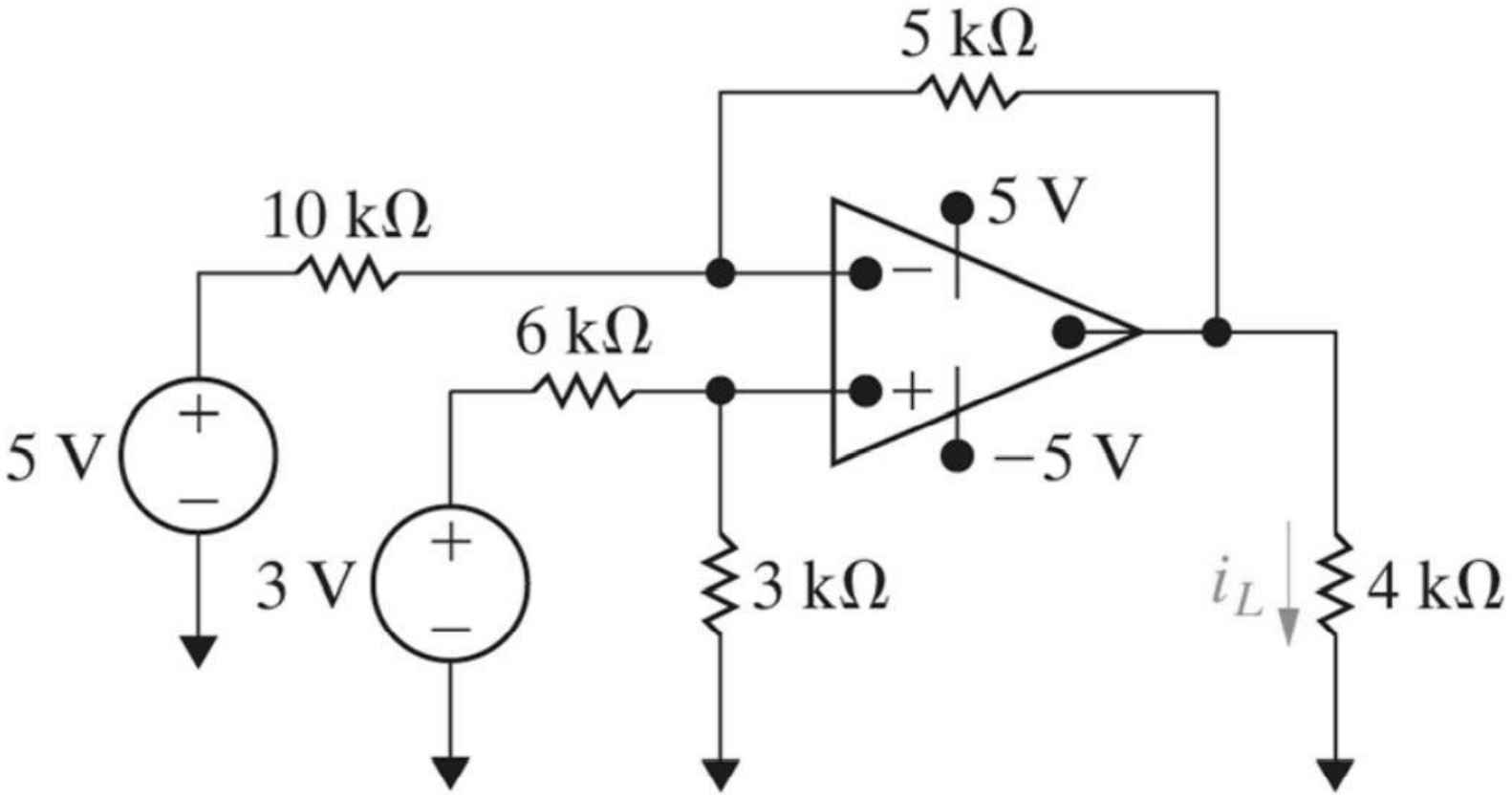
The op-amp in the figure below is ideal.

1. Find v_o if $v_a = 1V$ & $v_b = 2V$.
2. Specify the range of v_a such that the amplifier does not saturate. ($v_b = 1.6V$)



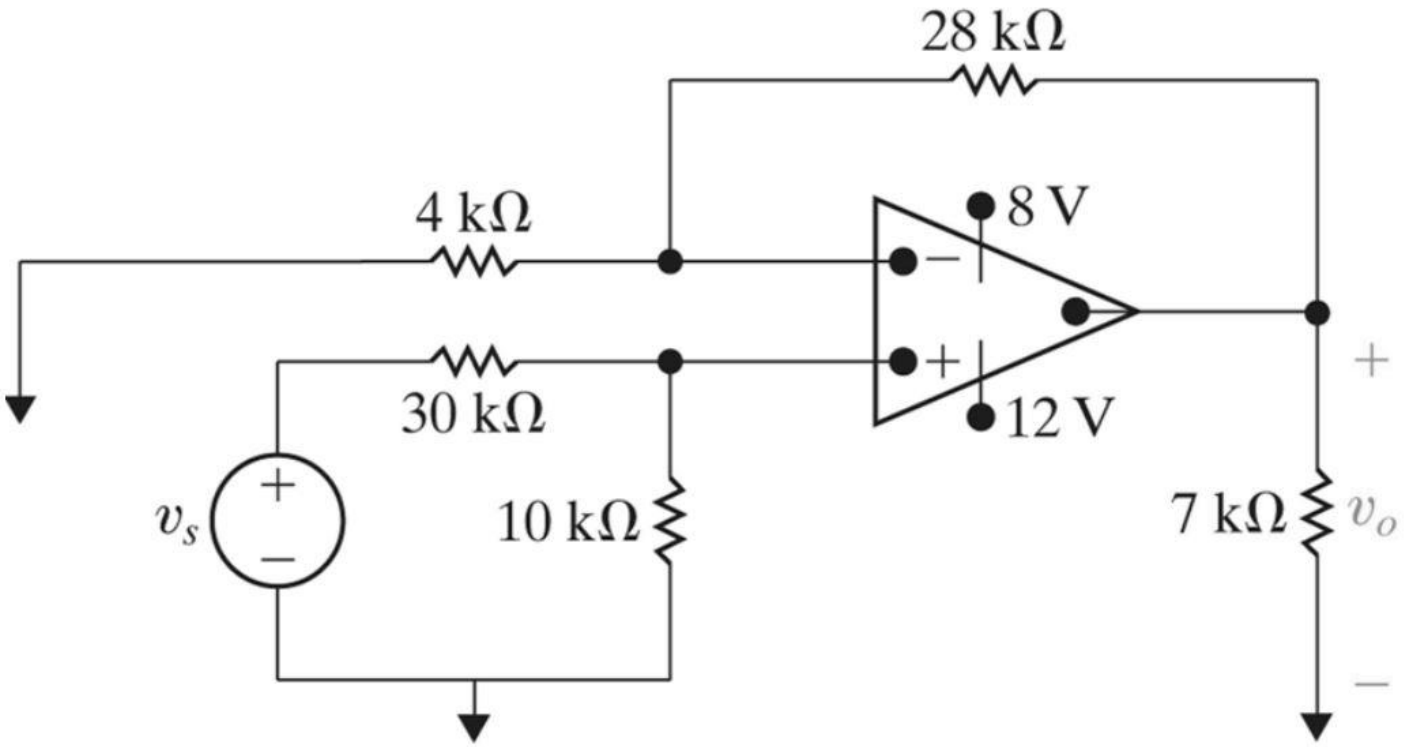
Problem 2:

The op-amp in the figure below is ideal. Find i_L.



Problem 3:

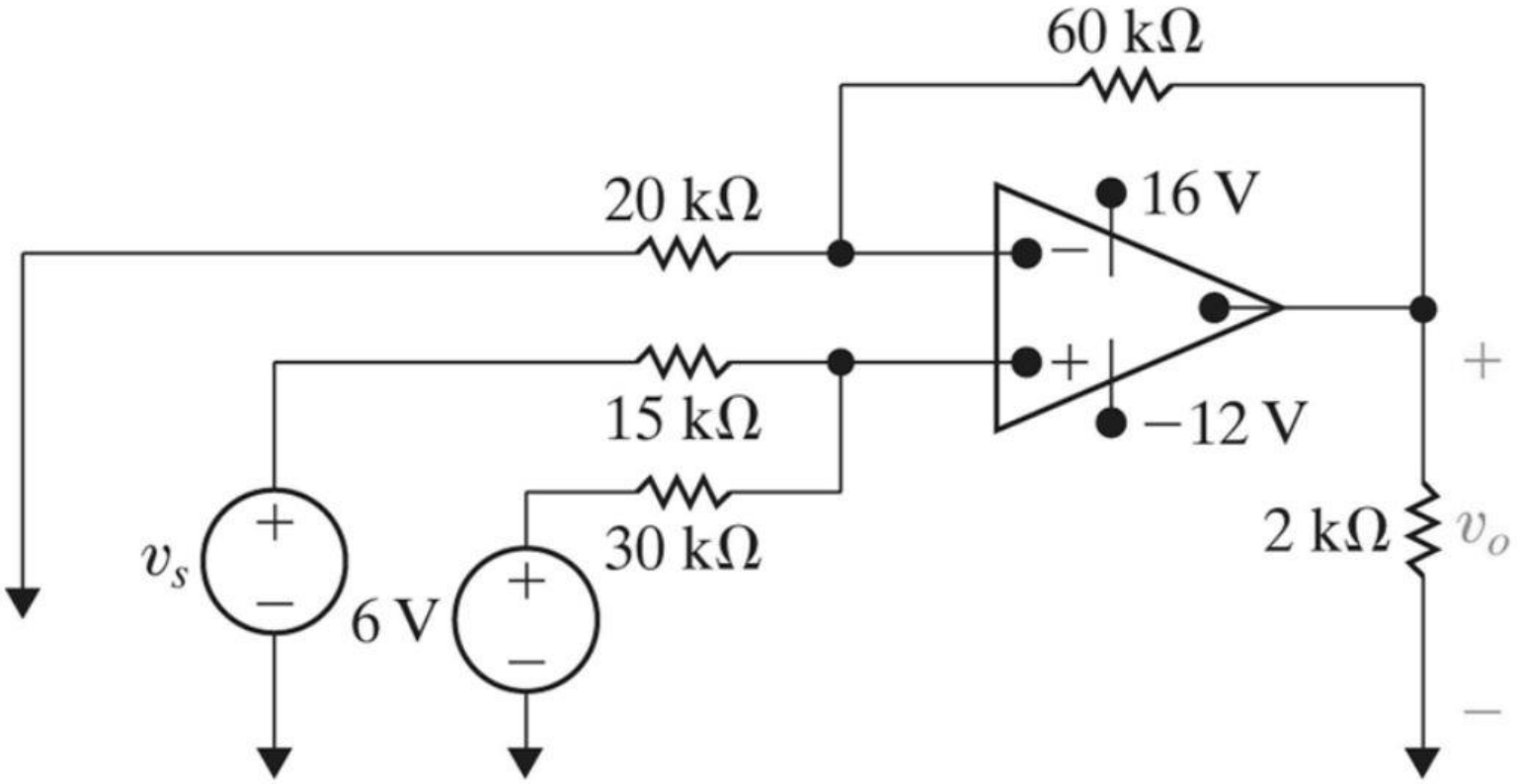
The op-amp in the figure below is ideal.



1. What circuit configuration is shown in this figure?
2. Find v_o in terms of v_s.
3. Find the range of values for v_s such that v_o does not saturate and the op-amp remains in its region of operation.

Problem 4:

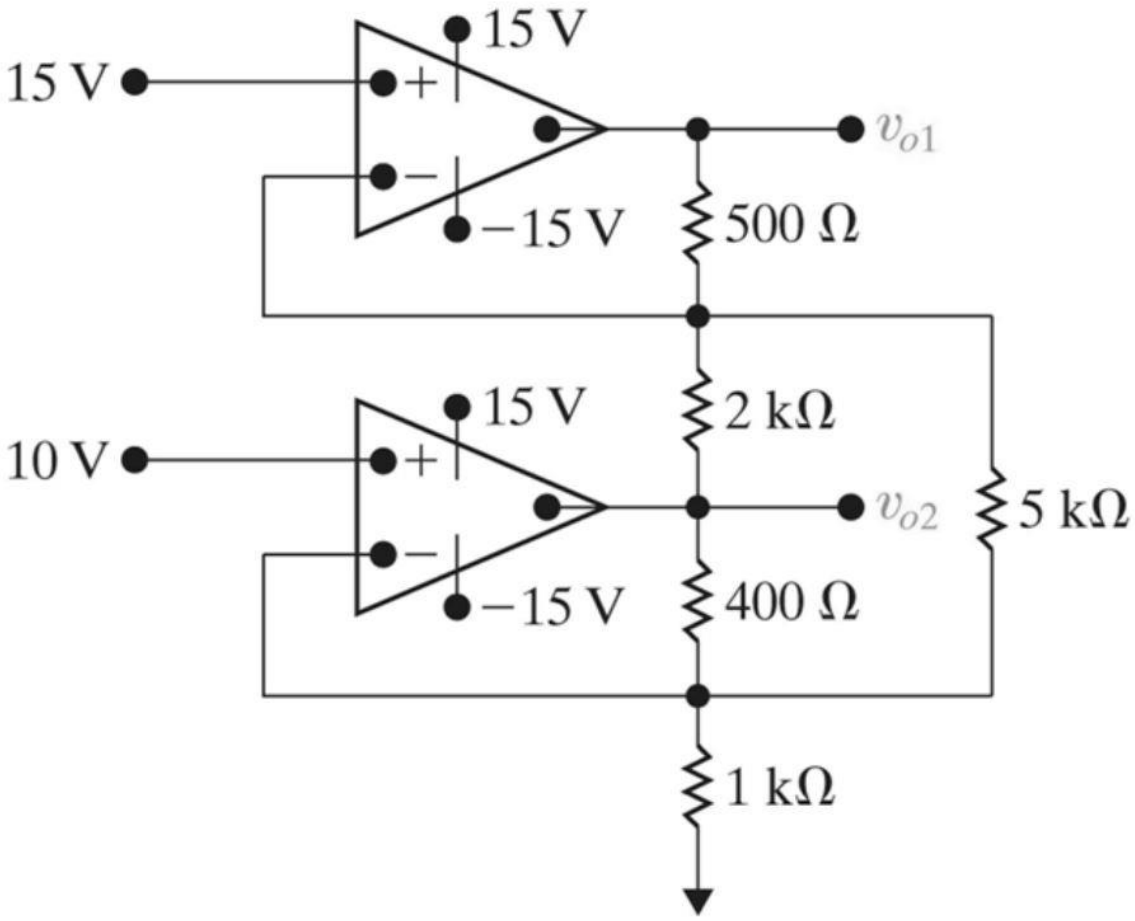
The op-amp in the figure below is ideal.



1. What circuit configuration is shown in this figure?
2. Find v_o in terms of v_s.

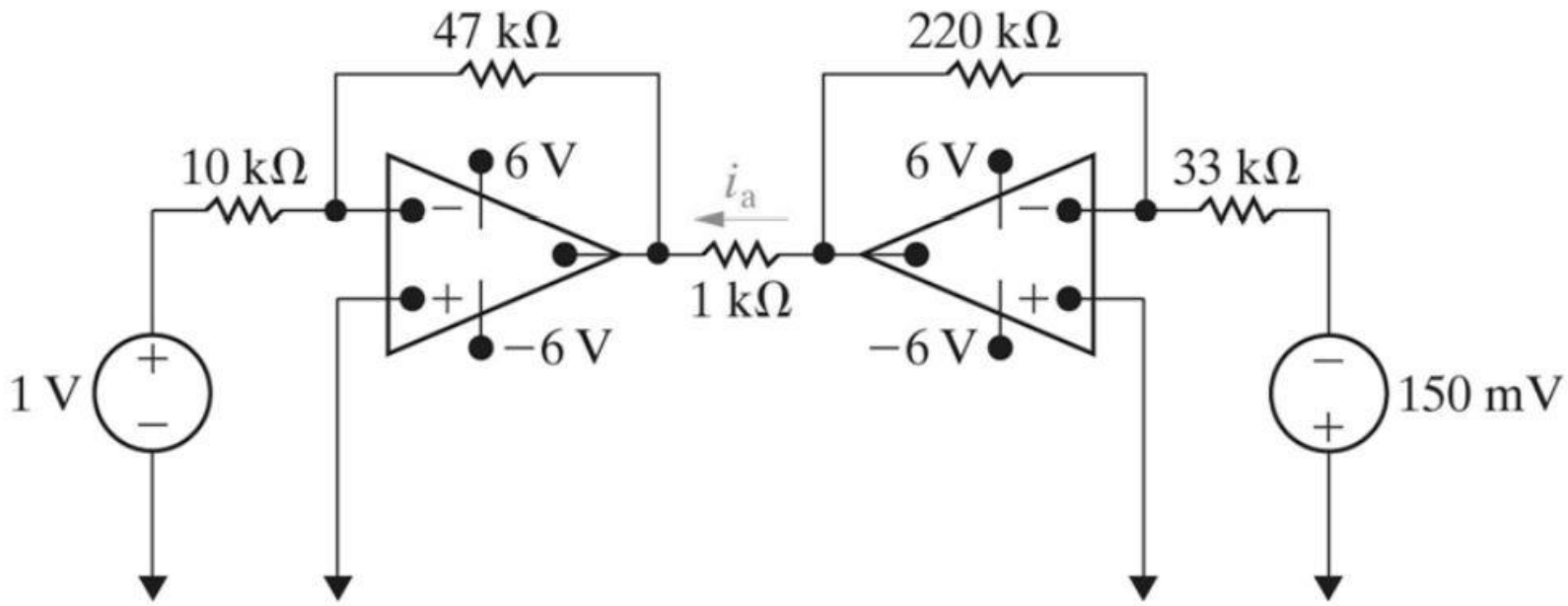
Problem 5:

The op-amps in the figure below are ideal. Calculate v_{o1} & v_{o2}.



Problem 6:

The op-amps in the figure below are ideal. Calculate i_a.



Find the value of the left source voltage for which $i_a = 0$.