Ibraheem El Sheikha

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EDUCATION

University of Toronto **Sept. 2023 – Apr. 2027**
BASc. in Computer Engineering & PEY Co-op *Toronto, Canada*

Relevant courses: *Computer Organization (RISC-V Assembly, Embedded C), Digital Systems (Verilog, FPGA programming), Programming Fundamentals (C++), Computer Fundamentals (C), Signals and Systems (MATLAB, SimuLink), Hardware Design and Communication (Altium, Circuit design, Electrical lab equipment), Introductory Electronics (LTSpice, Circuit building)*

Dean's Honours List (2023, 2024)

TECHNICAL & LEADERSHIP SKILLS

Software: Python, C/C++, JavaScript, RISC-V Assembly, HTML/CSS, MATLAB, Simulink

Hardware: Verilog, FPGA Programming, ModelSim, Arduino, Circuit design/analysis, Oscilloscope, Multimeter, LTSpice, Altium, KiCAD, Soldering, PyVISA

Leadership Skills: Teamwork, Communication, Collaboration, Problem-solving, Analytical thinking

EXPERIENCE

AI & NLP Research Assistant | University of Toronto ECE **Apr. 2025 – Present**

- Under the supervision of Prof. Salma Emara, building a **Chrome extension** for Piazza that leverages **AI and NLP** to capture student questions in real time and surfaces the top-N most relevant past discussions for immediate reference
- Implementing **semantic searching** by applying **transformer-based sentence embeddings** and **cosine similarity** ranking to match new queries with existing threads, ensuring **high-precision** recommendations
- **Awarded** Edgar McAllister Foundation Undergraduate Summer Research Fellowship

PCB Engineering Intern | Jitterware Inc. **Feb. 2025 – Mar. 2025**

- Designed and developed a **multilayer distortion pedal PCB** prototype in **KiCAD** for an electric guitar, complete with a power supply, gain knob, volume control, and tone control
- Selected/placed components in a BOM and optimized board dimensions/routing to reduce PCBA cost to **less than $20 CAD**

PROJECTS

Software-Defined Radio Receiver | Altium, LTSpice, PyVISA **Jan 2025 – Apr. 2025**

- Using **agile development**, led a team of three to design and manufacture a **RX receiver** for a flexible radio transceiver, with an emphasis on **power efficiency**
- Designed a 8-16 MHz **bandpass filter**, a ±0.7 V **limiter circuit**, a **diode ring quadrature mixer**, a 96 kHz cutoff **lowpass filter**, and a 32 db gain **amplifier**
- Simulated all subcomponents in **LTSpice** ensuring they meet the interface control document requirements
- Created and manufactured a **multilayer PCB** in **Altium** and routed traces to minimize heat loss, tested using **oscilloscope, waveform generator, power supply, DMM**, and the **PyVISA** Python module

Embedded C Reversi | Embedded C, RISC-V Assembly **Mar. 2025 – Apr. 2025**

- Developed a **real-time** multiplayer Reversi game in **embedded C** on a **RISC-V processor** running on the **DE1-SoC FPGA**, interfacing a PS/2 mouse and VGA display through **memory-mapped ports**
- Implemented and optimized a **60 FPS VGA graphics** pipeline via direct memory-mapped framebuffer and register access, rendering dynamic game elements: scoreboard, current-player indicator, legal-move highlights, and winner display
- Developed comprehensive **firmware game logic** (move validation, score tracking, win-condition detection), demonstrating seamless **hardware–software co-design** and efficient resource utilization

Homemade RISC-V CPU | Verilog, ModelSim, Quartus, FPGA Programming **Oct. 2024 – Dec. 2024**

- Collaborated with a teammate to implement and debug a **RISC-V CPU from scratch** using **Verilog** and **Quartus Prime Lite**, debugged in **ModelSim**
- Capable of executing **core instructions** (addi, add, sub, xor, and, or, sw, lw, beq, bne)
- Implemented **memory arbitration logic** to manage access between the CPU and **VGA display** that displays register values in **real-time**