Ibraheem El Sheikha

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EDUCATION

University of Toronto   **Sept. 2023 – Apr. 2027**
Computer Engineering (BASc) & PEY Co-op   *Toronto, Canada*

Relevant courses: *Computer Organization (RISC-V Assembly, Embedded C), Digital Systems (Verilog, FPGA programming), Programming Fundamentals (C++), Computer Fundamentals (C), Operating Systems (Linux), Data Structures and Algorithms, Digital Electronics*

Dean's Honours List (2023, 2024)

TECHNICAL & LEADERSHIP SKILLS

Software: C, C++, Python, RISC-V Assembly, HTML/CSS, MATLAB, Simulink

Hardware: Verilog, FPGA Programming, ModelSim, Arduino, Circuit design/analysis, Oscilloscope, Multimeter, LTSpice, Altium, KiCAD, Soldering, PyVISA

Leadership Skills: Teamwork, Communication, Collaboration, Problem-solving, Analytical thinking

EXPERIENCE

Software Research Intern | University of Toronto ECE   **May 2025 – Present**

- Developed **PiazzaPlus**, a **Chrome extension** for Piazza with a **Flask backend** that enhanced Piazza by enabling students to discover relevant discussions faster through **hybrid semantic + BM25** search.
- **Improved** search quality by **120% in MAP** and **152% in MRR** over Piazza's native search.
- **Awarded** Edgar McAllister Fellowship (**1 of 2 recipients** from all 1st to 3rd year ECE applicants at UofT)

PCB Engineering Intern | Jitterware Inc.   **Feb. 2025 – Mar. 2025**

- Designed and developed a **multilayer distortion pedal PCB** prototype in **KiCAD** for an electric guitar, complete with a power supply, gain knob, volume control, and tone control
- Selected components in a BOM and optimized routing for a PCBA cost of **under $20 CAD**

PROJECTS

Software-Defined Radio Receiver | Altium, LTSpice, PyVISA   **Jan 2025 – Apr. 2025**

- Using **agile development**, led a team of three to design and manufacture a **RX receiver** for a flexible radio transceiver, with an emphasis on **power efficiency**
- Designed a 8-16 MHz **bandpass filter**, a ±0.7 V **limiter circuit**, a **diode ring quadrature mixer**, a 96 kHz cutoff **lowpass filter**, and a 32 db gain **amplifier**
- Simulated all subcomponents in **LTSpice** ensuring they meet the interface control document requirements
- Created and manufactured a **multilayer PCB** in **Altium** and routed traces to minimize heat loss, tested using **oscilloscope, waveform generator, power supply, DMM**, and the **PyVISA** Python module

Embedded C Reversi | Embedded C, RISC-V Assembly   **Mar. 2025 – Apr. 2025**

- Developed a **real-time** multiplayer Reversi game in **embedded C** on a **RISC-V processor** running on the **DE1-SoC FPGA**, interfacing a PS/2 mouse and VGA display through **memory-mapped ports**
- Implemented and optimized a **60 FPS VGA graphics** pipeline via direct **memory-mapped framebuffer** and register access, rendering dynamic game elements: scoreboard, current-player indicator, legal-move highlights, and winner display
- Developed comprehensive **firmware game logic** (move validation, score tracking, win-condition detection), demonstrating seamless **hardware–software co-design** and efficient resource utilization

Custom RISC-V CPU | Verilog, ModelSim, Quartus, FPGA Programming   **Oct. 2024 – Dec. 2024**

- Collaborated with a teammate to implement and debug a **RISC-V-inspired CPU from scratch** using **Verilog** and **Quartus Prime Lite**, debugged in **ModelSim**
- Designed and implemented a robust **VGA display interface**, including **memory arbitration logic** and direct framebuffer management
- Developed the Arithmetic Logic Unit (**ALU**) to handle **core instructions** (addi, add, sub, xor, and, or, sw, lw, beq, bne)