

IBRAHEEM EL SHEIKHA

☎ (416) 804 5570 ✉ ibraheem.elsheikha@mail.utoronto.ca  [Ibraheem El Sheikha](#)  [Personal Portfolio](#)

EDUCATION

University of Toronto

Computer Engineering (BASc) & PEY Co-op

Sept. 2023 – Apr. 2027

Toronto, Canada

Relevant courses: *Computer Organization (RISC-V Assembly, Embedded C), Digital Systems (Verilog, FPGA programming), Programming Fundamentals (C++), Computer Fundamentals (C), Signals and Systems (MATLAB)*

Dean's Honours List (2023, 2024)

TECHNICAL & LEADERSHIP SKILLS

Software: C, C++, Python, RISC-V Assembly, HTML/CSS, MATLAB, Simulink

Hardware: Verilog, FPGA Programming, ModelSim, Arduino, Circuit design/analysis, Oscilloscope, Multimeter, LTSpice, Altium, KiCAD, Soldering, PyVISA

Leadership Skills: Teamwork, Communication, Collaboration, Problem-solving, Analytical thinking

EXPERIENCE

AI & NLP Researcher | University of Toronto ECE

Apr. 2025 – Present

- Under the supervision of Prof. Salma Emara, engineering a **Python pipeline** integrating **hybrid semantic and keyword-based** search for real-time Piazza query handling
- Implementing **semantic searching** by applying **transformer-based sentence embeddings** and **cosine similarity** ranking through a **vector database** to match new queries with existing threads, coupled with **BM25 keyword search**
- **Awarded** Edgar McAllister Fellowship (1 of 2 recipients from all second to fourth-year ECE applicants)

PCB Engineering Intern | Jitterware Inc.

Feb. 2025 – Mar. 2025

- Designed and developed a **multilayer distortion pedal PCB** prototype in **KiCAD** for an electric guitar, complete with a power supply, gain knob, volume control, and tone control
- Selected components in a BOM and optimized routing for a PCBA cost of **under \$20 CAD**

PROJECTS

Software-Defined Radio Receiver | Altium, LTSpice, PyVISA

Jan 2025 – Apr. 2025

- Using **agile development**, led a team of three to design and manufacture a **RX receiver** for a flexible radio transceiver, with an emphasis on **power efficiency**
- Designed a 8-16 MHz **bandpass filter**, a ± 0.7 V **limiter circuit**, a **diode ring quadrature mixer**, a 96 kHz cutoff **lowpass filter**, and a 32 db gain **amplifier**
- Simulated all subcomponents in **LTSpice** ensuring they meet the interface control document requirements
- Created and manufactured a **multilayer PCB** in **Altium** and routed traces to minimize heat loss, tested using **oscilloscope**, **waveform generator**, **power supply**, **DMM**, and the **PyVISA** Python module

Embedded C Reversi | Embedded C, RISC-V Assembly

Mar. 2025 – Apr. 2025

- Developed a **real-time** multiplayer Reversi game in **embedded C** on a **RISC-V processor** running on the **DE1-SoC FPGA**, interfacing a PS/2 mouse and VGA display through **memory-mapped ports**
- Implemented and optimized a **60 FPS VGA graphics** pipeline via direct **memory-mapped framebuffer** and register access, rendering dynamic game elements: scoreboard, current-player indicator, legal-move highlights, and winner display
- Developed comprehensive **firmware game logic** (move validation, score tracking, win-condition detection), demonstrating seamless **hardware-software co-design** and efficient resource utilization

Custom RISC-V CPU | Verilog, ModelSim, Quartus, FPGA Programming

Oct. 2024 – Dec. 2024

- Collaborated with a teammate to implement and debug a **RISC-V-inspired CPU from scratch** using **Verilog** and **Quartus Prime Lite**, debugged in **ModelSim**
- Designed and implemented a robust **VGA display interface**, including **memory arbitration logic** and direct framebuffer management
- Developed the Arithmetic Logic Unit (**ALU**) to handle **core instructions** (addi, add, sub, xor, and, or, sw, lw, beq, bne)