

Micro and Nanofabrication (MEMS)

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وقرأت بـ زدن علماً

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محمد

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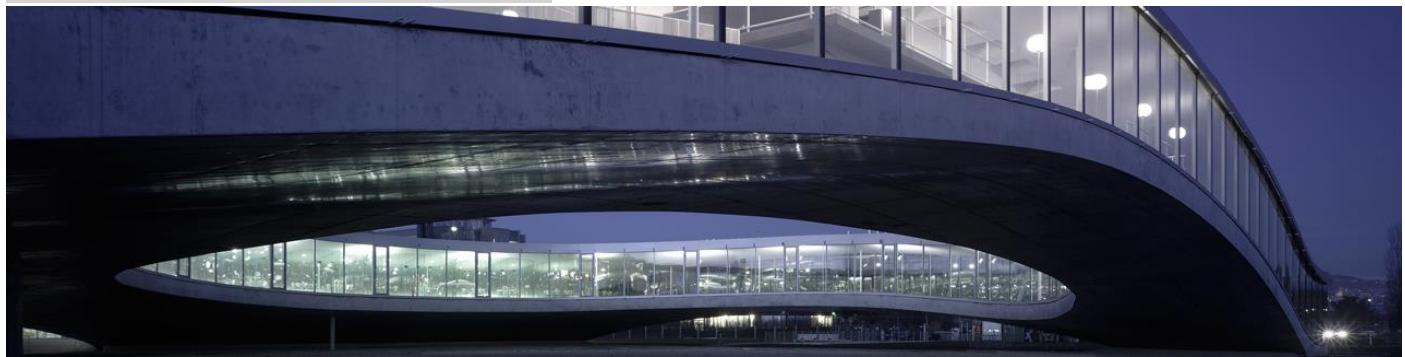


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- "Self Study" Aerospace Engineering .Tu Delft university and NPTEL
- "Self Study".....More



About this course



Micro and Nanofabrication (MEMS)

Learn the fundamentals of microfabrication and nanofabrication by using the most effective techniques in a cleanroom environment....Microfabrication and nanofabrication are the basis of manufacturing for nearly all modern miniaturized systems that are ubiquitously used in our daily life. Examples include; computer Chips and integrated sensors for monitoring our environment, cars, mobile phones, medical devices And more. Micro--- and nanofabrication can be taught to students and professionals by textbooks and ex--- cathedra lectures, but the real learning comes from seeing the manufacturing steps as they happen. In this engineering course, we will go a step beyond classroom teaching to not only explain the basics of each fabrication step but also show you how it's done through Section sequences and zooming into the equipment.

What you'll learn

- How to select the correct fabrication process for a specific micro-device or microsystem
- Establish the workflow for the cleanroom processes
- Identify how physical and chemical phenomena govern miniaturized systems for various applications
- Resource planning for a given microsystem fabrication

Teaser

Welcome to our “mooc” in micro and nano fabrication. My name is Juergen Brugger and I am one of the co-authors and teachers of this “mooc”. My name is Martin Gijs and I am the second co-author and teacher of this “mooc”. Together we will show you in the following lectures the basics of micro and nano fabrication techniques. We will show you in particular how they are carried out in a typical clean room environment. Today, we are constantly using micro devices so called MEMS that help us communicating and navigating measure our health parameters such as blood pressure and glucose level, monitor and control automotive safety parameters, such as airbags and tyre pressure, enable us to enjoy realistic augmented reality and video gaming etc These devices are ubiquitously available today because they can be fabricated in large volumes and cost efficiently The goal of this course is to introduce you to the fundamentals of the fabrication techniques that are behind these success stories which actually have enabled them. After this introduction, we would give you chapter by chapter the theoretical basis to understand the principal mechanisms of thin film deposition, lithography, etching and other techniques. Each chapter is completed by illustrations and examples so that you can clearly see the link between a particular fabrication step and the resulting functionality in the micro device During this “ mooc” lectures, I will first show some well known MEMs devices that we are using in our everyday life I will be showing particular how micro and nano fabrication has enabled their manufacturing in high volumes and at low cost. I will then take over to show you how a clean room is designed and operated to ensure that the fabricated MEMs devices are as clean as possible. We both we then follow up by describing the basics of the various fabrication steps such as thin film formation, lithography as well as etching. We hope that you enjoyed our “mooc” lecture. So let's get started!

Course structure

The course is structured into 7 Chapters:

Chapter 1: MEMS and cleanroom introduction

This module introduces the basics of micro-electromechanical systems (MEMS) and cleanroom fabrication. In a first part, the working principle of three successful MEMS devices, which are accelerometers, microphones and bulk acoustic wave resonators, are presented. Then a case study about the bimorph microactuator goes through each microfabrication step required to fabricate such a device. Finally, the last part explains you the basic principles of a cleanroom, the possible contamination sources, and gives you an overview of our cleanroom facilities on the campus.

Chapter 2: Chemical vapor deposition (CVD)

This module on chemical vapor deposition or CVD describes in detail basic principles of CVD and will show you the cleanroom infrastructure that is used to run a CVD process. CVD techniques at different operating pressures will be introduced, like atmospheric pressure CVD or APCVD, sub-atmospheric pressure CVD or SACVD, followed by low pressure CVD or LPCVD, and finally ultrahigh vacuum/CVD for the lowest pressure used. Next we will discuss a technique called plasma-enhanced CVD or PECVD and finally the technique metal-organic CVD or MOCVD. Atomic layer deposition or ALD will be introduced, which is a technique in which a thin film is deposited atomic layer-by-atomic layer, as well as the thermal oxidation process of silicon. We will introduce important theoretical concepts that play a role in CVD, like the velocity and concentration boundary layer near a substrate. We will subsequently present a theoretical model for the CVD film growth. Finally, specific CVD deposition processes will be introduced for depositing poly-crystalline and amorphous silicon, silicon oxide, silicon nitride, diamond and metal films.

Chapter 3: Physical vapor depositon (PVD)

This module on physical vapor deposition describes in details the two main PVD methods; thermal evaporation and sputtering. Physical principles, setups configurations, process parameters, deposited films properties, advantages and limitations, as well as examples are introduced and discussed for these two techniques. In addition, an overview of some alternative techniques such as ion assisted deposition, molecular beam epitaxy and pulsed laser depositon is also presented. Finally, thin films growth process on the substrate is also discussed.

Chapter 4: Lithography

This module on lithography describes in details the two main resist patterning methods: optical and electron beam lithography. Physical principles, setup configurations, process parameters, resist properties, advantages and limitations, as well as examples are introduced and discussed for these two techniques. In addition, an overview of some alternative techniques such as nanoimprint lithography or thermal scanning probe lithography is also presented.

Chapter 5: Dry etching (DE)

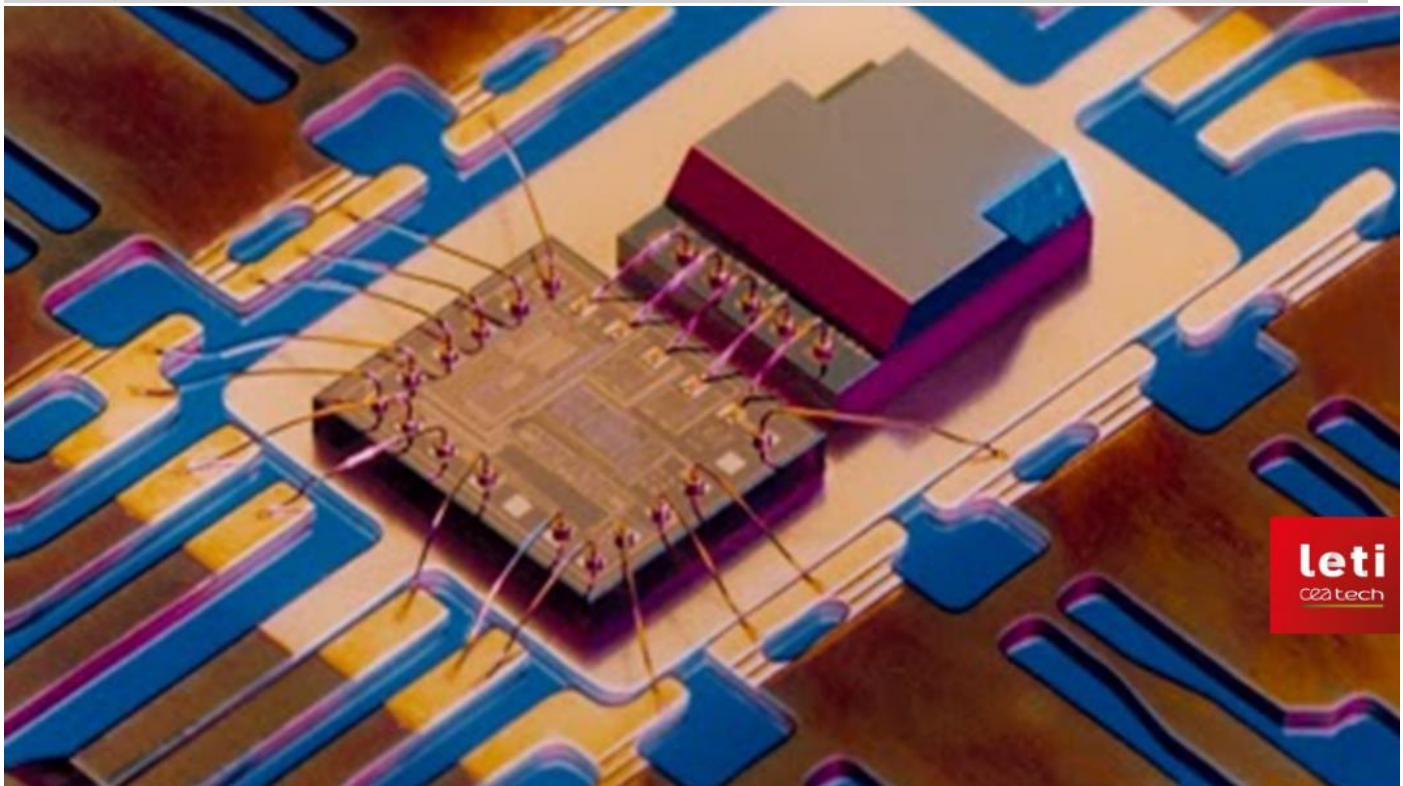
This module on dry etching describes etching in a gas environment. We will introduce etching directionality and anisotropy and give a few simple rules for choosing dry etching processes for specific materials in a plasma reactor and provide theoretical concepts that characterize a plasma in a dry etching equipment. We will discuss current dry etching reactors and ion beam etchers; in the latter, the substrate to be etched is not located within the plasma, but subjected to a beam of ions. We will present also dry etching processes that use intrinsically reactive gases and that do not require to have the gas in the plasma state, which leads to a significantly simpler etching system. We will finally give examples of specific dry etching processes for silicon dioxide, silicon nitride, silicon, polymers and metals.

Chapter 6: Wet etching (WE)

This module on wet etching describes etching in a liquid environment. We will introduce anisotropic wet etching of silicon substrates, where certain lattice planes are etched and others not, isotropic etching of silicon, and finally thin membrane microfabrication techniques using wet etching. We will also explain the hydrofluoric acid or HF bath that is used for silicon dioxide and glass wet etching. We will discuss applications of wet etching, like wafer cleaning and removal of sacrificial layers underneath a functional layer to realize free-standing structures. We will illustrate the potential of anisotropic etching for bulk micromachining, which is microfabrication by etching through bulk parts of a wafer. Finally, we will discuss electrochemical etching of silicon substrates for making porous silicon.

Chapter 7: Inspection and metrology

This module describes methods of inspection and metrology based on four technique categories: optical, mechanical, charged beam and electrical. Physical principles, setup configurations, advantages and limitations are introduced and discussed for various inspection and metrology methods. The MEMS bi-morph thermal actuator introduced in the first week is taken as the example for demonstration of each method. In addition, the comparison of measurement or inspection results obtained from different methods is also presented.



Introduction and objectives

This module introduces the basics of micro-electromechanical systems (MEMS) and cleanroom fabrication. In a first part, the working principle of three successful MEMS devices, which are accelerometers, microphones and bulk acoustic wave resonators, are presented. Then a case study about the bimorph microactuator goes through each microfabrication step required to fabricate such a device. Finally, the last part explains you the basic principles of a cleanroom, the possible contamination sources, and gives you an overview of our cleanroom facilities on the campus.

At the end of this chapter, you should be able to:

- Know the operation principle of a few selected commercially successful MEMS products.
- Understand in particular how micro fabrication has enabled that these miniature transducer systems can be fabricated with cost-efficient methods.
- Give a flavour of how some basic transducer functions can be designed and integrated into devices. Remember how a bi-morph micro-actuator is fabricated and characterised.
- Be aware of the different contamination problems that may arise when one wants to develop a microfabrication process in a cleanroom.
- Know different options for creating an environment with clean air and for cleanroom construction and know how to quantify the degree of cleanliness.

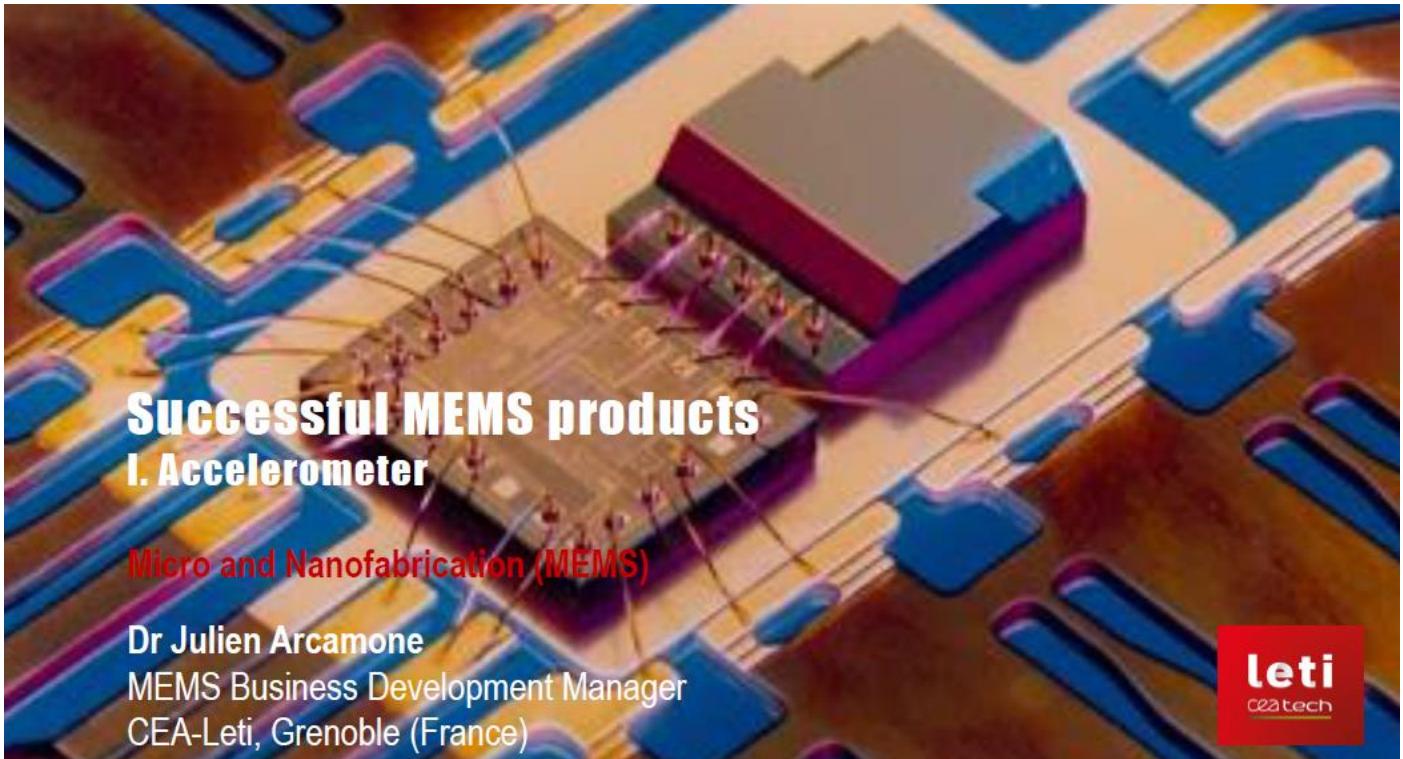
Intro quiz

Questions:

1. Describe what is the physical principle of thermo-mechanical micro-actuators?

- A difference in the Young's modulus of the two materials
- Specific shapes of the two materials
- A difference in the electrical conductivity of the two materials
- A difference in the thermal expansion coefficient of the two materials

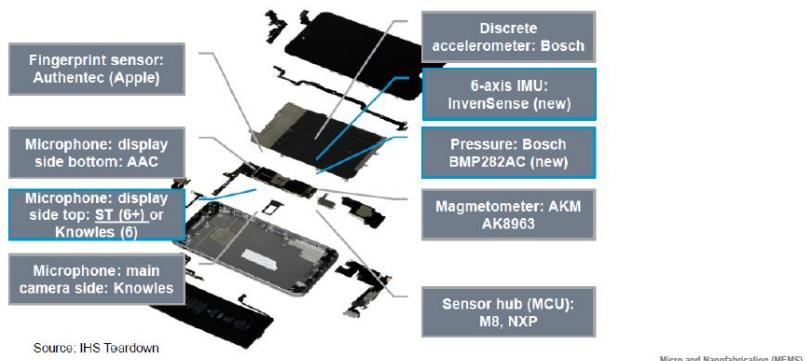
2. A possible operating principle for micromechanical pressure sensors is to detect the capacitance change resulting from the displacement of a movable electrode after a pressure variation. Assuming a sensor consists of a 1 mm^2 movable highly doped silicon electrode and a $1 \mu\text{m}$ air gap as dielectric. If a 0.1 pF capacitance increase is measured when pressing on the device (i.e. gap reduction), what is the corresponding displacement of the movable capacitor electrode in nanometers (absolute value)?



- Welcome to this lesson on MEMS success Stories .

Successful MEMS products that we use every day

- MEMS are now ubiquitous in our daily life

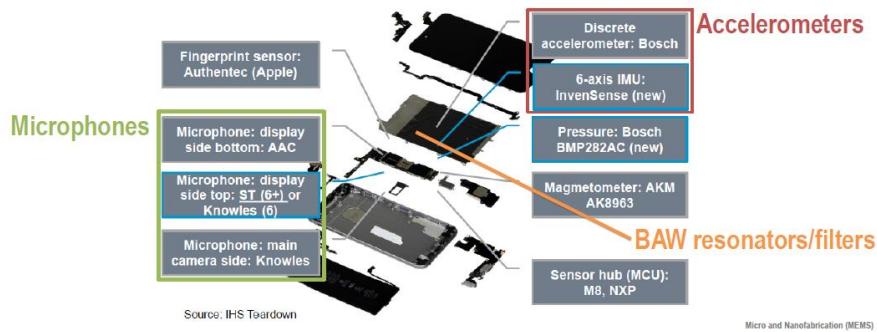


Dr Julien Arcamone ,MEMS Business Development Manager ,CEA-Leti, Grenoble (France)

Before we go into detail of the various micro nanofabrication methods, let's have a quick look what MEMS are and how we are actually using them day by day. We have invited for this lesson a guest lecturer who is a real expert in the field, so let me introduce Dr. Julien Arcamone. He is responsible for the industrial partnerships and business development in MEMS within the Silicon Components Division of CEA-LETI in Grenoble, France, one of the largest MEMS R&D centers and foundries. Julien will show you some selected MEMS examples, he will in particular highlight how micro fabrication has enabled such systems to become so performing and cost efficient to manufacture. So Julien, the floor is yours !- Thank you Jurgen for the

Successful MEMS products that we use every day

- MEMS are now ubiquitous in our daily life
- 3 focuses in this course

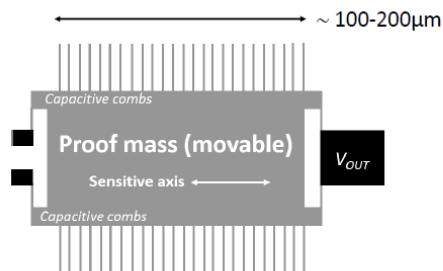


Dr Julien Arcamone ,MEMS Business Development Manager ,CEA-Leti, Grenoble (France)

introduction. Hello, it's my honor and pleasure to give this lesson on successful MEMS products. Let's start right away ! So maybe not everyone has noticed yet but MEMS have become ubiquitous in our daily life. One example is a multiplicity of MEMS devices inside smartphones. This scheme depicts a tear down view of the iPhone 6 and the various MEMS devices present inside it. In this lesson, I would like to focus on 3 applications. First accelerometers, so acceleration sensors. Second, microphones Third, BAW resonators and filters BAW stands for Bulk Acoustic Wave Resonators. Let's start with the accelerometers.

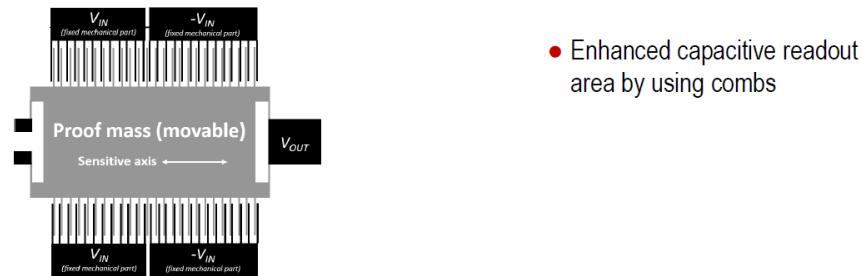
Example 1: Accelerometers

- Most classical device: **capacitive comb-drive accelerometers**
- Physical principle: capacitance variation induced by acceleration



Example 1: Accelerometers

- Most classical device: **capacitive comb-drive accelerometers**
- Physical principle: capacitance variation induced by acceleration



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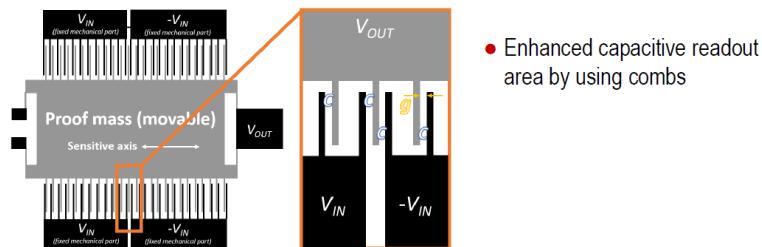
Technically speaking, the most classical device is a capacitive comb-drive accelerometer with electrostatic actuation and capacitive detection by means of a set of lateral combs. The physical principle

is rather simple. This sensor detects a capacitance variation induced by an acceleration. Let's illustrate how this device works.

Example 1: Accelerometers



- Most classical device: **capacitive comb-drive accelerometers**
- Physical principle: capacitance variation induced by acceleration



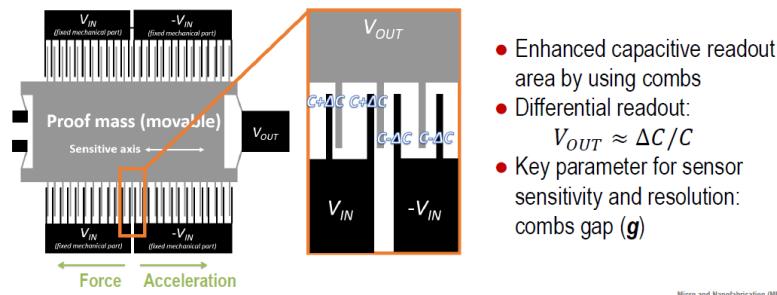
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This scheme depicts a top view of a proof mass, which is sensitive to accelerations along the x-axis. This proof mass acts as an inertial mass. It can move laterally and is anchored in 4 points. In this picture, the movable suspended parts are in grey, the anchored or fixed ones are in black. Typically a proof mass is between 100 and 200 microns wide and long. This proof mass is equipped with a set of lateral comb fingers. They all have an opposite and mechanically fixed comb finger.

Example 1: Accelerometers



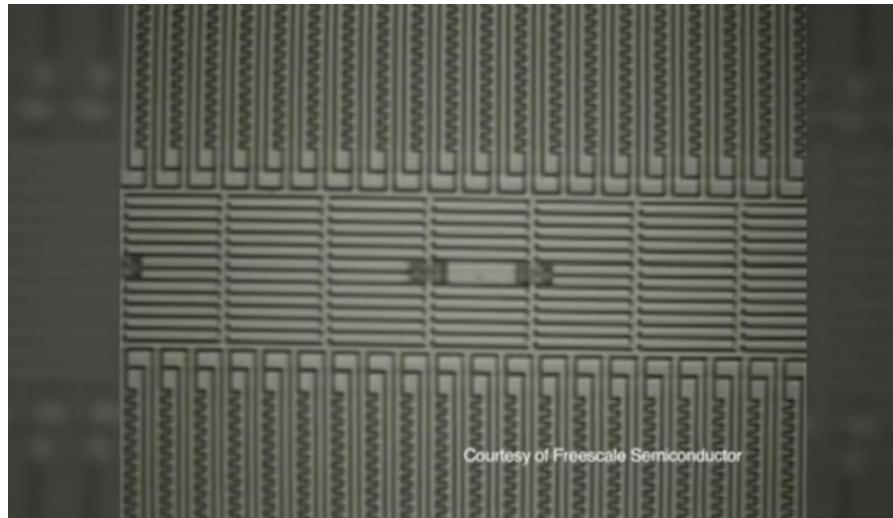
- Most classical device: **capacitive comb-drive accelerometers**
- Physical principle: capacitance variation induced by acceleration



Micro and Nanofabrication (MEMS)

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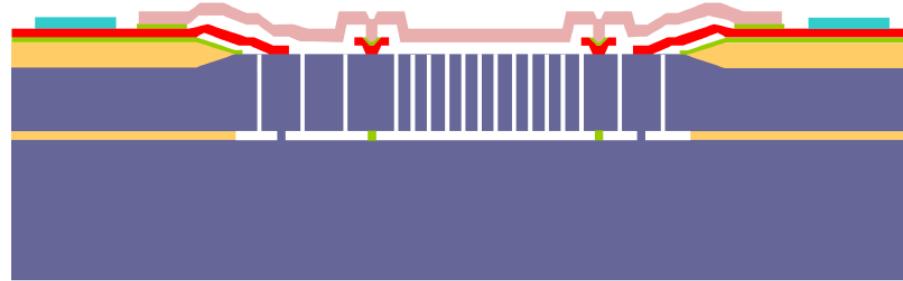
The fact of using combs provides a larger capacitive area which turns into an enhanced capacitive readout. Let's zoom in on a few fingers. In this example, 4 capacitors are depicted. Always a capacitance C, and a gap G. The 2 ones on the left are polarized at plus V IN. The 2 others at minus V IN. Let's suppose for example an acceleration towards the right side. It induces a counter force towards the left which makes the proof mass and its combs move towards the left too. So let's show it again. Consequently as the gap narrows, the capacitance of the 2 left capacitors becomes C plus delta C. The capacitance of the 2 right ones becomes C minus delta C as the gap widens. Overall, this provides a differential readout and the output voltage is approximately equal to delta C over C. The key parameter in terms of sensitivity and resolution, also named "limit of detection", is a gap G which must be minimized as much as possible. It is generally in the range of 1 micron. This section is recorded inside a scanning electron microscope. So the images here are recorded with an increasing zoom. Here you can see the polysilicon structures, with the moving parts, in particular the combs moving in front of the reference electrodes.



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So the motion is the combination of the electrostatic attraction and the restoring force of the springs. Basically here the motion is in the range of a few microns, naturally. This is just an example of layout but of course, many designs are possible to make the same function. Let's take an example of fabrication process of such capacitive accelerometers.

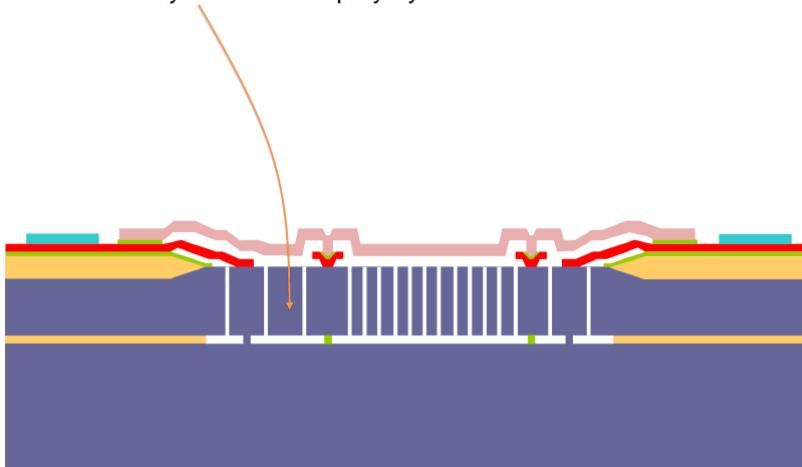
Accelerometers – example of fabrication process



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Accelerometers – example of fabrication process

- MEMS layer: mono- or polycrystalline silicon



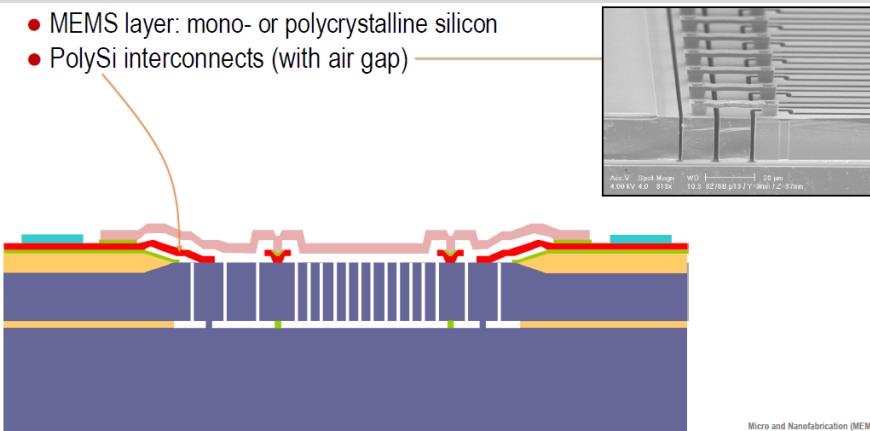
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This scheme depicts a cross sectional view at the end of the process. The MEMS layer can be either a monocrystalline silicon layer, if an SOI substrate is used or a polycrystalline silicon layer, also named "polysilicon". The routing of the mechanical structures is made with partially suspended polysilicon interconnects. the mechanical structures are released by removing the underlying silicon oxide sacrificial layer by wet or vapor HF etching. HF stands for hydrofluoric acid. The MEMS active parts are encapsulated by a polysilicon thin-film packaging which provides an hermetic cavity at ambient pressure protecting the MEMS from moisture, humidity and dust. The input and output signals are brought and picked up through

Accelerometers – example of fabrication process



- MEMS layer: mono- or polycrystalline silicon
- PolySi interconnects (with air gap)



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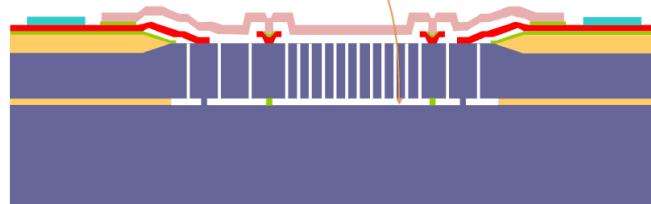
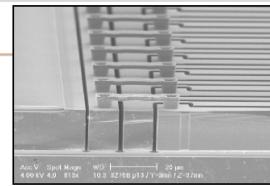
metal pads, here for example. Or here. Let's also mention that some silicon structures are on top of silicon nitride pillars, in order to electrically isolate them from the substrate.

Accelerometers – example of fabrication process

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- MEMS layer: mono- or polycrystalline silicon
- PolySi interconnects (with air gap)
- Final release of mechanical structures by local removal of SiO₂ sacrificial layer



Micro and Nanofabrication (MEMS)

Dr Julien Arcamone, MEMS Business Development Manager, CEA-Leti, Grenoble (France)

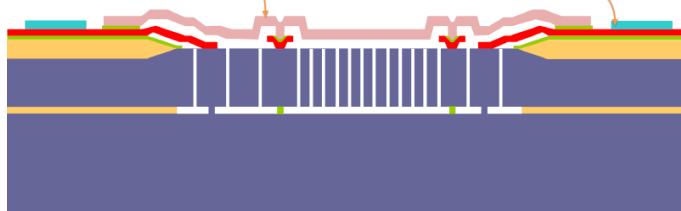
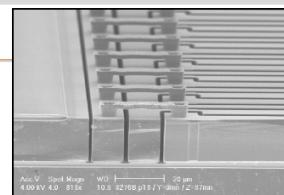
One of the key steps is the Deep Reactive Ion Etching, abbreviated as DRIE, of the silicon MEMS layer. This etching has to provide vertical and smooth side walls with a high aspect ratio of at least 20. The thicker a silicon MEMS layer, the wider is the gap due to the maximum affordable aspect ratio.

Accelerometers – example of fabrication process

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- MEMS layer: mono- or polycrystalline silicon
- PolySi interconnects (with air gap)
- Final release of mechanical structures by local removal of SiO₂ sacrificial layer
- Thin-film packaging (PolySi) and metal pads



Micro and Nanofabrication (MEMS)

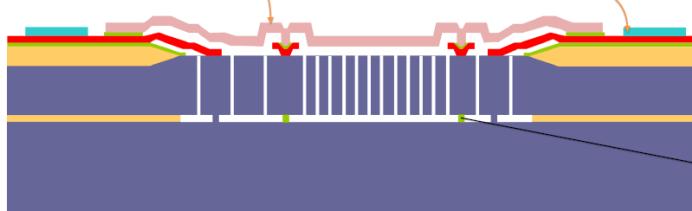
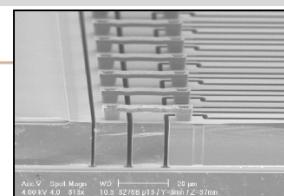
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Accelerometers – example of fabrication process

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- MEMS layer: mono- or polycrystalline silicon
- PolySi interconnects (with air gap)
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- Thin-film packaging (PolySi) and metal pads



Micro and Nanofabrication (MEMS)

Dr Julien Arcamone, MEMS Business Development Manager, CEA-Leti, Grenoble (France)

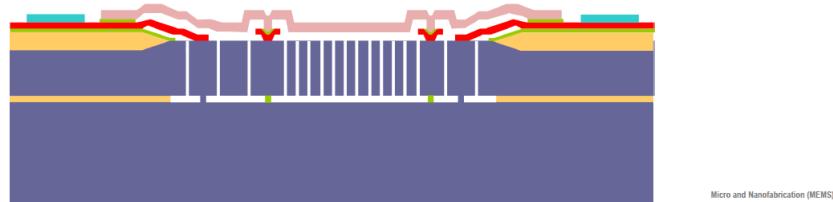
Typically, the silicon MEMS layer is around 20 microns thick and the gap is around 1 micron wide. Let's zoom on a particular area. This scanning electron microscope, abbreviated as SEM, image depicts a set of movable and fixed comb fingers. They feature all the necessary characteristics I mention. They have vertical and smooth side walls and small gaps. So let's talk about application now. First, which MEMS companies sell

these kinds of devices? Let's cite Bosch, STMicro Electronics, InvenSense, Analog Devices, etc. As I mentioned before, accelerometers are present inside smartphones, in particular for screen rotation and for gaming. I like to mention another use case.

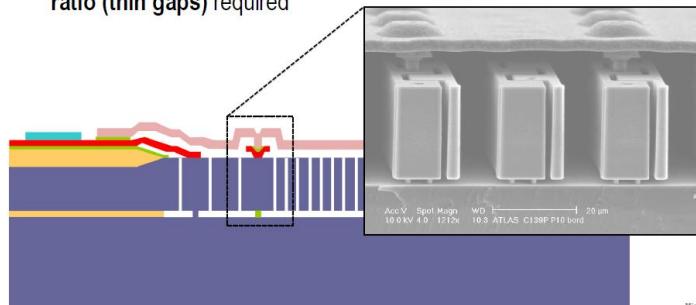
Accelerometers – example of fabrication process



- Critical process module: one of the key steps is the Deep Reactive Ion Etching (DRIE) of the Si MEMS layer → vertical & smooth sidewalls with high aspect ratio (thin gaps) required



- Critical process module: one of the key steps is the Deep Reactive Ion Etching (DRIE) of the Si MEMS layer → vertical & smooth sidewalls with high aspect ratio (thin gaps) required



Dr Julien Arcamone ,MEMS Business Development Manager ,CEA-Leti, Grenoble (France)

Inertial MEMS are also widely used in automotive for various purposes. Let's take the example of NXP's HARMEMS technology. Such accelerometers are implemented to detect front or side crash in order to trigger airbags. In the left picture, the car contains 5 so called accelerometer satellites or modules. At the center of the car, an airbag electronic control unit, ECU, also senses crashes and triggers airbags.

Application – Accelerometers in cars airbags



- Players: Bosch, STMicro, InvenSense, Analog Devices, etc...
- Accelerometers in smartphones are mostly used for screen rotation and gaming
- Other example: NXP (ex-Freescale) "HARMEMS" technology for automotive



Courtesy from NXP-Freescale

Accelerometer Satellites.

- Front or side crash detection
- Module content: integrated inertial sensor + few passive components



Airbag ECU (Electronic Control unit)

- Module content: MCU + analog components + XY axis inertial sensors

Micro and Nanofabrication (MEMS)

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Practice quiz successful MEMS products: accelerometer

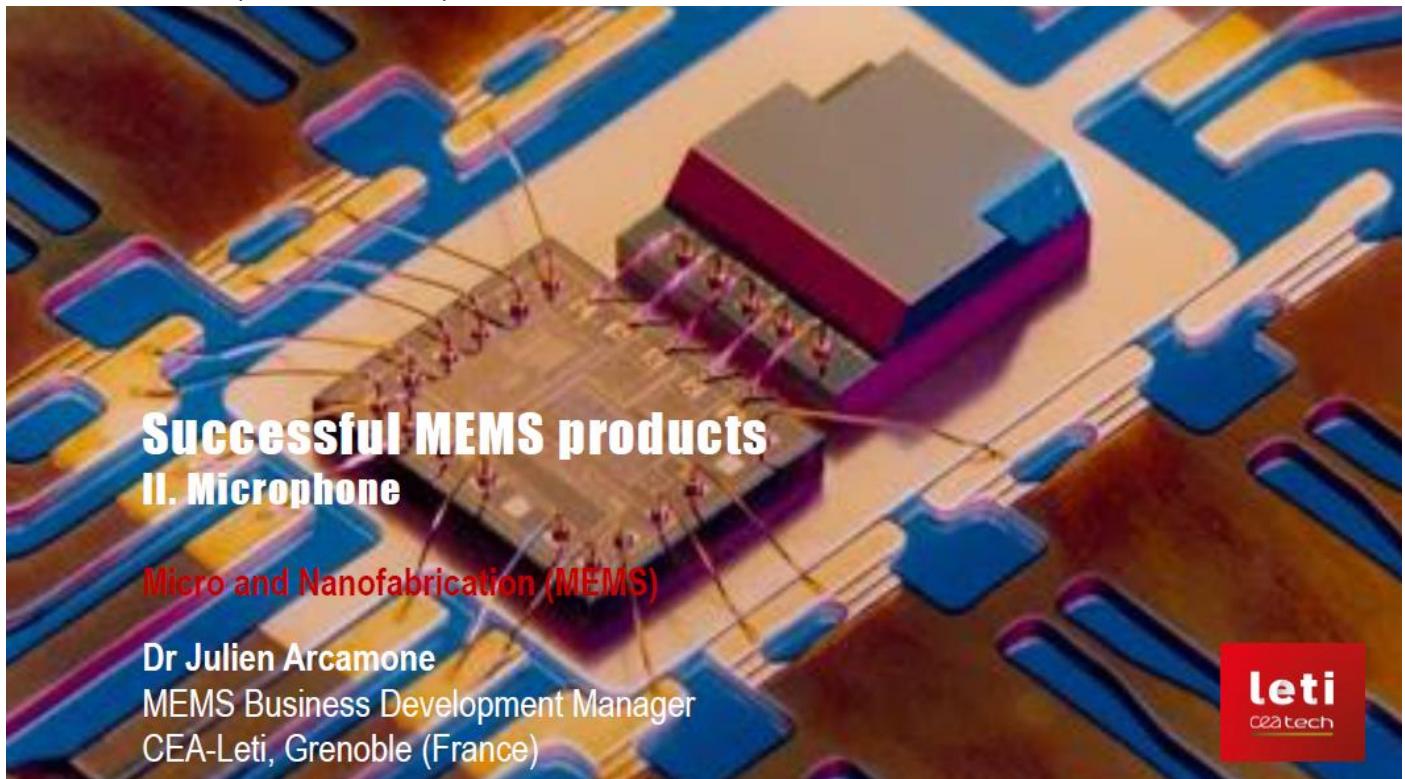
Questions:

1. Which of the following statements about MEMS capacitive comb drive accelerometer are correct?

- Combs provide larger capacitive readout
- The key parameter for the sensitivity of capacitive accelerometer is combs gap (g), which should be minimized as much as possible
- Accelerometer needs hermetic encapsulation

2. If you start with a SOI wafer, which of the following fabrication processes for capacitive comb drive accelerometer are needed?

- Deep reactive ion etching
- Wet or vapor HF etching
- KOH wet etching



Let's move to example 2 :

Example 2: Microphones in smartphones



- A microphone is a dual-die component: the MEMS microphone (most of them are based on capacitive detection) and its ASIC readout circuit



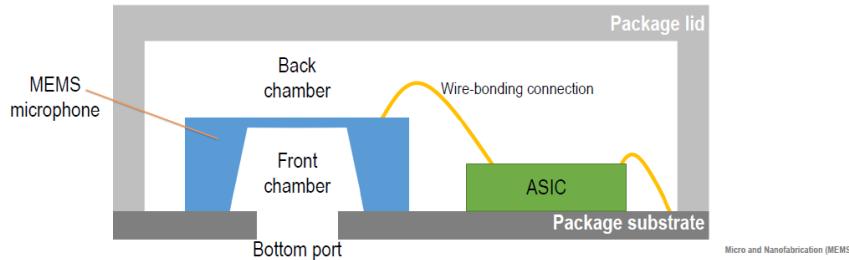
Micro and Nanofabrication (MEMS)

Dr Julien Arcamone ,MEMS Business Development Manager ,CEA-Leti, Grenoble (France)

microphones in smartphones. Generally, what is called a MEMS microphone is a dual-die component. The MEMS microphone itself most of them are based on capacitive detection and its ASIC readout circuit. ASIC as you may know stands for Application Specific Integrated Circuit.

Example 2: Microphones in smartphones

- A microphone is a dual-die component: the MEMS microphone (most of them are based on capacitive detection) and its ASIC readout circuit
- They are both housed in a package (top or **bottom sound port**)
 - For device protection and electromagnetic shielding
 - The back-chamber plays a very important role on the acoustic performance



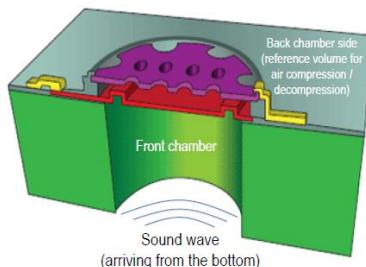
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They are connected to one another by wire bonding. MEMS and ASIC dies are both housed inside a package which has a sound port, either on the top side or at the bottom of the package. This scheme depicts a bottom port component. The package has multiple functions of course, as in all MEMS. It protects the device and provides a crucial electromagnetic shielding. In addition to that, the back chamber plays a very important role on the acoustic performance. The larger it is, the higher the signal to noise ratio, abbreviated as SNR.

Focus on capacitive MEMS microphones

- A movable membrane and a fixed back-plate form a variable capacitor which senses the membrane motion caused by an incoming sound wave

Incoming sound wave → Pressure differential → Membrane deformation → ΔC



Microphone drawing: courtesy from Infineon

Micro and Nanofabrication (MEMS)

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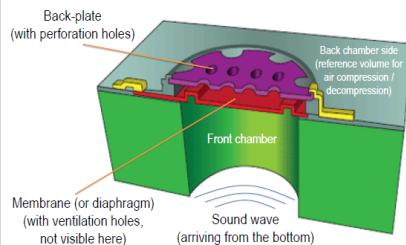
Although piezoelectric microphones are emerging, capacitive ones are by far the most widely used.

How do they work? Basically there are 2 suspended parts : a moveable membrane, here in red, and a fixed back plate, here in purple.

Focus on capacitive MEMS microphones

- A movable membrane and a fixed back-plate form a variable capacitor which senses the membrane motion caused by an incoming sound wave

Incoming sound wave → Pressure differential → Membrane deformation → ΔC



Microphone drawing: courtesy from Infineon

- Ventilation holes allows the compressed air in the back chamber to flow out
- Perforation holes for sound transmission
- Typical membrane diameter: 1mm
- Typical bandwidth: 20Hz – 20kHz

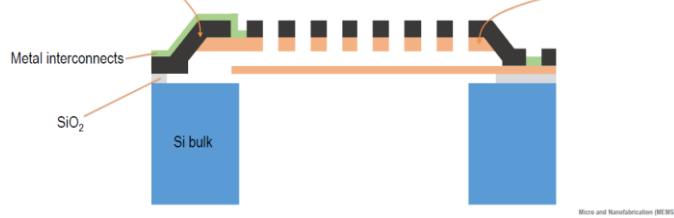
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Both form a variable capacitor which senses the motion of a moveable membrane caused by any incoming sound wave. In this example the sound comes from the bottom and the package is not depicted. To repeat again, the sound wave generates a pressure differential between the front and back chamber, consequently the membrane is deformed and this results in a capacitance variation. The membrane contains ventilation holes, not depicted here, to allow the compressed air of the back chamber to flow out. The back plate contains perforation holes basically to transmit the sound to the back chamber. The membrane diameter is typically in the order of 1 millimeter.

Microphones – example of fabrication process



- Process based on surface and bulk micromachining
- Critical process module n°1: deposition of low-stress polySi membrane
- Critical process module n°2: back-plate formation by deposition of thick polySi + highly tensile SiN (to obtain a rigid reference electrode)



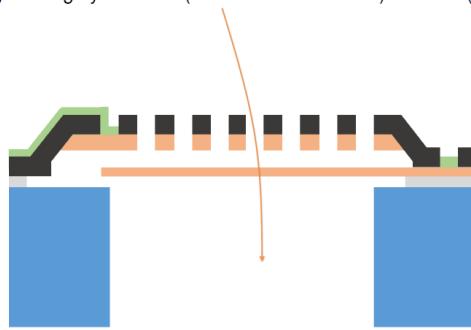
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Regarding the microphone bandwidth, it has to cover the human ear bandwidth, so from 20Hz up to 20KHz. Let's turn to the fabrication process of such sensors. This example is quite representative of all capacitive MEMS microphones.

Microphones – example of fabrication process



- Deep cavity etching by wet etch (with KOH for instance) or DRIE (more expensive)

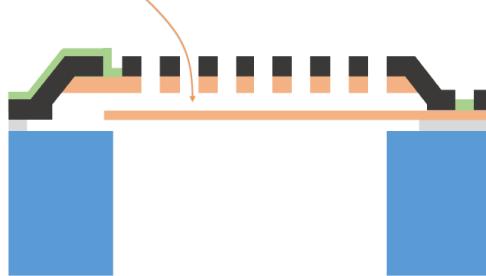


Micro and Nanofabrication (MEMS)

Microphones – example of fabrication process



- Deep cavity etching by wet etch (with KOH for instance) or DRIE (more expensive)
- Critical process module n°3: membrane release by removal of sacrificial SiO2 by wet etch



Micro and Nanofabrication (MEMS)

Dr Julien Arcamone ,MEMS Business Development Manager ,CEA-Leti, Grenoble (France)

Generally the process is a mix of surface and bulk micromachining. The first critical process module is a deposition of the low-stress polysilicon membrane on top of a SiO₂ layer. The second critical process module is a successive deposition of a thick polysilicon layer and of a highly tensile silicon nitrate layer. These 2 layers

form the back plate, which must be rigid enough to constitute a fixed reference electrode. Finally, metal interconnects are deposited in pattern. Another important step consists in realizing a deep cavity from the back side. It is obtained either by wet etch, for instance with KOH, or DRIE. The first option is cheaper but side walls are inclined. The second one, with deep reactive ion etching, represented here is more expensive, but side walls are vertical, which provides a larger cavity.

Application – Microphones in smartphones



- Players: Knowles, Infineon, OMRON, STMicro, InvenSense, etc...
- Already 4 MEMS microphones in iPhone 6S
- Functions: voice pick-up, noise cancellation, hands free



Source for pictures: Apple

Courtesy from IHS

Micro and Nanofabrication (MEMS)

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The final critical step is a membrane release by removal of a sacrificial SiO₂ layer by wet or vapor etch. Anti stiction control is crucial during this step. So let's talk about application now. First, which MEMS companies sell these kinds of devices? Let's cite Knowles, Infineon, OMRON, STMicro, InvenSense, etc.. As I mentioned before, microphones are present inside smartphones. The image below illustrates the number of MEMS microphones inside the iPhone as a function of its generation. Nowadays, the iPhone 6 contains 4 microphones. Some are used to pick up the voice, others for the cancellation of surrounding parasitic noise and the least main function is for the hands-free kit.

Practice quiz successful MEMS products: microphone

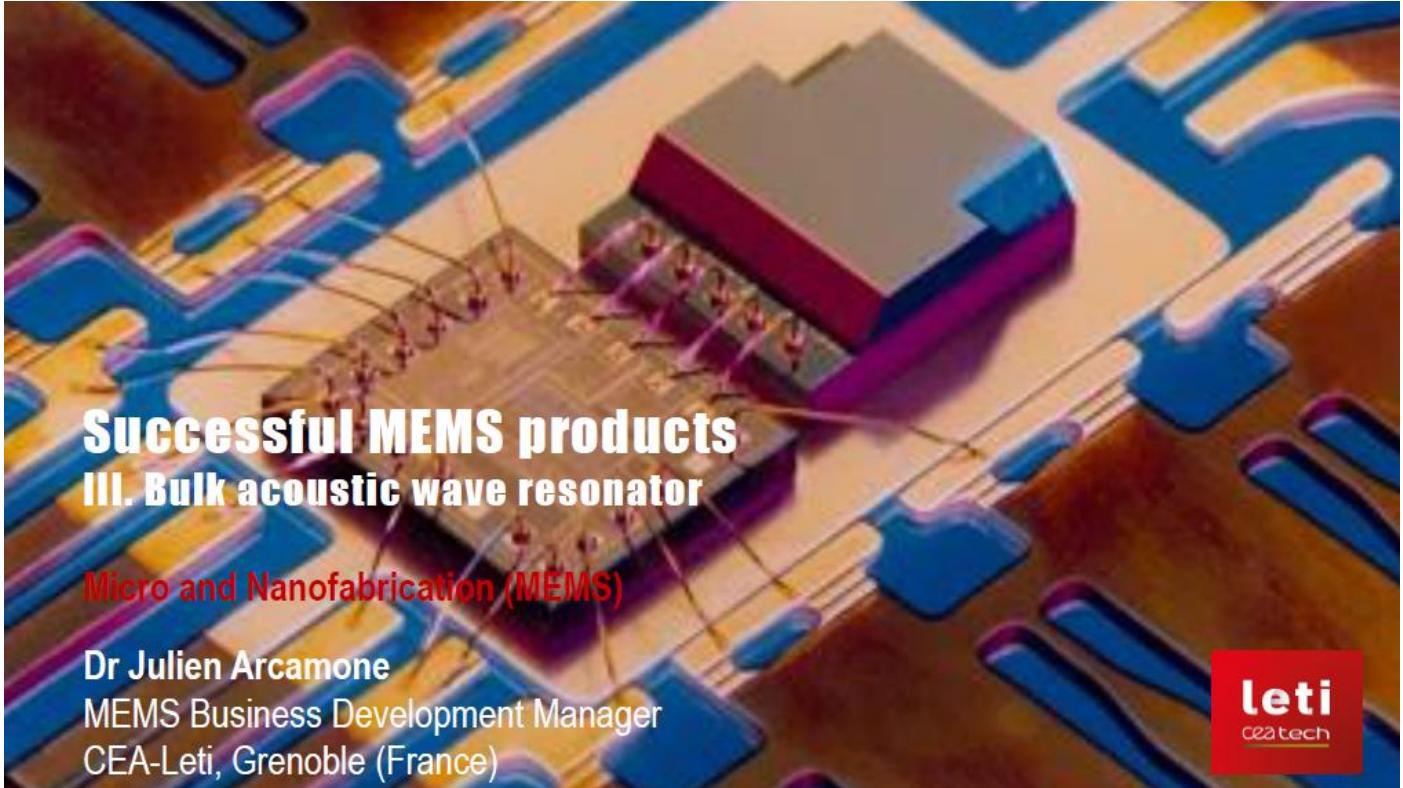
Questions:

1. Capacitive microphones contain two membranes for acoustic transduction. Which of the following statements are correct?

- Both membranes are movable
- Both membranes have holes
- Both membranes need to be metallic

2. Which of the following statements about the packaging of MEMS capacitive microphones are correct?

- The package protects the devices against dust
- The package provides an electromagnetic shielding
- The size of back chamber is relevant to the acoustic performance



Successful MEMS products III. Bulk acoustic wave resonator

Micro and Nanofabrication (MEMS)

Dr Julien Arcamone
MEMS Business Development Manager
CEA-Leti, Grenoble (France)

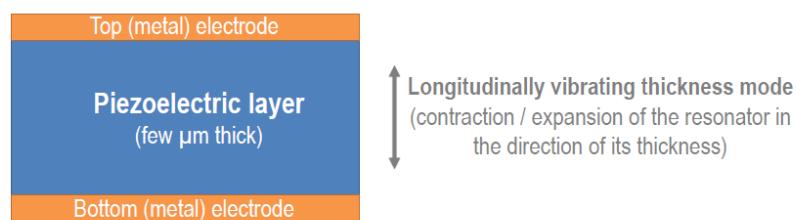
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Let's move to example 3 : BAW resonators in smartphones. As I said, BAW stands for Bulk Acoustic Wave resonators. The resonance frequency is generally in the range of the gigahertz.

Example 3: BAW resonators in smartphones

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- BAW (Bulk Acoustic Wave resonators) resonators use a piezoelectric layer (AlN most of time) sandwiched between two metallic electrodes
- Thickness mode with longitudinal (or shear) vibration: $f_0 = \frac{1}{2} \sqrt{\frac{E}{\rho}} \frac{1}{t_{Resonator}}$
→ with $t_{Resonator}$ in the μm range, $f_0 \approx 5\text{GHz}$



Dr Julien Arcamone ,MEMS Business Development Manager ,CEA-Leti, Grenoble (France)

In terms of structure, BAW uses a piezoelectric layer made of aluminium nitride most of the time sandwiched between a bottom and a top electrode, usually made of molybdenum. In terms of resonance mode, a thickness mode, either with longitudinal or shared vibration is operated. In the longitudinal mode, the resonator expands and contracts all the time in the direction of its thickness. Its resonance frequency is half the velocity of sound divided by the resonator thickness. The velocity of sound is the square root of the young modulus divided by the density. With a thickness of 1 micron approximately, the resonance is around 5 gigahertz. BAW resonators are used to implement band-pass filters - I will get back to this in the next slide. In this sense, the so-called KT square coupling coefficient is critical in terms of filter bandwidth and insertion loss. The KT square is given by the ratio between the difference between the resonance frequency and the antiresonance frequency divided by the resonance frequency. In fact, the KT square depends on piezoelectric material properties. Therefore, the deposition and further process of the piezoelectric layer is crucial.

How can we build a filter using BAW resonators? Basically by implementing a ladder filter architecture.

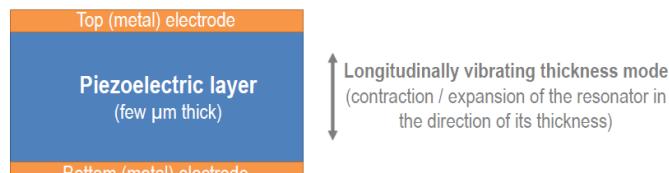
Its unit cell that can be replicated n times contains 2 BAW resonators : a series one and a shunt one connected to ground.

Example 3: BAW resonators in smartphones



- BAW (Bulk Acoustic Wave resonators) resonators use a piezoelectric layer (AlN most of time) sandwiched between two metallic electrodes

- Thickness mode with longitudinal (or shear) vibration: $f_0 = \frac{1}{2} \sqrt{\frac{E}{\rho}} \frac{1}{t_{\text{Resonator}}}$
→ with $t_{\text{Resonator}}$ in the μm range, $f_0 \approx 5\text{GHz}$



- BAW are used to make band-pass filters: the coupling coefficient $k_t^2 (= \frac{f_0 - f_{\text{antiresonance}}}{f_0})$ critical in terms of filter bandwidth and insertion loss

Micro and Nanofabrication (MEMS)

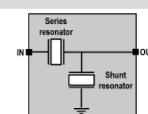
Dr Julien Arcamone ,MEMS Business Development Manager ,CEA-Leti, Grenoble (France)

Let's explain how it works by observing the filter response. At the center of the slide, the frequency response of the shunt resonator is depicted at the top. The one of the series resonator is depicted here and this is the response on the whole filter. Please note that the shunt resonator response is shifting down to lower frequencies, such that the shunt antiresonance coincides with the series resonance.

Filters based on BAW resonators



- Unit cell of "Ladder filter" (replicated n times): 2 BAW resonators



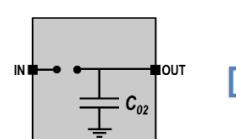
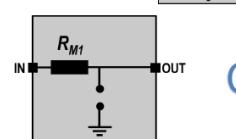
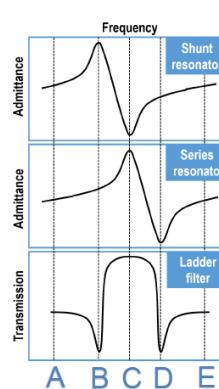
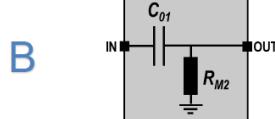
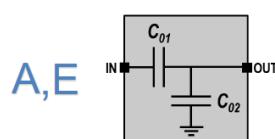
Dr Julien Arcamone ,MEMS Business Development Manager ,CEA-Leti, Grenoble (France)

In state A, both resonators are far from the resonance frequency. Therefore, they both behave as capacitors. In state B, the series resonator is still far from resonance. And it behaves as a capacitor while the shunt one is at resonance. In other words, its impedance is minimum. In fact, in this state, its impedance is equal to its so-called motional resistance which is less than 1 ohm.

Filters based on BAW resonators



- Unit cell of "Ladder filter" (replicated n times): 2 BAW resonators
- Ladder filter response



Micro and Nanofabrication (MEMS)

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As a consequence, the output node is almost grounded and there is no signal transmission. In state C, the series resonator is at resonance. In other words, its impedance is minimum and of less than 1 ohm. In the meantime, the shunt one is at its antiresonance. In other words, it is at its maximum impedance and it

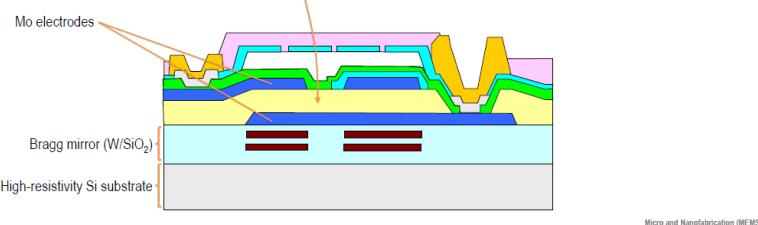
behaves as an open circuit. As a consequence, the impedance between input and output nodes is minimum and a signal transmission is maximum. In state D, the series resonator is at its antiresonance, in other words, at its maximum impedance. And it behaves as an open circuit. The shunt one is far from resonance and behaves as a capacitor. As a consequence, the impedance between input and output nodes is maximum and the signal transmission is minimum. In state E, the situation is very similar to state A. Both resonators behave as capacitors. So this is basically a summary of how a ladder filter using BAW resonators works. Let's turn to the fabrication process of BAW. Let's first mention that there are 2 types of BAW due to the fact that

there are 2 main approaches of acoustic wave confinement. So called FBAR, thin Film Back Acoustic wave Resonators are suspended resonators over an air gap. So-called SMR, Solidly Mounted Resonators, consist of unreleased resonators, so I mean not suspended, located over a Bragg mirror that.

BAW – example of SMR fabrication process



- 2 types of BAW (2 approaches of acoustic confinement): FBAR (suspended resonator over an air gap) and SMR (unreleased resonator over a Bragg mirror)
- **Critical process module n°1:** deposition process (PVD) of the AlN MEMS layer
→ critical to reach (i) a precise and uniform thickness (inducing f_0) and (ii) good piezoelectric properties (inducing k_t^2)



Micro and Nanofabrication (MEMS)

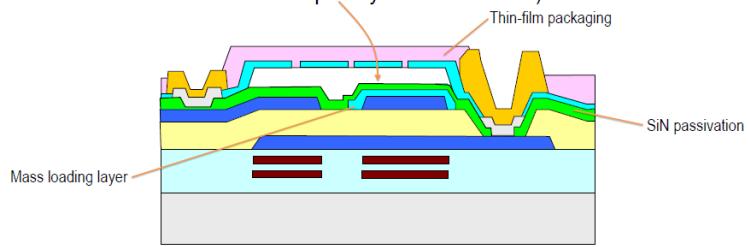
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reflects back the waves. We will focus on this type. This is a cross sectional view of an SMR, processed on a high resistivity silicon substrate. You can see the Bragg mirrors here which are made of tungsten plates surrounded by SiO₂. The first critical process module consists in depositing an aluminium nitride layer by physical vapor deposition on top of a properly oriented molybdenum bottom electrode. This sputtering technique allows .

BAW – example of SMR fabrication process



- All resonators are identical with one exception: some have a loading layer to separate them in frequency to obtain distinct shunt and series resonators
- **Critical process module n°2:** wafer-scale ion beam trimming
→ local removal of material on each resonator to adjust f_0 if needed (all filters must have the same center frequency and bandwidth)



Micro and Nanofabrication (MEMS)

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obtaining first, a precise and uniform thickness - have in mind that the resonance frequency is inversely proportional to the thickness - and second, good piezoelectric properties which result in high KT square.

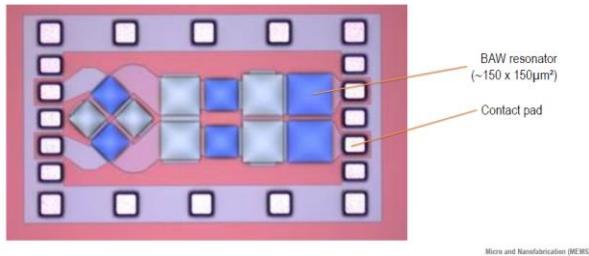
The top electrode is also made of molybdenum. Another important step is the mass loading of shunt resonators. In fact, shunt and series resonators are identical by design. Then, this mass deposition on top of the shunt resonators allows to adequately decrease the resonance frequency so that the antiresonance

coincides with the series resonator resonance, as I explained in the previous Section. The second critical process step is wafer-scale ion beam trimming. By locally removing some material, the ion beam allows precisely adjusting the resonance frequencies of each series and shunt resonators. It's indeed very important that each filter has the same bandwidth and center frequency. The resonators have a silicon nitride passivation, in green and are capped with a thin-film packaging, in pink, to provide them with an hermetic and clean cavity at ambient pressure.

BAW – example of SMR fabrication process



- Top view of a filter
- One square = one resonator
- Depending on whether they are mass loaded or not (series or shunt), the resonators color is different



Micro and Nanofabrication (MEMS)

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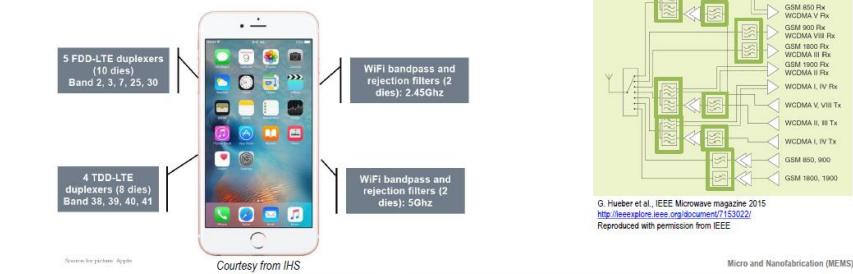
This optical microscope image shows the top view of a filter chip at the end of the fabrication process. Basically, the white squares and rectangles are metallic contact pads. And the coloured squares are BAW resonators which have a typical 150 by 150 square micron area.

Depending on whether they are mass-loaded or not, I mean series or shunt, the resonator's colour is different. So let's talk about application now.

Application – BAW filters in smartphones



- Key players: Avago (FBAR), Qorvo & TDK-EPCOS (SMR)
- A key element for RF front-end modules (RF stage located between the antenna and the ADC) – for telecom band selection (band-pass filter)
- More than 20 BAW filters dies in iPhone 6S



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First, which MEMS companies sell these kinds of devices? Let's cite Avago that produces FBARs and Qorvo and TDK-EPCOS that produce SMR's. BAW band-pass filters have become a key element of RF front-end modules of smartphones. Such modules are essentially the RF stage located between the antenna and the analog digital convertor. In this context, BAW filters are used to select a given telecom band. In green, you can see all the filters present in this example of front-end module. And for example the iPhone 6S contains more than 20 BAW filters dies either for 4G or LTE connection or for Wi-Fi connection. I would like to wrap up this lesson. We have analysed 3 examples of commercially successful MEMS devices All these devices

Acknowledgments

- Sophie Giroud, Guillaume Jourdan (Accelerometers)
- Stephanus Louwers (Microphones)
- Alexandre Reinhardt (BAW)



- Jérémie Bouchaud 

- Dave Monk 

NB: NXP and Freescale have merged on 7 Dec 2015, under the company name NXP.

Micro and Nanofabrication (MEMS)

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have been sold in the hundreds of millions of units and all of them rely on advanced micro and nano fabrication techniques that you will see in the upcoming lessons of this MOOC. Thanks for your attention.

Practice quiz successful MEMS products: BAW

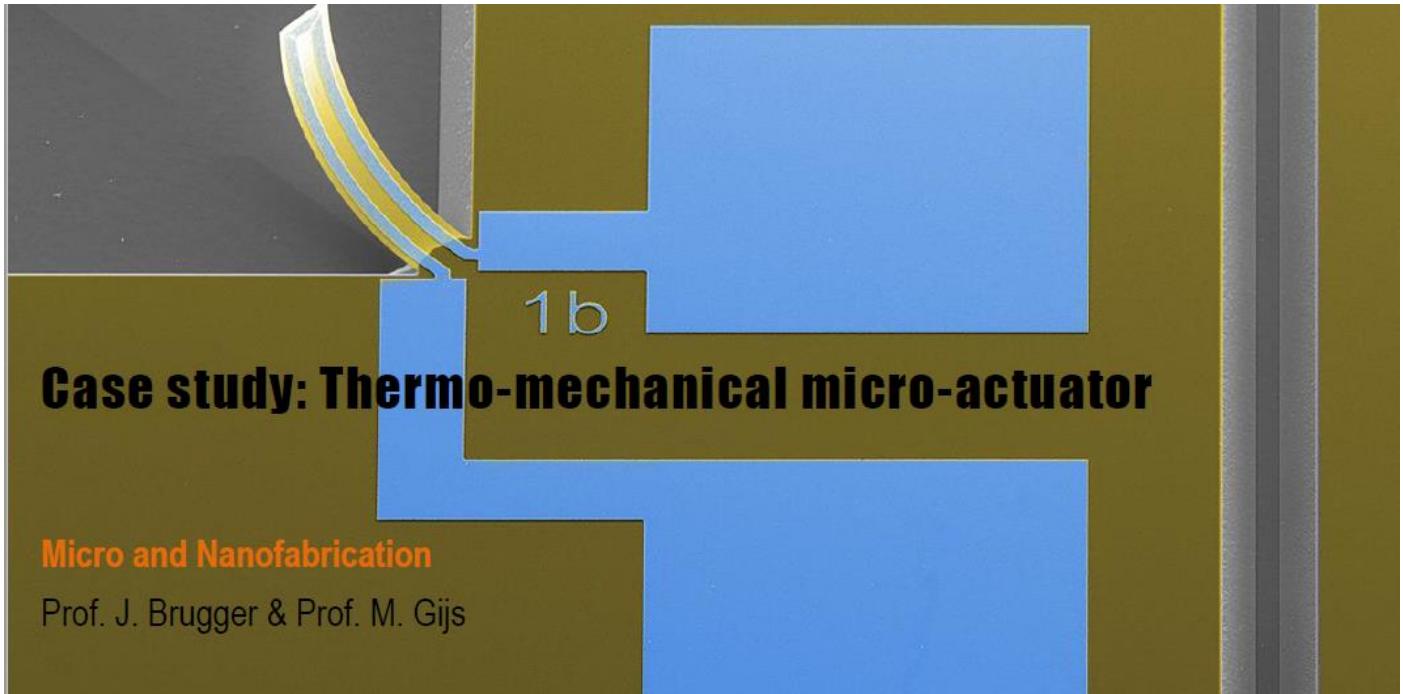
Questions:

1. Which of the following statements about BAW are correct?

- Solidly Mounted Resonators (SMR) are unreleased resonators located over a Bragg mirror
- Chemical vapor deposition is normally used to deposit piezoelectric materials for SMR
- Ion beam trimming is needed in order to adjust the resonance frequency

2. Before the thin-film packaging, Bulk Acoustic Wave (BAW) resonators are trimmed by ion beam. Which of the following propositions are correct?

- All resonators are equally trimmed
- The trimming shifts the resonance frequency upwards



Welcome to this lesson in micro and nano fabrication . The picture Above shows a colorful SEM image of a bi-morph MEMS actuator. And in the next few minutes, I will show how it was fabricated in our clean room at EPFL. Although it does not involve all possible fabrication steps that are nowadays available in advanced MEMS processes, It initiates you the students to the basics of a process flow.

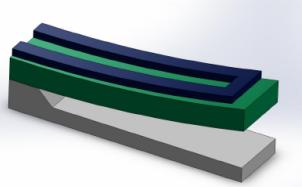
What is a bi-morph micro-actuator?



- Bi = 2; morph = shape
- Thermo-mechanical actuation
- Sandwich of two thin films
- Different thermal expansion coefficient α
- ΔT induces bending

$$\frac{1}{r} = \beta \cdot \Delta\alpha \cdot \Delta T$$

r: radius of curvature
 β : constant, f(t, E)
 α : thermal expansion coefficient [K⁻¹]
 ΔT : temperature difference [K]



$$k = \frac{3EI}{L^3} \quad \omega_{res} = \sqrt{\frac{k}{m_{eff}}}$$

I: area moment of inertia [m⁴]
 L: length of the beam [m]
 t: thickness [m]
 W: width [m]
 m_{eff} : beam effective mass [kg]
 k: spring constant [N/m]
 E: Young's modulus [N/m²]
 σ : strain [Pa]
 ω_{res} : resonant angular frequency [s⁻¹]

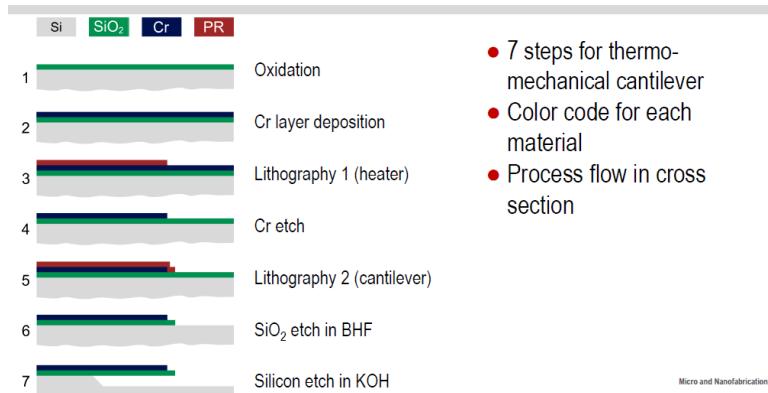
Micro and Nanofabrication

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As you will see, the fabrication is a well defined sequence of lithography, thin film deposition, as well as wet and dry etching. In my left hand, I'm holding a silicon wafer before the fabrication. And in my right hand, you see a similar wafer containing hundreds, if not thousands, of MEMS devices like in the background. But before diving into microfab aspects, let's briefly recall how a thermal mechanical device, or bi-morph, actually works. A bi-morph is a device that can take two or more shapes. 'Bi' means 2 in Latin, and 'morph' means shape in Greek. On the right side you see a typical example of a bi-morph made by 2 thin films. In our case, SiO₂ in green, and Chromium in blue. Since both materials have very different thermal expansion coefficients α , they induce a bending when the temperature changes. When you apply a voltage to the Chrome layer... you induce a current that will heat up, this... cantilever, and by the temperature change will induce bending. The curvature radius of the bending can be expressed by a formula shown here. Where the radius of curvature is described by β times the difference in thermal expansion coefficients of the 2 materials, Chrome and Silicon dioxide and the temperature change. β is a constant, as a function of the thickness of the device and its Young's modulus. Other formula to describe the system are the spring constant of the

cantilever, and the resonance frequency. And here's a list of all important parameters that can be used to describe the system. In the accompanying documents you can see how this formula can be derived from basic physics. The process flow is typically shown schematically by a sequence

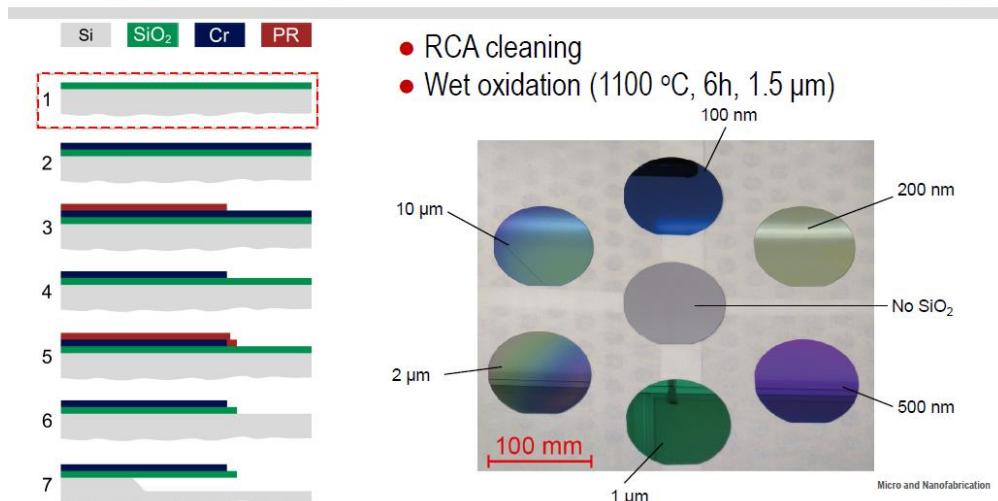
Overview of microfabrication sequence



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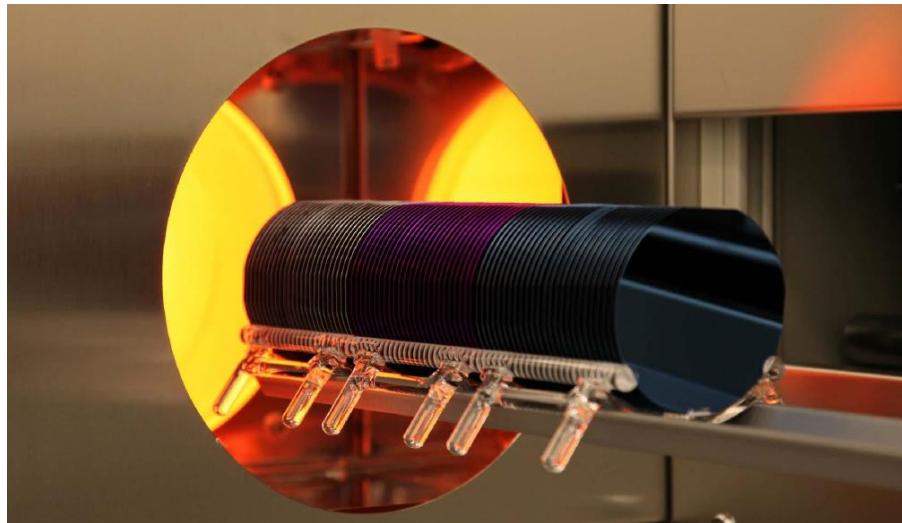
of cross section figures. In the case of the bi-morph cantilevers, there are 7 major process steps. The representation is in principle sufficient to show the effect of added thin films, and the effect of wet and dry etching on each layer. Such a document will accompany the wafer during the process To know always exactly at which step of the process the wafer is. And what process parameters have been applied to each wafer. Now let's have a look at each of the 7 steps in detail, 1 by 1. The first step is to grow a Silicon dioxide layer, which will be one of the 2 bi-morph materials. Before the actual oxidation, the wafer is thoroughly cleaned. This process is called RCA cleaning, which is an industry standard since the 1960s, and consists of a couple of steps. Wet oxidation is then carried out in the furnace with oxygen rich atmosphere.

Step 1: Wafer prep and wet oxidation



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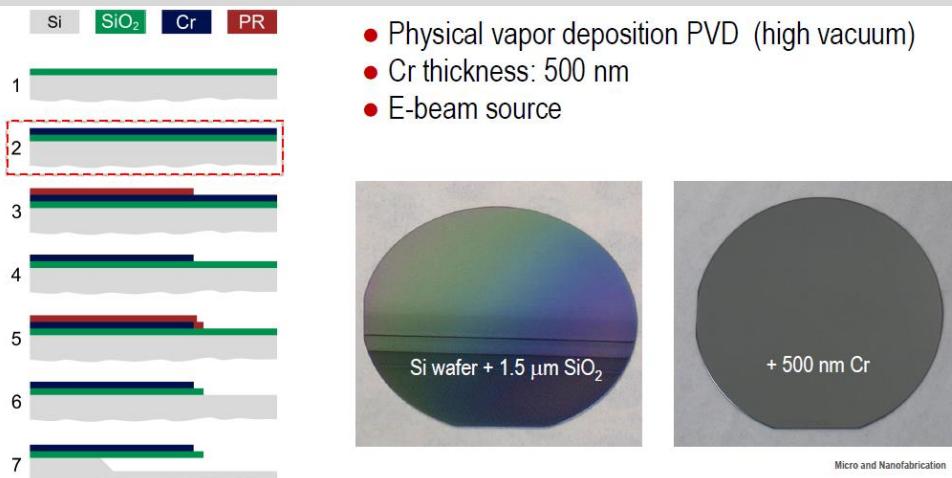
Silicon on the surface is thereby transformed into a Silicon dioxide layer that grows with time, while consuming the underlying silicon. To form a 1.5 micrometer thick SiO_2 layer, we typically oxidise the silicon wafer during 6 hours at 1100 degrees C. Here you see a couple of silicon wafers, 100 millimeters in diameter or 4 inch. The centre is a silicon wafer without any silicon dioxide, looks grey, and here is a couple of silicon wafers with different silicon dioxide thicknesses ranging from 100 nanometre, up to 10 micrometre.



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We can see clearly the difference in colour, which is due to the interference of the dielectric thin film on the silicon wafer. With experience, one can actually indicate already what thickness the wafer is. However, to measure precisely, one will then rely on an ellipsometer. Step 2 is the physical vapor deposition of the chromium layer. Which is the second material in the bi-morph cantilever. This layer serves 2 purposes. First, as a thin conductor, it will allow driving a current to heat up the surface that will result in the bi-morph activation. Second, chromium is chosen before other metals because it has very different thermal expansion coefficient than silicon dioxide. This mismatch will induce a very pronounced bi-morph effect when heated. In this particular case, we deposit a 500 nanometre thick chromium layer using an electron beam evaporator equipment. And here on the right side, you see 2 photos. The left one shows a silicon wafer with the 1.5 micrometer silicon dioxide appearing again, colorful. And the right photo shows the same wafer, after having been coated with 500 nanometer chromium. Now the wafer looks again like a reflecting mirror.

Step 2: Cr deposition by PVD



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This photo shows the PVD thermal evaporator equipment in our clean room. With the scientist loading evaporant material at the lower part. The substrate wafers will be mounted on the upper part, which gives a long source substrate distance for optimal film uniformity. Once the substrates are loaded, the door will be closed, and the air will be pumped out to install the high vacuum. Step 3 shows the first photo-lithography step that has to go to pattern the chrome layer into micro heaters that are subsequently used to heat up the cantilever and to induce its bending. Photo-lithography is the process step that creates the pattern in the photoresist by local elimination through an exposure mask. The exposed resist is developed

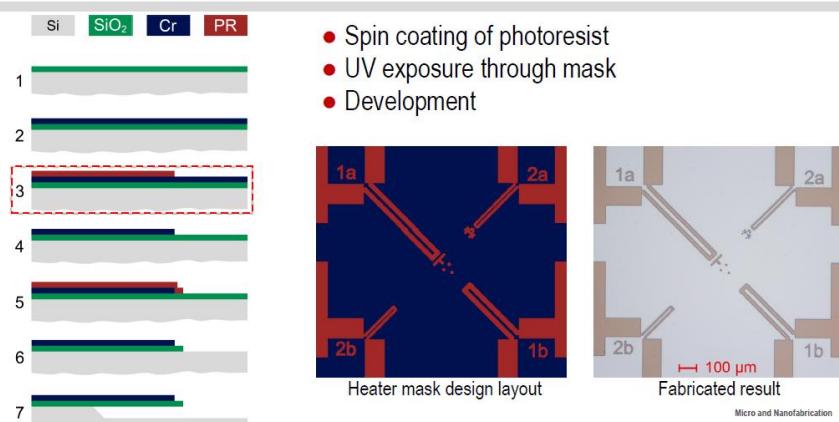
and remaining resist pattern protects the underlying material from being etched. So on these 2 photos, you see on the left side, a computer drawing of the design layout, where we see 4 heater loops in chrome. On the mask, and on the right side, we see the fabricated results.



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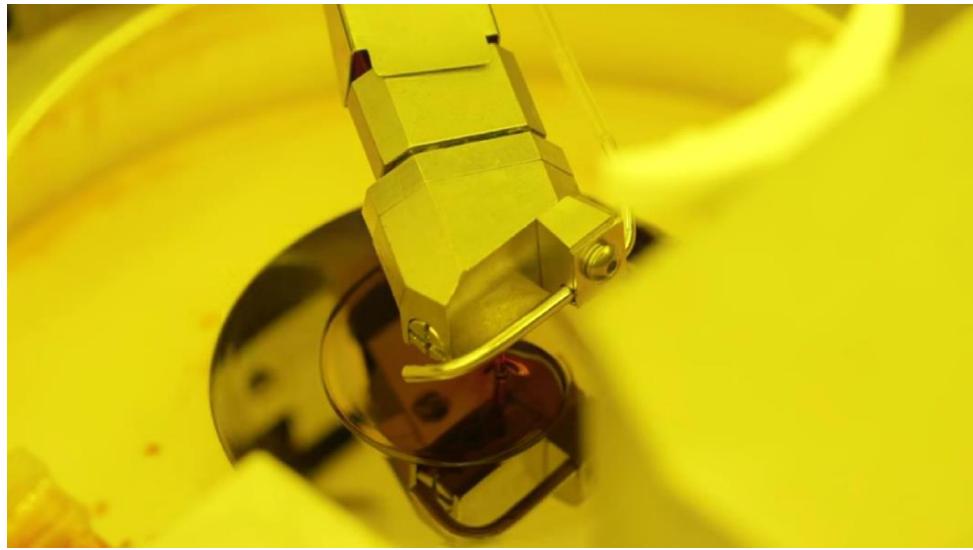
So what you see here in brownish, is the pattern photo-resist on top of the chrome layer. This is the step after the lithography before actually the chrome etching. In this Section sequence, you see how the photo-resist is spin coated on the wafer substrate.

Step 3: Photolithography to pattern the Cr heaters



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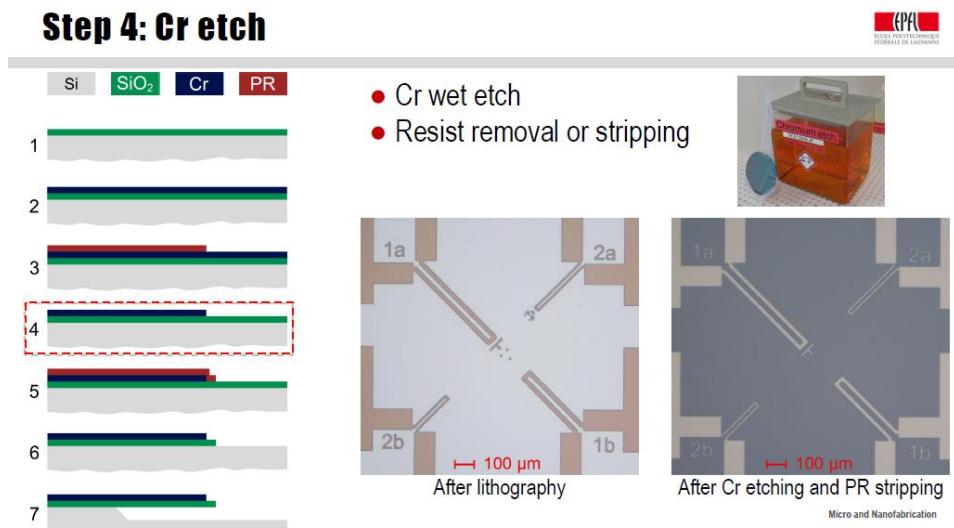
To this end, the wafer is spun at high speed and the resist is dispensed in the center. This forms a uniformed resist layer over the entire wafer surface. We will see details, how thick? And how uniformed the resist film is? In the dedicated lesson on lithography. Once the photo-resist is patterned, we can now proceed to etch the chrome. To this end, we use a dedicated chromate solution as shown on the upper right corner. The wafer with the photo-resist pattern is placed into the chromate solution after the chrome has completely etched through, a strong color contrast appears on the wafer. At this point, the photo-resist can be removed by a so called stripping process followed by thorough rinsing and cleaning. Here you can see 2 photographs.



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On the left side you see the situation, after the lithography, with the photo-resist on the chrome. And on the right side, you see the situation after the chrome etching, and the photo-resist stripping. We can see nicely, the well defined chrome pattern that will define the micro heaters on top of the SiO₂ layer. Now that the chrome is patterned, we can structure the underlying SiO₂ layer to carve out the cantilever shape. This step also defines the shape of the anisotropic silicon etch to release the beam from the substrate. Before UV exposure, the photo mask is aligned to the first one by means of a so called mask aligner.

Step 4: Cr etch

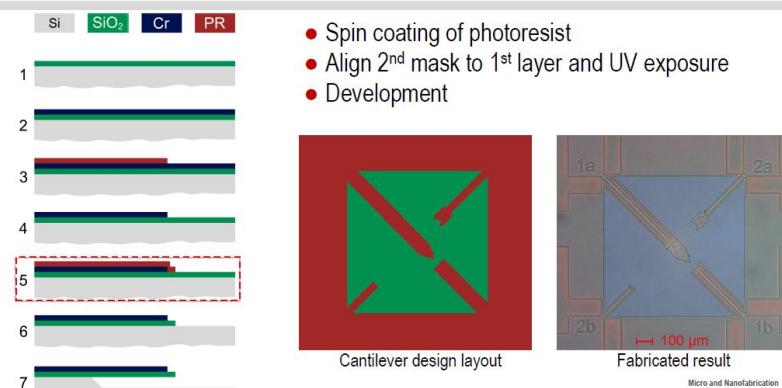


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The left image shows the cut mask lay out, whereas the right image shows the optical photo of the 4 cantilevers. One can actually see clearly the 2 layers now. The shape, of the cantilever in transparent photo-resist defined in the second lithography. And the chromium, that was defined in the first lithography step. This allows checking that the alignment of the mask is within the tolerance specifications. The photo-resist that we patterned in the previous steps serves now to protect the silicon dioxide during the etching in buffered hydrochloric acid, BHF. This etchant has SiO₂ .etch rate of about 80 nanometer per minute. And the etch selectivity to silicon is almost infinite. Thus for etching the 1.5 micrometer thick silicon dioxide, we typically need about 20 minutes etch time which stops naturally at the silicon surface. Be very cautious. BHF is dangerous and strict safety measures have to be applied. After the SiO₂ etch, the photo-resist can be stripped, exposing again the chrome layer. This Section sequence shows a clean room scientist, who puts a batch of wafers into the BHF etch bath, to etch the silicon dioxide. Please notice the serious protection that is needed.

On this right photo, you can see now the result after the fabrication, where we can see in dark grey the

Step 5: Photolithography to pattern the SiO₂ beams



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contours of the silicon dioxide cantilevers still on the silicon. And in light grey, the chromium heater pattern that runs on top of the 4 cantilever shapes.

Step 6: SiO₂ etch



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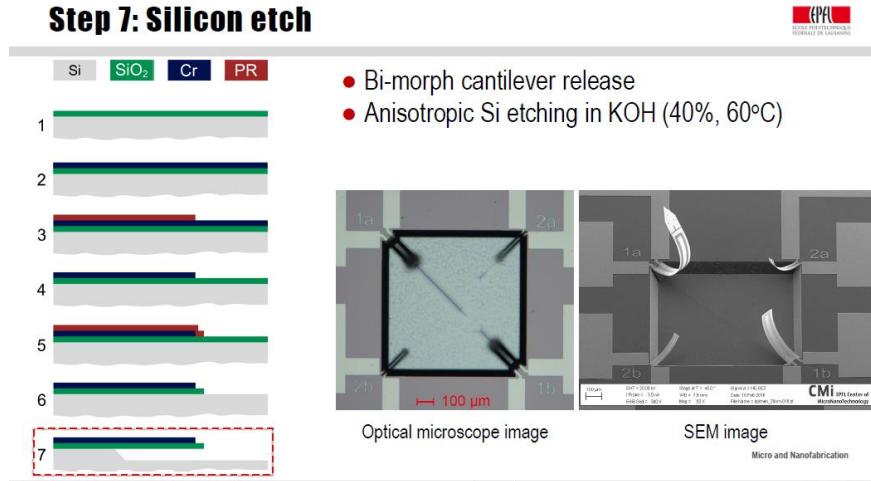
The final step releases the cantilever beam from the underlying silicon by anisotropic under etching. While there are several options that can be used to etch silicon, such as dry plasma silicon etching. We use here the anisotropic wet etching of silicon done in Potassium hydroxide, also called KOH. This method is very versatile, and widely used for these type of structures. The silicon 1,0,0 plane has an etch rate of about 20 micrometers per hour in KOH.



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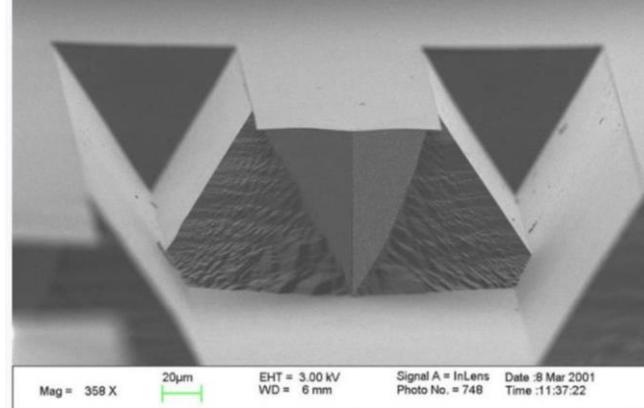
Whereas the 1,1,1 silicon planes are hardly etched at all which allows creating the well defined 3D etch structure in the shape of a truncated inverted pyramid. The SiO₂ thereby serves as an etch mask to define the borders of the etch structure. With the largest cantilever beam 80 micrometers wide, we need about 2 hours to under etch 40 micrometers from each side. When the under etching is completed, and the cantilever released from the silicon, the intrinsic stress in the SiO₂ chromium sandwich layer induces an out of plane bending of the cantilever. On the right side, we see 2 photographs showing the fabricated bi-morph cantilevers. On the left, an optical microscope image taken from above.

Step 7: Silicon etch



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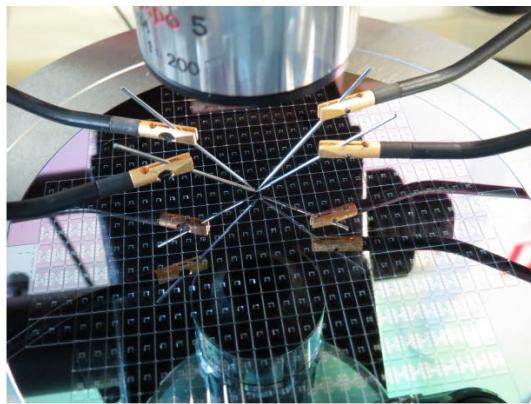
Where we see nicely the square that has been etched by the KOH into the silicon. And the 4 cantilevers in the corner that have been under etched. Cantilevers themselves are not easily visible because they are pre-stressed, and pre-bent largely, so they're out of focus of the microscope.



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To see them better, we're going to the scanning electron microscope. Where we see now nicely the cantilevers in all details. We also see nicely, the square that has been etched by the KOH into the silicon. The cantilevers are largely bent due to the stress between the SiO₂, and the chromium. Please note that at this point of time, there's no heating applied. So this stress, is the intrinsic stress due to fabrication, and not an actuated bending. The bi-morph thermo-mechanical micro actuators are now ready for characterization. For this, we use a probe station that can align micro needles to the contact pads to apply electrical signals to various devices on the chip or wafer, and to measure IV curves.

Thermo-mechanical characterization

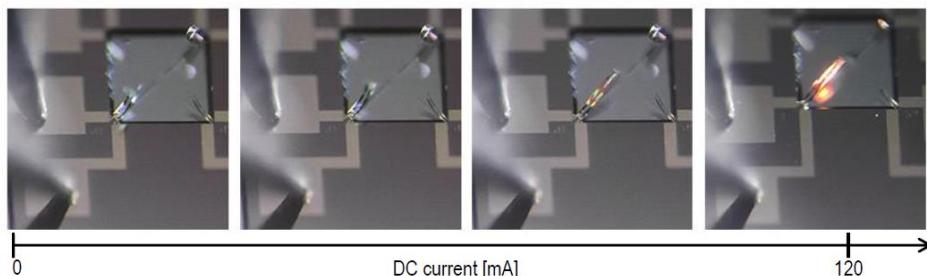


~ 50 Ohm
resistance

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In our case, we have measured the resistance of our chrome heaters, and they are typically in the order of about 50 ohm. These 4 optical images, show bi-morph device under various DC currents. Please remember, that the initial bending of the cantilever is due to the intrinsic stress and occurs already at room temperature. It is not due to heating. Heating in fact will bend the lever downwards. From left to right, the voltage is increased from 0 to about 6 volts, which gives us an increasing current as shown here. The current heats up the chrome layer by Joule heating. Already in photo 2, We can see that the bi-morph has moved downwards a bit. This actuation effect is more pronounced in this photo, where we also start seeing a color change. This color change is due to the heat

Thermo-mechanical characterization



Static mode ($R \approx 50 [\Omega]$)

Increase voltage from 0 to 6 V to Cr resistor → Joule heating increases
Difference in thermal expansion → cantilever bending
Cr heater starts to glow at high voltages

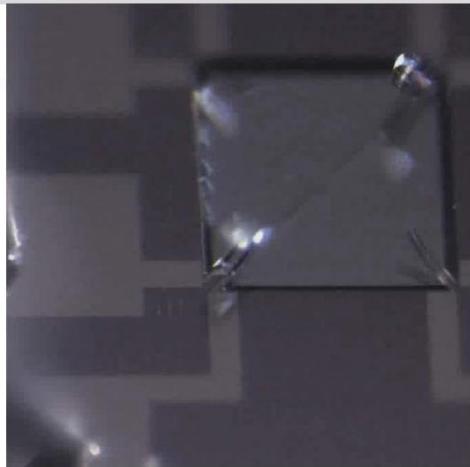
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generated in the chrome resistor, which emits radiation. Increasing the current further, we can see that the bi-morph starts to glow. Running this experiment for a very long time will damage the device like a fuse. Here you can see a movie that shows the actuation of the bi-morph cantilever driven by DC voltage. Using the same voltage range as shown in the slide before, from 0 to 6 volt.

Thermomechanical characterization

Movie showing the bi-morph cantilever driven by DC with the same voltage range as before (0 – 6 V)



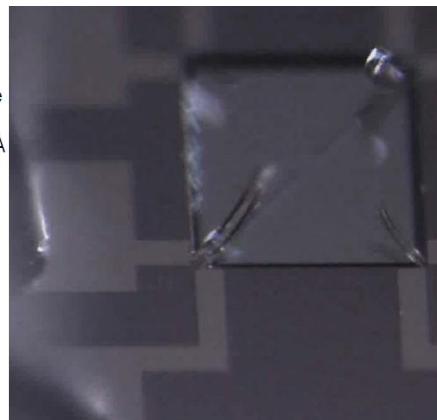
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You can see in real time when ramping up the voltage and current, that the cantilever starts bending down.

And at very high current levels, the cantilever starts to glow, and ultimately might burn like a fuse if the experiment is run too long. And here you can see, the actuation of the bi-morph when the voltage is changed manually. Details of the frequency response is provided by the accompanying documents. Please have a look, as they provide useful information on the bandwidth in which such a device can operate. As you can guess, this is not only a function of the mechanical resonance frequency of the cantilever, but also of the heat dissipation away from the cantilever. This concludes this chapter on the fabrication

Movie showing the bi-morph cantilever driven by AC by applying a peak to peak voltage of 4-5 Vpp.
Currents are between 0-100 mA
Frequency between 1 – 10 Hz



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of the bi-morph cantilever. I hope you learned how one can get from a blank silicon wafer, hundreds and thousands of micro devices, by series of micro fabrication steps. In the next chapters, my colleague and I will present more technical details on the different fabrication steps.

Thermo-mechanical micro actuator: computation of the radius of curvature:

Find [here](#) a PDF file containing the PhD Thesis of S. Schweizer about “Thermally actuated micro-mirror for one and two-dimensional optical beam scanning”. Pages 32 to 46 describe how to relate the stress in a material to the temperature change, how to compute the stress in a bimorph cantilever at initial rest position, and how to compute the radius of curvature of a bimorph micro-actuator as a function of the temperature change, the films thicknesses and the materials Young’s modulus and coefficients of thermal expansion.

Thermo-mechanical micro actuator: dynamic response:

Find [here](#) a PDF file describing the dynamic response of a bimorph micro-actuator when applying a sinusoidal AC current in the chromium track. The cantilever temperature, free-end displacement, as well as oscillation frequency are discussed for different AC current frequencies.

The figure below shows the finite element modeling (FEM) of the dynamic response of a bimorph micro-actuator. Sinusoidal AC currents are applied through the chromium electrodes at frequencies of 1, 10 and 100 Hz respectively. In blue is shown the displacement of the free-end of the cantilever. In red is shown the corresponding temperature at the free-end of the cantilever. In all cases, the amplitude (Vpp) of the excitation current is the same.

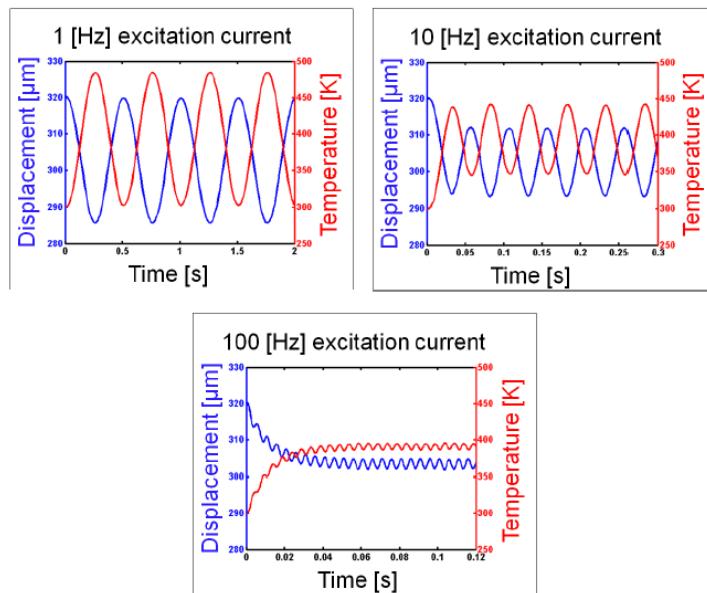


Figure: Finite element modeling of the dynamic response of a bimorph micro-actuator under 1, 10 and 100 Hz sinusoidal AC current excitations.

Several observations can be made out of these three simulations. First of all, the cantilever oscillation frequency is the same as the temperature variation frequency. This is in accordance with formula (1) relating the radius of curvature of the cantilever to the temperature change. β is a constant while $\Delta\alpha$, ΔT and r stand for the thermal expansion coefficient difference, the temperature difference and the radius of curvature. The full derivation of this formula is given in S. Schweizer's Thesis (see previous supporting information).

$$1r = \beta * \Delta\alpha * \Delta T \quad (1)$$

A second observation is that the cantilever oscillation frequency is twice the excitation current frequency. Indeed, for the 1 Hz excitation current, we clearly see that the cantilever makes two full oscillations during 1 second. The qualitative explanation is rather simple. We use a sinusoidal current as excitation current which means that within one period, the current has positive and negative values. However, no matter the direction of the current, it dissipates energy in the chromium track by Joule heating which actuates the cantilever. As a result, the cantilever oscillation frequency is twice that of the sinusoidal excitation current frequency.

Finally, we also see that the heat dissipation of the device has a limited bandwidth. By increasing the frequency of the excitation current, we observe that the cantilever temperature doesn't go back to its initial value around 300 K at each oscillation. This is due to the fact that at high frequencies, the cantilever has no time to cool down between two subsequent current peaks. In a general way, heating a material is faster than its passive cooling in air. As a result, the oscillation of the free-end of the cantilever also becomes smaller. It is important to note here that the decrease in the amplitude of the cantilever oscillation has two origins. The first one is the limited bandwidth of the heat dissipation, and the second one is the stiffness of the cantilever itself. If we further increase the excitation current frequency to match the mechanical resonant frequency

of the cantilever (in the 10 kHz range), then the amplitude of the free-end displacement would increase again at this specific frequency.

Practice quiz case study: thermo-mechanical micro-actuator:

Questions:

1. A typical microfabrication process consists of a series of steps that needs to be documented with sufficient details to ensure quality and reproducibility. What is the common name for the document that is used to describe each step of the fabrication process?

- Step by step description
- Process flow
- Standard operating procedure
- Cross-section view

2. The fabrication of the thermo-mechanical micro-actuator involves one step where the 500 nm thick chromium layer is etched in order to create a 20 μm wide chromium track. This etch step requires about 10 minutes. What is the time (in minutes) needed to create a 40 μm wide chromium track in the same chromium layer of 500nm thickness?

Cleanroom basics: introducing the issue of contamination :



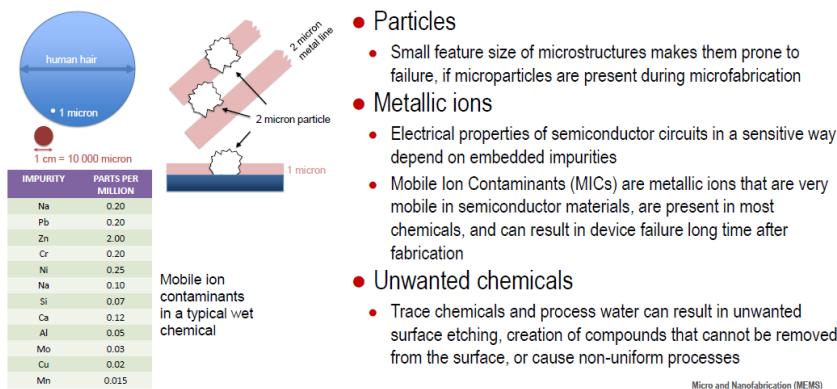
We have seen that many identical microelectronic devices can be realized on a single wafer which is a technology that is at the basis of many high performance applications in nearly every domain of our daily life. The reproducibility of microfabrication indeed is a key factor for economic realization of any consumer product. Therefore, these devices are most of the time realized in a clean room environment where experimental and manufacturing conditions are reproducible and very strictly controlled. In this lesson, we will introduce a few of the basic aspects of the design of and work in a clean room. We will start by discussing different contamination problems that may arise when one wants to develop a microfabrication process. We will discuss the different sources that are at the basis of contamination and that can result in failure of devices. We will introduce different options for creating an environment with clean air and for clean room construction. Finally, we will give an example of a clean room by introducing the center of micro and nano technology at EPFL.

- Contamination problems
- Contamination sources
- Clean air strategies
- Cleanroom construction
- A glimpse of the Center of MicroNanotechnology at EPFL

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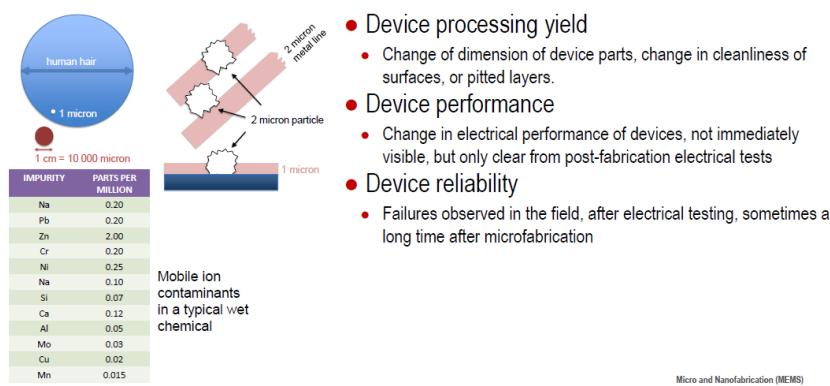
Different types of contamination exist which all can compromise successful realization of a microfabricated device. The first problem is posed by the presence of particles in the air which, when they have the size of the features of the microfabricated structure, can result in failure of the device. This drawing shows as an example two micron wide metal lines which can be realized using a thin film deposition technique. When during deposition, micro particles are situated on the substrate and when they have this size, they can give rise to these connected metal structures, like shown here. Another contamination problem is that of ion impurities. If one works with semiconductor circuits, the operation of a device can be severely disturbed when unknown metal impurities are present in the semi conductor. Especially so-called "mobile ion contaminants" or MICs, pose problems. These contaminants can be present in most of the chemicals that

are used for the microfabrication of a device. And when incorporated in the silicon, they can migrate to a sensitive area where they can cause device failure even a long time after fabrication. This implies that chemicals should be as pure as possible. The table here shows metal impurities that are present in a typical wet chemical that is used in the clean room. More generally, the presence of trace chemicals, unwanted chemicals and process water of insufficient purity, can result in unwanted surface etching effects.



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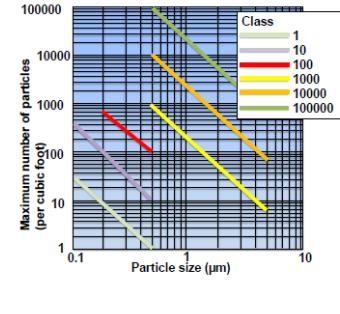
or deposition effects which are at origin of non-uniformities in microfabrication processes. If these contamination sources are present, they affect the devices in different ways. First of all, there is the device processing yield. Like shown in the drawing on the left, a change in dimension or an interruption of device parts results in a non-functional device. Such failure can be measured immediately after the microfabrication step by optical or microscopic inspection. Some defects are not directly visible but can be measured by evaluation of the device performance after completion of the full microfabrication process. Usually, electrical testing allows to eliminate devices from the wafer or chips from the wafer that are not functional. Contamination also affects device reliability and can cause the failure of the device a long time after its microfabrication. An example of such failure can be the diffusion of a mobile ion contaminant in an electronic circuit. The impurity can migrate to a sensitive region on the wafer, a long time after



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microfabrication leading to the disfunctioning of a microelectronic circuit. An important source of possible contamination in a clean room is the air. Small particles can float in the air and remain there for a long time. They are called also aerosols. The fewer and the smaller the particles are in the air, the better is the quality of the clean room. The quality of a clean room is therefore characterized by the clean room class number, which is the number of particles above a specified diameter in a cubic foot of air. For example, in this graph, we see that the class thousand clean room has not more than a thousand particles of half a micron in size per cubic foot. A class 10 clean room has not more than 10 of these particles in a cubic foot of air. The lower the class number, the better the quality of the clean room. As a rule of thumb, particles that are present in the air should not exceed half of the feature size of the microstructure to be fabricated.

As examples of air quality, a normal house room has a class of 100,000, while a very large scale integration area in a clean room should have class 10 for particles of 0.3 micrometer. A person can produce in between 100,000 and 1 million particles per minute which are flakes of dead hair and skin, while normal clothing adds more millions of particles. It is clear that the person has to be completely covered when he is in the clean room. And he needs to be covered with a special clean and dust free tissue. The photograph on the left shows the person wearing special overshoes which are on top of the normal shoes. The person has gloves, and he wears an integral clean room suit, a mask of the mouth and the nose and glasses to protect the eyes. A particular dressing protocol has to be followed when someone enters the clean room to minimize particle contamination. Such protocol is shown in the following Section. A person who works in a clean room, first takes care of not entering dust or contamination via shoes.



- Small particles ‘float’ in air and remain there for along time (=aerosols)
- Air quality is designed by **class number** of the cleanroom : **the number of particles above a specified diameter in a cubic foot of air**
- Rule of thumb: allowable particle size should not exceed 1/2 of feature size of the microstructure
- Examples
 - House room = class 100 000
 - Very Large Scale Integration (VLSI) area = class 10 (for 0.3 μm particles)

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There is a particular way of entering. Before the barrier, the environment is not clean and going in by this type of motion during which the shoes are covered with a clean protective coating, ensures that no contamination is released from the shoes into the clean room. Next follows putting on a coat, whereby one assures that the sleeves do not touch the ground. Then follows putting on this type of overshoes to further protect the clean room from contamination originating from the feet. Then follows putting on a mask for covering the heads and the hair and a mask that covers nose and mouth. Glasses are put on for eye protection and security. The last stage is that the operator puts on gloves for protection of the hands. And finally, he is ready to enter into the clean room. A second source of contamination in a clean room is the water used for processing the wafers. All water that is used has to be treated, as normal city water contains dissolved minerals, particles and bacteria, which can introduce impurities or non-uniformities during microfabrication. Dissolved ions like sodium and chlorine ions can compromise quality of microfabricated circuits and can originate from salts dissolved in the water. Therefore, the water has to be deionized and the degree of ion concentration in the water can be measured by measuring the resistivity of the water. Indeed, if there are very few dissolved impurities, the resistivity of the water is very large. 18 million Ohm centimeters. If there are more impurities, resistivity is much lower. For water used in a very large scale integration area in a clean room, the resistivity of minimum 18 M Ohm cm is required.



- Person can give 100 000 and 1 000 000 particles per minute (flakes of dead hair and skin), while normal clothing adds more millions of particles
- Solution: completely cover a person in a cleanroom by a cleanroom suit
- 'Dressing protocol' has to be followed to minimize particle contamination

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Deionisation is a chemical process that uses ion exchange resins that exchange protons and hydroxyl ions for dissolved ions in the water. After which protons and hydroxyl ions recombine to form a water molecule. Besides process water, all process chemicals and gases that are used in a clean room should be of high purity. The most serious impurities are the metallic mobile ion contaminants in chemicals. And in a chemical, concentrations smaller than one part per million are desired. Also common gases that are used in a clean room such as oxygen, nitrogen and hydrogen, and special gases like arsine and carbon

Resistivity ($\Omega\text{m}\cdot\text{cm}$) at 25°C	Dissolved solids (ppm)
18 000 000	0.0277
15 000 000	0.0333
10 000 000	0.0500
1 000 000	0.500
100 000	5.00
10 000	50.00

Resistivity of water versus concentration of dissolved impurities

- All process water has to be treated; city water contains dissolved minerals, particles and bacteria
- Dissolved ions (e.g. Na^+ and Cl^-) originate from salts in the water
- Water has to be de-ionised to give a very high resistivity, $18 \text{ M}\Omega\text{ cm}$ in VLSI areas
- Deionisation is a chemical process that uses ion-exchange resins that exchange H^+ and OH^- ions for dissolved ions, and then recombine to form water

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tetrafluoride, should be very pure. The gas quality can be classified according to four criteria: the percentage of purity of the gas; its water vapor content; the number of particulates in the gas; and the number of metallic ions in the gas. The photographs on the left show the typical infrastructure for water and gas handling which is present in proximity of the clean room.



- Metallic mobile ion contaminants are the most serious impurities in process chemicals; a concentration < 1 ppm is desired
- Common gases, such as oxygen, nitrogen and hydrogen, and specialty gases, such as arsine and carbon tetrafluoride, are used in the cleanroom
- Gas quality is classified according to four criteria
 - Percentage of purity
 - Water vapor content
 - Particulates
 - Metallic ions

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Practice quiz cleanroom basics: introducing the issue of contamination:

Questions:

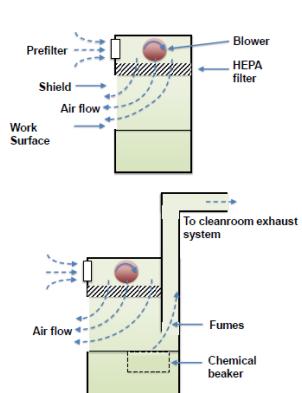
1. Device reliability is important when fabricating microsystems for commercial use, where long lifetime is required. Unfortunately, some reliability issues cannot be directly determined once the fabrication process is finished. Which of the following failure is not a long-term failure mode, but can be rather detected already during or shortly after the fabrication of a device?

- Slow diffusion of mobile charge carriers to sensitive areas of the device
- Delamination due to stress originating from moving parts
- Fatigue due to repeated use of the device
- Particle contamination

Cleanroom basics: cleanroom strategy:



How does one obtain clean air with a minimum number of particles? The first possibility is to do the processing of the wafers in individual work stations with filtered air.

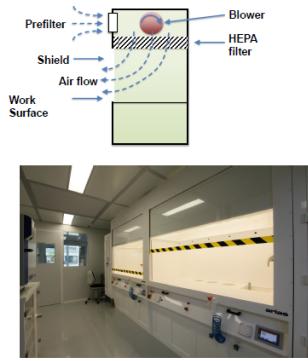


- Processing of wafers in individual work stations with filtered air
- Work stations (hoods) are arranged in rows and are provided with high-efficiency particulate arrestance (HEPA) filters, containing small holes and a large surface
- Vertical laminar flow (VLF) and horizontal laminar flow hoods are used

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These work stations or hoods are arranged in rows and are provided with high efficiency particulate arrest, or HEPA filters, which contain small holes and a large surface. Air is blown through such a filter and a vertical laminar flow exposes the wafers that are manipulated here in the hood. So the wafers are only exposed to highly purified air with a minimum number of particles. If chemicals are operated in the hood, this is not the right construction, as the toxic fumes of the chemical would go to the operator. If one needs to manipulate chemicals, the hood is of this type. Part of the laminar flow is evacuated via this line so that there is no risk for the operator who is working here to be in contact with these chemical vapors because basically, he is doing his manipulation here in this area. The picture on the left shows a hood for the manipulation of chemicals. A drawback of such laminar flow hood is that the environmental conditions can change due to the people that are present in the room and who can be the origin of particles underneath the hood. Therefore, a better but also a more costly solution, is to build these HEPA filters in the ceiling of the room and provide everywhere in the room clean conditions. That is what makes a really clean room.

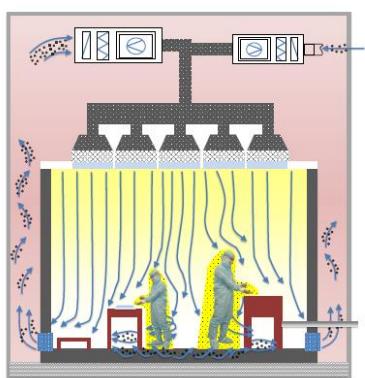


- Processing wafers in individual work stations with filtered air
- Work stations (hoods) are arranged in rows and are provided with high-efficiency particulate attenuation (HEPA) filters, containing small holes and a large surface
- Vertical laminar flow (VLF) and horizontal laminar flow hoods are used
- Drawback of laminar flow hood: vulnerability to contamination from people in the room → better build HEPA filters in ceiling of the room and provide clean conditions everywhere; this is more expensive

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This brings us to concept of the total clean room where the complete clean room has purified air due to the presence of continuous laminar flow from the ceiling to the floor. Also, through table tops with perforations, and so on. Purified air will expose the wafers and the people, and any generated particles will be transported away through the floor and be purified before being re-injected through HEPA filters in the clean room. The clean room not only has good purity of the air, but there is also a tight control of the temperature which is essential for operator comfort and for reproducibility of chemical processes. Also the humidity has to be controlled as the presence of moisture on wafers can influence many processes like the adhesion of a photoresist for example. Also, smoke needs to be avoided. As a reactive gas, it is like ozone, it can interfere with many chemical processes that are running in the clean room. These two photographs show part of the air-handling infrastructure of a clean room that is present above and below the clean room area. A high quality clean room is essential for high quality research in microfabrication related areas. At EPFL, we have such a clean room which really is a corner stone of many of our research and educational activities. The following Section provides a glimpse of the EPFL center of micro and nano technology. In this lesson I explained that the clean room is a necessary infrastructure for the reproducible microfabrication of miniaturized devices.



- Continuous laminar flow from the ceiling to the floor, also through tabletops with perforations, etc.
- Tight control of
 - Temperature (operator comfort and process control)
 - Humidity (e.g. moisture on wafers prevent adherence of photoresists)
 - Smog (e.g. ozone interferes with photoresist development processes)



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Air, process chemicals, water and gases should all be of high purity. We have discussed two approaches of creating a clean room environment. First there was the laminar flow hood for creating locally clean air conditions and next, there was a total clean room strategy. Finally, I introduce to you the center of micro and nano technology at EPFL.

Summary

- Cleanroom is necessary for microfabrication of miniaturized devices
- Air, process chemicals, water, and gases should be of high purity
- Two approaches: laminar flow hood for local clean air conditions and 'total cleanroom'
- Center of MicroNanotechnology at EPFL (CMI)

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Practice quiz cleanroom basics: cleanroom strategy:

Questions:

1. Which of the following list is the most important feature of a 'total cleanroom'?

- Precise temperature control
- Downward laminar flow of filtered air to ensure that the wafers are only exposed to clean air
- Regulated, fixed humidity
- A smog-free environment guaranteed

Conclusion and summary :

In this chapter about MEMS and cleanroom introduction, you have learned the working principle of three successful MEMS which are accelerometer, microphone and bulk acoustic wave resonator. You also learned the microfabrication steps required to fabricate a thermo-mechanical micro-actuator. Finally, you were introduced to the cleanroom environment and to the possible source of contamination. Here are a few important key points you should remember.

Successful MEMS products

- Accelerometers consist of a suspended proof mass which movement is measured by a capacitive detection.
- Accelerometers are fabricated using silicon on insulator wafers.
- Accelerometers are used in smartphones for screen rotation and in automotive for collision detection.
- Microphones consist of a moving membrane which displacement is measured by a capacitive detection.
- Microphones are fabricated using both bulk and surface micromachining processes.
- BAW resonators consist of a piezoelectric material sandwiched between two electrodes.
- BAW resonators circuits enable to create bandpass filters used in RF front end modules for telecom.

Thermo-mechanical micro-actuator

- Bimorph micro-actuator is based on the difference of the thermal expansion coefficients of two materials.
- The process flow to fabricate such a device includes cleaning, physical vapor deposition, photolithography and wet etching steps.
- Intrinsic stresses due to the different fabrication processes induce an initial bending of the cantilever when released from the substrate.
- Bandwidth of such devices is limited by the heat dissipation time.

Cleanroom basics and CMi overview

- A cleanroom is necessary for reproducible microfabrication of miniaturized devices.
- Air, process chemicals, water, and gases should be of high purity.
- Two approaches seen: laminar flow hood for local clean air conditions and ‘total cleanroom’.
- Classification of a cleanroom is based on the purity of the air, as quantified by the number of particles present per air volume.



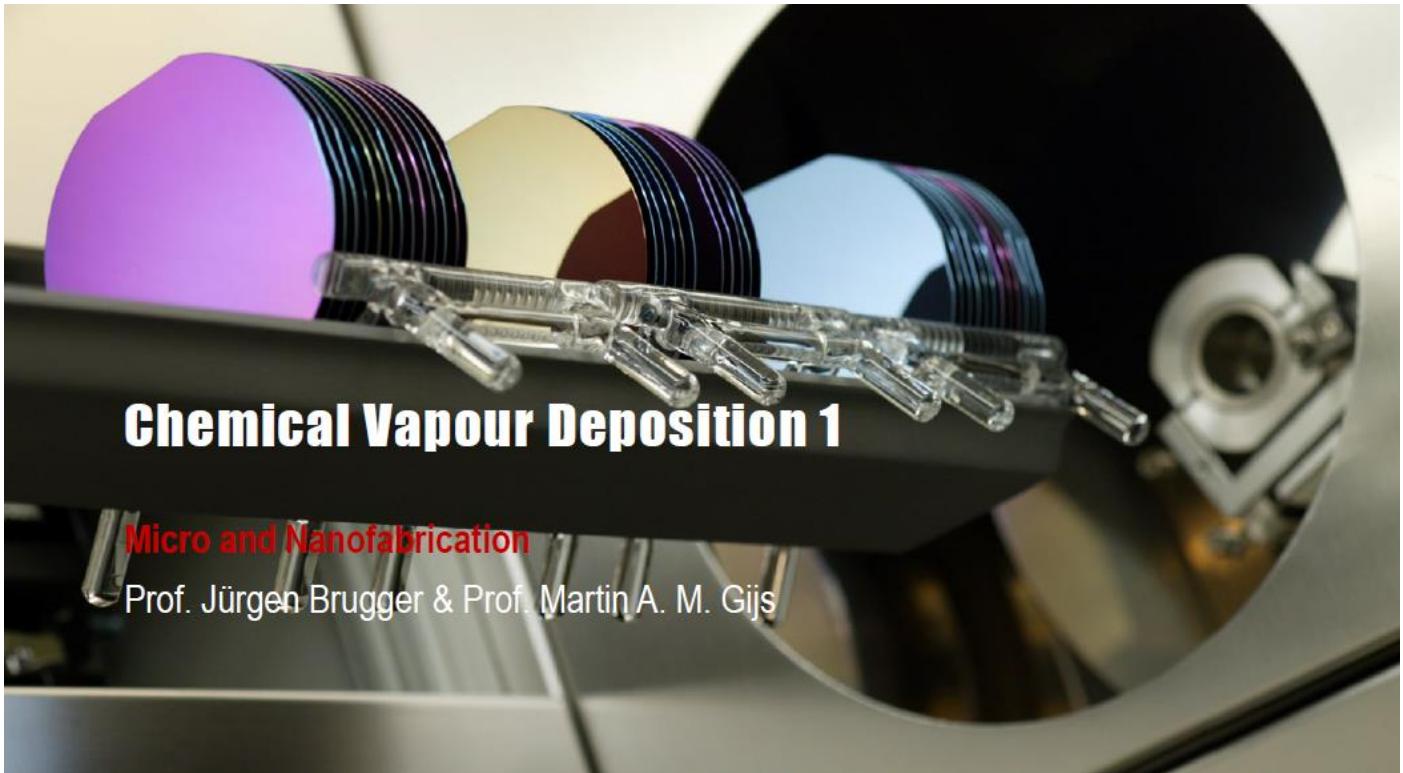
Introduction and objectives

Chemical vapor deposition (CVD)

This module on chemical vapor deposition or CVD describes in detail basic principles of CVD and will show you the cleanroom infrastructure that is used to run a CVD process. CVD techniques at different operating pressures will be introduced, like atmospheric pressure CVD or APCVD, sub-atmospheric pressure CVD or SACVD, followed by low pressure CVD or LPCVD, and finally ultrahigh vacuum/CVD for the lowest pressure used. Next we will discuss a technique called plasma-enhanced CVD or PECVD and finally the technique metal-organic CVD or MOCVD. Atomic layer deposition or ALD will be introduced, which is a technique in which a thin film is deposited atomic layer-by-atomic layer, as well as the thermal oxidation process of silicon. We will introduce important theoretical concepts that play a role in CVD, like the velocity and concentration boundary layer near a substrate. We will subsequently present a theoretical model for the CVD film growth. Finally, specific CVD deposition processes will be introduced for depositing poly-crystalline and amorphous silicon, silicon oxide, silicon nitride, diamond and metal films.

At the end of this Chapter , you should be able to:

- Name the different chemical vapor deposition methods and list their main advantages and limitations.
- Describe the technique of atomic layer CVD, in which a thin film is deposited atomic layer-by-atomic layer.
- Understand how the velocity and concentration of a gas near a substrate during CVD is strongly modified compared to the velocity and concentration in a free flowing gas.
- Understand how the Reynolds number plays a role in the gas molecule transport.
- Understand the deposition of a thin film on a substrate using a gas transport model.
- Describe the CVD of poly-crystalline and amorphous silicon, silicon oxide, silicon nitride, diamond and metal films.



Chemical Vapour Deposition 1

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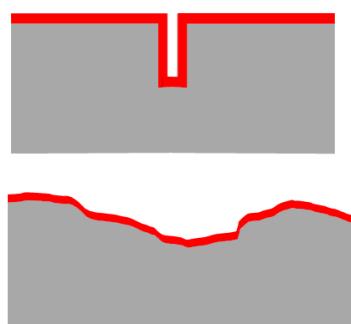
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Welcome in the introductory lesson on chemical vapor deposition or CVD. Here we will discuss the basic principles of CVD and will show you a glimpse of the clean room infrastructure that is needed to run a CVD process.

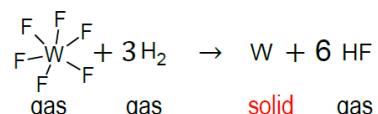
- Principle of CVD
- Clean room infrastructure
- Classification of CVD processes
- Common CVD reactor types

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Different types of CVD techniques will be introduced and finally, a few common CVD reactor types will be presented. As the name of the technique says, a chemical reaction is involved in depositing a thin film material using CVD. We give, as an example here, the deposition of tungsten at a high temperature of 600 degrees Celsius. To realize this deposition one introduces into a reactor two gasses, tungsten hexafluoride and hydrogen, which, upon chemical reaction, result in the deposition of the metal tungsten and the release of the gas HF. The word *vapor* used in this CVD technique indicates that the starting compounds to start a CVD deposition are gasses. As gas fills easily all parts of the reactor, every surface in the reactor is exposed in the same way by the gas. As a result, the solid tungsten is deposited everywhere in the same way,



- Chemical reaction is involved
- Example for **deposition of W** at high temperature



- Use of gaseous phase results in **conformal deposition** on substrate with arbitrary texture

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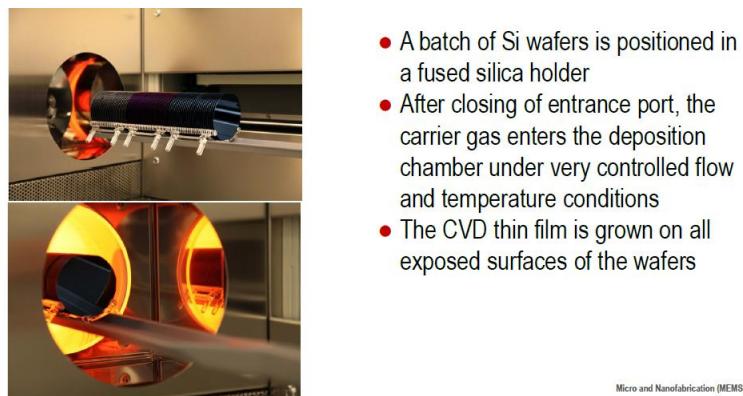
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conformal to the substrate. The conformal deposition of the tungsten is schematically indicated in this drawing. More interestingly, from the drawing on the top, it is clear that the gas can also enter into narrow holes or restricted spaces in the substrate. This opens possibilities for the technique to do a metalization inside cavities and provide electrical contacts between different levels on the wafer, for example. Here we show a typical CVD equipment, how it looks like. The picture on the left shows 4 circular entrances behind which a fused silica reactor is positioned, invisible in this picture. Use of fused silica allows operation until very high temperatures, typically up to 1000 or 1100 degrees Celsius. The picture also shows that boats made with fused silica have been charged with a number of silicon wafers. A boat can enter a tube via an entrance hole after which the door is closed and the CVD process can start.



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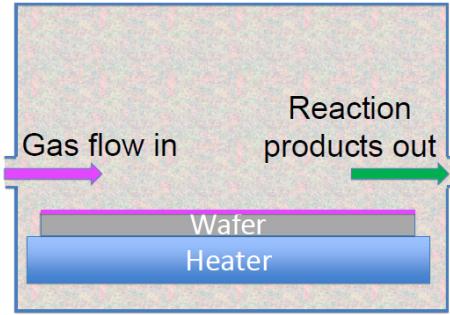
The picture on the right shows an operator who is charging the boat with silicon wafers. This slide shows the CVD equipment in more detail. The top picture shows a batch of silicon wafers that is ready to be inserted into the fused silica tube. The lower picture shows the silicon wafers that have been moved further in the tube. The yellow color results from the fact that one has switched on the heating elements



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that surround the fused silica tube. After closing of the entrance port, the carrier gas enters the deposition chamber and one can very accurately control flow and temperature conditions. Evidently, CVD thin films are grown on all exposed surfaces within the tube. We will now discuss in a very schematic way what happens in a CVD process. To this purpose we have drawn here a wafer positioned on a heating element.

The goal is to deposit by CVD a thin film on the wafer. The wafer and heater are positioned in a reactor chamber from which we can evacuate all residual gasses by pumping. We show here the reactor chamber that has been filled with a controlled gas atmosphere. There is a gas flowing into the reactor which undergoes a chemical reaction at the heated wafer's surface, which leads to the deposition of a thin film.



Aspects of CVD

- **Thermodynamics** of the chemical reaction: a solid product should be formed at the wafer temperature
- Thin film **growth kinetics**: the reaction should proceed fast enough
- **Gas flow** conditions: when flowing over the wafer, the gas is gradually depleted, yet the wafer should be uniformly covered

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As side products of this chemical reaction gaseous products are produced that are evacuated from the chamber. Different physical principles or aspects are involved for understanding a CVD process. First, one should understand the thermodynamics of the chemical reaction itself. It should be energetically favorable

$$t_{film}(x) = e^{-\frac{E_{activ}}{k_B T}} \times P_{growth} \times C_{gas}(x)$$

Aspects of CVD:

- **Thermodynamics** of the chemical reaction: a solid product should be formed at the wafer temperature
- Thin film **growth kinetics**: the reaction should proceed fast enough
- **Gas flow** conditions: when flowing over the wafer, the gas is gradually depleted, yet the wafer should be uniformly covered

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to produce a solid thin film reaction product on the wafer from the gas. Next, the CVD process should show favorable growth kinetics. This means that the reaction should proceed sufficiently fast so that the waiting time for depositing a thin film is not too long. A third important aspect of a CVD process is how the gas flow occurs. When the gas is flowing over the wafer's surface, it will be gradually depleted. However, it is required that a thin deposited film has everywhere the same thickness. Gas flow conditions should be such that this is enabled. If x is the coordinate in the horizontal plane in the direction of the flow, the thin film thickness, as a function of x , is influenced by the just-mentioned fundamental aspects of CVD. Thermodynamics provides an exponential factor which contains the activation energy needed to go from the gaseous to the solid phase as well as the thermal energy. The hotter the wafer becomes, the higher the growth rate will be, in principle. The next aspect in the CVD process is the growth kinetics. If a thermodynamically stable reaction product can be formed in the process this does not say a lot on the rapidity of the deposition.

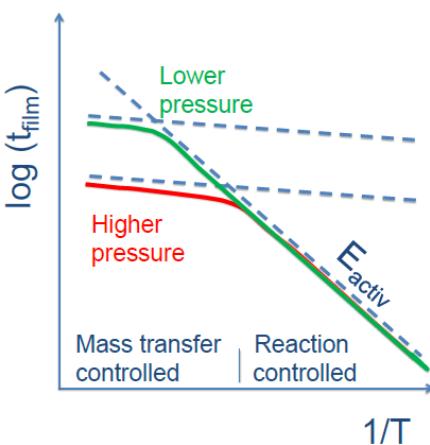
$$t_{film}(x) = C_{gas}(x) \times P_{growth} \times e^{-\frac{E_{activ}}{k_B T}}$$

- At high temperature, growth is in the **mass transport-limited regime**
→ control of gas flow and pressure is crucial for obtaining uniform films
- At low temperature, growth is in the **reaction-limited regime**
→ control of local temperature is crucial for obtaining uniform films
- A low gas pressure is beneficial for good film uniformity and step coverage

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Nucleation of solid material and further growth can be slow and need to be evaluated experimentally. This adds the probability factor P_{growth} to the formula for the thickness of the thin film. Finally, the thin film thickness at the position x is a function of the gas concentration at that point. Mostly one wants that the film thickness is everywhere the same so the gas flow conditions and the gas concentration ideally should not depend on x . We have written here again the formula for the film thickness. It was already clear that for the reaction to occur, a high temperature of the wafer is needed.



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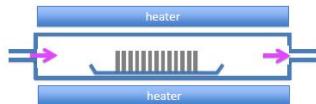
In practice, temperatures ranging from a few hundred degrees Celsius to almost a thousand degrees Celsius can be used. If one is at very high temperatures there is a lot of thermal energy, kT , and the reaction proceeds very fast due to the exponential factor. In this case, the control of the gas flow is very important as the local thin film thickness will be proportional to the local gas concentration. The gas concentration, hence, has to be uniform everywhere in the vicinity of the substrate. If one is at moderately high temperature, the film growth and the chemical reaction will not proceed that fast. The exponential factor in this case is limiting the growth rate while the gas usually has a uniform concentration within the reactor.

- Atmospheric pressure CVD (APCVD)
- Sub-atmospheric pressure CVD (SACVD)
 - $1000 \text{ mbar} > P > 10 \text{ mbar}$
 - Reduction of unwanted gas phase reactions
 - Improvement of film uniformity across the wafer
- Low-pressure CVD (LPCVD)
 - $1 \text{ mbar} > P > 0.1 \text{ mbar}$
- Ultrahigh vacuum CVD (UHV/CVD)
 - Initial vacuum of $10^{-7} - 10^{-8} \text{ mbar}$; growth at $P \sim 10^{-3} \text{ mbar}$
 - No gas phase reactions
 - No gas boundary layer near wafer surface, but molecular flow transport

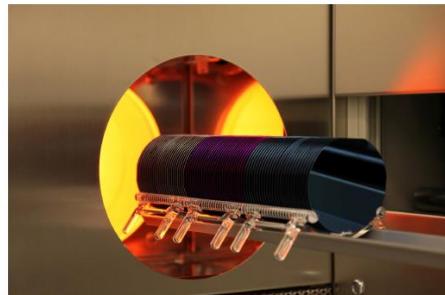
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In these conditions, the local temperature should be very well controlled as a small temperature variation evidently will give a variation in grown film thickness. Finally, one can say that, at low gas pressure, good film uniformity can be better obtained. Indeed, at low gas pressure, the mean free path of the gas molecules is long so that a short distance local variation of the gas concentration is less important.

Hot wall tube reactor



- Wafers are placed in a fused silica boat that is inserted in a fused silica tube
- Whole system is heated
 - Uniform temperature
 - Possible deposition on walls

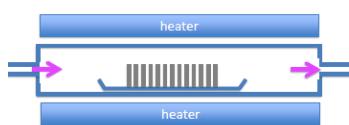


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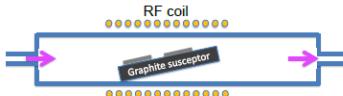
This schematic figure shows the thin film thickness on a logarithmic scale against the inverse of the temperature. When plotted this way one sees from the exponential facto that a linear slope will correspond to the activation energy of the chemical reaction. If one increases the temperature the film growth rate will go up, but ultimately the gas flow cannot provide sufficient concentration of molecules and the curve will adapt to a much flatter slope. So one can easily discriminate from such a plot the mass transfer controlled and the reaction controlled deposition regimes. Suppose the red curve was obtained at higher gas pressure. If one decreases the gas pressure, the deposition will stay longer in the reaction controlled regime. Despite the fact that there are fewer molecules at a lower pressure, the mean free path in the gas is higher so that gas molecules that come from further away from the substrate can be used in the reaction. Because pressure plays such an important role, CVD processes are typically classified according to the pressure at which the deposition takes place. The first technique is called atmospheric pressure CVD or APCVD which, as the name says, uses a gas at atmospheric pressure. The next technique is called sub-atmospheric pressure CVD or SACVD and the pressure of the gas is typically in between 1000 millibar and 10 millibar. The advantage of having a lower pressure

Hot wall tube reactor



- Wafers are placed in a fused silica boat that is inserted in a fused silica tube
- Whole system is heated
 - Uniform temperature
 - Possible deposition on walls

Cold wall tube reactor



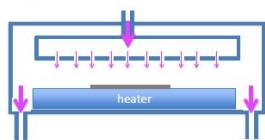
- Wafers are placed on a graphite susceptor that is tilted to reduce downstream depletion of the gas
- Graphite with wafers is inductively heated
 - Locally high temperature and gradient
 - No deposition on walls

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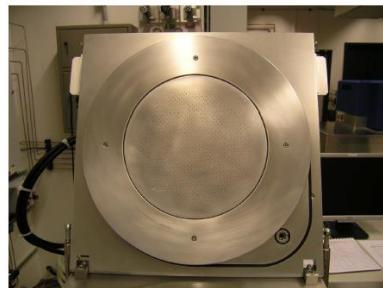
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is that interaction between different gas molecules is less probable so that there is less probability for unwanted particle synthesis in the gas itself.

Showerhead reactor



- Wafer is placed on a local heater
- 'Shower' of gas exposes the wafer

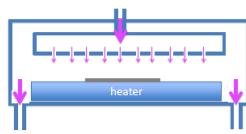


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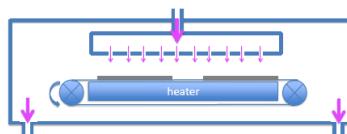
Also, because of the increased mean free path of the gas molecules local variation in gas concentration is reduced so that the film thickness across the wafer is more uniform. The next technique is low-pressure CVD or LPCV which typically operates in between 0.1 millibar and 1 millibar. Finally, we have ultrahigh vacuum CVD or UHV/CVD a technique in which the reactor first is pumped down to a very low pressure after which the growth of the thin film takes place at a pressure of 10^{-3} millibar, typically. In this case there is very little interaction between the gas molecules so that the gas behaves less like a viscous liquid but more like an ensemble of individual molecules. CVD processes are often categorized according to the reactor type in which they are performed. The first reactor type is called the hot wall tube reactor as we have already seen in the pictures before. In such a reactor, the wafers are placed in a fused silica boat that is to be inserted in the fused silica tube. After that, the complete system is heated so every part is at the same temperature and deposition will be uniform if the gas concentration is sufficient.

Showerhead reactor



- Wafer is placed on a local heater
- 'Shower' of gas exposes the wafer

Conveyor belt reactor



- Wafers are placed on transport belt situated above a local heater
- Increased wafer throughput

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Note that in this case, deposition also will occur on the walls of the system. Another type of CVD system is called the cold wall tube reactor. In this case, there is no external heater that heats up the complete system, but the wafers are positioned on a conducting graphite susceptor which is heated using an external RF coil. In this case, there is only locally a high temperature and there is a strong temperature gradient. There will be no deposition on the walls of the system and the graphite susceptor is tilted with respect to the direction of the flow typically, to take into account eventual gas depletion effects that would give a thinner film if one goes further downstream of the flow. In such a configuration, the wafers will be exposed always to a fresh stream of gas. This picture shows the principle of a so-called showerhead reactor. The gas enters a dedicated space within the reactor and exposes the wafer via a multitude of small holes like a shower of gas. The same principle is used for this so-called conveyor belt reactor in which the wafers are positioned on a transport belt and led over a heater. The wafer throughput of such a system evidently will be higher so this is a system that is more suitable for industrial production. This ends our introduction on CVD. We explained the basic parameters of CVD reaction and process.

and pointed out the various factors by which the film thickness can be controlled such as the temperature and the local gas pressure. We introduced different types of CVD processes according to the pressure at which the deposition takes place. Also, we have introduced some of the common CVD reactor types.

- Basics of CVD
- Factors controlling film thickness
- CVD processes classified according pressure
- Common CVD reactor types

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Practice quiz basic principles of CVD and CVD reactors

Questions:

1. Which is a key advantage of CVD as a thin film deposition method?
 - Efficient consumption of the gas in a uniformly heated reactor
 - Conformal material deposition across all surfaces of the substrate
 - Precursors used in CVD are rarely toxic or corrosive
 - All CVD processes operate at low temperatures, which are not harmful to substrates
2. What is correct in saying about the deposition rate of a thin film?
 - Local variations in the gas concentration occur less at lower pressure, in which case more uniform deposition rates can be achieved
 - A higher gas flowrate decreases the film deposition rate
 - If gas pressure is lowered at constant temperature, a deposition which is in the mass-controlled regime can never shift to the reaction-controlled regime
 - As the activation energy of the reaction increases, the deposition rate increases



Chemical Vapour Deposition 2

Micro and Nanofabrication

Prof. Jürgen Brugger & Prof. Martin A. M. Gijs

In this second lesson on Chemical Vapor Deposition we will discuss in somewhat more detail, common types of CVD processes. First, we will discuss the CVD as operated at different operating pressures. First technique is called Atmospheric Pressure CVD , or APCVD. Then, Sub-atmospheric Pressure CVD, or SACVD, followed by Low Pressure CVD, or LPCVD, and finally, Ultra High Vacuum CVD, for the lowest pressure used. Next, we will discuss a technique called Plasma-enhanced CVD, or PECVD. And finally, the technique Metal organic CVD, or MOCVD. This slide is taken from the first lesson and lists again the different CVD techniques according to the pressure of the gas used for deposition. The first technique is practiced at atmospheric pressure. SACVD is at lower pressure, down to 10 millibar. And low pressure CVD is in between 1 millibar and 0.1 millibar. While ultrahigh vacuum CVD is using very high initial vacuum but standard growth is typically performed at 10 minus 3 millibar of gas pressure. In atmospheric pressure CVD, the high pressure of the gas that is used leads to fast film growth rates. Typically microns per minute. This leads to a high consumption of gas and often a carrier or diluent gas is used like nitrogen or hydrogen.

- CVD at different operating pressures
(APCVD; SACVD; LPCVD;
UHV/CVD)
- Plasma-enhanced CVD (PECVD)
- Metal-organic CVD (MOCVD)

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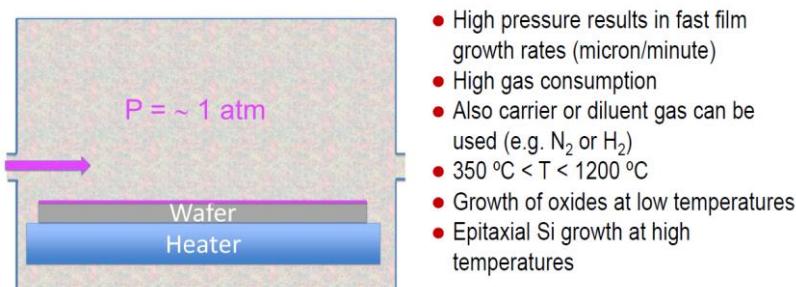
Typical deposition temperatures are between 350 degrees Celsius and 1200 degrees Celsius. The technique is used for growing oxides at lower temperatures and also for the growth of epitaxial silicon films on silicon substrates at higher temperatures. At the high temperatures that are used, film growth is in the mass transport-limited regime. Therefore gas flow control and local concentration of the gas is very important. To enable a good control of the gas flow, the wafer is placed horizontally so that the flow smoothly passes over it in a very controlled way. However, not so many wafers can be used at the same time as the exploitable surface in the reactor is basically limited by the area of the heater. As a consequence, the throughput of this technique is limited. A possible disadvantage of this technique is that the reaction may already start in the gas phase itself, rather than on the substrate. So there is formation of particles in the gas. This results in

deposition of unwanted precipitates on the wafer. And when continuing the deposition, this results in non-uniformities, or pinholes in the deposited film. In sub-atmospheric pressure CVD, the gas concentration is reduced. And also the deposition rate decreases but due to the larger mean free path of the gas inhomogeneities in the concentration are less important and more uniform films are grown. Also as the gas molecules have less probability for interaction, no or very little particles are formed. Still wafers need to be placed horizontally occupying a lot of surface and resulting in a relatively low throughput of the deposition process. In low-pressure CVD, the pressure of the gas is further reduced, leading to still longer mean free paths, and has an increased diffusion. Also, no gas concentration gradient is present perpendicular to the flow direction,

- Atmospheric pressure CVD (APCVD)
- Sub-atmospheric pressure CVD (SACVD)
 - $1000 \text{ mbar} > P > 10 \text{ mbar}$
 - Reduction of unwanted gas phase reactions
 - Improvement of film uniformity across the wafer
- Low-pressure CVD (LPCVD)
 - $1 \text{ mbar} > P > 0.1 \text{ mbar}$
- Ultrahigh vacuum CVD (UHV/CVD)
 - Initial vacuum of $10^{-7} - 10^{-8} \text{ mbar}$; growth at $P \sim 10^{-3} \text{ mbar}$
 - No gas phase reactions
 - No gas boundary layer near wafer surface, but molecular flow transport

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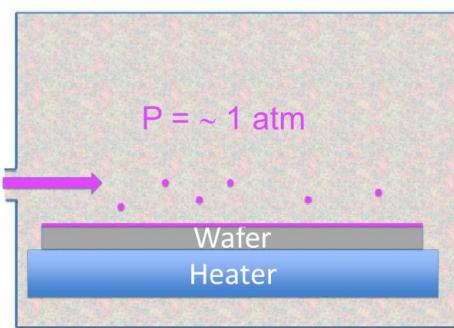
except of course the gradient that will develop very close to the wafer where deposition occurs. More uniform films can be deposited and typical growth temperatures are in between 400 degrees Celsius and 900 degrees Celsius. Growth of the film is in the reaction-limited regime, hence a precise temperature control is very important because the temperature variation immediately results in a changing reaction rate. Usually the LPCVD technique has 10 to 100 times lower deposition rates compared to APCVD. Due to the low pressure and the resulting homogenous gas conditions, wafers can be stacked vertically in batches, occupying less horizontal space. Therefore, in LPCVD, the wafer throughput can be enhanced. Wafers that are situated more upstream of the gas flow may be exposed to a higher concentration of gas than wafers that are placed further downstream. This would result in a different film thickness, but this gas depletion effect can be compensated by establishing with a heater system, a slightly higher temperature further downstream of the flow, so that the film thickness becomes uniform. In ultrahigh vacuum CVD, the molecular mean free path is as big as the reactor dimension itself. The gas behaves not so much as a viscous liquid but as a collection of individual molecules. There are no gas-phase chemical reactions and a typical temperature for operation is between 500 and 600 degrees Celsius.



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Due to the high initial vacuum, the partial pressure of contaminant gasses is reduced so that one can deposit during longer times at lower temperature without incorporating too much impurity molecules in the grown film. Keeping a low temperature during growth can be important for sensitive semiconductor micro-

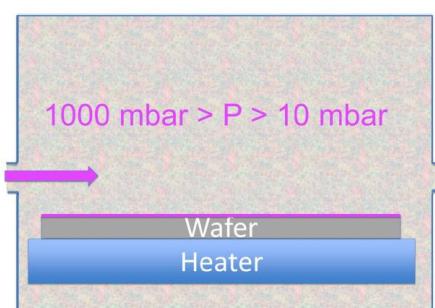
fabrication processes, where a too high temperature may result in too high diffusion of active dopants. Plasma-enhanced CVD is based on the LPCVD configuration we discussed before. The difference is that now a radio frequency power can be coupled via two electrodes into the gas. And typically this is done at a frequency of 400 kilohertz or 13.5 megahertz. The RF power induces a plasma, which is a partially ionized gas, containing ions, electrons, and neutral excited gas molecules. It can be perceived in the reactor by the gas that is lighting up. The light is caused mostly by accelerating free electrons, but all molecules in the plasma become agitated as a result of the applied RF power.



- At high temperature, growth is in the mass transport-limited regime → gas flow control is very important
- Wafer is placed horizontally in the gas flow → limits throughput
- Reaction may already start in the gas phase, resulting in unwanted precipitates on the wafer → non-uniformities or pinholes in deposited film

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As the film growth is in the reaction-limited regime, the exponential factor that contains the reaction activation energy and the temperature plays an important role. Schematically, one can imagine that without plasma there is initially a gas molecule that then, by a temperature fluctuation, has to acquire sufficient energy to be converted to a metal atom in this example. If now the RF plasma is switched on, all molecules gain in energy as indicated on the red curve, so energy goes up everywhere. As a result, the effective activation energy for the reaction to occur is lower-- the barrier height is lower. This immediately leads to a thin film growth that becomes possible at lower temperatures than before without the plasma. So in PECVD, deposition is done typically at lower temperature. Therefore with this technique substrates do not need to be heated as much as an LPCVD for the reaction to occur. So one has a wider choice of substrate materials. In this graph we show again the Arrhenius plot of the film growth rate, indicating the mass transfer controlled and the reaction controlled regimes. This was the case without using RF power. We have now switched on the RF power in the PECVD system and obtained the red curve for the thin film thickness. The slope of the red curve is not as steep because the slope gives the effective activation energy of the chemical reaction which is lower for the PECVD deposition. Also one observes that there is a more appreciable growth rate or film thickness



- Reduced gas consumption
- More uniform films grown
- No particle formation
- Wafers still horizontally placed → low throughput

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at lower temperatures-- that means at higher $1/T$ values. The last technique that we will discuss in this lesson is metal organic CVD, or MOCVD. This technique is also called, metal-organic vapour phase epitaxy. Here one wants to deposit certain metals from liquid precursor molecules that normally are not in the gaseous phase. To lead these molecules to the substrate, one uses a carrier gas, like hydrogen, that bubbles

through the precursor liquid and in that way one transfers the precursor molecules towards the substrate. Here we give an example in which trimethylgallium or trimethylindium is transported to the reactor. In parallel there is a line where the gaseous products arsine or phosphine can be led to the reactor chamber. Doing so one can deposit compound semi-conductors, like gallium arsenide or indium phosphide.

Typical growth temperatures are between 300 and 500 degrees Celsius. The vapor pressure of the metal-organic source is a critical parameter and also due to the use of the very toxic precursor compounds, safety aspects generally are very important in MOCVD deposition. This video shows a typical MOCVD equipment.

The MOCVD reactor itself, reagent sources, and supply lines are all inside of a cabinet that is isolated from the outside to avoid release of toxic products into the environment. One can manipulate items inside the cabinet via the use of gloves that are attached to the cabinet. We see here an operator who accesses the inside and in particular he opens the MOCVD reactor itself to take out a wafer after a deposition run. In this lesson we have given an overview of most common CVD processes as classified by the reactor operation pressure. These were atmospheric pressure CVD, sub-atmospheric pressure CVD, low pressure CVD, and ultrahigh vacuum CVD. We also introduced plasma-enhanced CVD, where the use of RF power results in a smaller effective activation energy for the chemical reaction so that deposition of the thin film can take place at lower temperature than in the LPCVD reactor. Finally, we introduced metal-organic CVD.

Practice quiz CVD techniques at different operating pressure, plasma-enhanced CVD and metal-organic CVD

Questions:

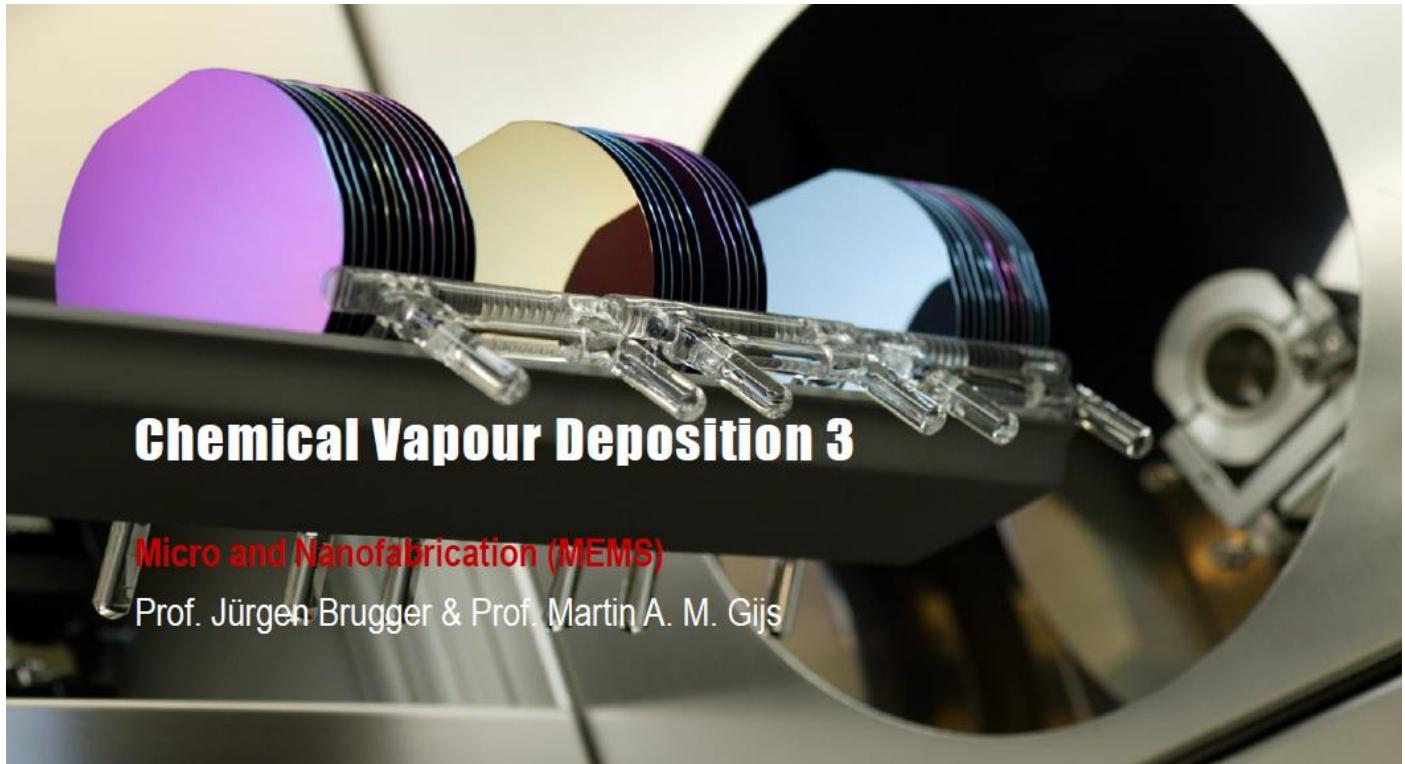
1. As the pressure in a CVD reactor is reduced well below 1 atmosphere, which of these statements is correct?

- Diffusional gas transport becomes less important
- The wafers can be stacked in vertical direction, so the throughput increases
- There are more fluctuations in gas pressure, which result in less uniformly deposited films
- Gas phase reactions become more and more important

2. Which is a critical advantage of plasma-enhanced CVD?

- Film growth is possible at lower temperatures
- The deposition is always in the mass-controlled regime
- Wafer throughput increases
- Thin films can be selectively deposited on the substrates surface

Atomic layer CVD (ALD) and thermal oxidation of silicon:

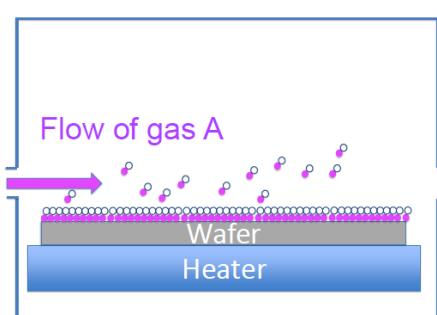


In this lesson, we will discuss two other CVD type deposition processes. The first one is atomic layer CVD, a technique in which a thin film is deposited, atomic layer by atomic layer.

- Atomic layer CVD (ALCVD)
- Thermal oxidation (not truly a CVD process)

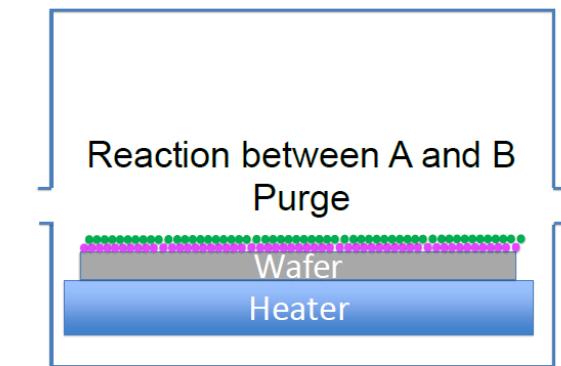
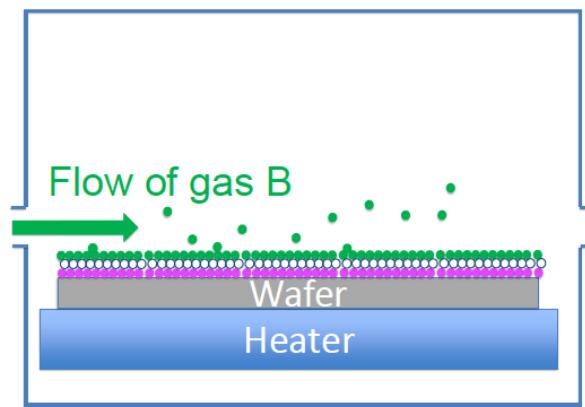
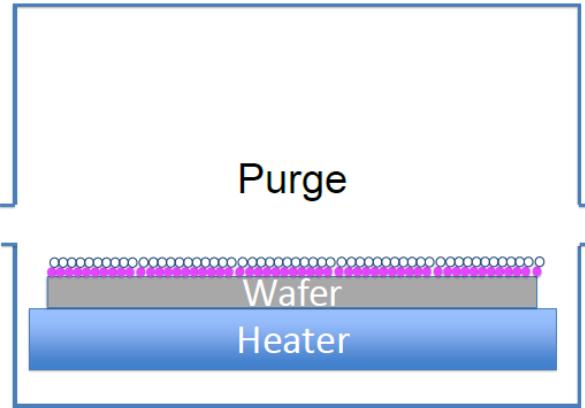
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This technique enables the deposition of extremely thin but continuous films without pinholes. The second technique is thermal oxidation. Here one leads oxygen gas into the reactor, which, at high temperature, oxidizes a surface of a silicon wafer.



- Individual application of two reactant gases A and B allowing sequential formation of layers
- Each of the two reaction steps is self-limiting → one molecular monolayer deposition at a time

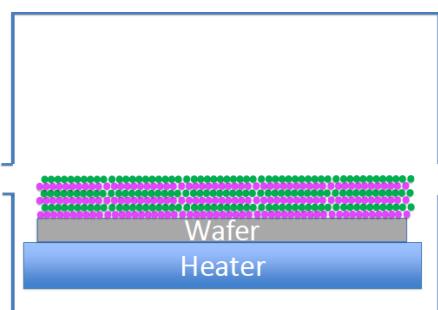
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It is not truly a CVD process in the sense that the silicon top layer is transformed to silicon dioxide, rather than there is a deposition of the oxide material from the gas on top of the substrate. In atomic layer CVD, we still have a heated wafer on which a chemical reaction starting from a gas is performed. The thin film is deposited by sequential deposition of atomically thin layers of two types of materials A and B. The characteristic of this process is that each of the two reaction steps is self-limiting. This means that once a monolayer is deposited, the reaction stops, like you see here, schematically for the gas A. When all the surface is covered with the molecules of type A, the residual gas within the reactor is purged by an external pump. Next follows exposure of the substrate to a flow of gas B. Gas B is chosen so that it chemically reacts with gas A. A monolayer of the gas B reaction product is deposited. Due to the high temperature of the wafer, a chemical reaction between A and B occurs, and the gaseous reaction byproducts are pumped away from the reactor. One has now deposited a continuous monolayer of the AB reaction product. This process is repeated as many times as required for depositing an aimed film thickness. The technique is very interesting for production of very thin conformal films with an atomically well-defined precision. Each

biolayer reaction is self-limiting. This means that the reaction stops once all reactive sites on the surface of the wafer are occupied. An example of atomic layer CVD is the use of three metal aluminum and water vapor exposure sequences to generate very thin aluminum oxide dielectric films. Silicon dioxide, or silica, is an extremely important material in microfabrication technology.

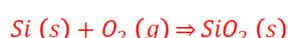
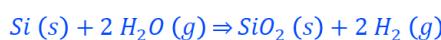
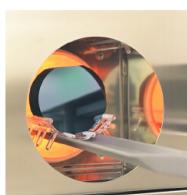


- Process is repeated generating a sequence of layers
- Technique to produce very thin, atomically specified conformal films
- Reaction is self-limiting, i.e. it stops once all reactive sites on the surface of the wafer are occupied
- Example: trimethyl aluminium $[Al(CH_3)_3]$ and H_2O vapour exposure sequences to form very thin and continuous Al_2O_3 dielectric films

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Thin oxides are used as dielectric in transistors, while thick oxides are widely used as protective coatings and for electrical isolation. Two types of thermal oxidation exist. In the first type, called wet oxidation, silicon is exposed to water vapor at high temperature, so that it oxidizes to silicon dioxide under generation of hydrogen. In so-called dry oxidation , the silicon reacts with oxygen to give directly the oxide.



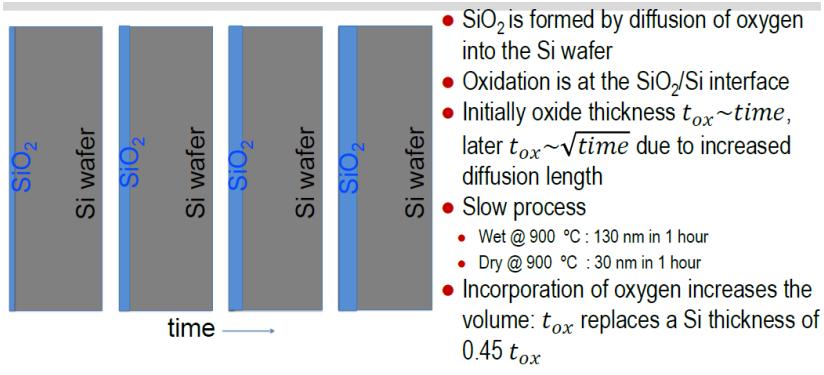
- SiO_2 is an extremely important material in silicon technology
 - Thin oxides (1-20 nm) are used as dielectric in transistors
 - Thick oxides (100-1000 nm) serve as protective coatings and for electrical isolation
- In thermal oxidation, silicon is transformed into its oxide at high temperature ($850^\circ C < T < 1100^\circ C$) using either water vapor ("wet oxidation") or oxygen ("dry oxidation").
- Water vapor is produced by combustion of H_2 and O_2 in a torch

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The water vapor that is used in the chemical reaction results from a combustion process of hydrogen and oxygen gas in a torch, as we will see later. This slide shows schematically the thermal oxidation mechanism.

In the beginning, the silicon atoms at the surface are easily oxidized. Later, when one continues in time, the oxide layer becomes thicker and thicker, and it becomes more difficult for the oxygen to diffuse through the thicker oxide layer, to reach the silicon surface. That is why, initially, the oxide thickness is proportional to the time of the process, but later oxidation is slower, and goes with the square root of time . Overall, it is a slow process. For wet oxidation, at $900^\circ C$, we have an oxidation rate of 130 nanometers in one hour, while for dry oxidation, it is only 30 nanometers for one hour. One should also note that because oxygen is incorporated in the silicon lattice, the volume of the material increases so that if one has an oxide thickness called t-ox , this corresponds to an initial silicon thickness of only 0.45 t-ox. So really the volume of the silicon is increased into a bigger volume of silicon dioxide. Here we show one slide that was discussed in our case study of the thermal mechanical micro-actuator.



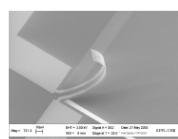
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Thermal oxidation was used in this microfabrication process to generate the oxide material from the silicon wafer to form the beam on which later the chromium heating element was patterned. This slide is a reminder of the concern micro-fabrication step. In the picture, we see different oxide thicknesses. In the middle, the silicon wafer has no oxide. Different thicknesses can be well discriminated by the different colors which originate from optical interference effects in the oxide layer. Thermal oxidation is also used in silicon integrated circuit technology. It can be used to define very thick oxide layers, the aim of which is to isolate the substrate from conducting layers. These conducting layers are deposited on the thick silicon dioxide

- At the micrometer scale

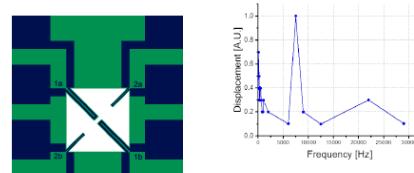
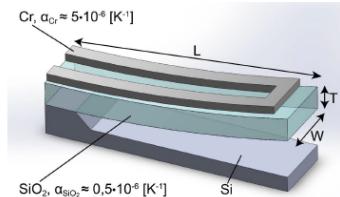
- Stress in thin films
- Applying voltage to Cr wire
- Joule heating
- Thermal expansion
- Bending the cantilever
- Pros: high amplitude and force ratio
- Cons: power dissipation and dynamic range
- Reliability: electromigration



$$k = \frac{3EI}{L^3}$$

$$\omega_{res} = \sqrt{\frac{k}{\beta m}}$$

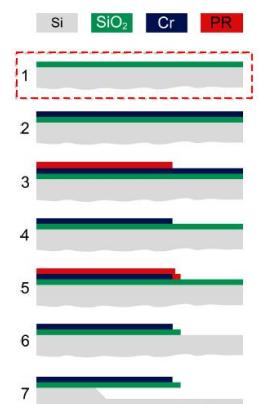
k: spring constant [N/m]
 E: Young's modulus [N/m²]
 I: area moment of inertia [m⁴]
 L: length of the beam [m]
 ω_{res} : resonant angular frequency [s⁻¹]
 β: correction factor for distributed mass
 m: beam mass [kg]



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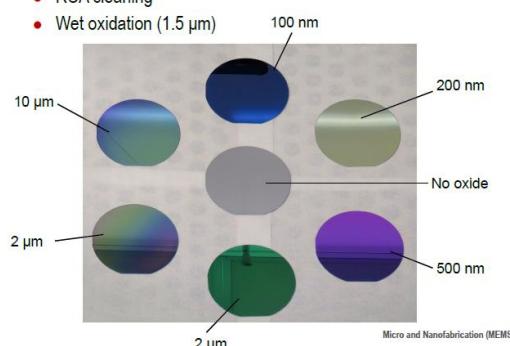
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and have then a low parasitic capacitance with the substrate due to the high thickness. To only locally deposit this thick oxide, one uses a silicon nitride mask. So here the silicon nitride mask is deposited on a very thin oxide layer. This mask is nontransparent to diffusing oxygen atoms; it is very inert. Because a thermal diffusion process is omnidirectional, one obtains an oxidation profile like shown in this scheme.



Step 1: wafer preparation & wet oxidation

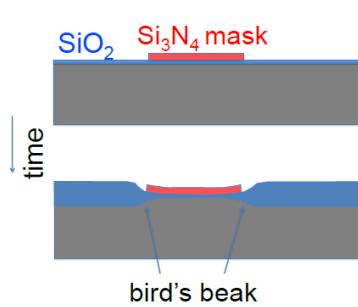
- RCA cleaning
- Wet oxidation (1.5 μm)



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This particular shape is called the bird's beak in silicon technology. Due to the bigger diffusion distance, it becomes more and more difficult for the oxygen to penetrate underneath the silicon nitride mask, and this gives this oxide this particular shape. Because the oxidation is only at specific places ,namely, those where there is no nitrite, this process is called ,local oxidation of silicon, or also the LOCOS process.



- $\text{SiO}_2/\text{Si}_3\text{N}_4$ mask forms a local barrier against diffusion of oxygen into the Si wafer
- However, limited diffusion can take place underneath the edge of the mask
- Volumetric increase of oxide with respect to Si results in the formation of the "bird's beak"
- Advantageous use in microelectronic circuits

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In this lesson, we have seen two CVD type techniques. The first one is atomic layer CVD for formation of very thin continuous layers. And the second one is thermal oxidation, which is not a true CVD process, but is performed in the same type of equipment as a CVD process.

- Atomic layer CVD for formation of very thin continuous layers
- Thermal oxidation process
 - All-wafer like used for bimorph microactuator
 - LOCOS process like used in microelectronics

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Practice quiz atomic layer CVD (ALD) and thermal oxidation of silicon

Questions:

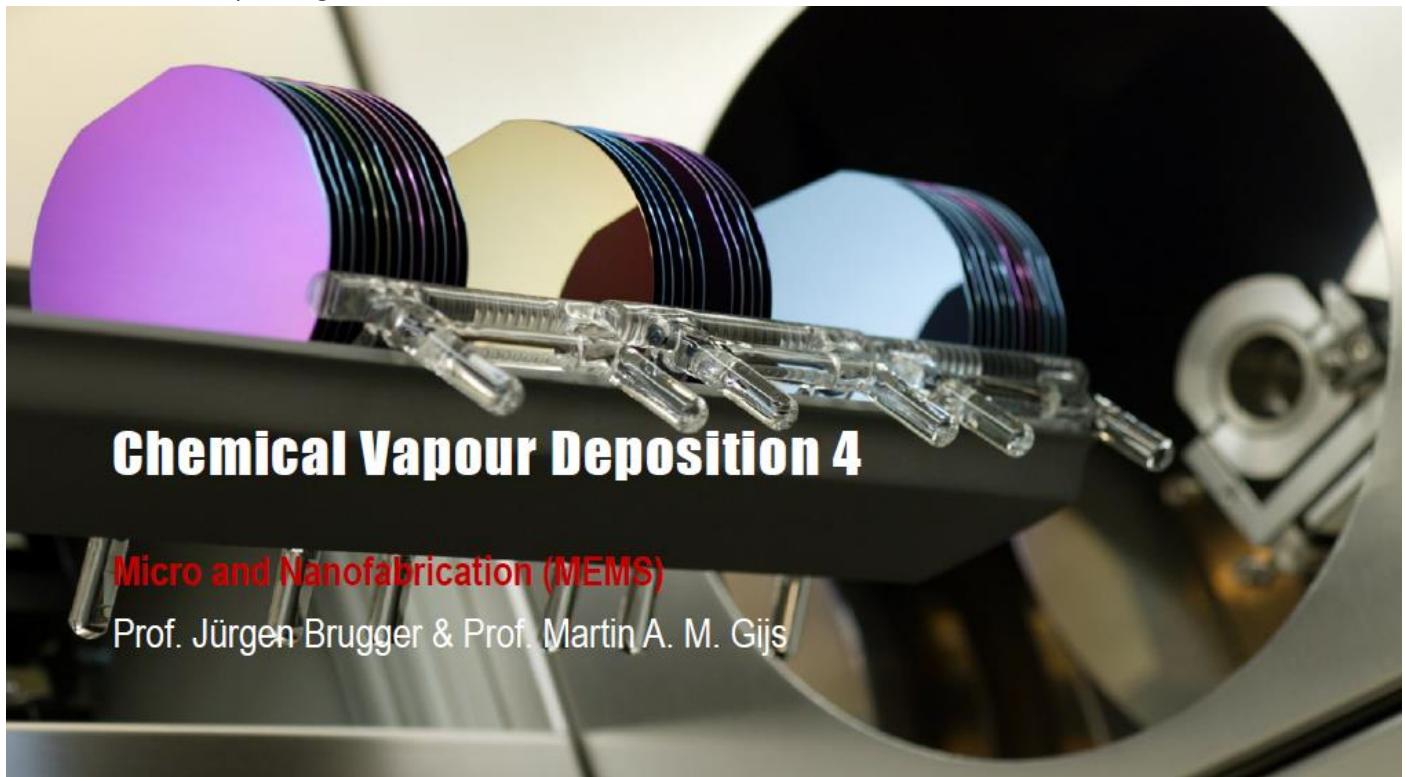
1. What is the meaning of a self-limiting reaction?

- A reaction which has a limited reaction rate due to low precursor concentration
- A reaction which stops once all reactive sites on the surface are consumed
- A reaction which stops once the product density is too high
- A reaction which stops once the precursor is consumed

2. What is limiting the thickness of SiO_2 layers deposited by thermal oxidation?

- The reaction is reversible and finds its equilibrium after a while
- The reaction rate at the surface of the substrate
- After a while, all oxygen in the reactor is consumed
- The long diffusion duration of oxygen molecules through previously oxidized silicon

Theoretical concepts of gas flow in CVD reactors:

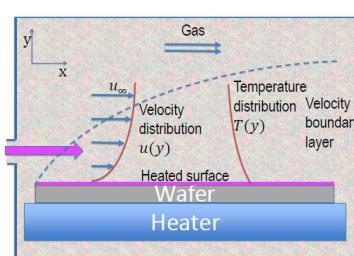


In this lesson, we will introduce some important theoretical concepts that play a role in CVD.

- Velocity boundary layer near a substrate
- Concentration boundary layer near a heated substrate
- Role of the Reynolds number in mass transport

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These are related to the flow of the gas over the heated substrate. Due to friction forces at the substrate, the velocity is essentially zero, and only when going sufficient distance away from the substrate, when we will reach the velocity of the gas in the free-flow regime. Also, as one consumes gas molecules in the process, the gas concentration at the substrate will be reduced so that there is not only a velocity boundary layer near the substrate, but also a gas concentration boundary layer. Finally, we will introduce how the concept of the Reynolds number plays a role in gas transport over the substrate. This slide schematically shows the velocity distribution u as a function of the coordinate y perpendicular to the surface. At the surface, the velocity is zero, and when going up in the y direction, one finds back the free-flow velocity, noted here as u -infinite. This velocity gradient develops in a region close to the substrate, and this region is known as the

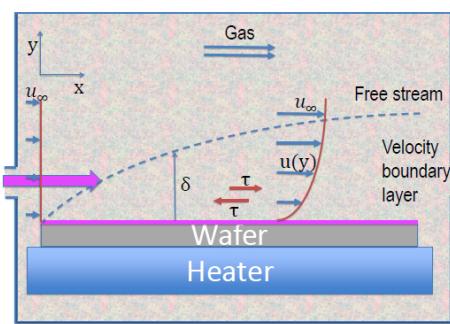


- Gas flowing over a surface at $y=0 \rightarrow$ velocity in the y -direction varies from 0 to value u_∞ at infinity
- Development of **hydrodynamic or velocity boundary layer**
- If temperature gradient, development of **thermal boundary layer**
- **Boundary layer grows** as flow progresses in the x direction

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hydrodynamic or velocity boundary layer. As the wafer is heated, the temperature of the gas close to the wafer will be higher than far away. So there's also a gradient of temperature near the substrate, and this can be associated with the temperature or thermal boundary layer. The boundary layer grows as one advances in the x direction along the flow, as if one goes further, the gas is more and more influenced by layers of gas underneath that have already been perturbed

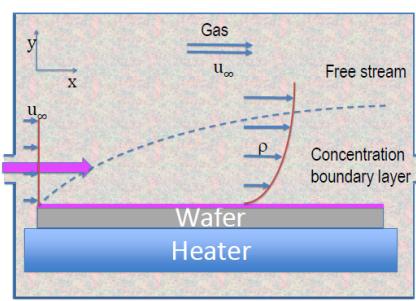


- Retardation of fluid motion associated with **shear stresses τ** acting in planes parallel to the fluid velocity
- $\delta(x)$: **boundary layer thickness**, defined as value for y for which $u(y) = 0.99 u_\infty$
- Boundary layer grows with x , as effects of viscosity penetrate further in the gas stream
- **Two distinct regions** in fluid flow: (i) boundary layer where velocity gradients and shear stresses are large; (ii) the region outside, where these are negligible

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by the viscous flow forces. Here we show the shear stresses, τ , that act on the gas layer. Shear stresses develop as the velocity of the gas layer underneath is lower than this layer and as the velocity of the gas layer above is higher. The dashed line in this diagram is a theoretical curve which corresponds to the coordinates in space where the velocity of the gas is nearly at equilibrium, that is, nearly u -infinite.

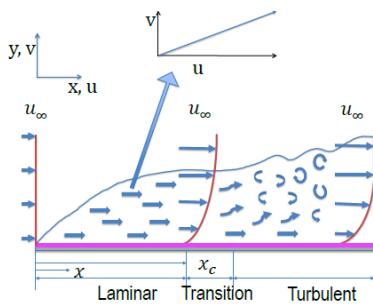


- Gas flows over the wafer surface and is transformed in a solid reaction product
- The gas stream thereby is gradually depleted and a gas concentration gradient $\rho(y,x)$ develops in the boundary layer
- Renewal of the gas from the free stream towards the substrate occurs by diffusion

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One defines this dashed line as the ensemble of all points where the velocity is 99% of the velocity u at infinity. As one goes from the substrate, where there is zero velocity, to this line, where there is 99% of u -infinite, it is clear that shear stresses are much higher in this region for small x than in this region for high x where the same difference in velocity is developed over a much larger distance. This slide shows the concentration boundary layer. During the deposition, due to the consumption of the gas, there is a lower concentration of gas near the wafer. This depletion effect of the gas is counterbalanced by gas flowing from further away by diffusion towards the substrate. In the same way as for the velocity distribution, one can define the concentration boundary layer. In general, two types of flow behavior can be distinguished in the boundary layer. For small x , the velocity is mainly parallel to the x direction due to the high shear forces in the y direction, because we see much bigger shear here where the boundary layer is smaller.

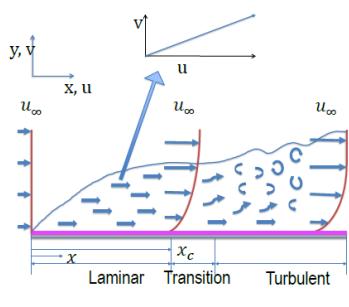


- In general, the boundary layer can be laminar or turbulent
- Laminar**
 - fluid motion is highly ordered
 - clear streamlines
 - presence of velocity component v necessitated by boundary layer growth in x direction
- Turbulent**
 - irregular flow with velocity fluctuations
 - increased surface friction and turbulent mixing
- CVD is normally operated in the laminar flow boundary layer regime

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For higher x , the thickness of the boundary layer is higher so that the shear forces are less important. In this case, turbulent behavior is seen. Somewhere in between is a critical coordinate x_c where the transition from laminar to turbulent behavior takes place. CVD is normally operated in the laminar flow boundary layer regime where flow is more ordered and regular. An important number in hydrodynamics is the Reynolds number which is defined as function of the density of the fluid of the gas in this case, ρ , the velocity denoted by u_∞ and the coordinate along the x direction, x_c . μ is the dynamic viscosity of the gas. Associated with the coordinate x_c , one defines a critical Reynolds number at x_c , and it appears that for all cases, this critical Reynolds number where the transition between laminar and turbulent behavior occurs is at the number 5 times 10 to the fifth. So one can vary density, velocity, or x , or μ . Always, the transition will be for this value of the Reynolds number. Here we want to give a physical interpretation



- The transition between the two regimes is located at x_c and is determined by a critical value of the **Reynolds number**
- $Re_{x,c} \equiv \frac{\rho u_\infty x_c}{\mu}$
with μ [Pas] the dynamic viscosity
- For flow over a flat plate, a representative value for $Re_{x,c}$ is
 $Re_{x,c} \equiv \frac{\rho u_\infty x_c}{\mu} = 5 \times 10^5$

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of the Reynolds number. It can be thought of as the ratio of inertia to viscous shear forces that act on a gas layer element in the boundary layer. An inertial force per unit volume can be written as the derivative in x of the kinetic energy density, and this can be crudely approximated by this formula: average density, average velocity, and L is the dimension of the system in the x direction. A shear force per volume element or per layer of gas can be written as a derivative with respect to y of the viscous shear forces that act on a plane with normal along the y direction. Again, in a very crude approximation, we can write this shear force by this expression with L , dimension of the system, this time in the y direction. Taking the ratio of these two approximative expressions, one obtains this, which is the Reynolds number.

- Re_x may be interpreted as the **ratio of inertia to viscous shear forces** on a gas volume element in the boundary layer

- Inertial force

$$F_i \equiv \frac{\partial[(\rho u)u]}{\partial x} \approx \rho V^2 / L$$

L : system size in the x -direction

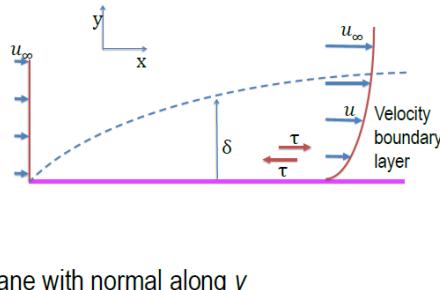
V : mean flow speed

- Shear force

$$F_s \equiv \frac{\partial \tau_{yx}}{\partial y} = \frac{\partial [\mu(\partial u / \partial y)]}{\partial y} \approx \mu V / L^2$$

L : system size in the y -direction

τ_{yx} : shear stress in the x -direction on plane with normal along y



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This gives us following understanding: In any flow there exist small disturbances that can be amplified to produce turbulent behavior. For small Reynolds number, the viscous forces in the beginning for small x are large enough so that this turbulent behavior cannot develop. With increasing Reynolds number, that means with increasing x , the viscous forces become relatively less important with respect to the inertia forces. As the same difference in velocity develops over the much larger boundary layer in the y direction. Therefore, for increasing x above the x corresponding to the critical Reynolds number, small disturbances may be amplified, and turbulent behavior develops.

- Ratio

$$\frac{F_i}{F_s} \approx \frac{\rho V^2 / L}{\mu V / L^2} = \frac{\rho VL}{\mu} \equiv Re_L$$

- In any flow exist small disturbances that can be amplified to produce turbulent conditions
- For **small Re** , viscous forces are sufficiently large relative to inertia forces to prevent this amplification
- With **increasing Re** , viscous forces become progressively less important relative to inertia forces and small disturbances may be amplified

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In this lesson, we have seen an important theoretical concept for understanding chemical vapour deposition, namely the development of the velocity boundary layer in the gas and the gas concentration boundary layer near the heated substrate. Also, we mentioned the role of inertial and viscous forces and the Reynolds number for inducing laminar or turbulent behavior of the gas flow in the boundary layer.

Summary

- Theoretical concepts of the velocity boundary layer and the concentration boundary layer near a heated substrate
- Role of inertial and viscous forces (Reynolds number) in the boundary layer

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Practice quiz theoretical concepts of gas flow in CVD reactors

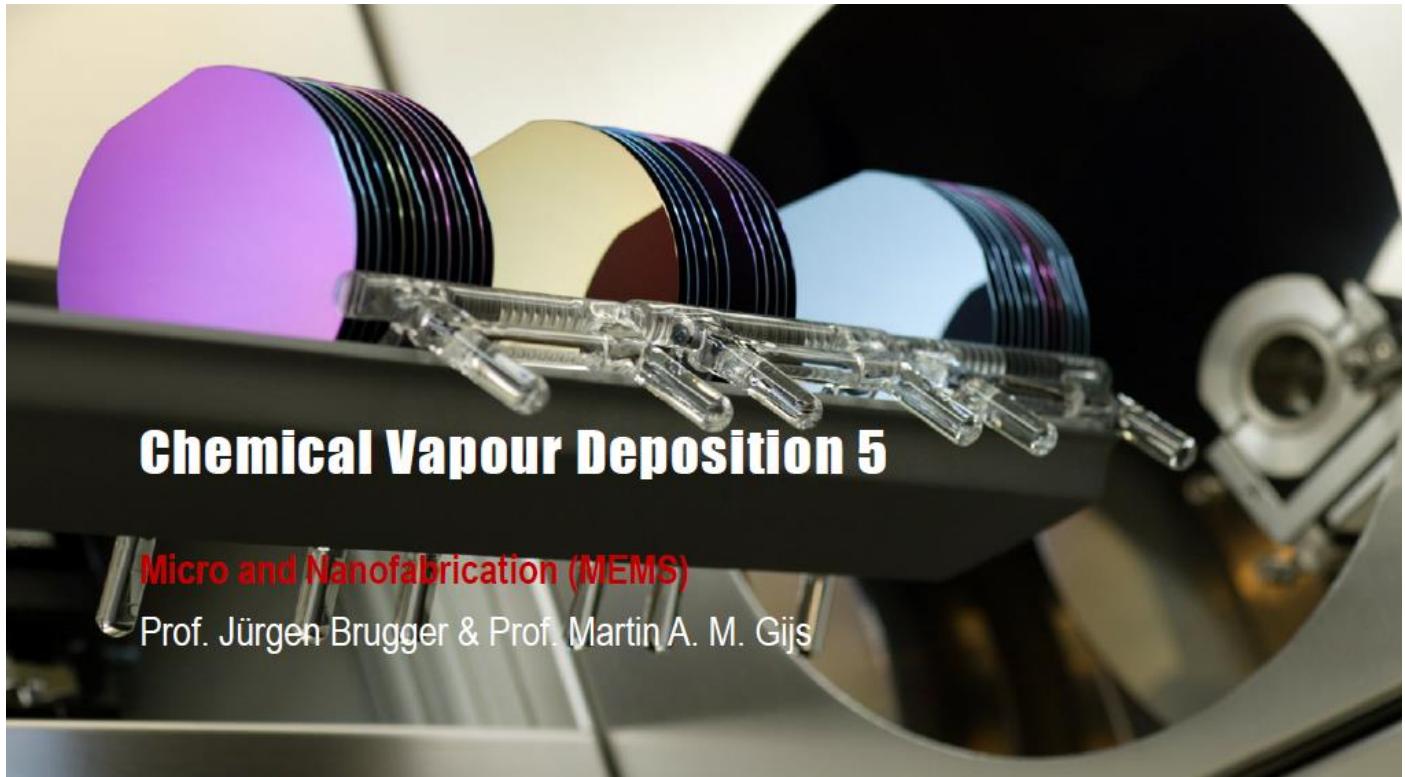
Questions:

1. What can be correctly said about the turbulent regime of the boundary layer?

- Viscous forces become progressively more important than inertial forces when the flow advances along the substrate
- The gas flow is more likely to be turbulent in a larger reactor
- The mean free path of gas molecules is longer than in the laminar regime
- Viscous forces are much larger than inertial forces

2. Which is the origin of shear stress in a gas flow?

- Density variations in the flowing gas
- Fast flowing gases cause local compressions
- Variable gas flow velocities at differing distances from the substrate
- High Reynolds number

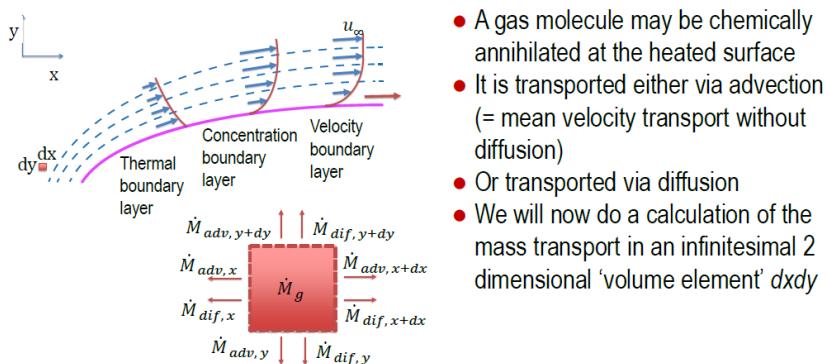


In the previous lesson we have introduced the concept of velocity and concentration boundary layer near a heated substrate during a chemical vapor deposition process.

- Mass transport in the boundary layer
- Modeling of the CVD film growth rate

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Now we will discuss theoretically what is the gas molecule transport from the bulk of the flow through the boundary layer towards the substrate. This transport is key for understanding the growth of the thin film on the substrate. We will subsequently present a simple model for the CVD film growth. If we have a heated surface of an arbitrary shape like represented by the pink line, and if we apply a flow of gas it is already clear that there will be development of a thermal boundary layer in which the temperature varies; of a concentration boundary layer in which the gas concentration varies; and a velocity boundary layer in which the velocity varies. For simplicity, we will do here a two dimensional treatment and we consider an infinitesimal surface element $dxdy$.



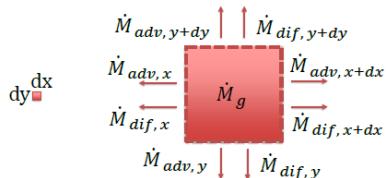
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We will consider now the transport of gas molecules in and out of such element. This element is again drawn here at a bigger scale. The transport can be either by advection-- that is, by an imposed ordered flow-- or by diffusion from all sides. If we have somewhere in our two dimensional surface element the boundary layer of the heated surface-- that means if this element would be here exactly where the pink line is-- then there the gas molecules can be annihilated leading to a deposition event. This expression represents the net rate at which the gas enters the two dimensional surface element due to advection in the x-direction. The first term represents the transport to the line element dy of our infinitesimal surface element with ρu -- the density of the gas-- and u the transport velocity in the x-direction. If we move further in the x-direction to the coordinate $x + dx$, we will have here the second line element dy to which the transport by advection is possible. Because we have moved over the distance dx , the term ρu can be different. That is why we write it as a variational term, as written here in the square brackets. For describing the diffusion through the two dimensional surface element we write Fick's law of diffusion for the transport to the first line element dy .

- Net rate at which the gas enters the control volume due to **advection** in the x-direction:

$$\begin{aligned}\dot{M}_{adv,x} - \dot{M}_{adv,x+dx} &= (\rho u)dy - \left[(\rho u) + \frac{\partial(\rho u)}{\partial x} dx \right] dy \\ &= -\frac{\partial(\rho u)}{\partial x} dxdy\end{aligned}$$



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And using a similar variational approach as before, the second term describes the transport by diffusion through the second line element dy . Here we have written the net transport through the surface element by diffusion in the x-direction. We can do a similar treatment for the y-direction and we define the advection velocity in this direction by v . This gives us eight terms: four advective terms and four diffusional terms. The last term in the equation describes the annihilation of the mass, which is only non-zero when the heated substrate is present in the surface element. Writing all these contributions in the x- and y-direction down, gives us the final equation with the two advection terms and the two diffusional terms and the annihilation term. So this is the equation we need to solve in general. Fortunately we can write this complex equation in a simplified way by assuming that one is close to the surface where there are no advective terms-- that means close to the surface u and v are zero-- and by considering that there is no lateral variation in x , which is a plausible assumption as we have a flat substrate so there is no dependence in the x-direction on the gas density. This equation is then simplified to this one where we only have a variational term in y and the annihilation term. The solution of this last equation is simple. Immediately at the surface where annihilation of the gas can occur-- where this term is non-zero-- this gives us a parabolic shape. Somewhat away from the surface this term becomes zero and this gives us a line.

- Net rate at which the gas enters the control volume due to **advection** in the x-direction:

$$\dot{M}_{adv,x} - \dot{M}_{adv,x+dx} = (\rho u) dy - \left[(\rho u) + \frac{\partial(\rho u)}{\partial x} dx \right] dy \\ = - \frac{\partial(\rho u)}{\partial x} dx dy$$

- Net rate at which the gas enters the control volume due to **diffusion** in the x-direction, using Fick's law of diffusion:

$$\dot{M}_{dif,x} - \dot{M}_{dif,x+dx} = \left(-D \frac{\partial \rho}{\partial x} \right) dy - \left[\left(-D \frac{\partial \rho}{\partial x} \right) + \frac{\partial (-D \frac{\partial \rho}{\partial x})}{\partial x} dx \right] dy$$

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The solution is schematically illustrated here in this diagram. This is the linear solution close to the substrate. In reality, we will have a concentration which gradually approaches the value for the density of the gas that is far away from the substrate, as denoted by the full line here. We now consider that we are in equilibrium conditions and that the density of the gas near the surface is lower than the density of the gas far away, which is logical during a deposition process. We can then write the gas transfer rate per unit surface in three dimensions as following. This is the difference between the surface and the far away concentration of the gas. And this is h -- the mass transfer coefficient. As close to the surface of the substrate there are no advective terms, Fick's law of diffusion should apply which, by equalization to this expression, leads to the value for the mass transfer coefficient h . We see that h is proportional to the diffusion coefficient. We will now find an expression for the diffusion coefficient.

- Net rate at which the gas enters the control volume due to **diffusion** in the x-direction, using Fick's law of diffusion:

$$\dot{M}_{dif,x} - \dot{M}_{dif,x+dx} = \frac{\partial \left(D \frac{\partial \rho}{\partial x} \right)}{\partial x} dx dy$$

- Species conservation requirement in volume element:

$$\dot{M}_{adv,x} - \dot{M}_{adv,x+dx} + \dot{M}_{adv,y} - \dot{M}_{adv,y+dy} \\ + \dot{M}_{dif,x} - \dot{M}_{dif,x+dx} + \dot{M}_{dif,y} - \dot{M}_{dif,y+dy} + \dot{M}_g = 0$$

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If we consider somewhere in the gas plane with a gas density ρ_{minus} at the left and a gas density ρ_{plus} at the right of that plane and if v is the molecular velocity, we can write down the effective number of molecules flowing through the plane by this expression. It is the difference between molecules flowing from left to right and right to left. We can now follow again, a variational approach to write down this difference in which we subsequently equalize the variational distance Δx by l which is the molecular mean free path in the gas. Comparing this expression with Fick's law

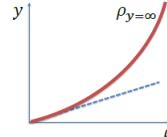
- This becomes

$$\frac{\partial(\rho u)}{\partial x} + \frac{\partial(\rho v)}{\partial y} = \frac{\partial(D \frac{\partial \rho}{\partial x})}{\partial x} + \frac{\partial(D \frac{\partial \rho}{\partial y})}{\partial y} + \dot{n}$$

- Assuming that one is close to the surface with no or little advection ($u=v=0$), and that there is no lateral variation (in the x-direction), this simplifies to

$$D \frac{\partial^2 \rho}{\partial y^2} = -\dot{n}$$

- Exactly at the surface, \dot{n} is constant \rightarrow parabolic $\rho(y)$ concentration dependence. Away from the surface, $\dot{n} = 0 \rightarrow$ linear $\rho(y)$ concentration dependence



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we find that diffusion coefficient is given by the velocity of the molecule times the mean free path of the molecule. Here we repeat the expression we just found for the diffusion coefficient. We can write the mean free path in the gas as function of the temperature and pressure of the gas using the ideal gas law. And we can write the molecular velocity-- which is here-- by the square root of the thermal energy. This provides then the following expression for the diffusion coefficient: $T^{1.5}$ and P^{-1} . Therefore the mass transfer coefficient has the same dependence.

- At equilibrium, the concentration at the surface ($y=0$) is maintained at a uniform value $\rho_{surf} < \rho_{y=\infty}$ and the gas transfer rate per unit surface can be written in three dimensions as

$$\dot{N} [m^{-2}s^{-1}] = h [m s^{-1}] (\rho_{surf} - \rho_{y=\infty}) [m^{-3}]$$

with h the mass transfer coefficient

- If mass flux associated with species transfer is by diffusion, Fick's law applies at the surface

$$\dot{N} = -D \frac{\partial \rho}{\partial y} \Big|_{y=0} \quad h = \frac{-D \frac{\partial \rho}{\partial y} \Big|_{y=0}}{(\rho_{surf} - \rho_{y=\infty})}$$

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We present here again, the formula we have found before for the diffusional flux of molecules through the boundary layer. The second formula describes the flux of reacted molecules that are consumed by the surface reaction, with k_{surf} the surface reaction rate. In equilibrium both fluxes should be the same and this allows us to find an expression for the gas density at the surface in function of h and k_{surf} . By substitution in the first formula of previous slide, we find the following expression for the growth rate. If the mass transfer coefficient by diffusion is much higher than the surface reaction rate, we obtain the film growth rate in the reaction-controlled case from this expression.

- Flow of molecules through a surface in the gas per unit area and time

$$\begin{aligned} J [m^{-2}s^{-1}] &= v [m s^{-1}] (\rho_- - \rho_+) [m^{-3}] \\ &= -v \left(\frac{\partial \rho}{\partial x} \Delta x \right) \approx -vl \left(\frac{\partial \rho}{\partial x} \right) \end{aligned}$$

with l the mean free path in the gas

- Comparing with Fick's law, we find that $D \approx vl$

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Under these conditions there is no dependence on h as sufficient gas is provided everywhere for the reaction to occur. In the opposite case, we have diffusion-controlled film growth and this evidently depends

on h . These theoretical findings allow us to understand the Arrhenius-type plot for the thin film growth, which we have already introduced before, with here the exponential temperature dependence and here the $T^{1.5}$ dependence.

- We just found that $D \approx v l$
- Using the ideal gas law, $l \sim \rho^{-1} \sim (k_B T / P)$
with T and P the temperature and pressure of the gas, resp.
- Moreover, equalizing kinetic and thermal energy in the gas, we find
that $v \sim \sqrt{k_B T}$
- Hence in the gas $D = D_0 T^{3/2} / P$
and therefore the mass transfer coefficient $h = h_0 T^{3/2} / P$

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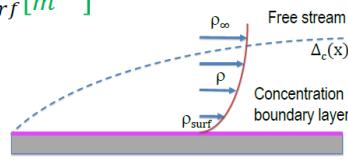
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Finally on this slide we have plotted a number of experimental data of the growth of silicon on a heated substrate. Here one has used silane as a gas and this gas is diluted in hydrogen as a carrier gas. The experimental curves indeed are in line with the result of previous theoretical finding. In this lesson we have discussed gas transport by diffusion in the boundary layer near the substrate during a CVD process.

- Diffusion flux of molecules through the boundary layer
$$\dot{N}_1 [m^{-2}s^{-1}] = h [m s^{-1}] (\rho_{surf} - \rho_{y=\infty}) [m^{-3}]$$
- Flux of reacted molecules consumed by the surface reaction
$$\dot{N}_2 [m^{-2}s^{-1}] = -k_{surf} [m s^{-1}] \rho_{surf} [m^{-3}]$$

with k_{surf} the surface reaction rate

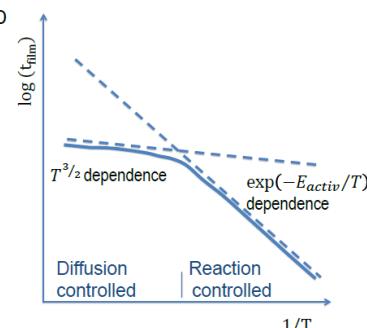
- In equilibrium, $\dot{N} \equiv \dot{N}_1 = \dot{N}_2$, giving
$$\rho_{surf} = \rho_{y=\infty} \left(\frac{h + k_{surf}}{h} \right)^{-1}$$



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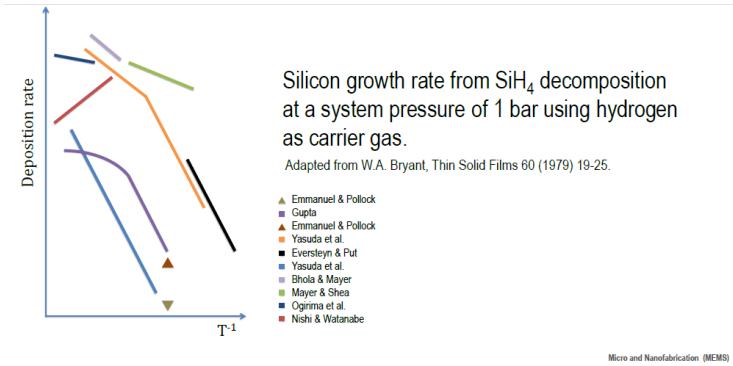
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- The film growth rate is then proportional to
$$\dot{N} = \frac{k_{surf} h}{h + k_{surf}} \rho_{y=\infty}$$
- If $h \gg k_{surf}$, we have the surface reaction-controlled case and
$$\dot{N} = k_{surf} \rho_{y=\infty}$$
- If $h \ll k_{surf}$, we have the diffusion-controlled case and
$$\dot{N} = h \rho_{y=\infty}$$



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We then have written a simplified expression for the mass transport towards the substrate as limited by diffusion. Finally, assuming equilibrium conditions, we have compared a reaction- and diffusion-limited growth rates which have allowed us to understand the dependence of CVD film growth rate as a function of temperature.

Summary

- Gas transport and CVD film growth rate equation
- Reaction- and diffusion-dominated growth regimes

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Practice quiz CVD thin film growth model

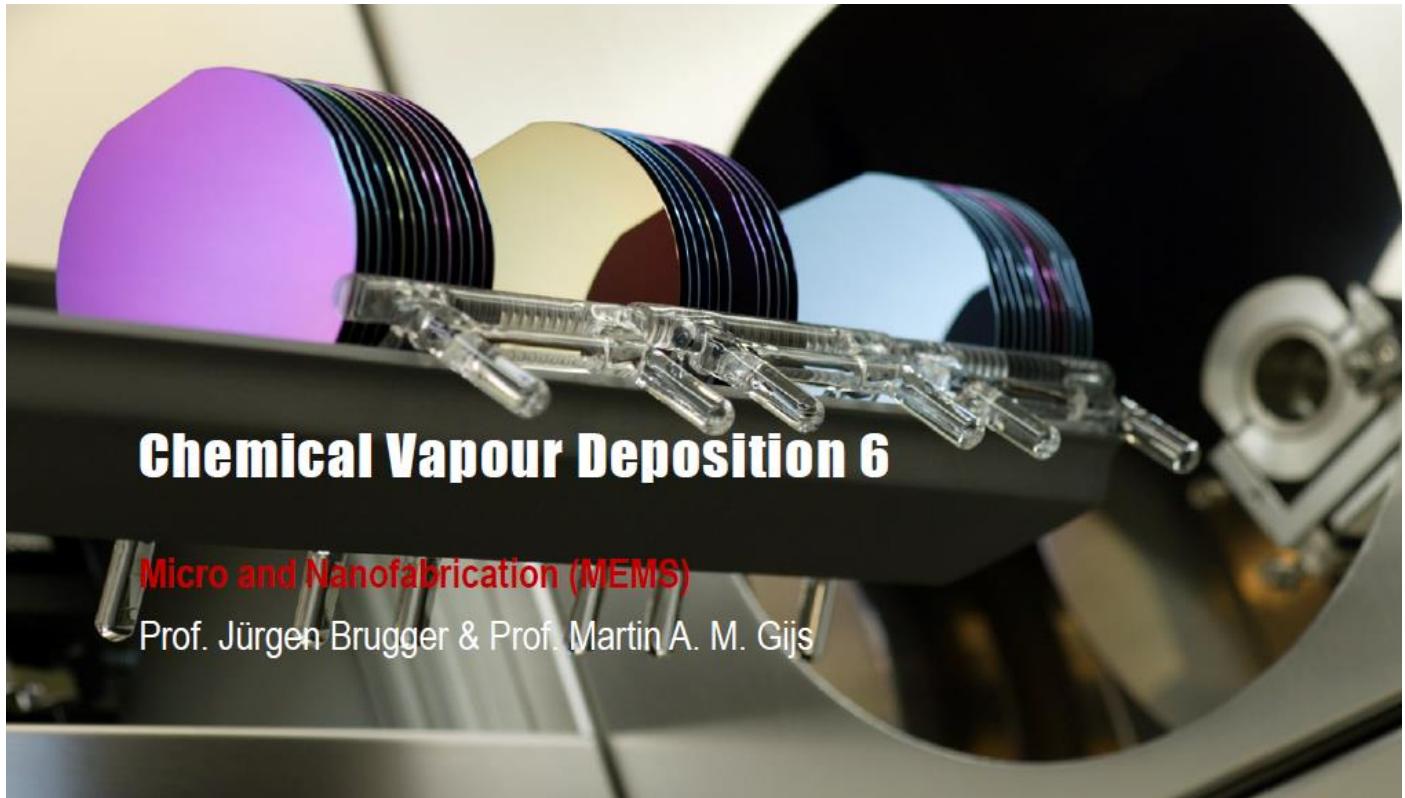
Questions:

1. Which are the assumptions made to obtain the simplified mass transfer equation?

- No advection close to substrate and no gas density variation in the vertical direction
- No advection far from substrate and no gas density variation in the vertical direction
- No advection close to substrate and no gas density variation in the horizontal direction
- No advection far from substrate and no gas density variation in the horizontal direction

2. Which statement is true for the simplified mass transfer equation?

- It is based on the assumption that there is no or little diffusion close to the surface
- When increasing the distance from the surface to $y = \infty$, the gas density approaches $\rho_{y=\infty}$ linearly
- It can still correctly describe non-equilibrium phenomena
- The annihilation term $-n'$ is only non-zero at the surface



Chemical Vapour Deposition 6

Micro and Nanofabrication (MEMS)

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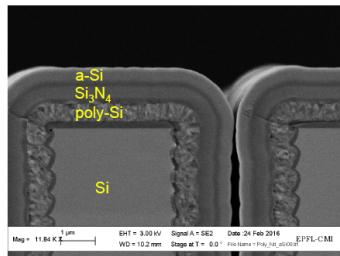
In this lesson we will give a few examples of CVD processes for depositing specific materials.

- LPCVD of polycrystalline and amorphous Si
- LPCVD of Si_3N_4 and $\text{Si}_x\text{N}_y\text{H}_z$
- LPCVD low-temperature oxide
- PECVD of diamond

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We will start by discussing the low-pressure chemical vapor deposition of polycrystalline and amorphous silicon. Then, we will discuss the LPCVD of silicon nitride and hydrogenated silicon nitride. The latter material has interest because of its lower intrinsic mechanical stress with respect to the pure silicon nitride. Next, we will discuss the LPCVD of so-called low-temperature oxide, or LTO. Finally, we will discuss the plasma-enhanced chemical vapor deposition of diamond films. Polycrystalline silicon, or polysilicon, is a very important material that is used in microelectronics for fabrication of the gate of transistors, the so-called MOSFETs, or metal-oxide semiconductor field-effect transistors.

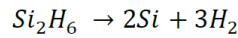
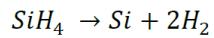
- Poly-Si is used in microelectronics as material for the gate of the transistors (MOSFETs)
- It can be used as electrical interconnection material when strongly doped with impurities
- It can be used as electrical resistor material when weakly doped with impurities
- It can be used as structural material in mechanical microsystems
- Amorphous Si (a-Si) is used in solar cells



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When the polysilicon is doped with impurities, it is a conducting material that can be used for realization of electrical interconnects. For microsystems applications it is used as a structural material, for example, for realization of mechanical inertial sensors. In the picture we see an etched silicon microstructure that was later covered by a polysilicon layer using LPCVD. We can recognize the crystalloid structure of the individual grains. Crystalloid formation is induced by underlying single-crystalline silicon. After the deposition of a silicon nitride layer, also by LPCVD, one has deposited, again, silicon by LPCVD-- there's this layer. This is now amorphous as the nitride does not provide nucleation sites for crystalloid generation. Amorphous silicon is used in solar cell applications. Here we show chemical reactions involved in the deposition of polysilicon.

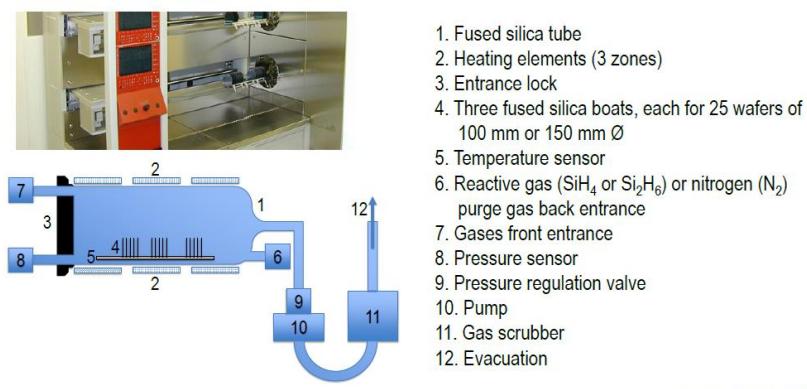


- Poly-Si is deposited from silane (SiH_4) or disilane (Si_2H_6) in a pressure range of 150-350 mbar and in a temperature window of 590-650 °C
- Amorphous Si is deposited in a temperature window of 525-585 °C
- Either Si or fused silica (SiO_2) substrates can be coated
- No float glass or Pyrex wafers are allowed, neither presence of metal or organic films
- Up to a few μm poly-Si can be deposited per run

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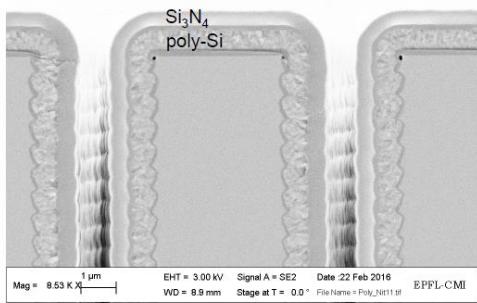
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One uses either silane gas or disilane gas in the pressure range of 150 to 350 millibar and in the temperature window around 590 to 650 degrees Celsius. Amorphous silicon is deposited at lower temperatures at which the mobility of deposited atoms on a substrate is lower. In the LPCVD reactor, one deposits the polysilicon on either silicon or fused silica substrates. Pyrex or float glass wafers are not allowed due to their low melting temperature. And also, the presence of metals or organic materials in the reactor is not tolerated. During a typical deposition run, a few micrometers of polysilicon can be deposited.



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This slide shows an LPCVD reactor, as we have seen before. Also, a schematic diagram is presented showing a fused silica boat filled with wafers. A boat can contain up to 25 wafers so that high throughput deposition is possible. The reactor is configured with a pressure sensor, with a pressure regulation valve, and with a pumping unit, so that one can well-control the pressure. A gas scrubber avoids that toxic byproducts of the chemical reaction are released into the environment. Another important material that is widely used in microfabrication is silicon nitride. It is used in microelectronic processes as passivation layer as it is a very inert and chemically-resistant material. It has also interesting mechanical properties and it can be used for realization of thin membranes, for example, or as an electrical insulating coating material. It is a material that is used in etching processes to resist to aggressive chemicals, for example, processes that use HF or KOH to locally protect the material underneath. In this picture we see again our etched silicon structure



- Si_3N_4 is used in microelectronic processes as passivation layer, mechanical protection or electrical insulation coating material
- It is used as chemically protective masking layer in HF or KOH etching
- Thin membranes can be made for microsystems applications

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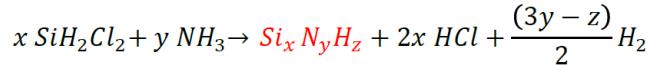
which has been covered with a polysilicon layer by LPCVD, followed by deposition of a silicon nitride layer by LPCVD. We see here the chemical reaction by which silicon nitride is deposited in an LPCVD process.

One uses two gases-- dichlorosilane and ammonia-- to deposit the silicon nitride layer, and the release of hydrogen chloride and hydrogen. Somewhat less than one micrometer is typically deposited per run.

This stoichiometric silicon nitride-- which is deposited at temperatures in between 700 to 840 degrees Celsius upon cooling down on a silicon wafer-- is characterized by a relatively large residual stress.



- Stoichiometric Si_3N_4 is deposited by thermal decomposition of dichlorosilane (SiH_2Cl_2) and reaction with ammonia (NH_3) in a pressure range of 150-250 mbar and in a temperature window of 700-840 °C
- Up to 0.8 μm Si_3N_4 can be deposited per run (residual stress ~1300 MPa)



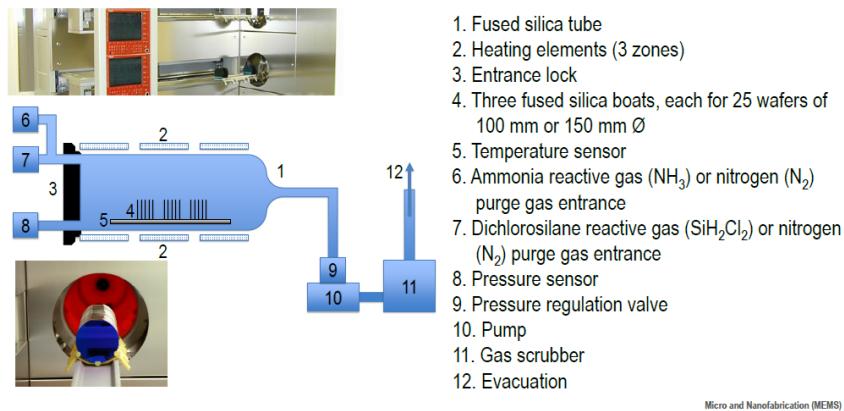
- Low-stress $\text{Si}_x\text{N}_y\text{H}_z$ can be deposited by tuning reaction gas concentrations
- Up to 2 μm of low-stress $\text{Si}_x\text{N}_y\text{H}_z$ can be deposited (residual stress ~200 MPa)
- Either Si or fused silica (SiO_2) substrates can be coated; no float glass or Pyrex wafers are allowed, neither presence of metal or organic films

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This may be unwanted for certain applications as it can lead to mechanical failure of devices. Therefore, it's also possible to deposit non-stoichiometric silicon nitride by adjusting the ratio of the two precursor gases,

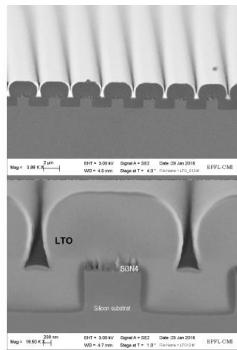
so one varies x and y . In this way we get hydrogenated silicon nitride which is characterized by a much smaller residual stress. Therefore, it is possible to deposit thicker layers. As a substrate that can be used in this type of process, we have to use either silicon or fused silica, like before. Here we show the reactor and schematic diagram that is used in an LPCVD process for silicon nitride. It is very similar to the reactor that is used for the deposition of polycrystalline and amorphous silicon, except that there are now two entrances for two simultaneously-used precursor gases. Another widely-used material in microfabrication is silicon dioxide or silica. We have already seen that silicon dioxide can be realized by thermal oxidation of the surface of a silicon wafer at high temperatures of about a thousand degrees Celsius. LPCVD enables to deposit silicon dioxide at much lower temperature that is at 400 to 450 degrees Celsius. That is why this oxide is known as Low-Temperature Oxide, or LTO.



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It is used as isolation layer in between metal layers or in between conducting polysilicon layers in microelectronics. It can be used as a protective mask and as a final passivation layer on silicon chips, too. In microsystems applications, it can be used as a sacrificial layer, that is, a layer on which a functional material like polysilicon is deposited, after which the silicon dioxide is chemically etched away so that one gets a freestanding polysilicon mechanical microstructure. The picture shows an LTO layer which is deposited on a silicon wafer that was microstructured using a silicon nitride mask.

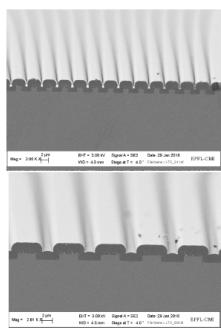


- Known as LTO (Low Temperature Oxide), it is used as isolation layer in between metal layers or poly-Si in microelectronics
- It is used as a mask against diffusion or implantation
- It is used as final passivation layer on Si chips
- It is used as sacrificial layer in microsystems

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It is also possible to dope the silicon dioxide with phosphorus atoms. Strongly phosphorous-doped LTO is known as phosphosilicate glass, or PSG. This material can be used as a diffusion source, that is, it is deposited on a silicon wafer after which, during heating, it releases its phosphorus by diffusion into the silicon. It can also be used as a smoothing layer-- as during heating, it shows creeping behavior-- or it can be used as a passivation layer. It is also possible to dope the LTO with both boron and phosphorus. And in this case, this material is known as Borophosphosilicate glass, or BPSG.



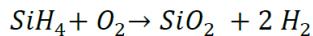
- Strongly phosphor-doped LTO (PSG: Phospho-Silicate Glass) or phosphor & boron-doped LTO (BPSG: Boro-Phospho-Silicate Glass) is used as diffusion source, smoothing layer due to its creeping behavior at high temperature, or passivation layer with barrier function against Na⁺ ions and H₂O
- PSG shows creep at 1000-1050 °C for P mass concentrations > 6%
- BPSG shows creep at 700 °C ; the B mass concentration should be < 5% for stability

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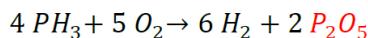
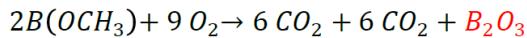
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It has similar properties as the PSG. This is the chemical reaction for the deposition of the silicon dioxide.

One uses silane and oxygen gas as precursor gases at pressures of about 90 to 250 millibar in a temperature window of 400 to 450 degrees Celsius. Up to a few microns of LTO can be deposited per run. For realization of the PSG or BPSG, additional precursor gases are needed, namely, trimethylborate and phosphene. This leads to incorporation of these oxides in the silica film. Here we see a schematic diagram of an LPCVD deposition system for silicon dioxide, which has also the option to realize Phosphosilicate glass and borophosphosilicate glass



- LTO is deposited by the reaction of silane (SiH_4) with oxygen (O_2) in a pressure range of 90-250 mbar and in a temperature window of 400-450 °C
- Up to 3 μm LTO can be deposited per run



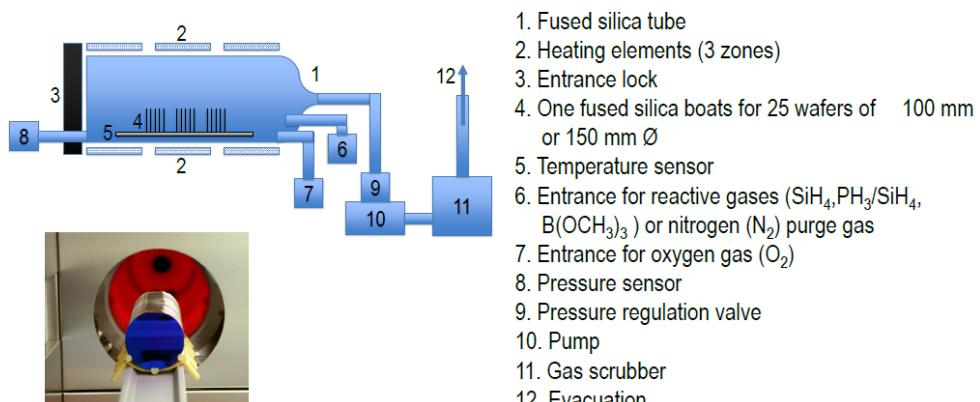
- Trimethylborate ($B(OCH_3)_3$) and phosphine (PH_3), in combination with silane (SiH_4), are used for deposition of PSG ($P_2O_5-SiO_2$) and BPSG ($B_2O_3-P_2O_5-SiO_2$)

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by switching on the supply of the appropriate precursor gases. The last application we want to show is the plasma-enhanced chemical vapor deposition process of diamonds. Diamond has a very high thermal connectivity and can be used as heat sink in high-powered diode and transistor applications, for example.

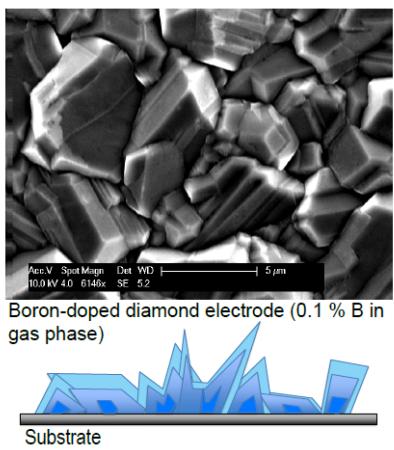
It is also chemically inert and can be used as electrode material in electrochemical applications.



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When doped with boron, the thus-obtained conducting material can be used in harsh chemical environments to probe the properties of the chemical liquid of interest without having substantial and unwanted chemical interaction with the electrode itself. The picture shows such boron-doped diamond electrode. In particular we see here, the crystalloid structure which is sketched here again, in cross-section,

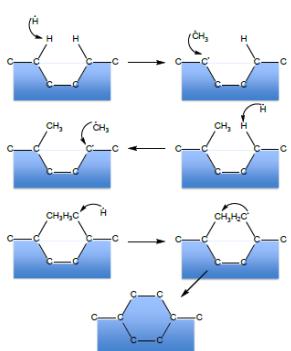


- Diamond has a high thermal conductivity, but negligible electrical conductivity; it can therefore be used as heat sink for high-power laser diodes and transistors
- Diamond is hard, chemically inert and has a low coefficient of thermal expansion
- Synthetic diamond can be used as a wide band gap (5.5 eV) semiconductor and can be doped with P or B
- B-doped diamond can be used as electrodes in electrochemical applications

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and which originates by the preferred growth of the diamond along certain crystal facets. This diagram illustrates the growth of the diamond layer, starting from the gaseous reactants, hydrogen and methane. The deposition temperature is in between 700 and 900 degrees Celsius.



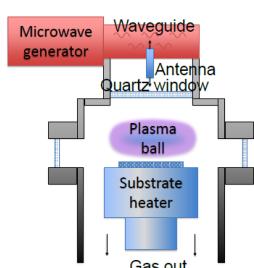
- Growth requires activation of the gaseous reactants, usually H₂ and methane (CH₄) at 50-200 mbar pressure
- The growing diamond lattice is prevented from rearrangement to graphitic carbon by termination with hydrogen atoms at 700 °C < T < 900 °C
- In the plasma, H₂ dissociates into H atoms, which react with the source hydrocarbon and create a complex mixture of hydrocarbon species, including reactive C-containing radicals
- The H atoms also remove hydrogen from the surface CH bonds, creating surface radical sites that will react with new hydrocarbon species to form a diamond lattice

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In the plasma, the hydrogen gas is dissociated in individual hydrogen atoms which react with hydrocarbons to create a complex mixture of hydrocarbon species. The individual hydrogen atoms can remove hydrogen from the surface by recombination into molecular hydrogen. Thereby, they create radical sites that can react now with hydrocarbon species to form the diamond lattice. This process is repeated continuously.

And finally, one gets here the diamond structure. Here we show a schematic illustration of a diamond plasma-enhanced chemical vapor deposition reactor. A microwave generator creates the energy for generation of the plasma in the reactor. A typical microwave plasma CVD growth rate for diamond is in between 0.1 and 10 micrometer per hour. In this lesson we have given several experimental examples of CVD processes.



- Microwave plasma can be generated above a substrate, minimising the effect of plasma heating on the sample, allowing almost independent control of plasma and substrate parameters
- Substrate temperature is typically in the 750 °C – 900 °C range
- Microwave plasma CVD growth rates are in the 0.1-10 μm h⁻¹ range

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We discussed the low-pressure chemical vapor deposition of some of the most important materials in microelectronics and microfabrication, like polycrystalline and amorphous silicon, silicon nitride, hydrogenated silicon nitride, and silicon dioxide. Finally, we have discussed a plasma-enhanced chemical vapor deposition process for deposition of diamond films.

Summary

- Several illustrative examples of CVD processes given
- LPCVD of Si, Si_3N_4 , $\text{Si}_x\text{N}_y\text{H}_z$, and SiO_2
- PECVD of diamond

Practice quiz specific CVD processes for silicon-based materials and diamond

Questions:

1. Which parameter has to be varied when a deposition of polycrystalline silicon instead of amorphous silicon is targeted?

- Substrate material
- Reactor temperature
- Precursor gases
- Chamber pressure

2. Why is diamond deposited with PECVD?

- Plasma is necessary for the generation of reactive species
- The cost of diamond deposition is too high when using other CVD methods
- It can only be deposited on pyrex substrates, therefore PECVD is the only option
- In PECVD, high pressure and high temperature are needed, which supports the diamond carbon allotrope over graphite



Chemical Vapour Deposition 7

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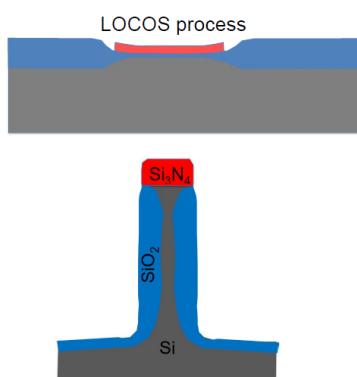
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In this lesson we will discuss three additional types of specific CVD and Atomic Layer Deposition processes.

- Wet thermal SiO_2 (not truly CVD)
- Dry thermal SiO_2 (not truly CVD)
- Atomic Layer Deposition (ALD) of Al_2O_3 , Ru, and TiN

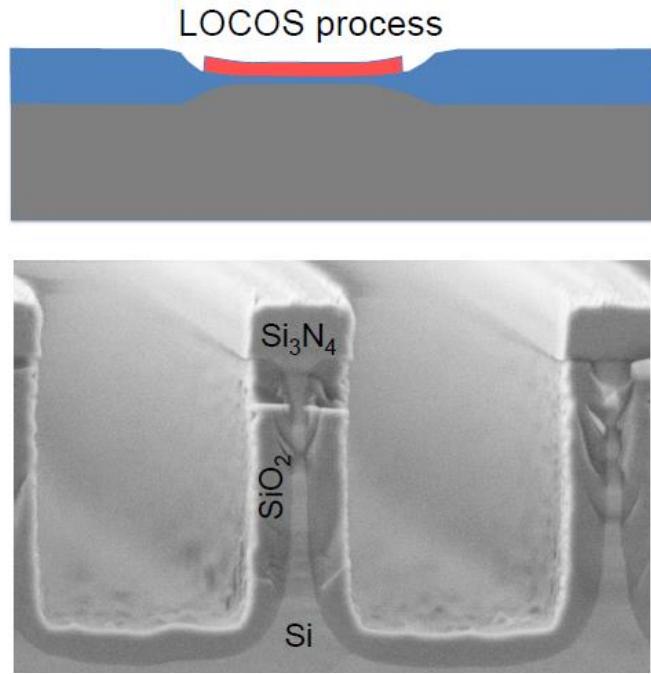
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We have already seen that wet and dry thermal oxidation, strictly speaking, are no true CVD techniques as they transform the silicone surface into an oxide by diffusion of oxygen atoms into the silicon lattice rather than depositing a layer on the substrate from the gas phase. However, the technique is using the same technological infrastructure as a true CVD process. As examples of atomic layer deposition we will discuss the deposition of aluminum oxide, ruthenium, and titanium nitrite films. Wet oxidation uses water vapor resulting in a relatively fast transformation of the surface of a silicon wafer into oxide. We have already seen that if one has a local thin silicon nitrite layer as protection it is possible to create locally thick silica layers while protecting the region in the middle against oxidation. And this process was named Local Oxidation of Silicon , or LOCOS .



- Wet oxidation (using H_2O vapour) allows fast transformation of the surface of a Si wafer, layers of poly-Si or amorphous Si into oxide
- Thick layers (up to 2 μm) can be realized
- Such oxide layers can be used e.g. as protective masking layer in plasma etching, or used as thick electrical insulation layers in microelectronic

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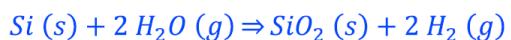


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Here we illustrate the wet thermal oxidation process using another type of silicon microstructure. One has prepared here a pillar structure by etching, using silicon nitrite as a masking material in the etching process. If one now performs the thermal oxidation step, the silicon nitrite again acts as a barrier against the diffusion of oxygen atoms. This gives relatively few oxidation underneath the silicon nitrite and thicker regions here where there is full access for the oxygen. This picture shows the experimental example.

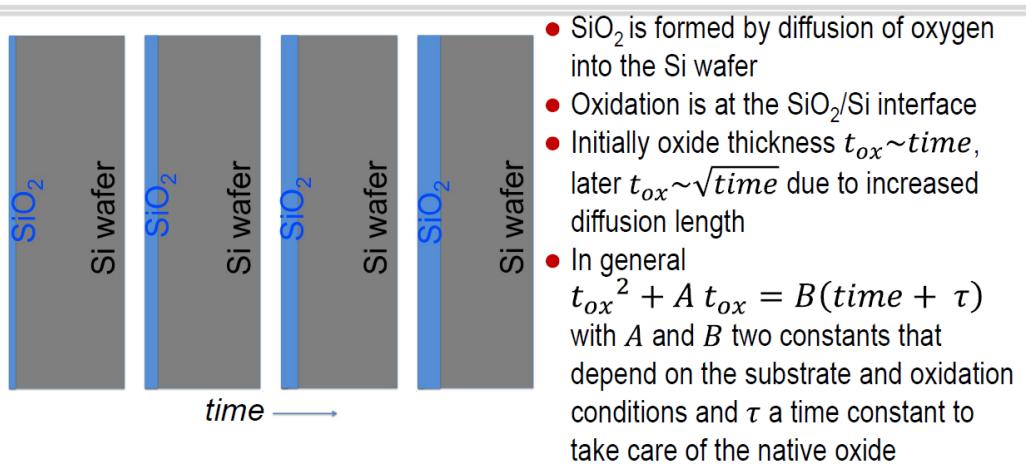


- In thermal oxidation, silicon is transformed into its oxide at high temperature ($850^{\circ}\text{C} < T < 1100^{\circ}\text{C}$) using either water vapor ("wet oxidation") or oxygen ("dry oxidation").
- Water vapor is produced by combustion of H_2 and O_2 in a torch
- Slow process
 - Wet @ 900°C : 130 nm in 1 hour
 - Dry @ 900°C : 30 nm in 1 hour



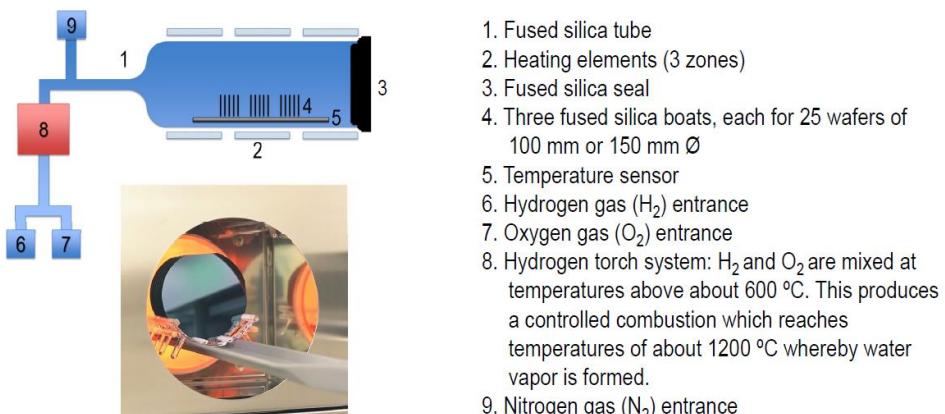
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And we clearly recognize here the three types of materials. So first we had here the silicon structure made using the silicon nitrite mask, and here we see the zones where the silicon is transformed to silicon dioxide. In thermal oxidation one uses temperatures in between 850 degrees Celsius and 1100 degrees Celsius. We have already seen that one can use either water vapor in the reaction, and then the process is called "wet oxidation", or one can use oxygen gas, and then the process is called "dry oxidation". Both processes are relatively slow. Wet oxidation is a few factors more rapid than dry oxidation, however. This slide shows the transformation of the silicon into silicon dioxide as a function of time. Initially, the oxygen easily diffuses to the silicon surface so that the oxide thickness is proportional to the time. However, when the oxide becomes thicker it becomes increasingly difficult for the oxygen atom to reach the silicon surface, and the oxidation will become slower. That is why the oxide thickness is proportional to the square root of the oxidation time. In general, we can have the following formula which fits both the initial linear behavior and the square root behavior for longer oxidation times. Here τ is a time constant that takes into account the thickness of an eventual initial native oxide of the silicon wafer. This is a schematic diagram of a wet thermal oxidation equipment.



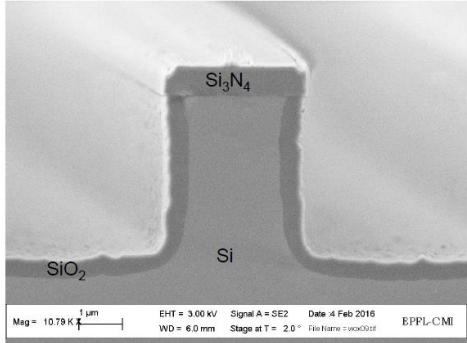
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The generation of the water in the wet thermal oxidation process is particular. Hydrogen and oxygen gas are mixed at a temperature of about 600 degrees Celsius and react in a controlled combustion process, reaching temperatures of about 1200 degrees Celsius. And as a result of this combustion water is generated which is then led into the reactor. Dry thermal oxidation is mainly used for the realization of thin oxide layers that form the gate oxide in MOS transistors. In this process, one uses dichloroethylene and oxygen to create together hydrogen chloride that cleans the surface from eventual metal contaminants. In this way, a very thin and pure oxide layer of high quality can be grown. The picture shows a similar type of structure like shown before-- a silicon pillar, made with a silicon nitrite mask and afterwards there is dry oxidation leading to these oxide layers. This is a schematic diagram of the dry thermal oxidation equipment.

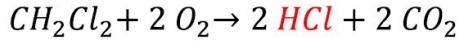


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It has the particularity that nitrogen gas is bubbled through the dichloroethylene bonds to transport the dichloroethylene molecules to the reactor. We will now discuss the deposition of thin aluminium oxide layers by atomic layer deposition. This material is used for its high dielectric constant in certain microelectronic components, like capacitors. It can also be used as a gas diffusion barrier in packaging and in flexible electronic devices. The deposition temperature during an ALD process is typically a few hundred degrees Celsius. ALD is very well suited for deposition of very thin layers without pinholes and/or for forming conformal layers onto microstructured substrates. In the picture we see a silicon etched structure which has been coated with an aluminium oxide layer by ALD. Four steps are involved in the deposition of aluminium oxide by ALD. The first precursor is tri-methyl aluminium; this molecule, which is chemisorbed onto a silicon substrate that has hydroxyl surface groups.

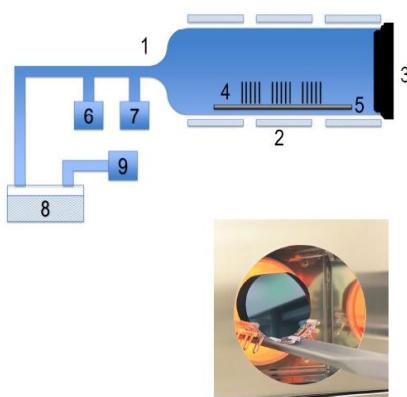


- Dry thermal oxidation is used for realisation of the thin gate oxide layer in MOS transistors
- A dichloroethylene ($C_2H_2Cl_2$) bubbler allows controlled growth of ultrathin oxides (20-25 nm)
- $C_2H_2Cl_2$ is a liquid source that generates high-purity HCl, which reacts with metal contaminants so that a high-quality low-defect thin oxide can be grown



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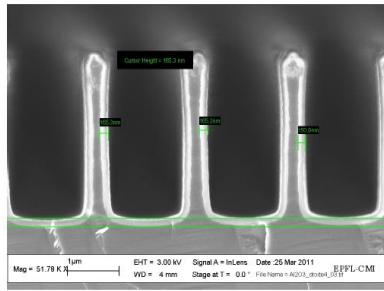
Methane is a reaction product that is generated in this step and is pumped away. Here we see the chemical reaction that was depicted in these two schematic illustrations.



1. Fused silica tube
2. Heating elements (3 zones)
3. Fused silica seal
4. Three fused silica boats, each for 25 wafers of 100 mm or 150 mm Ø
5. Temperature sensor
6. Oxygen gas (O_2) entrance
7. Nitrogen gas (N_2) entrance
8. Dichloroethylene (DCE) ($C_2H_2Cl_2$) bubbler
9. Nitrogen gas (N_2) - dichloroethylene ($C_2H_2Cl_2$) entrance

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The reaction chamber is then purged with inert nitrogen gas, thereby removing all methane reaction products and any excess of the precursor TMA. Next the second precursor water vapor enters the system. The water precursor reacts with the TMA at the surface forming methane byproducts. The reaction chamber is then, after this reaction, again purged and nitrogen and any excess of the water vapor and the byproducts of the reaction are removed.



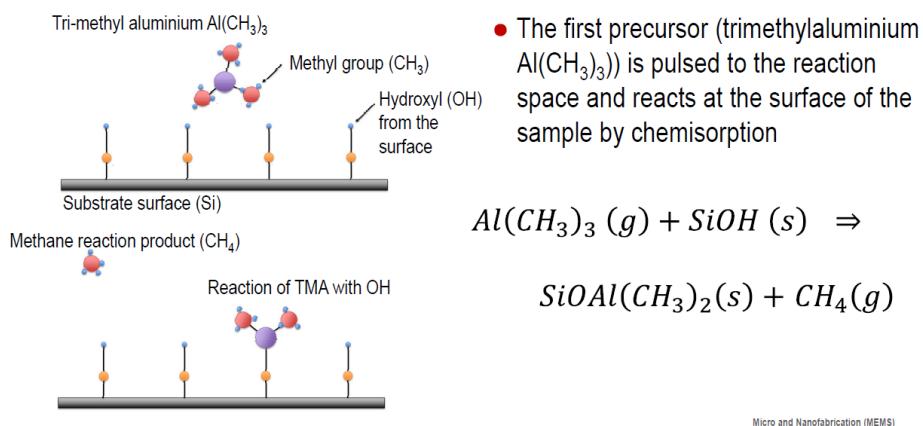
- Thin Al_2O_3 layers can be used as high dielectric constant ($\epsilon_r=7.5$) material in microelectronic components, as gas diffusion barrier layer in packaging, and in flexible electronic devices
- Substrate temperature during ALD deposition can be 100-500 °C
- Deposition is done under vacuum (around 5 mbar) from chemical precursors
- ALD is recommended for thin layers (<100 nm) and/or for conformal layers

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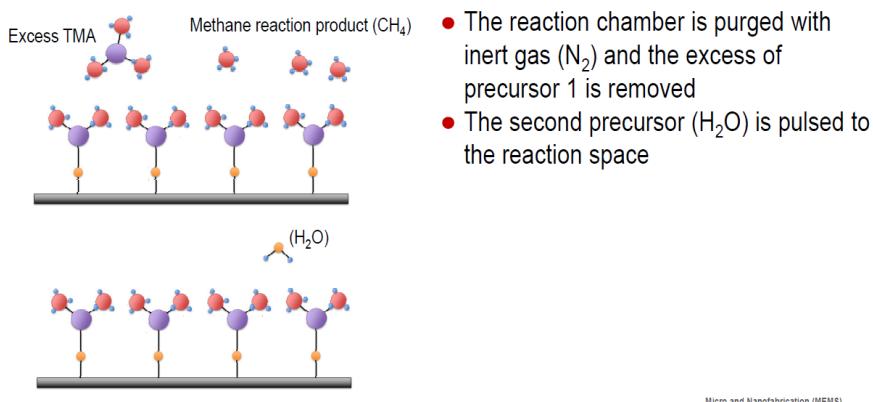
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One is then left with a surface of aluminium oxide with hydroxyl groups. In fact, one has created one monolayer of aluminium oxide with hydroxyl terminations so that the next monolayer deposition process can be executed. And this process can be repeated over and over again many thousand times. ALD exists for deposition of many types of materials. Here we show two other examples, namely the deposition of titanium

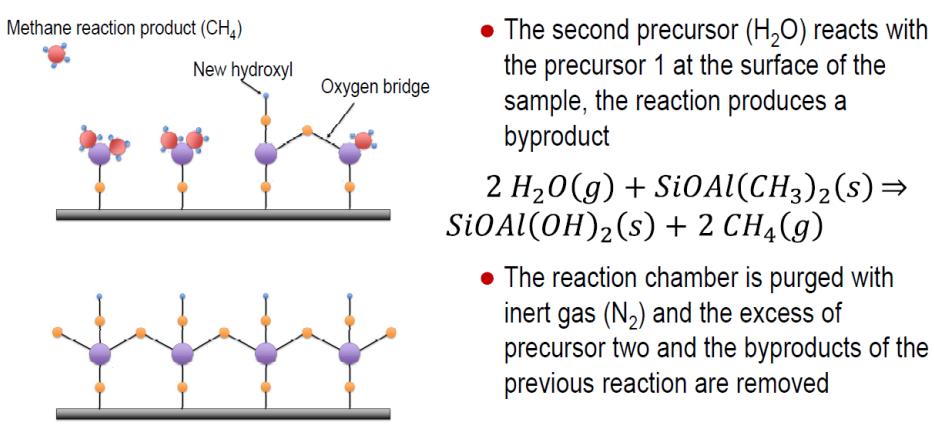
nitrite and the metal ruthenium. The table lists the used precursor gases for each case and the temperature for each step. The two pictures below demonstrate the end result after deposition during 2000 ALD cycles. So here we see the ruthenium which is covering the silicon pillar structure which was made, in this case, using an oxide etching mask. And here we see a picture of a cross-section of the titanium nitrite on silicon dioxide, also after 2000 cycles of ALD. Here we show an example of atomic layer deposition equipment. It is basically a chemical reactor-- if we look inside we see the reaction vessel.



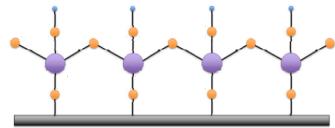
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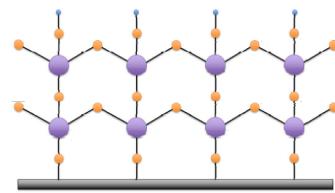
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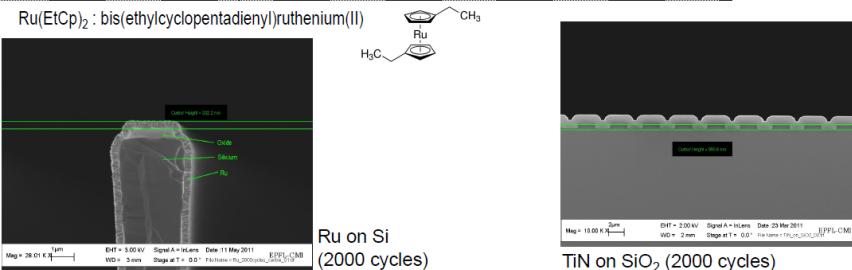
- Formation of a monolayer of Al_2O_3 with OH^- terminations



- The monolayer deposition process can be repeated over and over again

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	Precursor 1	Temp. (°C)	Precursor 2	Temp. (°C)
TiN	TiCl_4	Room temperature	NH_3	Room temperature
Ru	$\text{Ru}(\text{EtCp})_2$	110	O_2	Room temperature



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- The equipment is composed of a chamber with a reactor inside
- A loadlock system
- 4 liquid sources slots
- 2 hot sources slots
- 7 gas lines (for processes with O_2 , N_2 and NH_3 and purge with N_2)
- An ozone generator
- A primary pump

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and one can then lead into this reactor the different gases. For this type of reactor there are seven gas lines and there is an ozone generator, and of course there is also a pump involved to evacuate the reactor when needed. In this lesson we have given a few illustrative examples of CVD-like processes. We have started with oxide formation on silicon wafers-- by wet and dry thermal oxidation-- at temperatures of about 1000 to 1100 degrees Celsius. Subsequently we have discussed the atomic layer deposition of aluminium oxide, ruthenium metal and titanium nitrite.

Summary

- Several illustrative examples of CVD processes
- Oxide formation by wet and dry thermal oxidation (transformation) of Si
- ALD of Al₂O₃, Ru, and TiN

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Practice quiz thermal oxidation processes of silicon and ALD deposition of specific oxides and metals

Questions:

1. Why is the oxide thickness t_{ox} in a thermal oxidation process proportional to the square root of time?

- Diffusion of oxygen to the silicon surface takes longer when the SiO_2 gets thicker
- The temperature at the substrate surface gets lower when the SiO_2 gets thicker, which decreases the reaction rate
- Diffusion of silicon to the SiO_2 surface takes longer when the SiO_2 gets thicker
- Less oxygen is available at the substrate surface due to metal contaminants

2. In ALD of Al_2O_3 , how is it possible to achieve single atomic layer precision of the deposition?

- Slow reaction rates allow precise control of layer number
- Reaction byproducts limit the growth of new layers, which is why the reaction chamber must be purged
- By restricting the precursor gases to $\text{Al}(\text{CH}_3)_3$ only
- By using 2 precursors in a sequential, self-limiting manner

Conclusion and summary

In this module on chemical vapor deposition or CVD, we have introduced different variants of CVD and the typical cleanroom infrastructure that is needed to run a CVD process. Also we introduced atomic layer deposition or ALD, as well as the thermal oxidation process of silicon. Important theoretical concepts that play a role in CVD, like the velocity and concentration boundary layer near a substrate were discussed. Specific CVD deposition processes were introduced for depositing poly-crystalline and amorphous silicon, silicon oxide, silicon nitride, diamond and metal films. Here are a few important key points you should remember.

Different types of CVD processes

- The material to deposit is originating from a gas flow that is chemically reacting on a heated substrate to form a thin film.
- Conformal deposition on a substrate, even inside holes, is possible, as the gas accesses the complete volume of the reactor.
- Three aspects that play a role in CVD: thermodynamics, reaction kinetics and gas flow.
- In the reaction-limited regime at relatively lower temperature, the film growth rate is limited by occurrence of the reaction.
- In the mass transport-limited regime of CVD at relatively higher temperature, the film growth rate is limited by the supply of gas.
- CVD processes can be classified according to pressure of the gas used.
- Different reactor types are used in CVD depending if one is in the reaction-limited or mass transport-limited regime.
- In plasma-enhanced CVD (PECVD), application of a plasma permits lowering the deposition temperature as the effective activation energy for the chemical reaction is lower.
- Metal-organic CVD (MOCVD) is a technique to deposit a thin film from a liquid precursor by bubbling a gas flow through the liquid and transport this to the reactor.
- Atomic layer CVD or ALD is a technique in which a thin film is deposited atomic layer-by-atomic layer. This technique enables deposition of extremely thin but continuous films without pinholes.
- Thermal oxidation of silicon occurs by leading oxygen gas into the reactor, which, at high temperature, oxidizes the surface of a silicon wafer. It is not truly a CVD process, in the sense that the silicon top layer is transformed to silicon oxide, rather than there is a deposition of the oxide material from the gas on top of the substrate.

Theoretical concepts in CVD

- Due to viscous friction forces, the velocity near the substrate is strongly modified compared to the velocity in a free flowing gas. At the substrate, the velocity is essentially zero and going away from the substrate, one will reach the velocity of the gas in the free flow regime, i.e. a velocity boundary layer is formed.
- One consumes gas molecules in the process, the concentration at the substrate will therefore be reduced so that there is not only a velocity boundary layer near the substrate but also a concentration boundary layer.
- The Reynolds number plays a role in the gas molecule transport and physically corresponds to the ratio of the inertial to the viscous forces.

- If the mass transfer coefficient by diffusion is much higher than the surface reaction rate, we obtain the film growth rate in the reaction-controlled case.
- If the mass transfer coefficient by diffusion is much lower than the surface reaction rate, we obtain the film growth rate in the mass transport- or diffusion-controlled case.

CVD processes for specific materials

- For LPCVD of poly-silicon, one uses either silane gas or disilane gas in the pressure range of a few 100 mbar and in a temperature window around 600 °C. Amorphous silicon is deposited at lower temperatures, at which the mobility of deposited atoms on the substrate is lower.
- For LPCVD of silicon nitride, one uses two gases, dichlorosilane and ammonia, to deposit the silicon nitride under release of hydrogen chloride and hydrogen gas. This stoichiometric silicon nitride, upon cooling down on a silicon wafer, is characterised by a relatively large residual stress, which may be unwanted for certain applications, as it can lead to mechanical failure of devices.
- Therefore, it is also possible to deposit non-stoichiometric silicon nitride, by adjusting the ratio of the two precursor gases. In this way, we get hydrogenated silicon nitride, which is characterised by a much smaller residual stress.
- LPCVD enables to deposit silicon dioxide at a relatively low temperature of around 400 °C using silane and oxygen gas. This oxide is therefore known as low temperature oxide or LTO.
- Diamond films can be deposited in a plasma reactor from the gaseous reactants hydrogen and methane. The deposition temperature is in between 700° and 900°C.
- In thermal oxidation, one uses temperatures in between 850°C and 1100°C. One can use either water vapour in the reaction and this process is then called wet oxidation, or one can use oxygen gas and this process is called dry oxidation. Both processes are relatively slow, wet oxidation is a few times faster than dry oxidation, however.

Physical Vapor Deposition (PVD)

Micro and Nanofabrication (MEMS)

Prof. Jürgen Brugger & Prof. Martin A. M. Gijs

Introduction and objectives

Physical vapor deposition (PVD)

This module on physical vapor deposition describes in details the two main PVD methods; thermal evaporation and sputtering. Physical principles, setups configurations, process parameters, deposited films properties, advantages and limitations, as well as examples are introduced and discussed for these two techniques. In addition, an overview of some alternative techniques such as ion assisted deposition, molecular beam epitaxy and pulsed laser deposition is also presented as supplementary material.

At the end of this week, you should be able to:

- Name the different physical vapor deposition methods and list their main advantages and limitations.
- Describe how atoms from a source of material are transformed into a thin film on a substrate for the different PVD techniques. Relate how each methods affect the thin film parameters and growth.
- Discuss which process parameters affect the deposition by evaporation and by sputtering. Qualitatively explain how these parameters affect the deposition.
- Compare properties of thin films deposited with different PVD methods. Determine which PVD method should be used for a specific application.

Intro quiz

Questions:

1. Which of the following techniques are part of the family of physical vapor deposition (PVD) techniques?

- Evaporation
- Wet oxidation
- Atomic layer deposition
- Sputtering
- Molecular beam epitaxy
- Vapor phase epitaxy
- Pulsed laser deposition

2. What do you know of the advantages of physical vapor deposition over chemical vapor deposition?

- PVD requires lower processing temperatures than CVD
- Deposited PVD films are generally more conformal than CVD films
- PVD requires lower level of vacuum than CVD
- PVD enables the deposition of more diverse materials than CVD
- Deposition rates of PVD are higher than CVD

PVD 1: Thermal evaporation

Introduction and vapor creation

Micro and Nanofabrication (MEMS)

Prof. Jürgen Brugger & Prof. Martin A. M. Gijs

In this lecture, I will show you how we can form a high quality thin film on a substrate. You may remember the case study of the bimorph thermal actuator beam where we deposited a 500 Nanometer thick layer of chromium on a SiO₂ coated silicon wafer.

- Thermal (or vacuum) evaporation
 - Physical principles
 - Equipment
 - Examples

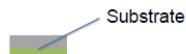
- Sputtering

- Other methods

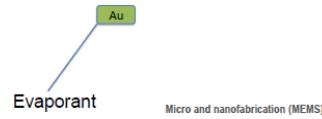
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Such thin films in metals are deposited by so-called physical vapor deposition or PVD. In this lecture, you will learn the basics of vacuum evaporation. I will start by showing the physical principle, then show how the equipment looks like, and finally present some examples. Don't confuse thermal evaporation with sputtering, which is another PVD method and that will be shown in the subsequent lessons part two. So in this first part, let's have a look at thermal evaporation, also called vacuum evaporation. I will introduce the topic and show how the vapor is created. So how do we get from the source of metal to a well controlled thin film on the wafer like shown here in grey.



1. Vapor creation
2. Vapor flux towards substrate
3. Condensation on the substrate



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This is done by so called evaporation. Let's take gold as an example. Evaporation occurs when the atoms of the evaporant achieve sufficient energy to overcome the solid and liquid binding forces and enter the gas phase. By drawing here. This is physically achieved by heating the material, but just heating is not enough for our purpose even at very high as you will see. In this process, we have to consider three distinct phases as follows. First of all, how is the vapor created? Second, how the vapor flux is directed towards the substrate? And third, how the material condenses on the substrate to form a thin film. So let's look at these steps one by one in detail now. As said, we will set gold as an example material but everything applies to other materials as well, just with different parameters and specificities. The transformation of a material from condensed phase, either solid or liquid into vapor is described by the Hertz-Knudsen equation.

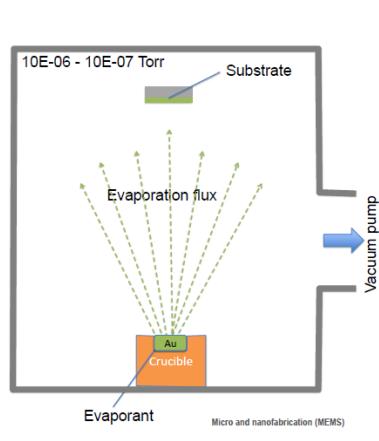
- Hertz-Knudsen equation

$$\Phi_e = \frac{1}{A_e} \cdot \frac{dN}{dt} = \frac{\alpha \cdot N_A \cdot (P_v - P)}{\sqrt{2\pi \cdot M \cdot R \cdot T}}$$

$$\Gamma_e = \Phi_e \cdot \frac{M}{N_A}$$

Φ_e = vapor flux in [molecules/(m²·s)]
 A_e = source surface area in [m²]
 N = number of gas molecules
 α = sticking coefficient (0< α <1 = ideal case)
 N_A = Avogadro constant in [mol⁻¹]

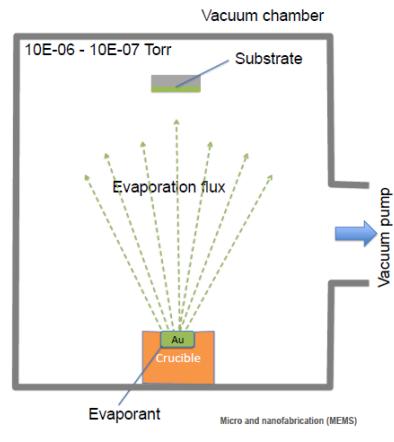
P_v = vapor pressure of the evaporant in [Pa]
 P = reactor pressure in [Pa]
 M = molar mass in [kg/mol]
 R = gas constant in [J/(mol · K)]
 T = temperature in [K]
 Γ_e = evaporation mass flux in [kg/(m²·s)]



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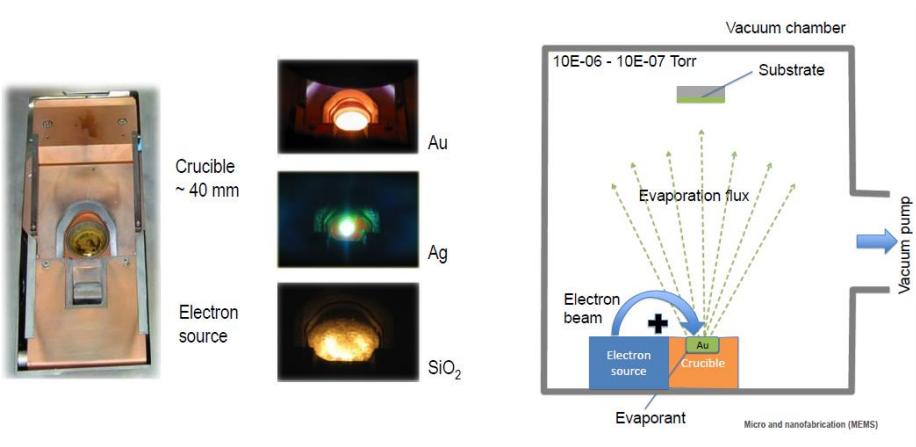
In fact, it was found experimentally that the vapor flux Φ is proportional to the difference between P_v and P . Where P_v is the equilibrium vapor pressure of the evaporant at temperature T , and P is the reactor pressure. It further depends on a series of parameters that are all listed here below. Another convenient way to quantify the deposition parameters is to use the evaporation mass flux in γ , which is the vapor flux multiplied by the molar mass divided by the Avogadro number.

- How to heat up the evaporant?
- By resistive heater
 - + simple / - contamination
- By electron beam
 - - more complex / + control



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It was found that the evaporation rate does not increase further by supplying more heat unless the equilibrium vapor pressure is also increased by this action. Thus, there is a maximum evaporation rate set by P_v and can only be achieved in a vacuum where P approaches 0. For highest vapor flux, one therefore operates the evaporation in a vacuum chamber and by heating up the material in the Crucible. Another advantage to operate in a vacuum is to avoid any contamination of the evaporant with residual gases. Please note that according to the formula, heating up should actually decrease the flux because T is in the denominator but this is compensated by the fact that P_v also increases with T . There are various ways to heat up the material to evaporate. One simple way is to wrap some evaporant material around a tungsten wire like shown here but which has a limited source lifetime. Therefore, one typically places the evaporant material in a so-called crucible or boat, which is made of a robust material that resists to very high temperature, meaning that it is not evaporating itself. Heating can be achieved by passing a current either around the bolt or by directly passing a current through the crucible that warms up and evaporates then the metal.



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This technique is simple, but has the drawback that there's a possible risk of alloy formation and contamination as we heat the entire container. Therefore another way has been developed which is based on the use of an electron beam to create the current that heats up the evaporant. So assuming here is an electron emitter, with a corresponding anode that accelerates the electrons, now the electrons are...have a trajectory that can be controlled by a magnetic field so that they hit the metallic target and close the current loop. So this induces the heat that melts the metal in the crucible. By changing magnetic field, one can scan the electron beam to uniformize the heat generation on this molten metal. On this photograph you see nicely, and the electron beam coming from the left and heating the molten metal here, in this crucible. The size of this crucible is in the order of four centimeters. The library of materials that can be evaporated is quite extensive and includes not only refractory metals but also dielectric and organic material. See the

accompanying documents for an overview of operation material and their corresponding specific parameters. On the left, you can see a crucible with the electron source. As we use it in our cleaning room evaporator, the typical size of the crucible here, shown here is about 40 millimeter and may depend on the equipment parameters. In the center you can see three optical images showing different materials being heated with the electron beam. This images has been taken from outside the vacuum chambers through a glass window. It is worthwhile mentioning that each material has a very different structure in the crucible. For instance, SiO₂ is in forms of beads shown here whereas gold and silver are completely molten under the e-beam current.



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This photo shows for instance how gold looks like as evaporant material when it is placed in the crucible before it is heated and molten. Atoms leaving the evaporant source into the vacuum follow straight line paths until they collide with other gas molecules or strike the substrate or the wall of chamber, condense there, and form a solid thin film. In Kinetic theory, one can define a distance that an object travels between collisions with other moving objects.

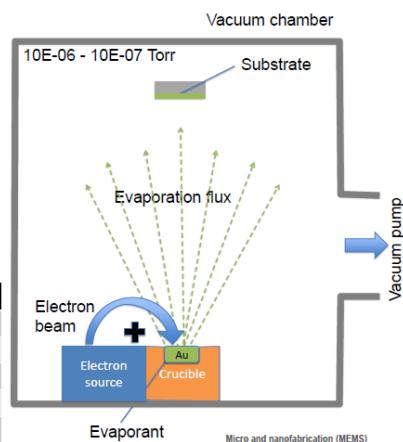
- Mean free path λ (in kinetic theory)

$$\lambda = \sqrt{\frac{\pi \cdot R \cdot T}{2M}} \cdot \frac{\eta}{P}$$

- Atoms follow straight lines until collision

λ = mean free path in [m]
R = gas constant in [J/(mol K)]
T = temperature in [K]
M = molar mass in [kg/mol]
 η = gas viscosity in [Pa]
P = reactor pressure in [Pa]

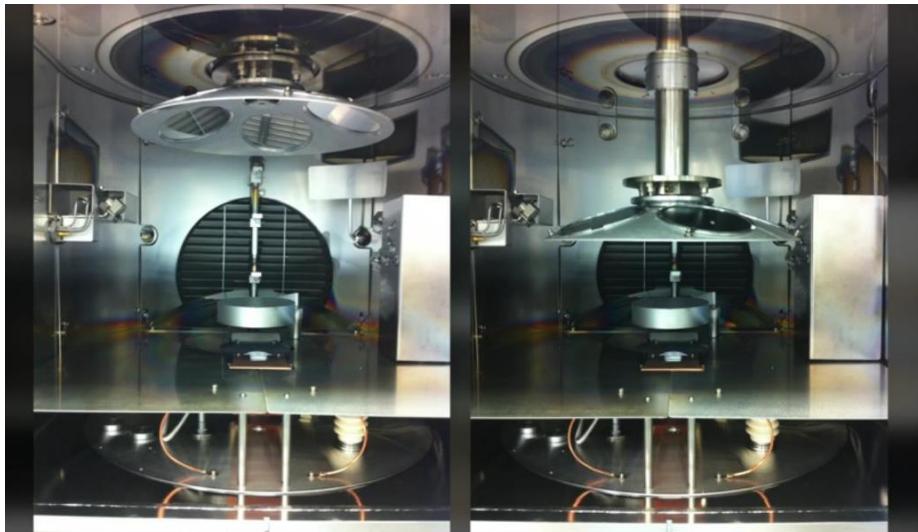
	Torr	MFP
atm	760	65 nm
LV	~1	50 μm
MV	~10 ⁻³	5 cm
HV	~10 ⁻⁷	500 m
UHV	~10 ⁻⁹	50 km



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This leads a mean free path, expression of lambda that is shown here, which primarily depends on the gas viscosity the molar mass, and last but not least, on the reactor pressure. So if we have less collisions, that means the deposit is more directional. This is one of the primarily characteristic of the vacuum evaporation and has some consequences for particular cases as you will see. One of them is that there's a certain risk of shadow formation. This table give an overview of various mean free path value as a function of chamber pressure. At atmospheric pressure, we have very short mean free path, and so the molecules are bouncing into each other and the average, every 65 Nanometer of travel if you go to low vacuum, or medium vacuum and high vacuum for example, we can already gain mean free path of several meters. So our chamber that we built is typically a half meter, one meter, in size. So an atom or molecule leaving the evaporant's source,

will not have any collision before it hits the substrate surface. That means this is a very directional flux from the source to the substrate. In contrast as you will see later, sputtering is performed at higher pressure and involves more collisions of target molecules and ions before deposition. This leads to a very different film morphology. For instance, much less shadowing, which favors smooth film formation. Let's now consider how we can derive the thickness of the film, deposited from an evaporation source. Consider a small sphere dS_1 that evaporates material in all directions at a given rate as shown here. We call such an evaporation source, a point source. In this case, the material passing through a solid angle $d\Omega$, in any direction per unit time is given by this equation. In reality, the evaporation comes from a plane source with the area dS_1 , and the material is evaporated from one side with a certain rate. In this case, dm can be written as the following. In the case, the material flux arrives at a small area dS_2 on a surface that is inclined by an angle θ with respect to the normal to the direction of the vapor stream as shown here, we can write the equations as follows. And we can rewrite the two equations for the point source and the planar source as follows. So how can we now get to the thickness of the film, let's assume that the material has a density ρ_d , in grams per cubic centimeter and the film thickness per unit time is T in centimeter per second. Then the volume of the deposit on dS_2 must be T times dS_2 , and we can rewrite dm as follows. Then our two formula for the planar source and the point source can be rewritten finally as shown here in green.



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For high throughput integrated circuit and MEMS processing, we need to be able to coat large numbers of wafers, each requiring a uniform film thickness. In this case, we use a planetary system that consists of rotating spherical sections. The principle behind is shown here. The receiving surface is spherical, having a radius r_0 that includes also the planar source. We can already state that the angle ϕ equals the angle θ and we can write $\cos \phi = \cos \theta$ is given by $r / 2r_0$. Taking what we did use in the previous slide, we can rewrite now the thickness like follows. So the thickness is independent from the radius r . That means that the deposition rate is the same for each point on the spherical surface. Thereby, a uniform film thickness can be obtained also for a large number of wafers. In a real evaporator system, the wafers are arranged therefore in a spherical holder called planetary, as you will see in the next section of this chapter in more details.

Thermal evaporation: materials and parameters

Find [here](#) a PDF file containing deposition parameters for various materials evaporated with the [Leybolds Optics LAB 600H at CMI](#). The different columns of the file correspond to the following points.

- Recipe number
- Recipe category according to the nomenclature defined in the first page of the document
- Sequence of deposited materials in the recipe
- Substrate holder temperature
- Base pressure prior to deposition
- Presence of oxygen to perform reactive deposition
- Use of ion assisted deposition (see section about other PVD methods for explanations)
- Deposited material and corresponding crucible
- Typical deposition rate
- Maximum film thickness in one deposition and possibility to repeat the depositio

Practice quiz thermal evaporation: introduction and vapor creation

Questions:

1. Which parameter determines the maximum evaporation rate in a PVD system based on thermal evaporation ?

- The condensation rate of the evaporant
- The equilibrium vapor pressure of the evaporant
- The boiling point of the evaporant
- The mean free path in the evaporation chamber

2. What phenomenon occurs when we increase the temperature of the evaporant in a PVD system?

- The evaporated atoms mean free path decreases
- The vapor pressure of the evaporant increases
- The thickness of the deposited film is more uniform
- The stoichiometry of the deposition is changed

PVD 2: Thermal evaporation Film formation and examples

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Now let's have a look in detail how the film forms on the surface. As mentioned before, the long mean free path allows for very directional flux of evaporant. This has an effect for surfaces that are not perfectly flat

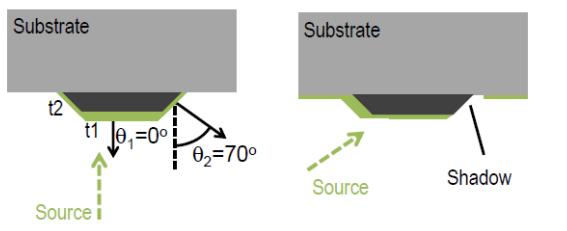
- Thermal (or vacuum) evaporation
 - Physical principles
 - Equipment
 - Vapor creation
 - Vapor flux
 - Film formation
 - Examples

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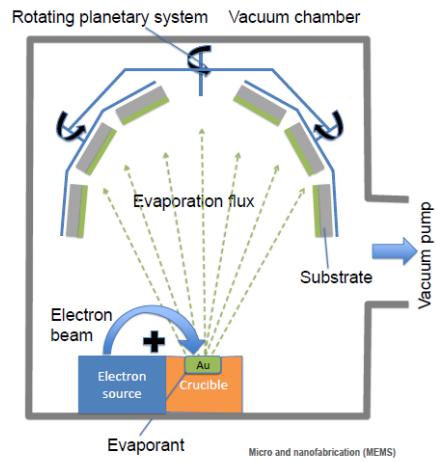
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as often encountered in MEMS and microfabrication with 3D surface features. The left image shows a situation for a tapered surface structure in grey, that has to be coated by the thin film in green with the source coming from the bottom.

- Uniformity issues by topographical surfaces and by shadowing



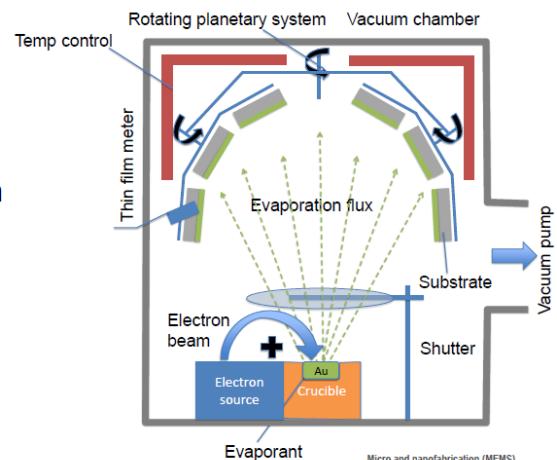
$$\frac{t_1}{t_2} = \frac{\cos(\theta_1)}{\cos(\theta_2)} \approx 3, \text{ when } \phi = 0^\circ, \theta_1 = 0^\circ, \theta_2 = 70^\circ$$



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Now, by simple geometrical consideration, one can already see that on the flat part, that is facing the source, we obtain the target of thickness t_1 , whereas on the sloped part of the structure, we have a thickness of only about one third of the target thickness in the case of an angle of 70 degrees like shown here. This can be calculated simply by geometrical considerations. Another important case is the off-axis position of the wafer, which we always have in this sort of arrangement, is that if we have surface features we can create a shadow effect because of the directionality of the beam.

- Shutter
- Thickness monitor
- Temperature control
- Pressure control
- Gas inlets for reactive evaporation
- Stress optimization



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which can not deposit on the lee side of this structure. Consequently, there is a much thicker film deposited on the slope, facing the source, than on the slopes that are under an angle to the source or actually invisible to the source. To overcome this important drawback, modern evaporator tools



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are equipped with rotating planetary systems as shown here which repositions the wafers during the evaporation and cancels the aforementioned effects. Thus, every wafer in the planetary system receives the exact same amount of material under various angles which yields a well controlled film thickness across a wafer's surface, and from wafer to wafer in a batch.



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In addition to the basic configuration of a thermal evaporator, there are some other features that have been incorporated for better control and monitoring. One of them is the mechanical shutter shown here that blocks the flux between the crucible and the wafers and allows for very precise timing of the deposition. It's much more precise than switching on and off the heat source. Another important feature is the thin film monitor, typically a quartz crystal microbalance that measures the added mass which can then be used to deduce the thickness that has been added on each of the wafer. We can furthermore control the temperature of the substrate.

- Thermal (or vacuum) evaporation
 - Physical principles
 - Vapor creation and vapor flux
 - Film formation
 - Condensation on the substrate
 - Examples
 - Lift-off and Stencil lithography
- Sputtering
- Other methods

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either by cooling or heating which has an important influence on the film morphology as the thin film grows.

Further, we can always control the pressure in the chamber and also inlet some specific gases for reactive evaporation. All these features have an influence on the stress of the thin-film as it grows on the surface and can be optimized if one knows how they influence the growth mechanism. Here on this photograph, you can see the inside of one of our clean room thermal evaporators. On the bottom you can see the crucible with the mechanic shutter, and on top, you can see the wafer holder system that holds a couple of wafers for thin film coating. And here you can see a close up photograph of the crucible area with the mechanical shutters. More details of these equipment aspects will be shown later in a dedicated Section taken in our clean room. So now that we have seen the basic principles and equipment aspects of thermal evaporation, let's have a look at some characteristic examples. I want to show you in particular the so-called lift-off technique and

then stencil lithography. They both rely and benefit from the long mean free path and shadowing effect that we can obtain in thermal PVD. Let's have a look at the lift-off which is a particular example where thermal evaporation PVD is very useful.

1. Photoresist patterning (Slope!)
2. PVD with shadow effect (directional)
3. Photoresist stripping

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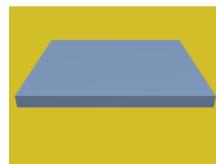
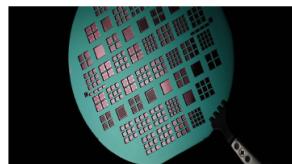
Lift-off is done typically on a substrate like shown here, like a silicon wafer that has been coated with a layer of photoresist and patterned by lithography, it is a photoresist layer that has an opening by lithography and development and now we come with the source that is far away, that emits chromium as material in a vacuum chamber, which deposits now all over the surface and forms a film which has more or less this shape. Where this is chrome. You notice now that the photoresist was designed to have a certain sloped angle which prevents that the directional flux of material creates a bridge from the part of the film that is on the photoresist and part that is directly on the substrate. Now the actual lift-off is then the stripping of the photoresist, which is a liquid, a solvent, that can penetrate through the openings and start to remove the photoresist from this part and removes everything that is also on top of it. And the same on this side.



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Which leaves us at the end... the chrome pattern that we want and this chrome pattern now has been made simply by one lithography and deposition without the need for etching. Some materials are indeed very difficult to etch so the lift-off is a very convenient way to create micro and nano patterns by this technique. Here you can a live demonstration of a lift-off step in our clean room. A glass wafer has previously been patterned with a photoresist and then coated by PVD evaporation with a thin film of chrome. When placing the wafer in a solvent, for example, Acetone, that photoresist dissolves after some time and also removes the metal layer on top of it. This lift-off process takes a few seconds depending on the materials involved and the dimensions. It helps to mechanically move the wafer in the bath. Also ultrasound can be applied in some cases. In this step, the appearance of the patterned metal structures

1. Align and position stencil
 2. PVD with shadow effect (Long mean free path)
 3. Third: remove stencil
- No heat and chemical process



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become visible. At the end, the glass substrate is rinsed with the solvent to remove remaining residues on the surface, then rinsed in DI water and finally dried for further use. The second example that benefits from the long mean free path and the shadow effect in PVD is stencil Lithography which is shown here where a very thin membrane with apertures is approached close to the surface to be coated and then when we get material evaporated with a very directional flux, there is the deposition of the material on the stencil but also through the apertures on the substrate like shown here. The third step would then be to remove the stencil simply mechanically and the surface features are created without any further heat or chemical processes which makes this technique very suitable for patterning fragile substrates. In the animation, you can see now how the, material is deposited through the stencil on the surface leaving their features and the second step here also shows that this stencil technique can be used for local etching. Here you see photos of our clean room equipment from thermal evaporation. One the left side is shown the front panel with a loading port and the control panel. On the right photo you see how the equipment looks from the back side with all the connections for pumps, heat sources, monitors, et cetera. A sophisticated equipment like this has many features as you can see here, an e-beam source with the pockets



- Leybold Optics LAB 600H
 - 1 x e-beam, 6 pockets
 - 1 x resistive heating
 - 1 x ion source for IAD + cleaning
 - Ag, Al, Au, Cr, Ge, In, Mo, Ni, NiFe, Nb, Pd, Pt, Ta, Ti, Y, Al₂O₃, ITO, La₂O₃, MgO, SiO₂, Ti₂O₃, Ti₃O₅, Y₂O₃, ZrO₂, MgF₂
 - 4 and 6 inches wafers
 - Large source-substrate (1010 [mm]) distance for lift-off
 - Deposition from RT to 200 [°C] (heaters)
 - Cryopump to reach high vacuum of 10⁻⁶ to 10⁻⁷ [Torr]
 - Quartz-crystal deposition rate monitor

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for various materials, resistive heating, then here is a list of possible materials that can be evaporated in such an equipment, it can hold four and six inches wafers. It has a very large distance between the source and the substrate, more than one meter and you remember this is important for the directionality and shadow, and which is therefore very good for lift-off, it can deposit from room temperatures to 200 degrees, and it has a very strong pump to reach a vacuum in the order 10 to -6, 10 to -7 Torr. And it has the before mentioned quartz, crystal deposition rate monitor. This concludes this part of the PVD lesson on thermal evaporation. You have seen that it is a fast and simple technique to coat a wafer with a thin material film. There is no surface damage, it is done in a high vacuum which yields high purity films. No atoms from the atmosphere are incorporated into the film. Limitations come from the shadowing poor step coverage of high aspect ratio structures, non uniformity over large areas and the difficulty to evaporate compounds because of their

decomposition or phase change at high temperature. So let's now have a look in the clean room how such an equipment is operated in details. In the next lesson, I will explain to you how sputtering can be used to form a thin-material film.

Simple, fast and affordable technique
No surface damage
Electrically conducting and insulating materials
High purity films

Shadowing
Poor step coverage of non-planar structures
Non-uniformity over large areas
Difficult to evaporate compounds

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Thermal evaporation in CMI



Evaporation is performed in the vacuum chamber. The evaporant is heated in a crucible at the bottom of the chamber and the vapour flux condensates on the wafer surface placed in the upper part of the chamber. A large source substrate distance, here roughly 1 meter, enables directional deposition that is important for lift-off processes. Different standard evaporants are permanently loaded in various crucibles inside the evaporation chamber. The material to evaporate is selected by rotating the crucibles at the bottom of the chamber. If an additional material is required, a crucible filled with the material to be evaporated can be placed in an empty pocket. In this specific case we used chromium. A shutter is used to control the deposition. When the shutter is covering the evaporation source no vapour flux can reach the substrate. To start the deposition the shutter is moved on the side and the flux can reach the substrate. Such a mechanical shutter is much better to control the on off state of deposition, compared to switching on or off the evaporation itself. This sequence shows some typical substrate before evaporation. For standard micro nano fabrication, we typically use silicon or glass substrates. Here are shown a couple of silicon wafers that are either bare silicon in grey, or silicon with dielectric coating, silicon nitride in this specific case, which gives the nice blue colour. The wafers are first loaded upside down into the sample holder which has an opening at the bottom which itself is then loaded into the evaporator chamber. The chamber is closed and pumped down to reach a vacuum of about 10 to the minus 7 torr. The pumping is the longest step in the evaporation process. It takes a few minutes to several tens of minutes depending on the required level of vacuum. This leaves some time for the scientists to discuss with students and technicians. The evaporant is then heated in this case with an electron beam. Depending on the material the electron beam movement varies. For chromium for example which is not a very good thermal conductor the beam sweep is rather large. Here the sweep speed is reduced compared to the one used in a real process for the purpose of this Section . When using gold on the other hand the sweep area is smaller as it is an excellent thermal conductor. Finally this last example shows titanium in the crucible under the bombardment of the electron beam.The deposition time depends on the rate and required thickness Typical times for 30 nanometer gold are in the order of 1 to 1.5 minutes. Once the desired film thickness is reached, the shutter is closed and the e-beam power is ramped down. After a cooling period of about 20 minutes, the chamber is vented opened and the wafers are unloaded. Note that here we see the back side

of the wafers and not the coated sides. After removing the wafers from the holder and turning them around we can see here the wafers after deposition. Gold in yellow and chromium in grey. The blue ring of the underlying silicon nitride layer at the wafer edge stems from the shadow of the wafer holder.

Practice quiz thermal evaporation: film formation and examples

Questions:

1. So-called shadowing effects are causing problems when aiming for smooth and uniform film thickness on a substrate. How do modern thin film deposition tools based on thermal or e-beam evaporation avoid issue related to shadowing?

- Rotating the substrates with a planetary system
- Using multiple sources
- Reducing the pressure inside the chamber
- Implementing a mechanical shutter

2. Several parameters influence the deposition rate during thermal evaporation. In practice, what is the parameter used to control the deposition rate during evaporation?

- The gas pressure inside the evaporation chamber
- The amount of heat supplied to the evaporant
- The mean free path of the atoms in the chamber
- The distance between the source and the substrate

PVD 3: Sputtering

I. Introduction and plasma formation

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Prof. Jürgen Brugger & Prof. Martin A. M. Gijs

In this lesson, I will introduce the second PVD technique that is called sputtering, and which allows for a whole variety of thin film materials to be deposited.

- Physical principle
 - Plasma, spatial zones, Paschen law
- Sputter variations
 - DC sputtering
 - RF sputtering
 - Magnetron sputtering
- Ions-target interactions
- Sputter examples
- Other PVD methods
- Film growth and control parameters

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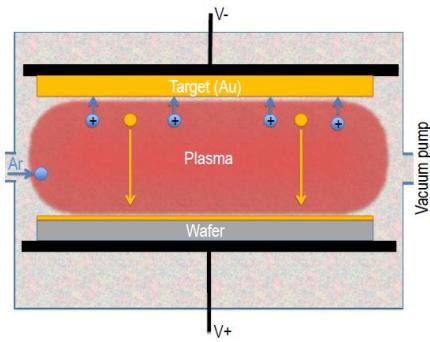
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In fact many more than for thermal evaporation. I will first show some basic physical principles on how a plasma is created for our purposes, show the different plasma zones in the sputter chamber, and how to optimize it for efficient sputtering and also introduce the Paschen law.

- Working principle

- Target made of material to deposit
- Plasma ions collide on target
- Atoms from target are ejected
- Atoms deposit onto the wafer

- Deposition of compounds
- Deposition of refractory materials
- Good adhesion
- Good step coverage
- Deposition of relatively thick layers

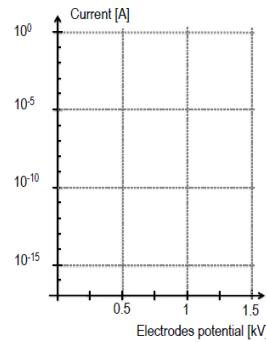
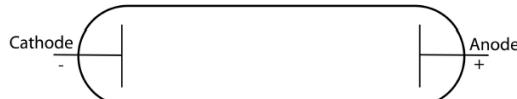


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The goal of the sputter process is to remove physically material from a target and deliver it to the receiving substrate or wafer. This is done by ion bombardment in the plasma. Ions that hit the target with sufficient energy eject atoms from the target. These atoms are then deposited as a thin film on the wafer placed adjacent to the target. So how is this done exactly? Let's have a look. First, the air is pumped out of the chamber to create a vacuum. It is shown here, this is the chamber with the vacuum pump

- High voltage between electrodes
- Breakdown of the gas
- Ar ions collide on the cathode
- Secondary electrons sustain plasma



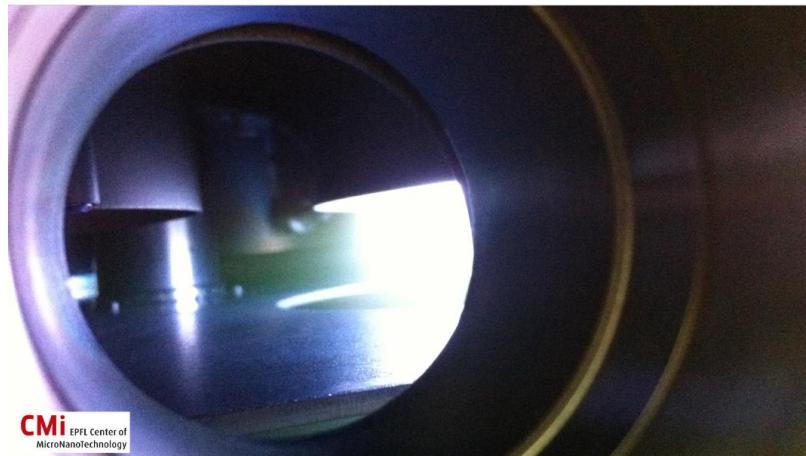
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that evacuates this area from air. That chamber is then filled with argon, an inert gas, until the pressure reaches values in the order of a couple of hundred mTorr. A plasma is then created by applying a high voltage of about 1500V between two electrodes, shown here. The positive argon ions in blue are accelerated towards the cathode which is the negatively biased electrode and hits the target here, so the target - in this case we choose gold as a material - and here is the wafer on which we want to deposit the gold. The target is in fact made of the material that we want to deposit and it is mounted directly onto the cathode. With the impact energy, atoms are ejected from the target, here in yellow, travel through the plasma, and finally deposit on the wafer as a thin film. Sputtering allows to deposit all kinds of materials including metals, compounds as well as refractory materials. The deposited thin film has a generally good adhesion and excellent step coverage. We will come to these details later in this lecture. Let's have a short look at what plasma is and how it works for our purpose here. Plasma is defined as a partially ionized gas that is neutral, and thus has the same number of ions and electrons. It is commonly also referred to as the fourth state of matter. By the way, plasma is also used for dry etching processes that my colleague, Martin Gijs, will cover in detail in his corresponding lesson. The simplest form of plasma for our purpose, the DC plasma, is created as follows. First, the chamber is pumped down and filled with argon gas to reach a deposition pressure in the order of 10 to 100 mTorr. It is shown here, some argon atoms in the chamber. Second, a DC voltage can be applied between these two electrodes, shown here. So with the source... with the thermal resistance, and here the potential that can be applied to the cathode and the anode. At low voltages, the only measurable current comes from the so-called

"background ionization", which is always present, but often negligible. The origin of this background ionization comes for example from a photon that hits one of the argon atoms and ionizes it. The result of this ionization is that we get an electron and an argon ion. This current is very low and the voltage on the electrodes is about the same as the voltage of the source as there is nearly no voltage drop over R_s .

If you increase the voltage, the current first remains constant since the voltage does not affect the background ionization. We can draw here a typical curve, how this current increases if you increase the potential between the electrodes. There is a slight increase, but it is not very drastic because it is only based on the available ions due to the background ionization. When the voltage is further increased, over 600V approaching 1kV, depending on the gas and the pressure, electrons and ions resulting from the background ionization gain enough energy to ionize other atoms. So this electron, for instance, can ionize this argon atom which would release another electron, and be able to release another argon ion. As a result, the current increases exponentially with the voltage. So, now we are increasing drastically the current for the given voltage. The regime described here is called "dark discharge" as no light is generated.



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It is not used for microfabrication applications as plasma in this regime is neither energetic nor stable. When the electric field between the two electrodes is further increased, breakdown of the gas occurs. The medium becomes ionized, and an avalanche of inelastic collisions between electrons and ions appear. So now, even argon atoms that have not been ionized by the background radiation, can be ionized by the strong electric field between the two cathode and anode. So, one can create here electrons, and here argon ions with all the available argon atoms in the chamber. And this is creating an avalanche effect, because they can then ionize other argon atoms that are available. That means we suddenly have a very strong current that can be installed between the cathode and the anode. So, this is also shown here in the curve, where we now get a very strong current, up to a couple of hundred milliamperes but with a drop in the voltage. Indeed, as the current increases, the voltage drop in the source resistance becomes very important. When argon ions collide on the cathode, secondary electrons are ejected and sustain the plasma. Without these electrons, the plasma would rapidly vanish. Finally, the plasma reaches a steady state and the loss and gain of electrons is equal. In this regime, electrons have enough energy to excite atoms to an energy level where they emit light, when they relax, to a lower energy level. The plasma is luminous, and this regime is called "glow discharge". In this regime, the plasma is stable and energetic enough to be used in microfabrication technology, either for sputtering or for etching. Typically, to achieve this regime, a voltage of about 1.5kV is applied between electrodes separated by 15cm, which results in an electric field in the order of 100V/cm. In this photograph, you can see the glow of the plasma in one of our sputter equipment. We will see more of this later when we go and see what the equipment looks like.

Practice quiz sputtering: introduction and plasma formation

Questions:

1. Which of the following statements related to sputtering techniques are correct?

- Sputtering allows for the deposition of metal, compounds, and refractory materials
- Sputtered thin films usually have a poor adhesion
- Sputtering shows better step coverage than evaporation
- Sputtering heats up material in a crucible using an electron beam

2. Which of the following statements related to plasma are correct?

- Plasma is defined as partially ionized gas and it is overall electrically neutral
- Plasma can be used for sputtering as well as dry etching
- Plasma in “Dark discharge” region is used for microfabrication
- Secondary electrons are needed to sustain the plasma

PVD 3: Sputtering

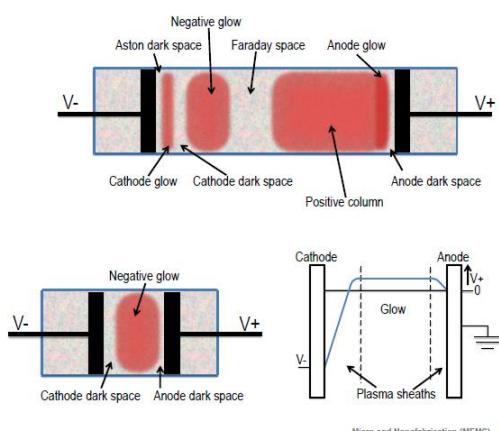
II. Spatial zones and Paschen's law

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Electrons and ions don't have the same mass. Electrons are lighter and thus have a higher mobility when accelerated in an electric field gradient.

- Electrons are lighter than ions
 - Electrons and ions mobility differs
 - Charged areas along the plasma
 - Electric field is not constant
 - Electrons energy varies
 - Bright and dark spatial zones
-
- Small inter-electrodes distance



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As a result, in a plasma, ions and electrons don't move at the same speed which creates positively and negatively charged areas. Consequently, the electric field is not constant along the plasma and the electron energy varies and creates thus bright and dark areas, as shown here in this slide on the upper right side. And we have the plasma chamber with the cathode and the anode and different zones in the plasma due to the different mobility of ions and electrons. For more details about plasma zones, please have a look at the accompanying documents. Bright areas are called glow, and dark areas are called dark space. In the practical setup for sputtering or etching, the distance between the two electrodes is rather small. In the order of 15cm, as we have seen before. This is showing a chamber with the cathode and the anode and the plasma in between. As a result, the anode, which is the positive electrode, is placed in the negative glow. Therefore, the plasma column can be simplified from here to here and only the cathode dark space, the negative glow and the anode dark space subsist. Negative glow, cathode dark space, and the anode dark space. The potential changes very abruptly close to the electrodes in the plasma sheets and it is constant in the glow

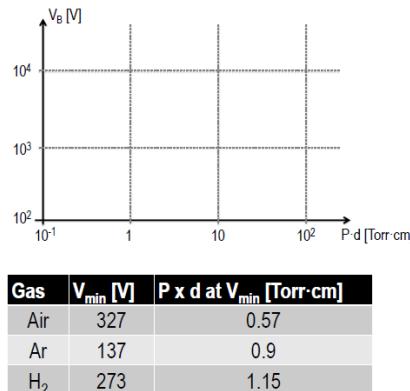
region of the plasma. As shown here. There is a very steep slope of the potential difference of the cathode into the plasma vacuum, then the plateau where the glow area is and here again a steep slope, and we approach the anode. And these are the two plasma sheets. The origin of this plasma sheet, as well as the computation of the potential along the plasma, is studied in more details in the chapter about dry etching. The required voltage to initiate the breakdown of the gas and create the plasma, depends on three main parameters which are the pressure, the inter-electrode distance and some gas properties. This was first observed by Paschen who found out that the breakdown voltage could be plotted as a function of the product between the pressure and the inter-electrode distance. It results in an asymmetric parabola with a minimum at a specific Pd product, like shown here. Here we have the typical curve, for example a gas like argon. And we plot the breakdown voltage and the plasma is breaking down as a function of the product, the pressure and the distance. Paschen has found that this curve in fact can be expressed by an equation that is shown here which gives the breakdown voltage as a function of this series of parameters like for example the pressure and the electrode distance as we already know, times an empirical constant which is observed in experiments, and then as a function of the secondary electron emission coefficient at the cathode which plays an important role. Here, three example gases with the breakdown voltage for a given value of pressure and distance. On the left side of the curve minimum, one needs a higher voltage to reach breakdown because there are less molecules between the electrodes available for the reaction. As a result, when the gas, atom, or a gas molecule is ionized free electrons reach the anode without colliding with other gas molecules, and they are lost. For the breakdown of the gas to occur, higher voltages have to be applied in order to increase the number of free electrons and thus the probability of collisions with other molecules. However, on the right side of the minimum of this curve we have another effect for the breakdown voltage to increase again.

- Breakdown voltage

$$V_B = \frac{BPd}{\ln(APd) - \ln\left(\ln\left(1 + \frac{1}{Y_{SE}}\right)\right)}$$

V_B = breakdown voltage in [V]
 P = chamber pressure in [Pa]
 d = anode-cathode distance in [m]
 Y_{SE} = secondary electron emission coefficient at the cathode
 A, B = empirical constants

- Minimum breakdown voltage



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Now, due to the large number of gas molecules between the electrodes, electron molecule collisions become more frequent and the electron's mean free path becomes shorter. As a result, electrons don't gain enough kinetic energy to ionize other gas molecules when colliding with them, unless a higher potential is applied. For each gas, the minimum breakdown voltage and the corresponding Pd product is different. These values depend on the gas molecules, mean free path, the ionization potential and the speed at which the gas molecules can recapture electrons after they have been ionized. Numerical values for the most common gases are given in the table here at the bottom right of the slide but values for many other gases can be found in the reference book. For sputtering, it is not always favorable to work at the minimum breakdown voltage. Indeed, it is more important to work with lower pressures and thus with a higher breakdown voltage in order to have energetic ions striking the cathode and removing atoms that can be deposited as a thin film on the wafer. So now we have seen some basic physical principles behind sputtering, about how to create a plasma

and the Paschen law. So now, let's have a look at the three main implementations of the sputter technique, that is the DC, the RF, and the Magnetron sputtering.

- Physical principle
 - Plasma, spatial zones, Paschen law
- Sputter variations
 - DC sputtering
 - RF sputtering
 - Magnetron sputtering
- Ions-target interactions
- Sputter examples
- Other PVD methods
- Film growth and control parameters

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Sputtering: plasma detailed explanation

Find [here](#) pages 160 to 167 of the book “Fundamentals of Microfabrication and Nanotechnology, Volume II, Manufacturing Techniques for Microfabrication and Nanotechnology” by Marc J. Madou. These pages describe physics of DC plasma, spatial zones in a DC glow discharge and the Paschen’s law. Some typical minimum breakdown voltage values for several gases are also given.

Practice quiz sputtering: spatial zones and Paschen law

Questions:

1. In a standard DC sputtering tool using an Ar plasma, you plan to deposit a thin film using a chamber pressure of 400 Pa. However, it is not possible to initiate the plasma under these conditions because the voltage provided by the power supply is too low. What would be the most suitable practical solution?

- Increase the gas pressure in order to decrease the breakdown voltage
- Decrease the gas pressure in order to decrease the breakdown voltage
- Increase the distance between the target and the substrate
- Decrease the distance between the target and the substrate

2. We know that in DC plasmas, there are spatial zones with different plasma characteristics. Which of the following statements is correct?

- The cathode dark space has the strongest electric field in the discharge
- Lack of collisions between electrons and gas molecules leads to formation of dark spaces
- Electrons gain more energy as they pass negative glow and accelerate toward anode
- Emission of light in negative glow zone is due to higher temperature of this region compared to the rest of plasma

PVD 4: Sputtering DC, RF, magnetron

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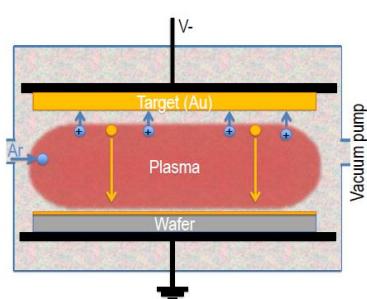
- Physical principle
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Now, we'll have a closer look how in a clean room the various sputter equipment are working. I will show DC, RF, and Magnetron sputtering.

- Target on cathode
- Substrate on anode
- High DC voltage to create a plasma
- Advantages
 - Simple setup
- Limitations
 - Substrate cooling is required
 - Only for electrically-conductive materials



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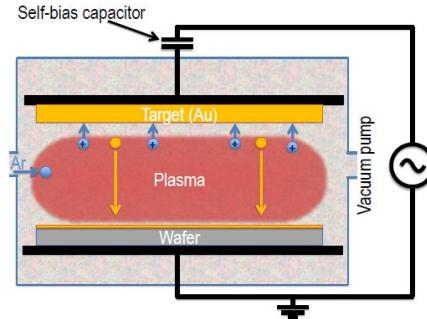
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DC sputtering is one configuration of a sputtering system shown here on the right of the slide. As in every sputtering systems, the material target is placed on the cathode while the substrate is placed on the anode.

To create a plasma, a high DC voltage in the order of 1kV or more, is applied between the electrodes. This is why we call the system "DC sputtering". Usually the anode is grounded and the negative voltage is applied to the cathode. Atoms that are ejected from the target under the bombardment of positive ions condense on the wafer thereby forming the desired thin film, like shown here.

- Target on cathode
- Substrate on anode
- RF voltage to create a plasma
- Capacitance for self-DC bias

- RF sputtering conditions:
 1. Avoid target charging: $f > 50$ [kHz]
 2. Energetic ions sputtering the target: $f > 5$ [MHz] & cathode capacitive coupling
 3. Sputtering on cathode only: anode larger than cathode



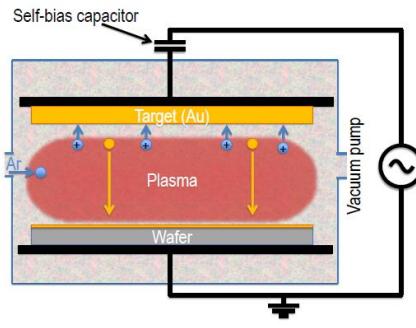
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- Target on cathode
- Substrate on anode
- RF voltage to create a plasma
- Capacitance for self-DC bias

- Advantages
 - Dielectric deposition
 - Higher deposition rate than DC sputtering
 - Lower power consumption than DC sputtering

- Limitations
 - Target cooling is required
 - Substrate cooling is required



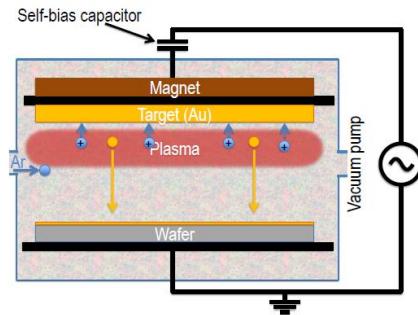
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The main advantage of this system is its relative simplicity. However, it suffers from two main limitations. Firstly, the plasma is present in the entire area between the electrodes which has the consequence that this space is filled with electrons which are repulsed by the negative cathode and collide on the substrate. As a result, the substrate substantially heats up and efficient substrate cooling is required. Secondly, it is possible to deposit only electrically conductive materials with DC sputtering. Indeed, if an electrically insulating target is used it will charge within a few milliseconds due to the accumulation of positive Argon ions on the target. As a result, the plasma would stop. RF sputtering main difference with DC sputtering is the way how the plasma is created. As in the case of DC sputtering, the target is placed on the cathode to attract the positive ions and the substrate is placed on the anode. The difference is that, here the plasma is created applying a high frequency RF voltage between the electrodes. As you will see in details, using AC voltage instead of DC voltage has the main advantage to avoid target charging and thus allows the position of electrically insulating materials such as dielectrics. The key element to add to a system using an AC voltage is a self-bias capacitor, shown here. To enable RF sputtering, the following three conditions are required. First, avoid target charging as the cathode where the target is placed will alternate between positive and negative voltages. Both ions and electrons will accumulate on the target resulting in a null overall charge of the target. However, if the frequency is too low accumulation of ions during one single negative period of the signal can be sufficient to charge the target if it's electrically insulating, and to terminate the plasma. Using frequencies higher than 50kHz allows overcoming this drawback as charging time becomes shorter than a millisecond, which is too short to charge the target. Second, it is required to have energetic ions colliding on the target. If you simply use the AC voltage to accelerate ions the energy they will gain during one cycle is too low to eject atoms from

the target. A solution to overcome this effect is to use frequencies larger than 5MHz typically, 30.56MHz, and the capacitor at the cathode for DC self-bias. At such high frequencies, ions cannot follow the RF field anymore, due to their mass. On the other hand, electrons are lighter and can follow the RF field. They will then alternatively strike the cathode and the anode. However, because of the capacitor at the cathode they will accumulate there, and the cathode will progressively be negatively biased. This negative DC voltage will then accelerate positive ions from the plasma, and enable the sputtering process.

- Target on cathode
- Substrate on anode
- RF voltage to create a plasma
- Capacitance for self-DC bias
- Magnet to confine the plasma



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● Lorenz force $\vec{F} = q\vec{v} \wedge \vec{B}$

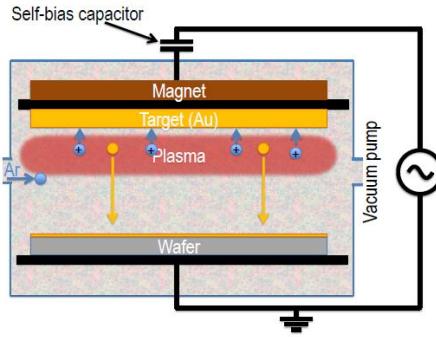
$$\begin{aligned} F &= \text{force in [N]} \\ q &= \text{elementary charge in [C]} \\ v &= \text{particle speed in [m/s]} \\ B &= \text{magnetic field in [T]} \end{aligned}$$

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The third condition is to avoid sputtering of other surfaces than the target. For example, avoid having ions colliding somewhere else than on the target. To do so, the anode must be larger than the cathode. This result is studied in more details in the chapter about dry etching given by my colleague, professor Martin Gijs. The reason behind is that having a smaller cathode allows having a larger potential drop and thus more bombardment, because of current conservation. In a typical RF sputter system, the anode and the entire chamber are therefore grounded to satisfy this condition. The main advantage of RF sputtering over DC sputtering is its ability to overcome charging problems and thus to deposit electrically insulating materials, such as dielectrics. In addition, electrons oscillating in the RF field couple the energy more efficiently to the plasma, as a result, compared to DC sputtering, higher deposition rates are achieved and lower power consumption is required in the RF sputtering. However, there's one main drawback leading to the deposition of the electrically insulating materials. These materials are often poor heat conductors which requires very efficient cooling of the target during the sputtering. In addition, as for the DC sputtering, the plasma is not localized and many electrons hit the substrate and heat it up thus substrate cooling is also required. To even further increase the plasma efficiency and thus the deposition rate

- Advantages
 - Lower voltages
 - Lower pressure = higher purity
 - Higher deposition rate
 - Less substrate heating
- Limitations
 - Complex system
 - Non uniform wear of the target

- Magnetron with RF and DC sputtering



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magnetron sputtering systems are introduced. The added feature compared to the RF system is the magnet placed behind the cathode, shown here which creates a magnetic field, who's goal is to confine electrons so they stay close to the cathode, and induce a lot of collisions with argon atoms to ionize them and contribute to the sputter process. Let's have a closer look how this works and what it brings. So, let's assume that we have here our target material that we want to sputter any metal or dielectric so we mount our target on a setup that includes a magnet so, here we have a magnet, which has magnetic field lines showing like this and that means we have here to close the magnetic field here, magnetic field, that are going into the plasma and here we have an electron in this area it will spiral and follow the field line as schematically show here.



Target after short usage
~ 254 x 127 mm



Extensively used target

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So why is that? You all know that we have here the south and north pole of the magnet and we have here, an electron that has a certain velocity V and within the magnetic field B , that we have then a force that is orthogonal to the two vectors of the velocity and the magnetic field so that, this electron has no other choice than spiraling around the magnetic field line, and follow it, basically. Due to Lorentz forces, electrons follow a helical trajectory while ion trajectory is not influenced because of their higher mass. So, having a magnet behind the target allows to confine electrons close to the target. This improves ionization efficiency, because of the larger amount of collisions between Argon atoms and electrons. As a result, it is possible to use lower voltages and lower pressure, which allows deposition of film with higher purity. In addition, the plasma is localized. This enables higher deposition rates because of the larger amount of ions impacting the target, and also decreases substrate heating, as less electrons collide on the wafer. On the other hand, the system becomes more complex and the wear of the target is non-uniform. Here on these two photographs you can see two targets of a magnetron sputtering tool. The left image shows the target after some short term usage where we can start seeing how the material is being eroded. On the right photo, we see a similar target after extensive use where a lot of the material has actually been removed. The pattern here shows the ion distribution as a function of the magnetic field provided in the magnetron sputtering tool. So now we have

seen how DC, RF and magnetron sputtering are working. Let's have a closer look how actually the ions are interacting with the target material to be able to remove material and deposit it on the substrate.

- Physical principle
 - Plasma, spatial zones, Paschen law
- Sputter variations
 - DC sputtering
 - RF sputtering
 - Magnetron sputtering
- Ions-target interactions
- Sputter examples
- Other PVD methods
- Film growth and control parameters

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Practice quiz sputtering: DC, RF, magnetron

Questions:

1. Which of the following equipment allows depositing a SiO₂ thin film?

- DC sputtering tool
- RF sputtering tool
- Magnetron DC sputtering tool
- Magnetron RF sputtering tool
- Electron beam evaporation tool

2. Choose the correct order of the listed sputtering techniques variations that have the following characteristics:

- I. This technique is suitable for the deposition of SiO₂
- II. With this technique, the plasma extends to the entire chamber
- III. This technique enables high purity films
- IV. With this technique the target wear is uniform

- I. RF sputtering – II. DC sputtering – III. RF magnetron sputtering – IV. DC magnetron sputtering
- I. DC magnetron sputtering – II. DC sputtering – III. RF magnetron sputtering – IV. RF sputtering
- I. RF sputtering – II. DC magnetron sputtering – III. RF magnetron sputtering – IV. DC sputtering
- I. RF magnetron sputtering – II. RF sputtering – III. DC magnetron sputtering – IV. DC sputtering

PVD 5: Sputtering

I. Ion target interactions

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So in this lesson, we will now have a closer look at how ions are interacting with the target material in order to remove the material from the target, and to sputter it on the substrate.

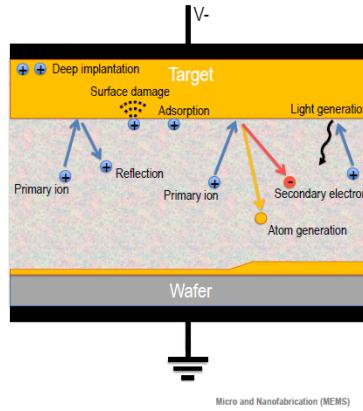
- Physical principle
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When a so-called primary ion collides with a target, made of the material to deposit, several interactions may occur, as illustrated in the figure on the right side of the slide. The interaction depends primarily on the ion kinetic energy, the type of ion, and the target material. Negatively charged electrons in the cathode will then neutralize the positive ion, argon in most cases. When the energy is low, smaller than 10 eV, ions hitting the cathode may be reflected, adsorbed, or may migrate on the surface. During the impinging, it can induce some surface damage such as point defects, or topographical changes. It may also induce some chemical reactions on the surface. Ions with high energy, 10 keV or more, will penetrate deeply into the target material and form an implant or compound like shown here. When ions are in the energy range between 10 eV and 10 keV,

- Ions-target interactions
 - Reflection, adsorption, surface damage, gas desorption
 - Secondary electrons, ions and atoms generation
 - Deep implantation
 - Photons and x-rays generation
- 95% of ions energy heats up the target
 - Target cooling is required
- Mechanical energy ejects atoms
 - Compounds and alloys deposition is possible



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they will eject atoms from the target like the ones shown here. This is the action that we want for sputtering. By doing so, they will simultaneously create secondary electrons, and secondary ions. Finally, ions interacting with the target can also result in the emission of photons and x-rays. 95% of colliding ions transmit the energy as heat to the target, therefore cooling is required. Finally, it is worth noting that in sputtering, the deposition of compounds such as carbide, nitrite and oxide is indeed possible, because mechanical energy is used to eject atoms from the target. This differs significantly from the case of the thermal or electron beam evaporation where thermal energy is used to vaporize the solid target material.

Target ejection rate

$$W = \frac{k * V * i * S}{P * d}$$

W = ejection rate in [molecule/m² s]
 V = working voltage in [V]
 i = discharge current in [A]
 S = sputtering yield in [atom/ion]
 P = gas pressure in the chamber in [Pa]
 d = anode-cathode distance in [m]
 k = proportionality constant in [m⁻²]

Metal	Sputtering yield S*
Al	1.05
Cr	1.18
Au	2.4
Ni	1.33
Pt	1.4
Ti	0.51

* With 500 [eV] argon ions

→ Maximize V

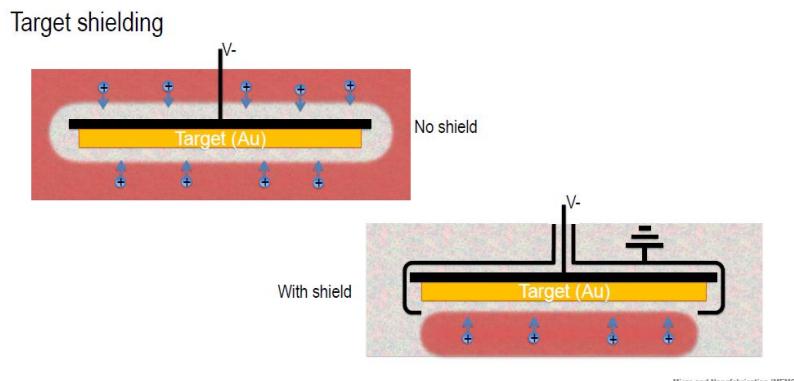
→ Minimize P and d

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So once again, on the drawing you see here the target material in orange, which is biased negatively. And the wafer in grey, that is biased, positively on ground. And now, a primary ion, with a correct energy will hit the target material, will remove atoms from the target, which then fly through the vacuum and will land on the wafer and form the thin film of the target material. Unlike for evaporation, the amount of material ejected from the target does not depend on the vapor pressure, but is given by the so-called ejection rate, W. The ejection rate W depends on parameters such as the sputtering yield, the voltage between the electrodes, the discharge current, as well as the pressure and the inter-electrode distance. From the equation on the left side here on the slide, we see that the target ejection rate increases with the voltage, but is inversely proportional to the pressure and the inter-electrode distance d. This can be explained as follows. When increasing the voltage, argon ions are accelerated more rapidly and strike the cathode with more kinetic energy. On the other hand, when decreasing the pressure, the argon mean free path is increased, and when decreasing the inter-electrode distance, argon ions will collide with less argon, before striking the cathode. As a consequence, argon ions impact the cathode with more kinetic energy. Finally, the target ejection rate also depends on the sputtering yield, S, which is the ability of one ion of a specific gas to eject an atom from the target made of the specific material. Obviously, the sputtering yield depends on the ion energy which itself depends on the voltage, the pressure, and the distance. But it is also related to the type of gas in the reactor, and to the target material. In general, heavier ions usually have larger sputtering yields

and harder target materials result in lower sputtering yields. A few typical sputtering yield values for common materials are shown in the table on the right side here. The different metals, with their corresponding sputtering yield. So here, the target is bombarded with 500 eV argon ions.



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We can see for instance that the titanium sputtering yield is significantly lower than that of for example gold, because titanium is much harder than gold. As explained previously, only the target should be bombarded by energetic ions. To avoid sputtering of other surfaces than the cathode, the anode as well as the entire chamber, is grounded to increase, in fact, the anode area. Still, this would not be enough to prevent sputtering on the backside of the cathode. Indeed, when all the walls of the chamber are grounded, a plasma will still install between the two electrodes, as wanted, but also between the walls and the backside of the cathode as shown here, on the top left image. In this case, energetic argon plus ions, shown here in blue, will also sputter the backside of the cathode and deteriorate it. To prevent sputtering of the structural elements of the cathode, a grounded shield is placed at a distance less than that of the plasma sheath as shown here on the lower right illustration. This way, the space between the shield and the cathode is too small to allow plasma formation and the plasma is contained in front of the target.

Practice quiz sputtering: ion target interactions

Questions:

1. If the plasma ions that impinge on the target have kinetic energy in the range of 10 eV - 10 keV, then the ions will...

- ...be mainly reflected and adsorbed by the target
- ...eject atoms from the target as well as secondary electrons and ions
- ...cause surface migration and surface damage, such as topography changes on the target
- ...create deep implantation and compound formation in the target

2. A grounded shield is used in the chamber of sputtering tools. What is the reason for this?

- To avoid too high temperature
- To avoid damaging the cathode
- To avoid too high pressure
- To avoid too high voltage

PVD 5: Sputtering

II. Film growth and control parameters

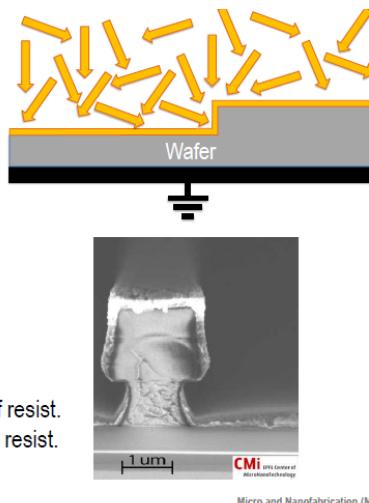
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In order to create a plasma, a certain amount of gas molecules is required between the electrodes. Consequently, the pressure at which the deposition in a sputtering system occurs is higher than that used for thermal or electron beam evaporation.

- Plasma requires atoms between electrodes
 - Pressure in sputtering is higher than in evaporation
 - Atoms undergo many collision from target to substrate
 - Atoms deposit on substrate with random incidence angles
 - Good step coverage: 20-50%
- Reactive and co-sputtering is possible
- Collimated sputtering is possible

Cross section of sputtered Al on double layer lift-off resist.
Large metal sidewall coverage under the T shaped resist.
No real shadow effect.



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We use typically 10^{-1} to 10^{-3} Torr for sputtering, instead of 10^{-6} to 10^{-7} Torr for evaporation. As a result, the mean free path in sputtering is only a few millimeters compared to meters in evaporation. Atoms ejected from the target will therefore collide with many gas particles and ions before reaching the substrate. Due to the multiple collisions, the atoms impinge on the surface with random incidence angles, shown here, with the yellow arrows on this cartoon. Thus, the way atoms deposit onto the substrate and the film grow is different from evaporation. For instance, having a random incident angle allows having a better step coverage compared to evaporation, where a long mean free path produces a line of sight deposition with a possible shadowing effect, as you may remember from the evaporation lesson. If we add a reactive gas in the chamber, reactive sputtering is possible. Atoms ejected from the target react with the gas, for instance oxygen, and form compounds such as oxides. Another deposition technique to deposit compounds is called "co-sputtering". Finally, if needed, a directional sputtering deposition is possible by using a collimated

sputtering. It is done by placing a grid in between the electrodes and thus filtering atoms with high angles of incidence. So on this micro-graph, taken by an electron microscope, you can see an example showing the capability of sputtering aluminum on a double layer lift-off resist. So you see here two layers of photoresist with an overhanging geometry, like a small mushroom, that has been coated by sputtering aluminum. And since the aluminum came under various angles, it was able to deposit also underneath the mushroom. If I'm drawing here again, where we see the aluminum on the mushroom structure, on top, then also here, we have again aluminum that has been deposited.

Sputter parameter	Effect
Voltage/Power	→ Deposition rate Film adhesion
Pressure & inter-electrodes distance	→ Plasma stability, film adhesion, deposition rate, purity, crystal structure
Temperature	→ Film adhesion, uniformity, stress, crystal structure

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Only just underneath the overhanging structure, there has been no or non visible deposition of aluminum because the incoming angles were for the aluminum. Atoms could not reach this shadow part. So let's have a look at how various parameters influence the sputter film quality .Increasing the voltage results in more energetic ions striking the cathode. Consequently, more atoms and more energetic atoms are ejected from the target which leads to a higher deposition rate, and a better film adhesion. Indeed, more energetic atoms have a longer penetrating depth at the wafer surface, and also allow cleaning the wafer surface from remaining contaminants. Adjusting the pressure and the inter-electrode distance is a question of trade-off. As explained previously, Paschen's law gives the breakdown voltage as a function of the product between the pressure and the inter-electrode distance. Thus, for a fixed voltage changing either the pressure or the inter-electrode distance will alter the plasma stability. In addition, increasing the pressure or the inter-electrode distance leads to more collisions of the atoms on their travel between the target and the substrate. As a result, less atoms and less energetic atoms will deposit on the substrate which will lower the deposition rate and also the film adhesion. There is also a risk of contamination of the deposited thin film by argon atoms from the plasma if the pressure is too high. Too high pressure and large inter-electrode distance should thus be avoided. Finally, the pressure also impacts the morphology of the deposited thin film, if it is an amorphous, or forms crystal. This point will be seen in more details in the lesson about film growth. The substrate temperature is another controlled parameter. Increasing the substrate temperature increases the atom energy on the surface and thus improves the diffusion. This leads to better film uniformity and adhesion and lower internal stresses. The temperature also impacts the crystal structure as it will be explained in the film growth chapter. One of the main advantages of sputtering over thermal evaporation is stability to deposit almost any kind of material including metallic and non metallic elements, alloys, ceramics and polymers. In addition, reactive and co-sputtering enable the deposition of oxides and chemical compounds such as nitrites, and carbides, among others as depicted in this table here on the right side. In addition to the wide choice of material to deposit, sputtering ensures a good adhesion of the deposited thin film because of the relatively high kinetic energy of the atoms when they impinge on the substrate. Due to the non directional nature of sputtering, it means atoms arrive on the substrate with random angles of incidence. This deposition technique enables good step coverage, good uniformity over large areas and suppresses shadowing problems typically of thermal evaporation. Sputtering targets can be relatively large and thick, which allows to deposit more material than with evaporation. Sputtering systems are compatible with production processes as large amounts of material can be uniformly deposited over large areas. In addition, sputtering systems can be adapted to roll-to-roll deposition tools. Finally, surface cleaning and activation is possible

Wide choice of materials

Type of Material: Examples
Metals: Al, Cu, Zn, Au, Ni, Cr, W, Mo, Ti
Alloys: Ag-Cu, Pb-Sn, Al-Zn, Ni-Cr
Nonmetals: graphite, MoS ₂ , Ws ₂ , PTFE
Refractory oxides: Al ₂ O ₃ , Cr ₂ O ₃ , SiO ₂ , ...
Refractory carbides: TiC, ZrC, HfC, NbC
Refractory nitrides: TiN, Ti ₂ N, ZrN, HfN, ...
Refractory borides: TiB ₂ , ZrB ₂ , HfB ₂ , CrB ₂ , ...
Refractory silicides: MoSi ₂ , WSi ₂ , Cr ₃ Si ₂

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with a process called "sputter etching". Reversing the electrode's polarity and creating a low energetic plasma will result in ions colliding on the substrate. As a result, these ions will remove contamination layers or particles on the surface and break oxide and surface bonds to activate the surface. Such dry cleaning process using a plasma is less efficient than wet cleaning but has no surface tension effects, doesn't require any drying step, and is performed directly in the chamber where the deposition will take place. In practice, a cleaning step is very common before starting the sputtering process. Sputtering can be done at room temperature, but unless used with magnetron, substrate heating is substantial because of the atom's kinetic energy and bombardment by secondary electrons. The chemical reaction between the substrate and the deposited layer can start. In addition, surface damage can also occur. Because of the substrate cooling system, the setup and material change is more complex than with the thermal evaporation system.

Wide choice of materials
Good adhesion
Good step coverage and uniformity
Deposition of large amount of material
Surface cleaning and activation

Substrate heating (unless magnetron)
Surface damage
Complex and expensive
High purity films are not possible

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And thus the sputtering equipment is more expensive. Finally, due to the high deposition pressure, it is difficult to have high purity films.

Practice quiz sputtering: film growth and control parameters

Questions:

1. Which of the following statements about sputtering are correct?

- During deposition, the pressure in the sputter chamber is higher than in a thermal evaporation chamber
- Atoms deposited on the substrate surface impinge with random incident angles
- It is possible to add a gas in the chamber for reactive sputtering
- Directional sputter deposition is possible

2. What parameter control allows you to increase the adhesion between a sputtered thin film and the substrate surface?

- Increase the voltage between the electrodes
- Increase the pressure at fixed voltage
- Decrease the inter electrode distance at fixed voltage
- Decrease the substrate temperature

PVD 6: Sputtering Examples

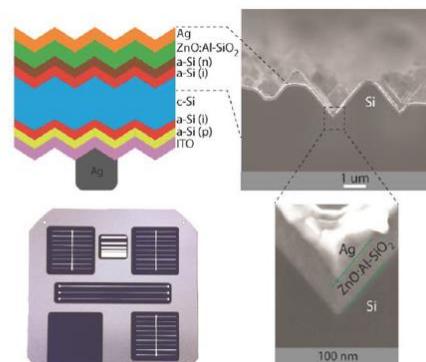
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After having seen the basic principles of sputtering and details on the film growth, let's now present a couple of relevant examples where sputtered films are used in MEMs. At the end of this lesson I will also show some details of the sputtering setup and take you into the clean room to see the real tools at work.

- Goal

- To decrease ohmic losses between absorbing medium (silicon) and metallic electrode (silver) in PV solar cells
- Antireflection coating at the front of the device
- IR light management at the rear of the device



Dabiran A. et al., "Tuning the Optoelectronic Properties of ZnO:Al by Addition of Silica for Light Trapping in High-Efficiency Crystalline Si Solar Cells", *Adv. Mater. Interfaces*, 2016.
<http://onlinelibrary.wiley.com/doi/10.1002/admi.201500462/abstract>
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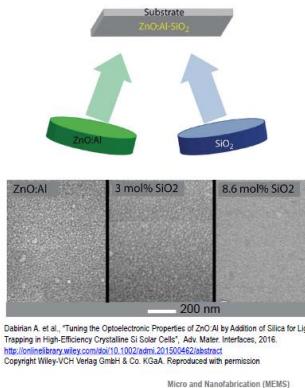
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At first, application where sputtering is advantageous is the fabrication of transparent conductive oxide films for photovoltaic solar cells (PV).

- Fabrication
 - Co-sputtering of ZnO:Al and SiO₂
 - Controlled ZnO:Al/SiO₂ ratio
 - Background pressure: 2e-7 mbar = 1.5e-7 Torr
 - Deposition pressure: 1-3 μbar = 0.75-2.25 mTorr
 - Gas flow: 20 sccm Ar, 1.4 sccm 95%Ar-5%O₂

- Results

- High transparency
- Controlled low refractive index
- 20% increase in efficiency at $\lambda > 1050$ nm (IR)



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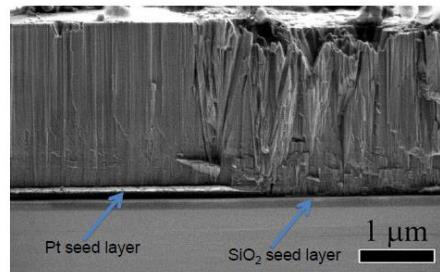
A photovoltaic solar cell is a device which transforms light into an electrical current. In most common solar cells, the absorbing material is made of crystalline silicon contacted with metallic electrodes. Incoming photons are absorbed in the crystalline silicon layer and generate electron-hole pairs. These electron-hole pairs are then extracted through the electrodes. Although a simple cell made of silicon directly contacted with metallic electrodes could work, its efficiency would be very low because of ohmic losses in the silicon metal junction and because of the surface recombination of electron-hole pairs. To improve the efficiency of crystalline silicon solar cells, amorphous silicon or alpha silicon and transparent conductive oxide so-called TCO are added in between the active crystalline silicon area and the metallic electrodes, in silver. As shown here in the right side of the slide.

- Goal

- Ultrasound transducer
- Mass sensors
- Bulk acoustic wave filters

- Fabrication

- DC magnetron reactive sputtering of AlN (1.2 μm)
- Al target and 50 sccm N₂ gas flow
- Deposition pressure: 2.1 mTorr
- Deposition rate: 60 nm/min
- Crystallinity is highly dependent on seed layer



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In this specific example, two different TCO are considered. First, the indium tin oxide or ITO is added at the front side of the device where the light comes in. And the second a zinc oxide aluminum silicon dioxide alloy, shown here, is added at the rear of the device. The first call of the TCO in the photovoltaic solar cells

is to decrease ohmic losses between the electrode and the absorbing medium. However, TCO also functions as anti-reflection coatings at the front of the solar cell, as well as for infrared light absorption management at the rear of the cells. In order to fabricate cells with the highest efficiency as possible, TCO layers must have low resistivity, high transparency, and a low refractive index. To satisfy all these three requirements at the same time it is not that straightforward by using standard thin film materials. One way to succeed to match all of these properties is, for instance, to add SiO₂ to zinc oxide aluminum TCO layer On the right side of the slide, we can see a TCO layer made of zinc oxide aluminum SiO₂ in between the silicon absorbing medium and the silver rear electrode. Like shown here.

Silicon, the TCO and the silver layer This sputtered composite layer allowed for tuning the optoelectronic properties

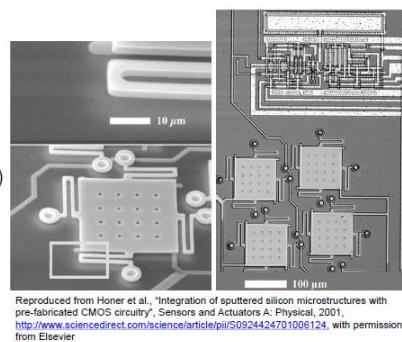
and for improving the PV efficiency. Let's see in the next slide how this film is actually made. To deposit a zinc oxide aluminum SiO₂ layer cool sputtering of zinc oxide aluminum and SiO₂ is performed. As shown here, two targets are used within the same vacuum deposition chamber. Tuning the voltage on each target

- Goal

- Silicon surface micromachined MEMS
- CMOS compatible
- Organic sacrificial layer compatible

- Fabrication

- Sputtering of Si (2 μm)
- Pressure and power tuning to control stress (<100 MPa)
- 350 °C annealing
- Background pressure: 1e-7 Torr
- Deposition pressure: 8 to 14 mTorr
- Deposition rate: 19-37 nm/min



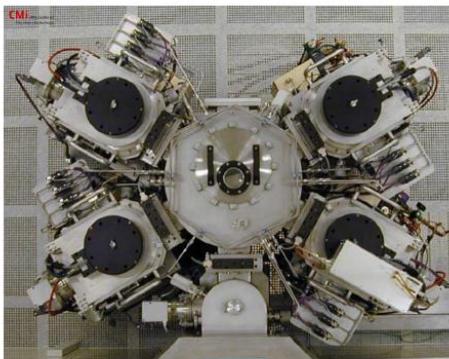
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enables to change the zinc oxide aluminum SiO₂ ratio into film. Formed here on the substrate. And thereby to adjust the film microstructure and refractive index. The more SiO₂ we add, the less crystalline becomes the material and the lower is the refractive index. In this concrete example, sputtering enables the deposition of two compounds at the same time and thereby tuning the final stoichiometry of the deposited film. Such a performance is impossible to achieve with thermal evaporation. The fabricated films exhibit high transparency and low refractive index. Three different coatings are shown here. First, on the left, the zinc oxide aluminum film without addition of SiO₂. And then with increasing SiO₂ concentration.

It shows that the texture is changing towards less grainy morphology. At the same time, the solar cell efficiency increases by 20% in the infrared when using the zinc oxide aluminum SiO₂ TCO layer at the rear of the device, instead of a standard zinc oxide aluminum layer. For further details please have a look at this cited paper. Our second thin film example of interest is based on piezoelectric materials, that are often deposited by reactive sputtering. Piezoelectric materials are very important and used in many MEMS devices such as ultrasound transducers, that means these devices convert a pressure wave into an electrical signal. Or mass sensors, where the mass change induces a resonance frequency shift. And bulk acoustic wave filters. For this latter application, suspended piezoelectric microstructures are sandwiched between electrodes. When an incoming electrical signal which matches the mechanical resonance frequency of one of the microstructures is applied to the input electrodes, the device enters into a mechanical resonance and an electrical signal is transmitted to the output electrode. Typically, bulk acoustic wave filters are made of aluminum nitrate; because of the excellent electroacoustic properties of this material and its chemical compatibility with micro-fabrication processes. The quality of the filter is determined by the piezoelectric film crystal structure. Reactive sputtering with an aluminum target in a nitrogen atmosphere is used to deposit the aluminum nitrate film. As it is the only deposition method which allows for high film quality below 500° C. However, the film crystal structure is highly dependent on the underlying seed layer. Film growth structure and stresses are explained in details in the film growth lesson. In the case of bulk acoustic wave-filters this underlying seed layer consists either of the platinum bottom electrode. Shown here. Or of a silicon dioxide layer. Indeed, the platinum electrode is patterned and the wafer surface, prior to the aluminum nitrate deposition, is thus made of two different materials, platinum and SiO₂. As you can see here on the right, the aluminum nitrate deposited on top of platinum, has a well-defined crystalline structure, compared to the aluminum nitrate that grows on top of the SiO₂

which is less uniform. In addition, the residual stress of aluminum nitrate grown on platinum seed layer

is also lower in the order of 200 MPa, tensile stress, versus minus 700 MPa, compressive stress, respectively on the SiO₂. So the challenge here is to optimize crystallinity of the overall film



● Pfeiffer Spider 600

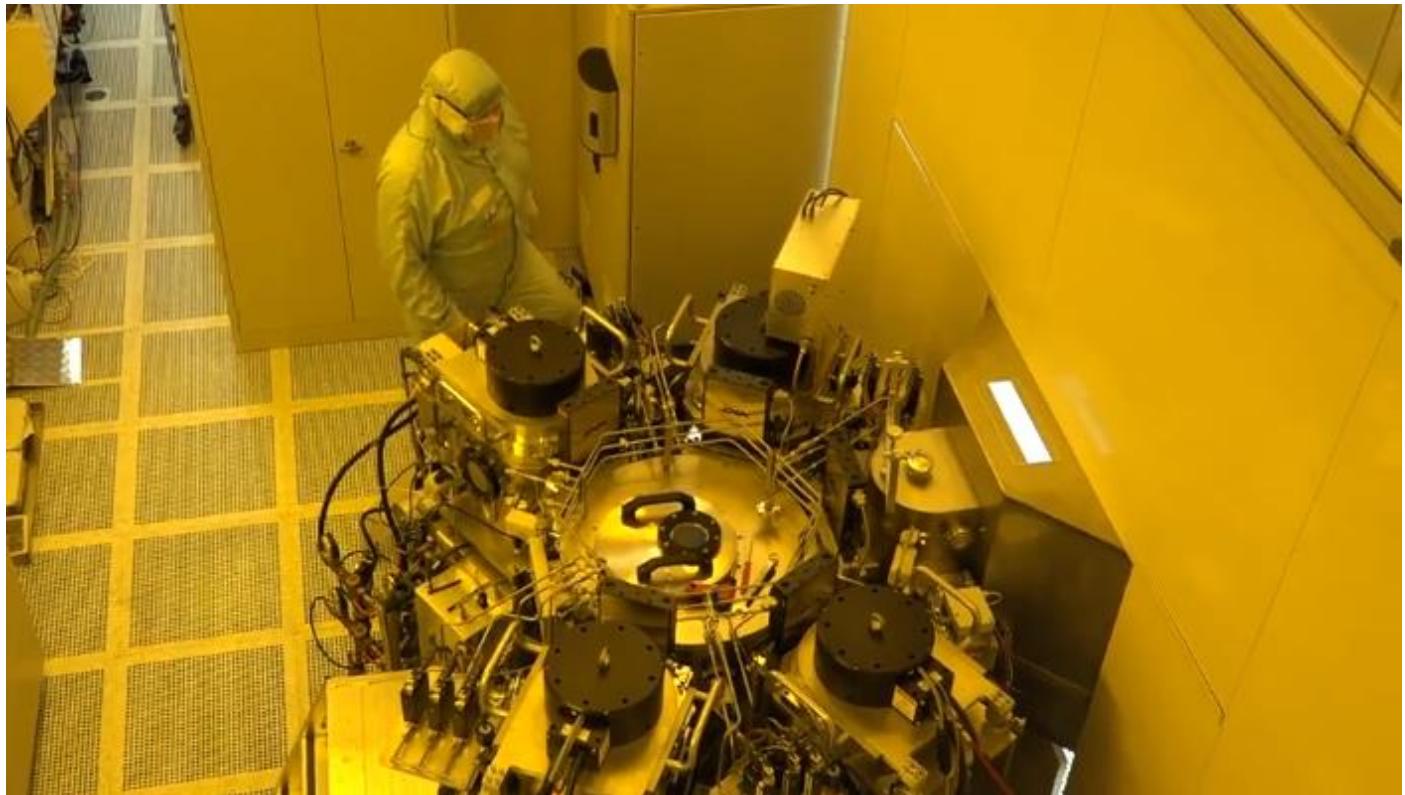
- Sputter cluster system (25 wafers)
- 2 x DC Magnetron: Al, AlSi, Mo, Nb, Pt, Ru, Si, Ta, Ti, W
- 1x pulsed DC Magnetron: Al, AlSc
- 1 x RF Magnetron: Al₂O₃, GeO₂, ITO, MgO, Ru, SiO₂, Ta₂O₅, Ti, TiO₂, V₂O₅
- 1 x RF-etch for cleaning
- 4 and 6 inches wafers
- Deposition from RT to 350[°C] (heaters)
- Turbomolecular pump to reach high vacuum of 10⁻⁶ to 10⁻⁷ [Torr]
- Deposition pressure is around 3 [mTorr]
- Reactive sputtering in O₂ atmosphere

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in order to acquire the best piezoelectric properties as possible. Here is one further example which illustrates how sputtering enables the manufacturing of MEMs. In this case, we are depositing a silicon thin film by sputtering and followed by lithography and etching. Many suspended microstructures are made of low-pressure chemical vapor deposition (LPCVD) polysilicon. Because of the well-characterized mechanical properties of polysilicon and because of the residual stress in thin films deposited by LPCVD can be tuned. However, the LPCVD process requires temperatures higher than 600° C. And is thus not CMOS-compatible. Building the MEMs device directly on top of a CMOS circuitry to control a MEMs device, however, would increase the device performance as well as its functionality. Indeed, having signal amplification close to the signal source allows decrease in the noise, and on-chip multiplexers enable the dense integration of a large number of devices. We thus look for a low temperature, silicon deposition technique, and use sputtering instead of CVD. Tuning the pressure and power of the sputtering process, and performing a post-annealing at 350° C, allows depositing up to 2 μm thick silicon films with residual stresses lower than 100 MPa. In addition to be CMOS-compatible, such a process can also be performed on a polymeric or organic sacrificial layer. As a result, suspended silicon structures can be fabricated on top of CMOS circuitry using a dry relief process in oxygen plasma to remove the sacrificial layer. This process is much simpler than the usual SiO₂ sacrificial layer using HF, wet release, and critical point drying process. An example of a sputtered silicon microstructure suspended with 4 springs next to its CMOS circuitry is shown here. The silicon plates, shown here in the magnification, is electrostatically actuated and its deflection is quantified measuring the change of capacitance with a dedicated on-chip CMOS amplifier. Like, shown here. And like it is nowadays integrated in many state of the art commercial MEMs. Here is an example of a cluster sputtering tool from our clean room. A load-lock system. Here. Enables to load the wafers into the tool, without venting the deposition chambers themselves. This way pumping time is shorter and there is less contamination of the deposition chambers with gaseous atmospheric components. A robotic arm, located in the central chamber, automatically moves the wafer from load-lock, here, into one of the 4 deposition chambers. Shown here. Each chamber has a different target of material, which enables serial deposition of multiple materials without venting the sample in between each deposition. This is an advantage when the deposited material are very sensitive to native oxides, for instance. To conclude this chapter about sputtering, let's now have a look how such a system really works in reality. So let's come together in the clean room.

Sputtering in CMi



The sputtering system that you see here is called a cluster sputtering tool. In this case with four deposition chambers allowing to pass wafers to various sputtering chambers without breaking the vacuum. Per sputter process step, only one wafer is used per chamber in this particular equipment. Wafers are loaded in the load lock chamber of the system from behind the wall on the right side of the image. Then a robotic arm located in the centre of the tool transfers the wafers from the load lock into one of the 4 sputtering chambers. The robotic arm enters into the load lock, moves up to lift the wafer from the chuck, leaves the load lock and distributes the wafer in the desired sputtering chamber. Let's now have a further look at the inside of the tool and see how the clean room engineer changes the sputter target. Remember the target is a plate made of the material that we want to sputter deposit on our substrate. In that specific case, the target which is changed, is used for RF magnetron sputtering. You can see the RF generator the grey metallic box and the magnet, the black cylinders. The other 3 chambers are DC magneton sputtering with only the magnet and no RF generator. The first step when changing the target is to remove the target shield. This shield is used to avoid sputtering of the structural elements of the cathode and to improve gas diffusion. Then the target itself can be removed. The home made tool is used to remove the target in order to allow a single person to perform this manipulation. In this specific case, the target is made of titania.

It is changed not because it is worn out, but because we need to sputter another material in this particular chamber. We can also see that a copper grid is used at the back of the target to ensure a good electrical contact. When a sputter target is worn out it also needs to be changed. This operation is shown here which also shows nicely how a sputter target in magnetron sputtering looks after some use. The wear, clearly is not uniform, because of the magnetic field which concentrates ions along magnetic field lines so that they optimise the sputter yield. In comparison, here are shown new sputter targets where the surface is still uniform. The two examples shown in the Section are aluminum oxide and silicon dioxide new targets. To mount a target in the tool the operation steps shown in this Section sequence are performed in the exact reverse order.

Supplementary

PVD 7: Other techniques Ion plating, MBE, PLD, ...

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Welcome to this lesson on other PVD techniques that are of interest for micro/nanofabrication. I will first show the so-called ion assisted methods, which are combination of evaporation and ion induced surface preparation. Second, I will introduce MBE which is an important technique to create crystalline thin films.

- Ion plating
- Molecular beam epitaxy
- Pulsed laser deposition
- Supplementary methods
- PVD methods comparison

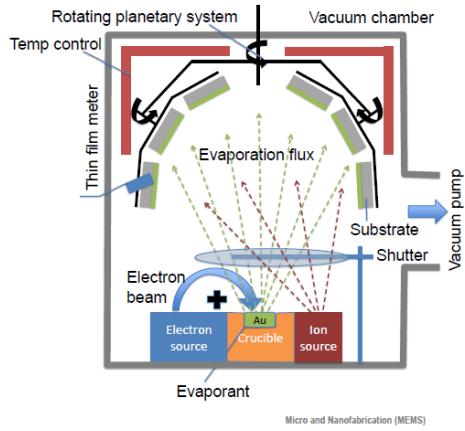
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Third, I will present PLD, which is a further method to deposit composite material with complex stoichiometry at high quality. These methods are more complex and expensive than the previously shown evaporation and sputtering but they are very important for advanced film control and formation. This lesson will conclude with some supplementary methods and the comparison of the various PVD methods shown.

Evaporation
 +
Substrate sputtering with ions

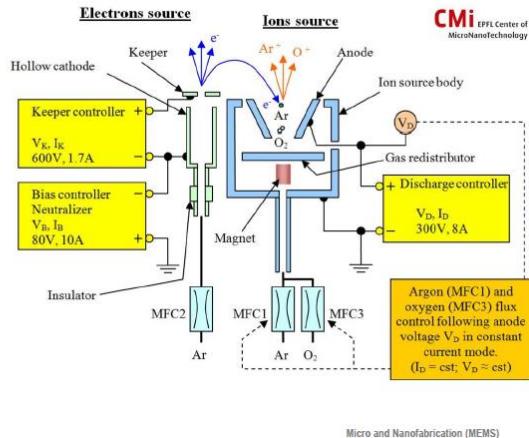
- Used prior to deposition for:
 - Substrate cleaning
 - Substrate activation
- Used during deposition for:
 - Improved film thickness uniformity
 - Improved film adhesion
 - Dense and hard films



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Ion assisted deposition (IAD), and ion beam assisted deposition (IBAD), are 2 techniques combining material evaporation and substrate sputtering with ions. They differ in how the ions are created. In the case of IBAD, ions are generated using an ion source or ion gun as shown in the schematics on the right side of the slide. So here you can see the setup that we already introduced in the evaporation. Now, in addition to the crucible and the electron source that evaporates the material that is going to be deposited on the substrate in the chamber. We have, in addition, an ion source or ion gun, which emits ions into the vacuum chamber that heats the substrate before or during the deposition. In such we can clean the surface, and add additional energy, to enhance the control of the film growth on the wafer during the deposition. In the case of IAD, a plasma is created in the evaporation chamber and ions are accelerated

- Ion source
 - Hollow cathode to create electrons
 - Magnetic field to deflect electrons
 - Positive anode to accelerate ions
- Advantages of IBAD
 - Films with higher purity
 - Good internal stress and microstructure control
- Advantages of IAD
 - Compounds deposition
 - Conformal coatings
- IAD and IBAD are also possible with sputtering deposition and CVD



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by applying a negative bias voltage on the substrate. In both cases, the high energy ion bombardment of the substrate is used to clean and activate the surface prior to the deposition and to improve the film quality during the deposition. By doing so, thickness uniformity, as well as film adhesion can be improved. In fact, energetic ions enable atoms to diffuse on the surface and also enable atoms to penetrate

into the surface. By this mechanism, film density and hardness can be increased, which is particularly useful when depositing dielectric films. As we know, denser films have lower etch-rates and higher dielectric constant. Let's now have a look at how a typical ion source for IBAD works. You can see on the right side of the slide a schematic of a source used in one of the evaporator in the EBF clean room.

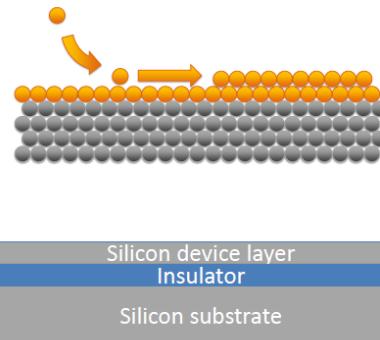
The substrate is not shown, it will be somewhere on the top of the slide. The source consists of two parts, the hollow cathode electrode source, and the ion source itself. Firstly, argon gas enters the hollow cathode

and a high voltage is applied between the keeper and the hollow cathode, creating a plasma within the hollow cathode. Shown here. Once the plasma is stable in the hollow cathode, a bias voltage is applied with a bias controller to emit electrons out of the hollow cathode. Emitted electrons are deflected towards the ion source using a magnetic field. Shown here. In the ion source electrons collide with gas atoms, here we use argon or oxygen, and ionize them. Resulting ions are then repulsed by the positive anode and bombard the substrate. Upwards. Which is not shown here. Electrons emitted from the hollow cathode are also used to neutralize the substrate, which charges positively with ion bombardment. Ion beam assisted deposition has 2 main advantages over non-beam ion assisted deposition. Both come from the fact that no plasma is used in the actual deposition process in contrast to sputtering. Firstly, better film purity is achieved as a higher vacuum can be used. Thin films, with improved internal stress and microstructure control, can be deposited as substrate temperature can be better controlled. As there is no plasma close to the substrate. On the other hand, non-ion beam deposition also has some advantages over the beam assisted deposition.

Epitaxy: deposition of a single-crystal overlayer on a crystalline substrate

- Epitaxy conditions
 - Homo- vs heteroepitaxy
 - Crystal structures match
 - Atoms energy and diffusion time

- Epitaxy main uses
 - Si membranes on Si
 - Abrupt doping level change
 - Silicon on insulator wafers



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As evaporated atoms travel through the plasma, they will be scattered and some of them will ionize.

As a result, conformal coatings and compound deposition can be achieved. For compound deposition, an additional gas is added to the chamber and it will react with evaporated atoms that will have been ionized in the plasma. For instance, dense and very hard titanium nitrate coatings are thereby possible. Finally,

IAD and IBAD can be combined with sputtering deposition as well as chemical vapor deposition. Let's have now a look at epitaxy which is a method to create crystalline material films that are not possible with evaporation and sputtering processes. Indeed, in evaporation and sputtering PVD the deposited layers are

- Evaporation from a Knudsen cell

$$Kn = \frac{\lambda}{D} > 1$$

Kn = Knudsen number
 λ = mean free path in [m]
 D = cell orifice diameter in [m]

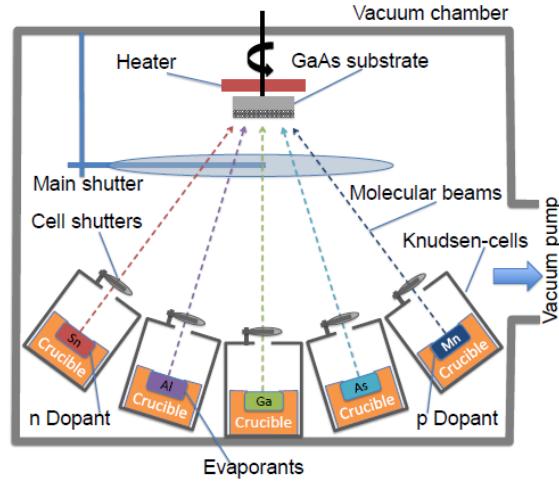
- Molecular flow

- Ultrahigh vacuum: 10^{-11} [Torr]

- Line-of-sight deposition

- Multiple cells

- Alloys and compounds deposition

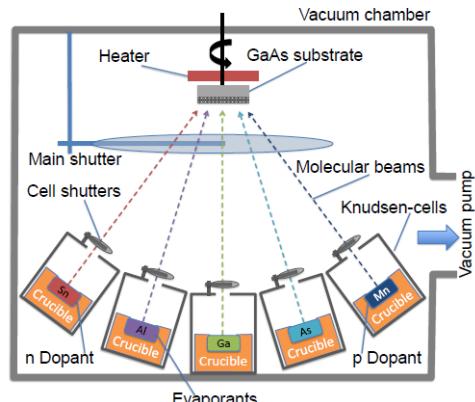


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either amorphous or sometimes polycrystalline, but never monocrystalline. The crystal structure of deposited thin films will be studied in more detail in the chapter about film growth. Epitaxial deposition consists in growing a single crystal film on the crystalline substrate, as shown in the top schematic on the right side of the slide. If the film is of the same material as the substrate, the process is called "homoepitaxy". It is called "heteroepitaxy" if the materials differ. In order to have a successful growth of the epitaxial layer, several conditions have to be satisfied. In a general way, the epitaxial layer crystal structure is the same as the substrate crystal structure. In the case of homoepitaxy, this is rather straightforward. On the other hand, in the case of heteroepitaxy, things are more complex. Indeed,

- Atoms needs enough energy and time to diffuse to the right location
 - Substrate must be absolutely clean
 - Substrate is heated to 400-800 °C
 - Rate is very slow: 0.1-2 Å/s
 - Rates depends on crystal orientation
 - Lattice mismatch limits epitaxial layer thickness
- Slow rate and shutters allow precise and accurate thickness control



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if there is a lattice mismatch between the material to grow and the substrate, the single-crystal film thickness will be limited or even zero. In addition to the crystal structure condition, there is also a condition on the energy and diffusion time atoms have when they arrive on the substrate. If they are too low or too short, respectively atoms will not be able to go to the right location in order to grow a single crystal. There are several main applications of epitaxy, such as the fabrication of silicon membranes

Lower temperature than CVD epitaxy

Compatible with doped substrates

Better thickness control than CVD epitaxy

Quantum wells fabrication

Laser diodes fabrication (CD, laser-pointer, ...)

More expensive than usual PVD system

Deposition rate is slow

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on silicon substrate with predetermined thicknesses and doping levels. And stacks of silicon layers with sharp and large doping level changes. Such stacks can be used in microprocessors, high-performance logic circuits, and as electrochemical etch stop for MEMs fabrication. More details are given about this last application in the chapter about wet-etching. Another widely used application of epitaxy is silicon-on-insulator wafers or SOI. SOI wafers consist of a thin surface or device layer of silicon an underlying layer of insulating material typically SiO₂ or aluminum oxide and a support silicon wafer as shown in the bottom schematic on the right side of the slide. Such wafers can be used to fabricate faster and more compact transistor chips in the thin epitaxial device layer. It can also be used to fabricate mechanically and electrically insulated layers in MEMs devices Two main types of epitaxy exists: Chemical vapor deposition and physical vapor deposition In this chapter we will focus on the latter one, also called "Molecular Beam Epitaxy", or MBE. Molecular beam epitaxy, or MBE, is a PVD technique very similar to resistive heating evaporation, but with significant technical differences. Firstly, the crucible containing the evaporant is placed in a cavity with a very small aperture in the millimeter-side range called Knudsen cell as you can see on the figure on the right side of the slide. Typically, graphite crucible with tantalum foil, resistive heatings are used here. The use of a Knudsen cell allows to better control both the temperature of the evaporant and the flow of atoms exiting the cell. The flow of atoms is characterized by the Knudsen number, which is defined as the ratio of the atoms mean free path over the Knudsen cell orifice diameter.

High energy UV excimer laser pulse ablates material from target forming high temperature vapor plume incident on sample

- Laser-target interactions:

1. Short laser pulse: 10-30 [ns], 15 [pulses/s]
2. Absorption at the target surface: ~10 [nm]
3. Energy relaxation to the lattice through electrons-phonons interactions: 1-10 [ps]
4. Heat diffusion, melting (tens of ns) and evaporation of a small amount of material
5. Plasma creation
6. Interactions of target and ablated species with plasma
7. Cooling and resolidification between pulses

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Shown here. If the Knudsen number is smaller than 0.01 the mean free path is comparable to the orifice diameter. This means that atoms bounce against the orifice sidewalls. In such a case, atoms exit the cell in a continuous viscous flow. In the case of MBE, the mean free path is in the range of ten-to-the-sixth meters, and the orifice diameter in the range of 10 to the -3 meter. As a result,

the Knudsen number is much greater than 1 and atoms are passing through the orifice one by one in a single, straight track. Secondly, MBE requires an ultrahigh vacuum of about 10 to the -11 Torr. in contrast to a vacuum of 10 to the -6, 10 to the -7 used in standard evaporation. As a result, atomic stream evaporated from Knudsen cells in MBE, impinged on the substrate surface in a line-of-sight manner, and then diffuse to their thermodynamically minimal crystallographic location. Finally, as shown in the schematic on the right side of the slide multiple Knudsen cells can be used with the same MBE chamber, which allows depositing compounds, alloys, and even multiple types of dopants. In addition to the main shutter, that covers all the cells, each cell has its own shutter. This way, stacks of different material with various different doping levels can be deposited.

High energy UV excimer laser pulse ablates material from target forming high temperature vapor plume incident on sample

- Deposition at room temperature
 - Deposited film is amorphous
- Substrate heating: 700-900 [°C]
 - Deposited film is crystalline
 - Heater in substrate holder
 - Heating with CO₂ laser

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In order to grow a single crystal film, having molecular flow of atoms impinging the substrate is not sufficient. As mentioned in the introduction slide about epitaxy, once the atoms land on the surface they need to move around until they find an atomic site to chemically bind to it. To do so, atoms on the surface must have enough energy and time to reach the right crystallographic location. Several conditions have then to be satisfied. Firstly, the substrate has to be absolutely clean. Secondly, the substrate is heated from 400° C up to 800° C, to increase the atoms energy. And thirdly, giving atoms enough time to travel to their energy minimum location leads to very low deposition rates in the range of 0.1 to 2 ångström (Å) per second. Which results in very long deposition times. Finally, in the case of heteroepitaxy, if the lattice from the material to grow is different from that of the substrate epitaxy might still be possible, but the thickness of the thin crystal film will be limited. Indeed, the film will strain in order to match the substrate lattice and at some point internal stresses will become too important and dislocations will appear. Such a slow deposition rate and fast acting shutters to control the atomic stream allows very precise and accurate thickness control for each material. Ultra-sharp doping profiles and layers with a thickness precision of +/- 2 Å can be achieved routinely. So in comparison to other PVD techniques epitaxy allows for better thickness control and enables the deposition of single crystal layers. And in addition, in comparison to chemical vapor deposition epitaxy molecular beam epitaxy requires lower temperature 400° to 800° C versus 1200° C. And allows better thickness control. Working at lower temperatures enables to work with doped substrates and to deposite doped films without auto-doping and diffusion problems. Better thickness control allows for fabricating quantum wells where layer control of 40 +/- 2 Å is required. Finally, both low temperature and precise thickness control are required to fabricate semi-conductor lasers, such as laser diodes. They are made of a stack of different materials with very specific doping levels and they are widely used for CD, DVD, BluRay Discs, reading and recording, as well as pen-sized laser pointers. On the other hand, MBE is more expensive than other PVD systems because of the required ultrahigh vacuum and because the deposition rate is very slow. It is used only for applications where no other technique can be used. Pulse laser deposition (PLD) consists in using a high-energy UV excimer laser to ablate material from a target. The physical ablation forms a high-temperature vapor plume that reaches the sample surface. We will see that the main advantage of

such a system is its ability to deposit compounds with very complex stoichiometry. The working principle of PLD is as follows: First, a high-energy UV excimer laser pulse is focused on a target made of the material, to deposit. Shown here. The laser is focusing on the target in green. Typically, a krypton fluoride laser, at 2.48 nanometer is used and pulses of 10 to 30 nanoseconds with an energy in the focus of 2 Joules per centimeter square. Pulse repetition is in the order of 15 per second. The energy of the pulse is absorbed by the target a plasma plume is created at the surface of the target and it interacts with ablated pieces and the target itself. Finally, the vaporized material rapidly expands and condenses on the substrate. In between pulses, the target cools down and solidifies. For metal, the absorption depth is about 10 nanometer. The energy is further relaxed through electron phonon interactions in a phenomena which takes 1 to 10 picoseconds time. Concretely, the electrons are removed from the atoms and oscillate in the strong magnetic field, created by the laser. The generated heat diffuses around due to collisions of these free electrons with other atoms. In the first time, this melts the material. And finally, a small amount of material is evaporated and ionized PLD deposition at room temperature usually results in amorphous thin films. However, heating the substrate to 700° to 900° C, allows to get crystalline thin films. Substrate heating can be achieved in two ways. One conventional way is to use a substrate holder with an integrated heater. Another way is to use a CO₂ laser which is focused on the substrate. Pulse laser deposition has several advantages that make it an attractive PVD technique.

- Large deposition pressure range
- Many materials on many substrates
- Target stoichiometry conservation
- Superconducting materials: $\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$
- Hydroxylapatite biocompatible coating: $\text{Ca}_{10}(\text{PO}_4)_6(\text{OH})_2$
- Risk of splashing
- Poor step coverage
- Not well suited for large scale

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Firstly, the deposition pressure range varies from atmospheric pressure to high vacuum. Secondly, it is almost possible to deposit any material on any substrate and there is no X-ray generation as it is the case with sputtering. Finally, the most important strength of PLD is that the target material is deposited onto the substrate with almost no decomposition. A stoichiometry is conserved complex compounds and alloys can be deposited. This makes PLD a unique technique to deposit, for instance, functional oxides, such as super conducting materials or bio-compatible based ceramics to protect sensors from body fluid.

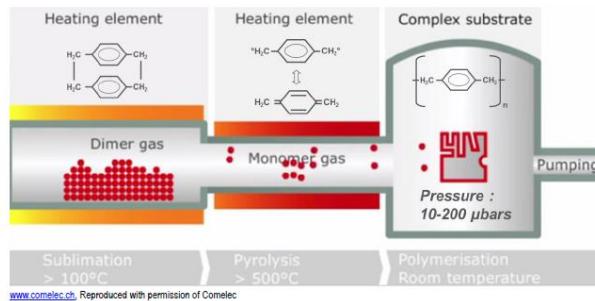
On the other hand, PLD also has some severe limitations. Firstly, there is a risk of splashing, because of surface boiling or shockwaves due to the plasma plume expansion. Boiling occurs when the layer below the surface of the target reaches its evaporation point before the surface of the target itself. As a result, micrometer particles are injected and impinged to substrate surface. This problem can be partially solved

using ultra-short laser pulses of less than 1 picosecond. A such pulse with a shorter than the electron lattice relaxation time, the heat diffusion and melting is reduced and the material is forced directly into plasma state without going into liquid phase first. This leads to cleaner, smoother and higher quality films.

Secondly, PLD is a line-of-sight technique, and results in poor step coverage which means on the positive side that it can be used for lift off and shadowmask techniques. Finally, because of the small source size

this technique is not suited for large scale deposition. Call for new equipment is being developed for this purpose. To conclude this chapter, I briefly want to introduce one important and recently very prevailing coating material for MEMS, which is parylene. It is widely used in microfabrication

- Structural material
 - 50 nm to 10 μm thick layers
- Protective coating:
 - chemically resistant, conformal
- Thermal insulator
- Thermally stable
- Biocompatible



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as structural material, thick protective coating and thermal insulator. Deposition process consists of 3 subsequent steps. During the first step, a solid parylene diamond is evaporated in a chamber at 150°C .

Then, in a second chamber, the temperature is further increased up to 670°C , in order to separate the dimers into monomers. And finally, in the third chamber, the monomer gas is cooled at room temperature

so that it condenses on the substrate and polymerizes. Layer thicknesses ranging from 50 [nm] to 10 μm double side coating, as well as conformal and stress-free layer are possible. In addition, parylene shows excellent thickness uniformity below 1%. Is thermally stable. Has a good resistance to solvents, acids, and bases. Last but not least, it is biocompatible, which makes it an ideal candidate for packaging application for bioMEMS. This table summarizes the key features of the main PVD techniques introduced so far. It allows to compare the various parameters and to select the proper method for one's own use. Please have a look at the variations

	Evaporation		Sputtering			IAD / IBAD	MBE	PLD
	Resistive	E-beam	DC	RF	Magnetron			
Rate [\AA/s]	0.1 - 20	10 - 100	1 - 100	1 - 100	1 - 200	0.1 - 200	0.1 - 10	1 - 10
Thickness range [nm]	10 - 2000	10 - 2000	10 - 6000	10 - 6000	10 - 6000	10 - 6000	0.4 - 1000	0.1 - 1000
Material	Metals	Metals, oxides	Metals, alloys	Metals, alloys, dielectrics, compounds	Metals, alloys, dielectrics, compounds	Metals, alloys, dielectrics, compounds	Si, Ga, Al, As, In, P, Sb, Mn, ...	All materials + complex compounds
Purity	+	++	--	--	-	-- / -	+++	+
Step coverage	-	-	+	+	+	+ + / +	++	--
Adhesion	-	-	+	+	+	+ +	+ + +	+
Large area uniformity	-	-	+	+	+	+ +	+ + +	--
Pressure [Torr]	$10^{-6} - 10^{-7}$	$10^{-6} - 10^{-7}$	$10^{-1} - 10^{-2}$	$10^{-1} - 10^{-2}$	10^{-3}	$10^{-1} - 10^{-2}$	10^{-11}	$750 - 10^{-9}$
Substrate temp. [$^\circ\text{C}$]	20 - 400	20 - 400	20 - 400	20 - 400	20 - 400	20 - 400	400 - 800	20 - 900
Other	Lift-off	Lift-off	Substrate cleaning & activation	Substrate cleaning & activation	Substrate cleaning & activation	Cleaning & activation, densification	Single-crystal, expensive	

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in parameters and try to get an overview of the pros and cons of each of the methods. We have looked at the wide range of different PVD methods, such as thermal evaporation sputtering, ion plating, molecular beam epitaxy and pulse laser deposition. The underlying physical principles have been explained. So you should now be able to distinguish the various methods and to eventually choose the proper one for your

purpose. In an upcoming video lecture, we will analyze more in details how PVD films grow onto the substrates.

SUPPLEMENTARY Practice quiz other techniques: ion plating, MBE, PLD, ...

Questions:

1. Which of the following propositions about ion assisted deposition (IAD) and ion beam assisted deposition (IBAD) are correct?

- The IAD technique cannot be used prior to deposition for substrate cleaning
- The IBAD technique cannot be used during deposition for improving film adhesion
- The IBAD technique can be used during deposition for improving film thickness uniformity
- The IBAD technique generates ions in the evaporation chamber

2. In order to deposit a monocrystalline film by molecular beam epitaxy (MBE), you should...

- Keep the chamber pressure between 10^{-6} to 10^{-7} Torr to prevent ultra-high vacuum
- Clean the substrate prior to the deposition to prevent any dust particle or organic contamination
- Heat the substrate to 400°C-800°C to increase the atoms' energy
- Limit the deposition rate

3. Which of the following propositions about Parylene coating are correct?

- Parylene is a polymer which is widely used in microfabrication, but its chemical stability is weak
- Parylene coating technique can be used to realize double-side, conformal, stress-free coating layers
- In general, solid Parylene dimer is heated at 150°C and then cooled down to form a coating layer
- Similar to other polymeric deposition techniques, thickness control is difficult with Parylene coating

PVD 8: Film growth

I. Atoms arrival and adhesion

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This lesson on the growth of thin films in physical vapor deposition presents the basic parameters that influence the morphology of the added material on the substrate.

- Atoms arrival
- Film-substrate interface
- Adhesion
- Growth modes
- Crystal structure
- Stress in thin films

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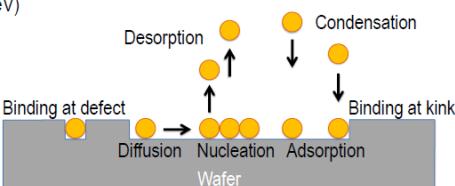
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I will start by describing what happens when the atoms arrive on the surface. An important factor here is the interface property which determines the adhesion of the added film as well as the way the film actually grows. I will then show how the various growth modes influence, on their turn, the crystal structure of the film, and I will conclude with some remarks on the mechanical stresses in the thin films. with some remarks on the mechanical stresses in the thin films. Thin film deposition and film growth depend on the materials involved as well as on several process parameters. These include the energy of the impinging atoms, their arrival rate and the substrate temperature. When atoms condensate on the substrate they are adsorbed and attached to the surface either by chemisorption or by physisorption. In the first case, atoms create chemical bonds on the surface with a bonding energy in the order of 1 electronvolt (eV). The available energy depends on impinging atoms energy as well as on the substrate temperature. On the other hand, physisorption occurs when there is a chemistry mismatch or when the energy is too low to create chemical bonds and which leaves the chemical species of the adsorbate and the surface intact. In other words, there is no chemical reaction occurring. Physisorbed atoms are weakly attached to the surface by Van Der Waals forces, with a

bonding energy in the order of 0.3 to 0.5 eV. As a result, physisorbed atoms can diffuse on the surface. And the diffusion of physisorbed atoms increases with the available energy but is inversely proportional to the atoms arrival rate. Why is that so? The explanation is as follows: if the arrival rate is high, atoms on the surface will rapidly collide with new arriving atoms. And this limits the diffusion and strongly influences the growth mode. Growth modes are detailed later in this chapter. Here on the figure you can see various events that can occur after the arrival of the atoms on the surface. As a result of the surface diffusion, physisorbed atoms will either bind at the kink - shown here, a small step - or at the defect. Shown here.

- Atoms adsorption on the surface
 - Chemisorption = chemical bond (≈ 1 eV)
 - Physisorption = van der Waals forces ($\approx 0.3\text{--}0.5$ eV)

- Once on the surface, atoms can:
 - Stay: when chemisorbed
 - Diffuse: when physisorbed
 - Desorb: when physisorbed and high energy

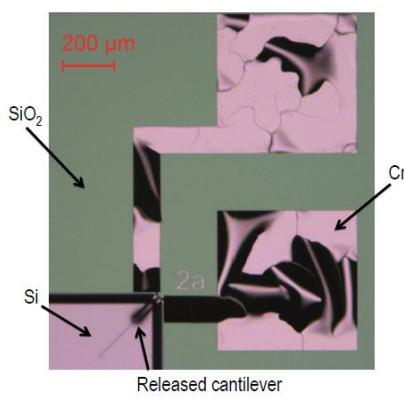


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Or nucleate with other atoms and form clusters. Nucleation is increased with available surface energy. Finally, if the atoms energy is high enough, they can also desorb again from the surface. The likelihood of desorption is lower for clustered atoms in comparison to single atoms. The adhesion of the added thin film to the substrate is a very important issue in microfabrication and special attention is therefore required. Particularly, substrate cleanliness is of a major significance as residues from the environment or from previous process steps will almost inevitably lead to poor adhesion. The thin film deposition process itself also plays a role if there is a strong or weak adhesion. For instance, in sputtering, highly energetic ions and atoms knock out surface contamination and loosely bound atoms. This enhances the adhesion a lot. Thus, sputtered films tend to have a better adhesion compared to films formed by evaporation. However, as explained in the previous slide sometimes it is not possible to grow a thin film of a desired material directly on the given substrate because of thermodynamics.

- Substrate cleanliness is primordial
- Process parameters affect adhesion
 - Sputtering is better than evaporation
- Noble metals adhesion is poor
 - Adhesion layer of a few nanometers



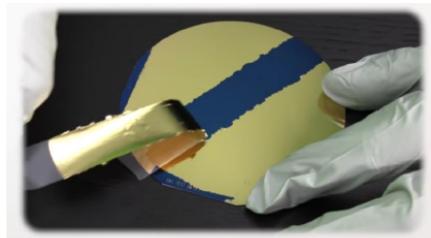
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Examples are the cases of noble metals, which are inert and do not react by nature. As a result, they do not adhere well to silicon or SiO₂. So, what do we do? To deposit noble metals, adhesion layers are therefore required. These adhesion layers, which are chosen according to their ability to make chemical bonds, consist of few nanometers-thick films deposited just before the noble metal, in the same vacuum chamber. This ensures that we have a clean interface and substrate. Two common pairs of adhesion noble materials in

micro and nano fabrication are titania and platinum as well as chrome and gold. Here is the example that shows the silicon substrate with the chrome adhesion layer, and then the deposited gold, that is now well adhering to the substrate. This photo here, on the right side, actually shows a failure process. A 500 nm thick chrome layer aimed as electrical conductor to drive current through a bimorph actuator has poor adhesion to the substrate, and is detached, or "delaminated" as we call it, from the substrate. You can see this in this optical microscope. This is either due to poor adhesion, and/or to high intrinsic stress, or both. This will eventually lead to the complete failure of the device and needs to be overcome. To test thin film adhesion, a first, straightforward test called the "tape pull test", can be performed.

- Substrate cleanliness is primordial
- Process parameters affect adhesion
 - Sputtering is better than evaporation
- Noble metals adhesion is poor
 - Adhesion layer of a few nanometers
- “Tape pull test” adhesion test



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A standard office tape is attached to the wafer and then pulled off. If the film peels off with the tape, then adhesion is not good enough, and the process or adhesion layer should be modified. In the second example, we added 10 nm chrome, between the silicone nitrate and the added 100 nm of gold film, and as you can see, now the gold film adheres very well, under the tape pull test. There are, of course, more sophisticated equipments that measure the adhesion of thin films, but for a first order information, this tape-test is very convenient.

Practice quiz film growth: atoms arrival and adhesion

Questions:

1. After depositing a thin film you realize that no film was formed on the substrate because the deposited atoms desorbed from the substrate surface. What could you do to overcome this problem? Think generic.

- Increase the substrate temperature
- Increase the sputtering rate
- Use evaporation instead of sputtering
- Use magnetron sputtering

2. After depositing a silver (Ag) layer by thermal evaporation on a glass wafer, you observe that the film delaminates. What could you do to solve this problem?

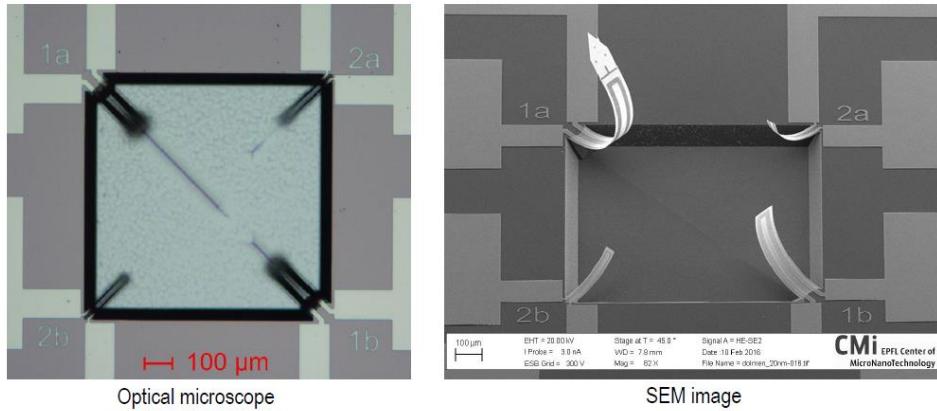
- Deposit a thin Cr layer prior to the silver deposition
- Use sputtering instead of evaporation
- Consider to adapt the cleaning procedure of the substrate before the evaporation
- Add an Au adhesion layer below the silver

PVD 8: Film growth II. Stress in thin films

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You will remember the case study of the bimorph actuator that we saw in one of the introduction lessons of this “MOOC”. After the KOH release of the beams, the cantilevers did not remain flat, but were bent upwards.



(see the lesson on the bimorph actuator example)

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This is due to residual stress in the thin films resulting from the different process steps. Let's now have a more extensive look at the different kinds of stress that exist in the thin films, and to their origin. As mentioned in the previous slide, the deposition method and the process parameters influence the crystal structure of the thin film. In addition, they also influence the residual stress in the thin films. Stress in thin films can be divided in two categories: extrinsic stress and intrinsic stress.

- Extrinsic stress = f(expansion coefficients mismatch)

σ_f = stress in film in [Pa], by convention negative stresses are compressive
 E_f = film Young's modulus in [Pa]
 v_f = Poisson ratio of the film
 α_f and α_s = film and substrate coefficients of thermal expansion (CTE) in [K⁻¹]
 ΔT = difference between deposition and working temperature in [K]

- Uniform stress over film thickness
- Most material used in microfabrication have higher CTE than silicon, except SiO₂, SiN and diamond

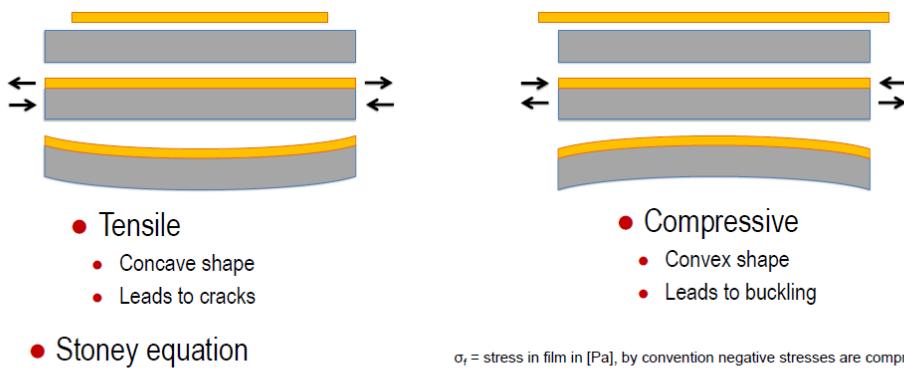
- Intrinsic stress = f(film microstructure, deposition method)

- Lattice mismatch
- Voids and incorporated foreign atoms
- Bombardment during deposition pinches off loosely attached atoms and reduces stress
- Stress gradient over film thickness

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Extrinsic stress results from a mismatch between the film and the substrate's coefficient of thermal expansion, CTE. If both the film and the substrate undergo the same temperature difference, a simple formula, shown here, describes the stress which is directly proportional to the difference between the two expansion coefficients and to the change in temperature. Such a situation occurs, for instance, during cooling after a CVD process. Indeed, during CVD, the film and the substrate are at the same elevated temperature.



• Stoney equation

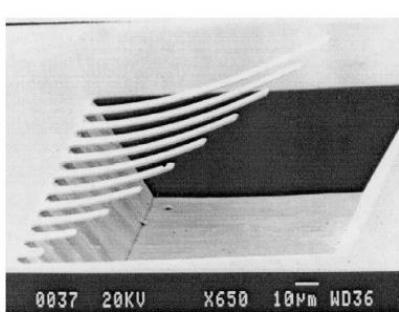
σ_f = stress in film in [Pa], by convention negative stresses are compressive
 E_s = substrate Young's modulus in [Pa]
 v_s = Poisson ratio of the substrate
 t_f and t_s = film and substrate thickness in [m]
 r_{sf} = radius of curvature of the substrate with the thin film in [m]
 r_s = radius of curvature of the substrate before deposition in [m]

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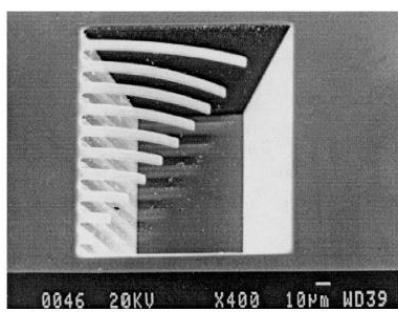
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By convention, a negative stress is compressive and generally extrinsic stresses are uniform over the film thickness. Finally, it is worth mentioning that most materials used in micro-fabrication have a higher CTE value than silicon except SiO₂, silicon nitrate, and diamond. On the other hand, intrinsic stress is less understood. There is no simple theory that allows computing them. Their understanding relies on empirical results. Intrinsic stress is closely related to the film material, and microstructure, as well as to the deposition method and parameters. For instance, a lattice mismatch between the film and the substrate, or the incorporation of voids and foreign atoms generate intrinsic stress. On the contrary, bombarding the substrate during the deposition pinches off loosely attached atoms which can reduce stress, and intrinsic stress is not uniform over the film thickness, which creates stress gradients. These gradients are inducing the bending of cantilevers, even if they are made of a single layer material. Intrinsic stress can be partially removed by means of an annealing step. The total stress in a thin film is equal to the sum of the extrinsic and the intrinsic stress. Usually films deposited by evaporation result in tensile stress. Stress in sputtered films depend on many parameters, such as bias power, argon pressure, sputtering gas mass, substrate temperature and deposition rate. As a guideline, sputtering at low pressure at about 1 millitorr usually results in compressive stress, while sputtering at higher pressure, 10 millitorr, usually results in tensile stress. Depositing sequential layers with tensile and compressive stress enables to perform stress compensation. Residual stress in thin films leads to substrate or device curvature. To qualitatively understand why, let's

consider the schematics on the top left corner of this slide. This is the case corresponding to an extrinsic tensile stress. If a thin film, here in yellow, is deposited by operation on a substrate, here in grey, at room temperature, for instance, the film, which is initially hot, shrinks more relatively to the substrate, which is cold. However, the lateral dimension of the substrate and of the thin film have to be the same. Therefore, the film is under tensile stress while the substrate is under compressive stress. Shown here, in this second line of the drawing. To satisfy the sum of the force's equilibrium, the tensile force in the film is equal to the compressive force in the substrate. However, the mechanical equilibrium is not satisfied yet because of the sum of the moment. Thus, the wafer and the film bend in a concave way, for the case of tensile thin films. Indeed, the film tends to retrieve its shorter, unstressed state. In the case of compressive thin films, in the top right corner, the same reasoning leads to convex bending of the film. It is worth to notice that if a wafer with a thin film was manually bent, a tensile stress in the thin film would occur in the case of a convex shape. It is the opposite, then, for residual stresses. Tensile stress in thin films leads to cracks while compressive stress leads to buckling. The well-known Stoney equation quantitatively relates the wafer curvature to the residual stresses in the thin film. By measuring the radius of curvature of the wafer before and after the film deposition and knowing the substrate and film thicknesses, it is possible to compute the average stress in the thin film. Here we see 2 SEM images showing 2 different cantilever arrays. In both cases, we have free-standing SiO₂ films, 1 to 1 μm thick grown by thermal oxidation at 1050°C. They are between 40 and 200 μm long. The bilayer microcantilevers were obtained after an additional titanium (left) and aluminum (right) that was deposited onto the SiO₂ cantilevers. The aluminum films with thicknesses ranging from 0.3 to 1.7 μm were deposited using thermal evaporation. In addition, the titanium films with thicknesses ranging from 0.1 to 0.3 μm were deposited using electron beam evaporation. The SEM images here show the bilayer microcantilever array and their respective bending due to intrinsic stress. In the case of titanium, it bends upwards, and in the case of aluminum it bends downwards. In both cases, we have SiO₂ as material plus the titanium. And here we have the SiO₂ plus the aluminum. So we can obtain different types of stresses in free-standing cantilevers, by playing with different material compositions. In this chapter we first saw that depending on the chemistry, the deposition method and the process parameters, atoms can either be chemisorbed or physisorbed at the wafer surface. Once arrived on the surface the atoms stay, move or desorb. Once the film starts to grow, an important parameter is the film substrate interface. Will the film adhere or not? To answer this question, thermodynamics allows computing interface stability and several types of different interfaces were shown in this lesson. We have seen that all the following factors influence the thin film adhesion: interface compatibility, substrate cleanliness and deposition method, as well as adhesion layers.



- Ti/SiO₂ cantilever
 - Bends upward
 - Ti = tensile
 - SiO₂ = compressive



- Al/SiO₂ cantilever
 - Bends downward
 - Al = compressive
 - SiO₂ = tensile

Wenlong Fang et al., "On the thermal expansion coefficients of thin films", Sensors and Actuators A: Physical, Volume 84, Issue 3, 1 September 2000, Pages 310–314 with permission from Elsevier.
<http://www.sciencedirect.com/science/article/pii/S0924424400000013>

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Film growth can be categorized into different modes, which are 2D, 3D and columnar modes. These modes, as well as the resulting film crystal structure are strongly dependent on the deposited material, the deposition method, as well as on the process parameters. There is no general theory that allows determining the final crystal structure of a thin film. Some empirical data can sometimes be used, but most of the time, the trial and error method is required. Finally, as a signature of the deposition method and process parameters, residual stress in thin film was also studied. Extrinsic stress is differentiated from intrinsic stress, and the final total average stress in a thin film can be related to the radius of curvature of the wafer using the Stoney equation. With this lesson, we close the chapter on physical vapor deposition.

- Atoms arrival
- Film-substrate interface
- Adhesion
- Growth modes
- Crystal structure
- Stress in thin films

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Practice quiz film growth: stress in thin films

Questions:

1. Both CVD and PVD are deposition techniques, which may induce extrinsic and intrinsic stress inside or at the interface of the deposited thin films. What kind of stress do you expect in a SiO₂ film deposited on a silicon wafer by CVD? Hint: CTE of SiO₂ is smaller than that of Si.

- No stress because CVD deposition is conformal
- Compressive extrinsic stress
- Tensile intrinsic stress
- Tensile extrinsic stress

2. Which of the following statements about stress in thin films are correct?

- Extrinsic stress is induced from CTE mismatch between two materials
- Extrinsic stress is uniform across the film thickness
- Intrinsic stress is related to the microstructure of the thin film and the deposition method
- Intrinsic stress is uniform across the film thickness

Supplementary

PVD 8: Film growth

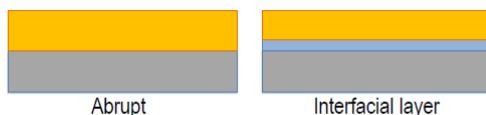
III. Growth modes and crystal structure

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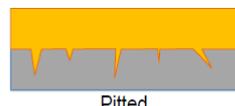
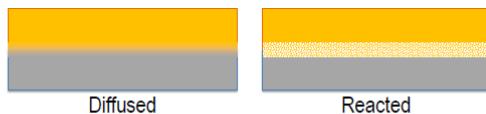
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Once there are enough atoms on the substrate surface, the film starts growing. A very important parameter here is the interface stability. Or in other words, the question whether the layer will adhere to the substrate or not. Thermodynamics allows determining if the atoms will be chemisorbed on the surface or not. So if the change in Gibbs energy, which is given by the Gibbs energy of the products minus the Gibbs energy of the reactants, is smaller than zero, then the reaction is possible. Let's take the example of titania on SiO₂. So the Gibbs free energy is the product Gibbs free energy of TiO₂ minus Gibbs of SiO₂ which is, in numerical values, known to be 160 - 165 Kcal, which is -5 Kcal which is smaller than zero, so this reaction can happen. It means we can deposit titania on SiO₂. Another material of interest may be cobalt. Depositing cobalt on silicon is also possible, as a corresponding Gibbs free energy calculation would show.

- Interface stability:



- Ti deposition on SiO₂



ΔG = Gibbs free energy difference in [kcal]
 G_{products} = products Gibbs free energy in [kcal]
 $G_{\text{reactants}}$ = reactants Gibbs free energy in [kcal]

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But the deposition of cobalt on SiO₂ is not possible as the delta G is larger than zero. Thus, the cobalt deposition on silicon is very sensitive to the presence of native oxides. Besides the initial interface stability criteria, different types of interfaces exist. An abrupt interface, shown here, is encountered in most PVD and CVD depositions and it produces an almost ideally sharp material transition. However, if the goal is to grow a thin film directly on silicon, this is not as straightforward as it sounds, because without special precaution,

silicon is often covered by a few nanometer-thick native SiO₂ layer. In this case, an interfacial layer exists between the substrate and the added film. Shown here. To remove the interfacial SiO₂ layer, typically, a special surface etching and cleaning has to be done prior to the deposition. So in some other cases, for instance during the deposition of copper on silicon dioxide, the added copper atoms diffuse into the substrate. Chemical reactions between the thin film and the wafer may also occur. This is the case of nickel, cobalt and titanium deposition on silicon which forms a so-called "silicide" at 400°C, 500°C and 600°C, respectively. There is a reaction going on at the interface. In some cases, an annealing step is sufficient to ensure a good electrical conductivity between the added thin film and the silicon. See the case of the pitted interface, for example. This is the case of silicon in aluminum when heated over 425°C. The spikes of the film into the wafer can be several micrometers deep. On the positive side, they allow for better electrical contact between aluminum and silicon and is even able to break through this thin native silicon dioxide interface

- 2D / Layer-by-layer mode (Frank-van der Merwe)
 - Strong atom-surface bonds
 - E.g. MBE, ALD, PLD

- 3D / Island mode (Vollmer-Weber)
 - Strong atom-atom bonds
 - E.g. evaporation and sputtering with heated substrate or ionic bombardment

- Columnar mode
 - Not enough energy to merge islands together
 - E.g. deposition at room temperature

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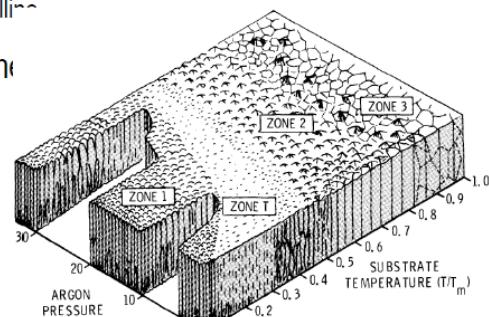
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that we have presented here before. Now let's have a closer look at how the thin films grow classify their modes, and identify the important parameters on which this depends. The 2D, or layer-by-layer mode, also called "Frank-van der Merwe mode", occurs when the added atoms, here in orange, bond more strongly with the substrate than with other atoms and when they have enough energy and time to diffuse around to their energetic minimum location. This is the case in ALD, MBE, and also PLD. Here, we have a relatively slow growth rate, so that the atoms have time to rearrange themselves before the atoms for the second layer are coming. The second growth mode is the 3D, or island mode. Also called "Vollmer-Weber mode". It typically occurs during the deposition of metal atoms onto an insulator, since bonds between metal atoms are stronger than bonds between insulator and metal atoms. In the island mode, surface atoms have enough energy and time to diffuse around but not as much as in the 2D mode, because the growth rate is higher than in the previous case. As a result, a few surface atoms nucleate together and form clusters, or islands. At some point, islands merge together and form a uniform film. For films formed by sputtering and evaporation, a continuous thin film forms at around 10 to 20 nm thickness. Before this threshold value, the film does not yet cover the entire surface. Island mode typically occurs with sputtering deposition or with evaporation when the substrate is heated. A mixed mode, combining 2D and 3D modes also exists. It is then called the "Stranski-Krastanov mode". Finally, when the surface atoms' energy and mobility is low, atoms stick where they land, and islands are not able to merge together. In this last mode, which is called the "columnar mode", grains grow upwards and voids between the grains can remain. Columnar mode typically takes place when the deposition is performed at room temperature. The growth mode determines the way in which the film forms. For us as users, what is more important is actually the resulting film intrinsic structure. It plays a key role for many physical properties of the thin film, such as electrical band structure, conductivity, hardness, transparency, and piezoelectric properties. The first important question to ask is if the film is amorphous polycrystalline or monocrystalline? As a rule of thumb, thin films made of silicon covalently bonding materials, compounds and alloys are often amorphous if no special precaution is taken

- Will the film be amorphous, polycrystalline or monocrystalline?
 - Silicon, covalently bonding materials, compounds (TiN , Al_2O_3) and alloys (TiW , $SiCr$) are often amorphous
 - Metals (Al , Au , Cu , W , Ti , Cr , Pt) are often polycrystalline

- Thornton's zone model for sputtering of metals

- Zone 1
 - Low temperature and/or high pressure
 - Low energetic atoms → porous tensile films
- Zone T and zone 2
 - Increase temperature and/or decrease pressure
 - More energetic atoms → denser compressive films
- Zone 3
 - High temperature → annealing
 - Film loses process details memory



Reproduced from John A. Thornton, "Structure-Zone Models Of Thin Films", Proc. SPIE 0821, Modeling of Optical Thin Films, 95 (1988) and John A. Thornton, "Influence of apparatus geometry and deposition conditions on the structure and topography of thick sputtered coatings", J. Vac. Sci. Technol. 11, 666 (1974), with the permission of SPIE and the American Vacuum Society. <http://scitation.aip.org/content/avs/journal/jst/11/4/10.1116/1.1312732>

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during the deposition. Metals, on the other side, are often polycrystalline. In order to grow monocrystalline films very special deposition techniques, such as MBE or PLD, are required. However, it is sometimes difficult to predict the exact structure of the thin film, as it depends on so many several parameters, such as the material itself, the deposition method, and the process. In case of sputtering of metals, for instance, a well-known model, called the "Thornton's zone model", shown here, can be used. It shows in empirical diagrams the morphology of thin films as a function of the chamber pressure, shown here on this axis, and the substrate temperature, normalized by the melting temperature of the thin film (T_m), shown here. Sputtered metal thin films have a poorly crystalline structure. At high pressure, or low temperature, zone one, atoms do not have much energy to diffuse around. Which results in columnar grains. We see them here. Usually, this leads to porous films with tensile stress unless oxygen is present in the chamber, which leads to compressive stress in the film. At lower pressure and higher temperature, impinging atoms are more energetic and can knock out loosely attached atoms and diffuse on the surface. This results in denser films with compressive stress. Simultaneously, the film grain structure moves from zone 1 to the zone T, for transition, and zone 2, where the grains are larger. At some point, if the temperature is further increased the film crystal structure reaches zone 3, where annealing occurs, and the film loses memory of the deposition process, as it is called in technical terms. In the case of sputtered aluminum, typical grain size can go up to $0.5 \mu m$ and can be in the order of the film thickness. Processes which depend on grain boundaries such as diffusion and electromigration, are strongly affected by the ratio between grain size and the characteristic dimensions of the thin film in the microdevice. For some materials, the film crystal structure does not change continuously as described in the Thornton's zone model. Instead, it changes abruptly due to a phase change occurring at specific temperatures. An example of such a material is tantalum. Finally, it is relevant to note that the texture of the added thin film is inherited from the underlying film. Seed layers are therefore often used to obtain a well defined crystal orientation on the subsequent deposition of a thicker film.

SUPPLEMENTARY Practice quiz film growth: growth modes and crystal structure

Question:

1. Which of the following statements about growth modes and crystal structure are correct?

- 2D growth mode typically occurs when depositing a thin film by sputtering
- Thornton's zone model enables to predict the crystal structure of sputtered thin films
- Metal thin films have generally an amorphous structure
- Depositing a cobalt thin film on a glass wafer is not possible

Conclusion and summary

In this chapter about physical vapor deposition, you have learned the physical principle, the different setup configurations as well as the advantages and limitations of the two main PVD techniques which are thermal evaporation and sputtering. Supplementary material also introduced you to other PVD techniques such as ion assisted deposition, molecular beam epitaxy, pulsed laser deposition and parylene coating. Finally film growth was also studied. Here are a few important key points you should remember.

Thermal evaporation

- The material to deposit is heated and evaporated from a crucible and condensates on the substrate to form a thin film.
- E-beam heating of the evaporant enables to deposit higher purity films than resistive-heating.
- Evaporation is a line-of-sight technique which can be used for lift-off and stencil lithography.
- If a good uniformity is required, rotating planetary systems can be used.

Sputtering

- Ions from plasma impinge on a target made of the material to deposit. Atoms from the target are ejected and deposit on the substrate.
- Plasma creation, plasma zones and Paschen's law.
- DC vs. RF vs. magnetron sputtering.
- Sputtering enables good film adhesion and step coverage.
- Sputtering enables to deposit more various materials than thermal evaporation.

Other PVD methods (SUPPLEMENTARY)

- IAD/IBAD can be used to clean and activate the substrate, to improve film adhesion and uniformity and to increase film density and hardness.
- MBE can be used to grow epitaxial layers at relatively low temperature with a precise thickness control.
- PLD enables deposition of complex stoichiometry materials at atmospheric pressure.
- Parylene coating enables thick conformal protective coatings.

Film growth

- Thin films adhesion depends on materials, substrate cleanliness and deposition method.
- Thin films growth results in intrinsic and extrinsic stresses which induce bending of the wafers.
- Growth modes and crystal structure of thin films depend on the deposition method as well as on atoms energy and diffusion time when they arrive on the substrate surface. (SUPPLEMENTARY)

Chapter 4: Lithography



Introduction and objectives

Lithography

This module on lithography describes in details the two main resist patterning methods: optical and electron beam lithography. Physical principles, setup configurations, process parameters, resist properties, advantages and limitations, as well as examples are introduced and discussed for these two techniques. In addition, an overview of some alternative techniques such as thermal scanning probe lithography is also presented.

At the end of this week, you should be able to:

- Name the different lithography techniques and list their main advantages and limitations.
- Describe how the different lithographic tools operate and what are the important technologies that enable each method.
- Discuss the underlying physical interactions between photons, electrons and other probes with the resist to describe the lithographic process.
- Analyze, describe and classify different lithographic results with a specific patterning technique.
- Evaluate and associate different methods and processing conditions with a desired result taking into account both the end goal and the practical possibilities.

Intro quiz

Questions:

1. In a typical lithography process flow, the photoresist is locally exposed to UV light through a mask and is then developed. While the resist serves as etch mask for a subsequent etching step, the developed parts give access to the substrate below for the pattern transfer. During the development step, by which mechanism is the resist removed?

- The resist is evaporated
- The resist is dissolved
- The resist is sublimated
- The resist is delaminated

2. When performing lithography, one can rely on either photons in optical lithography or electrons in electron beam lithography to expose the resist. Choose which of the following statement(s) is/are true.

- Electron beam lithography requires the substrate to be conductive or to have a conductive layer on the resist.
- In optical lithography the substrate should be transparent.
- While diffraction is a limiting factor in optical lithography, it is not the limiting factor in electron beam lithography.

>>3. Which of the following statements about photolithography and electron-beam lithography, is/are correct?

- Electron-beam lithography can be used to expose a full wafer through an electron-mask
- UV photolithography can be used to expose a full wafer through a photomask
- Electron-beam lithography can be used without an electron-mask as a serial beam writing method
- Photolithography can be used without a photomask as a serial writing method
- Electron-beam writing can generate smaller features than UV photolithography
- Photolithography can generate smaller features than electron-beam writing



Lithography 1: General concepts

I. Introduction to lithography

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As there are several possibilities to perform lithography, I will start by providing some definitions and by explaining some general concepts that are recurring for all the lithography variations.

- General concepts
- Mask writing and Direct Write Laser
- UV lithography
- Electron Beam Lithography (EBL)
- Alternative lithographies

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- Lithography process flow
- Exposure methods
- Photoresist
- Pattern transfer

Then I will dive into details how one fabricates the lithography masks using a direct write laser tool. This will be followed by a closer look into UV lithography and electron beam lithography which are to date the two main categories of lithography. I will then conclude by presenting new emerging and alternative lithographies which are not yet part of the main stream applications, but that offer interesting opportunities for niche applications. Lithography is the fundamental process of transferring geometric shape from a design to a thin layer of radiation sensitive material called resist, which is covering the surface of a wafer substrate. These shapes or patterns define the various regions in an integrated circuit, such as the implantation regions, the contact windows, the metallic wiring etc. The resist patterns made by lithography are not permanent but only temporary replicas of circuit or MEMS features. To produce the final features in the material of interest, these resist patterns must be transferred once more into the underlying layers, for instance by an etching process which selectively removes unmasked portions of a layer. The pattern transfer techniques are described in more details in the lesson on wet and dry etching.

- Processes involved
 - Radiation generation and shaping by an exposure tool to tune the intensity, wavelength and surface where the resist is exposed.
 - A chemical reaction involving both the resist and developer
 - Mechanical control over the relative position of substrate and exposure tool for alignment of possibly multiple layers

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The lithography exposure step itself can be done by various sources of electromagnetic radiation, either by using photons or electrons. All lithography processes must be performed in an ultra clean environment to avoid that any dust particle in the air can settle on the wafers or lithography masks and can cause defects in the device. Lithography is also carried out in yellow light. Indeed, the photo resist is sensitive to light with shorter wavelengths. UV light is therefore filtered out from lithography areas in a clean room. More on clean room specific features are given in the corresponding lesson. This slide provides an overview of possible parts from a design file

- Fundamental step in microfabrication
 - From design to physical patterning
 - Enabling step for local dry etching or metal deposition
- The lithography step is based on
 - Electromagnetic interaction and modification of a resist via photons or electrons, followed by development
- In a cleanroom & under yellow light

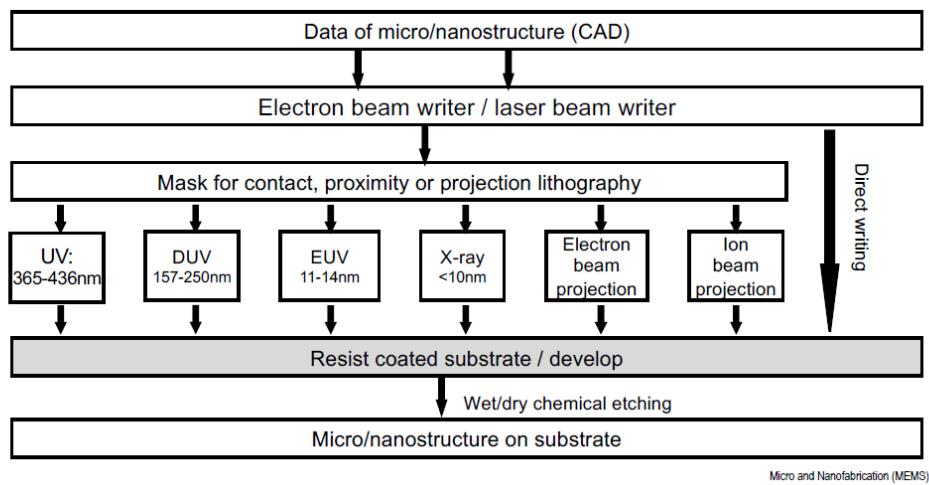


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or a CAD file, on a computer to define a micro or nano structure or circuit on a wafer. Here is the start of the data on the CAD file, on a computer. And at the end, we want to have the micro or nano structures on a

substrate. From the CAD file, we can steer by computer control, the write head of a beam writer that uses either focused laser or electrons. This is the first conversion from a virtual computer design feature into a physical reality. In the majority of the cases the beam writer is used to fabricate masks for lithography. This is because the writing can take a lot of time. Only in cases of R&D when only few devices are needed. One considers the direct writing of the final structure. Depending on the radiation source, one speaks about UV, deep UV, extreme UV, x-ray, electron beam projection, or ion beam projection masks, all with their own specificities. In each case, the radiation impinges locally onto a resist coated substrate and modifies the resist which can then be developed. The resist subsequently serves as a mask for pattern transfer by etching to complete the micro or nano fabrication step. So once again to summarize, the processes involved in lithography firstly include the generation of a radiation that needs to be tuned and precisely shaped to impinge on the sensitive resist where needed. Second, it involves a chemical reaction between the resist radiation, and then the resist and the developer. Last but not least, it requires a very precise mechanical tool for the positioning of the mask or the beam on the resist coated substrate, in particular for the patterning of alignment and multi-layer features. Each lithography follows a well defined series of process steps, called process flow. It may vary according to the lithography used and the materials involved. But a typical generic

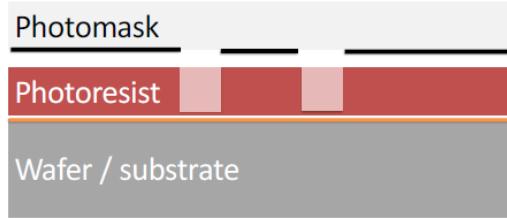


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example is shown here, where we go step by step through it. First the substrate - it can be a silicon wafer or glass plate - is cleaned and prepared and eventually coated with a thin film of material that needs to be patterned. Second, the photo resist is being coated on the substrate to form a layer of it with a well controlled thickness in the order of a micrometer, but this can vary a lot.

- Substrate preparation
 - Resist coating and pre-baking
 - Resist exposure
 - Resist development
 - Pattern transfer (etching, lift-off)
 - Resist stripping

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And most importantly, with a very uniform thickness over the entire substrate surface. Some pre-baking is done to remove excess solvent and to dry the resist. Then comes the essential step, which is the resist exposure. This step can be done either by photons or electrons. In this example shown here, I show the use of a UV light source and expose the resist through a photomask that contains transparent (here), and opaque regions. Only under the transparent portions of the mask we will expose the resist. The other method would be using electrons that can be scanned over the surface, and thereby writing the pattern - this will be shown in details later. In both cases, the goal is to chemically modify the resist under the radiation so that it becomes either polymerized by creating new chemical bonds, or by breaking existing chemical bonds. The choice to use either optical UV lithography or electron beam is driven by the quest for resolution and throughput. The step after the exposure is resist development, shown here, which is a chemical bath that dissolves the part of the resist that has not been polymerized or whose bonds have been weakened by the exposure.



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Then the resist pattern is transferred into the layer of interest by etching or by lift-off. These steps will be explained elsewhere in this course. At the end, the resist is not used anymore and can be removed by a so-called stripping process in solvent and cleaning acids. And the target device pattern is now completed.

Practice quiz introduction to lithography

Questions:

1. Photolithography is done in areas of the cleanroom under yellow light conditions. What is the reason for this?

- Yellow light causes less strain on the operator's eyes.
- To prevent the photoresists (which are sensitive to UV-light) from being exposed by ambient light.
- Sodium lamps are used to prevent contamination in the cleanrooms.

2. What are the advantages of using UV-lithography compared to E-beam?

- Higher resolution
- Lower cost of the equipment
- Higher throughput in wafer per hour

3. Consider that some micro-structures have to be etched into a silicon wafer for a micro-fluidic device. Put the necessary fabrication steps in the correct order.

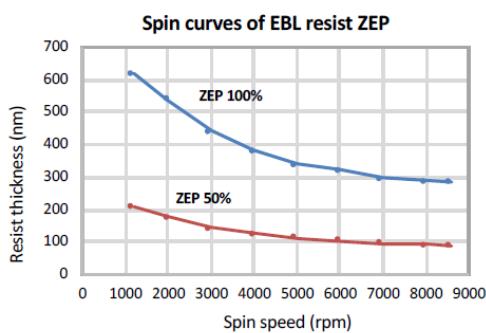


Here I explain a few details on the resist coating steps. First, one needs to ensure that the surface is clean and free of any contamination particles such as dust to allow a uniform film formation. Besides that, it is very important to tune the surface properties of the substrate for a good resist adhesion. This is typically done using HMDS coating either in the liquid or gas phase. This ensures that the photo resist, also in very thin layers, adheres well and uniformly on the surface.

- Substrate preparation
 - Surface cleaning
 - Resist adhesion
- Resist coating
 - Spin coating
 - Spray coating
 - Casting
 - Lamination

$$T = K C^\beta \eta^\gamma / \omega^\alpha$$

Resist thickness T
 K = overall calibration constant
 C = polymer concentration in g/100 mL solution
 η = intrinsic viscosity
 ω = rotations per minute



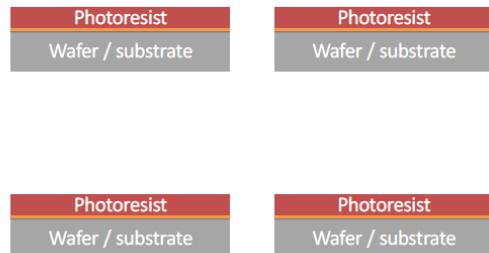
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For the resist coating, the wafer is held on a vacuum spindle and a well defined amount of liquid resist is applied to the wafer center like shown here. The wafer is then accelerated up to a constant rotational speed which is then maintained for around 30 seconds. The thickness of the resulting resist film is given by this formula shown here which depends on the polymer concentration and viscosity as well as on the spin speed. Spin speed is quite fast, generally between 1,000 and up to 10,000 RPM to give uniform films from as thin as sub 100 nanometers to several micrometers, depending on the lithography application. The curve here shows the film thickness as a function of spin speed for a typical electron beam resist called ZEP. Such curves are done for each resist product and are available on the product information sheet. Besides spin coating,

there are also other resist coating techniques. For instance, spray coating allows using non planar substrates. Another technique is "casting", that uses a mechanical doctor blade to uniformly spread a very viscous resist. Finally, a technique called "lamination" transfers an already formed dry resist film directly onto the substrate. The two latter examples are of great interest for very thick photo resist layers. There are several ways to expose resist.

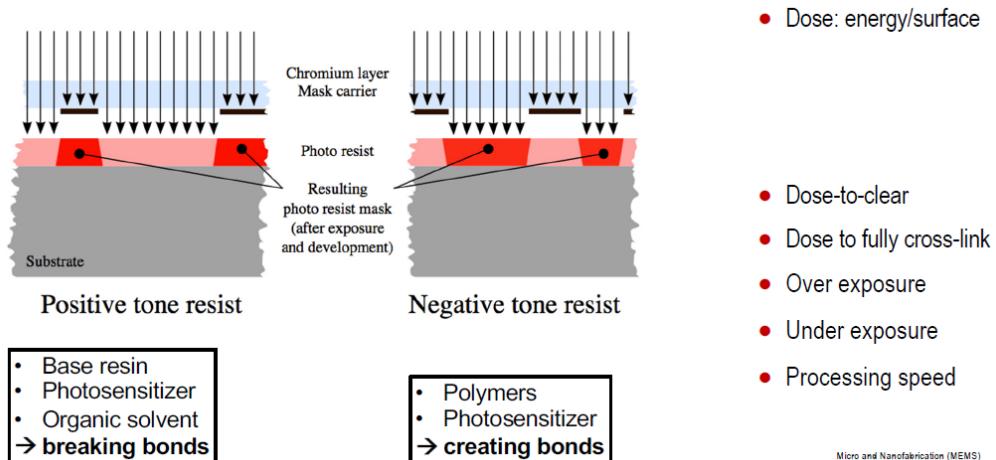
- **Exposure** brings localized energy in the form of photons, electrons or ions
- Resist is **sensitive** to the energy used
- Optical lithography uses photons (resolution limited by diffraction $\sim \text{wavelength}/2$)
- Electron beam lithography uses electrons (limited by scattering)
- X-ray lithography (complicated mask)
- Ion beam lithography (complicated tool)



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In every case, it is a sort of energetic radiation that alters the resist chemistry as explained before. The first and mostly applied way is to use photons. Indeed, the majority of exposure tools for integrated circuit components and MEMs, are optical systems using ultraviolet light. Optical lithography uses masks to create the pattern, either in contact for 1 micrometer scale, typically for MEMs, or by projection systems for deep UV, typically for CMOS. Optical exposure is limited by diffraction. However, state of the art deep UV exposure tools are capable of high resolution down to 10 nanometer scale thanks to the deep UV wavelengths, new resist chemistry, and resolution enhancement. The advantage of optical lithography is that the entire wafer or part of it can be exposed at once which allows for high throughput. Electron lithography is primarily used to produce the photo masks



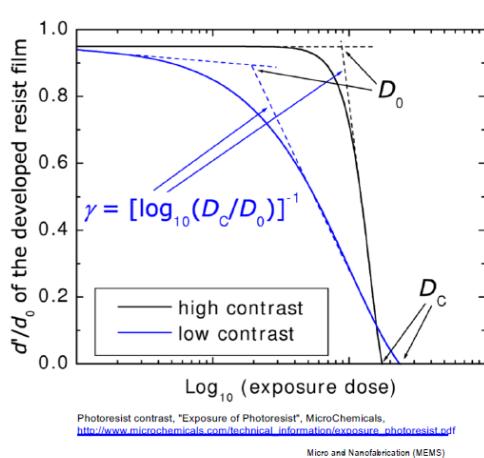
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that are then used in UV and deep UV litho. But more and more direct writing using modern EBL systems is now possible with reasonable throughput. Here the electron beam is focused on the resist and then raster or vector scanned to write the pattern. The resolution limit of EBL is given by the back scattering of electrons that expose all the resist area near the writing zone. More details on this will be provided in the dedicated lesson. X-ray lithography uses a highly energetic beam to expose the resist.

It has in principle extremely high resolution as diffraction is much smaller than for deep UV and UV photons. But this technique requires a very special and complicated mask that is opaque to the x-rays. Therefore it is not used for integrated circuit or MEMS fabrication but is used for specific niche applications. One of them is the exposure of very thick PMMA resist in the so called NIKA process.

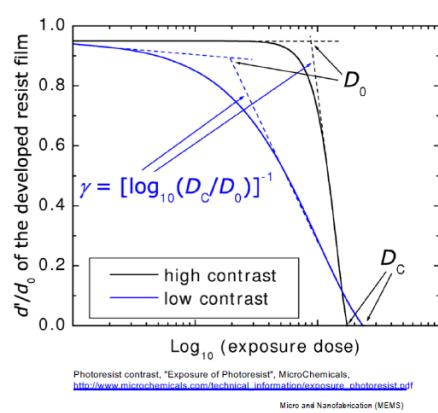
- Contrast is an intrinsic parameter that defines from which dose a reaction starts and at which dose it is completed
- Determines the critical dose for a lithography process
- High contrast gives steeper sidewalls
- Low contrast allows for gray scale lithography



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A further possibility is to use ions which are like electrons, charged particles, but they are also much heavier and have therefore less back scattering in the resist and the substrate which increases the resolution. Ion beam lithography systems are constantly developed further but it is not clear whether they will be used for mainstream lithography. So they should be considered as a niche technique. Now let's talk about resist, which is besides the exposure tool, the other very important ingredient of a successful lithography at micro or nano scale. The photo resist is a radiation sensitive compound. Photoresist can be classified as positive and negative depending on how they respond to radiation. For positive resist, the exposed regions become more soluble, and thus more easily removed in the development step. The net result is that the patterns formed in the positive resist are the same as those on the mask. For negative resist, the exposed regions become less soluble and the patterns formed in the negative resist are the reverse of the mask pattern. A similar classification can be done for electron beam sensitive resist. Thereby the exposure is not done via a mask, but by direct writing. Depending on the writing area, it is beneficial to choose either positive or negative e-Beam resist. Positive photoresist consists of 3 components.

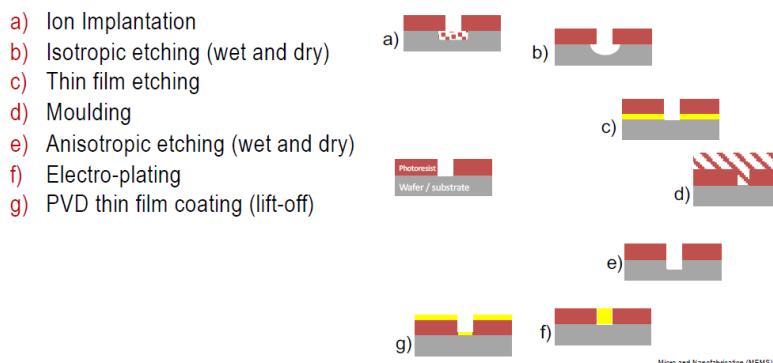
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A base resin, a photo sensitive compound, and then organic solvent. Before the exposure, the photo sensitive compound is insoluble in the developer solution. After exposure, the photo sensitive compound absorbs radiation in the exposed pattern areas, changes its chemical structure and becomes soluble in the developer solution. Upon development, the exposed areas are removed. Negative tone photoresists are polymers combined with a photo sensitive compound. After exposure, the photo sensitive compound

absorbs the optical or electron energy and converts it into chemical energy to initiate a chain reaction. This reaction causes cross linking of the polymer molecules. The cross link polymer has a higher molecular weight and becomes insoluble in the developer solution. Upon development, the unexposed areas are removed. One major drawback of negative tone resist is that in the development process, the entire resist mask swells by absorbing developed solvent, which may limit the attainable resolution of negative resist.



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The resolution of a lithography process depends on one hand on the exposure tool and on the other hand on several key parameters of the photo resist. One of them is the resist sensitivity and corresponding required dose. Because the radiation is also absorbed in the resist medium, there is a minimum amount of radiation dose required to expose the resist from the top to the bottom so that it can be cleared in the development step. The required dose is called "dose to clear", or "dose to fully cross link" in the case of negative resist. The dose can be calculated by knowing the lamp's intensity distribution in watts per centimeter squared and the exposure time in seconds. So the dose is equal to the intensity times the time.

The performance of any photo resist can be characterized by its contrast curve. It is an intrinsic resist parameter that defines the minimum dose limit that is required to start a reaction, and the upper dose limit at which the reaction is completed. Photoresist contrast is important for both resolution and profile.

The example here is for positive photoresist but the same holds also for negative resist. The contrast curve of a photo resist, plots the remaining resist thickness after developing in relation to the thickness before the development, D' over D_0 , as a function of the logarithmically plotted exposure dose. The transfer of information from a given contrast curve to an individual lithographic process requires information of all process parameters which impact on the developing rate such as the resist thickness, soft bake, rehydration, air temperature, and humidity, etc. The contrast curve of an ideal positive resist, is a step function where the contrast is infinite. Realistic contrast curves show a D' over D_0 already smaller than 1 for an exposure dose of 0, which is the dark erosion, and a non-infinitesimal logarithmic decay in the D' over D_0 , bigger than zero over a non-zero range of the dose towards D_c which is the dose to clear. The slope of this decay defines the contrast. High contrast is beneficial for the resist profile. On the one hand, it is easy to achieve vertical walls while on the other hand it can be tricky to find the correct dose for high contrast resist as they are easily over exposed or saturated. Low contrast may be good for example for grey scale lithography. So this shows the slope for a low contrast photoresist versus the one for high contrast photoresist. Once the lithography step is done in the resist, we can now see what pattern transfer steps can be done using the resist as a local mask. Here is an overview of possible process steps. The first example a) is using the photo resist as a mask for local implantation with ions to do a local doping of the substrate with incoming ions that are masked by the photoresist. Or... Example b) is to use it for isotropic etching, the mask is protecting the substrate and when the etching reaches the substrate it shows isotropic etching, that means etching in all directions with the same speed

- Lithography process flow
- Exposure methods
- Photoresist
- Pattern transfer

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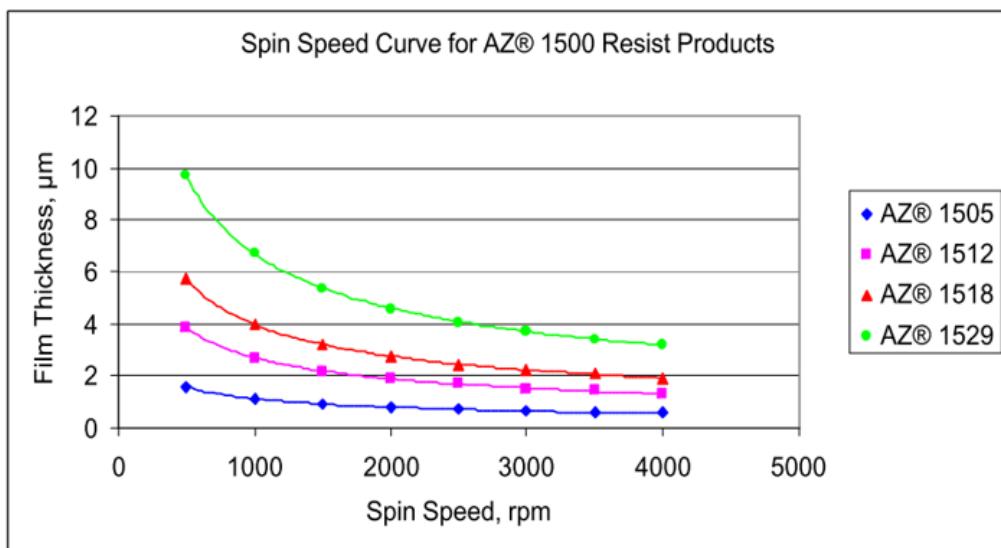
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which gives this circular shape. Or example c) would be to etch a thin film that has been previously coated on the substrate so an example of gold, or another metal layer can be etched locally through the opening in the photoresist. Example d) would be to use the photo resist structure on the surface as a mold, for creating a replica by pouring for example, another polymer over and cross linking, and then creating the negative of the opening of the photoresist pattern. Example e) would be to use the mask for anisotropic etching, in this case, in contrast with the isotropic etching we create vertical walls the well defined geometrical feature in the substrate. Or example f) would be to do electroplating, that means filling the opening in the photoresist by growing a layer locally in that aperture. And the last example g), would be to use the photo resist as a mask for lift-off processes in a physical vapor deposition step. So this concludes this introduction lesson on the lithography. I have shown you the process flow of a typical photo lithography process, and showed you some exposure methods that exist to irradiate the photoresist. I gave you some first information about intrinsic resist properties, and also showed at the end, how the photoresist pattern can then be transferred into a layer of interest.

Practice quiz resist properties and exposure methods

Questions:

1. The following spin curve is given by a photoresist provider, showing the resist thickness as function of spin speed. We want to coat a silicon wafer with a 2.0 micrometer-thick layer of AZ1518 photoresist.
Which spin speed (in rotations per minute) do we need to apply?



2. Our goal is to etch small holes in a silicon wafer that has a diameter of 100 mm. The photoresist will be exposed by direct-laser writing, followed by developing. The structured photoresist will subsequently be used as an etch-mask for the dry-etching of the small holes into the silicon. Which kind of photoresist should be used to minimize the writing time of the laser writer?

- Positive or negative; it does not matter
- Negative photoresist
- Positive photoresist

3. Spin-coating is one of the most used coating methods for defining a well-controlled photoresist layer onto a wafer. Which of the following methods can also be used for special coatings?

- Resist spray coating
- Resist casting
- Resist lamination



The lithography resolution is the function of several parameters. Besides the exposure tool performance, it largely depends on the photoresist properties. Two important features are the intrinsic sensitivity, and the resist contrast. We will briefly discuss both. The intrinsic sensitivity ϕ of a photo resist, is the incident energy necessary to produce the photo chemical reactions required for defining patterns.

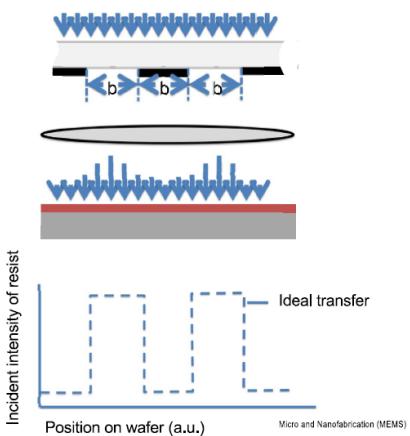
- Intrinsic sensitivity Φ = necessary incident energy needed to produce photochemical reaction
- single component resist \sim quantum yield
- $\# \text{ photon-induced events} / \# \text{ photons}$ absorbed
- $\Phi_{\text{PMMA}} = 0.02$
- $\Phi_{\text{DQN}} = 0.2 - 0.3$

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For single component resists, it is given by the quantum yield, which is the number of photon-induced events over the number of photons absorbed. The intrinsic sensitivity of two typical photo resist PMMA and DQN are shown here. We can see that PMMA is ten fold less sensitive than DQN for instance. The intrinsic sensitivity can be determined experimentally by a systematic series of exposure tests with subsequent structural, and microscopic analysis of the resist. Details on how this is done can be found in the text books or resist data sheets. The resist that one plans to use must be insensitive to the ambient radiation, that means the yellow light in a clean room and must be sufficiently sensitive to the range of radiation energy provided by the exposure tool, in order to absorb the maximum of energy in a

minimum of time. The resist should not be too sensitive either to avoid too short exposure times for a more comfortable process window. The optical transfer function (OTF) also called modulation transfer function (MTF), is the transfer function of an optical exposure system onto a resist.

- MTF is a measure of the optical contrast in the areal image by the exposure system.
- The higher the MTF the better the optical contrast.
- MTF of an image is defined as:

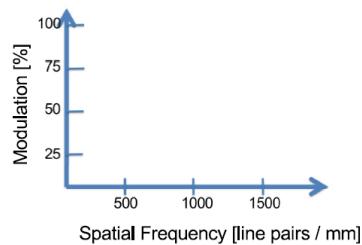


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The function specifies the translation and contrast reduction of a periodic sine wave pattern after passing through the lens system as a function of its periodicity and orientation. Formally, the optical transfer function is defined as the Fourier transform of the point spread function or impulse response of the optics. That means the image of a point source. While figures of merit such as contrast, sensitivity, and resolution give an intuitive indication of performance, the optical transfer function provides a comprehensive and well defined characterization of optical systems. When using a lithography mask, with line width b and pitch b the light beam passing the mask, and reaching the wafer at a certain modulation due to diffraction.

This modulation can be described by the MT effect expression which is the maximum intensity minus the minimum intensity over the maximum intensity plus the minimum intensity that passes the mask. This transfer function combined with the resist characteristic, the contrast, allow to define the condition for the optical image. For high contrast resist, it is easier to get a high resolution than for a low contrast resist with the same MTF.

- MTF increases with decreasing λ
- MTF = 1 for larger features
- MTF $\rightarrow 0$ for closely spaced features

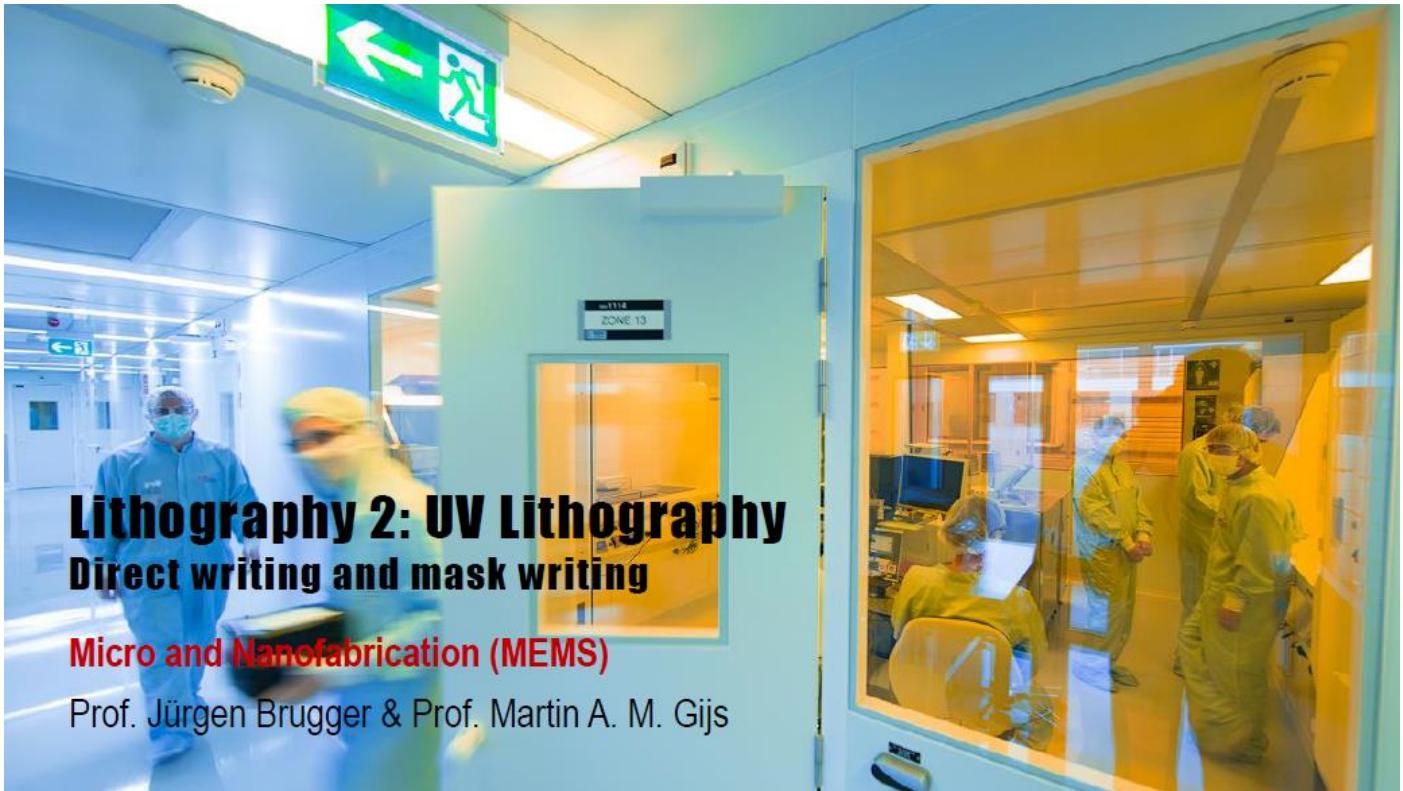


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On the other hand, the MTF depends heavily on the motif and the mask. The more b is reduced, the more the difference between the minimal and the maximal irradiation intensity reduces and it becomes difficult or impossible to selectively irradiate the different resist parts under the mask. For low contrast resist, it becomes difficult to resolve the image of the mask and to clear the resist under exposure,

while keeping the full thickness of the opaque regions in the case of a positive resist. The modulation transfer function can also be expressed in a curve, shown here, that relates the spatial frequency, line pairs per millimeter, versus the modulation in percentage. For increasing spatial frequency of closely spaced

opaque patterns in a chrome mask, as expected, the modulation drops. This all depends of course on the wavelength used, the optical transfer function as well as the resist contrast.



In this lecture I will describe the process flow for making a photo mask. I will in particular focus on the use of a direct laser writer that allows to convert a CAT file into a physical mask. I will also show a couple of cleanroom Section that demonstrate the technique and conclude with some examples. In this lesson we are going to focus on the direct laser writing and the fabrication of a photo mask used in a mask aligner

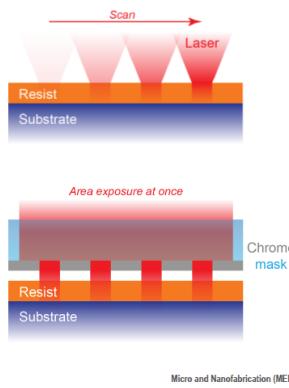
- Photo mask process flow
- Direct Laser Writer
- From the CAD file to the mask
- Cleanroom videos
- Examples

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for UV photolithography. There are 2 main approaches in light based lithography. One being the serial writing using a scanning laser beam on the substrate referred to as 'direct laser writing'. The second approach consists of exposing the substrate through a mask. The exposure duration for direct laser writing, being a serial process will heavily depend on the surface and dose to deliver to the photoresist. In practice, the exposure of a 4 inch wafer or a 5 inch mask can take from a few minutes to more than an hour depending additionally on the required resolution. Direct laser writing is therefore mainly used for mask making and eventually for some prototyping and fabrication of small batches where a mask based exposure will be preferred in the case of large series. Additional features of direct laser writing include the possibility to obtain high resolution features in a non-contact manner. The laser-based light source additionally allows for very high power densities and narrow line width. For ultimate resolution of mask features such as needed for deep UV, e-beam lithography is an alternative.

- Two approaches in photolithography
 - serial laser writing vs parallel using photomasks
- Single serial writing of a photomask
 - Exposure from minutes to hours
 - High resolution without contact
 - Single wavelength
- Exposure through mask for pattern replication
 - Exposure time in seconds
 - High throughput
 - Laser writing required for the original mask



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In the exposure through a mask method, here shown, we gain a lot in time as now the entire wafer or part of it is exposed in just a few seconds so we can get high throughput and produce many wafers per hour. Still, for making the mask, we need a writer; either laser or electron based. Before going into details of direct laser writers we will first have a look at the process flow for the fabrication of a photomask that will stand as a motivation throughout this chapter. A photomask consist of a thick quartz or soda-lime square plate coated with a thin, opaque chromium layer. In order to pattern this chromium layer, that will selectively block or allow light to pass during the exposure, we must perform the following sequence of steps. After coating the mask with a layer of photoresist, that is typically of positive tone and sub-micrometer thick, a laser writer is used. By scanning and blanking the laser beam one can expose arbitrary patterns into the resist layer. Then follows the development of the resist to reveal the desired portions of chromium. The metal can then be etched in wet chemistry before removing the resist in solvents to obtain the final photomask. A direct laser writer consists of a laser light source and a variety of optical components that will shape the beam and tune its intensity before impinging the wafer, which would be down here. This would be the place where we place the wafer. The beam may either be focussed into a single spot or shaped by



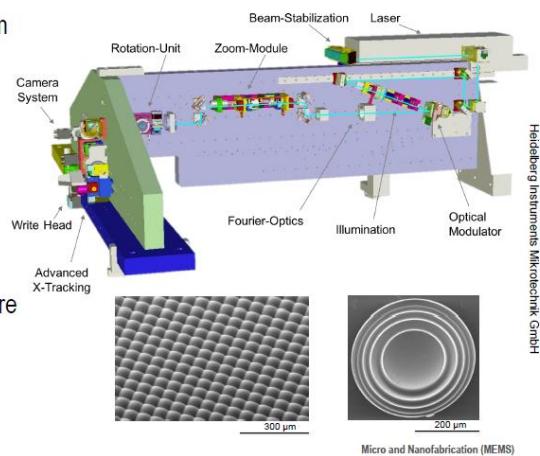
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a spatial light modulator (SLM) or digital mirror display (DMD) to project a line or area of pixel at once in order to improve throughput. Various elements, including the final write head enable the control of demagnification of the projected pattern as well as final resolution. Additional important elements include a high resolution mechanical stage equipped with an optical interferometer to displace the wafer under the static write head as well as an independent camera and illumination system in order to image and register alignment marks for multiple layer processes. When compared to parallel exposure in a mask aligner, direct laser writing enables convenient dose modulation throughout the exposure. This allows, for example, greyscale lithography where the dose is modulated to partially expose the resist layer and tune its final form in 3D. This is additionally useful to perform dose tests on sensitive patterns. The 2 SEM images

here show examples of such 3D greyscale lithography. A micro-lens area here on the left and the planar lens with circular fragmented slopes here. But these patterns are impossible to make with planar UV lithography and can only be made by a direct laser writer where one can control the exposure dose locally on the photoresist. The ultimate resolution limit in direct laser writing is based on the Rayleigh criterion and is approximately $\lambda/2$ times the objective numerical aperture. This gives a good idea of how finely the laser beam may be focused on the surface of the resist. In practice this theoretical value must also be compared to the resolution limit and processing of the photoresist, resulting in an ultimate resolution which is typically in the order of 600 to 800 nm. The final write head of the laser writer may also be exchanged with a finer lens of different focal lengths to adapt to the writing surfaces and required resolution. Longer focal lengths will allow, for example for the projection of a space light modulator over a larger area and thus allowing for faster writing but will result in a lower resolution. This is due to 2 effects: First, the contribution of longer

- Direct writing of resist with a laser beam
 - Point by point, single pixel raster scan
 - Partial area exposure with an SLM or DMD
 - Projection of a multi-pixel area at once
 - Semi-parallel approach improve throughput
- Stage based displacement
 - High resolution interferometers
- Tunable dose and focus during exposure
 - Greyscale lithography
- High power density
 - Thick and absorbing layers



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focal lengths reduces the length's numerical aperture for a given entrance pupil and second, the fact that the same number of pixels being projected over a large area effectively increases the pixel size and minimal feature size. In this context, one may also indirectly relate the number of assignable elements on the SLM to the final resolution of a system. Typically the CAT files that define the design to write consist of a vectorial description of different layers and repetition of basic cells. They are of a standard format called CIF or GDS. It is interesting to point out that the fully written 4 inch wafer may contain hundreds of millions of features that must be handled when converting the design from its original form to a laser writable one.

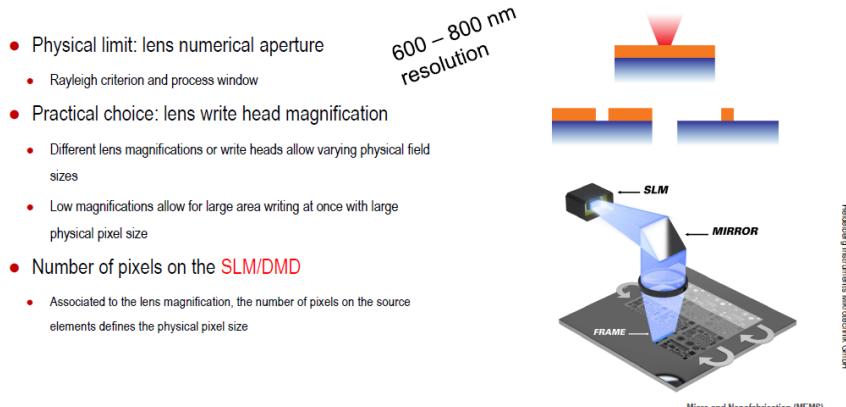
- Resist development
 - Positive resist type (e.g. AZ1512)
 - Resist thickness 0.6 μm for high resolution
 - Development in MP 351 (water diluted 1:5)
 - NaOH aqueous alkaline solution
- Dissolution of exposed resist
 - Chromium wet etching
 - $\text{HClO}_4 + \text{Ce}(\text{NH}_4)_2(\text{NO}_3)_6 + \text{H}_2\text{O}$
 - 90 second etching
- Resist strip in solvent and water rinse



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Essentially the final design preparation may include simple steps such as the mirroring of the design in order to obtain the desired pattern after projection through a photo mask. More complex operations include the fracture of the design into sub-elements or stripes that the laser writer will write. This will essentially depend on the desired resolution. Advanced features include shape corrections that take the entire process into

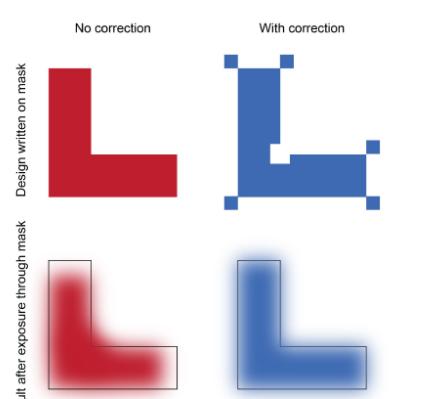
account in order to obtain final features as close as possible to the original design. One example is the use of serifs, shown here to compensate for diffraction at sharp edges or to add some bias to the exposure to compensate for the final beam size as well as the axial asymmetry. Now that the resist layer on the chrome coated mask has been exposed the positive resist is developed. Here we are using 600 nm thick positive photoresist. The development is performed in an alkaline solution. After thorough rinsing, the exposed areas are cleared and ready for the etching. The etching of chromium is here done via wet chemistry. The process is isotropic and may result in a slight under-edge. It may also take longer time to clear the chromium in small apertures due to limited chemical renewal at the surface. These aspects may be compensated for at the design stage and will have a strong impact when aiming for ultimate resolution. After the chrome etch, the photoresist is removed from the mask using solvents before a final rinsing and drying of the photo mask. Here you can see a photomask in chrome and glass that has been written by the laser writer in our cleanroom and that will be used for the UV lithography. As said, the main application field of direct laser writing is mask writing however, one further interesting application of direct laser writing is the fabrication of, for example, SU-8 structures.



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This epoxy like negative resist can be coated up to mm thick and stands as a robust functioning material used for optical elements, MEMS and master molds for further processing. As the mold may be further replicated and only one single master is needed, direct write laser is ideal for the production of such elements. On the top you can see 2 images with test patterns that demonstrate the high aspect ratios; up to 10:1 in this case, reached in direct writing laser and below you can see 2 examples of structural elements. A radial test structure with narrow tapers here on the left and the mold for microfluidic channel here. Direct laser writing is not limited to flat 4 inch wafers as seen up to now. In the direct laser writing setup the laser head is fixed

- Typical CAD files .CIF or .GDS
 - Repetition of base cells
 - Multiple layers
- Mask writing: design mirroring
- Choice of resolution
 - Design discretized on a grid: affects speed and resolution
- Shape corrections
 - Serif: compensate corner smoothing
 - Bias: compensate for finite beam size
 - Axial bias: compensate for beam shape/ asymmetry

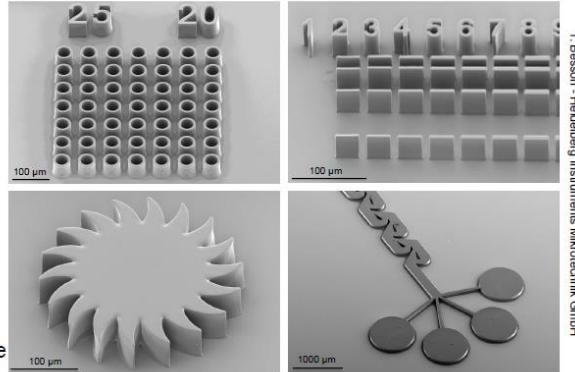


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but if the substrate motion can be controlled freely, lithography on 3D features is possible as shown here in this Section .Another extreme application of direct laser writing is that it may be scaled up for the writing of several square meters surfaces for example, in the case of large displays which are used in production in consumer electronics. Here you can see some specialists preparing the table and stage of such a large system. This concludes this chapter in the lithography where I introduced to you the mask making process using a direct laser writer.

- SU-8: negative-tone resist
 - Epoxy-like functional material
 - Large thickness range from μm to mm
- Applications:
 - Optical elements
 - MEMS and cantilevers
 - Molds for post-processing
- Unique property:
 - Self focussing via refractive index change during exposure: high aspect ratio



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I have shown you some details about the process flow of the photomask fabrication and showed you some insights into the direct laser writer equipment and how we get from the CAT file to the mask. At the end I showed you some examples that can be done by playing with the energy and the dose of the direct laser writer.

- Large scale masks
 - Over 1400x1400mm writing area
 - Source output up to 10W



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Practice quiz UV lithography: direct writing and mask writing

Questions:

1. In UV-lithography we typically use a photomask, which is made of a transparent glass plate coated with a structured chromium film. What is the process flow to fabricate such a mask, assuming that the chromium and resist layer are already added on the glass plate?

- Development, laser writing, etching, resist stripping, dehydration
- Laser writing, development, etching, resist stripping, dehydration
- Development, etching, resist stripping, laser writing, dehydration

2. When using direct laser writing, which statements listed below are correct?

- Micrometric features can be achieved without contact to the photoresist.
- The exposure is a serial point by point process that is limited to millimeter areas.
- Laser writing can be used for the fabrication of a UV photomask.

3. When writing with a direct laser writer, what are the unique advantages compared to mask-based lithography?

- The ability to tune the dose along a single exposure to create 3D structures in the photoresist
- The ability to change the focusing distance when exposing thick photoresist layers
- To obtain a resolution below the diffraction limit
- To obtain higher throughput by exposing only the desired areas

UV lithography in CMi: mask fabrication



Now that we have seen the theory on mask fabrication, let's go to our clean room to see how this is done in practice. We will start with a commercial soda lime plate that is coated with chromium and photoresist and we will see the different steps required to make a mask that we will then use for the UV lithography. Here you see the engineer taking out a mask plank from the black storage box where it was kept during the transport outside the yellow light zones. The user then loads the mask into the cassette of the laser writer.

Now that the mask is inside the tool, we perform a final design check and upload the data with the appropriate settings to the laser writer. The mask plank is now loaded from the cassette into the stage.

The laser then begins to raster scan across the mask in order to write the pattern that was previously created on the CAT system. As the writing progresses you can see the mask coming forward towards the camera. A typical writing time for a 5 inch mask can vary from 5 minutes to a couple of hours depending on the pattern density and complexity. After exposing the resist with the laser, the mask plank is processed by a developer to reveal the resist pattern. Here the user loads the mask into an automatic development tool that applies several programmed cycles of development, rinsing and drying. Once the development sequence is initiated, 2 nozzles successively come into action. The first one that you see coming from the left is applying deionized water and is used to first clean the mask from possible dust particles. Then a second nozzle coming from the right dispenses the developer. By alternating such cycles and managing the wafer rotation, efficient renewal of the developer at the resist surface is ensured in order to remove uniformly the exposed resist. You can now see the wafer rotating at very high speeds; up to 5000 rpm in order to remove all liquid. Observe the concentric rings that appear and fade out as the DI water is dried off. Before etching the chrome, we perform a check using an optical microscope to verify that the resist is correctly developed. Notice that the mask design was mirrored to take into account that we will use it upside down when exposing the wafer in the UV lithography step. Having confirmed that the development was done properly, the user, who wears appropriate protection gear, dips the developed mask plank into a chromium etch bath for 90 seconds. Here this is sped up. After rinsing you can already see that the selected portions of the mask where the chromium has been etched away become transparent. In one of the last steps we stripped resist that was not exposed.

You can in fact see the dark, resist loaded drops of solvent dripping off the mask into the beaker.

After final rinsing and drying, the mask is now ready for UV photolithography.

Practice quiz UV lithography: mask fabrication

Questions:

1. When writing features by direct laser writing you can choose to write your pattern as it appears in the desired design or you can choose to mirror it with axial symmetry. When would the mirroring be in fact necessary?

- When writing a mask, one writes through the glass plate and the design will thus be mirrored when using the mask to expose the wafer. For this reason, one mirrors the design when writing the mask to obtain the correct final features on the wafer.
- When using a UV photomask to expose a wafer, the mask is used with the chromium in contact with the photoresist-coated wafer. For this reason, it is necessary to mirror the design when writing the mask to obtain the correct final features on the wafer.
- A laser writer is optimized to write masks and one should mirror the design if writing on wafers directly, i.e. when doing mask-less lithography.

2. Laser writers are used for the fabrication of UV photomasks because:

- A high power density is needed to pattern the chromium layer on the glass plate.
- It is a good alternative to electron beam lithography, used for lower-resolution features.
- Electron beam lithography is too slow at writing a full mask.
- Because it allows for a dose modulation during exposure in order to reach better resolution.

UV lithography: mask based lithography



This lesson will now focus on the details of UV lithography which is the most widespread lithography technique in microfabrication. It uses UV light as exposure which allows patterning devices at the micrometer scale and on large wafers in a few seconds.

- Alignment and exposure tool
- Contact, proximity and projection
- Resolution limit and enhancement
- UV resists
- Post processing
- Examples

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I will talk about the tool that allows us to align wafers to masks and to control the exposure dose of UV light. Then I will show the three different mask based illumination systems which are the contact, proximity and projection. Then I will recall the limit of resolution and what can be done to enhance it. I show some typical UV resists along with their post processing capabilities and will conclude with some examples. In the previous lesson we have seen how to write the Chrome mask by direct laser writer. We are now using such a mask for the UV lithography. For this purpose we rely on a so called mask aligner shown here, which is a mechatronic equipment that allows the positioning of the wafer with respect to the mask. By means of alignment marks on both the mask and the wafer one can use the microscope and X, Y, Theta stages to align for multiple layer fabrication. This can be done in UV systems at a resolution of about one micrometer. Some tools also allow for back-side alignment which is important for MEMS processing when micromachining of both side of the wafer is needed. The tool allows furthermore controlling the distance between the mask and the wafer for either contact or proximity printing. It then allows for controlling the exposure dose and lamp intensity which will ultimately define the dose on the resist. It is needless to say that such equipment

is one of the most used in any clean room around the world. The picture here shows the UV mask aligner

- Mechatronic equipment
- X, Y, Theta control of Chrom mask w/r to resist coated wafer
- Alignment marks (double-side optics, or Infra-red)
- Control of mask – wafer distance
- Control of exposure intensity and dose (time)
- One of the most used equipment in any cleanroom

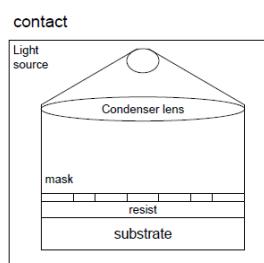


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in our clean room in the yellow light for the lithography section. Two modes of exposure exist for the one to one mask UV lithography, contact and proximity. The only difference between the two modes in fact is that there's either no gap between the mask and the resist or a well-controlled gap drawn here between the mask and the resist. This gap is in the order of a couple of micrometers. Contact exposure yields the best resolution but it may suffer from issues such as mask contamination mask sticking and substrate damage. The minimum feature size called MFS that one can estimate for contact exposure can be expressed roughly by the expression shown here which is thickness d, the wavelength of the light being used, in the square root of the product of the two. To avoid these problems mentioned here in contact mode one can lift the mask a little bit from the wafer and then perform the exposure in this so-called proximity mode. In this case we lose resolution and the minimum feature size can be expressed now by this equation as before, wherever you have to add the gap that has been introduced between the resist and the mask. Again, d is the thickness of the resist the gap (g) and the wavelength of the light source.

- Contact exposure:
 - Mask is in physical contact with substrate
 - Best resolution (diffraction limited)
 - Risk of contamination
- Proximity exposure:
 - Mask is a few micrometers above the substrate
 - Loss in resolution
 - No risk of contamination

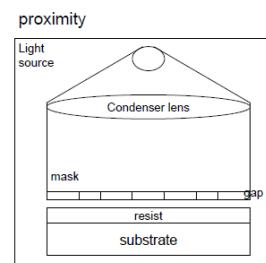


$$MFS = \sqrt{d \lambda}$$

$$d = \text{thickness(resist)}$$

$$\lambda = \text{wavelength}$$

* MFS = Minimum Feature Size



$$MFS = \sqrt{(d+g)\lambda}$$

$$d = \text{thickness(resist)}$$

$$g = \text{gap}$$

$$\lambda = \text{wavelength}$$

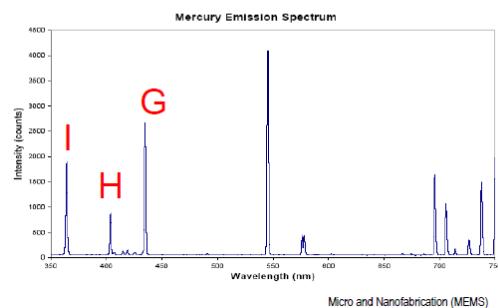
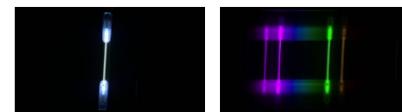
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If one requires high resolution in the order of one micrometer then one chooses the contact mode. If one is happy with the 5 or 10 micrometer resolution one can relax the conditions and work in the proximity mode which preserves the masks and the resist better. One important part in the UV exposure tool is the light source. In fact it is the source that emits the energy of the radiation to expose the resists. We can see here a table that gives an overview of different light sources and what physically is actually behind the light emission, starting from the macro lamp with the different lines and wavelengths. You'll also see the sources for the deep UV, Extreme UV and X-ray lithography. Deep UVs are the industry standard for CMOS whereas EUV and X-ray are future options. Here you can see the light coming out from a Mercury Arc lamp and then separating the radiation into its spectral distribution, we can see the different colors with the, I, H and G lines respectively. For most microfabrication one uses the well-known I line at 365 nanometers. Another

important class of UV lithography is using projection of a mask via an optical magnification system, 4 or 5X times on to the resist. This is the main technique for deep UV and high end semi-conductor systems and reaching clearly sub 20-nanometer resolution.

Wavelength [nm]	Source	Range
436	Hg arc lamp	G-line
405	Hg arc lamp	H-line
365	Hg arc lamp	I-line
248	Hg/Xe arc lamp, KrF excimer laser	Deep UV (DUV)
193	ArF excimer laser	DUV
157	F2 laser	Vacuum UV (VUV)
~ 10	Laser-produces plasma sources	Extreme UV (EUV)
~ 1	X-ray tube, synchrotron	X-Ray

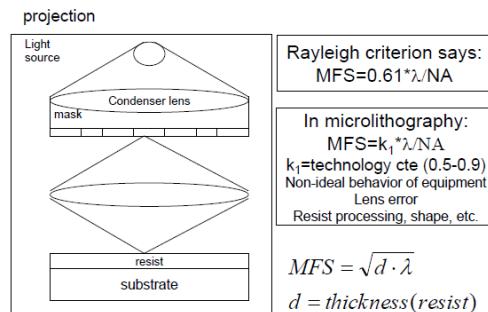


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So here, the picture of the mask is projected by an optical system onto the resist. There's no contact at all when there's no risk of mask deterioration. They are very expensive in fact. The reduction effect not only allows for excellent resolution but also reduces any error in the mask by the same factor. On the down side one cannot expose the entire wafer one to one as shown before but has to take a step and repeat the procedure a couple of times per wafer. The resolution estimate for the minimal feature size is shown here.

- Mainly used today for IC industry
- Picture of the mask is projected
- No contact
- No deterioration
- Excellent resolution (reduction e.g. 4x, 5x)
- Reduction of errors
- Stepper, x-y movement, from field to field



- MFS = Minimum Feature Size
NA = Numerical Aperture

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At this point of the state of the art, the resolution is not anymore given by the pure optical diffraction limit as there are additional technological parameters named K1 or later we see also K2 that help enhancing the resolution. These K factors are linked to the non-linear resist chemistry from design optimization, phase shift mask, double exposure, etc., etc. In optical lithography it is not only the resolution that is important but also the depth of focus, DOF, shown here. Why is that? It is because the resist has a non-zero thickness and to expose a sharp image at high resolution for the entire resist thickness we need to have a large DOF. Resolution and DOF are closely linked together by the wavelength, numerical aperture, and then the technological parameters K1 and K2. So we see for example that if we aim to decrease R to get higher resolution we need to decrease the wavelength, lambda and increase numerical aperture in our optical stepper system

- Resolution R: $R = k_1 \frac{\lambda}{NA}$
- Depth of Focus DOF: $DOF = k_2 \frac{\lambda}{NA^2}$

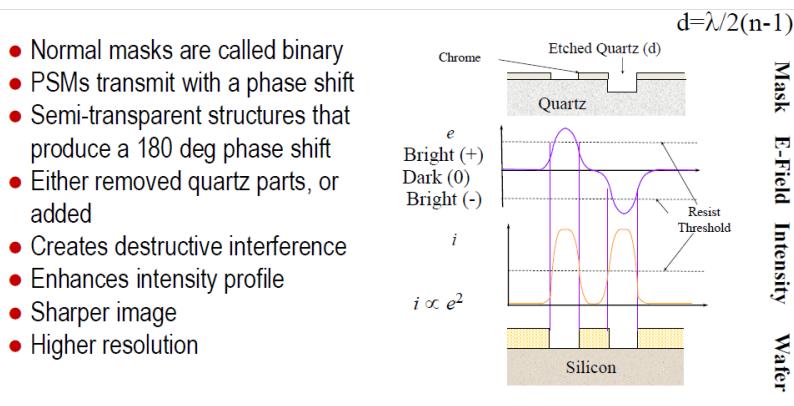
* NA = Numerical Aperture, λ = wavelength

- To decrease R: → need to decrease λ and increase NA (stepper)
- But: DOF decreases too
- → need to decrease k_1
- k_1 = optical engineering = f(resist, mask, illumination)
- Examples: Optical Proximity correction (OPC), Phase shift mask (PSM), Off-axis illumination (OAI)

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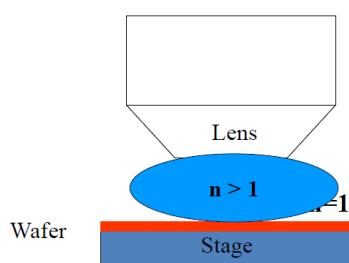
but then DOF decreases too which is not good. The only way to optimize R and DOF simultaneously is to work on these parameters K1 and K2. I will show a couple of examples. Normal masks are binary, Glass and Chrome to create transparent and opaque portions. We have seen the modulation transfer function of such a system just before. Phase shift masks are shown here, they are masks that transmit light with the phase shift at some strategic positions in the mask. To this end, we either remove (like shown here) or add some dielectric materials such as quartz, SiO₂ or similar. By creating 180 degree phase shift between two adjacent transparent parts, we create a destructive interference in the E-field of the radiation and thus improve the intensity curve shown here.



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This allows for creating a sharper image in the resist and ultimately to reach higher resolution. This image shows the end length between the exposure optics and the wafer with the photoresist. It shows the numerical aperture, NA, and how it is defined as the sine alpha times the index of refraction of the medium and the related resolution and DOF values.



$$NA = n \sin \alpha$$

$$R = k_1 \lambda / NA$$

$$DOF = k_2 \lambda / NA^2$$

	Medium	n	λ/n
193 nm dry	Air	1.0	193 nm
193 nm immersion	H ₂ O	1.44	134 nm
157 nm dry	N ₂	1.0	157 nm
157 nm immersion	PFPE	1.37	115 nm

$$R = k_1 (\lambda/n) / \sin \alpha$$

$$DOF = k_2 \lambda / NA^2$$

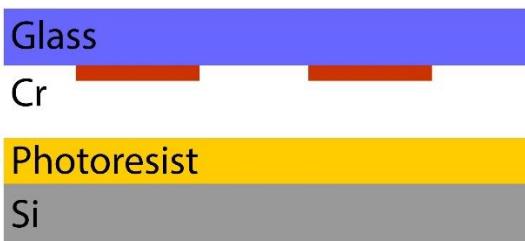
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Immersion lithography is a photo lithography resolution enhancement technique for manufacturing integrated circuits, ICs, that replaces the usual air gap between the final lens and the wafer surface with the liquid medium that has a refractive index greater than one. The resolution is increased by a factor equal to the refractive index of the liquid. Current immersion lithography tools used highly purified water or oil for this liquid, achieving feature sizes needed in current semiconductor manufacturing. In fact, we can see by changing the refractive index one gets another equivalent factor here in the resolution and DOF equation which gives an equivalent shift in the wavelength as a function of the index of refraction.

Practice quiz UV lithography: mask based lithography

Questions:

1. Consider the following mask:



To what tonality of photoresist does this cross section correspond to?



- Positive resist
 - Negative resist
2. Which of the following technique is used to minimize the effect of standing waves in the photoresist?
- Fluid immersion lenses in the laser-writing systems
 - Antireflective coatings between the substrate and the photoresist
 - Decreasing the photon energy of the laser beam
3. When performing exposure with a chromium mask, different gaps may be used between the chromium mask and the resist-coated-substrate. Which of the following statement(s) is/are correct?
- Contact exposure allows for the best resolution.
 - Alignment cannot be performed in contact exposure mode.
 - The resolution achieved in proximity mode is equal to the distance between the mask and wafer.

UV lithography in CMi: mask based lithography

Now that we have seen the theory on mask fabrication, let's go to our clean room to see how this is done in practice. We will start with a commercial soda lime plate that is coated with chromium and photoresist and we will see the different steps required to make a mask that we will then use for the UV lithography. Here you see the engineer taking out a mask plank from the black storage box where it was kept during the transport outside the yellow light zones. The user then loads the mask into the cassette of the laser writer.

Now that the mask is inside the tool, we perform a final design check and upload the data with the appropriate settings to the laser writer. The mask plank is now loaded from the cassette into the stage.

The laser then begins to raster scan across the mask in order to write the pattern that was previously created on the CAT system. As the writing progresses you can see the mask coming forward towards the camera. A typical writing time for a 5 inch mask can vary from 5 minutes to a couple of hours depending on the pattern density and complexity. After exposing the resist with the laser, the mask plank is processed by a developer to reveal the resist pattern. Here the user loads the mask into an automatic development tool that applies several programmed cycles of development, rinsing and drying. Once the development sequence is initiated, 2 nozzles successively come into action. The first one that you see coming from the left is applying deionized water and is used to first clean the mask from possible dust particles. Then a second nozzle coming from the right dispenses the developer. By alternating such cycles and managing the wafer rotation, efficient renewal of the developer at the resist surface is ensured in order to remove uniformly the exposed resist. You can now see the wafer rotating at very high speeds; up to 5000 rpm in order to remove all liquid. Observe the concentric rings that appear and fade out as the DI water is dried off. Before etching the chrome, we perform a check using an optical microscope to verify that the resist is correctly developed. Notice that the mask design was mirrored to take into account that we will use it upside down when exposing the wafer in the UV lithography step. Having confirmed that the development was done properly, the user, who wears appropriate protection gear, dips the developed mask plank into a chromium etch bath for 90 seconds. Here this is sped up. After rinsing you can already see that the selected portions of the mask where the chromium has been etched away become transparent. In one of the last steps we stripped resist that was not exposed. You can in fact see the dark, resist loaded drops of solvent dripping off the mask into the beaker. After final rinsing and drying, the mask is now ready for UV photolithography.

Practice quiz UV lithography: overview photon based lithography

Questions:

1. For a given photolithography equipment, what can be done to increase the resolution?

- Decrease the thickness of the photoresist
- Increase the thickness of the photoresist
- Decrease the distance between the photomask and the resist
- Increase the distance between the photomask and the resist
- Use a lower contrast photoresist
- Use a higher contrast photoresist

2. Let us consider that projection lithography is used to expose a photoresist film. Which of the following measures will increase the resolution?

- Using a phase-shift mask
- Exposing the resist with light of longer wavelengths
- Exposing the resist with light of shorter wavelengths
- Decreasing the index of refraction of the medium between the lens and the resist

3. Assuming a numerical aperture of 0.5 and a proportionality factor $k_1 = 0.35$, which of the lithographic wavelength or wavelength couples are available for the patterning of 180 nm features?

- 248nm and 193nm
- 365 nm
- 436 and 365 nm



After the introduction to the general concepts of lithography, and the details on mask writing and UV lithography techniques, I will now focus in this lesson on Electron Beam Lithography, E-Beam Litho or EBL.

- System overview
- Vacuum levels
- Electron guns
- Electron lenses
- Lens aberrations
- Beam deflection and writing
- Typical tools

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It allows for pattern resolution down to 5 nanometer level. This is important for many devices in nano-science and nano-technology. This lecture will first describe the equipment and then detail e-beam litho specific process steps. This chapter will thus show details on the e-beam litho tool, like the one you saw on the cover slide of this lesson. I will first introduce the main components that are required for an EBL system, starting from the different vacuum levels, show how electrons are emitted by the electron gun, how the electrons are then focused into a probe by lenses and also mention the imperfections called aberrations. Then I will describe how the electrons are deflected and controlled over the sample to write into the resist, and I will wrap this lesson up with some example tools. E-beam lithography is motivated by the possibility to overcome the optical diffraction limit. As we have seen, resolution in optical projection systems is limited to about $\lambda/2$. Of course, industrial Deep UV lithography has developed many process tricks to push the resolution of optical lithography down to a deep sub hundred nanometer scale.

- Why use electrons instead of photons?

- Overcome the optical diffraction limit
- Electron wavelength, De Broglie equation

kV	1	10	100
nm	0.038	0.012	0.0038

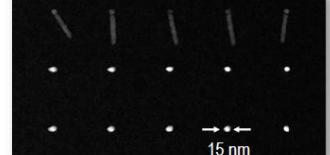
- sub-20 nm features feasible
 - Writing tool for UV/DUV masks
- What are the «cons»?
- Expensive
 - Slow when compared to projection lithography systems

SEM image of two layer lithography with negative resist (HSQ)



V. Flauraud - EPFL

Negative resist (HSQ) pillars 15 nm diameter, 150nm height



V. Flauraud - EPFL

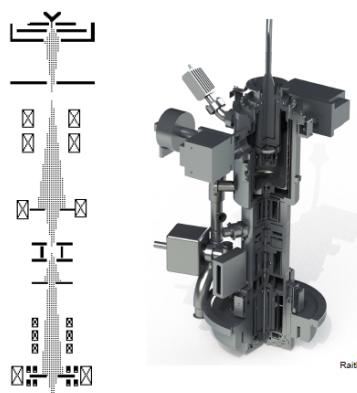
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But these methods can be extremely costly and complex while they still require an original high resolution mask. Instead of photons, we are now considering electrons which are charged elementary particles. Electrons can also be described as a wave with a corresponding wavelength, even by the De Broglie equation that depends on their velocity. The equivalent wavelength of an electron, is given by the Planck constant over the momentum of the electron. So we have a look at some numbers. At 1 kV acceleration voltage, the wavelength of the electron is in the order of 0.038 nanometer, much smaller than an Angstrom. At 10 kV, it gets even smaller below 0.1 Angstrom, and for 1 kV we have already 0.0038 nanometer wavelengths. Typically e-beam is performed between 30 and 100 kV. The effective wavelength of the electron that is accelerated in an e-beam lithography tool is in the order of a few picometers. But unfortunately, the resolution limit using electrons in an EBL lithography tool is not given by its wave properties, but rather by other effects such as beam focusing, electron scattering, and charging and can reach down to a sub 10 nanometer scale in good cases. The main disadvantage of e-beam lithography is the low throughput because it is using a single electron beam to write, and therefore, there are high fabrication costs. Here on the right side you see two nice example images. Here is an SEM image of two layers of HSQ, which is a negative e-beam resist. The scale bar here is 1 micrometer, so these are lines in the order of a couple of hundred nanometers wide, with a varying pitch to check their resolution and alignment capability. This SEM image shows a high resolution and high aspect ratio HSQ resist pattern, which is 15 nanometers in diameter, and 150 nanometers in height. These white spots here are the pillars seen from the top.

- Key components:

- An electron gun
- Electron optics and blankers
- A pattern generator
- A load-lock as the system operates in vacuum
- A high resolution interferometric stage
- An interferometric height measurement



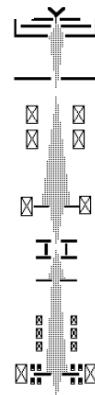
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Whereas these ones are pillars that have collapsed during the last drying process. It shows their width and high aspect ratio of the pillar. The key ability of an e-beam lithography system is to focus a beam of electrons into a few nanometer range, and then to directly write with electrons in the resist a relative displacement of beam and substrate. EBL is therefore a direct write serial technique, similar to laser writing that we discussed

earlier for the mask making in UV lithography. The electrons are first extracted from the gun, and then accelerated towards a series of electron lenses that will focus and correct aberrations in order to obtain the smallest and brightest possible electron beam. Additional features include beam blankers, and beam deflectors. The resist coated wafer is placed on a stage, whose position can be controlled by optical interferometers. The user interacts with a column indirectly via exposure software that controls the hardware's so-called "pedal generator". Samples are loaded and unloaded into a system via a vacuum load lock, not shown on this slide. E-beam lithography requires a high vacuum chamber so that electrons can freely travel from the gun to the wafer. The e-beam column is built inside a vacuum system, like shown here. Different vacuum levels are required for the different parts of the electron column. High vacuum is required at the electron gun region to avoid source contamination by residual gas molecules. Further down in the column, the vacuum requirement becomes less stringent.

- Electron source
 - 1.10^{-10} mbar
 - Ion pump
- Electron optics column
 - 1.10^{-8} mbar
 - Ion pump
- Substrate transfer and stage
 - 5.10^{-7} mbar
 - Turbomolecular pumps



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Ionic pumps are required for the gun and the optics. At the sample level, turbo pumps are typically sufficient. So how can we have different vacuum levels in one chamber? The electron optic section of the EBL tool is almost entirely separated from the sample stage, except for a small aperture called a "differential pumping aperture", which is large enough to let the electrons down the column, but which is small enough to maintain a differential pressure. Note that the high vacuum air does not get sucked through holes like in a domestic vacuum cleaner, because the mean free path of air atoms at low pressure can be many meters, so that they never bump into each other. They just bounce around the chamber and rarely pass through the small aperture. In this way, it is possible to have a poor vacuum in the sample stage region, say 10^{-7} mbar, but a high vacuum, 10^{-8} mbar or better, in the gun, an electron optics part of the column. So lets now have a look at the electron source, also called gun. Different options exist to emit electrons from a metal source into a vacuum. One variation is to use thermionic sources, where the source is heated to overcome the work function to bring electrons into the vacuum. Another way is to use the so-called "field emitters", where high electric potential is applied to the sharp tip. In e-beam lithography, the electron source must combine the two following properties: first, ideally it is monochromatic to reduce chromatic aberrations; second, it has a high brightness and a current stability.

- 2 types of sources:
 - Thermionic
 - Field Emitter
- High voltage
- Maximum beam current
- Electron virtual source size
- Electron energy spread
- Lifetime and stability

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Field emitters fulfill these requirements much better than thermionic sources. So, let's see how a field emitter electron gun looks like. So the cathode, the tip, is at the negative potential with respect to the first anode, which is the extractor, in order to create a high field to extract the electrons from the tip. Between the extractor and the second anode, the electrons are further accelerated. The main function of the suppressor, up here, is to limit electron emission to the end of the tip. This helps to reduce the effective source size and improves resolution. The potential of the suppressor is negative, relative to the tip. Typically, Schottky field emitting guns are used, which are thermal field emitting sources. In such FEG, a single crystal tungsten tip is coated with zirconium oxide, which has the unusual property of increasing in electrical conductivity at high temperature. Zirconium oxide allows lowering the work function compared to tungsten alone. Compared to cold field emitting guns, these guns are less bright but deliver stable high currents and are less demanding in operation. The cathode for field emitter systems is typically a single crystal sharpened tungsten wire.

- Field emitters
 - electric-field driven tunnelling
 - Schottky field emitter
 - High current density
 - 1800° C
 - Energy spread 0.9 eV
 - Source size 20nm
 - Cold field emitter
 - Low current stability
 - 20° C
 - Energy spread 0.22 eV
 - Source Size 5nm

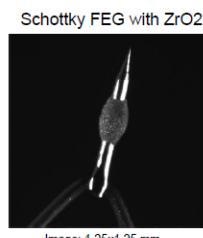


Image: 1.25x1.25 mm

- Thermionic
 - Work function overcome by heat
 - Large source size >20um
 - Low cost

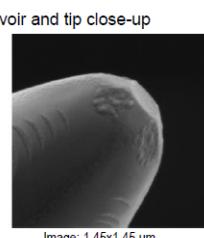


Image: 1.45x1.45 μm

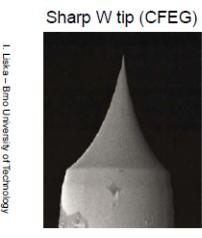


Image: 1.45x1.45 μm

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This allows for virtual source diameters of a few tens of nanometers for Schottky emitters, all the way down to 5 nanometers for cold field emitting guns. Schottky field emitters are ideal for e-beam lithography due to the excellent current stability, which is below 1% probe noise versus up to 10% for cold field emitting guns. They have low current drift, below 1% versus over 5% for cold field emitting guns. And thermionic emitters are typically not used in e-beam lithography due to their large source diameter, energy spread and limited lifetime. The electric field on the tip of a Schottky field emitter is applied to decrease the material working function. For this reason, such field emitters are coated with low working function materials such as zirconium dioxide. Even if the Schottky field emitter is a thermionic emitter, the brightness and the current density are compared with that of a cold field emitter. Here we can see two images of a Schottky field emitting gun. On the left, the zirconium oxide reservoir is nicely seen below the tip. In the central image, one

can identify the crystalline planes of the tungsten tip in the Schottky emitter and for cold field emitting guns, here on the right side, the tip is sharpened to about 100 nanometers. In high electric fields the electrons are thus extracted directly from the tip.

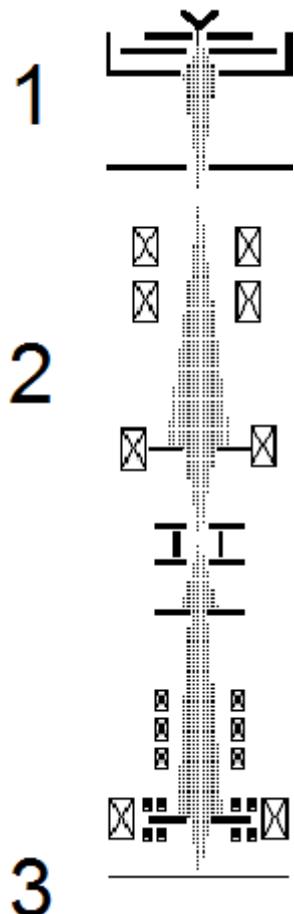
Practice quiz electron beam lithography: tool overview

Questions:

1. Why do electrons allow higher resolution in lithography compared to UV photons?

- Because electrons are smaller than photons and therefore overcome the optical diffraction limit.
- Because electrons are lighter than photons and therefore overcome the optical diffraction limit.
- Because electrons have a larger momentum than photons, hence a lower wavelength compared to photons and therefore can be focused to much smaller spots than optical light in the UV range.

2. The image below is a scheme of an ebeam system. Match the components with the corresponding description.



1:

2:

3:

3. Which of the following statement(s) is/are correct?

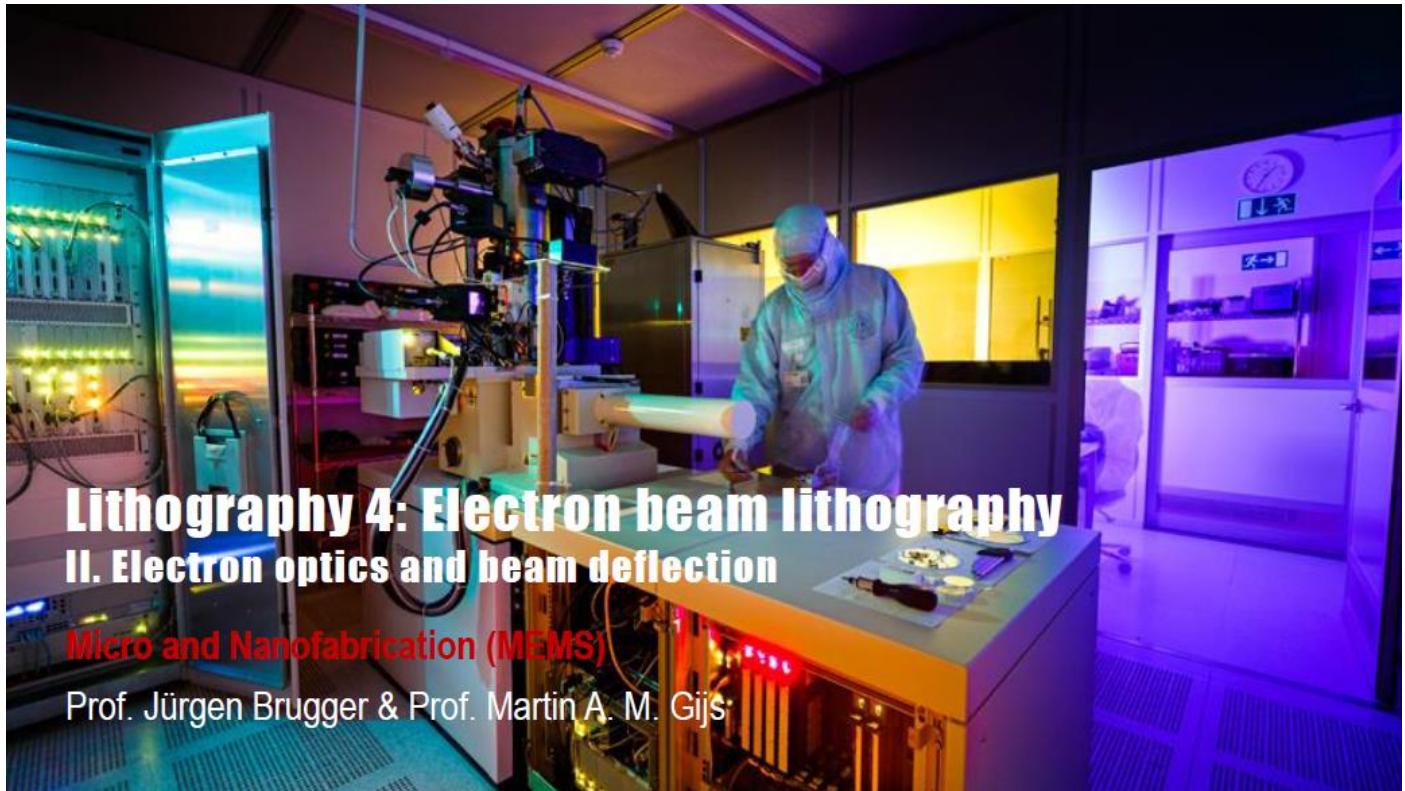
- A differential pumping aperture is a small opening that allows electrons to travel through the electron column while maintaining distinct vacuum levels in different parts of the column.

- Turbomolecular pumps are used to maintain high vacuum and avoid source contamination of the electron gun.
- The long mean free path of molecules at high vacuum allows maintaining different vacuum levels between the column and the sample stage because they rarely pass the connecting aperture.
- The differential pumping aperture allows gradual shaping of the electron beam.

4. Several possibilities exist to emit electrons from a metal source into vacuum. In thermionic sources, the source is

to overcome the work function to bring the electrons into the vacuum. In field emitter a high

is applied to the sharp tip.



So now let's have a look how we can control and focus the electrons. Typically, light in optical systems is focused by dielectric lenses, like shown here. We have here the lens, and if you come with the light... it will focus on the focal point here, further down. Electron trajectory, on the other hand is controlled by electrostatic or electromagnetic lenses, according to the Lorentz force, shown here. And you can see that we can exert a force on a charged particle, either by an electric field or by a magnetic field and the velocity of the particle. Electrostatic lenses are typically used for beam blankers or the gun region. They have a high operation speed, but they have also large aberrations. Therefore, electromagnetic lenses are used for beam shaping. A magnetic lens is formed from two circularly symmetric iron, or some other high permeability material, pole pieces with a copper winding in between. A divergence of the magnetic flux along the z-axis applies a force on the electrons back towards the z-axis, resulting in focusing action.

- $F = q(E + v \times B)$

F = Lorentz force
q = charge
E = electric field

v = velocity
B = magnetic field

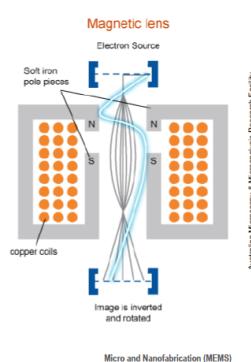
- Electrostatic vs electro-magnetic

- Electrostatic

- Fast but large aberrations
- Ideal for the beam blunker

- Electro-magnetic

- Aberration correction possible
- Electrons spiral through the lens
- Inductance of the magnetic coils limits their frequency response



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The magnetic field also causes a rotation of the electrons and the image about the z-axis in a corkscrew fashion. Although this does not affect the performance of the lens, it does impact the design, alignment and operation of the system. For instance, the deflection system must be rotated physically with respect to the stage coordinates. Also when aligning a column, x and y displacement in the upper region of the column will not correspond to the same x and y displacement at the target. And finally, changes in focus or changes in the height of the sample can cause a slight rotation in the deflection coordinates. This must be properly

corrected or stitching and overlay errors will result. The electron beam may be deflected over a range of typically from a few tens of micrometers up to a millimetre. Writing a larger area requires that the stage is physically moved to reach a neighbouring region and ultimately to write the entire wafer surface. This writing region is called a field that is itself divided into subfields. The main fields correspond to the maximum beam deflection range and if you choose a certain beam step size, the tool can only handle a finite number of pixels. If the step size is too small, then the field size is limited to the beam step size times the maximum number of pixels. Deflecting an electron beam across main fields that are hundreds of microns in size is associated with very large electric or magnetic coils and correspondingly with big settling times due to the larger fields that need to be applied, which at the end will slow down the writing process.

- Typical beam deflections
 - up to 1x1mm at best
 - The pattern must be split into fields to write at wafer scale
- Fields are devided in sub-fields
 - Approximately 10x10 μm in order to avoid large deflections that would be slow
- Beyond one write field the stage is physically moved at the wafer scale
- Field stitching
- Raster or vector scan

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In order to increase writing speed, an additional subdivision of the pattern into trapezium subfields is implemented into the system. These fields are approximately two orders of magnitude smaller and inside them, the electron beam is raster scanned at very high speed by another set of coils. These coils are much smaller due to the small deflection they need to exert and thus, their settling time is also much smaller compared to the main field ones. Beyond fields, the sample is mechanically moved, so a high resolution stage is typically allowed for resolutions below the nanometre. However, mechanical stage drifts result in possible mismatch at the field boundaries known as field stitching. As you will see, different methods exist to manage field stitching and within a single field, different writing strategies are possible. Either raster scanning, like shown here, or vector scanning, like shown here. The raster scanning, one wants to expose the green parts. One raster scans the electron beam and blanks it on and off when it passes over the design area. Whereas the vector scan is that the electron beam is already steered to only expose the area that has to be written. Here we can see an animation of a field stitching approach, where the stage is mechanically moved between two writing fields and where the alignment is very critical. Another strategy involves a fixed electron beam and a continuous stage movement. This way, no field stitching is involved, resulting in continuous patterns, but this method is much slower.

Practice quiz electron beam lithography: electron optics and beam deflection

Questions:

1. In EBL the electron beam can be shaped and deflected by electrostatic and electromagnetic forces. The electrostatic forces are used for:

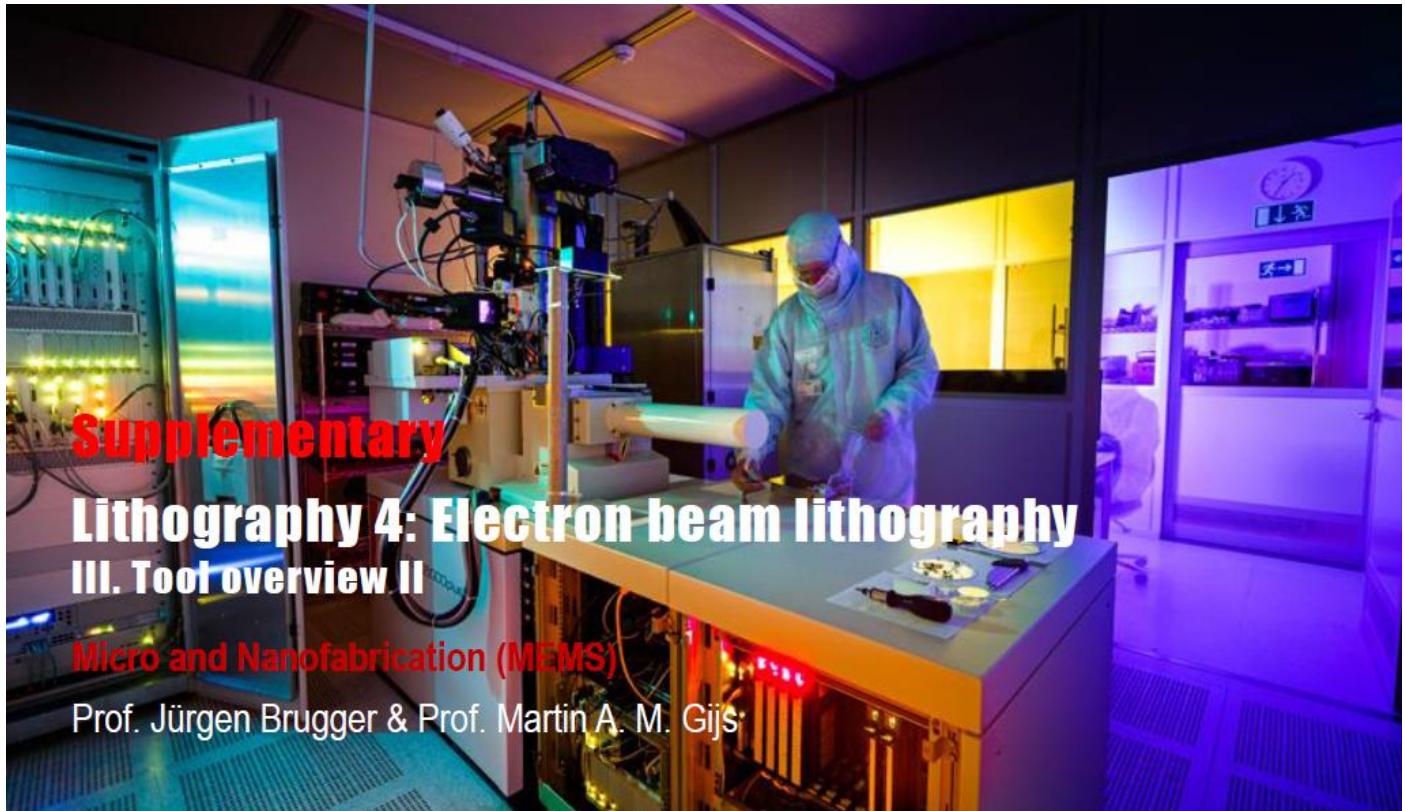
- Beam shaping
- Beam blanking
- Scanning of the beam inside the field write area
- Electron extraction from the gun

2. In EBL the electron beam can be shaped and deflected by electrostatic and electromagnetic forces. The electromagnetic forces are used to:

- Beam shaping
- Beam blanking
- Scanning of the beam inside the field write area
- Electron extraction from the gun

3. When using the writing mode "vector scanning" in EBL, it means that the system ...

- ... will blank the electron beam on and off when raster scanning and passing over the design area
- ... will only expose the areas that need to be written



The electron gun choice has a large impact on the beam diameter, that is also called "probe diameter". As can be seen on the graphs here on the right, different gun types are compared where the probe current

is displayed as a function of the probe diameter for two acceleration voltages, 30 kV here, and 1 kV down here. In EBL, one typically employs currents from a few hundred pico amps range, to several tens of hundreds of nano amps. As seen in the graphs, at these current values, the electron beam diameter undergoes large changes: from a few nanometers to several tens of nanometers. You can also see that these current diameter relations are not linear and they vary largely from one gun type to the other.

- Probe size depends on

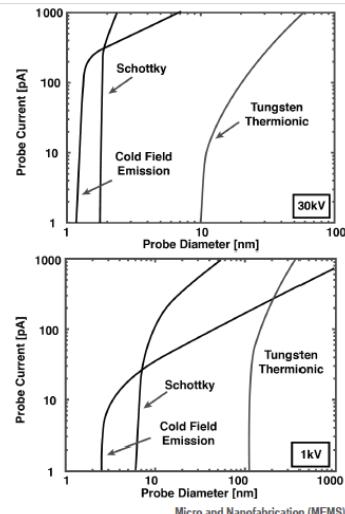
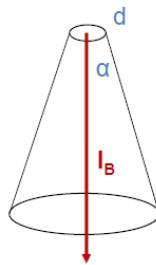
$$\beta = \frac{\text{beam current}}{\text{area} \cdot \text{solid angle}}$$

- Gun type
- Acceleration voltage
- Extraction current

$$\beta = \frac{4 I_B}{\pi^2 d^2 \alpha^2}$$

- Gun brightness β

- EBL writing speed: varying beam properties for different features

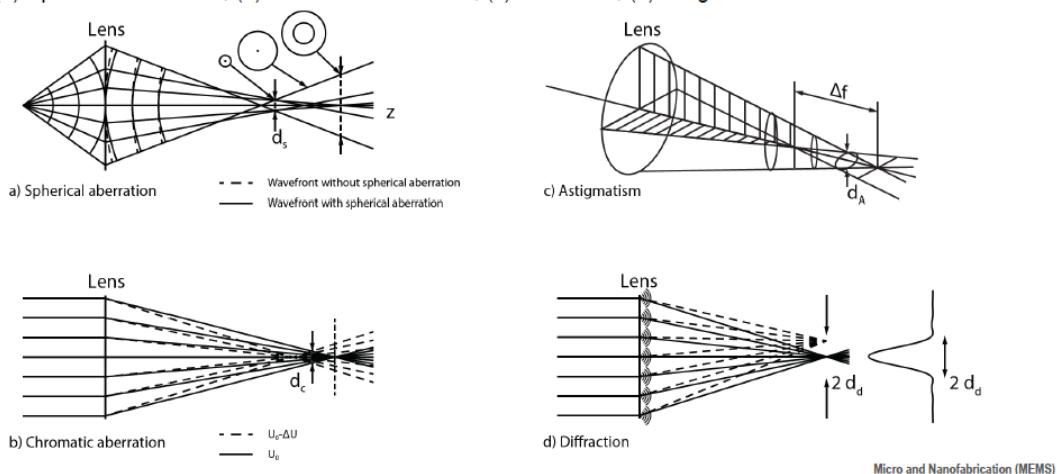


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Therefore, a good metric to compare gun types, is needed and introducing the concept of brightness or beta. It is defined as how much current is emitted per unit solid angle, per unit area of the emitting surface, described in this drawing here. This should be compared at equivalent acceleration voltages and takes into account beam current diameter and the incident angle on the sample. For example, thermionic emitters may have very high beam currents, shown here, but very low brightness, due to their large spot size. It is

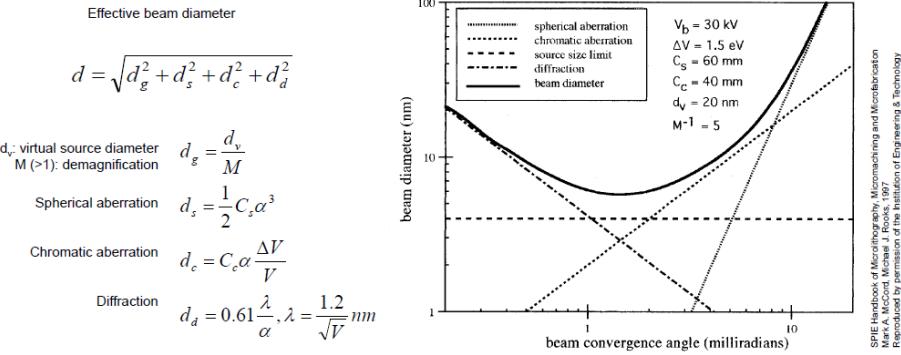
additionally important to be able to tune the electron beam so that one can write large features with a large beam and then use low currents to write the finer features. Like in optical microscopy, a number of aberrations limit the ultimate resolution of the electron probe. There are 4 types of aberrations listed here from A to D. Spherical aberrations (a) are the result of an inhomogeneous focusing property, for electrons travelling on or off the axis. Chromatic aberrations (b) are the result of varying focus for electrons of different energy. Both of these aberrations can be minimized by reducing the convergence angle of the system so that electrons are confined to the center of the lenses, at the cost of greatly reduced beam current. Astigmatism (c) occurs when the electrons sense a non consistent magnetic field as they spiral around the optical x, which arises from construction errors. The result is a non symmetric beam cross-section. At low energies and with convergence angles, altered diffractions (d) may play a significant role, shown here. The understanding of aberrations is essential to reach minimal effective beam diameters that enable high patterning resolutions. As you can see here on the graph on the right side, all the aberrations mentioned previously must be taken into account at once, also in relation with the beam convergence angle. In practice, the effective beam diameter is indeed expressed by the square root

(a) Spherical aberration, (b) Chromatic aberration, (c) Diffraction, (d) Astigmatism



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of each contribution squared and summed. Whereas the virtual source size limit does not depend on the beam convergence angle, this line here. Chromatic and spherical aberrations obviously increase with greater convergence angle. This relation is inverted for diffraction. Reaching an optimal work configuration requires the optimization of all contributions rather than seeking the individual minimization. Notably, and in relation to the previous slides, each aberration and contribution to the final beam diameter are subject to additional parameters other than the beam convergence angle and may be optimized in part independently by the instrument design or choice of acceleration voltage. Electron beam lithography tools for research can be configured in 2 ways: one is to convert a scanning electron microscope SEM, here on the left side, as a scanning electron microscope already includes the main elements required to perform lithography. The only component that needs to be added is the pattern generator. It consists of a beam blanker to switch on and off the beam, as it raster scans the sample, as well as a computer control.



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These low cost EBL systems are typically using acceleration voltages of 30 kV and they do not benefit from the advantages of a dedicated EBL column in terms of speed and stability. So, dedicated EBL tools operate at a higher voltage, up to 100 kV, and allow for high throughput and stability. They have higher costs of several millions of euros - but they are essential and needed for mask writing in deep UV masks and nano-science research.

- Converted SEM*

- Conventional SEM column (30kV)
- Almost no SEM modification
- Add beam blanker
- Add hardware controller and software
- SEM + extra \$100K



*SEM: scanning electron microscope

- Dedicated EBL

- High energy column (100kV)
- Dedicated electron optics
- High reproducibility
- Automatic and continuous (over few days) writing
- >\$5M



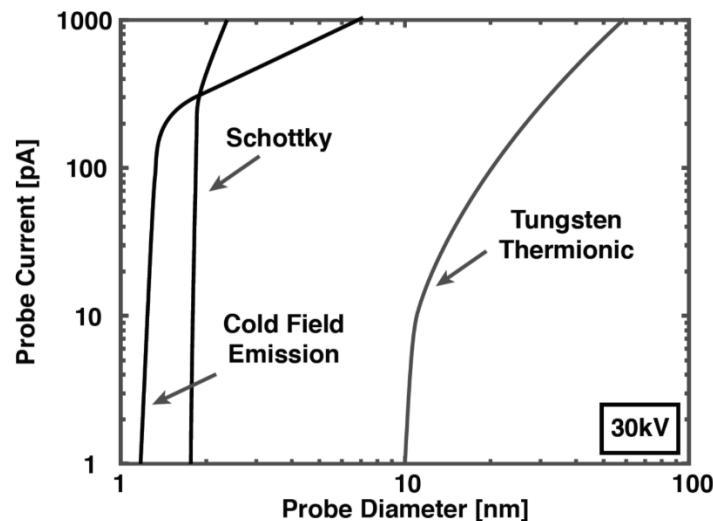
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SUPPLEMENTARY Practice quiz electron beam lithography: tool overview II

Questions:

1. Let us consider a fixed electron beam current of 20 pA and a fixed solid angle of 2π sr. Which of the three gun types provides the highest gun brightness at 30 kV?

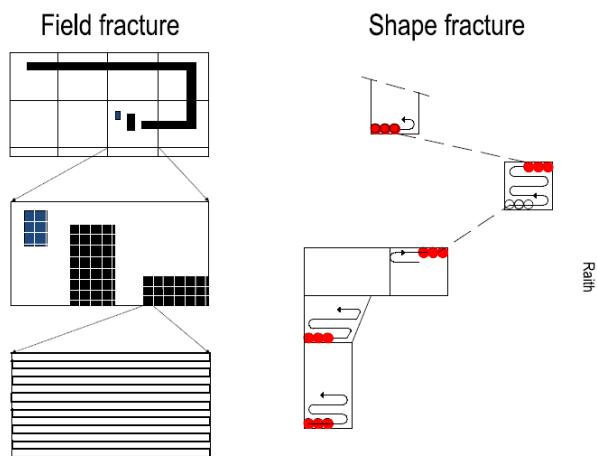


- Schottky
- Tungsten Thermionic
- Cold Field Emission



In this second lesson on Electron Beam Lithography We will now focus on the different processing issues for EBL, that are the design optimization and the writing parameters. Remember that in the previous lesson we have seen the main elements that are required to form a focused electron beam, and how these different elements operate and interact to guarantee efficient scanning of the electron beam on the sample. In the second chapter on EBL, we will now focus on the actual process of writing with the EBL tool and that a user typically follows in the clean room.

- Fracture
 - Conversion from shape to «shots»
- Fracture influences
 - Resolution
 - Line edge roughness
 - Aliasing and discretisation
- Beyond beam step size (BSS)
 - Fracture scheme
 - Shape specific fracture
 - Example: optimise for circles



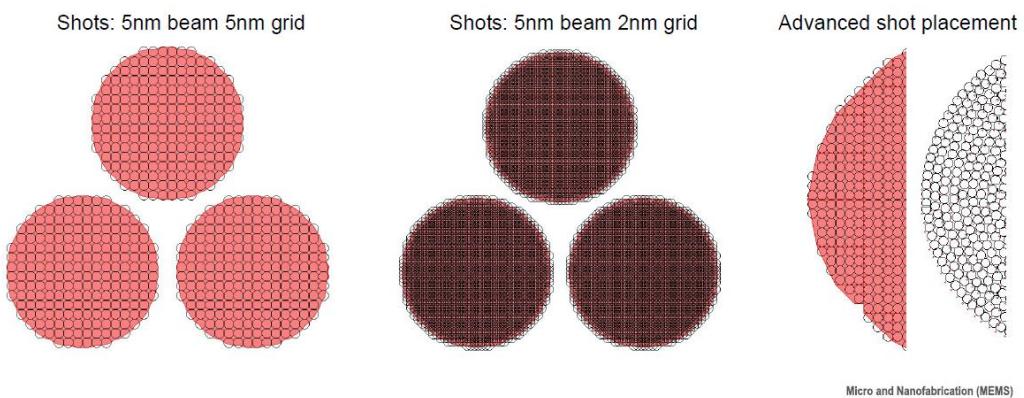
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Starting with the design preparation we will study electron-matter interaction, followed by practical examples of positive and negative resist exposure. We will continue by seeing how proximity effect and alignment procedures are performed in EBL. I will conclude the chapter by showing a few examples that are typical and unique for Electron Beam Lithography. The electron beam is typically of corrosion profile, and is scanned across fields and sub-fields to expose the resist with the desired patterns. Here, we will take a closer look at what truly happens within one of the sub-fields. The CAT design files are typically in .cif or .gts format. The patterns in these files are either fully vectorial or built from n-gons, with a finite number of edges. They must be discretized in a number of basic trapezoids that are filled by shots that will be exposed. This process is referred to as Fracturing. Besides the fracturing of design into shapes and shots, additional steps may be

included at this preparation stage for the EBL writing, in order to specify local design modifications or those assignments.

- Beam step size

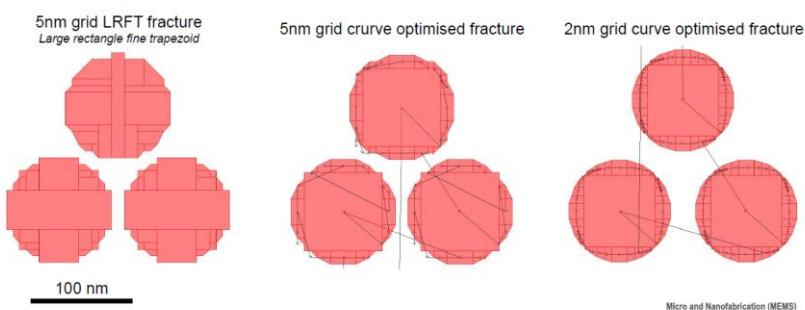


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These details will be presented towards the end of this lesson. The essential principle related to fracturing is the assignment of a physical beam step size BSS, to split the design in individual shapes and exposer shots. Essentially, one must choose a grid size where the e-beam tool will lay down individual shots. The choice of BSS is related to two important considerations: one, the resolution target, and two, the beam diameter. As for the first criteria concerning the design and resolution target the BSS must be a multiple integer of the minimal features for appropriate discretization. The choice of BSS is basically a down-sampling of the vectorial design.

- Shape discretisation and fracture optimisation



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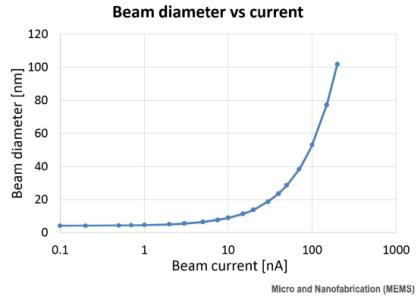
For features that do not lie strictly on the fracture grid this down-sampling may induce aliasing and artifacts requiring a grid size significantly smaller than for simple horizontal vertical lines. The second criteria is the beam diameter. In order to expose patterns with the homogeneous dose the BSS should be equal, or ideally smaller than the beam diameter. If this is not the case, wavy line edges or disconnected dots will be written instead of smooth filled patterns. The left figures here show the black structure that is to be written with the electron beam. Each of the squares represents the sub-fields in which the beam can be scanned quickly. In the sub-fields, there are shapes which are themselves cut into trapezoids, which are shown here, which are here simply squares but can be any trapeze-shapes. Each trapezoid is written line by line, shown here, by the scanning e-beam. The same concept is shown on the right for a more complex shape here the beam jumps from one trapezoid, which is here, to the next one and then raster scans in each of them and jumps to the next one to write the next pattern. Let's start by only considering the effect of BSS alone without taking into account the trapezoid fracture. The goal here on this slide is to expose three round disks with the electron beam. We choose a beam diameter 5nm, but vary the grid size from 5nm here on the left to 2nm

here on the center. We can see step-like artifacts on the edge of the disk at 5nm grid, but less on the 2nm grid, which is obvious. We see that by reducing the grid of 2nm minimizes this effect even though the beam diameter is still the same. An advanced method, shown here on the right, allows for the positioning of the shots beyond an orthogonal grid. This method offers good shape approximation associated with the limited number of shots, but it implies specific

- Beam step size (BSS) and beam diameter (beam current) influence writing time
- Beam diameter/current should be scaled according to BSS chosen when fracturing
- Bandwidth limit for tool (MHz)
 - Minimal exposure time/shot
 - Limits writing speed
 - For small grids time/shot may be too low

$$t = \frac{D \cdot A}{I} \quad f = \frac{I}{D \cdot BSS^2}$$

t = writing time
 D = desired dose
 A = writing area
 I = beam current
 BSS = beam step size



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design preparations. In practice, depending on the position of the features on the orthogonal BSS grid, large deformation may be unintentionally induced by the fracturing of the design into the trapezoids that the tool can write. This may effect the structure symmetry, pitch or overall dimensions and may be critical for the final device. Here on the left, we see a result of a large rectangle fine trapezoid LRFT fracture on a 5nm BSS. In the center, the design was fractured to optimize the structure symmetry in curve-edge approximation. The trapezoids are now symmetric on both axes on the disk. Following the same example as before reducing the BSS further to 2nm improves the disk approximation. Still considering a 5nm beam, this 2nm grid size also benefits from a smoother line edge due to the beam overlap. The black lines shown here, and here, indicate the writing order of the electron beam across the trapezoids. Let's now have a look how the fracture method influences the EBL write time. A total writing area is a major component in the design write time but is not affected by fracture. On the other hand, the direct link between beam step size, beam diameter, and therefore the current, has a large influence on write time.

- Example: how long does it take to write the following matrix?



Choosing the optimum parameters for this design:

- Grid size: BSS = 5 nm
- Current: I = 3 nA, 5.6 nm diameter
- Bandwidth limit of our tool: f = 50 MHz
- Dose: D = 160 μC/cm² (resist dependent)

$$t = \frac{D \left[\frac{\mu\text{C}}{\text{cm}^2} \right] \cdot A [\text{cm}^2]}{I [\text{nA}]} = \frac{160 \cdot 10^{-6} \frac{\mu\text{C}}{\text{cm}^2} \cdot (100 \cdot 2.5 \cdot 10^{-11}) \text{ cm}^2}{3 \cdot 10^{-9} \text{nA}} = 1.33 \cdot 10^{-4} \text{ s}$$

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Typically, beam current may be varied over three orders of magnitude, from 100 pA, to over 100 nA.

Thereby, effectively decreasing write time by the same order. With the beam step size equal to the beam diameter moving from a 5nm to a 50 nm step size will decrease write time by a factor of 100, as we can see from the diameter versus current relation shown here in this graph. When choosing a beam step size for fracture, one usually scales the choice of beam and associated diameter accordingly. In practice, large beam step size and associated beam, therefore allow for faster writing. Another important consideration for the

choice of beam current and beam step size is the EBL tool speed, also called bandwidth limit. It determinates the minimal exposure time per shot that the equipment is capable of controlling. This value is in the range of several tens of MHz. For grid sizes where large shot overlap is desired and where the beam step size is smaller than the beam diameter, the dwell time per shot is too short for the tool capability. Imagine that we want to write the pattern shown here, consisting of one hundred squares of 50x50nm each. We start by choosing the parameters for the experiment. A grid size of 5nm is a good first approach to this design as the minimum feature size is 50nm. Smaller grids would be possible, but would require reducing current and consequently would take longer writing time. The next step is to choose the current and beam diameter. As each fraction of the grid is 5nm the beam diameter should be similar in size to have smooth contours in our shapes. From our tool specification. a 5.6nm beam is generated by choosing a 3nA current. We know that our particular tool has a bandwidth limit of 50MHz. This depends of the equipment, and we are now trying to determine the parameters as close as possible to this limit

$$f [\text{MHz}] = 0.1 \frac{I [\text{nA}]}{D \left[\frac{\mu\text{C}}{\text{cm}^2} \right] \cdot BSS^2 [\mu\text{m}]} = 0.1 \frac{3 \text{nA}}{160 \frac{\mu\text{C}}{\text{cm}^2} \cdot (5 \cdot 10^{-3})^2 \mu\text{m}} = 75 \text{ MHz}$$

Over tool capabilities

- Adjust new current: $I = 2 \text{nA}$, to obtain a 5 nm beam

$$t = \frac{D \left[\frac{\text{C}}{\text{cm}^2} \right] \cdot A [\text{cm}^2]}{I [\text{A}]} = \frac{160 \cdot 10^{-6} \frac{\text{C}}{\text{cm}^2} \cdot (100 \cdot 2.5 \cdot 10^{-11}) \text{ cm}^2}{2 \cdot 10^{-9} \text{ A}} = 2 \cdot 10^{-4} \text{ s}$$

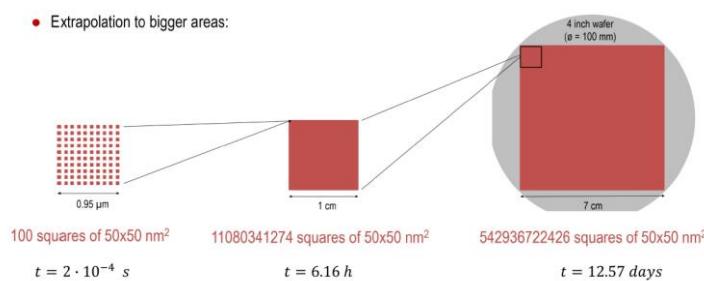
$$f [\text{MHz}] = 0.1 \frac{I [\text{nA}]}{D \left[\frac{\mu\text{C}}{\text{cm}^2} \right] \cdot BSS^2 [\mu\text{m}]} = 0.1 \frac{2 \text{nA}}{160 \frac{\mu\text{C}}{\text{cm}^2} \cdot (5 \cdot 10^{-3})^2 \mu\text{m}} = 50 \text{ MHz}$$

Max tool bandwidth

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to be able to write as fast as machine can do. This is not only because of the time, but also because of the processing cost. The dose speed depends of the resist we are using. For this, typically some dose tests are done to confirm the proper value. With these parameters we now calculate the time, according to this formula. Here it takes $1.33 \times (10^{-4})$ s for the electron beam writing alone. To this time we must add about 30 minutes of pumping, loading, and unloading of the wafer, and the time commuting from one square to the other without the writing. Also, this may seem extremely fast, when scaled to the area of practical designs and full wafer sizes writing may easily reach hours. If we now calculate the frequency with the previous parameters we see that this writing experiment is over the tool capability, as it is over 50MHz that we have defined before. The tool cannot write as fast as we are asking to and it cannot control and blank the e-beam fast enough and we have to adjust the writing parameters. The best alternative we have is to adjust

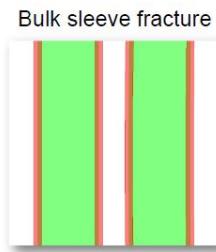
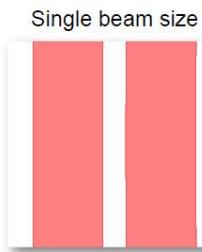
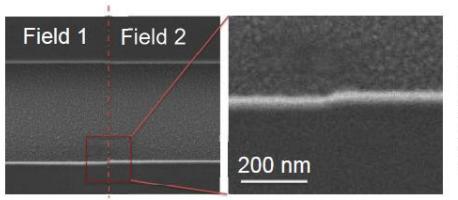


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the beam current, and choose a smaller beam. As you see, it now takes more time than before, but now the frequency is at the maximum speed of the tool. Thus we can write with these parameters our pattern. If you now extrapolate these writing patterns to bigger areas which are more meaningful for applications ,we can see again our small square, hundred squares of 50x50nm square each, takes about $2 \times (10^{-4})$ s,so extremely fast. If you want to write the same density pattern over one centimeter square, of the same density and pitch, we already have to account for more than six hours e-beam writing time, and if you want to write a full wafer of 100mm diameter, with the same pattern density we already have to take into account a writing time of more than twelve days. When preparing the design for writing and before

- Writing schemes

- Field positioning
 - Avoid field boundary in pattern
- Multiple pass
 - Smooth out drifts and field boundaries
- Bulk sleeve
 - Variable grid or beam size
- Writing order
 - Speed, short range accuracy



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considering local dose or design changes, a few other options are important to consider. The first one concerns field placement, although one might intuitively position the fields adjacent to each other on an orthogonal grid, this might result in field boundaries within the pattern that will induce field stitching errors as seen in these images. So, here two fields are stitched together, but they are not perfectly aligned, which is due to the error in the tool drifts and other effects. If the features are smaller than the field size one may allow, so called, floating fields in order to encompass all the features smaller than the field size within single fields. If the designs are larger than the fields writing the structure in multiple passes may reduce the sharpness of the field boundary, due to the random nature of field stitching. As we mentioned, large patterns, when considering advance design preparation, it is important to mention that patterns may be fractured using varying BSS. This may for one, allow the writing of large and small features with different beams to speed up the writing. Alternatively, a large beam may be used for the inner part of the pattern that will be written fast, and a finer beam for the outer part in order to guarantee low edge roughness and overall critical dimensions accuracy. This method is called "Bulk Sleeve", shown here. To use different beam diameter for the center part and to the edge of the structure. Without going into further details, writing order of the trapezoid within fields and sub-fields may play a large role on short-range accuracy and periodicity and consequently will have an impact on the writing time. So this concludes this introduction part for the design preparation and fracture of electron beam lithography, and now we have a closer look at how the electrons interact with the resist to write nano features on substrates.

SUPPLEMENTARY Practice quiz electron beam lithography: design preparation and fracture

Questions:

1. Why are patterns written by ebeam lithography divided into fields and subfields?

- To increase writing speed
- To increase resolution
- To cover areas larger than the beam deflection range by field stitching

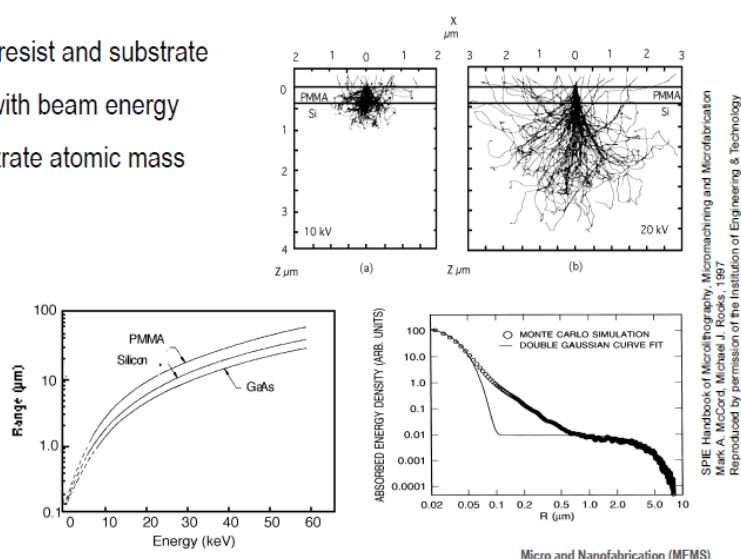
2. Complete the following sentences: The beam step size (BSS) must be a [] unanswered
of the minimum feature in the design for an appropriate discretization. To write smooth patterns the BSS
must be []
or []
than the selected beam size.



In the previous lessons, we have seen how the design is prepared for electron beam lithography, and in particular about the fracturing of the pattern into convenient units to ensure best beam writing quality such as resolution, but also keeping in mind the writing speed. Here we will now see further details on the e-beam lithography in particular how the electrons interact with the resist-coated sample, and what parameters are to be understood and optimized. These are the resist contrast, the various types of e-beam resist, proximity effects, as well as alignment processes. The electrons are accelerated to high energy and are focused onto the surface. As the electrons penetrate the resist, they experience so called "scattering".

- The electron beam scatters into the resist and substrate
- Beam penetration/range increases with beam energy
- Electron range decreases with substrate atomic mass

- Effectively two main contributions:
 - Forward scattering
 - Backscattering

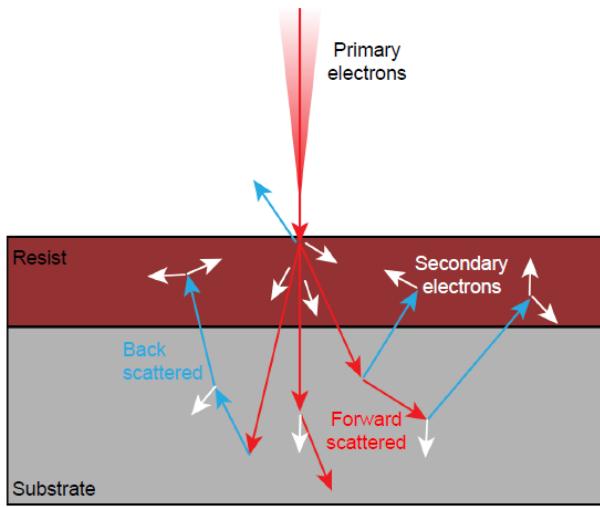


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Forward scattering at small angles occurs to the incoming electrons which tend to broaden the initial beam diameter. When the electrons reach the substrate, they undergo large angle scattering, which also leads to back scattering. The increase in effective beam diameter in nano meters, due to forward scattering, can be given apparently by the following formula. So the forward scattering can be expressed by 0.9

times the resist thickness R_t , over the acceleration voltage, to the power of 1.5. Using the thinnest possible resist and the highest available accelerating voltage can minimize forward scattering. Back scattered electrons may return back to the resist at a significant distance from the incident beam, causing additional resist exposure. This is called the "electron beam proximity effect". The range of the electrons is defined here as the distance a typical electron travels in the bulk material before losing all its energy. The range depends on both the energy of the primary electrons and the type of substrate. So here, on the upper right side, you can see two examples of simulated results showing the distribution of the electrons from the incoming beam, from the top here, that hits the surface, the PMMA photoresist and then the scattering into the resist and the silicone substrate for a voltage of 10 kV and the same is done here for a voltage of 20kV. We can already see that for example, the forward scattering, which is the widening of the incoming beam during the impact is much more narrow for higher voltages compared to the lower voltages. So, if one aims for high resolution patterning one obviously goes to higher voltages to minimize these

- Primary electrons hit the sample
- Forward scattered
 - Small angles
 - Affects most electrons
 - Travel through the resist with high energy
- Some electrons are back-scattered
 - Large angles and high energy, thus large range
- Secondary electrons
 - Ionisation products
 - Have lower energy and penetration
 - Responsible for the broadening of resist exposure



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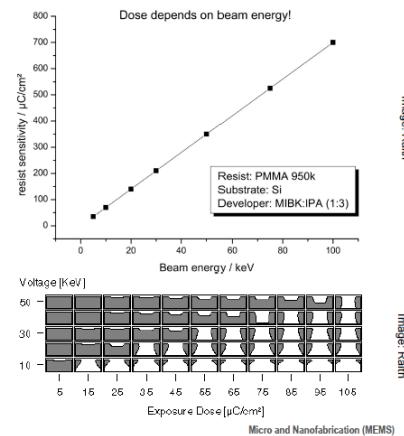
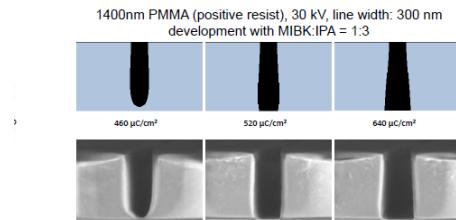
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scatter effects, forward scatter effect, during the impact. On the other hand, please note also that all these back scattered electrons that come out through the photoresist at some further distance location, also cross-link or alter the photoresist, which then will also be exposed which is then called this proximity effect. If we now focus on how the atomic mass Z of the substrate material influences the electron range, for a given acceleration voltage, we obtain the following dependents for gallium arsenide, the lower curve, silicone in the middle and PMMA on top. So as expected, high atomic mass materials show a reduced electronic range. And here on the right side, we see a typical radial energy profile away from the beam impact point. The forward and back scattering are approximated by two gaussians. Please, note that this scale is done in a logarithmic scale. Now let's have a more detailed look at how the path of the incoming primary electrons and generated secondary electrons influence the resist exposure, shown here. The photoresist with the substrate and the incoming primary electrons. Forward scattering at small angles of the primary electrons is the first source of beam broadening. As these primary electrons slow down, much of the energy is dissipated in the form of secondary electrons, with energies that are per definition between 2 and 50 eV, so about three orders of magnitude lower than the primary electrons which are at keV. The secondary electrons are responsible for the majority of the actual resist exposure process. The travel range is only a few nanometers, which results in a slight broadening of the exposed area. These two effects largely account for the minimum practical resolution obtainable in the highest resolution electron beam systems, and contribute to the bias that is seen in positive resist where the exposed features develop larger than the size they were nominally written. Primary electrons may also back scatter at high angles, so in back scattering an electron collides

with a much heavier nucleus which results in an elastic scattering event and the electron thereby retains most of its energy but changes direction. These back scattered primary electrons can travel a long distance away from the beam impact point and thereby they create secondary electrons that will expose the resist quite far away from the intended impact location. This results in the well known white background exposure known as proximity effect. Due to the scattering effect, the interaction volume or exposed zone depends on the beam energy. Indeed, a similar exposure dose which is the total charge per surface

- Scattering implies

- Beam energy affects interaction volume
- The dose to clear depends on beam energy
- Forward scattering affects the resist profile



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delivered at different acceleration voltages results in different lithography results. For instance, at high acceleration voltage the electrons mostly penetrate through the resist with little interaction and require a higher dose to clear. As seen in the cross section images, forward scattering is well visible in the tapered resist profiles. As expected, forward scattering is more pronounced for low acceleration voltages. On the top right, we can see that at higher acceleration voltages a greater dose is needed to obtain full opening of the PMMA after development. High energy electrons penetrate through the resist and scatter in a large volume and thus interact less with the resist than for lower acceleration voltages. At low voltages the interaction volume is limited more within the thin resist layer. In the two figures here below, we can see further illustration of this concept. Additionally from the schematic on the lower right you can see the evolution of dose to clear, as well as the resist profile due to forward scattering. This is shown experimentally from the images on the left. At 640 $\mu\text{C}/\text{cm}^2$ we can see the characteristic tapered angle induced by the forward scattering. For now, let's have a look at the actual resist exposure details

- Sensitivity: dose to clear positive or cross-link negative resist
 - High sensitivity – fast writing
 - Moderate sensitivity – high resolution

$$\gamma = \frac{1}{\log_{10} \frac{D_{100}}{D_0}}$$

γ = positive resist contrast
 D_{100} = dose for 100% resist removal
 D_0 = threshold dose

- Contrast: slope of thickness to dose variation
 - High contrast – high resolution
 - Low contrast – grayscale lithography

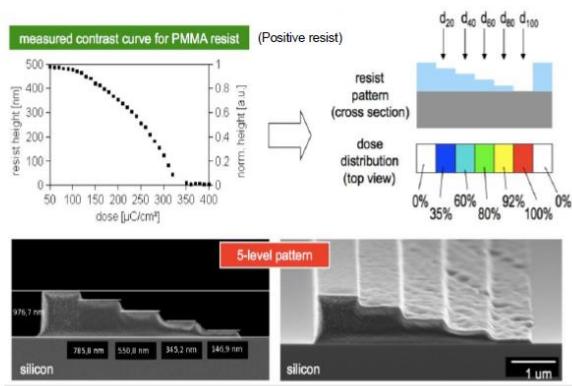


Image: Courtesy PSI, Switzerland
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which are contrast and sensitivity. Sensitivity is the dose needed to fully clear positive or cross-link negative resist. The high sensitivity resist allows for fast writing. On the other hand, most high resolution resists are of moderate sensitivity for the following reasons. When targeting ultimate resolution, an electron beam of

a few nanometer width is used to expose a correspondingly small area. A highly sensitive resist requires only a very limited number of electrons to be exposed. The process is consequently very sensitive to beam shot noise. In order not to be affected by shot noise one typically chooses a lower resist sensitivity so that a relatively large number of electrons are needed for the exposure of very fine patterns. Another important feature of the resist is the contrast, which is defined as the slope of the dose to thickness variation. It is shown here, so D₁₀₀ is the dose to clear, meaning the lowest dose when the resist is fully opened after development, and D₀ is the largest dose where the resist is still not exposed enough to induce a thickness difference after development. In typical processing conditions, high contrast resists are preferred as it is often correlated with resolution. Essentially, a high resolution resist will result in a binary system. The lower dose threshold resist is unaffected, above the dose threshold it is fully removed in case of positive, or cross-linked in case of negative. Although proximity effects may still distort the pattern, higher contrast results allow reduced blurring of the written pattern. Low contrast resists, on the other hand, find interesting applications in grey-scale lithography. As seen here, the low contrast allows for fine modulation of the final resist thickness in order to create out of plane features. One important point to consider is that resist contrast characterizes the full processing of the resist, which with developing playing an equally important role as exposure. So here in the bottom you see two SEM images that show the result of an exposure and developing of a grey-scale 3D e-beam lithography, and we can see here the entire thickness of the resist, which is roughly 1 μ m and then it goes down step by step, 785, 550, 345, and 146 nm. With the low contrast resist, one is able to perform such grey-scale lithography which is not possible with the high contrast resist.

Practice quiz electron beam lithography: electron-sample interactions

Questions:

1. Resolution in EBL is limited by forward scattering of the electrons in the resist. Which of the following measures favor higher resolution?

- Use a thinner resist layer
- Use a thicker resist layer
- Apply higher electron-beam accelerating voltage
- Apply lower electron-beam accelerating voltage

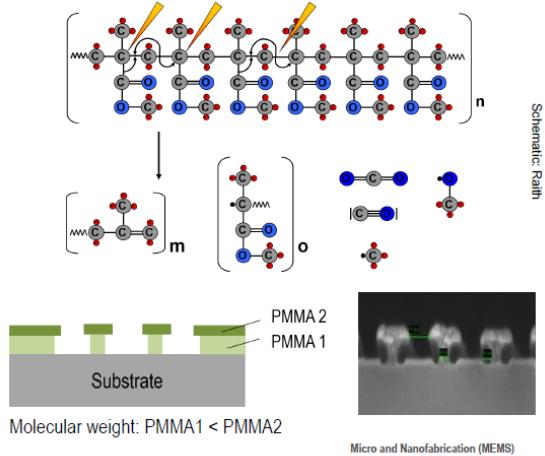
2. In EBL, to realize the highest resolution possible, resists of unanswered

contrast should be used. For grayscale lithography, resists of unanswered contrast should be used.



Let's now have a look at some typical EBL resists. We start with PMMA, that is a positive resist widely used in electron beam lithography due to its high resolution and low cost. PMMA usually provides a relatively low etch resistance but it is an excellent choice for lift-off processes. When an electron is hitting the molecule of PMMA, it breaks the bonds and dissociates the large molecule into smaller byproducts and mono-mass, which are then removed by the developing step. By tuning the molecular weight of PMMA, the resist sensitivity can be fine-tuned to a large extent. Therefore, by coating two layers of PMMA, starting with one of higher and the second one of lower sensitivity, T-shaped undercuts are produced.

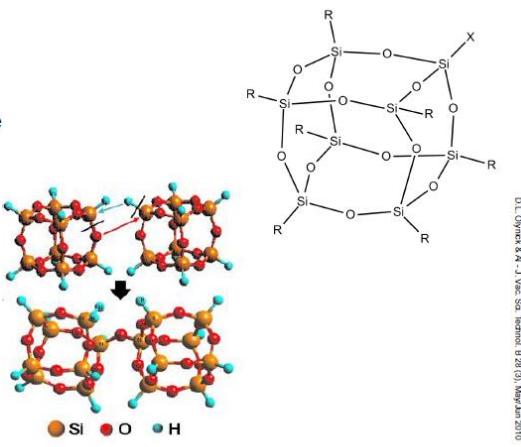
- PMMA (polymethyl methacrylate)
 - High resolution positive resist
 - Various molecular weight
 - Higher dissolution / sensitivity at low weight
 - Bi-layer process for undercut
- Reaction
 - Chain scission upon exposure
- Alternative resist:
 - ZEP, CSAR better mask for dry etching



Indeed, via a single exposure, the chain scission reaction of PMMA after e-beam exposure will produce a wider opening in the first resist layer. This bi-layer process is a standard for EBL based lift-off that guarantees limited sidewall coverage of the evaporated material to ensure a successful lift-off, like shown here in this SEM picture. In the context of positive resists, other alternatives such as CSAR and ZEP provide higher sensitivity and a better etch resistance but to the expense of a slightly lower resolution and much greater cost. HSQ is one of the highest resolution EBL negative photoresists. Its inorganic, cage-like network resembles that of low density silicone dioxide. Upon exposure, HSQ is cross-linked and very resistant to

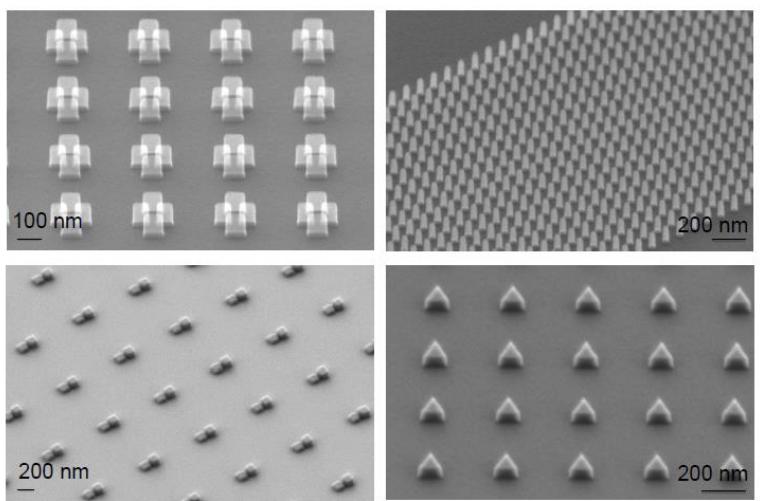
further post-processing, making it an ideal candidate as mask for dry etching. It is interesting to note that the unexposed regions are developed by chemical reaction with NaOH, producing H₂, and not by simple dissolution. Ultimate contrast and resolution is reached in so-called salty developers. HSQ is efficiently removed, or stripped, by diluted HF. All the structures here are exposed and developed HSQ.

- Hydrogen silsesquioxane (HSQ)
 - Very high resolution negative resist (few nm)
 - Inorganic material ($H_8Si_8O_{12}$)
 - Resistant to solvents and O₂ plasma after exposure
 - Well suited as mask for dry etching
- Cross-linking upon exposure
- Developed in base solutions
 - Chemical reaction with NH₄OH or NaOH that produces H₂, not dissolution.
 - Ultimate contrast in salty developers
- Removed in HF solutions



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negative resist patterns, imaged under a tilted angle in a scanning electron microscope. From clockwise from top left, you see first groups of four HSQ fins due to the 20 kV electron acceleration voltage one can actually see through the HSQ structures. The top right image shows arrays of HSQ posts exposed with single electron beam lithography shots. The bottom right image shows triangular arrays of HSQ imaged at 2 kV acceleration voltage. And the bottom left image shows HSQ squares of two different thicknesses done by exposing successively two different layers. Very few lithography processes rely on a single layer alone. Often we need to add a second layer of structured material with high precision to a previous structure, for example to make contact electrode to some nano wires. To this end, reference markers are patterned on the surface. They allow aligning the electron beam in subsequent exposure steps.



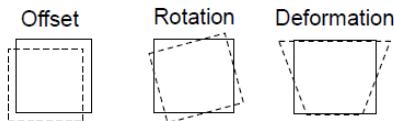
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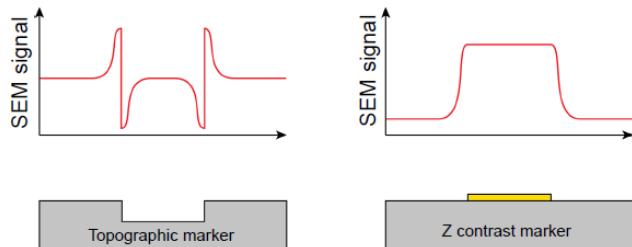
In optical lithography, as you may remember, these markers are imaged by optical methods. The one-to-one transparent mask with the chrome pattern is then aligned mechanically by means of a high precision stage controlling x, y and theta to correct for rotation and translation. In electron beam lithography, the markers cannot be imaged optically, but as we know the e-beam tool is also functioning as a scanning electron microscope, allowing to see the surface. Due to large acceleration voltages and associated penetration depths, the markers, which are 10-20 μm wide, are either etched in the substrate, like shown here, with a

depth of several microns or made of a high atomic number material to provide sufficient contrast. In both cases, the tool finds the marker etch by monitoring signal variation. But not looking at the marker itself but at the edge of the marker which gives a strong signal in the back scattered electron. Also, markers may be large: the typical marker edge detection accuracy is in the order of a few tens of nanometers. Due to back scattering and the search range of the marker these shouldn't be positioned closer than a few hundreds microns from the region of interest to be patterned. Beside the SEM imaging approach, electron beam lithography offers another unique advantage when compared to mask aligner schemes. Indeed, a large number of markers per pattern may be used for redundancy and the patterns may be corrected beyond rotation and translation. The dynamic nature of electron beam lithography allows, for example, for a deformation of the design in order to project it on the base defined by the marker. Well, this wraps up the lesson on electron beam lithography. We have seen the various stages of the process starting from the design preparation, electron resist interaction, various resist

- Processes are inherently multi-layer
 - Reference markers
 - Imaging methods



- EBL as an SEM
 - Markers should provide contrast
 - High topography: etched
 - High Z contrast: metal markers
- EBL alignment corrects
 - Position and rotation
 - Stretches and deformation



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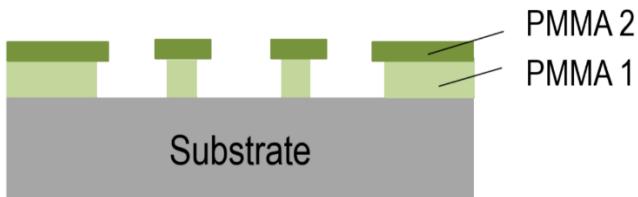
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properties as well as limitations, such as proximity effect, and how alignment is done. In the accompanying exercises, you will have a chance to train your knowledge and apply it to some real application cases.

Practice quiz electron beam lithography: resists

Questions:

1. The goal is to obtain a T-shaped cross-section in PMMA ebeam resist, as shown in the following figure:



To fabricate T-shaped structures using PMMA, one should coat the substrate with two layers of PMMA. First PMMA 1 followed by PMMA 2, then expose and develop the two PMMA layers simultaneously. What kind of PMMA should be used?

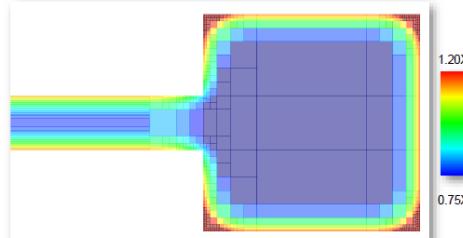
- The molecular weight of PMMA1 should be larger than the molecular weight of PMMA2
 - The molecular weight of PMMA1 should be smaller than the molecular weight of PMMA2
 - The molecular weight of PMMA1 should be equal to the molecular weight of PMMA2
2. In order to write an ebeam pattern that is precisely aligned to a pattern from a previous lithography step, one uses...
- ...high resolution optical interferometers that allow for sub-wavelength distance measurement
 - ...profilometers or atomic force microscopes for the imaging of alignment marks
 - ...electrons that are back-scattered by the substrate to form an image of the markers in the EBL system



We will now have a more detailed look at the proximity effects that are at the heart of the electron beam lithography. As exposure occurs beyond the beam diameter and the impact point, the dose outside of the intended area may be sufficient to expose the resist. If the patterns are significantly smaller than the back scattering range, and uniform in density, this will result in a uniform background dose. Therefore, a simple dose scaling is applied to correct for the unwanted proximity effect.

- Exposure beyond beam diameter
- The dose outside of the pattern may increase enough to expose the resist
- Small patterns of uniform density
 - PEC by adjusting dose uniformly
- Large and inhomogeneous features
 - Requires a pixel per pixel dose correction
 - A model of the beam point spread function is needed

The color scale is the ratio to 50% nominal dose



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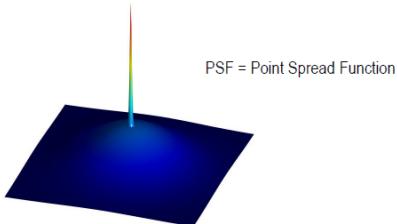
For large patterns, or complex geometries, this is more complicated. As seen in the image on the right, for a large pad in the order of 500 μm size and an associated connecting wire of 100 μm width, the dose is locally adjusted by proximity effect corrections. One can see for example that the dose in the edges must be increased compared to the dose at the center of the square. Red is more dose, blue is less dose. The base of these corrections relies on the modeling of energy distribution away from the beam impact point, which is commonly referred to as the point spread function or PSF. As seen previously, two main effects are responsible for energy distribution in the substrate: forward and backward scattering. The simplest, yet efficient model to approximate the point spread function is therefore a double Gaussian. One Gaussian accounts for forward scattering and depends on the alpha parameter mostly affected by acceleration voltage, and resist thickness. The second Gaussian is defined by beta that accounts for the back scattering

that heavily depends on the atomic mass Z of the substrate and acceleration voltage. A last parameter eta modulates the ratio between forward and backward scattering: if eta = 0, this means that there is no back scattering, whereas if eta = 1, it allows for equal weight of both Gaussians in the point spread function. Eta is here, and here. The 3D plot of a double Gaussian system shows well, the sharp center peak here and the broad background distribution of the back scattered electrons. If one can determine experimentally the alpha, beta and eta parameters, one can compute the effective dose delivered at each shot location, taking into account the background exposure from the neighboring pixels.

- Input parameters: beam model
 - Double Gaussian approximation: forward and backscattering
 - α : forward scattering parameter
 - Lowered with higher acceleration voltage
 - Dependent on resist thickness
 - β : backscattering parameter
 - Reduced with low Z substrate
 - Increased with higher acceleration voltage
 - η : forward/backscattered energy ratio

$$I(r) = \frac{1}{\pi(1+\eta)} \left(\frac{1}{\alpha^2} e^{-\frac{r^2}{\alpha^2}} + \frac{\eta}{\beta^2} e^{-\frac{r^2}{\beta^2}} \right)$$

Forward scattering Backscattering



PSF = Point Spread Function

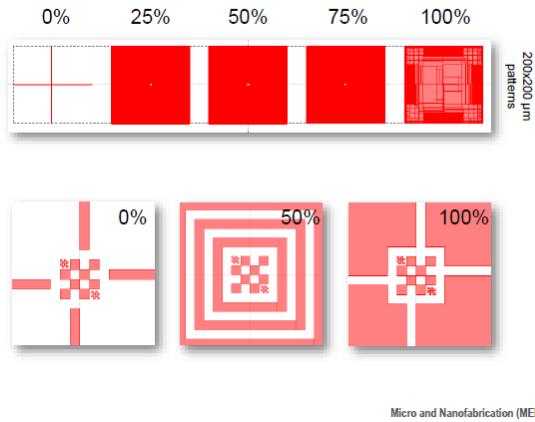
Micro and Nanofabrication (MEMS)

Micro and Nanofabrication (MEMS) , Prof. Jürgen Brugger & Prof. Martin A. M. Gijs

Once this computation is done, the proximity effect correction consists in scaling the dose per pixel to provide a uniform, effective energy delivered on the substrate, regardless of pattern density. In practice, we choose that the 50% density patterns have the nominal base dose and are not scaled, whereas isolated features are corrected to receive a higher dose, while the patterns denser than 50% receive a lower dose. In order to obtain the proper point spread function for double Gaussian approximation, that will allow for the proximity effect corrections, nested structures of different densities are written to isolate the various parameters. While alpha is typically affecting the short range and is difficult to measure, it is in the range of 10 nm to 20 nm at most, beta and eta are more easily determined experimentally. Using standard substrates such as silicon or silicon dioxide on silicon, large amounts of experimental values for beta are available. Different methods allow determining beta experimentally. Here we will focus on eta, because it largely depends on the resist type and can therefore vary widely. The test patterns used our checkerboards, like shown here, the 250 nm squares and 50 nm squares, that provide a good basis for the measurement of critical dimensions. They are surrounded by periodic patterns of varying density with an extent greater than the back scattering range in order to reproduce different background conditions. So this checkerboard is surrounded by zero patterns around, this one is completely filled 100% with writing area and this is a 50% writing area coverage around the checkerboard test pattern. Knowing alpha and beta from literature, the user will run software proximity effect corrections on these patterns for a wide range of eta and will write the patterns for different doses to perform metrology and identify optical proximity effect correction conditions. At 50% density, the effective dose in the central pattern region is not affected by the choice of either. In fact, when performing proximity effect corrections the dose is augmented or reduced for lower or higher densities only. The 50% pattern shown on the previous slide will therefore be used to determine our base dose. Three levels of features allow for the assessment of the base dose: the dimensions of the loading lines, as well as the checkerboards with a square edge length of 250 nm and 50 nm, like shown here.

- Experimental approach

- Nested patterns
 - Uniform density variations
 - Decorrelate multiple parameters
- Dose sweep
 - 50% loading dose
 - Does not depend on Eta
- Eta sweep
 - Check dose scaling vs density
- Convenient metrology
 - 250 nm & 50 nm checkerboard

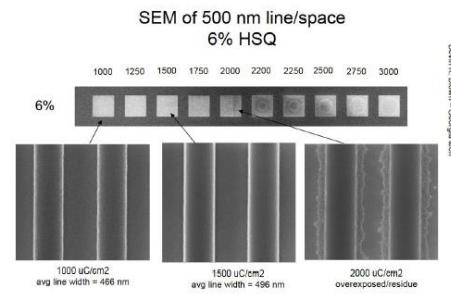
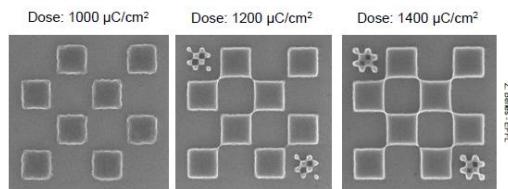


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Let's now look at some real examples using HSQ resist. First, looking at the image at the top right, here the base dose is determined by measuring the line width of the 50% density pattern. When underexposed, 1000 $\mu\text{C}/\text{cm}^2$, the lines are narrow whereas when overexposed, residues of line broadening are observed.

If looking at the central checkerboard one can see that when underexposed, the small checkerboard is absent and gradually appears and widens with the increasing dose. It is important to note that our double Gaussian model is an approximation for the electron distribution during exposure. Additionally, development may be affected by feature size and aspect ratio, and that due to the finite contrast and process latitude of the resist, the perfect critical dimension at all scales may be hard to reach. This is already apparent for the checkerboard pattern between dose 1200 and 1400. At the lower dose, the apertures in the fine checkerboard are well defined, whereas the blanks in the large checkerboard are too large. For the higher dose, the apertures in the large checkerboard are reduced, although still too large, but the fine checkerboard is already showing signs of overexposure. Additionally, we only tune the dose of the written areas but cannot physically apply a negative dose in the non written areas that suffer from background exposure. In a way, we are here limited to a dose leveling rather than a true correction.

- HSQ 6% (negative resist) 150nm thick
 - 50% density base dose
 - Loading pattern line width
 - Fine features: checkerboard



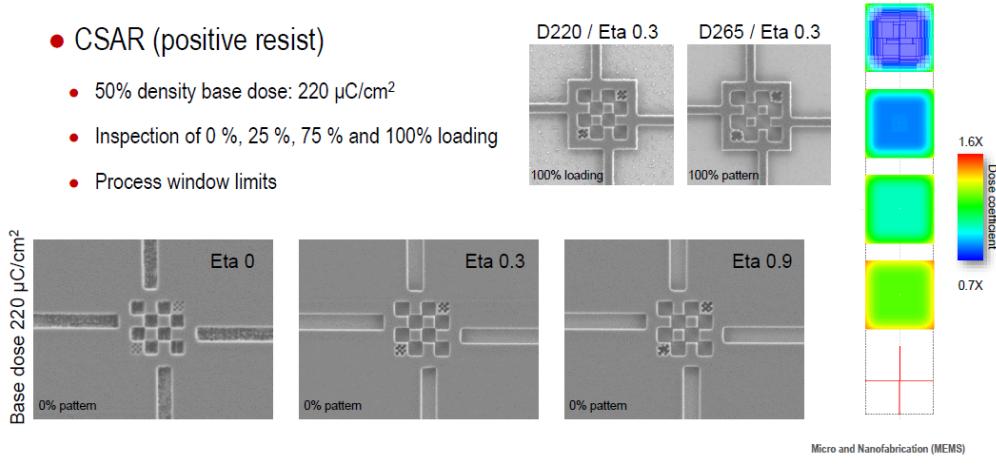
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Once the base dose is extracted from the 50% density patterns, the eta parameter may be investigated.

Let's now have a look at this for CSAR, a positive resist with a base dose of 220 $\mu\text{C}/\text{cm}^2$. Inspecting the 0% loading, one can see that at eta=0 the feature is still full of undeveloped resist, like shown here. At eta=0, hence, there is no compensation to boost the dose for the low density pattern and the resist is therefore underexposed. As eta is increased, a back scattering contribution is assumed and the dose in low density areas slowly rises. At eta=0.3, the fine checkerboard is very well defined, you can see here. By increasing eta

further to 0.9, we can see the collapse of the fine checkerboard and the separation of the large 250 nm squares, slightly overexposed. On the right you can see how the dose correction is applied for the different patterns and associated density. It is interesting to know that if you look at the 100% loading pattern, the eta=0.3 at 220 base dose provides good results on the checkerboard. But the large area written around shows a lot of remaining resist scum.



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Increasing the dose further clears the large areas but the fine patterns are distorted. This is again another illustration of process window limitations. Proximity effect corrections should preferably be performed taking into account the actual density of the target patterns and shape corrections, or bias may be used to further correct the exposure.

SUPPLEMENTARY Practice quiz electron beam lithography: proximity effect

Questions:

1. Electron beam proximity effect depends on both forward- and back-scattered electrons. Assuming a rectangular pattern, how should the dose be modulated?

- Higher dose in the corners than in the center.
- Lower dose in the corners than in the center.
- The proximity effect only affects circular patterns.

2. When performing proximity effect corrections, one needs to determine the base dose that is:

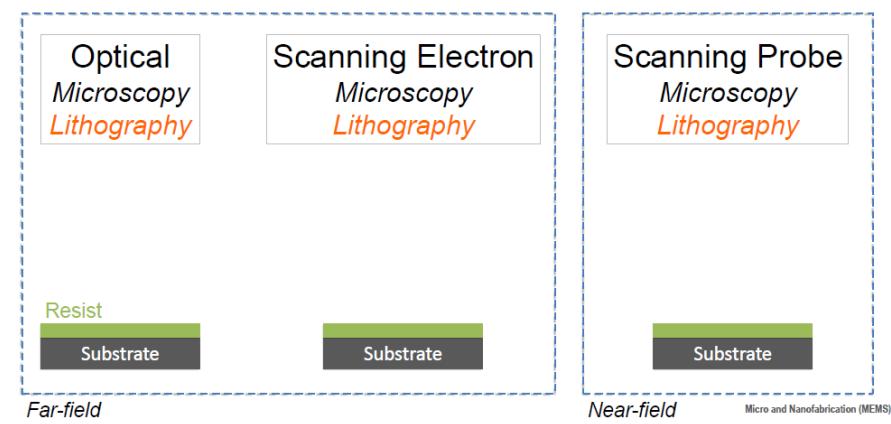
- The dose required to fully clear or cross-link the resist
- The dose at which patterns of 50% density have the nominal dimensions
- The dose at which both high-density and low-density structures present an equal delta to the target critical dimension

3. Considering that you are already working at the upper frequency (=speed) limit of your EBL tool with a fixed beam current, an optimized exposure dose and beam step size for a given pattern. How will the beam step size change if you add proximity effect corrections that will locally increase and decrease the dose?

- The grid increases
- The grid decreases
- The grid remains the same



After the lessons in UV and electron beam lithography, this lesson will show some alternative emerging lithography methods. They offer new functionalities, enable micro nano structures that are otherwise not feasible and allow for rapid prototyping at the nanometer scale. Some of them are also scalable for cost efficient nano manufacturing. I will begin with scanning probe lithography for direct writing. Then I will introduce nano imprint lithography, soft lithography, and stencil lithography for replication. Before looking into these new lithography techniques, let's quickly remind that lithography and microscopy have many similarities. In both cases the main goal is to achieve the best possible spatial resolution, for either imaging or patterning. A lithography tool is often very similar to the tool used for microscopy, with some added features to control the dose of resist exposure for example. In microscopy, we inspect the sample ideally without changing it and in lithography, the goal is to modify the sample so to speak, to write into it.

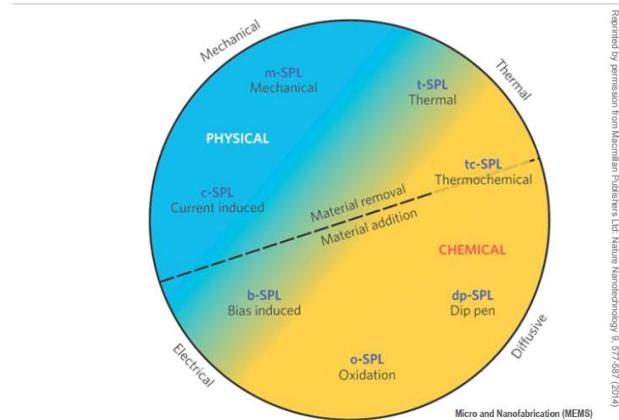


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If we take the equivalent of optical microscopy and lithography we have an optical system with a lens and then our optical beam is focused through that lens system to the surface and the resolution is given here by diffraction limitations, $\lambda/2$. In the case of the scanning electron system for microscopy or lithography, we are using a system with electro-static lenses or magnetic lenses that can focus and control the electron beam that comes onto the resist coated substrate, and then here we have a limitation by

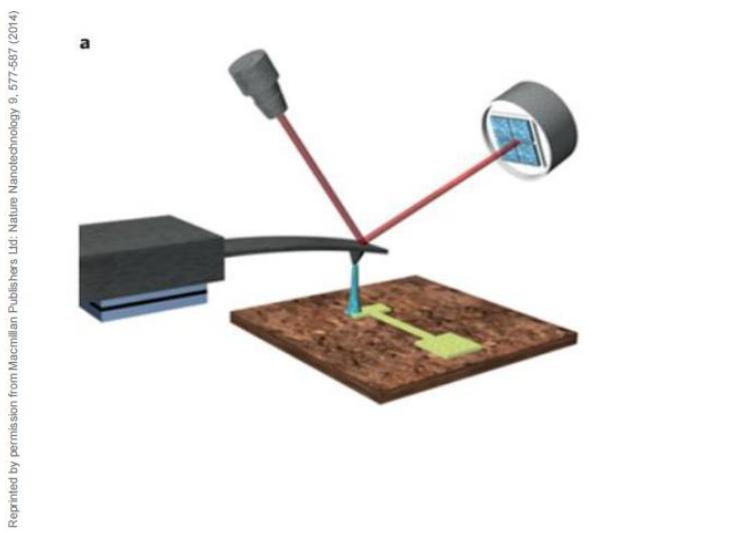
electron scattering and focusing and charging effects. The last example is scanning probes, where we are using a sharp tip on a cantilever, and the resolution of this microscope or lithography as you will see, is given by the near field effect between the tip and the substrate. So these two systems are called far-field microscopy or lithography, because the energy source is coming from far away and is focused on the substrate and the scanning probe is a near-field system, where we are approaching our probe very close

to the surface to interact with it either for imaging microscopy, or for patterning in lithography. Here you see an overview and classification of scanning probe lithography according to the tip surface and the action used for patterning. These interactions can be electrical, thermal, or mechanical. They can also be based on diffusive processes. We can see that there are interactions that are rather physical or chemical, and which can be used to remove material from the surface or to add material onto the surface. So it is evident that there are quite a variety of effects between a tip and the surface that can be used for patterning.



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The illustration here shows the general setup of an AFM based probe lithography technique. You can see the AFM cantilever, the sharp AFM tip, and the laser beam based deflection sensing, to monitor the probe position. What is also shown here is that the material underneath the tip is altered. This is done typically by means of an ultra small capillary liquid cone that exists between the tip and substrate due to humidity effects. Due to this capillary liquid, and eventually an applied bias voltage, one can induce specific and very local electro-chemical reactions that modify the surface material directly for lithography purposes. In such a way for instance, patterned graphene-oxide patterns can be created directly in the graphene film.

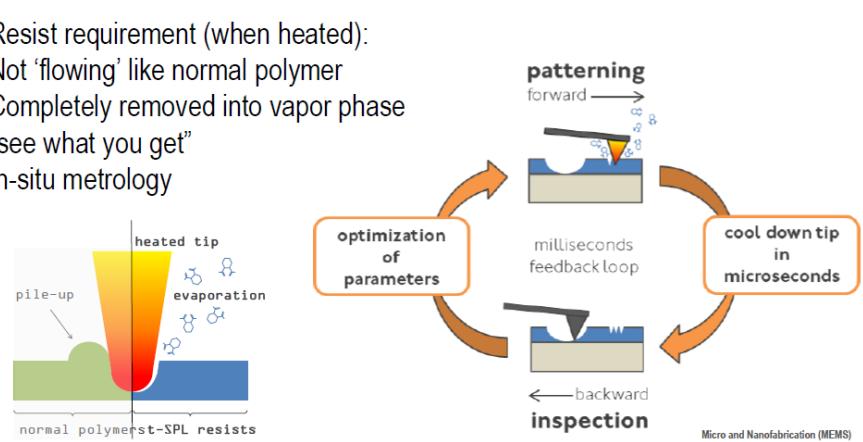


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The previous examples are still on an exploratory level. They have potential as future nano-fabrications as they allow creating patterning directly in functional materials. But they are not easily adaptable for general

purpose lithography that we know so well, using resist layers. Patterning resist however would ease the implementation of these new lithography methods as one could benefit from existing know-how, such as pattern transfer by etching. This is where thermal scanning probe lithography comes into play. Here, a resist is locally removed, which is therefore very close to what we normally do in photo lithography. Let me explain in detail how this works. A nanotip at the end of an AFM cantilever is heated to very high temperatures, up to 800°C or more, by an integrated resistive micro heater and is brought close to a polymer. A normal polymer reacts by softening and can be displaced or piled up under the pressure of the tip as shown here. In case one uses special polymers, that evaporate when brought above a threshold temperature, then the local heat of the AFM

- Resist requirement (when heated):
- Not ‘flowing’ like normal polymer
- Completely removed into vapor phase
- “see what you get”
- In-situ metrology



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will not push the polymer away, but the resist will be completely removed, thereby creating an open pattern in the resist. This resist pattern can then be transferred by an etch step into the underlying substrate material, and the patterning step is completed. The resolution that can be obtained is in the order of 10 nanometers corresponding more or less to the apex radius of the tip. This is the benefit of the near field interaction. It is also a function of the nano probe thermal time constant which is in the order of 10 microseconds. A unique feature of thermal scanning probe lithography is that writing and reading of the pattern can be done hand in hand. Indeed, the integrated heaters enable not only the writing but also the in situ reading and metrology of the written patterns. This allows immediate feedback control, field stitching without the use of alignment markers and the use of pre-patterned structures. Another important difference compared to other lithography techniques is the following. Due to the ablative nature of the patterning process, no development step is needed. Neither are optical proximity corrections or issues



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with electron scattering or electron damage in electron beam lithography to worry about. Here you see an animation of how the thermal scanning probe lithography tool is working. On the top, you see the side view, with the cantilever and thermal sensitive resist, and on the bottom, you see a top view of the scanning

surface. The layout on the left, and the output AFM image on the right. The tool writes line by line. On the way from left to right, the hot tip is writing into the resist, and on the way from right to left, the tip is reading the written pattern. This is repeated line by line, until the 2D pattern has been completed.

Practice quiz alternative patterning methods: scanning probe lithography

Questions:

1. For thermal scanning probe lithography, the main factor that limits the pattern lateral resolution in the resist is...

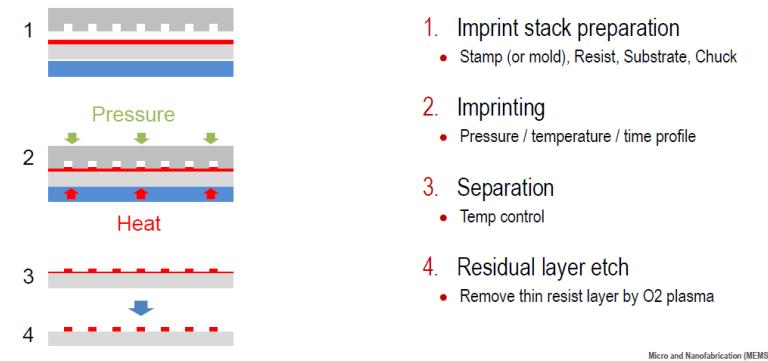
- ...the temperature of the integrated heaters
- ...the thickness of the resist
- ...the apex radius of the tip

2. In thermal scanning probe lithography, why is resist development not needed?

- The resist that has been thermo-mechanically displaced by the tip and will not return to its initial position.
- The heat induced by the tip is above the glass transition temperature and will liquify the resist.
- The local heat of the tip will cause the resist to evaporate, thus realizing the removal of the resist.



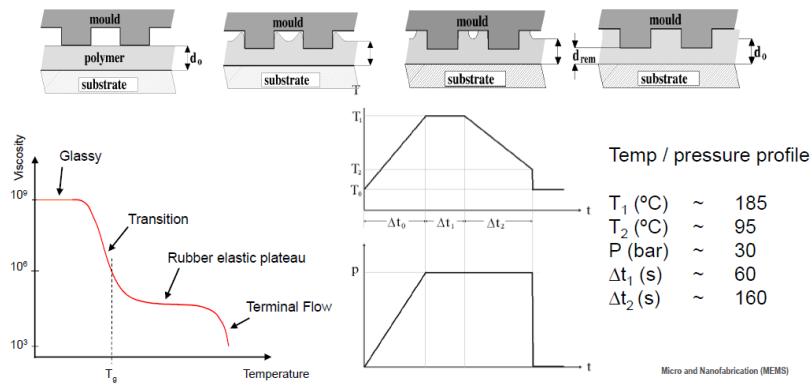
Scanning probe methods are single tip serial techniques. So they are very useful for direct writing and for rapid prototyping, but they are very slow for production. Hence, we will now look at so-called replication methods. The first one I will show is nanoimprint lithography. Nanoimprint lithography, or NIL, is already well advanced and industrialized and even appeared on the semi-conductor road map.



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It was indeed first shown already in the 1990's, that it is possible to directly imprint nano structures, from a stamp into a polymer at the 10 nanometre scale by a combination of heat and pressure. This outstanding achievement has triggered a lot of interest from the scientific and technical communities. It is foremost the simplicity of the imprinting technique that has some striking arguments, despite some serious drawbacks. As conventional photo lithography reaches the feature size limits due to light defraction and scattering effects, nanoimprint being a mechanical technique instead relies on a one-to-one master template that is replicated in an imprinting process. Using a silicon-quartz or nickel or polymer master the nanostructures can be replicated in the imprint tool using the following procedure. First, the template or stamp has to be fabricated. This is typically done by electron beam lithography and etching. Stamp and substrate are then put in intimate contact with each other, as well as with the chuck, in order to get optimal thermal contact to the imprinting polymer. The temperature and pressure is software controlled during the imprint process. This process step replicates the inverse pattern of the stamp by viscous flow of the resist due to the pressure from the

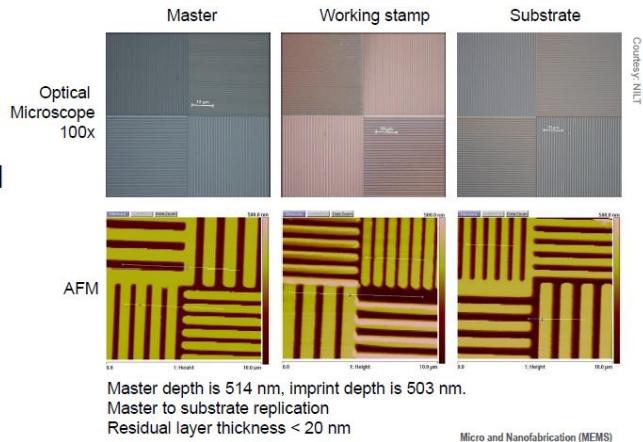
protrusions. Stamp and substrate are separated at the end of the process and the nanoimprint always leaves behind a so-called residual layer of resist underneath the stamp protrusions.



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This layer must be removed by a so-called residual layer etching, before further processing can be done on the substrate. NIL has been shown to deliver excellent results for regular features such as periodic lines for gratings or areas of dots for filters. It is more difficult or impossible to replicate very irregular geometries because of the resist rheology. Here on this slide, we zoom into some details on the molding process and the imprinting process, where we see in particular how the polymer is displaced from the areas under pressure into the stamp cavities until they are completely filled, shown here from left to right. Different stages of the imprint process until the cavity of the mold is completely filled by the flowing polymer. The viscosity of NIL resists depends on the temperature. A typical temperature-viscosity curve is shown here, with the various transition temperatures of the polymer.

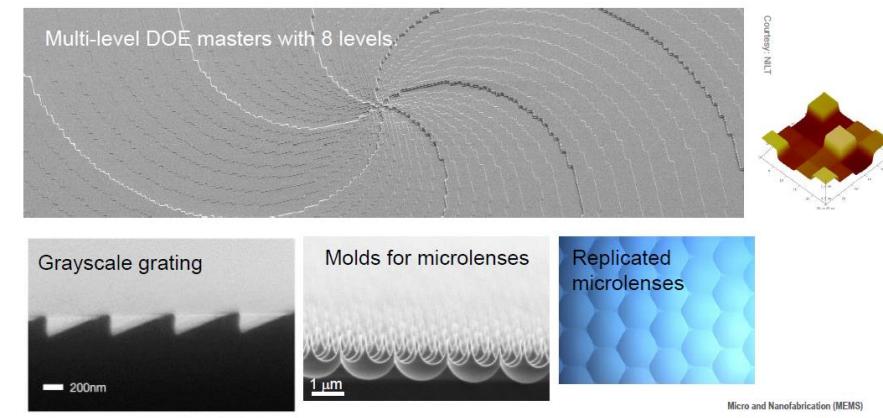
- Master stamp is costly
- Replicate master in working stamp
- Use working stamp for substrate imprinting and for mass fabrication
- Working stamp can be Nickel, Polymer, etc.



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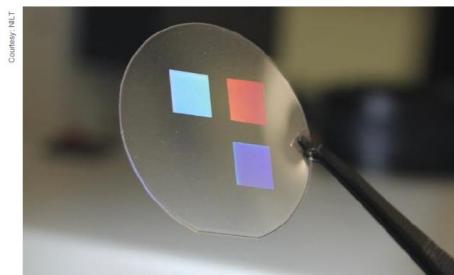
Typical NIL processes follow a well defined temperature and pressure profile, some realistic numbers are shown here on the right side. Please note that some imprinting times can be several hours long. Current R&D is focusing to speed up this step for high throughput manufacturing. Since the making of the first master mold by e-beam lithography is very expensive, one normally replicates it into working stamps. Here on this slide you can see some typical examples of NIL. On the top row, they are 100X magnified optical images taken by a microscope of sub-micrometer test features. The scale bar is 10 micrometers. This shows the master, the working stamp, and the substrate respectively. The lower row shows corresponding AFM images of the master, stamp, and substrate respectively. It shows the very accurate replication from the initial high-resolution master here, over the stamp and the final imprinted product. This is a demonstration of the supremacy of NIL for replication features at a sub micrometer scale, for example for optical effects. Here on this slide, there are some other unique NIL samples such as diffractive optical elements with eight height levels, as shown here. In the bottom images we can see from left to right, a grey-scale grating with extremely

high resolution, and here some molds for microlenses, with the corresponding replicated lenses in polymer. This image shows a photograph of a NIL stamp to be used for optical gratings.



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This is one of the most powerful and beautiful examples where NIL outperforms other lithography techniques in terms of resolution and throughput. One note please, these examples in fact use the NIL stamp to imprint the feature into the surface. There is actually no pattern transfer into a layer underneath, so strictly speaking this should be called nano molding and not nano lithography. In the next section of this lesson, I will introduce soft lithography or micro contact printing. As the name already suggests, there is a soft or a gentle contact between a stamp and a substrate. Soft lithography is a collection of techniques based on printing, molding and embossing using an elastomeric stamp mostly based on PDMS polymer. The key element of soft lithography is an elastomeric stamp, here in blue, with patterns as relief structures on its surface. The stamp is fabricated by casting a liquid polymer precursor onto a master, with the complementary structures. The mechanical properties of this stamp are critical to its ability to transfer a pattern with high fidelity. In principle, any elastomer can be used to cast the stamp, also most work has focused on the silicon based rubber, or cross-linked PDMS.



Large area standard pillar stamp insert.

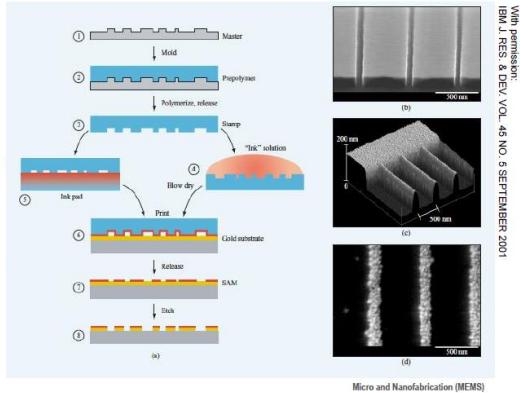
Courtesy: NLT

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The stamp, shown here again, is then inked with a liquid solution containing functional molecules. This can be done either by using a pad, shown here on the left, or by wetting the entire stamp with the liquid ink. The stamp thereby functions like a sponge where the ink diffuses into the PDMS, and later out again. The actual micro-contact printing step is then when the ink is transferred from the PDMS stamp to a surface. Depending on the ink, the print transfer can be done on a thin film of gold or silver supported on a silicon wafer, or on a glass slide, which is shown here. Conformal contact at the molecular scale between the PDMS stamp and the substrate surface is the key to successful transfer of ink molecules from the stamp to the substrate. Micro contact printing is widely used in printing alkyl-thiols on thin films of gold, silver, palladium and platinum and to a smaller extent and with more difficulties of alkyl-siloxanes on silicon and silicon-dioxide or glass. The ink molecules form self-assembled monolayers, or SAMs, on these surfaces during the imprinting process. Here, the thiol-based SAM serves as an etch mask to transfer the printed pattern into

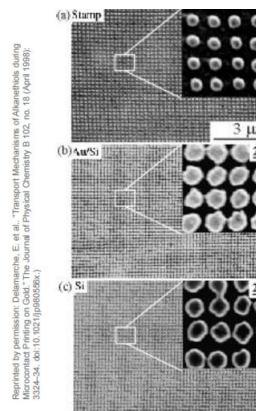
gold. Which then is used as a mask for further etching. The photos on the right show some examples of high resolution soft lithography, with on top here the mold, the stamp, and the final gold pattern, from the top to the bottom. So this slide shows another example of high resolution soft lithography or micro contact printing, here is a SEM image of the PDMS stamp showing a regular area of pillars of 60 nanometers size, which has been used to transfer thiol on a gold surface, which then has been etched in the gold. We can see here that we lose some resolution due to the diffusion of the thiol molecules on the gold surface. And then using a gold pattern to transfer to the silicon we get here the final structure into the silicon.

1. Master
2. Pre-polymer
3. Demolded stamp
4. Stamp inking by pad
5. Stamp inking by immersion
6. Printing on the substrate
7. Forming a SAM
8. Selective etching into layer



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It is a nice example demonstrating how we can get from a relatively low cost PDMS stamp, via printing techniques to the final silicon structures at the sub 200 nanometer length scale. Here on this slide you can see the schematic illustration of a PDMS stamp and two possible problems that may arise due to the softness of the elastomer. One is the lateral collapse of the relief structures or commonly known as "pairing", where the aspect ratio H/L is typically bigger than five. The other problem is called "sagging of recessed structures" with aspect ratio where H/D is smaller than 0.05 during the printing.



- High-resolution μCP:
- Scanning electron micrograph of a stamp with 60 nm dots.
- The corresponding gold dots fabricated by printing and etching were slightly broadened due to ink diffusion and substrate roughness.
- The gold pattern served as a mask to etch the bare regions 250 nm deep into the underlying silicon by reactive ion etching.

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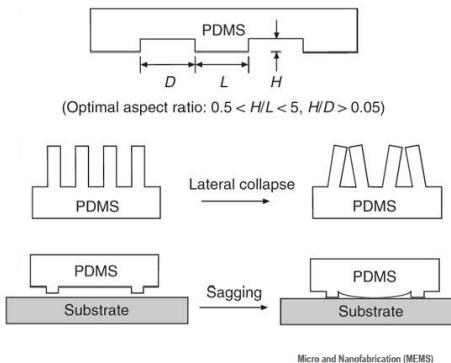
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To avoid these issues one can rely on a hybrid stamp that is made of two different types of polymers with different Young's modulus to have an elastic layer on a more rigid stamp backbone. This is not shown in this slide. This brings me to the last example of alternative lithography which is called "stencil lithography". Vacuum deposition through micro nano stencils, also called "lens lithography", is based on a very thin membrane with engineered apertures that is approached to a surface, like shown here. When using physical vapor deposition, such as thermal evaporation, the flux of the incoming atoms will be partially blocked by the mask and only where the membrane stencil has apertures, atoms can reach the surface. This allows creation of metal patterns without the use of photo resist and associated process steps such as development and baking. It is therefore applicable to virtually any surface and substrate material. Stencil lithography is a convenient way to directly fabricate nano wires and their contact pads. For this, a so-called "dog bone geometry" is often used as shown here on the left side. PVD of a conducting thin film material directly creates

the nano wire without any additional process steps such as developing and baking. Thus reducing the risk of contamination, which may affect the electronic transfer property in the nano structure. It does allow studying new materials for this type of devices without the need for electron beam lithography for the final step. Here on this photo we can see an SEM of a stencil with the nanowire slit and the two openings for the contact pad and the corresponding metallic nano wire, shown here with the bigger contact pads that can then be interfaced with some probe systems.

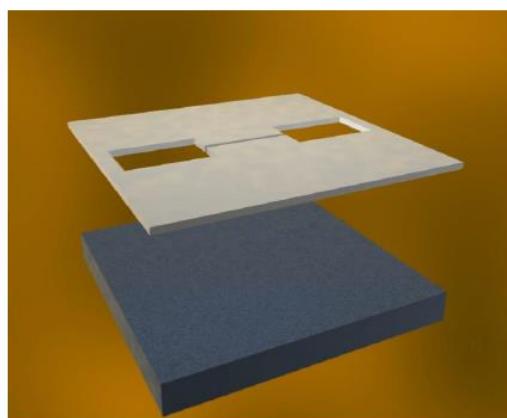
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- Possible problems and limitations
 - Aspect ratio of stamp features
- Lateral collapse
- Sagging



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And here is a typical resistivity curve of a metallic nanowire as a function of the cross section, anti-length. Stencils are fabricated by UV or e-beam lithography and aperture etching in a very thin silicon-nitrite membrane. Shown here, in red-ish. This image shows a 100mm sized wafer stencil containing hundreds and thousands of micro nano apertures. Such stencils can be reused many times. Challenges are the stencil's mechanical robustness, aperture clogging, and membrane stress issues, as well as alignment overlay. Please have a look at the accompanying references for more details. For creating small structures with sharp edges, the best deposition method is the physical vapor deposition technique, which has a long mean free path, such as thermal, or e-beam evaporation which occurs, as we remember, in high vacuum.

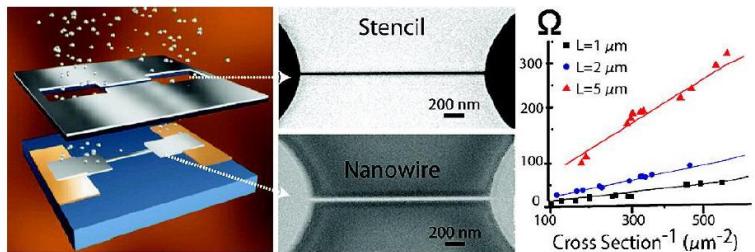


Direct fabrication of nanostructures
without resist.

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This figure shows the geometry during the stencil lithography with the dimensions and locations of the source, the stencil apertures, shown here, and the substrate. Assuming line of sight deposition, straight lines, one can predict very precisely the pattern as a function of the various parameters. Another contribution to the pattern widening is not only geometry, but also the surface diffusion of the arriving thermal atoms. From this observation it becomes obvious that highest resolution can be achieved by placing the stencil very close to the substrate, and by placing the emission source as far away as possible. Stencil lithography is not meant

to replace conventional lithography, but it has some attractive assets for particular cases, as summarized here. In all these cases, normal lithography in fact is not possible. The left image shows how sub micrometer gold dots can be deposited directly on organic, self-assembled monolayers on a SiO₂ substrate, which is an important layer for organic electronic devices. These are the gold dots directly on the SAM patterned through the openings of a stencil.

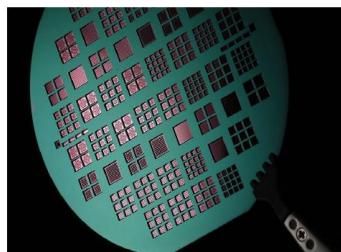


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O. Vazquez et al. Nano Lett., 2008, 8 (11), pp 3675–3682

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The middle example shows nano structures directly deposited on freestanding MEMS cantilevers which is otherwise difficult, if not impossible, to pattern because resist coating on a freestanding mechanical device is hard to realize or impossible to make. Here, one can see gold nano dots deposited on an AFM cantilever and the AFM tip.

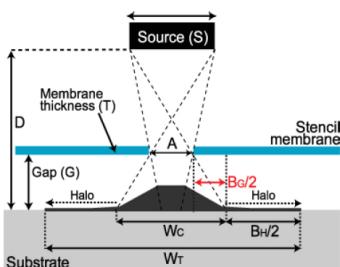


- 100mm size wafer stencil for high-resolution shadow-mask technique
- Aperture resolution down to ~ 50 nm

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The right example shows stencil nano structures that are directly and locally deposited onto a CMOS circuit without the need for resist chemistry and temperature steps.

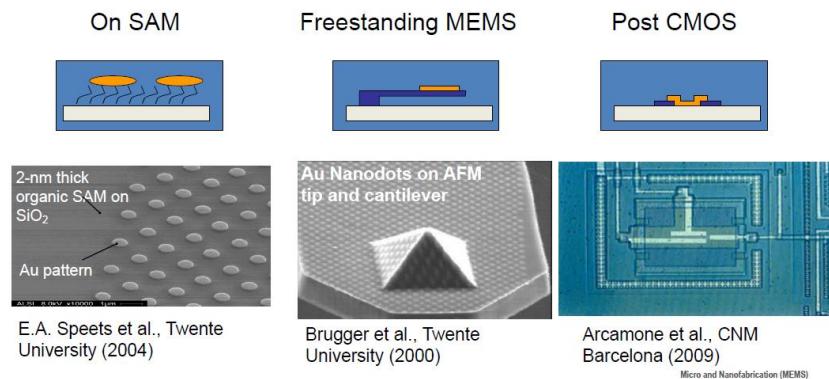


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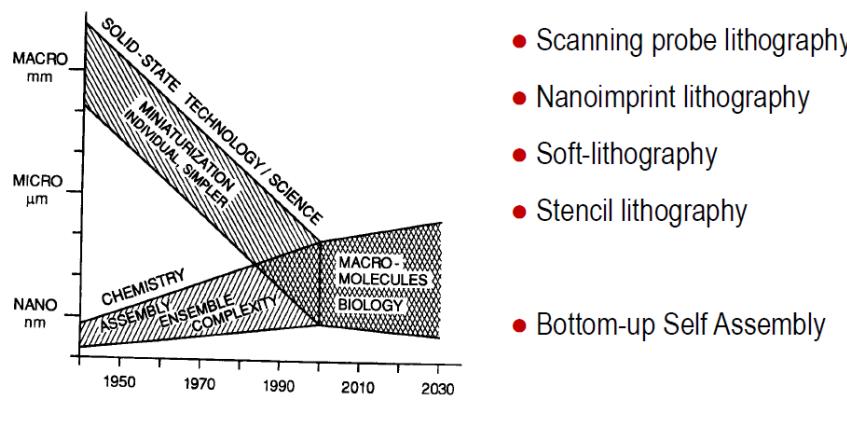
This allows for post-processing highly sophisticated CMOS circuitry by locally adding metallic or other material nano structures. This concludes this chapter on alternative and emerging lithography. We have seen

direct writing using scanning probes and the replication using soft stamps, nano imprint stamps and vacuum stencils. Please note that all these methods are so-called "top down patterning".



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They are approaching the length scale of resolution in the order of 10 nanometers to overlap with so-called "bottom-up self assembly" where molecules and nano particles are using natural forces for creating ordered structures.



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SUPPLEMENTARY Practice quiz alternative patterning methods: replication methods

Questions:

1. Nanoimprint lithography (NIL) often faces the issue that the stamp adheres to the resist and cannot be detached. What measure can be taken to assist detaching the stamp from the resist after the imprint replication step?

- Oxygen plasma of the stamp or mold
- Silanization of the stamp or mold
- UV curing of the resist
- Hard bake of the resist

Conclusion and summary

In this chapter about lithography, you have learned the physical principle, the different setup configurations as well as the advantages and limitations of the two main lithographic techniques which are either based on photons or electrons. You were also introduced to alternative patterning techniques such as scanning probe lithography. Here are a few important key points you should remember.

General concepts

- The principle of lithography is based on the local modification of the sample often via the exposure of a resist.
- A resist and process are characterized by contrast and sensitivity.
- There are positive and negative resists.

UV lithography

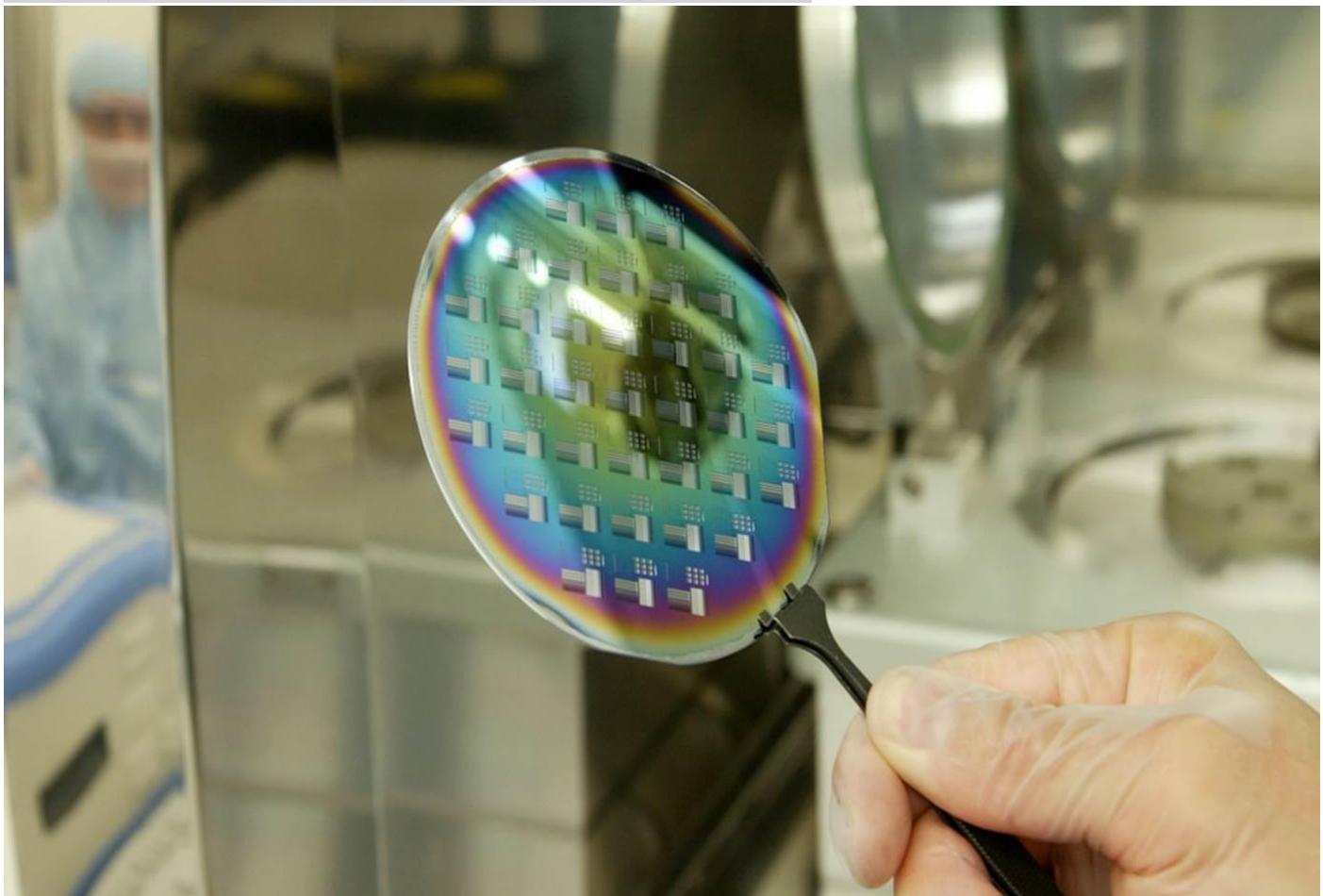
- The fundamental step of UV lithography relies on the fabrication of a mask by serial writing, often by scanning a laser.
- Exposure through masks allows for high throughput with the exposure of full areas at once.
- Different exposure wavelengths are available to expose photoresist with different spectral sensitivities.
- Various techniques such as phase shift or immersion allow to push the resolution of optical lithography further.

Electron beam lithography

- By using electrons one can reach resolutions far below the optical diffraction limit down to few tens of nanometers in practice.
- Electromagnetic lenses are used to shape the electron beam.
- Alignment in electron beam lithography is based on the same imaging approach as in a SEM.

Alternative techniques

- Scanning probe lithography allows 3D patterning.



Introduction and objectives

Dry etching (DE)

This module on dry etching describes etching in a gas environment. We will introduce etching directionality and anisotropy and give a few simple rules for choosing dry etching processes for specific materials in a plasma reactor and provide theoretical concepts that characterize a plasma in a dry etching equipment. We will discuss current dry etching reactors and ion beam etchers; in the latter, the substrate to be etched is not located within the plasma, but subjected to a beam of ions. We will present also dry etching processes that use intrinsically reactive gases and that do not require to have the gas in the plasma state, which leads to a significantly simpler etching system. We will finally give examples of specific dry etching processes for silicon dioxide, silicon nitride, silicon, polymers and metals.

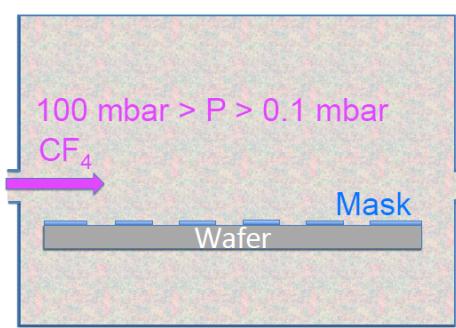
At the end of this week, you should be able to:

- Know what a plasma is and how directionality of a dry etching process and etching anisotropy, that is a stronger etching rate in a direction perpendicular to the substrate than parallel to it, can be obtained.
- Know dry etching processes that are not based on creation of a plasma, but merely on exposure of a substrate to vapor of a reactive gaseous compound.
- Theoretically describe a plasma in a dry etching equipment and understand how RF electrodes couple electrical power into the gas to maintain the plasma.
- Know main dry etching equipment and plasma sources that are used in modern dry etching.

- Know the technique of ion beam etching, in which the substrate to be etched is not located within the plasma, but subjected to a beam of ions that are generated in a separate environment within the etching reactor.
- Know of specific dry etching processes for silicon-based materials, like silicon dioxide, silicon nitride and silicon itself, and organic materials as well as metals.



In this lesson, we will introduce dry etching in a gas plasma. A plasma is defined as a collection of excited gas molecules, ions, and electrons. Excitation is obtained by applying a high voltage inside the reactor via electrodes, which leads to ionization events in the gas. We will then introduce the directionality of the dry etching, and the etching anisotropy.

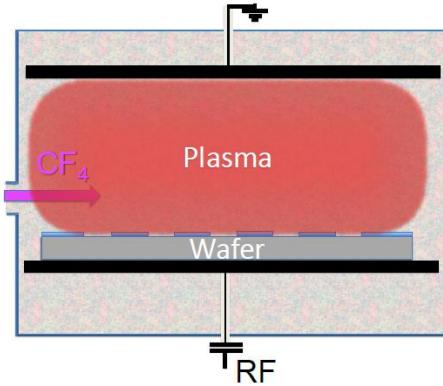


- Etching is done by molecules in the gas (=dry) phase, typically in the 0.1-100 mbar pressure range
- A mask locally protects the wafer from etching
- Example: chemical etching of Si in carbon tetrafluoride (CF₄), an inert fluorocarbon gas
- It becomes a reactive gas when brought in the plasma state

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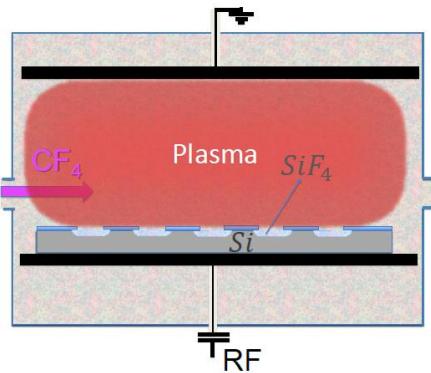
That is the ratio of the etching rate in a direction perpendicular to the substrate, and parallel to it. Finally, we will give a few simple rules for choosing dry etching processes to etch specific materials. In a dry etching process, etching is done by molecules in the gas phase, which is the so-called dry medium, and one is typically in the 0.1 to 100 millibar pressure range. The wafer is positioned in the reactor, which is subsequently filled with the gas. An etching mask locally protects the wafer against etching. A typical gas that is used in many of the processes is carbon tetrafluoride, or CF₄.



- Chemically reactive fluorine radicals are produced in a plasma upon impact on the CF₄ with an electron e⁻ from the plasma
- $$CF_4 + e^- \rightarrow CF_3^+ + F + 2e^-$$
- $$CF_4 + e^- \rightarrow CF_3 + F + e^-$$

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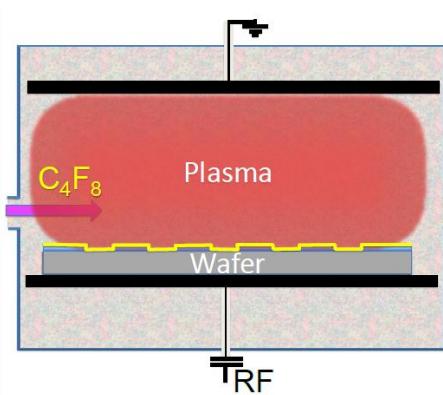


- Chemically reactive fluorine radicals are produced in a plasma upon impact on the CF₄ with an electron e⁻ from the plasma
- $$CF_4 + e^- \rightarrow CF_3^+ + F + 2e^-$$
- $$CF_4 + e^- \rightarrow CF_3 + F + e^-$$
- Fluorine radicals etch the Si in an isotropic way, i.e. mask underetching occurs
- $$Si(s) + 4F(g) \rightarrow SiF_4(g)$$

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This gas normally is an inert fluorocarbon gas, nothing happens. However, this gas becomes reactive when it is brought to the plasma state. The plasma can be created by applying a high voltage radio frequency field in the reactor. This high voltage ionizes gas molecules, thereby creating ions and electrons. The electrons are accelerated then in the electrical field that is created by the electrodes, and ionize other gas molecules, creating additional ions and electrons. An electron can also dissociate a gas molecule in neutral species, but this can be reactive too. For example, this fluoride atom is, chemically, very reactive. From the gas, CF₄, fluorine radicals can be created that etch the silicon in an isotropic way. That means that the etching speed in the vertical direction is the same as the etching speed in the horizontal direction, so mask underetching occurs, so one broadens the details of the mask in such a process.



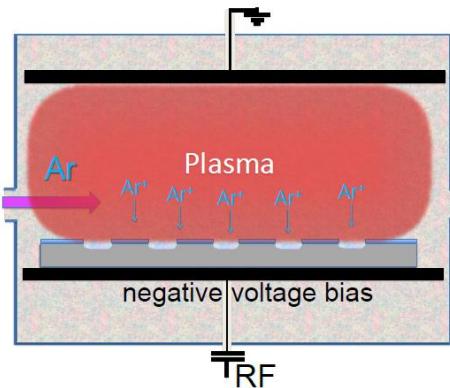
- Also CF₃ radicals can get adsorbed on the Si but can recombine with F after which CF₄ is desorbed
- However, if a carbon-rich gas like octafluorocyclobutane (C₄F₈) is used, this can lead to deposition of (CF₂)_n-type polymer chains
- The result is deposition of a smooth fluorocarbon polymer passivating film, rather than etching

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In this process, the silicon is recombining with the reactive fluorine radicals to form this gas, which is evacuated. A lot of different interactions and processes can occur in a plasma. For example, CF₃ radicals can get adsorbed on the wafer where they can recombine with the fluorine radical, after which the resulting

regenerated CF₄ molecule is desorbed and pumped away. If, instead of the gas CF₄, one uses a gas that is much richer in carbon, like the gas, octafluorocyclobutane, or C₄F₈, these radical adsorption processes become relatively more important, and can lead to degeneration of fluorocarbon-type polymer chains that get deposited on the substrate. The result is a thin fluorocarbon layer, as depicted here by this yellow material. So, instead of etching, when one uses this gas, one has deposition. If an inert gas, like argon, is used, ions can be created too, but these are not chemically reactive species that can react with the silicon, so, in principle, no etching occurs. However, suppose that on top of the radio frequency voltage that one applies, one can apply a negative voltage bias on this electrode. This will provide an attractive force to the positive argon ions. They can then be accelerated towards the wafer. If the kinetic energy of the argon ions is high enough, it is possible for them to remove silicon atoms from the wafer by physical impact. Such process leads then to anisotropic etching, only etching in the vertical direction, because there is the DC voltage bias, and there is no such bias in the horizontal direction. As a result of this physical impact, also the mask material will be slowly deteriorated and gradually consumed during the etching process. The mask lifetime, that is the time during which the mask resists to the physical impact, evidently will provide a limit to the etching depth that one can obtain in such a process. Here, we illustrate the directionality of the etching process, as defined by the factor, A. It's also called the anisotropy ratio A. It is defined in function of the vertical etching distance, z and the mask underetching distance, x. This is the formula.

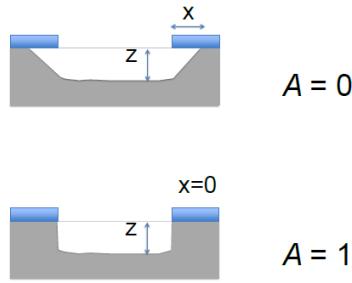


- If an inert gas like Ar is used, there is no reaction with the silicon
- However, if a negative voltage bias is applied to the wafer, Ar⁺ ions are accelerated towards the wafer and remove Si by physical impact
- This leads to anisotropic etching, i.e. there is no mask underetching
- Also the mask will be exposed to the physical impact and will be consumed

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For isotropic etching, that means a purely chemical process, $x = z$, and A is zero. For perfectly anisotropic etching, x is zero, so that A becomes one, and in general, the A value is in between zero and one. The use of halocarbon-based plasmas, that is plasmas that contain fluorine, chlorine, or bromine etching species, and carbon halogen radicals, like these ones, offers interesting possibilities in dry etching. These gases have a very low spontaneous etching rate when no negative voltage substrate bias is used. This figure illustrates the case for fluorine-based plasmas. It shows the conditions under which etching occurs, and one finds, on the x-axis, the fluorine-to-carbon ratio of the gas. One can vary this by changing the gas in the reactor. Here, one has CF₄, which is richest in fluorine, and, here, one has a gas, C₂F₄, which is richest in carbon. So, when one moves from right to left, one will move from an etching regime towards a polymerization, a deposition regime, due to the increased carbon in the reactor. If one moves along the y-axis, one goes from zero voltage bias, where there will be polymerization, to a regime where there will be etching, as here, these gases have sufficient kinetic energy for etching the silicon by physical impact. This explains the boundary layer between etching and polymerization as given by the dashed curve here. We give here, as an example, the etching in a halocarbon gas, with the fluorine-to-carbon ratio of 2.5, and using 200 eV ion energy. Under these conditions, one is clearly in the etching regime in this region. However, in a direction that is parallel to the substrate, there is no electrical field, and hence, it is equivalent to having here zero voltage, so in that case, there will be polymerization. So in the vertical direction, there is etching, in the horizontal direction there is polymerization on the substrate. The result is the absence of underetching of the mask,



- Anisotropy ratio A

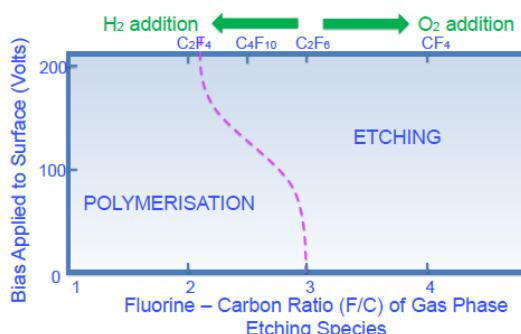
$$A \equiv \frac{(z - x)}{z}$$

- For isotropic (purely chemical) etching $A = 0$
- For perfectly anisotropic etching $A = 1$
- In general $0 < A < 1$

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and one obtains a purely anisotropic etching profile. Also, it is possible to add to the halocarbon gas, oxygen gas. In this case, the oxygen will react with the carbon forming CO₂, leaving relatively more fluorine so that etching is favored. Also, an option is to add hydrogen gas and the hydrogen will combine with fluorine radicals, forming HF which is pumped away. So, one is left, in that case, with much more carbon, and hence, addition of hydrogen will lead to polymerization. This slide shows specifically what happens when one adds hydrogen to the CF₄ gas under a negative substrate voltage bias of 150 volts. The vertical etching rate is v_z , and when one adds more hydrogen, the etching rate is reduced because fluorine radicals are removed by the hydrogen and one is left with more carbon. v_x is the horizontal etching rate, so it also the mask underetching rate. There is some etching rate without hydrogen, however, it is lower than the vertical etching rate. But, if one now adds hydrogen, also this etching rate diminishes until, here, it passes the curve, and here, one has zero etching rate in x direction, because the polymerization events, in a way, compensate for the etching in that direction. So, the result of this process is shown in these diagrams. If one has pure CF₄ etching gas, one has such a profile, where there is here, underetching and vertical etching, and adding 10% of hydrogen, one has zero etching in the horizontal direction, and only vertical etching. So, it is possible to obtain an anisotropic etching profile by adding 10% of hydrogen to the CF₄ gas. Based on what we have learned, we will give now a few simple rules that can help in choosing a dry etching gas. In a halocarbon plasma, the first important parameter is the fluorine-to-carbon ratio, and we have seen, just before, what we can do to change this ratio. A dry etching process can also be selective.



Boundary between etching and polymerization in fluorocarbon plasma as a function of F/C ratio (feed gas) and of the ion bombardment of the surface

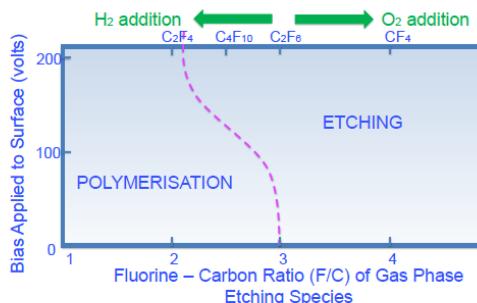
- Halocarbon-based plasmas contain etchant species (F, Cl, Br) and carbon halogen radicals (CF_x, CCl_x, CBr_x, 0 < x < 3) and have very low spontaneous etch rate without negative voltage substrate bias
- Polymeric thin film formation decreases for increasing F/C ratio, ion energy and flux towards the substrate (related to the substrate bias), and the substrate temperature

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That means it only etches the material to be etched and not the mask material. Selectivity can be enhanced by tuning the polymerization point of the gas. More polymerization will lead to extra masking material that gets deposited, so the mask can withstand longer the etching. We also learned before that the more negative

voltage bias is in favor of etching. It favors physical impact and higher anisotropy. For etching metals, one can use chlorocarbon and fluorocarbon gases.



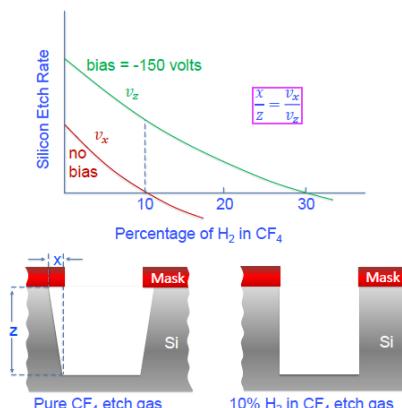
Boundary between etching and polymerization in fluorocarbon plasma as a function of F/C ratio (feed gas) and of the ion bombardment of the surface

- Example: for a ratio of F/C=2.5 with 200 eV ions, the horizontal bottom surface of the feature will be etched, but deposition will be dominant on the sidewall, where ion bombardment is lacking
- This results in the absence of underetching and an anisotropic etching profile
- Adding O₂ increases the F/C ratio
- Adding H₂ decreases the F/C ratio

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They can reduce the native metal oxides chemically. When etching metals, oxygen gas and water vapor must be excluded because they are in favor of oxidation, and metal oxides are normally difficult to remove.



- Adding H₂ to the CF₄ gas decreases etching rate, because fluorine reacts with H so that carbon compounds polymerise
- For 10% of H₂, this results in the absence of underetching and an anisotropic etching profile

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For metal etching, ion bombardment is also essential for successful etching. Dry etching of organic films, like photoresist, is relatively easy. A CF₄ oxygen plasma severely etches resists. If one wants to retain an organic masking material, like photoresist, one can work close to the polymerization point to regenerate the mask during the etching. We have introduced plasma-based dry etching, and exposed the parameters that control the etching and isotropy in the halocarbon plasma, like the fluorine-to-carbon ratio and the negative substrate bias. We have pointed out the possibility to vary the conditions of the plasma to result in etching or in polymerization, for example, by adding oxygen or hydrogen gas. Also, we have provided simple rules for designing dry etching processes for silicon, metals, and polymeric materials.

Summary

- Introduction to plasma-based dry etching
- Parameters controlling etching anisotropy in a halocarbon plasma : F/C ratio and substrate voltage bias
- Effect of adding oxygen and hydrogen gas
- Simple rules for design of dry etching processes for silicon, metals and polymers

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Practice quiz dry etching in a gas plasma; etching anisotropy

Questions:

1. Which of the following must be performed to convert an isotropic CF_4 etching process to a purely anisotropic etching process?

- Increasing the chamber pressure
- Increasing the bias voltage
- Adding 10% H_2 to decrease the F/C ratio
- Adding O_2 to increase the F/C ratio

2. In a CF_4 plasma to which hydrogen gas is added due to which the side walls of an etched hole can be protected from etching by deposition of a fluorocarbon polymeric layer, how can the selectivity of dry etching be increased?

- By increasing the temperature
- By decreasing the H_2 concentration
- By increasing the monomer concentration
- By decreasing the pressure

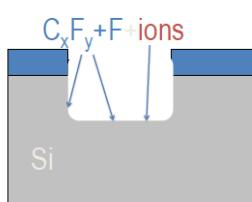


Dry etching 2

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In this lesson we will discuss various so-called deep dry etching processes for silicon, which are processes with a high anisotropy so that one can etch deep vertical holes with little or no mask underetching. We will also give an example of dry etching equipment. Finally, we will present a few special dry etching processes that use intrinsic reactive gases and that do not require to have the gas in the plasma state, which leads to a significantly simpler etching system. For deep dry etching of silicon, one can design a plasma-based etching process by combining the gases SF₆ and C₄F₈ in the etching reactor.



- Example: combining SF₆ and C₄F₈ chemistries, whereby C₄F₈ is the passivation gas
- Etching and passivation are simultaneous
- Substrate temperature typically is 20 °C
- Low etch rate: 1 to 3 μm/min (good depth control possible)
- High selectivity to photoresist : > 50
- Smooth sidewalls, very anisotropic process

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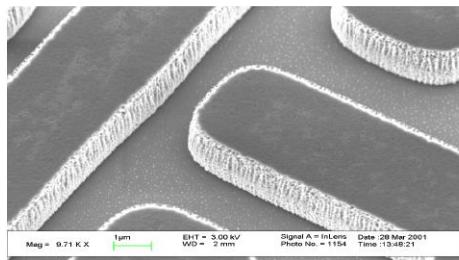
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The first gas is an etching gas, as it contains a lot of fluorine, while the second is a passivation gas while it contains relatively a lot of carbon. The substrate bias has to be chosen such that there is an effective vertical etching rate while the horizontal etching rate should be zero, due to the hole sidewall passivation by the deposition of the polymer. The process can be designed to have a high selectivity to photoresist. Silicon can be etched 50 times faster than the photoresist. These pictures illustrate some results of this type of etching process.

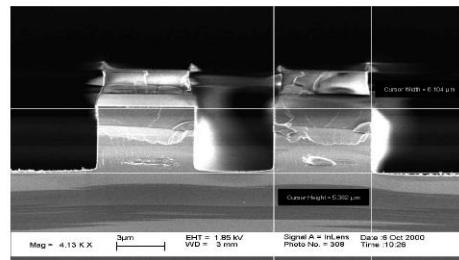
The first picture shows the etching of a polycrystalline silicon film which was deposited on a silicon dioxide layer. The second picture shows profiles of etched channel structures which were etched in a silicon wafer.

On the previous slides, both the etching and the passivation gas were simultaneously let into the reactor.

It is also possible to apply the etching and polymerization gas sequentially in a pulsed process. The pictures show what happens.



Etching of poly-Si on SiO_2

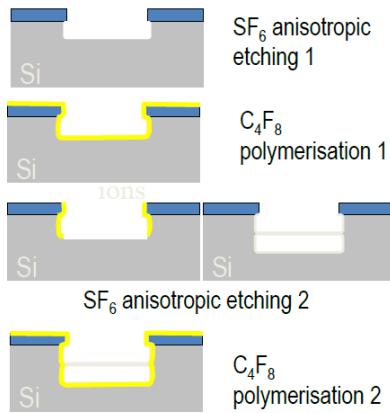


Etching of bulk Si wafer

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In the beginning, during a few seconds, chemical etching is performed in an SF_6 plasma, which gives a little underetching of the mask. Then the etching gas supply is switched off and C_4F_8 gas is introduced, which is known to lead to polymerization. During a few seconds, a thin polymer layer is deposited, as indicated by the yellow line here. The next step in the process is again an etching sequence. Due to the substrate bias, the polymer film that is deposited on the horizontal faces of the structure is quickly removed in the etching, and hereafter, silicon is etched in that direction. Because there is no electrical field in the horizontal direction, there is little or no etching, but polymerization is chosen such that at the end of this second etching cycle, all polymer has disappeared, and then one stops this second SF_6 etching cycle. One has effectively etched, now, a hole with little or no mask underetching. Next follows a second polymerization step, as illustrated in the lower picture. These pulsed etching and polymerization sequences can be repeated many times to realize very deep and anisotropic holes in the silicon. A high etching rate is obtained this way and a high selectivity of the silicon etching to silicon dioxide and photoresist masks can be obtained.



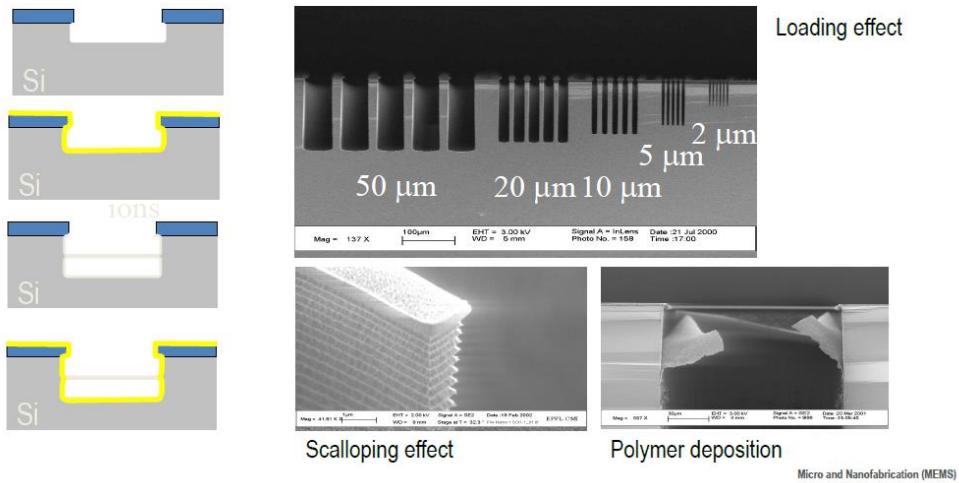
- Adding SF_6 and C_4F_8 chemistry is applied in sequences, C_4F_8 is the passivation gas
- Etching and passivation alternate (scalloping effect)
- Substrate temperature typically is 20 °C
- High etch rate: 3 to 15 $\mu\text{m}/\text{min}$
- High selectivity to SiO_2 : 100 to 400
- High selectivity to photoresist: 50 to 200

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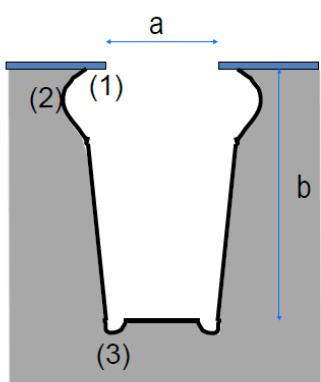
These pictures show some results of a deep dry etching process for silicon. The pulsed nature of the process is immediately recognizable by this so-called scalloping effect which originates from the alternating etching and polymerization cycles. The picture on the lower right shows a residual polymer layer, which was not completely removed from the sidewalls of the etched hole. The top picture shows that one can indeed etch vertical, anisotropic structures. It also shows that if there is a wider mask opening, the etching goes deeper than if there is a narrow mask opening, and this is related to the fact that the gas has easier access into a

larger hole than in a small hole, and etching is more favored in that way. This pulsed process of etching in silicon is also called the Bosch process, after the origin of the researchers who first developed this process. This picture shows, in general, the features that can be observed for an etched hole structure. The selectivity is defined as the ratio of the substrate etching to the mask etching, and ideally there should be little or no mask etching when the mask material is well chosen.



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For a hole opening a , one can etch a depth b , and this defines the aspect ratio b/a . Also illustrated here are some phenomena that are observed when doing dry etching of silicon. There is first the phenomenon of undercut, so there is some horizontal etching, which gives you mask underetching. There is also bowing, this kind of rounded shape, and there is drenching, at the bottom of the hole one sees some deeper recesses in the corners. Another important parameter of the etching process is the uniformity of the etching over the whole wafer. Ideally the etched profile should not depend on the position of the hole on the wafer. The origin of the microtrenching effect is illustrated here.



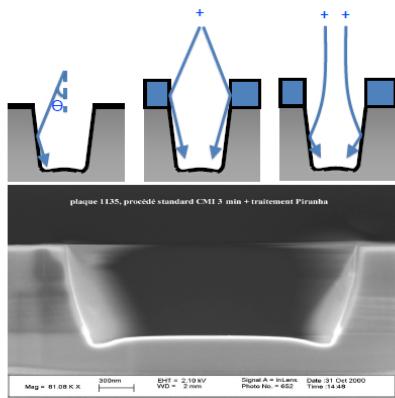
- Selectivity: etching rate ratio of the substrate with respect to the mask
- Etch rate/process time
 - Depth (b)
 - Aspect ratio (b/a)
 - Shape of the trench
 - Undercut (1)
 - Bowing (2)
 - Sidewall (roughness, slope)
 - Bottom (microtrenching (3), roughness, ...)
- Uniformity of etching over the area

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It is caused by the forward scattering of ions to the sidewalls of the etched structure. And this gives extra etching near the lower corners of the hole structure. This phenomenon can occur during etching of dielectric materials, semiconductors and metals. We take back, here, one of the pictures shown before, to illustrate the so-called aspect ratio dependent etching effect, ARDE effect by which the etch rate depends on the hole or trench width, as shown in this picture. Also, micro-loading effects exist in dry etching, which means that two identical trenches can have a different depth depending on if they were in a local environment on the wafer where there was more material to be etched away. That means where there was more competition for the gas to be consumed. If more silicon is to be etched away locally, the depth of a trench

or hole in such micro-environment will be smaller. On this slide, we summarize experimental process variables that can be varied in a dry etching process, and we mention, also, the way they effect the dry etching. The gas mixture, or gas chemistry, directly effects etch rate and etch profile, as well as variations in the gas flow rate and pressure.



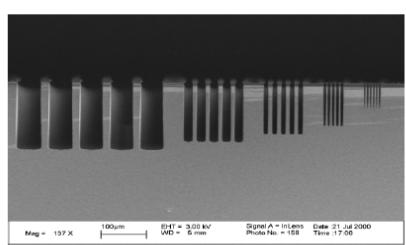
- Narrow grooves at the bottom of the sidewalls in the direction of ion bombardment
- Widely attributed to forward scattering of ions
- Can occur during etching of dielectrics, semiconductors and metals

Cross section of 1 μm wet oxide etching on Si using C_2F_6 plasma

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The RF power affects the etching rate, as for a higher power, more and more gas molecules get dissociated and the etching rate increases. The wafer temperature, or the temperature of the chuck on which the wafer is fixed, as well as the bias voltage on that chuck, directly influence the etching profile and the anisotropy. On this slide we give a schematic example of a dry etching reactor. It is a very sophisticated system which has a load chamber in which one puts the wafer to be etched.



Cross section of deep anisotropic etching of Si (Bosch process) for different trench widths

- Very present in deep Si etching
- Etch rate depends on the trench width
- Critical size about 100-200 μm
- Originates from transport phenomena: introduction of radicals and extraction of etch products is easier in big trenches
- Should be taken into account for mask design
- Also **micro-loading effect** exists: two identical trenches have different depth due to the local microstructure density, inducing a different environment of gas consumption

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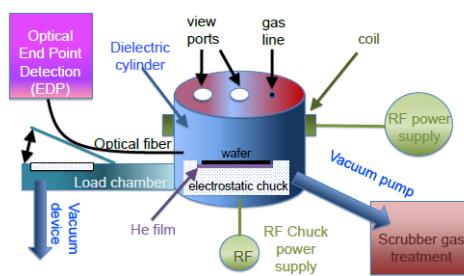
This wafer is then translated into the reactor without breaking the vacuum present in the reactor. The wafer in the reactor is clamped then to a chuck, it can be by electrostatic forces as we will explain later, and the chuck is kept at a fixed temperature and the etching can start.

<u>Process variable</u>	<u>Effect</u>
• gas mixture (chemistry)	• etch rate, etch profile
• gas flow rate	• etch rate (residence time)
• pressure	• etch rate (residence time), etch profile, selectivity mask/ material
• RF power (source)	• etch rate (dissociation rate)
• wafer temperature (chuck)	• etch profile (chemistry)
• bias of the wafer (chuck)	• selectivity mask/ material, etch rate, shape profile

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The reactor is equipped with a radio frequency power supply for generating the plasma, and in case an electrostatic chuck is chosen, there is an RF chuck power supply to generate these electric forces. There is also a scrubber that eliminates toxic side products of the etching reaction before leading the reactor output gases away into the environment. There is also an equipment for live monitoring of the optical emission from the gas

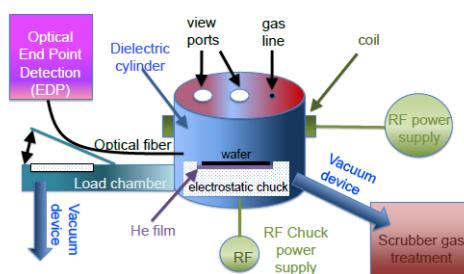


A dry etcher is a sophisticated and high-tech equipment, usually containing

- A loadlock/transfer arm system to keep the process chamber always under high vacuum during loading/unloading procedures, which optimizes process duration
- A processing chamber with RF plasma source and antenna, diffusion chamber, electrostatic and biasing substrate holder

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- Powerful pumping systems
- An end point detection system for monitoring the etching process
- Mass flow controllers for different gases, e.g. N₂, H₂, O₂, SF₆, C₄F₈, CF₄, BCl₃, Ar, and Cl₂. These controllers can be used in pulsed mode with fast response time

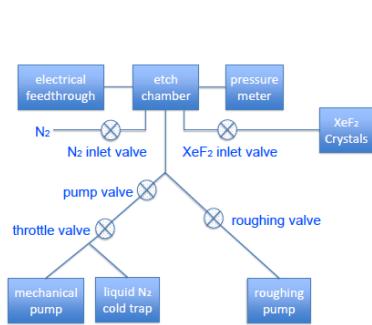


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to provide information on the materials that are etched away. And this can be used to determine when one has reached the endpoint of an etching process. The reactor is configured with several gas flow lines and mask flow controllers. For example, one uses nitrogen, hydrogen, oxygen, argon gas or any of the halocarbon etching gases. The picture on the right shows a real reactor with in front of it the chamber in which one loads

the wafer. Xenon fluoride gas etching of silicon without development of a plasma is also used in microfabrication. This process requires much simpler equipment than a plasma etcher. The xenon fluoride is placed, in the form of solid crystals, into a closed reactor from which fluorine vapor is spontaneously released, which etches the silicon according to this chemical reaction. The process has an etching rate of a few micrometers per minute. The figure shows a schematic diagram of the etching chamber interfaced with simply a few valves and pumps.



- Much simpler equipment
 - XeF_2 sublimates from solid crystals to form a vapor phase etchant (~4 mbar at 25 °C)
 - XeF_2 gas adsorbs and dissociates to Xe and F on the surface of silicon
 - Reaction of silicon with XeF_2
- $$2 \text{XeF}_2(g) + \text{Si}(s) \rightarrow 2 \text{Xe}(g) + \text{SiF}_4(g)$$
- XeF_2 has a few $\mu\text{m}/\text{min}$ etch rate and Si etching does not require ion bombardment or a plasma

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Another example of gas phase etching without a plasma is the etching of silicon dioxide using HF vapor. For hydrofluoric acid vapor phase etching, one only needs a container into which one pours the HF, and a wafer holder to which the wafer is mechanically clamped. The reaction with the HF vapor is written here, and is controlled by the wafer temperature. The technique can be used to remove an oxide layer underneath an etched silicon microstructure to provide a freestanding structure. So here the silicon was etched, then putting it into HF vapor slowly etches away the oxide, until in the middle, these silicon parts are now freely moving, and, of course, they are somewhere anchored to the substrate. In this way, one can release the silicon structure without applying a liquid. If one applies a liquid here, this can give surface tension forces which can deform the delicate mechanical structures. This slide gives an impression of the equipment that is needed for HF vapor phase etching, which indeed is orders of magnitude less complex and much cheaper than a plasma reactor.

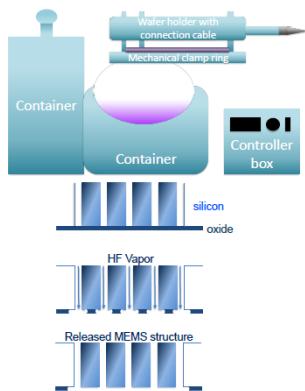


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There is a container for the HF, and there is control of the temperature, basically. Here we see how silicon dioxide is partly removed from under a polysilicon layer so that this becomes a freestanding electrode.

In this lesson, we have presented several processes for the deep dry etching of silicon, like the continuous process in which the etching gas and the polymerization gas are simultaneously introduced in the plasma reactor, as well as the pulsed, or Bosch, process in which the two types of gas exposures are alternated.

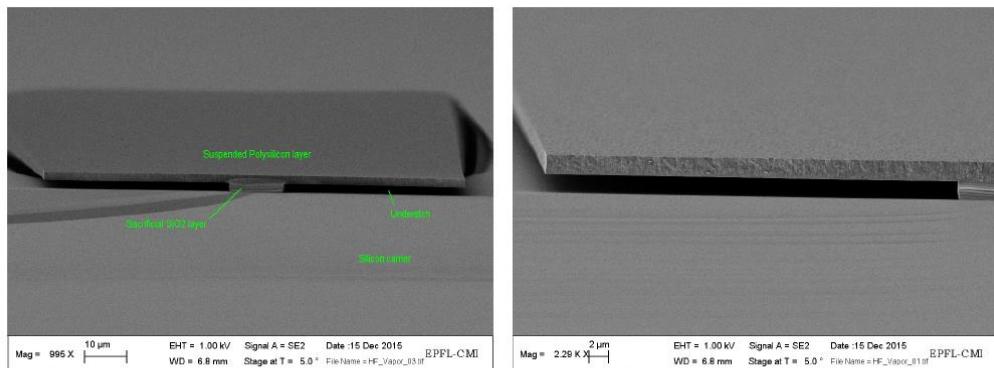


- A hydrofluoric acid vapor phase etcher consists of a reaction chamber and a wafer holder
 - HF evaporates at room temperature and the etching process starts spontaneously
- $$SiO_2(s) + HF(g) \rightarrow H_2O(g) + SiF_4(g)$$
- The etch rate is controlled by the wafer temperature that can be adjusted from 35 °C to 60 °C
 - A dry release etch avoids stiction of free-standing parts of a MEMS device

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We gave an example of a typical dry etching equipment and also introduced dry etching without a plasma, which requires much less complex and much less sophisticated infrastructure. Subsequently, we introduced xenon fluoride etching of silicon, and HF vapor phase etching of silicon dioxide.



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Practice quiz deep dry etching of silicon; dry etching without a plasma

Questions:

1. Which of the following is true related to the pulsed deep dry etching process of Si (Bosch process)?
 - SF₆ is used in the sequence as the passivation gas
 - A loading effect is observed when there is a wide mask opening and a narrow mask opening on the same wafer
 - The etching rate can be increased by adding Ar in between etching and passivation steps
 - C₄F₈ is used in the sequence as the chemical etching gas
2. Which of the following is true for a dry etching equipment?
 - An electrostatic chuck is used to stabilize the electron density in the chamber
 - A load chamber is utilized to load the desired gas for the etching process
 - Optical end point detection is used to monitor the stability of the fixation of the wafer on the electrostatic chuck
 - A scrubber gas treatment is necessary to avoid toxic side products to be released in the environment

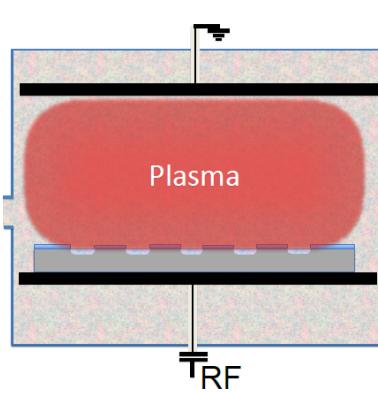


In this lesson, we will introduce some theoretical concepts, that characterize a plasma in dry etching equipment.

- Theoretical concepts of plasma generation
- Ion sheath in a plasma
- Electrode area design rule for efficient ion bombardment on the wafer to be etched

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A plasma is a collection of excited neutral molecules, of ions and of electrons. Close to an electrode in the plasma, electrons are repelled so that mainly ions and, of course, neutral molecules remain there. Such a layer close to an electrode is therefore called an ion sheath.



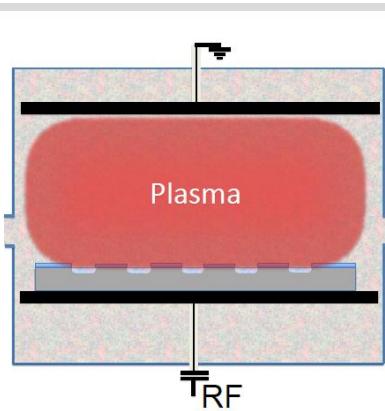
- Plasma is an ionized gas (10^{-3} - 1 mbar), with about the same densities of electrons (n_e) and ions (n_i)
- The degree of ionization in a plasma is on the order of 10^{-6} - 10^{-4}
- Radio frequency (RF) power applied to electrodes in an etch chamber creates an electrical field that accelerates the lighter electrons
- Electrons collide with neutral atoms/ molecules, ionize them and sustain the plasma
- Plasma 'glows' by photon emission during transition between electron excited and ground states

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As a plasma is a special electrically conducting medium, it has to be interfaced in a proper way with a radio frequency power source. We then present a design rule for the RF electrodes that enables magnetization of ion bombardment to the electrode on which the wafer to be etched is positioned. An ion impact on the

counter electrode, which would lead to reactor damage, is reduced or absent. A plasma is defined as an ionized gas, and has about the same densities of electrons and of ions. A plasma is usually generated starting from a gas of pressures



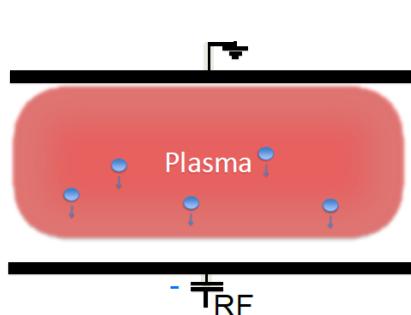
- Such glow discharge plasma is characterized by a lack of thermal equilibrium between the electron temperature T_e and the gas temperature T_g
- T_e corresponds to the kinetic energy of the electrons via
$$\frac{1}{2} m_e v_e^2 = \frac{3}{2} k_B T_e$$
- with v_e the mean electron velocity
- $T_g \sim 3 \times 10^2 \text{ K}$, $T_e \sim 10^4 \text{ K}$, $T_{ion} \sim 10^3 \text{ K}$
- Glow discharge plasma is called a 'cold' plasma

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of 10^{-3} to 1 millibar. The degree of ionization in a plasma is rather low, of the order to 10^{-6} to 10^{-4} .

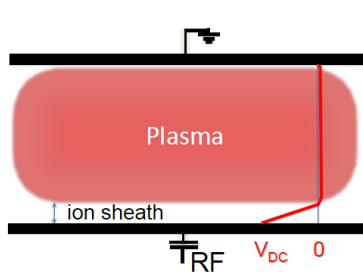
That means that one of a million, or one of 10,000 molecules is ionized. This means, also, that the majority of molecules in the plasma are neutral. In the picture, we show how radio frequency power is applied via two electrodes. Initially, there is a discharge in the gas when a high electric field is applied due to discrete molecule ionization events, but rapidly, the RF power is distributed over all gas molecules due to collisions when energetic electrons that are accelerated in the electric field.



- 13.56 MHz is typically used RF frequency
- Blocking capacitor is placed between RF source and the plasma
- Initially, no DC bias voltage V_{DC} is present on the lower electrode

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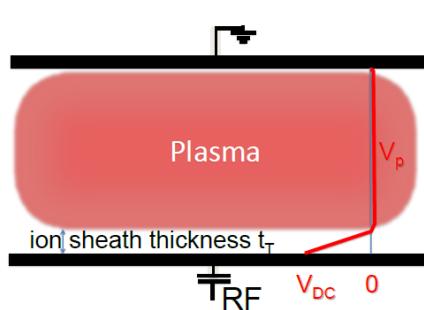
- 13.56 MHz is typically used RF frequency
- Blocking capacitor is placed between RF source and the plasma
- Initially, no DC bias voltage V_{DC} is present on the lower electrode
- After a few RF oscillations, e^- accumulate on the lower electrode due to their higher mobility, typically generating a voltage $-300 \text{ V} < V_{DC} < 0$
- Few e^- are present in the dark ion sheath near the working electrode

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The presence of a plasma is revealed by a glow of the excited gas, which is due to photon emission events during transition of an electron between an excited and a ground state. This so-called glow, discharged

plasma, is characterized by a lack of thermal equilibrium between the electron temperature, T_e , and the gas temperature, T_g . The electron temperature, T_e , can be obtained if one equals the thermal energy to the kinetic energy of the electron with v_e , the typical electron velocity in the electrical field.

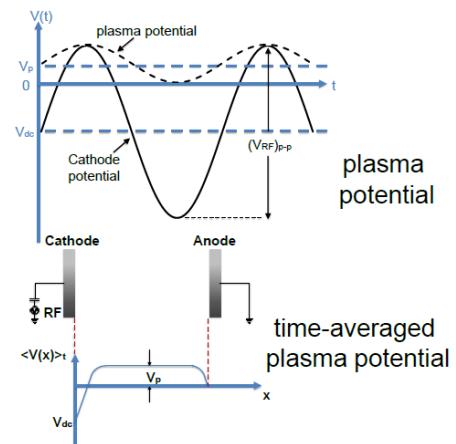
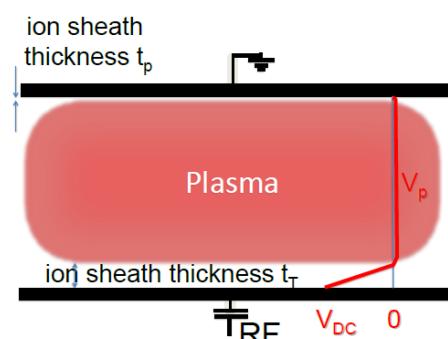


- The bulk of the plasma is slightly positive (voltage V_p) due to e^- loss to the walls of the system
- Ions approaching the interface between plasma and ion sheath with thickness t_I are accelerated to the lower electrode in the electrical field $\frac{V_p + V_{DC}}{t_I} \equiv \frac{V_T}{t_I}$

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While the gas temperature is typically at room temperature in the plasma, that means a few hundred Kelvin, the calculated electron temperature can reach 10,000 Kelvin this way. The ion temperature, due to the heavier ion mass and lower velocities, is around 1,000 Kelvin. Due to the low gas temperature, a glow discharge plasma is therefore called a cold plasma. A typical frequency that is used for the generation of a plasma is 13.5 megahertz. In the schematic diagram, the upper electrode is connected to earth, while the lower electrode, on which the substrate will be positioned, has a so-called blocking capacitor in between the electrode and the RF power source.

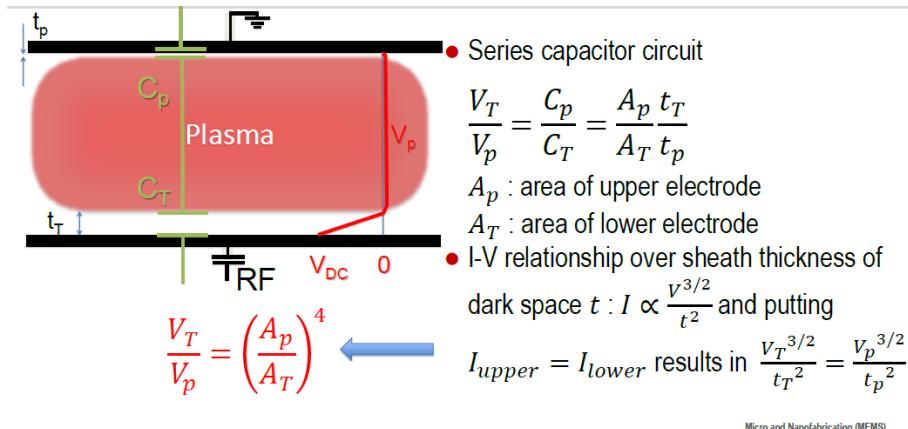


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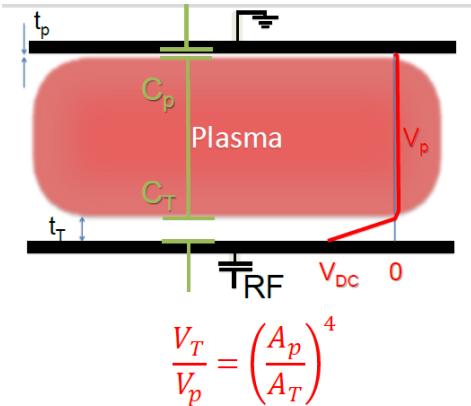
This capacitor allows accumulation of charges on the lower electrode, and, if this happens, one generates a so-called voltage bias, V_{DC} , on that electrode. Initially, no such voltage bias is present on the lower electrode. When the radio frequency power is switched on, there is an alternation of positive and negative voltages on the lower electrode. Suppose one is in part of the cycle where the voltage on the lower electrode is positive. The RF frequency is very high, but electrons are so light that in one-half cycle they can reach the lower electrode, and they will charge this electrode, so they stay trapped on the electrode because they are blocked by this capacitor. Suppose one is in the next half-part of the cycle where the voltage on the lower electrode is negative. In this case, the ions, which are positive, get attracted, but they are much heavier, and they do not acquire enough momentum to reach, initially, the lower electrode. So, as a result, after one cycle, one has accumulated here negative charge due to the electrons, and, after a few RF cycles already, a static negative surface bias is here on the electrode and on the substrate that is positioned on it. The generated DC voltage bias can be minus a few hundredfold. Once this negative voltage is developed, one

reaches an equilibrium electron ion transport regime with strong ion impacts to the lower electrode and on the wafer, as attracted by this negative charge. Once this negative charge is accumulated, also electrons are more and more pushed away from this electrode, and this leaves a zone near the electrode where there are predominantly ions, and, of course, also the neutral gas molecules.



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That's why this layer, where there are little or no electrons, is called the ion sheath. Also, on the other side, we have the electrode, which is connected to earth. The electrons will be evacuated to earth, so, very close to that electrode, there is also a thin ion sheath. The top electrode is always at zero volts because it's connected to earth. The average voltage within the plasma itself is slightly positive, as some electrons from the plasma can get lost to the walls of the reactor. So, the time-averaged voltage, is shown by the red curve here. We can now calculate the electrical field that is present near the lower electrode. So, the electrical field is determined by the drop of voltage, that is V_{DC} , plus V_p , over this distance, t_T . Now we define the sum of V_p plus V_{DC} as V_T , the total. In a similar way, one can calculate the electrical field near the top electrode, which is given by the voltage drop, V_p , over this small distance, t_p . One should keep in mind that all these are time-averaged voltages in the plasma, as shown in the figure below. In fact, this is the same graph as we have shown before in the red curve. The time dependence is presented in the figure above, so it shows the RF oscillations, which are centered around these mean voltages. As the two ion sheaths near both electrodes contain very few electrons, but rather the heavier and less mobile ions, we can represent them to good approximation by a series circuit of a capacitor, C_T , and a capacitor, C_p , and the plasma, with a lot of electrons is then considered to be a conductor. We can now write the ratio of the total voltage drop, V_T , over the voltage drop, V_p , as the ratio of the capacitors. Then we rewrite each capacitor in function of the area of the electrode and of the thickness of the ion sheath. It is not necessary, a priori, that the areas are equal between the two electrodes, and also the thickness of both ion sheaths doesn't have to be equal. Of course, an ion sheath is not a simple dielectric as in a normal capacitor, but it is a high resistance layer over which current transport from the plasma to the electrode is still possible. We present here the expression for the current voltage relationship over such an ion sheath as a function of the thickness of the ion sheath. The current is proportional to the power 1.5 of the voltage, and inversely proportional to the square of the thickness of the ion sheath. Now we simply assume that the current, which is flowing on the lower and on the top electrode are equal, so we can equalize these two current expressions; once for the lower electrode and for the top electrode. We can now combine this expression with this expression to obtain this formula. What does this learn us now? We should remember now that what we aim for in etching is that ions are predominantly accelerated by the large total voltage, which is near the lower electrode. While we do not aim to create



- In order to maximize etching on the lower electrode, one should choose the lower electrode area smaller than the upper electrode area
- However, such asymmetric electrode system tends to have a non-uniform plasma, peaking in the center, resulting in different etching between the center and edges

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a strong ion bombardment on this side, as you would cause damage to the reactor electrode. This formula says that we can achieve this by choosing the lower electrode, smaller than the top electrode because there is a power of four in the formula. An inconvenience (disadvantage) of such so-called asymmetric electrode systems is however, that the plasma on this electrode is less uniform, and has more intensity in the center of the small electrode than at the edges of that electrode. In this lesson, we have explained the basic properties of a cold plasma, which has a gas temperature of a few hundred Kelvin, and an electron temperature of 10,000 Kelvin. We then explained the phenomenon of formation of an ion sheath near an RF electrode, and explained how placement of a blocking capacitor allowed to generate a DC voltage bias, by which ions are attracted towards the electrode that carries the wafer that needs to be etched. Also, we presented a design rule for the areas of RF electrodes, which resulted in a major bombardment of ions on the electrode where the wafer is positioned, and not on the counter electrode.

Summary

- Glow discharge plasma or ‘cold’ plasma
- Ion sheath and DC bias voltage
- Design rule for the RF electrode area

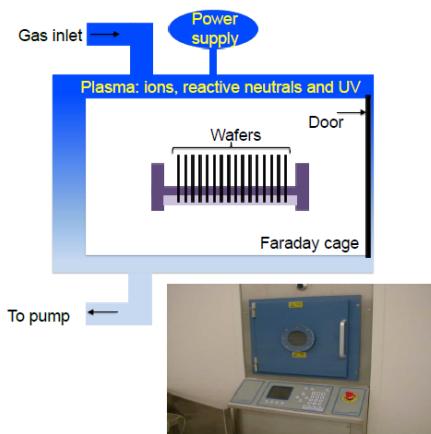
Practice quiz theoretical concepts of plasma generation

Questions:

1. Which of the following is true for an RF plasma assuming that the top electrode is connected to the ground and the bottom electrode is connected to the RF source?
 - The current passing through the ion sheath is proportional to the square of the thickness of the ion sheath
 - Due to the loss of electrons to the walls, the bulk of the plasma becomes slightly negative
 - After accumulation of electrons on the lower electrode, the remaining electrons in the plasma are pushed away and an ion sheath is formed near the electrode
 - After a couple of RF oscillations, electrons tend to charge the top electrode
2. What can be done in RF plasma etching for enhancing the etching rate on the RF electrode side where the wafer is placed?
 - The gas flow rate must be enhanced
 - The frequency of the RF voltage can be increased
 - The pressure inside the chamber must be increased
 - The RF electrode area must be chosen smaller in size than the electrode on the opposite side



In this lesson, we will present main dry etching equipment. Also we will introduce some of the plasma sources that are used in modern dry etching reactors. This is a schematic diagram of a so-called *<i>barrel reactor*. It is one of the first etching reactors used in semiconductor microfabrication. It exploits a chemical oxygen plasma to remove polymers or photoresist from wafers. Such a reactor is also used for descumming. And descumming is removal of thin polymer residues after development of a photoresist, for example. The technique is also called plasma ashing or plasma stripping because it removes the organic molecules. There is no ion bombardment in this technique, and chemical action from the oxygen atoms



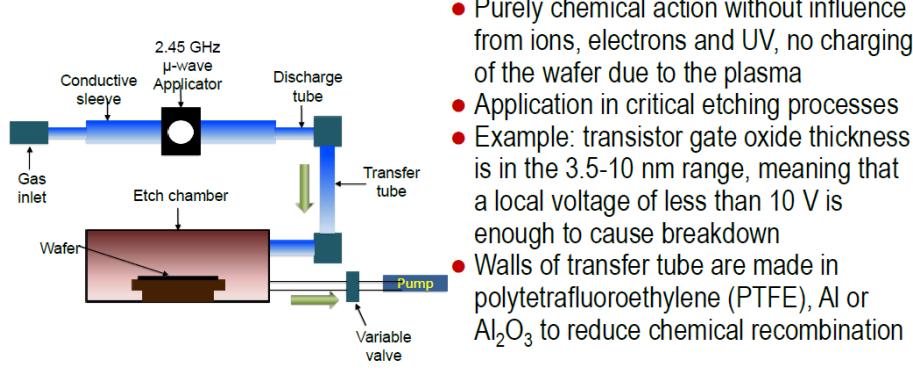
- First etching reactor used in semiconductor processing that dates from the late 1960s
- Oxygen plasma to remove photoresist
 - Plasma ashing or plasma stripping
 - No ion bombardment, but action from oxygen atoms + UV radiation
- Working pressure 0.1 to 10 mbar
- Descumming
- Isotropic etching of polymers in O₂ plasma
- Isotropic etching of Si in CF₄ plasma

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and UV radiation is solely responsible for the etching. The typical working pressure is in between 0.1 and 10 millibar. Besides the use of oxygen for removal of organic layers, one can also use a CF₄ plasma in this reactor for silicon etching without bombardment. The picture below shows the entrance door of such a barrel reactor and its command panel. This is a schematic diagram of a so-called chemical downstream reactor. A microwave plasma is generated remotely from the etching chamber and then transferred to the etching chamber. The wafer which is positioned here, is hence not influenced by accelerated ions, electrons, or by ultraviolet irradiation and the etching is purely chemical. The technique is used in critical etching processes. For example, for the etching of transistor gate oxides which are extremely thin, so that even a low voltage

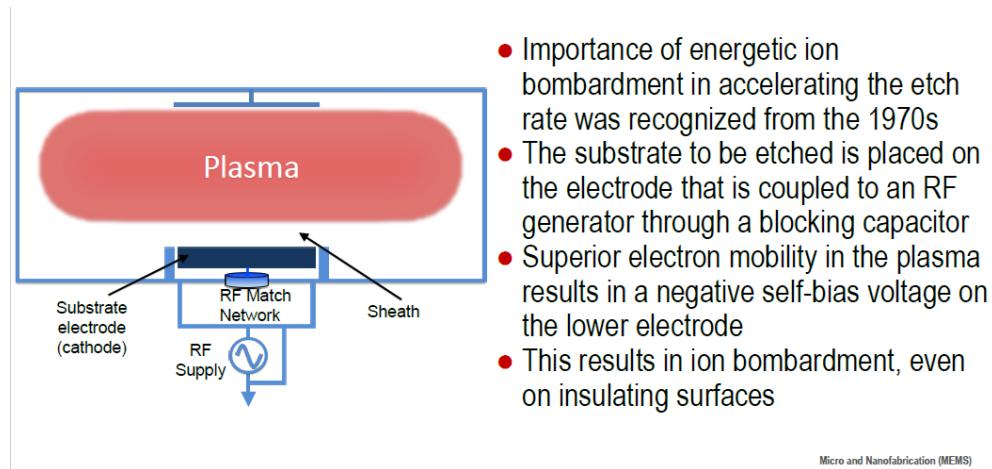
can cause dielectric breakdown of the transistor. The walls of this transfer tube are covered with inert materials like polytetrafluoroethylene, or Teflon, or can even be made of that material.



- Purely chemical action without influence from ions, electrons and UV, no charging of the wafer due to the plasma
- Application in critical etching processes
- Example: transistor gate oxide thickness is in the 3.5-10 nm range, meaning that a local voltage of less than 10 V is enough to cause breakdown
- Walls of transfer tube are made in polytetrafluoroethylene (PTFE), Al or Al_2O_3 to reduce chemical recombination

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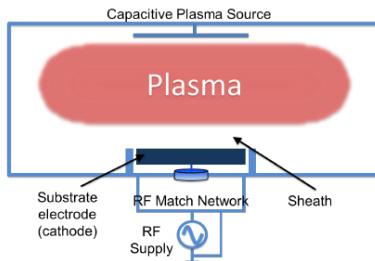
Also, aluminium or aluminium oxide is used for this transfer tube to reduce chemical interactions with the plasma during transfer. This schematic diagram is that of a so-called diode reactor due to the presence of two electrodes, and we have already introduced this reactor before in our discussion of dry etching. We explained how the substrate electrode can acquire a negative voltage bias by incorporating a blocking capacitor in the circuit. Also of importance for this high negative voltage bias was the superior electron mobility over the ion mobility in the RF plasma. The developed negative voltage bias results after a while in strong ion bombardment, even on insulating surfaces on the wafer. The electrical impedance of a capacitive plasma source is that of a capacitor in series with a resistor. A match network is required



- Importance of energetic ion bombardment in accelerating the etch rate was recognized from the 1970s
- The substrate to be etched is placed on the electrode that is coupled to an RF generator through a blocking capacitor
- Superior electron mobility in the plasma results in a negative self-bias voltage on the lower electrode
- This results in ion bombardment, even on insulating surfaces

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to couple the impedance of this plasma to the RF power supply. Such a match network has variable series and shunt capacitors to minimize power reflection and recirculating power losses. The difference between a symmetric and an asymmetric configuration is shown here. In the asymmetric reactor, the electrode on which the wafer is to be positioned is smaller than the counter electrode. It's much bigger. While in the symmetric configuration, both electrodes are nearly the same. In the asymmetric reactor, the electrode on which the wafer is to be mounted was smaller than the counter electrode, and we have seen before that this leads to a strong voltage bias on the small electrode, hence, heavy ion bombardment. The voltage V_p in that case was very small so that there is little or no impact on the counter electrode, so there is no degradation of the reactor.

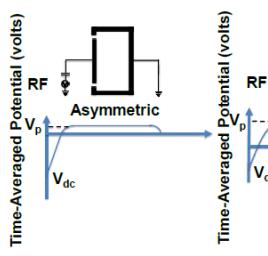


- Electrical impedance of a capacitive plasma source behaves like a capacitor in series with a resistor
 - $Z_{\text{plasma}} = R - j/\omega C$ with $|Z_{\text{plasma}}| > 50 \Omega$ and $R < |1/\omega C|$
 - $C \sim 100 \text{ pF}$ due to the capacitance of the driven electrode sheath
- A match network is required to make the plasma impedance, in series with the match impedance, look like a 50Ω impedance for the RF power supply
- The match network has variable series and shunt capacitors to minimize recirculating power losses

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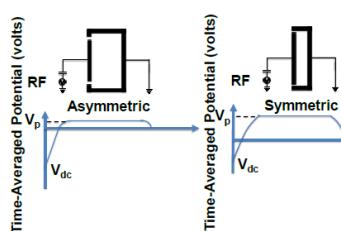
In the symmetric diode reactor, both electrodes have about the same surface area and in this case, all electrode surfaces can be bombarded and thus sputter materials can eventually diffuse into the plasma when the gas pressure is too low. To avoid this diffusion into the plasma, one chooses typically the gas pressure not too low. At first sight, a diode reactor with a smaller size working electrode is advantageous but the RF power will be peaked in the center so that there is different etching, whether one is in the center or at the edge, and this can be problematic for some applications. If that is the case, one uses a symmetric diode reactor where the field is uniform over the wafer. To reduce the effect of bombardment of the counter electrode one chooses the pressure of the gas sufficiently high, so that sputtering from that counter electrode can be reduced. And as high pressure, we mention here pressures of the order of 100 millibar. A diode reactor, like we have now discussed, has as limitation that there is no independent control of the ion energy and the ion flux. Both increase with increasing RF power.



- V_p is only a few tens of Volts in case of the asymmetric diode geometry, but can reach the amplitude of the RF voltage (few hundreds Volts) in case of the symmetric geometry
- In a symmetric system, the ion energy is the same for the powered and grounded electrode. Sputtering of surfaces can occur at low pressure and materials can diffuse in the plasma

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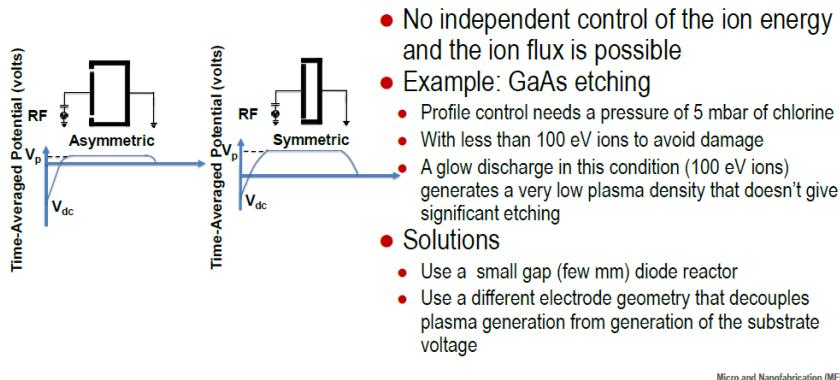


- Asymmetric systems tend to have non-uniform plasma, peaking in the center, resulting in different etching between the center and edges
- Consequently, a symmetric planar diode can be advantageously used, at a pressure that is high enough (>100 mbar) to limit sputtering

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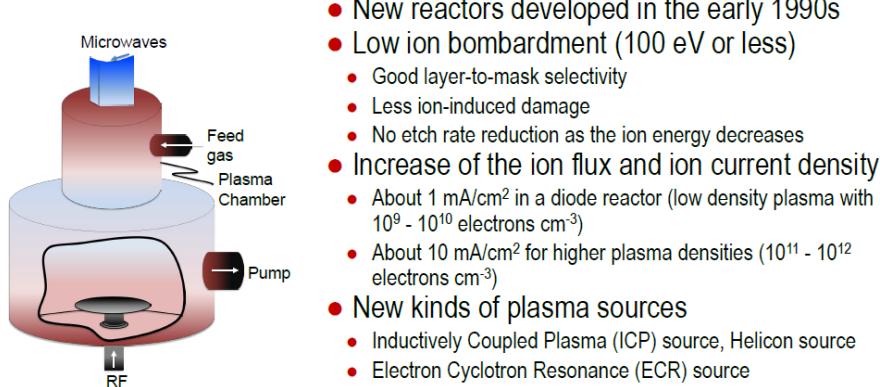
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As an example where this can be problematic, we mention here the etching of gallium arsenide. We need here a chlorine plasma at a considerable pressure but we want to avoid a large voltage bias to the wafer to avoid damage of the material by the ion bombardment. However, this obliges to have very low plasma density that does not give significant etching. Two solutions exist to the problem.



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One can use a small gap diode reactor where the electrical fields and voltages are lower, or one can exploit a different electrode geometry than a diode to decouple plasma generation from the generation of the negative substrate voltage bias. Such decoupling of the plasma generation from the generation of the bias was exploited in the newer etching reactors that were developed from the early 1990s on. These reactors are characterized by a low energy ion bombardment on the wafer, which results in a good layer-to-mask selectivity, less ion induced damage of the etched materials, and no etch-rate reduction when the ion energy decreases. In these new reactors, the ion flux and ion current density were significantly increased, typically by an order of magnitude.

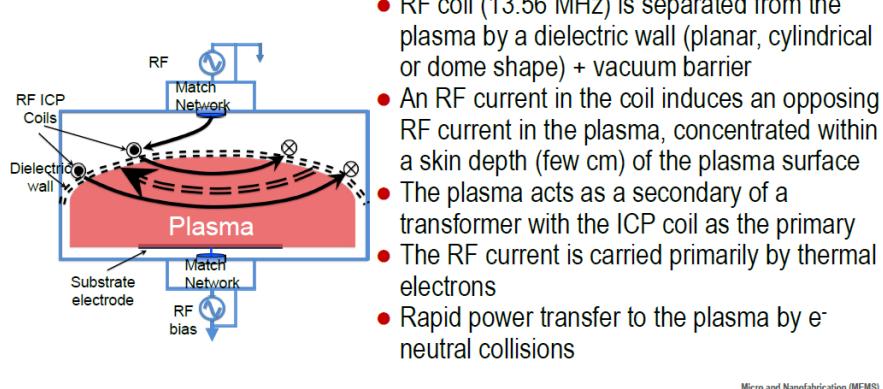


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As examples of these new plasma sources, we will explain now briefly, the so called <i>inductively coupled plasma source or ICP source, the helicon source, and the <i>electron cyclotron resonance or ECR source.

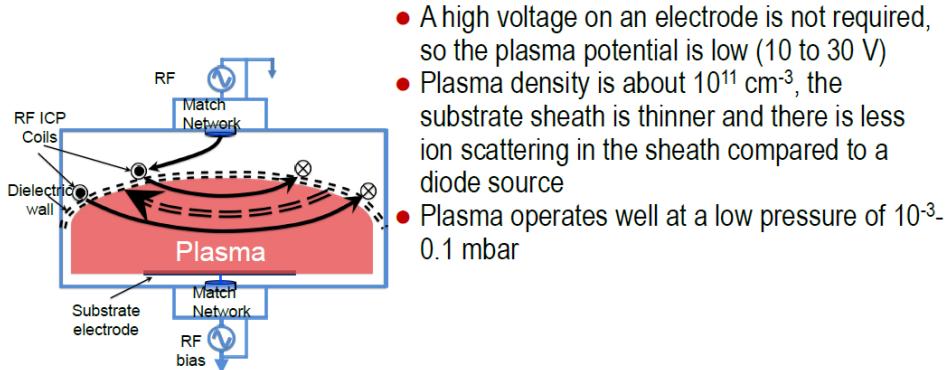
In an ICP source, an RF coil operated at 13.5 megahertz is separated from the plasma by a dielectric wall which can have cylindrical, or in this case, a dome shape. An RF current which passes in this coil will induce a counter current in the plasma, within the skin depth of the plasma, which is a few centimeters. The plasma acts like a kind of secondary transformer with the ICP coil, the primary. The RF current is primarily carried by thermal electrons that rapidly transfer their energy to neutral atoms in the plasma. For an ICP reactor, a high voltage on the lower electrode is not required, so the plasma potential can be low.

Still, the plasma density can be high, as it is generated by the other RF source. The substrate sheet layer is thinner and there is less ion scattering in the sheet, compared to a diode source. The plasma operates well at low pressures of 10^{-3} to 0.1 millibar. An ICP source needs to be properly interfaced with an RF power generator. The electrical impedance of an ICP source is that of an inductor in series with a small resistor.



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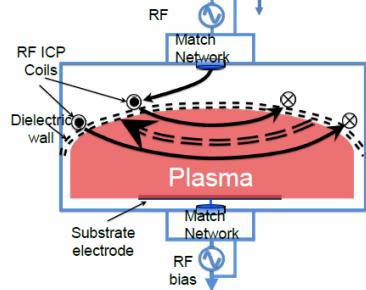
The match network, to avoid or reduce reflection of power back to the source, can be accomplished with the so-called L network which consists of a number of variable series and shunt capacitors that are adjusted here. This type of plasma has a small capacitive coupling compared to the plasma generated in a diode reactor, because the coil is separated from the plasma by a rather thick, dielectric wall. However, the plasma needs to be initiated in the beginning via capacitive coupling. Note that besides the RF power for generation of the plasma, there is an extra RF power source for generating the surface voltage points. We are here in the cleanroom and show the outside of an ICP reactor. Inside of the plasma source is a coil that surrounds a ceramic cylinder. Here we show such a cylinder that has been used and removed after a certain time of operation. At the inside of the cylinder, we see some degradation effects of the material due to the plasma, which is the reason why the cylinder has to be exchanged regularly to a new one during maintenance of the ICP etching system. Another type of new plasma source is the electron cyclotron resonance or ECR source. In this design, microwave power at a frequency of 2.45 gigahertz is carried by a wave guide and coupled to the plasma through a dielectric window.



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The source has built-in magnetic field lines generated by these electromagnets around which electrons can circulate. The plasma absorbs power at a location where the electron cyclotron resonance condition is satisfied, that is, where the natural cyclotron motion of the electron around the field line is in phase with the rotating electrical field of the ECR wave. Finally, we mentioned as one of the new plasma sources, the helicon source, in which an antenna coil with a special shape is wound around the plasma. The helicon wave source works at 13.5 megahertz, also in presence of a magnetic field. Plasma parameters of the helicon

source are comparable to that of ICP and ECR sources. This slide summarizes the plasma densities that are obtained with the various plasma sources as indicated here, as well as the gas operation pressure regimes. What we see on this slide is that going through more modern equipment, we go to lower working pressures and higher plasma densities.

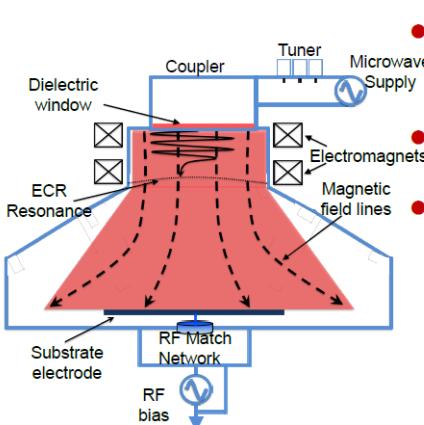


- Electrical impedance of an ICP source is an inductor in series with a small resistor
- $Z_{\text{plasma}} = R - j\omega L$ with $|Z_{\text{plasma}}| > 50 \Omega$ and $R < |\omega L|$
- The inductance is several microHenry in a typical ICP
- Matching can be accomplished with a "L" network: variable series and shunt capacitors
- Small capacitive coupling compared to diode plasma, because the coil is separated from the plasma by a thick (1 cm) dielectric wall
- However, capacitive coupling is needed to initiate the discharge

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Here we show a picture and a schematic diagram of an ICP etcher which we have already introduced before. We want now to explain the mechanism of the electrostatic chuck for clamping of the wafer into the reactor. The wafer was introduced via a load mechanism to the chuck and in the chuck, there is a part which is called gripper, which contains two electrodes to which one can apply a voltage.

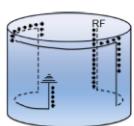


- Microwave power at a frequency 2.45 GHz is carried by a waveguide and coupled to the plasma through a dielectric wall
- Matching is usually accomplished by a three-stub tuner
- Power absorption occurs at the location where the ECR resonance condition is satisfied, i.e. where $\omega = \omega_{ce}$, i.e. where the cyclotron motion of the electrons is in phase with the rotating electric field of the ECR wave

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Here, a positive voltage, here a negative voltage and this induces an opposite voltage in the wafer which is then clamped to the gripper. For removal of this electrostatically bound wafer, one needs to apply opposite voltages to the electrodes. In this lesson, we have discussed three types of dry etching equipment, like a barrel reactor, a chemical downstream reactor and a diode reactor.

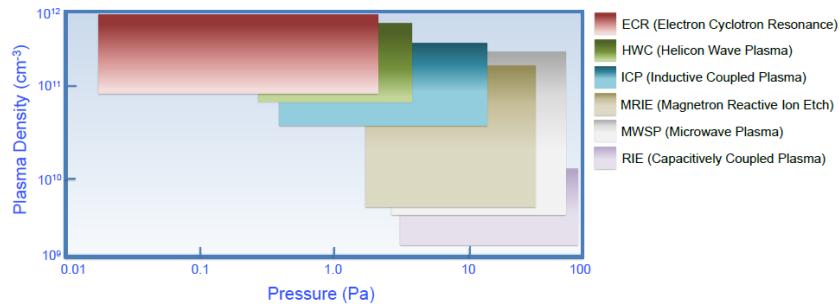


- Power is coupled through the outside of a cylindrical dielectric wall surrounding the plasma, using an antenna coil wound around the plasma column
- Matching network similar to that of an ICP source
- Helicon wave source works at 13.56 MHz in presence of a magnetic field (10^{-5} - 10^{-2} T)
- Plasma parameters of a helicon source are similar to that of ICP and ECR sources

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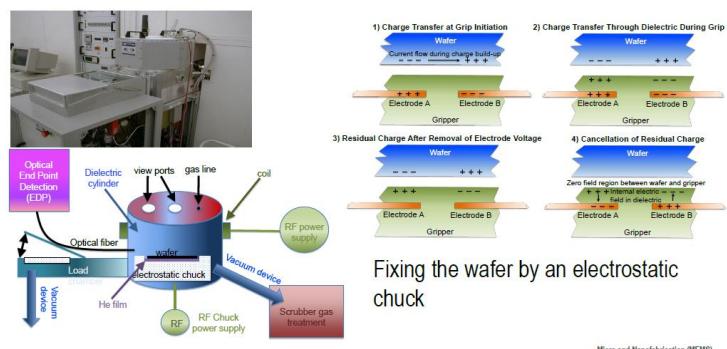
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We pointed out the limitations of a conventional diode reactor where one cannot vary independently the negative substrate voltage bias, and the flux of the reactive species towards the wafer.



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We then introduced three of the newer plasma sources in which one has decoupled the generation of substrate bias from the reactive species flux. These were the inductively coupled plasma source, the electron cyclotron resonance source, and the helicon source.

Summary

- Types of dry etching equipment
 - Barrel reactor
 - Downstream reactor
 - Diode reactor
- Plasma sources
 - Inductively Coupled Plasma (ICP) source
 - Electron Cyclotron Resonance (ECR) source
 - Helicon source

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Practice quiz types of dry etching equipment and plasma sources

Questions:

1. Which of the following is a correct statement for an Inductively coupled plasma (ICP) etching system?

- The plasma can only be activated when the pressure is set to an extremely high value
- There are two RF power sources: one for generation of the plasma and one for generating the surface voltage bias
- A high voltage on the working electrode is needed, so that the plasma potential is kept at high values
- The electrical impedance of an ICP source is a capacitor in series with a small resistor

2. Which of these equipments can be used for directional physical etching?

- A diode reactor
- A barrel reactor
- An atomic layer chemical vapor deposition system
- A chemical downstream reactor



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In this lesson we will introduce ion beam etchers, in which the substrate to be etched is not located within the plasma, but subjected to a beam of ions. One can also use ion beams to etch wafers. Ion beams originally were used for low-thrust space applications.

- Low energy ion beam sources originally were developed for use in low-thrust space applications
- If no volatile products are formed during etching process, physical sputtering is the dominant etching mechanism (e.g. Ar beam)
- Low operation pressure (10^{-4} - 0.1 mbar), collision-less transport, no re-deposition of sputtered material
- Easy to vary the angle of incidence of the ion beam onto the sample, which is impossible in a plasma-based process



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The main etching mechanism of an ion beam is physical sputtering due to the high kinetic energy of the ions. The technique uses a low operation pressure leading to large mean free paths and little or no re-deposition of material that is etched away from the substrate. Here we see an ion beam etching system. Inside such a system, it is possible to vary the angle of incidence of the ion beam onto the wafer, which is not possible in a plasma-based process. This picture shows the inside of the ion beam etcher.

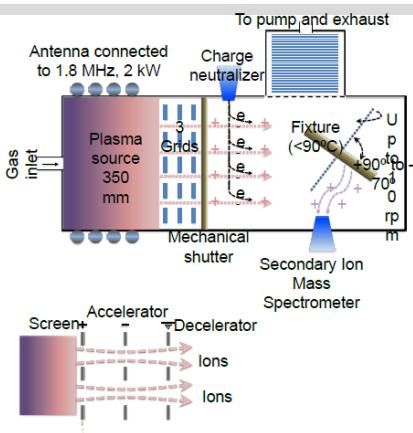


- Injection of a **reactive gas** directly into the ion source: Reactive Ion Beam Etching (RIBE)
 - Reactive ions (e.g. Cl^+ , Cl^{2+}) are extracted through grids and directed onto the sample with appropriate energy (few hundreds of volts)
 - No control of neutral radicals flux
- **Inert gas** is used in the ion beam and a flux of reactive gas may be added and is directed onto the sample: Chemically-assisted Ion Beam Etching (CAIBE)
 - Independent control of ion flux and neutral flux
 - Rapid diffusion of reactive gas (0.1 mbar) and ion source contamination possible

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Ions pass through this grid structure and will bombard the wafer, which is here placed on this fixture. An analytical, secondary ion mass spectroscopy equipment is incorporated to probe the evolution of the etching. Two main techniques are used in ion beam etching. One can inject a reactive gas into the ion source and then the technique is called reactive ion beam etching. Examples of such reactive ions are chlorine or fluorine ions. Use of a single reactive gas allows no independent control of ions, and neutral radicals flux in the system because there is only a single gas. The second option is to use an inert gas, like argon, for the ion beam. Then it is possible to add a flux of neutral reactive gas via another entrance close to the substrate. So here is the reactive gas, and then the argon ions come to bombard the wafer. This combination of physical etching with chemical activity of the second gas makes that one calls this chemically-assisted ion beam etching. (CAIBE) Here one can independently control ion flux and a neutral flux. However, an inconvenience (disadvantage) of this latter technique



- Argon ions are extracted from an ICP source, accelerated and directed to form a mono-energetic beam
- Uniformity and high collimation of the 350 mm ion beam is ensured by a three-grids collimation optics system
- A charge neutralizer that emits electrons is placed downstream from the ion optics in order to balance the charges in the sputtering beam and to avoid space or surface charging

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is that the reactive gas may diffuse through the system back through the grids and contaminate the ion source. Here we show schematic diagrams of the inside of the ion beam etchers. Argon ions are created in an ICP source and then are accelerated via three grids towards the substrate. The three grids on which different voltages are applied are schematically drawn here. After having passed through this grid structure, a charge neutralizer emits electrons to balance the charges in the ion beam to avoid excessive electrostatic charging in the reactor. The wafer is mounted on a fixture that can be rotated, so one can change the angle of impact on the wafer. The lower schematic diagram details the voltages applied to the three grid structures that are here. The first grid is for capturing electrons. The second one, for acceleration of the ions. And a third grid for slowing down the ions before being lead into the reaction chamber. What are the limitations and opportunities of ion beam etching? A clear limitation is posed by the low gas flow when the operating pressure needs to be as low as 0.1 millibar. To maintain a high etching rate under such conditions,

one needs a high ion flux while one does not want to enhance too much the ion energy for applications where this can cause damage to the wafer with possibly sensitive devices. Another limitation is that etching processes that consume or generate significant quantities of gas are not possible. An advantage of an ion beam source over a plasma reactor is found for special applications. For example, the ion beam has the possibility to expose the substrate at an angle. Also, etching in an ion beam system is more easy to understand as the number of species and possible chemical reactions are limited, contrary to what happens in a plasma reactor. It is possible to study specific etching processes where one applies, in a controlled way, ions and neutrals. Finally, we mention the existence of focused ion beam systems for the local etching at high resolution. The picture shows such a focused ion beam system. Such a system has a very narrow, single ion beam, and it has not the wide area uniform beam that we showed before



Focused Ion Beam system

- Limitation of the gas flow at an operating pressure of 0.1 mbar
 - In sensitive processes (ion energy below 100-150 eV), to maintain the etch rate, a high ion flux is needed, which is difficult to obtain with a remote ion source
 - Etching processes that consume/generate a significant quantity of gas are not possible
- Advantages over plasmas in specific applications
 - 45° etching shapes are possible
 - Characteristics of an ion beam are well understandable
 - Specific etching processes (ions/neutrals) can be studied
 - Focused Ion Beam (FIB) for local etching at high resolution

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for the etching of a complete wafer. The narrow ion beam allows local etching and sputtering of certain parts or devices on the wafer, like shown in this picture. So here one has selected a specific spot on the wafer and there, one has locally applied the focused ion beam to make a cross section through the interior of the wafer. A focused ion beam is therefore an important tool for process control as one can have access to any part of the wafer one wants, and one can analyze technological device aspects on a local scale. In this lesson we introduced the technique of ion beam etching, which is operated at low pressure and offers special possibilities in microfabrication, and fundamental studies of dry etching.

Summary

- Ion beam etching

Practice quiz ion beam etching

Questions:

1. What is the main advantage of Ion Beam Etching (IBE) to a plasma-based etching process?
 - High-aspect ratio structures can only be fabricated by IBE
 - The pulsed deep dry etching process of Si (Bosch process) is only possible by using IBE
 - The angle of incidence of the ion beam onto the sample can be varied and etching profiles with different angles with respect to the surface can be fabricated
 - The power consumption is extremely low
2. Which of the following is a limitation of IBE?
 - There are a lot of collisions of ions among themselves during their transport, which sometimes damage the sample surface
 - Operation pressure is quite high, which causes instability of long etching processes
 - The sputtered material redeposits on the sample surface if the operation pressure is kept too low
 - Etching processes which consume or generate a significant quantity of gas are not possible



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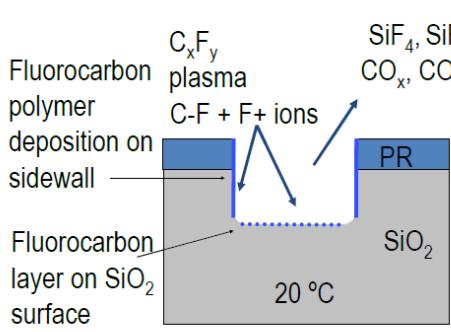
In this lesson we will give examples of a few dry etching processes of silicon based materials. We will subsequently discuss dry etching of silicon dioxide, silicon nitrite, and silicon itself. Etching of silicon dioxide, or silica, requires breaking silicon-oxygen bonds and the removal of both silicon and oxygen atoms.

Etching processes of Si-based materials

- SiO_2
- Si_3N_4
- Si

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In practice, one uses frequently carbon and fluorine chemistry generating volatile reaction compounds like silicon tetrafluoride, carbon monoxide, and carbon dioxide. Due to the stable silicon-oxygen bonds, one needs energetic ions to break these bonds. So one etches at low pressure where it is possible to have such highly energetic ions. The fluorine to carbon ratio is chosen in the middle between the etch and deposition regimes so that etching in the vertical direction occurs, while in the horizontal direction, where there is no electrical field, there is polymerization and hence no mask underetching.

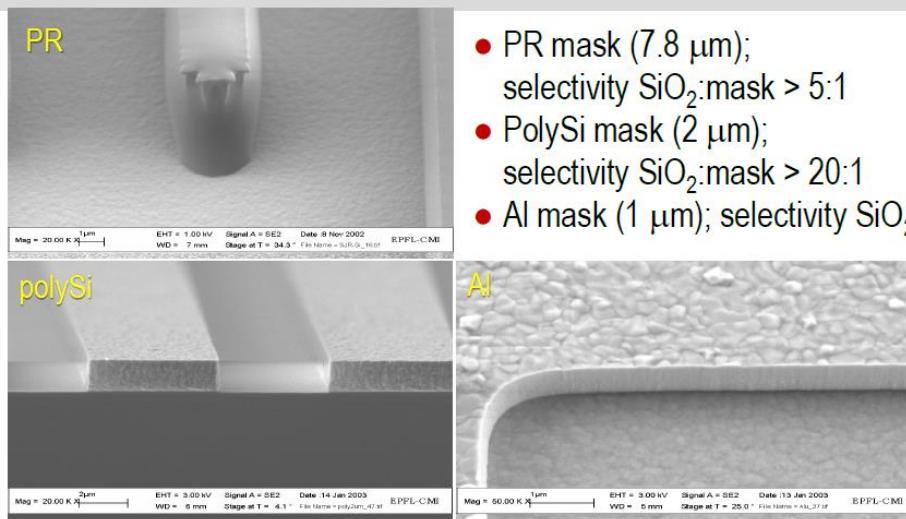


- Removal of Si and O atoms needed
- Use of C, F chemistry (C_2F_6 , CHF_3 , CF_4), resulting in volatile SiF_4 , CO, and CO_2
- **AND** energetic ions to break Si-O bonds (low pressure, hence energy >100 eV)
- F/C ratio chosen between the etch and deposition regime
- Wall reactor heating (>150 °C) to avoid polymer deposition

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The substrate is kept at room temperature during etching but the wall of the reactor can be heated at higher temperature to avoid polymer deposition there. This slide shows a few pictures of mask materials that are used for silica etching. The first picture presents a photoresist mask and one obtains here a selectivity towards silica etching of 5:1 for the conditions of the plasma used. That means the silica etches five times more rapidly than the photoresist. Polysilicon is a better masking material and one obtains a selectivity of 20:1. An aluminium mask is even better and has a selectivity of 50:1. This picture shows the result of the silica etching using a photoresist mask. The silicon dioxide layer that was etched has been deposited on a silicon wafer. One sees that the photoresist is more attacked on the top corners and is slowly eroded by the etching process. As gas for this etching, one has used C_4F_8 with CH_4 at a pressure of 5×10^{-3} millibar. The silica etch rate was 0.25 micrometer per minute. The top picture illustrates the etching of silica using a polysilicon mask. The silica layer that was deposited on the silicon substrate

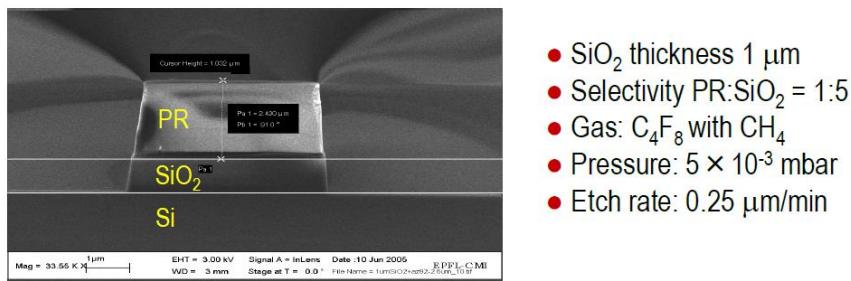


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had the thickness of 9 micron. One uses the same gases as in the previous slide but one can vary, of course, composition and substrate bias to optimize the anisotropic etching. The lower picture shows a circular hole that has been etched in a bulk silica wafer using a polysilicon mask. This slide illustrates a particular process that uses helium gas in combination with a halocarbon plasma with high carbon to fluorine ratio. That means one uses C_4F_8 with CH_4 or hydrogen. The top picture is the result of the etching without helium gas. And one sees that the sidewalls are not vertical. This changes when we add helium gas and one can obtain much more vertical sidewalls. The helium gas is inert but it is believed to increase the residence time of the active

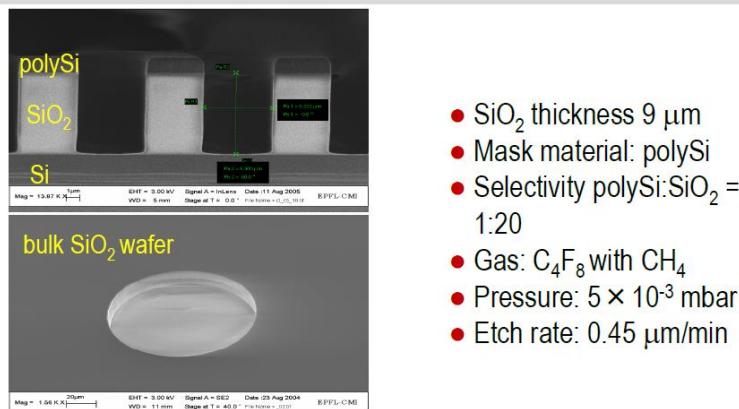
species at the bottom of the etched structures because of collisions with the helium gas. That is why etching becomes more efficient there resulting in more vertical sidewalls of the etched structures. In this example, one has used a strong negative substrate voltage bias of minus 300 volts. Pyrex, or borosilicate glass, has as ingredients mainly silica, but it contains also boron oxide, aluminium oxide, and sodium oxide.



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Pyrex is an interesting material because it has a low thermal expansion coefficient and a high chemical durability. In dry etching, one can use silicon as mask material and one obtains a selectivity towards Pyrex of 1:10 for a typical halocarbon gas etching condition. The pictures show dry etched channels and a chamber made in a Pyrex wafer. Silicon nitrite is an interesting material in microfabrication and is often used for thin membrane fabrication, as barrier layer in high-temperature oxidation processes, and as mask material for silicon wet etching. The silicon-nitrogen bond is a stable one and needs to be broken for etching to occur and subsequently the nitrogen and silicon atoms need to be removed. Pure fluorine chemistry with the gas SF₆ or halocarbon chemistry gases can be used. The reaction product is silicon tetrafluoride. Also, in this case, energetic ions are essential to break the silicon-nitrogen bonds so negative substrate bias is important. Now we will discuss three silicon etching processes. First, there is the deep anisotropic continuous etching of silicon at room temperature; then there is the anisotropic pulsed process, also known as the Bosch process, at room temperature; finally, we present a cryogenic process for silicon etching. We have already seen this slide before and it illustrates the continuous dry etching process for silicon. We already explained before how one can combine the etching gas SF₆ and the polymerization gas C₄F₈ to obtain anisotropic silicon structures using photoresist as a mask. We also have already introduced the dry etching of silicon using the pulsed, or Bosch, process. Here one alternates in time

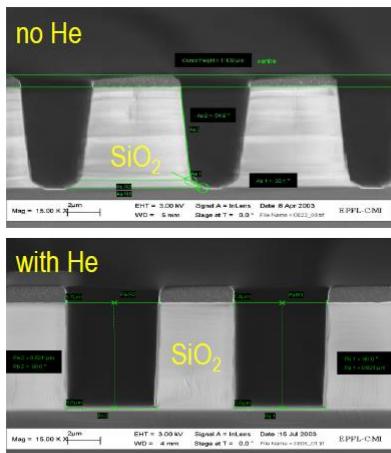


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the etching and the polymerization cycles. The picture on top shows how wider holes get etched deeper than the narrower holes because the gas can enter more easily a wider hole. The fact that the depth of the etching is not the same everywhere is also called the loading effect . The picture at the lower left shows a

detail of the structure with a scalloping effect characteristic for the Bosch process. One can clearly discriminate the different cycles of etching and passivation. The picture on the lower right shows a whole structure with still polymer layers that were attached to the side walls.

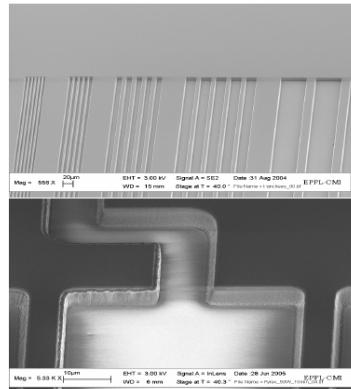


- Gas: high C/F ratio using C_4F_8 with CH_4 or H_2
- Pressure: 5×10^{-3} mbar
- He flow improves vertical etching (increases residence time of active species in a hole)
- High substrate voltage biasing (typically 300 V)

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The surface quality of etched microstructures in the pulsed process depends on the used etching conditions. We already have seen that the scalloping effect gives rise to non-planar sidewalls. If this corrugation is too important, one can reduce the etching and polymerization cycle duration. Sometimes when polymerization is not sufficient, we can see mask underetching , so here was the mask and there is a lot of attack in this direction, so there was strong mask underetching .



- Borosilicate glass or Pyrex has a typical composition $80 SiO_2 + \sim 10 B_2O_3 + 2 Al_2O_3 + \sim 5 Na_2O$
- Properties of Pyrex: low thermal expansion coefficient 3-5 ppm/ $^{\circ}C$, high chemical durability
- Etching mask material: Si
- Selectivity Si:Pyrex = 1:10
- Etching gas: C_4F_8 with CH_4
- Pressure: 5×10^{-3} mbar
- Etch rate: $0.45 \mu\text{m}/\text{min}$

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By increasing the relative importance of polymerization one can avoid such mask undercut like shown in this picture, which has the correct vertical wall at the right position. The picture here shows the bottom of an etched structure with a very smooth character. This was under good etching conditions. Sometimes one has redeposition of mask material into the hole which results in local micromasks that resist to the etching resulting in the formation of so-called "grass", as we see in this picture. The balance between etching and polymerization in the pulsed process is very delicate. If there is too much polymerization, micromasking effects due to the presence of polymer on the horizontal parts of the structure can give grass formation. When there is not enough polymerization the structure can simply disappear completely and one etches away all silicon. Here we see what was left from a silicon microstructure that has disappeared almost completely due to important etching in the horizontal direction, due to a lack of polymerization. Also the pressure of the etching gas is important. When it is too high, the mean free path in the gas is low which can give rise to reduced gas access and removal of reaction products

from the bottom of a hole structure. Therefore at the bottom of an etched structure we can have less vertical sidewalls as shown in this picture. This picture shows a condition where there was not enough polymerization. So in this case, not everywhere one has coated with polymer, and then laterally etched holes in the silicon appear. These two pictures illustrate other consequences of having not enough polymerization.

- Si_3N_4 main application is in membrane fabrication, as barrier layer in high-temperature oxidation processes, and as mask material for Si wet etching
- Both Si and N atoms need to be removed
- Pure F chemistry (SF_6) or F, C chemistry (C_2F_6 , CHF_3 , CF_4) can be used
- F atoms form SiF_4 and eventually C atoms form CN, but etching works without presence of C
- Energetic ions needed to break Si-N bonds

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This picture shows some bowing effect, some mask underetching, while the right picture shows a much higher width at the top than at the bottom, which is clearly a consequence of insufficient polymerization.

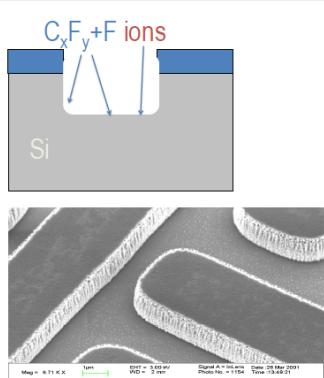
The scalloping effect of the pulsed process is again shown on this slide. The picture on the left shows a corrugation that is obtained when applying gas application times of 7 seconds for the etching gas and 2 seconds for the polymerization gas. If this roughness is too important one can reduce these times.

- Room-temperature deep anisotropic continuous etching process
- Room-temperature deep anisotropic pulsed process or Bosch process
- Cryogenic process

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The structure on the right was obtained by gas application times of 3 seconds and 1 second respectively.

And indeed, this structure benefits from a much reduced corrugation, hardly recognizable on this picture.

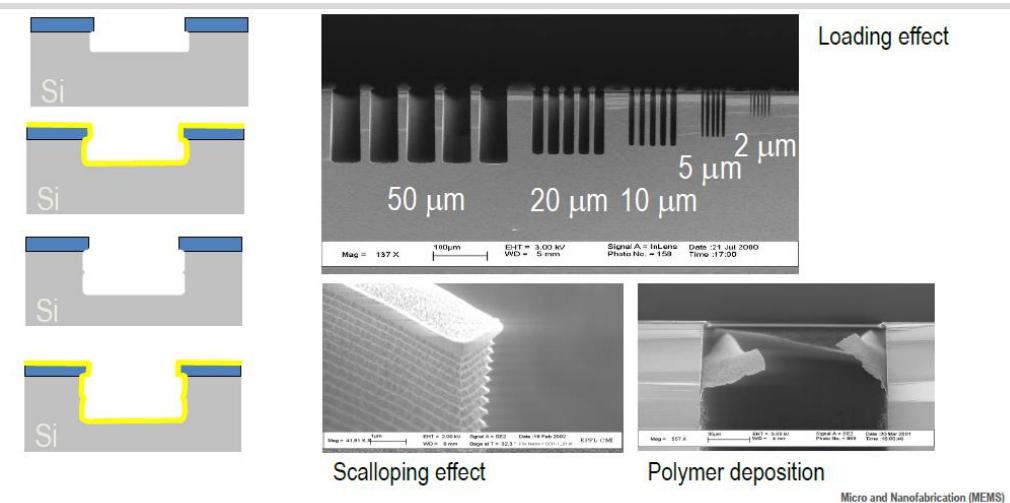


- Example: combining SF_6 and C_4F_8 chemistries, whereby C_4F_8 is the passivation gas
- Etching and passivation are simultaneous
- Substrate temperature typically is 20 °C
- Low etch rate: 1 to 3 $\mu\text{m}/\text{min}$ (good control possible)
- High selectivity to photoresist : > 50
- Smooth sidewalls, very anisotropic process

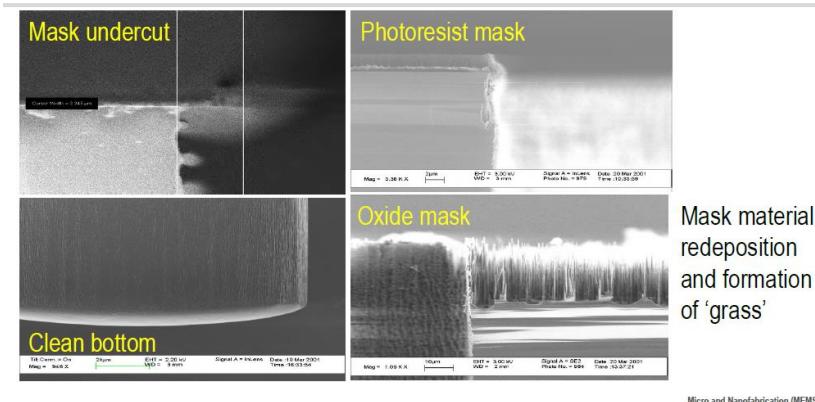
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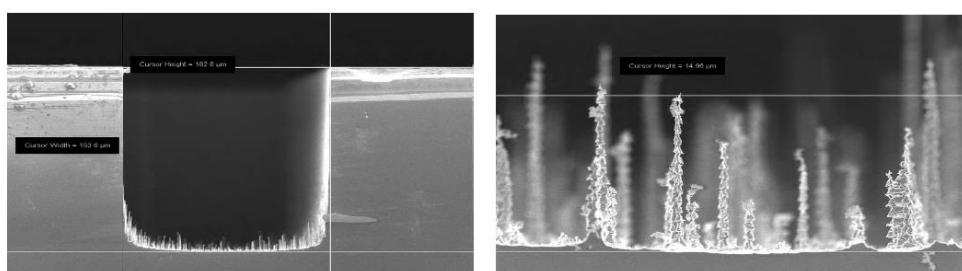
For some micromechanical applications, it is necessary to realize locally freestanding structures with vertical sidewalls. By applying a voltage between a freestanding structure and a fixed structure, one can, via electrostatic forces, activate the movable part-- for example, if this is a fixed electrode, and if one applies a voltage here, it will attract the movable part in a certain direction. An elegant way to realize such micromechanical devices is by using silicon on insulator wafers. These special wafers have a silicon dioxide layer embedded and beneath this layer is single crystalline silicon, on top of this layer is also single crystalline silicon. If one etches through the top silicon to reach the oxide one can then simply remove the silicon dioxide so that the top layer becomes suspended. So in this way we can make freestanding parts.



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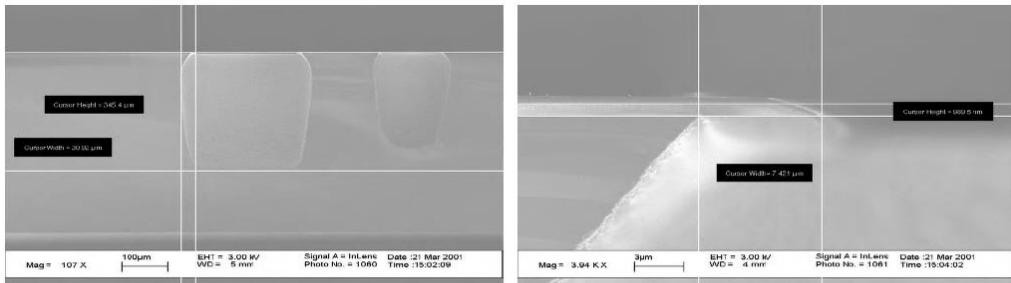


Bad equilibrium between etching and polymerization

- too much polymerization: grass formation
- not enough polymerization: disappearance of structure

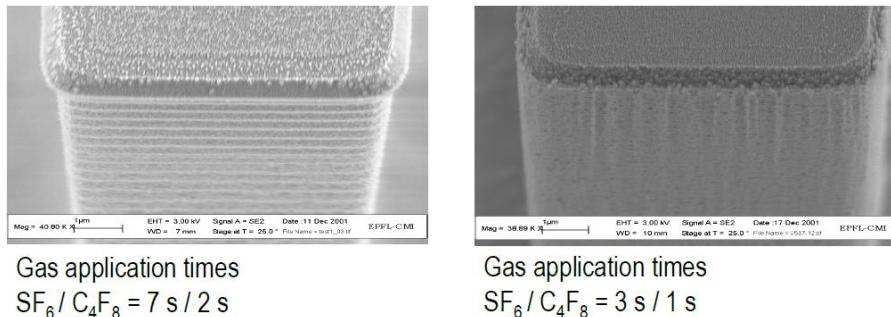
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Non-equilibrium between etching and polymerization:
not enough passivation leads to bad shape

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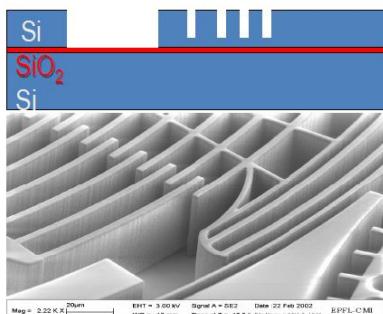
Gas application times
 $SF_6 / C_4F_8 = 7 \text{ s} / 2 \text{ s}$

Gas application times
 $SF_6 / C_4F_8 = 3 \text{ s} / 1 \text{ s}$

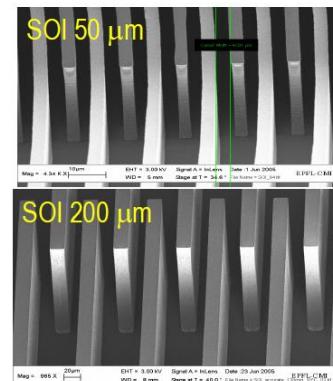
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These pictures show finger-like electrodes made by the pulsed etching process. And here one has etched through 50 micrometer, that is this dimension, or through 200 micrometer.



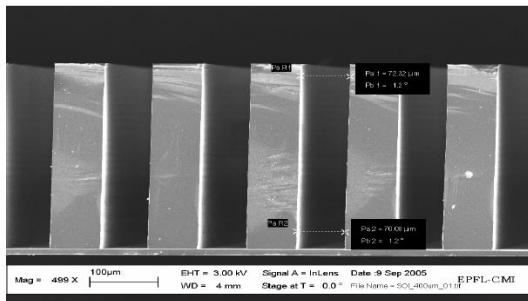
Application in mechanical microsystems and
inertial sensors with electrostatic actuators



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This picture shows another result of an optimized silicon on insulator wafer etching. The walls are nearly vertical and the etch rate can be very high: more than 6 micrometers per minute, in this case. The etch depth in this case was very high: 400 micrometers. However, one can also encounter unexpected results during the etching of an SOI wafer as shown in the pictures on the right. When going lower in the hole structure, one gets increased etching and roughness with even a much bigger hole etched just near the silica layer.

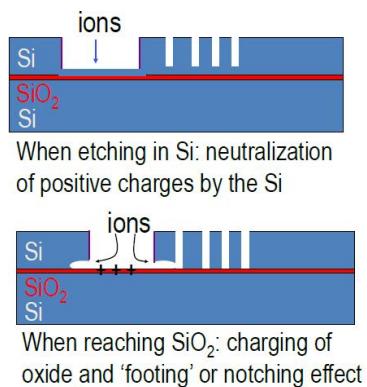


- Etch time: 60 min
- Etch depth: 400 μm
- Feature size: 70 μm
- Mask material: SiO_2
- Si: SiO_2 selectivity is 200:1
- Wafer diameter: 100 mm
- Etch rate: 6.6 $\mu\text{m}/\text{min}$
- Mask undercut: about 2 μm

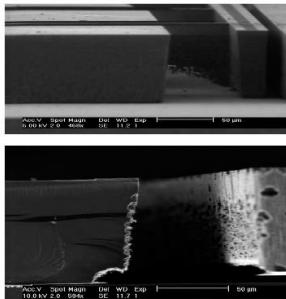
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This effect is known as the footing or notching effect and can be explained as follows: As long as one etches through the top silicon layer, as shown in this picture, the normal etching and polymerization cycles result in vertical sidewalls. However, when reaching the embedded oxide layer, due to its insulating properties, it can be charged by the ions from the plasma so that further incoming ions get deflected and give enhanced etching in this direction.

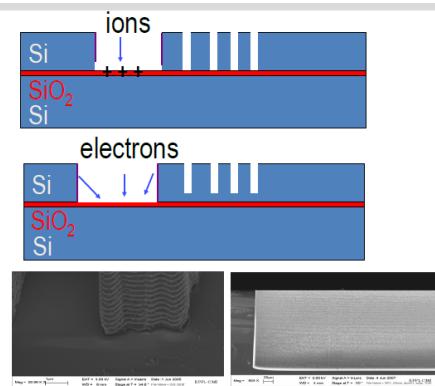


Continuous RF(13.56 MHz) voltage biasing



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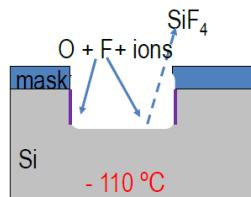


- Pulsed process with pulse duration from a few ms to tens ms with an adjustable duty cycle of 10 to 50%
- Ion bombardment is pulsed; in the period without energetic ion bombardment, electrons can discharge the buried SiO_2

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That is what we have seen here. And you see the same in this picture where the lower part of a narrow, movable beam has been etched away. This footing effect can be avoided when one gives sufficient time to the positive ions to be evacuated to the plasma. This is achievable by a pulse process with short pulse duration and reduced duty cycle resulting in a pulsed ion bombardment, and then one waits and there is a compensation of these charges by electrons from the plasma. In this way, structures with vertical sidewalls down to the oxide layer can be obtained as shown here. So this is the lower part of a silicon structure and this is the oxide layer. Another technique for the deep dry etching of silicon is the so-called cryogenic process

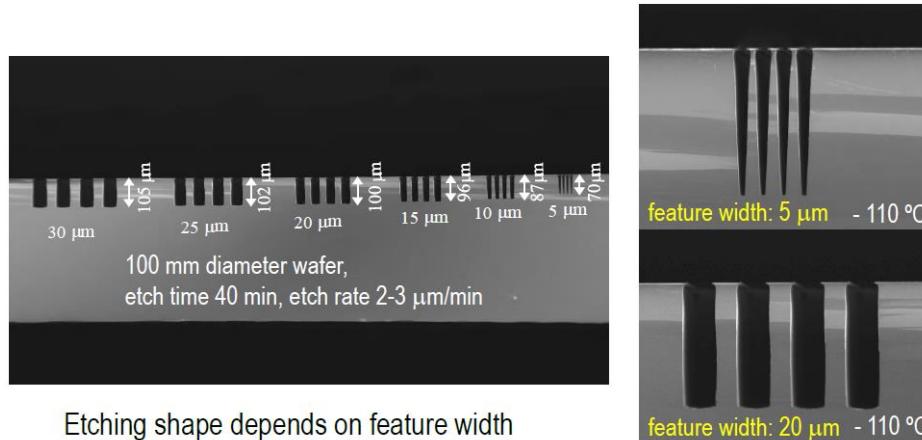


- SF₆ + O₂ chemistry
- O₂ is the passivation gas
- Etching and passivation are simultaneous
- Substrate temperature: -110 °C
- High etch rate: 1 to 10 µm/min
- Very high selectivity to thermal SiO₂ > 3000
- Very high selectivity to photoresist > 500
- Micro-loading and loading effects are present
- Advantages: free of polymer, no reactor contamination and smooth sidewalls

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The silicon wafer in this case is brought at a temperature of -110° Celsius. And one uses SF6 and oxygenchemistry. SF6 is the etching gas and oxygen is the passivation gas



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for protecting the sidewalls with oxides. This process does not require a polymerization gas which eventually avoids reactor contamination. High etching rates, up to 10 micrometer per minute, can be obtained. And at this low temperature there is a very high etching selectivity when using silicon dioxide or photoresist as the mask. So these are the selectivities which are indeed very high: 3000 and 500. These pictures show the etching performance of the cryogenic process. Holes with different diameters are etched and show vertical sidewalls indeed. For a hole with a feature width of 5 micrometers some mask underetching can be observed and there is a reduced etching rate at the bottom of such a narrow hole.



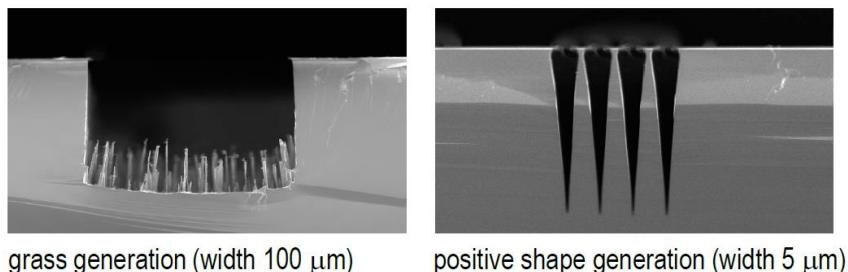
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The hole with the bigger feature width shows nicely vertical walls on the scale of the microstructure. The etching profile depends in a sensitive way to the temperature of the substrate which is also the temperature

of the chuck on which the substrate is fixed. If one raises the temperature from -110° Celsius, where everything goes pretty well, to -100° Celsius, mask underetching becomes much more important.

Increase of the O₂ flow rate leads to

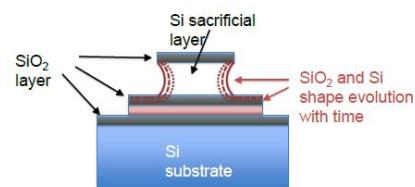
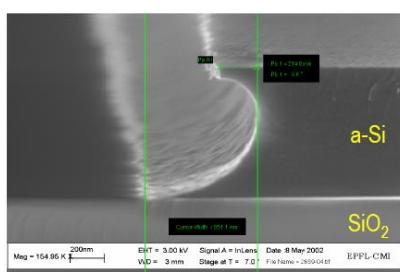


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Clearly the chemical reactions involved in the etching and sidewall protection in this process depend in a very sensitive way on the temperature. And the balance between the two processes is easily disturbed. Also, an oxygen flow rate variation can result in less well-defined hole structures. For example, we can see here grass at the bottom of an etched hole because there was too much oxygen supply. If there is too much oxygen, we will have too much passivation and we can also see deviations from verticality when etching through the wafer. While a lot of work has been focused on generating anisotropic silicon microstructures, it is of course also possible to design an isotropic dry etching process for silicon.

Use of a SF₆ plasma



Cross-section of an amorphous Si (a-Si) sacrificial layer and SiO₂ layer shape evolution during the release step

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Here one can use the gas SF₆ which has a predominantly chemical action on the silicon. The picture shows the result of such etching, while the diagram here shows the structure, how it was realized. It consists of several silicon dioxide layers and in between two of them is an amorphous silicon layer and it is this amorphous silicon layer that has been isotropically etched, which is shown in this picture here. This brings us to the end of this short overview of deep dry etching processes that are used in the clean room to etch important microfabrication materials like silicon dioxide, Pyrex glass, silicon nitrite and silicon. For anisotropic silicon etching we have introduced continuous room temperature etching where there is simultaneous polymerization and etching, followed by pulsed room temperature etching, where one alternates the etching and polymerization cycles. And finally, cryogenic etching where oxygen gas passivation replaces the vertical sidewall protection using polymer layers. Also we mentioned the isotropic etching of silicon in a pure chemical etching plasma.

Summary

- Dry etching processes of SiO_2 , Si_3N_4 and Pyrex glass
- Three processes for anisotropic etching of Si
 - Continuous room-temperature
 - Pulsed room-temperature
 - Cryogenic
- SF_6 process for isotropic etching of Si

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Practice quiz examples of etching processes for Si-based materials

Questions:

1. When in the Bosch process the pressure of the etching gas is chosen too high, it happens that initially vertical etched structures get a more and more tapered and less steep profile when etching deeper in the substrate. What is the main reason behind this?

- The increase of pressure in the etching gas causes a decrease of pressure in the polymerization gas and therefore polymerization gas accumulates in the bottom
- The mean free path in the gas is low, which can give rise to reduced gas access and removal of reaction products from the bottom of the structure

- The overpressured etching gas turns into deposition mode and it starts stacking on the bottom of the structures

- The etching gas is overexcited, which causes the amount of atoms per volume to decrease gradually

2. Which of the following is true for a cryogenic deep dry Si etching process?

- The chuck temperature does not have a significant influence on the etching profile

- The etching rate and the selectivity are low

- Addition of too much oxygen can cause grass generation

- The loading effect is eliminated for this process



Dry etching 7

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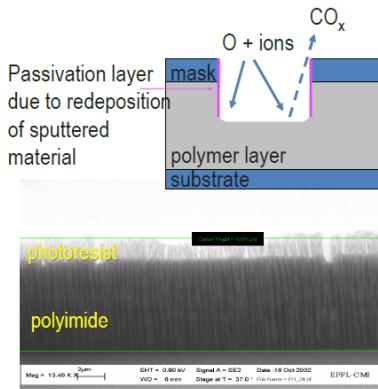
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While previously we have discovered some of the processes used in dry etching of silicon and silicon-based materials, now we focus on the dry etching of organic films, like photoresists, and the material, polyimide, and of metals. One typically uses an oxygen plasma for the etching of organic materials like photoresist, polyimide, etc. If one uses ion bombardment, one gets anisotropic structures when one exploits the redeposition of sputtered material to the sidewalls.

- Dry etching of organic films
- Dry etching of metals

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Etch products are water, CO gas, and CO₂ gas, typically. There is a vast choice in mask materials, like silicon, silicon dioxide, photoresist, or metal. The picture shows a photoresist mask, which was put on a polyimide film to etch a microstructure in the polyimide layer. These pictures show the etching of a 7 micrometer thick polyimide layer that was deposited on a silicon dioxide layer, and where one has used silicon dioxide as a mask. The silicon dioxide was deposited using a plasma enhanced chemical vapor deposition system because one can apply then

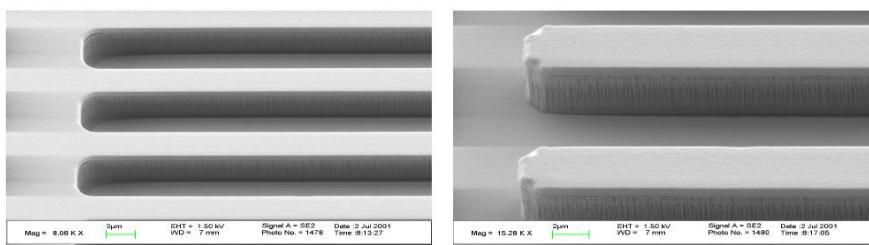


- Organic materials: photoresist, polyimide,...
- O₂ plasma
- Highly assisted by ion bombardment, leading to anisotropy
- Etch rate: 1 μm/min
- Etch products: CO_x and H₂O
- Mask materials: Si, SiO₂, photoresist (erodible), or metal (Ti, Pt, Al...)

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a relatively low temperature to the polyimide during deposition of the masking layer. The etching selectivity of the polyimide, with respect to the silicon dioxide, is over 50.

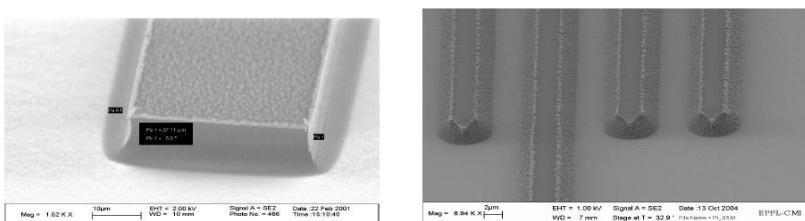


Etching of 7 μm depth in polyimide (stop on SiO₂) using a SiO₂ PECVD mask, selectivity PI:SiO₂>50

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These pictures show the result of polyimide etching using an erodible mask of photoresist. Both polyimide and photoresist have similar etching rate, so that the photoresist is gradually consumed during etching, especially at its edges. That is why the resulting polyimide structure has tapered sidewalls, as the photoresist mask at its edges became thinner first, and first disappeared there.



Polyimide etching using an erodible PR mask

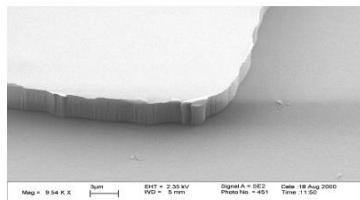
Polyimide etching with erodible mask to get tapered sidewall

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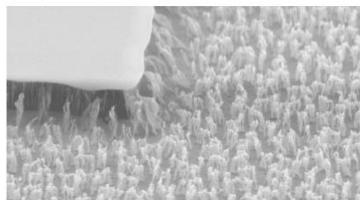
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A metal mask, like platinum or aluminum, is much more resistant to the plasma, and hence, can be used to etch structures with vertical sidewalls. This picture shows effects of aluminum redeposition in the etched structure. So, this material is removed, and it creates micro-masks in this region, resulting in the generation of grass as the etching proceeds. Generally, such redeposition phenomena can be reduced when one uses a plasma at the lower pressure, in which the mean free path of molecules is larger. In this case, sputtered

material can then be more easily evacuated from the zone of etching. Now we will give a few examples of dry etching processes for metals. We will discuss the etching of aluminum and aluminum alloys. These materials are used for making interconnecting structures on integrated circuits. They can also be used as membranes in switching applications, or as hard masks in a dry etching process. Next, we discuss the dry etching of platinum, which is an important material for microfabrication of electrodes.



Polyimide etching using a Pt mask



Polyimide etching using an Al mask
Problem of 'grass' at the bottom of features because of Al re-deposition

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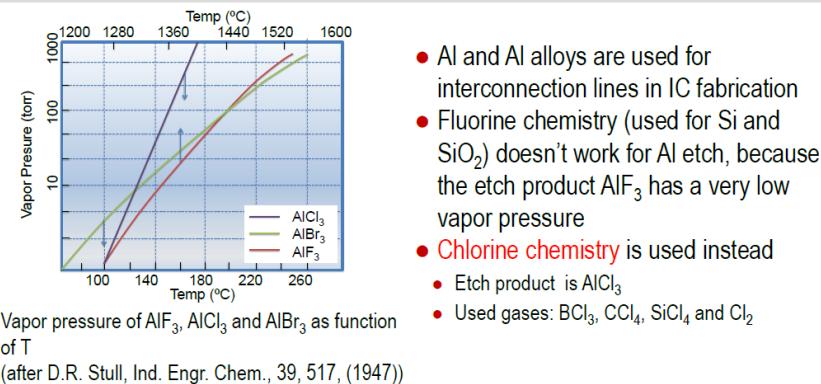
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Finally, we will discuss the etching of titanium, tantalum, tungsten, and molybdenum, which are frequently used as adhesion materials for the deposition of the noble metal, platinum, or aluminum. These materials also serve as hard masks in etching processes. Aluminum and aluminum alloys are used for making interconnection lines in integrated circuit fabrication.

- Al and Al alloys
 - Interconnections on IC's
 - Membranes (capacitive switches)
 - Hard masks
- Platinum (Pt)
 - Electrodes
- Titanium (Ti), Tantalum (Ta), Tungsten (W), and Molybdenum (Mo)
 - Adhesion layers for Pt and Al
 - Hard masks

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Because dry etching is a consequence of the use of a reactive gas, etching will be easier if the formed chemical product is more volatile. This diagram shows the vapor pressure as function of temperature for three reaction compounds. If one uses fluorine as a reactive gas, the formed aluminum trifluoride product has a relatively low vapor pressure, so this curve refers to this temperature axis. So, vapor pressure is significant only at very high temperature, much higher than used in etching. These temperatures are clearly too high for microfabrication. That is why fluorine chemistry, which is successful for silicon and silicon dioxide etching, does not work for aluminum. Instead, one can use chloride chemistry.



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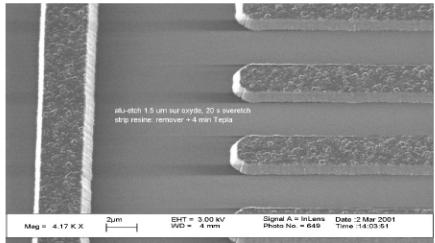
As the formed reaction product, aluminum trichloride, this curve refers to this temperature. So, for this material, one has an appreciable vapor pressure at much lower temperature, a temperature which is compatible with the dry etching temperature. The result is that this reaction product can be easily removed from the substrate after the chemical reaction. If one would have a pure aluminum surface that is not covered by an aluminum oxide layer, the reaction with chlorine radicals and molecules can immediately proceed. However, as aluminum is very reactive with oxygen, it always has a native aluminum oxide layer of about 30 angstrom, which should be etched away first. This thickness is, more or less, variable, and the oxide is so stable that there is no reaction with chloride atoms, except if sputtering with energetic ions is used. Then, only, the aluminum oxide can be dissociated, forming the volatile aluminum trichloride reaction product.

- If the Al surface is not covered by aluminum oxide (Al_2O_3), the reaction $\text{Al} + \text{Cl}$ or $\text{Cl}_2 \rightarrow \text{AlCl}_3$ can proceed
- The native Al oxide layer (about 30 Å) should be etched first
 - Thickness can vary from run to run
 - No reaction with Cl and Cl_2
 - Sputtering with energetic ions is needed
 - Chemical reduction is possible: BCl_3 or CCl_4 dissociation generates oxide species capable of reducing Al_2O_3
$$\text{Al}_2\text{O}_3 + \text{CCl}_x \rightarrow \text{AlCl}_3 + \text{CO}$$
 ions
- Water vapor in the chamber should be avoided
 - It scavenges the oxide-reducing species
 - It reacts with exposed Al to form Al_2O_3

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Also, one should avoid water vapor in the reaction chamber as water can easily react with the chlorine radicals and with the exposed aluminum to form aluminum oxide. Here, we show the etching of a 1.5 micrometer thick aluminum silicon alloy that was deposited on silicon dioxide. One has used photoresist as a mask, and obtained a selectivity around 1.5.



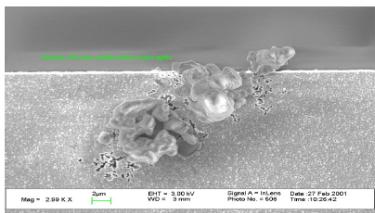
Anisotropic etching of $1.5 \mu\text{m}$ AlSi(1%) on SiO_2 ; photoresist mask; etch rate: $0.4 \mu\text{m}/\text{min}$; selectivity Al/PR ≈ 1.5

- Formation of an inhibiting layer on Al surfaces
- Removed on horizontal surfaces struck by energetic ions
- Nature of the layer: chlorocarbon polymers (CCl_x) from CCl_4 or from photoresist etch product
- With SiO_2 mask and no carbon-containing species in the plasma, isotropic etching will occur

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That is, the aluminum etches almost as fast as the photoresist. Anisotropic etching profiles are, more or less, obtained because one has used a chlorocarbon plasma that results in polymer deposition on these sidewalls. Also, redeposition of sputtered photoresist on the sidewalls is possible. If, instead of a photoresist mask, one would have used a silicon dioxide mask, and a plasma gas that did not contain carbon, or few carbons, one would have obtained a purely isotropic etching process.



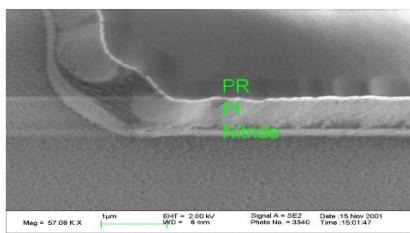
Anisotropic etching of $1.5 \mu\text{m}$ AlSi(1%) on SiO_2 , after waiting 24 hours before stripping of photoresist

- Chlorine-containing residues remaining on the film sidewalls
- Moisture absorption leads to HCl formation and formation of the Al corrosion product AlCl_3
- More severe problem in case of Al-Cu alloys etching, due to the galvanic couple between Cu and Al
- Can be avoided by rinsing wafer in DI water, plasma ashing (O_2) to remove PR and Cl atoms, restoring the passivating Al_2O_3 layer, or exposing Al to a fluorine plasma, replacing Cl atoms by F atoms

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Sometimes, we observe corrosion phenomena on the etched aluminum structures. This is believed to originate from chlorine-containing residues that remain on the etched film sidewalls. If these residues are combined with moisture absorption, the corrosive acid, HCl, forms, and this leads to aluminum corrosion products like aluminum trichloride. The problem is even more severe for aluminum copper alloys.



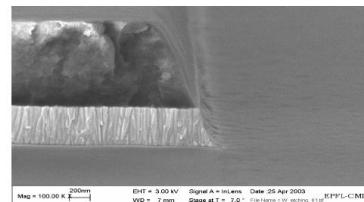
Anisotropic etching of $0.3 \mu\text{m}$ Pt on $\text{Si}_3\text{N}_4/\text{SiO}_2$, photoresist mask

- Etching in Ar/Cl_2 mixture
- Low pressure (few mbar)
- High bias (-200/300 V)
- Low etch rate: $0.03 \mu\text{m}/\text{min}$
- Low selectivity Pt:PR = 8

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Corrosion can be prevented by rinsing well the wafer in deionized water after removal from the chlorine plasma. Also, one can apply a plasma etching step in oxygen to remove residual photoresist and chlorine atoms, and at the same time, restore a thin passivating aluminum oxide layer. Another possibility is to expose the etched structure to a fluorine plasma, during which chlorine atoms are replaced by fluorine atoms.



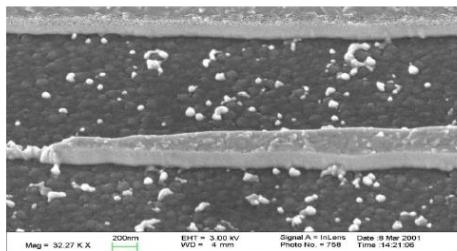
- Tantalum etching: fluorine chemistry (etch product TaF_3 vapor pressure 4 mbar at 25 °C)
- Tungsten etching: fluorine chemistry (etch product WF_6 vapor pressure 1.3 bar at 25 °C)

Etching of 0.5 μm W on SiO_2 using SF_6 chemistry; photoresist mask; etch rate: 0.5 $\mu\text{m}/\text{min}$; selectivity W:PR ≈ 1

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Here, we show the etching of a platinum film using a photoresist mask. The platinum was deposited on a thin silicon nitride layer on a silicon dioxide layer. The etch rate is very low, and the selectivity is also relatively low: 8, because the platinum is such chemically inert material. We have used here a low pressure argon chlorine mixed plasma with a high negative voltage bias on the substrate. In the picture, almost all of the photoresist has been consumed for etching through the platinum layer. The picture here shows the etching of a 0.5 micron thick tungsten layer deposited on a silicon dioxide layer, and one has used here fluorine chemistry and a photoresist mask. The selectivity is only 1.



- Titanium etching: chlorine chemistry (etch product TiCl_4 , vapor pressure 20 mbar at 25 °C) or fluorine chemistry (etch product TiF_4 vapor pressure 3×10^{-4} mbar at 25 °C)
- Molybdenum etching: fluorine chemistry (etch product MoF_6 , vapor pressure 700 mbar at 25 °C)

Etching of 0.2 μm Ti on amorphous carbon using chlorine chemistry, photoresist mask; etch rate: 0.1 $\mu\text{m}/\text{min}$; selectivity ≈ 2

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The etched product formed is tungsten hexafluoride. The metal tantalum can be etched in a very similar way. This picture shows the etching of a 0.2 micrometer thick titanium layer, which was deposited on an amorphous carbon film. One has used chlorine chemistry and a photoresist mask. The process has only a low selectivity, 2. When etching molybdenum in a fluorine plasma, similar results can be obtained. This ends our lesson on the dry etching of organic materials, like photoresist and polyimide and metals. Etching organic layers is a relatively easy task using a plasma, as volatile reaction products can be easily created. On the other hand, etching metals is more difficult, and one needs ion bombardment for etching to occur. Whether one uses a chlorine or a fluorine plasma depends on if a suitable volatile chemical reaction product can be formed at the temperature of the etching process.

Summary

- Dry etching of photoresist and polyimide
- Dry etching of metals that are used in microfabrication technology

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Practice quiz examples of etching processes for organic films and metals

Questions:

1. If polyimide etching is performed using an Al mask, there might be 'grass' at the bottom because of Al re-deposition. How can this problem be solved?

- The plasma can be used at a lower pressure, resulting in a higher mean free path of the sputtered material reaction products
 - An erodible mask can be used instead
 - After the grass formation, the wafer can be placed in an oxygen plasma chamber to remove this layer
 - A thin Si_3N_4 layer can be predeposited on the surface of the wafer to avoid this accumulation
2. Sometimes, in Cl plasma etching, a corrosion phenomenon is observed in Al etching under the form of chlorine-containing residues remaining on the film sidewalls. Which of the following is a correct approach to avoid this problem?
- Exposing the etched structure to a fluorine plasma immediately after the Cl plasma
 - Immersing the wafer in HF
 - Dipping before etching the wafer in isopropanol alcohol solution
 - Applying an oxygen plasma to transform the Al completely in to Al_2O_3

Conclusion and summary

In this module on dry etching we introduced directionality and anisotropy of a dry etching process in a plasma reactor. We discussed dry etching reactors and ion beam etchers and presented also dry etching processes that use intrinsically reactive gases and that do not require to have the gas in the plasma state. We presented examples of specific dry etching processes for silicon dioxide, silicon nitride, silicon, polymers and metals. Here are a few important key points you should remember.

Dry etching basics

- Dry etching is due to molecules in the gas phase, which is a so-called ‘dry’ medium, and is typically in the 0.1 to 200 mbar pressure range. Generally the gas becomes reactive to the material to be etched away when it is brought in the plasma state.
- Depending on the type of gas, the action of the gas can be chemical, which can be either etching (example: high F-containing gas) or polymer deposition (example: high C-containing gas); the action of the gas can also be physical sputtering (example: Ar gas).
- A lower F/C ratio of the feed gas and higher physical ion bombardment of the surface due to a more negative surface bias permit to obtain more anisotropically etched structures.
- For deep dry etching of silicon, one can design a plasma-based etching process by combining the gases SF₆ and C₄F₈ in the etching reactor. The first gas is an etching gas, as it contains a lot of fluorine, while the second is a passivation gas, as it contains a lot of carbon. The substrate bias has to be chosen such that there is an effective vertical etching rate, while the horizontal etching rate should be zero due to the hole sidewall protection by the deposited polymer.
- It is also possible to apply the etching and polymerization gas sequentially in a pulsed process, known as the Bosch process.
- Xenon fluoride gas etching of silicon without development of a plasma requires a much simpler equipment than a plasma etcher. The xenon fluoride is placed in the form of solid crystals into a closed reactor from which fluorine vapor is released, which etches the silicon.
- Silicon dioxide can be etched without a plasma using HF vapor. The technique can be used to remove an oxide layer underneath an etched silicon micro structure to provide a freestanding mechanical MEMS structure without having to use a liquid etching bath.

Theoretical concepts in dry etching

- Close to an electrode in the plasma, electrons are repelled, so that mainly ions and, of course, neutral molecules remain. Such layer close to an electrode is therefore called an ion sheath.
- A glow discharge plasma is characterized by a lack of thermal equilibrium between the electron temperature and the gas temperature. The gas temperature is typically at room temperature, that means a few hundred Kelvin, while the calculated electron temperature is typically 10 000 Kelvin. Due to the low gas temperature, a glow discharge plasma is therefore called a cold plasma.
- A negative voltage bias can be developed over the substrate-carrying working electrode and during etching one reaches an equilibrium electron/ion transport regime with strong ion impacts on the working electrode.
- What we aim for in etching is that ions are predominantly accelerated by the large total voltage near the lower electrode, where the wafer to be etched is positioned, while we do not aim to create ion bombardment to the top electrode, which would damage the reactor. This can be achieved by choosing the lower electrode area smaller than the upper electrode area.

- Decoupling of the plasma generation from the generation of the substrate bias was exploited in the newer etching reactors, for which electron cyclotron resonance sources, inductively couple plasma sources and helicon sources were developed.

Specific dry etching processes

- A barrel reactor exploits a chemical oxygen plasma to remove polymers or photoresist from a wafer. The technique is also called plasma ashing or plasma stripping. There is no ion bombardment in this technique and chemical action from the oxygen atoms and UV radiation are solely responsible for the etching.
- Physical sputtering due to the high kinetic energy of the ions is the main etching mechanism of ion beam etching. The technique uses a low operation pressure, leading to large mean free parts and little or no re-deposition of material that is etched away from the substrate.
- Etching of silicon dioxide or silica requires breaking the Si-oxygen bonds, and removal of both silicon and oxygen atoms. In practice, one uses frequently carbon and fluorine chemistry, generating volatile reaction compounds like silicon tetra fluoride, carbon oxide and carbon dioxide.
- For etching silicon nitride, one needs to break the stable silicon-nitrogen bond for etching to occur, and subsequently the nitrogen and silicon atoms need to be removed. Pure fluorine chemistry with the gas SF₆ or halocarbon gases can be used. The reaction product is silicon tetra fluoride.
- Deep anisotropic continuous etching of silicon can be obtained at room temperature, but also using an anisotropic pulsed process, known as the Bosch process. Also a cryogenic process for anisotropic silicon etching was developed.
- One typically uses an oxygen plasma for the etching of organic materials like photoresist, polyimide, etc. If one uses ion bombardment, one gets anisotropic structures when one exploits the deposition of sputtered material on the vertical planes. Etch products are water, CO gas and CO₂ gas, typically.
- Fluorine chemistry, which is successful for silicon and silicon dioxide etching, doesn't work for aluminum. Instead, one can use chloride chemistry, as the formed reaction products have higher vapor pressure at lower temperature and can then be more easily removed from the substrate after the chemical reaction.

Chapter 6: Wet etching (WE)



Introduction and objectives

Wet etching (WE)

This module on wet etching describes etching in a liquid environment. We will introduce anisotropic wet etching of silicon substrates, where certain lattice planes are etched and others not, isotropic etching of silicon, and finally thin membrane microfabrication techniques using wet etching. We will also explain the hydrofluoric acid or HF bath that is used for silicon dioxide and glass wet etching. We will discuss applications of wet etching, like wafer cleaning and removal of sacrificial layers underneath a functional layer to realize free-standing structures. We will illustrate the potential of anisotropic etching for bulk micromachining, which is microfabrication by etching through bulk parts of a wafer. Finally, we will discuss electrochemical etching of silicon substrates for making porous silicon.

At the end of this week, you should be able to:

- Know anisotropic etching of silicon substrates, a process in which certain lattice planes are etched and others not.
- Know the mechanism and applications of the hydrofluoric acid or HF bath that is used for silicon dioxide and glass wet etching.
- Know the mechanism and applications of the so-called HNA bath for isotropic etching of silicon, a mixed bath that consists of nitric acid, HF, and acetic acid.
- Understand how wet etching can be used to fabricate thin membranes and how microstructures can be used to diagnose stress in thin films or membranes.
- Be aware of applications of wet etching, like wafer cleaning or removal of sacrificial layers underneath a functional layer to realize free-standing structures.

- Know the technique of electrochemical etching of silicon substrates for making porous silicon.



Wet etching 1

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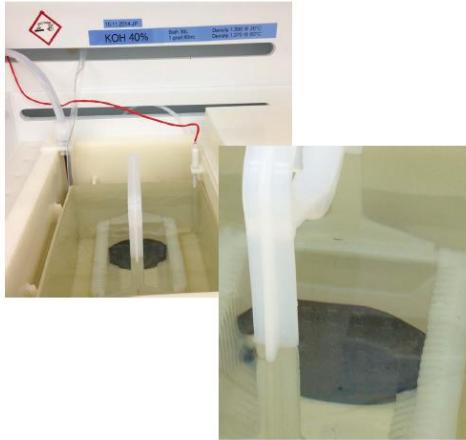
Prof. Jürgen Brugger & Prof. Martin A. M. Gijs

This is our introductory lesson on wet etching where one uses liquid chemical baths to etch away materials. Wet etching can be used to etch away thin films that are locally not protected by a mask, but one can also etch through thick substrates.

- Thin films
- Thick Si substrates
 - Anisotropic etching
 - Isotropic etching
 - Thin membrane microfabrication
- Applications
 - Wafer cleaning
 - Removing sacrificial layers to realize free-standing structures
 - Electrochemical etching for porous Si

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In the present lesson we will introduce several topics which will be more completely discussed in upcoming lessons. We will introduce anisotropic etching of silicon substrates where certain lattice planes are etched and others not. We will discuss isotropic etching baths of silicon and finally how we can make thin membranes using wet etching. We will then discuss applications of wet etching, such as wafer cleaning and removal of sacrificial layers underneath a functional layer to realize free-standing structures as has already been presented in a previous lesson on dry etching. Finally we will discuss electrochemical etching of silicon substrates for making porous silicon.

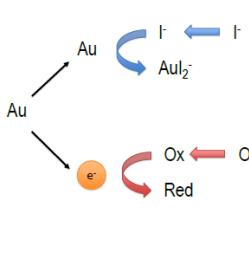


- Use of a liquid bath for removing material
- Baths exist for all type of materials (metals, oxides, polymers,...)
- Based on a chemical reaction
 - Transport of etching solution to the material (by diffusion or agitation)
 - Occurrence of chemical surface reaction generating soluble reaction product
 - Transport of reaction product away from the surface
 - The slowest step of these determines the reaction rate

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As the name wet etching says, we will use a liquid bath for removing material. Chemical baths exist for all types of materials, like metals, oxides, polymers and so on. As there is a chemical reaction involved, the different stages of an etching process involve, first, the transport of the etching solution to the material to be etched. And this can be done by diffusion or by agitation in the bath which is faster than a purely diffusion-like transport. Then one should have a chemical surface reaction that generates a soluble reaction product. And finally, one has to transport the reaction product away from the surface, and this is mostly by diffusion or by agitation. The slower step of these three determines the actual reaction rate.



- Important material for interconnections, contacts, etc..
- Example: iodine-iodide system (0.6 M KI and 0.2 M I_2 aqueous solution; etch rate of about 1 $\mu\text{m}/\text{min}$ at room temperature)
- Oxidant is needed for electron transfer, in this case the triiodide ion I_3^-
- Complexing ligand is needed for gold dissolution

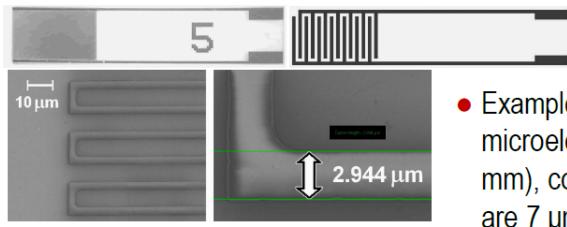
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The two pictures illustrate the etching of a silicon wafer which was immersed in a KOH bath. As an example of thin filler material that can be etched, we present here the etching of gold films. Gold is an important material for interconnections and for making contacts due to its very inert character.



- Isotropic etching process, resulting in widening of etch features over time
- For Au, a thin adhesion layer, like Cr, is necessary to apply



- Example of interdigitated microelectrode sensor (3.2 mm x 16.0 mm), consisting of 500 fingers that are 7 μm wide with 3 μm gaps)

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For etching gold, one needs a special bath as it is not easily etched by common etching solutions. A popular bath is the iodine-iodide system which is made by adding iodine and potassium iodide to an aqueous solution. One obtains an etching rate of about one micrometer per minute at room temperature. The mechanism of this bath is the following: Iodine and a negative iodide ion recombine into a tri-iodide ion. By reception of two electrons, this is converted in three iodide ions.



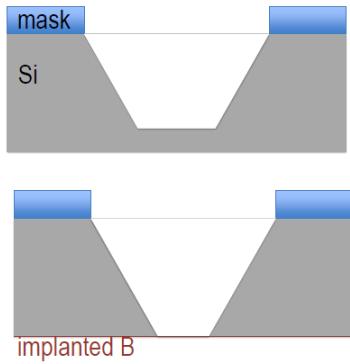
- A silicon substrate is about 500 μm thick and is single-crystalline material
- Both **isotropic** and **anisotropic** etching baths exist
- Anisotropy results from the fact that atoms in certain planes are more bound than in other planes and is hence a direct consequence of the single-crystallinity
- While **acidic baths** etch Si in an **isotropic** way, **alkaline baths** result in **anisotropic** etching



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The gold atom reacts with two iodide ions that forms a complex that goes into the solution under the release of an electron. This is a purely chemical etching process, so that etching occurs in all directions. If you have a gold film covered by a photo-resist masking layer etching goes both in the vertical and the horizontal direction. The structure gets more and more underetched with time and the underetching only stops when one removes the substrate from the etching solution. In order to avoid a too-important mask underetching, one needs to control the etching time.

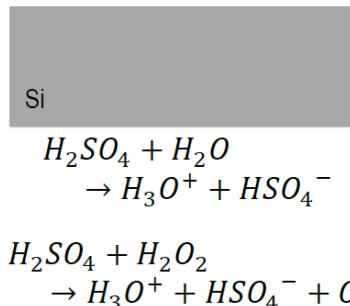


- A silicon substrate is about $500 \mu\text{m}$ thick and is single-crystalline material
- Anisotropic etching in a KOH bath can be designed into a 'self-stopping' process resulting in very thin membranes (of order $1 \mu\text{m}$) by implanting B in the membrane layer; no need to control the etching time
- A thin membrane can be used, for example, in pressure sensors, thermal sensors, etc..
- This is an example of 'bulk micromachining'

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A problem that can occur when depositing gold directly on a substrate is that it can be easily peeled off due to the weak film-to-substrate interaction. Therefore, often one deposits a very thin metal adhesion layer, like chromium, just before the position of the gold. The pictures below illustrate the gold etching process. Here one has made an interdigitated electrode structure as schematically illustrated here. In reality, there are much more of these fingers, more than 500 in this area, which you cannot see anymore in this picture. This is a detail of these electrodes where you see that we have seven micron-wide electrodes with three micrometer-wide gaps.

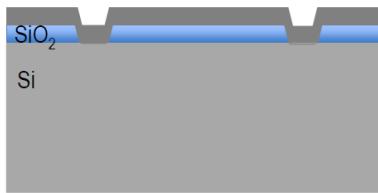


- Piranha solution is a mixture of concentrated sulphuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2)
- It is used for cleaning of organic residues (e.g. from photoresists) on wafers
- 1st process: rapid (violent) dehydration by H_2SO_4
- 2nd process: generation of reactive oxygen species that can dissolve elemental carbon

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Next, we introduce etching of a hole in a silicon substrate. The substrate is covered by a masking layer with an opening. Both isotropic and anisotropic etching baths exist. If one has an isotropic etching bath, etching proceeds both in a vertical and in a horizontal direction, so mask underetching occurs. If one has an anisotropic etching bath, etching does not occur for certain directions or certain planes of the silicon crystal structure. For example, here etching stops when the etchant comes into contact with this plane.

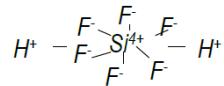
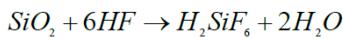


- A thin membrane can also be made by removing a sacrificial layer beneath a functional layer
- Step 1: patterning of SiO_2 sacrificial layer
- Step 2: deposition of polySi layer (for example by LPCVD)

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Such anisotropic etching results from the fact that atoms in certain planes are more bound than in other planes and that we have a single-crystalline substrate and that the etching bath is only strong enough to remove the weaker bound atoms here and leave the stronger bound atoms on these planes. While acidic baths etch silicon in an isotropic way, alkaline baths usually result in anisotropic etching. Anisotropic etching baths can also be used for making very thin membranes of the order of one micrometer thickness. The single crystalline silicon substrate normally is around 500 micrometers in thickness. If we have, again, our mask opening structure and we put the silicon wafer in an alkaline potassium hydroxide or KOH bath, the etching stops at a certain plane of the crystal, we will see later in more detail.



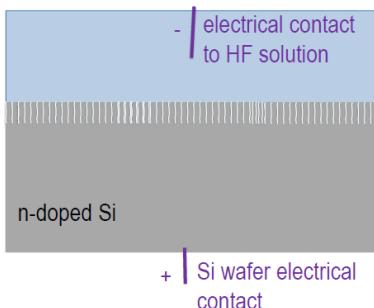
- A thin membrane can also be made by removing a sacrificial layer beneath a functional layer
- Step 1: patterning of SiO_2 sacrificial layer
- Step 2: deposition of polySi layer (for example by LPCVD)
- Step 3: wet etching of SiO_2 in a HF bath forming fluorosilicic acid (H_2SiF_6) and water
- This is an example of '**surface micromachining**'

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So there is no etching for these planes here. If we proceed in time, the thickness of the silicon layer in the middle becomes always smaller but it is impossible to stop this process exactly when there is only one micrometer left by just looking at the time of the etching process. Instead, as we will see later, one can implant boron in a very thin layer and when the KOH etchant reaches this boron-implanted layer, the etching stops. This technique of microstructuring a whole substrate wafer for making a thin membrane or device, is also called **bulk micromachining**, as one etches away part of the bulk of the substrate. As an example of a wet etching application, we discuss here the so-called **piranha** wafer-cleaning procedure. A piranha solution consists of a mixture of concentrated sulphuric acid and hydrogen peroxide. It is used for removal of organic residues like photoresists from wafer surfaces. The schematic diagram illustrates some organic residues that have been left on a silicon wafer. These organic residues are first attacked by the sulphuric acid, which violently dehydrates the organic molecules. These get a black appearance as water molecules have been extracted and a carbon-based structure remains. Subsequently, a second reaction starts: the sulphuric acid reacts with the hydrogen peroxide to produce atomic oxygen, which can dissolve elemental carbon. After these two reactions in the process, all organic residues are removed from the surface. This movie illustrates the violent cleaning of a substrate in a piranha bath. One first prepares the sulphuric acid at the right

temperature and then adds the hydrogen peroxide, which results in the development of fumes. In this bath, a silicon wafer is immersed and cleaning proceeds here at a temperature above 130 degrees celsius. The violent action of the bath on the substrate is like the attack of piranha fish on their prey and this fact gave the bath its name. Before we have seen that one can use bulk micromachining to realize a thin membrane on a wafer. Now we will see that wet etching permits to make thin membranes by another way. This technique uses the removal of a so-called sacrificial layer by the wet etching bath from beneath a functional layer. The first step in this process is the deposition and patterning of a sacrificial layer, in this case, a silicon dioxide layer. This patterning can be by dry or wet etching of this oxide layer. The next step in the process is deposition of a functional layer, and this can be polysilicon in our example. It can be deposited by a low-pressure chemical vapor deposition technique. The final step in the process is the wet etching of the silicon dioxide



- Si can be made micro- or nano-porous by etching in a HF bath under certain conditions
- The unidirectional pores provide a large effective surface area and create a mechanically more fragile material

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using an HF bath, forming fluorosilicic acid as a reaction product. This is a fluorosilicic acid molecule. To remove the silicon dioxide from underneath the polysilicon layer, evidently one needs locally some access holes through the polysilicon layer so that there is access to the HF bath. Such a process where one makes a very thin membrane on top of a wafer is an example of a so-called surface micromachining process. As a final application example of wet etching micromachining, we mention here the realization of so-called porous silicon. We will see later that silicon can be made micro- or nano-porous, as illustrated by these pores in the drawing, by etching the wafer in an HF bath while connecting the wafer to a positive voltage and the counter-electrode is in the HF solution. Doing so, one can create unidirectional pores that go into the silicon and that have a large effective surface area per wafer surface. Also, we can create locally at the top of the wafer a mechanically more fragile material due to the presence of so many pores. This ends our introduction of wet etching. We have seen the isotropic etching of a thin gold film and subsequently, we have shown the phenomena of anisotropic and isotropic etching of a bulk silicon substrate. As well as the realization of a thin membrane in a silicon substrate, a technique we called bulk micromachining. Then we introduced wet etching applications such as piranha wafer cleaning, the removal of a sacrificial layer underneath a functional layer, a technique we called surface micromachining. Finally, we discussed the realization of porous silicon in an HF bath, under application of a voltage bias on the silicon wafer.

Summary

- Thin Au films
- Thick Si substrates
 - Anisotropic etching
 - Isotropic etching
 - Thin membrane microfabrication; bulk micromachining
- Applications
 - Piranha wafer cleaning
 - Removing sacrificial layers; surface micromachining
 - Porous Si

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Practice quiz anisotropic and isotropic wet etching of Si and applications

Questions:

1. Which one is a useful step for fabricating a thin Si membrane by wet etching starting from a monolithic Si substrate?

- Instead of taking pure Si, take a wafer which is completely doped with boron at a concentration above 10^{14} atoms/cm³
- Placing the Si wafer in a KOH anisotropic bath
- Immersing the Si wafer in Piranha solution
- Dipping before etching the wafer in a concentrated acetone solution

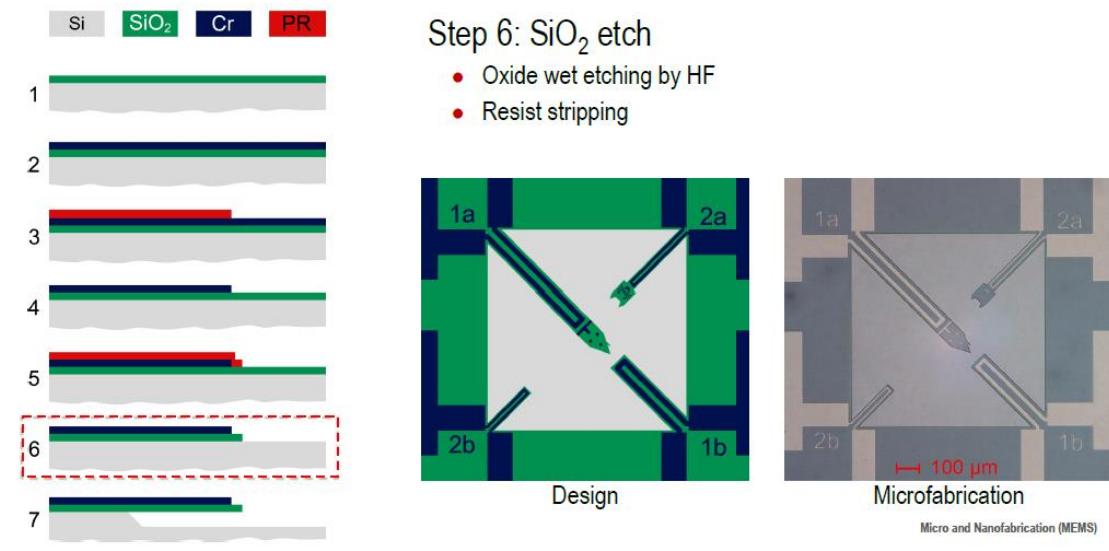
2. In surface micro-machining, a thin Si membrane can be fabricated by removing a SiO₂ sacrificial layer beneath a Si functional layer. Which of the following is true for this process?

- No access holes are needed on the polySi to remove the SiO₂ layer by wet etching
- The SiO₂ layer can only be patterned by KOH etching
- Wet etching of SiO₂ is performed by adding an electrical contact to the Si wafer
- A polySi layer is deposited in the form of a thin film on top of a patterned SiO₂ layer

HF bath for SiO₂ and glass wet etching



In this lesson, we will explain the hydrofluoric acid or HF bath that is used for silicon dioxide and glass wet etching. This type of etching was already used in the process for the microfabrication of the thermal mechanical micro-activator for locally removing the silicon dioxide layer to define the oxide cantilever beam. We used a diluted HF solution, known also as buffered hydrofluoric acid , or BHF , and locally protected the chromium and silicon dioxide layer by a photoresist.

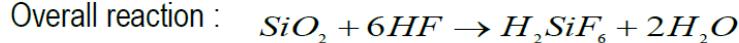


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During the buffered hydrofluoric acid etch, the chromium layer was then completely covered with the photoresist, so that it is not affected by the HF solution. Here, I show again the mask design of the micro-activator, and this is the result after this processing step. Glass is dissolved by HF or HF-containing solutions. When HF is dissolved in water, it is a weak acid. That means it is partially split in protons, fluorine ions, and HF₂ minus ions. Vitreous silicon dioxide and multicomponent silica glasses are etched according to this overall reaction, where this compound is called fluorosilicic acid, so this is the molecule that goes into solution, and that originates from the silicon dioxide. These are the two reaction constants at 25 degrees

Celsius. K1 describes the splitting of HF into protons and fluorine ions, and the fact that this number is not large means that it's a weak acid. A second reaction constant says that also HF₂ minus ions are present in the bath, and in comparable concentration to the fluorine ions. It's revealed by this number. Sodium fluoride or ammonium fluoride are known to not etch silicon dioxide, so that means that it is not the fluorine ions that are responsible for the etching. Also, the etching is not sensitive to agitation of the bath and that means it's not a question of transport, but it's kinetic control of the reaction at the surface which is the limiting step.

- Glass is dissolved by HF or HF-containing solutions
- HF in water is a weak acid; the solution contains H⁺, F⁻ and HF₂⁻ ions
- Vitreous SiO₂ and multicomponent silica glasses are etched



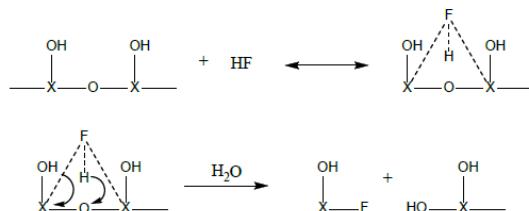
- Reaction constants at 25 °C : $K_1 = [\text{H}^+][\text{F}^-]/[\text{HF}] = 6.7 \times 10^{-4} \text{ mol/l}$
 $K_2 = [\text{HF}][\text{F}^-]/[\text{HF}_2^-] = 0.26 \text{ mol/l}$
- NaF or NH₄F do not etch SiO₂ → reactivity of F⁻ ions is negligible
- Insensitivity of etch rate to agitation → etching is kinetically controlled

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The following etching mechanism is believed to occur. HF is chemisorbed on the silicon oxide network, and there is a combined action of the hydrogen on the oxygen atom, and of the fluorine to the silicon atom, which weakens the bond between the silicon and oxygen. This is a so-called siloxane bond. At the end, this bond breaks, and the network is cut in two parts. The etching rate can be written by the following formula: theta is the degree of coverage of active adsorption sites on the glass, so this means that there are protons on the surface. This says that the etching rate is there if there are protons on the surface, and there is a second species, which is necessary: these are HF₂ minus ions. So, this says that there is a combined action of the two to etch. And also this protein concentration is working together with HF, together, to remove the silicon dioxide. There is another process where there are only protons, so only protons can already dissolve the silicon dioxide. In practice, the etching rate in the HF bath, at this temperature, is a few micrometers per minute for 50 weight percent of HF in water. An etching bath that is frequently used is the one in which one adds the non-etching ammonium fluoride to the HF baths.

- Nucleophilic chemisorption of HF to a X-O (X=Si) network
- Opening of silica surfaces from dissociated water species
- H⁺, HF₂⁻ and HF adsorb on lattice bonds
- Rate-determining step : breakage of siloxane bond by combined action of the adsorbed species
- Etching rate = $k_1 \cdot \theta(\text{H}^+) \cdot \{k_2 \cdot \theta(\text{HF}_2^-) + k_3 \cdot \theta(\text{HF})\} + k_4 \cdot \theta(\text{H}^+)$
 θ : degree of coverage of active adsorption sites
in practice a few μm/min for 50 wt % HF at 25 °C



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The ammonium fluoride contributes with fluorine ions, which has an impact on this reaction constant, but, as this reaction constant still has to be the same, this means that this increased concentration here gives a

decreased concentration of protons so, hence, less etching. So, the etching rate goes down by addition of the ammonium fluoride. A mix of 40 weight percent ammonium fluoride, with 49 weight percent HF, in these ratios, is called buffered oxide etch, BOE, or what we have called, in the beginning, buffered HF, BHF. 49 weight percent of HF is also called pure HF, as HF is, intrinsically, a gas which is dissolved in water, and this is the maximum dissolvable weight percent concentration. The use of buffered HF produces a slower and less aggressive etch so that photoresist masks can be used, as we have seen for the micro-activator. Photoresist would be very strongly degraded in pure HF baths. The exact glass composition also has an influence on the etch rate. A glass can contain multiple other oxides apart from silicon dioxide. It can contain so-called network-forming oxides, which are compounds that induce additional molecular bonds which need to be broken, resulting in slower etching. Boron oxide is an example of such network-forming oxides. A glass can also contain network modifying oxides, such as sodium oxide, and when these are introduced in the silica network, they generate so-called non-bridging oxygen sites, resulting in faster etching. So, here, we see, by adding the sodium oxide to the network, splits somewhere the network, as the bond is fulfilled by the sodium ion.

- Addition of NH_4F shifts reaction equilibria

$$K_1 = [\text{H}^+][\text{F}^-]/[\text{HF}] = 6.7 \times 10^{-4} \text{ mol/l}$$

$$K_2 = [\text{HF}][\text{F}^-]/[\text{HF}_2^-] = 0.26 \text{ mol/l}$$

results in increase in HF_2^- concentration and pH

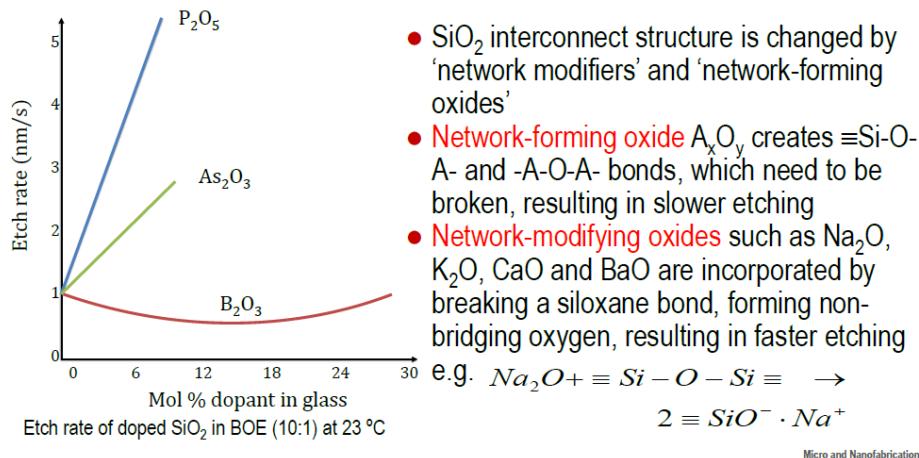
- Mix of 40 wt% NH_4F with 49 wt% HF (in ratios from 6:1 to 10:1) is called **buffered oxide etch (BOE) or buffered HF (BHF)**
- Less aggressive etch, so photoresist masks can be used

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The effect of network-forming oxides and network-modifying oxides is illustrated in the curves obtained in buffered oxide etch for silica doped with the network-forming boron oxide, and these two network modifying oxides. So, here, when there is more dopant, these etch rates go up, and this goes down, at least initially. Here, we introduce a pure HF-based microfabrication process for Pyrex wafer. A mask that resists

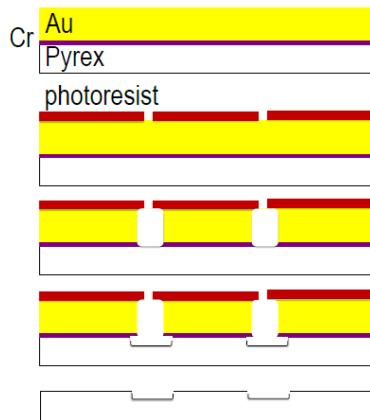
to this aggressive bath is gold, which, for good adhesion, needs to be deposited on a very thin chromium layer. On top of this gold layer, one deposits a photoresist, which is prebaked, developed, postbaked, after which an oxygen plasma descum step is performed to clear the liberated gold surfaces from organic molecules. Now follows a gold-etching step in a potassium iodide-iodine solution, followed by a chromium etch to remove the very thin chromium adhesion layer. Next follows the etching in pure HF.



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That means the 49% HF in water solution. Etching rates of five to ten micrometers per minute are obtained. At the end, the photoresist is removed, and the gold is etched away, as well as the chromium, leaving behind the microstructure etched in the Pyrex wafer.

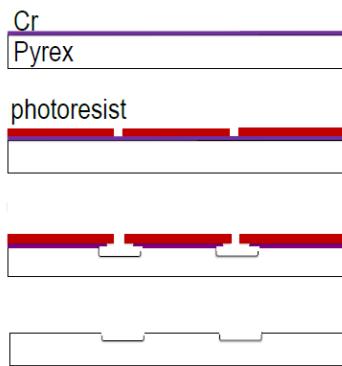


- Pyrex Corning 7740, 525 μm, Cr 60 nm, Au 200 nm
- Spin coat with positive photoresist, prebake, development, postbake, O₂ plasma descum
- Au-etching with KI + I₂ solution, Cr-etch
- Bake, Pyrex etching with 49 % HF; etch rate 5-10 μm/min
- Stripping of resist with remover, Au etch with KI+I₂, Cr-etch

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Now we present a Pyrex-etching process, in buffered HF, that does not require the microfabrication of the expensive gold mask, as photoresist can be maintained in the buffered HF bath. The process starts by sputtering a very thin chromium layer onto the Pyrex to which there is a good adhesion by the photoresist. Then we spin coat the photoresist layer in which the mask structure is patterned via the usual procedure. Next, we have to do the chromium etch, and then the Pyrex etch using the BHF solution.

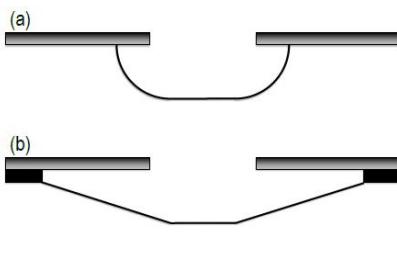


- Pyrex Corning 7740, 525 µm, Cr 60 nm
- Spin coat with positive photoresist, prebake, development, postbake, O₂ plasma, descum, Cr-etch
- Cr-etch, Pyrex etching with **BHF [1:7 49 % HF : NH₄F]**; etch rate 5 µm/hour
- Strong mask underetching

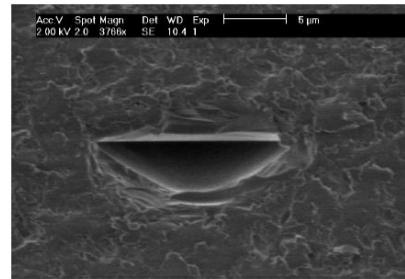
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The etch rate is now five micrometers per hour, much slower than with a pure HF bath. However, we do not need to use a gold mask now. Note that, like in the pure HF case, there is mask underetching in this process, because it's a pure chemical process. The process ends by removal of the photoresist and chromium adhesion layers. Here, we show typical profiles that result from an HF or BHF etching process. The profile in a) is the normal one, but, sometimes, one obtains a profile like shown here; much more widened with respect to the original hole dimension in the mask.



(a) Good adhesion of masking material
(b) Etchant penetration between mask and Pyrex



Pyrex-etched profile with second bonded Pyrex wafer to form microchannel

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This is an indication that there was not a good adhesion of this mask to the glass, and that the etching liquid could infiltrate in between the glass wafer and the mask, so that there is continuous etching underneath the mask. The picture on the right shows an etched channel in Pyrex, and, here, this was patterned on top of the wafer, which was then bonded, at high temperature, with another Pyrex wafer to make a closed channel. In this lesson, we have explained the mechanism of HF etching of glass wafers. We demonstrated the effect of adding ammonium fluoride to the bath, which produced a buffered oxide etch, or BHF bath. Then we explained the effect of glass composition on the etch rate by incorporating either network-forming oxides or network-modifying oxides in the silica network. Finally, we showed cleanroom processes for Pyrex microfabrication using both HF and BHF baths.

Summary

- Mechanism of HF etching of glass
- Effect of adding NH_4F
- Effect of glass composition
- Cleanroom processes for HF and BHF etchants

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Practice quiz HF bath for SiO₂ and glass wet etching

Questions:

1. What is the main advantage of a buffered HF (BHF) over a pure HF bath for the Pyrex etching process?

- A Au layer is not required in preparing the mask
- One can completely avoid mask underetching effects
- The etching rate is significantly enhanced, yielding a higher throughput
- The Cr layer is not required for depositing the photoresist mask on the Pyrex substrate

2. What is a commonly used application of HF etching?

- To make the wafer surface more hydrophilic
- To remove the residual organics from the wafer surface
- To thermally stabilize the structures on the wafer
- To form free standing structures

Isotropic wet etching of silicon in the HNA bath



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Now we will discuss a chemical etching bath for the isotropic etching of silicon, which is a so-called HNA bath consisting of nitric acid, HF, and acetic acid.

- Hydrofluoric acid + nitric acid + acetic acid bath ('HNA' bath)
 $HF + HNO_3 + CH_3COOH (A)$
for Si etching
- HF bath for electrochemical etching
and for creating porous Si

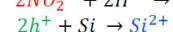
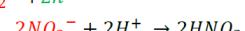
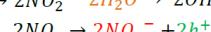
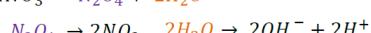
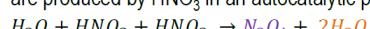
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Then we present the HF bath for electrochemical etching of silicon, and for creation of porous silicon. The HNA bath has three components, two of which are active in the etching, namely, the nitric acid and the HF. The acetic acid is a diluent for reducing and for better controlling the etching rate. That is why we only see these two components in the reaction. The silicon is etched from the substrate, and transported into the solution in the form of this molecule, which is called fluorosilicic acid, while the HNO₃ and HF are consumed. Now we will detail what happens during etching.

- Overall reaction



- In acidic media, the Si etching process first involves **hole injection into the Si valence band** by an oxidant. In the absence of photons or applied field, holes are produced by HNO₃ in an autocatalytic process



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In acidic media, like nitric acid, the silicon etching process first involves hole injection into the silicon valence band by the oxidant, in this case, the HNO₃, which is meaning the same as removing an electron

out of the valence band of silicon. In the absence of light, or an electric field, holes are produced by nitric acid in an autocatalytic process. HNO_3 , when it is dissolved in water, partially splits up in HNO_2 , and it is this HNO_2 that reacts with HNO_3 to form this compound, N_2O_4 , or dinitrogen tetroxide, and water. The dinitrogen tetroxide decomposes in 2NO_2 , or nitrogen dioxide molecules, while the water splits up in two hydroxyl ions and two protons. The nitrogen dioxide is the active molecule that generates the holes, denoted as h^+ , as well as NO_2^- , or so-called nitrite ions. The nitrite ions recombine with protons to form HNO_2 molecules, while the holes charge the silicon. We see here that a nitrous acid, the HNO_2 , is regenerated because, in the beginning, we spoke of an autocatalytic process.

- Si^{2+} combines with OH^-

$$\text{Si}^{2+} + 2\text{OH}^- \rightarrow \text{Si}(\text{OH})_2$$
- Generation of SiO_2 with release of H_2O
Overall oxidation reaction

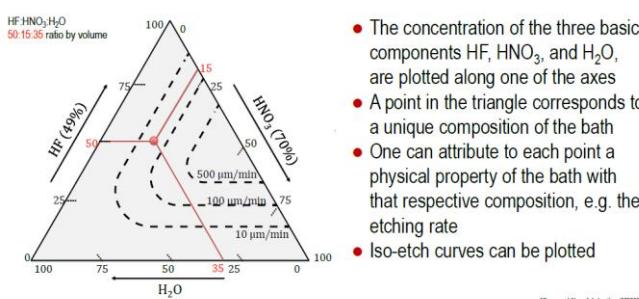
$$\text{Si} + 2\text{HNO}_3 \rightarrow 2\text{HNO}_2 + \text{SiO}_2$$
- Next follows the dissolution of the oxide by HF

$$\text{SiO}_2 + 6\text{HF} \rightarrow \text{H}_2\text{SiF}_6 + 2\text{H}_2\text{O}$$
- Acetic acid (CH_3COOH) is a diluting agent (also water can be used)

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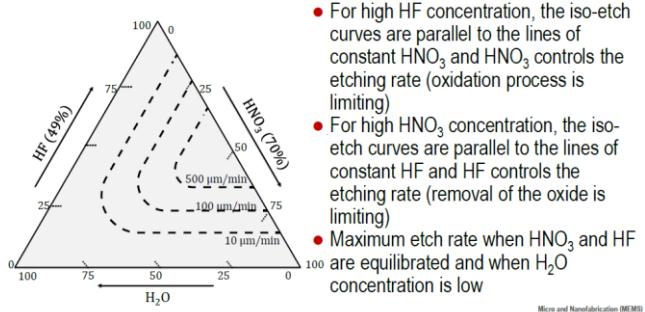
HNO_2 is not consumed, but the HNO_3 , in a way, is consumed, as, on the other side, we have 2HNO_2 molecules. Now we have a double positive charge on the silicon, and this combines with two hydroxyl ions to form this $\text{Si}(\text{OH})_2$ group, and these groups on the surface, they recombine to generate silicon dioxide and the release of water. The overall reaction until now is the transformation of silicon in silicon dioxide, under the reduction of nitric acid into nitrous acid. Now the HF comes into play. We have seen, in the previous lesson, how HF reacts with the silicon dioxide, forming the molecule, fluorosilicic acid, and water. As said before, the acetic acid is not entering in these chemical reactions because it's a diluent. Also, water can be used in the bath as a diluent, by the way. A ternary diagram like this allows to plot the three chemical components of the bath on a two-dimensional sheet of paper.



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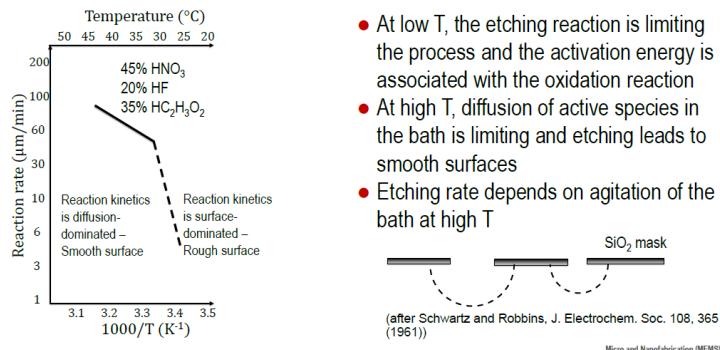
So, this is an axis where we plot the HF concentration from 0 to 100%. This is an axis where we plot the nitric acid concentration from 0 to 100%, and on this axis, we plot the diluent, in this case water, from 0 to 100%. Each point of the triangle corresponds to a unique composition of the bath. For example, this red point corresponds to a mixture with 50% pure HF, 15% of HNO_3 , and 35% of water, and you see, together, this forms 100. This red line says that, all along this line, if I continue just like that, there is, everywhere, 50% of HF, and, when moving on the line, one interchanges HNO_3 with water. So, the more we go in this direction, more will there be HNO_3 and less water. Now we can measure the etching rate for each bath composition, and then plot the ensemble of points where the etching rate is the same.



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This is a so-called iso-etch curve . For example, this dashed line corresponds to all compositions of the bath, where the etch rate is 500 micrometers per minute. On this line, it is 100 micrometers per minute. We see that the highest etching rates are obtained in a zone of the diagram where one has about the same quantities of HNO₃ and HF, because both are needed, and where there's only a small concentration of water, which is logical. For high HF concentration, that's in this region, the iso-etch curves are parallel to the lines of constant HNO₃, and this means that it's the HNO₃ concentration that controls the etching rate. In fact, there is enough HF, and the little number of HNO₃ molecules limit the etching rate. And, in the same way, for high HNO₃ concentration, the iso-etch curves are parallel to the lines of constant HF concentration, and this means that HF controls the etching rate, as there are relatively few HF molecules, and the removal of the oxide represents the limiting step. Here, we present the temperature dependence of the etching rate for a bath of particular composition, namely that having 45% of nitric acid, 20% of HF, and 35% of acetic acid.



(after Schwartz and Robbins, J. Electrochem. Soc. 108, 365

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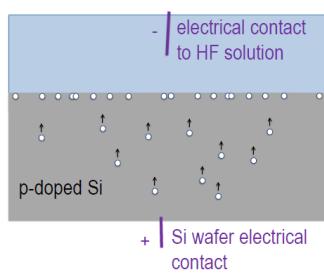
The x-axis is linear in one over the temperature, while, on the top, we have plotted the temperature corresponding to this linear axis. At low temperature, that means at a high one over T value, the etching reaction is limiting the process, and the activation energy, that is the slope of this curve, is associated with the oxidation reaction which is the slowest. After etching, the surface shows some roughness. At high temperature, that means at low one over T, diffusion of the active species in the bath is limiting the etching reaction, and the etching results in smooth surfaces.

- Etch rates for
 - Si : 50 μm/min (66% HNO₃, 34% HF)
 - SiO₂ : 30-80 nm/min
- SiO₂ can be used as mask material
- For very deep etching, Au or Si₃N₄ masks are required
- Photoresists do not withstand strong oxidising agents like HNO₃
- Problems with isotropic etchants
 - Etch rate is agitation-dependent
 - Isotropic etching = charge transfer process, hence there is etch rate dependence on dopant type and concentration. N- or p-type regions with dopant concentration of 10^{-17} cm^3 or smaller etch 15 times slower than for high dopant concentrations → technique is used for wafer defect analysis

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At high temperature, this etching rate depends now on the agitation of the bath, as, by agitation, transport of molecules is better than by diffusion only. Also, when diffusion is limiting the reaction, when one has a wider opening in the mask, this results in deeper etching, as the access for the reactive molecules is facilitated. What are the mask materials that one can use in an HNA etching process? If one is at a temperature where the silicon etching rate is 50 micrometers per minute, the silicon dioxide etching time is in between 30 and 80 nanometers per minute, much slower, so that silicon dioxide can be used as a mask when etching silicon. For very deep etching, one needs gold or silicon nitrite masks. One cannot use photoresists as they do not withstand long to a strong oxidizing agent like nitric acid. There are some issues with isotropic etchants, like the etch rate that is agitation dependent and depends on the local condition of the bath. We explained, during the discussion of the isotropic etching mechanism, that there is a hole transfer process to the silicon, hence, there is an etch rate dependence on the dopant type and concentration of the dopant in the silicon, so it makes a difference whether one has n- or p-type regions doped in the silicon, or if they have different dopant concentrations.

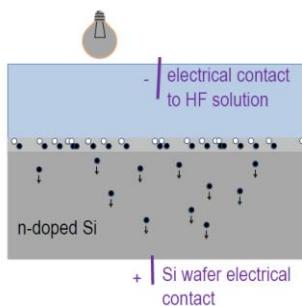


- A high temperature aggressive chemical etching process can be replaced by an electrochemical procedure utilising a milder solution, thus allowing a simple photoresist mask to be employed
- Oxidation can be promoted by a **positive voltage bias applied to the p-Si** causing an accumulation of holes h^+ in the Si at the Si/electrolyte surface
- No need for HNO_3 , 5% HF solution can be used for etching

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However, this characteristic can be used to reveal the number of defects on the surface of a silicon wafer, for example. One etches the surface, and defects can be etched faster, and can then be directly seen on the surface. We explained that etching of silicon in an acidic solution involves the transfer of a hole from the nitric acid to the silicon. It is possible to replace this chemical injection of a hole by an electrochemical procedure, utilizing a milder solution, so that a photoresist mask can be used.



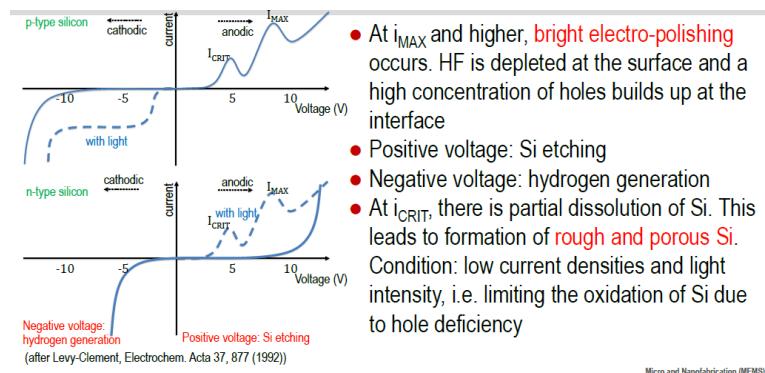
- Applying a **positive voltage bias to the n-Si** causes a depletion of electrons e^- in the Si at the Si/electrolyte surface
- Applying light generates $e^- - h^+$ pairs in the depletion region
- Electrons e^- are transported to the positive voltage
- Holes h^+ at the surface promote oxidation
- Etching occurs

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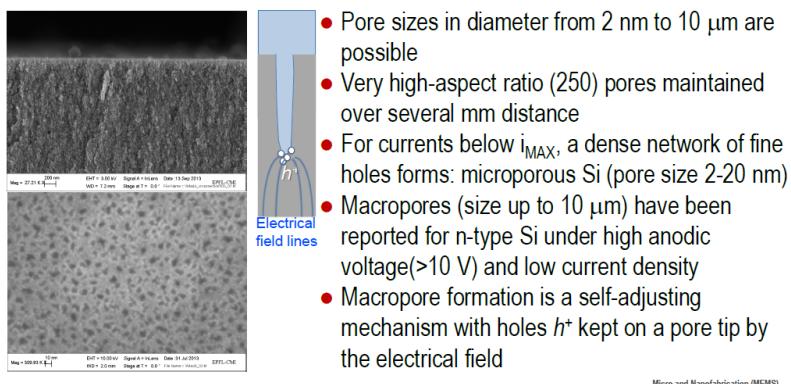
Suppose one has a p-doped silicon wafer, and that one attaches a conducting wire where one puts a positive voltage bias. By this, holes will be transported in the silicon, and accumulate at the silicon electrolyte interface. We have seen that these holes are essential for oxidation, so the oxide forms, and this can now be removed by just having an HF solution, so there is no longer nitric acid, but there will be etching because there was oxidation at the surface. Now we change to silicon with n-doping, and we attach, again, a wire to the back of the substrate, and apply the positive voltage. What will happen now is that the electrons, that are the mobile carriers, will be attracted towards the positive voltage and we will get, here, an electron depletion zone at the contact with the solution. No etching will occur in a diluted HF solution as no holes are present at the surface, except if this positive voltage would be so high that there is an electrical breakdown

by which holes can be transported to the surface. We are now again in the case with n-type doping, and we have applied here a moderate positive voltage. If we now add to the setup a light source, we create photons that generate electron hole pairs, and the electrons go towards the positive voltage, while the holes remain here. Now there can be oxidation, and, subsequently, the HF etches away the oxide. We are now looking at the current voltage characteristics of p-doped silicon, which is put into the dilute HF solution.



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When we apply a positive voltage, we transport holes to the interface, due to which there is oxidation, and etching occurs. More voltage means more holes, means more etching, and it follows this particular behavior. If we apply a negative voltage, this attracts the holes to the wire, leaving a depletion of holes at the interface. No reaction is occurring, hence, no current is flowing, except if the voltage is so high that one has electrical breakdown. If one now shines light, the photons generate electron hole pairs, the electrons of which stay at the interface, and these electrons recombine with protons from the electrolyte, thereby generating hydrogen gas. So, under negative voltage bias, there is a current that is generated by the generation of hydrogen and not by etching. If you look back again at the positive part of the curve, we know that, for high currents, the surface that was etched appeared bright. Due to the high number of holes, electro-polishing results. If one is at lower current, the number of oxidation events is reduced and one gets only locally oxidation and etching, resulting in a rougher surface. If we now take an n-type doped silicon wafer, and bring it in the diluted HF solution, and we apply a negative voltage, electrons will be transported to the silicon electrolyte interface, in a straightforward way, to generate hydrogen gas. If we apply a positive voltage we will have the depletion layer effect, which we have introduced before, so there will be no current except if there is voltage breakdown. Shining a light to the wafer creates holes at the interface leading to oxidation and this positive current, represented by the dashed line.



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A condition for realization of porous silicon is to have a low current and low light intensity in order not to have too many holes at the electrolyte silicon interface. The top picture shows a cross-section of an n-type wafer, the surface of which was transformed into porous silicon. The lower picture shows a view from the top of the wafer. Pores can be created with diameters ranging from a few nanometers to 10 micrometers.

The bigger pores are obtained by applying a high positive voltage, resulting in electrical breakdown of the n-doped silicon. The smallest pores are realized at low voltages and by tuning the intensity of the light source. Pores can be very narrow and very deep, with an aspect ratio of up to 250: they can be 250 times deeper than wide. These very long and narrow pores originate from the fact that the electrical field lines are focused towards the bottom of a pore, where the holes accumulate, resulting in oxidation only there, and continuing etching in the vertical direction. If one has too many holes, the holes will be everywhere, and one will not have porous silicon. If there are just enough holes, only etching will occur at the bottom of the hole, and the pore becomes deeper and deeper. This ends our lesson on the isotropic wet etching of silicon. We have first explained the chemistry involved in isotropic wet etching in a so-called HNA bath, pointing out the importance of having holes originating from the nitric acid at the silicon surface to induce oxidation, after which the HF removes the oxide. Then we have explained the electrochemical etching in an HF bath. If you apply a positive voltage to the wafer, holes can be transported to the surface, and the nitric acid can be avoided. We then explained how porous n-type silicon can be made by electrochemical etching in an HF bath by applying moderate current and light intensities so that the number of holes at the surface is limited, and they accumulate only at the bottom of the pores.

Summary

- Chemistry of isotropic wet etching in a HNA bath
- Electrochemical etching in a HF bath
- Realisation of porous Si by electrochemical etching in a HF bath

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Practice quiz isotropic wet etching of silicon in the HNA bath

Questions:

1. Which of the following is true for the mask material selection for the etching of Si in an HNA bath?
 - Wet etching of SiO_2 is performed by adding an electrical contact to the Si wafer
 - For very deep etching, a Au or Si_3N_4 mask is needed
 - Photoresists can be used as masking material, as they tolerate strong oxidizing agents like HNO_3
 - One has to dip the wafer first in a pure HF bath, after which one dips it in a HNO_3 bath
2. Which of the following is true for the current-voltage characteristic of a p-doped Si wafer that is put into a diluted HF solution, whereby one electrode is attached to the p-doped Si and the other electrode is placed in the diluted HF solution?
 - At large negative voltage values, electrical breakdown of the semiconductor occurs
 - A positive voltage applied to the wafer transfers electrons to the interface and hence Si etching occurs
 - Because of electro-polishing during positive voltage values, p-doped Si looks dark
 - A negative voltage applied to the wafer causes the accumulation of electrons in the liquid at the wafer-HF bath interface

Anisotropic wet etching of silicon in alkaline baths

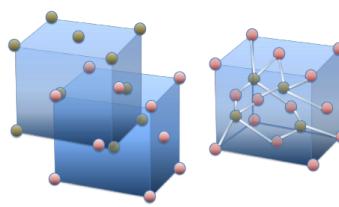


In this lesson, we will explain the anisotropic etching of silicon by which certain crystal planes will be chemically attacked by an etchant, while other planes will not react.

- Si crystal structure
- Etching mechanism
- Etching baths

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These etching phenomena are observable because the silicon wafer is essentially single crystalline, that is, it has an ordered lattice structure on the scale of the wafer. We will explain the etching mechanism and some of the etching baths that can be used. These drawings illustrate the silicon crystal structure which is that of a diamond lattice and can be represented by two interpenetrating face-centered cubic lattices.



- Si has the crystal structure of the diamond lattice and can be represented by two interpenetrating face-centred cubic lattices
- A Si atom forms four covalent bonds which are part of tetrahedrons
- Packing density and bonding strength of atoms in different plane orientations is different
- This can give rise to plane-dependent etching rates

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A silicon atom forms four covalent bond with other silicon atoms. If one cuts the silicon crystal along different planes, one will see that the packing density of atoms and the bonding strength between silicon atoms on different plane orientations is different. And this gives rise to etching rates that can depend on the

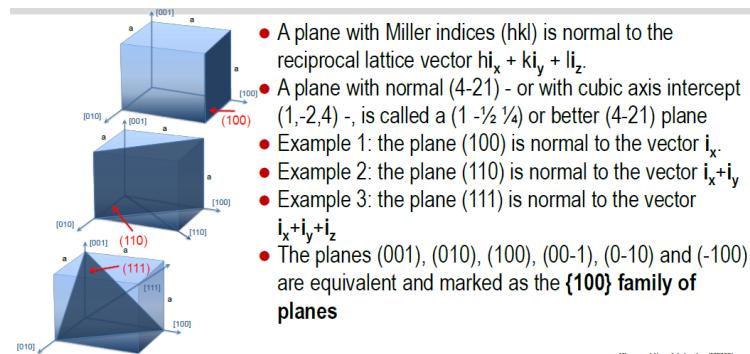
plane orientation. A cubic crystal unit cell has three basis vectors and every point in real space can be written as the coordinate of a vector written in function of the three basis vectors. A real space coordinate or vector can be represented by three numbers as put in between the square brackets.

- Cubic crystal unit cell has three basis vectors with magnitude $\mathbf{a}_x = a\mathbf{e}_x$, $\mathbf{a}_y = a\mathbf{e}_y$, and $\mathbf{a}_z = a\mathbf{e}_z$ ($a=5.43 \text{ \AA}$ for Si)
- **Directions in real space**
Example: vector $\mathbf{r} = 2\mathbf{e}_x + 4\mathbf{e}_y + 0\mathbf{e}_z$ is characterised by direction [120] (or [240])
Directions [100], [010] and [001] are crystallographically equivalent: they form the group of <100> directions
- **Crystal planes** are characterised by sets of three Miller indices. They describe vectors in the reciprocal lattice, normal to the crystal planes in question, and are the inverse of the intercept of the plane at the axis in real space

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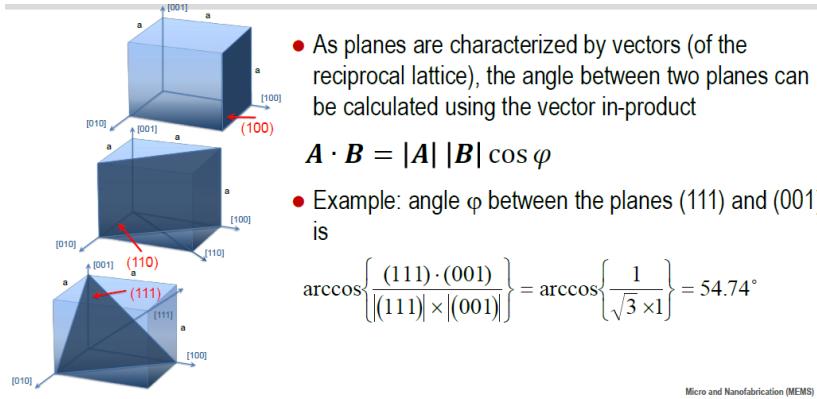
So this direction is the same as this direction, only the vector here is shorter by a factor of two. In the crystal, the directions [100], [010] and [001] are crystallographically equivalent. One is along a different axis but for the environment of the silicon atom, there is no difference. If one wants to speak of all these directions, together, one puts 1 0 0 with these triangular brackets: {100}. In micro-fabrication, we are not so much interested in knowing the real space coordinate of each atom, but rather, we would like to know how the crystal planes are oriented in the wafer. A crystal plane can be characterized by three so-called Miller indices which describe a vector in the so-called reciprocal space that is normal to the crystal plane.



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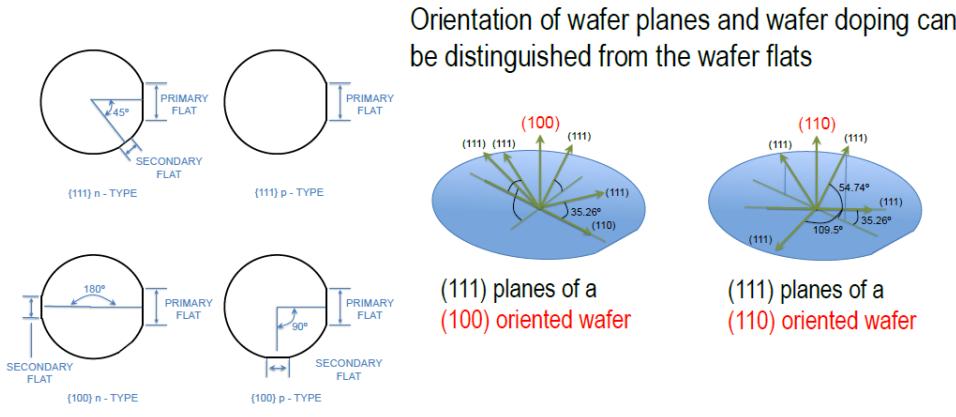
The Miller indices are defined by taking the inverse of the intercept of the plane at each axis in real space, and we illustrate that now in the following. A plane with Miller indices (hkl) , and we use here now rounded brackets because it's a plane, is normal to this reciprocal lattice vector where these are the basis vectors of the reciprocal lattice, these three. A plane with a normal $(4-21)$, means that the plane intercepts the three cubic axes at 1, -2 and 4. Indeed, if we invert 1, -2 and 4, we obtain this reciprocal lattice vector and as one likes better whole numbers, one multiplies this vector by 4 to get this vector. By this operation, the orientation of the vector does not change, so it's the same plane. As we already pointed out, a reciprocal space vector is denoted by the rounded brackets. The upper drawing illustrates the position of a (100) plane which intersects the x -axis at 1, and the y and z -axis at infinity. So if we invert these, we get (100) . The planes (001) , (010) , (100) , and so on are equivalent, and if you want to speak of all of them together, we write it with these brackets: $\{100\}$. So this means this is the family of identical planes. In the same way, the drawing in the middle indicates the (110) plane. And the drawing below, the (111) plane.



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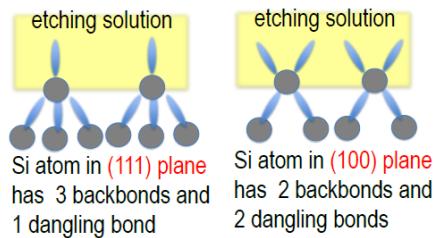
So this intersects, for example, each axis at one. As planes are characterized by vectors of the reciprocal lattice, one can simply calculate the angle between two planes by calculating the vector inner product; this product. And as an example, the angle phi between the planes (111) and (001), is 54.74 degrees. If one has in mind a cubic crystal structure, one can know the orientation of the different planes. For example, if the surface of the wafer has a (100) orientation, there are four (111) planes that have each an angle of 54.74 degrees with the plane of the wafer. If the wafer has been cut from a crystal that had a (110) orientation, two (111) directions are now pointing outside of the wafer and two (111) directions are inside. That means in this case, the (111) plane is vertical. There are two vertical (111) planes for a (110) oriented wafer. In practice, wafers have so-called flats : a primary flat and a secondary flat. Here, there's only a primary flat. If you see a wafer, in principle you know by looking at the flats what is the type of orientation of the wafer.



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So here is the orientation and here is the (100) orientation, and also you know the type of doping in the wafer by looking at the flats. The reason why an etching bath preferentially attacks a certain lattice plane, and does not etch another plane is illustrated here.

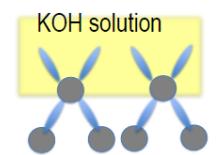


- A Si atom located in a certain plane is differently ‘anchored’ to the back of the substrate and has a different number of dangling bonds that are in contact with the etching solution
- This can give rise to plane-dependent etching rates
- Example: a (111) plane will etch much slower than a (100) plane in an alkaline etching bath

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A silicon atom that is present in a (111) plane has three backbonds to the interior of the silicon wafer and one dangling bond which is interfacing with the etching solution. So this bond can be attacked by chemical molecules from the etching solution. A silicon atom within a (100) plane has only two backbonds and two dangling bonds pointing in the etching solution. The second type of silicon atom is hence less well anchored to the silicon wafer and will be more easily etched away. An example of such an etching bath is potassium hydroxide or KOH solution.



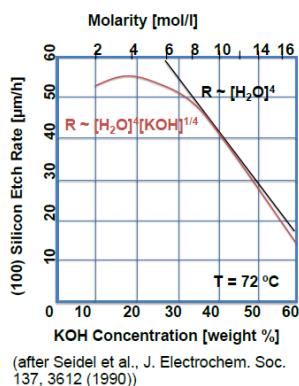
Si atom in (100) plane
has 2 backbonds and 2 dangling bonds

- Four hydroxyl groups bind to a Si atom and the molecule $Si(OH)_4$ moves into the solution
- $$Si + 2OH^- \rightarrow Si(OH)_2 + 2e^- (\text{solid})$$
- $$Si(OH)_2 \rightarrow Si(OH)_2^{2+} + 2e^- (\text{solid})$$
- $$Si(OH)_2^{2+} + 2OH^- \rightarrow Si(OH)_4$$
- In the solution $Si(OH)_4 \rightarrow SiO_2(OH)_2^{2-} + 2H^+$
 - Four electrons are injected into the valence band of Si and stay at the surface
 - These electrons ‘reduce’ H_2O and form OH^- ions and H_2
- $$4H_2O + 4e^- \rightarrow 4H_2O^- \rightarrow 4OH^- + 2H_2$$

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In such a bath, 4 hydroxyl ions bind progressively to a silicon atom in a two-step process leading to the formation of this molecule. This molecule is called silicic acid. It is converted in the solution to this molecule and into two protons. The four electrons that came from the four hydroxyl ions have been injected in the silicon. These four electrons, they are used here to generate four new hydroxyl ions so that there is no charging of the silicon and the etching continues. The four hydroxyl ions that are generated at the silicon surface originate from water molecules and not from hydroxyl ions initially present in the KOH solution.

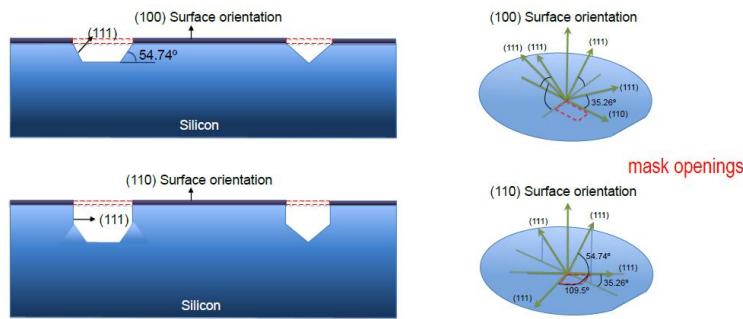


- The OH⁻ ions generated at the Si surface react in the oxidation step, while the OH⁻ concentration in the bulk solution does not play a major role
 - Reaction rate
- $$R = k[H_2O]^4 [KOH]^{1/4}$$
- Four water molecules are needed in the reaction explaining the power 4 for [H₂O]
 - OH⁻ ions are generated by water explaining the small power 1/4 for [KOH]
 - Etch rate in anisotropic etching is reaction rate-controlled and thus temperature-dependent

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The reaction rate of the KOH etching bath can be written as this formula and between brackets, you have the molar concentrations. So this is the molar concentration of water, if there is more water, the concentration of water is higher. The power of four gives the water concentration the most prominent importance, while the KOH has only a power of 1/4. The red curve shows the actual etching rate as a function of the KOH concentration. And we indeed see if there is more KOH dissolved in the water, the etching rate goes down. The black curve gives the power of four dependence on the water molar concentration. Note that this etching rate was for atoms on a (100) plane while to first order, there is no or very, very little etching of atoms on a (111) plane. We draw here again our wafer with (100) surface orientation and cover it completely with the masking layer, except for a rectangular opening that is oriented along the (110) direction. The diagram on the left side shows the same wafer in cross section with two of these rectangular openings also indicated by the dashed lines. Atoms along the (100) plane will be etched away. So etching will go vertical and if one encounters a (111) plane like here or here, there will be no etching. So gradually, the (111) planes will become visible.

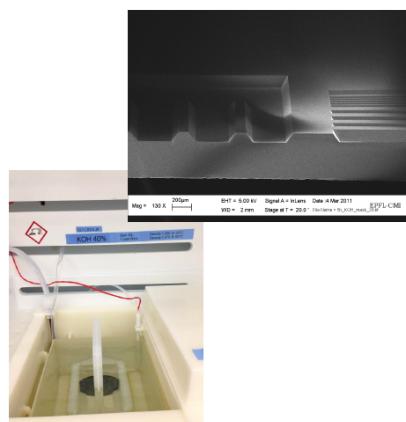


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The hole here has reached the final V shape and no further etching will happen. In a similar way, we can draw again our wafer with (110) surface orientation, cover it completely with a mask material and make now an opening in the mask, given by this dashed line again. So this opening is parallel to the (111) directions. If we look to the cross section of the wafer after etching, we see following profiles with the structure on the right representing a hole in its final state where only (111) planes are in contact with the KOH solution, and this (111) plane indeed is vertical. Anisotropic etching is possible in different alkaline aqueous solutions but the most popular solution is the KOH bath. It is typically composed of 20 weight percent of KOH, 16 weight percent of propanol and 64 weight percent of water. The bath is typically operated under agitation at 80 degrees Celsius. These are the etching anisotropies for different silicon planes. Here we see that the (100) plane etches 400 times faster than the (111) plane. So the (111) plane etching rate is not completely zero. The etching rate of a (110) plane is 600 times higher than that of a (111) plane. The picture shows the result

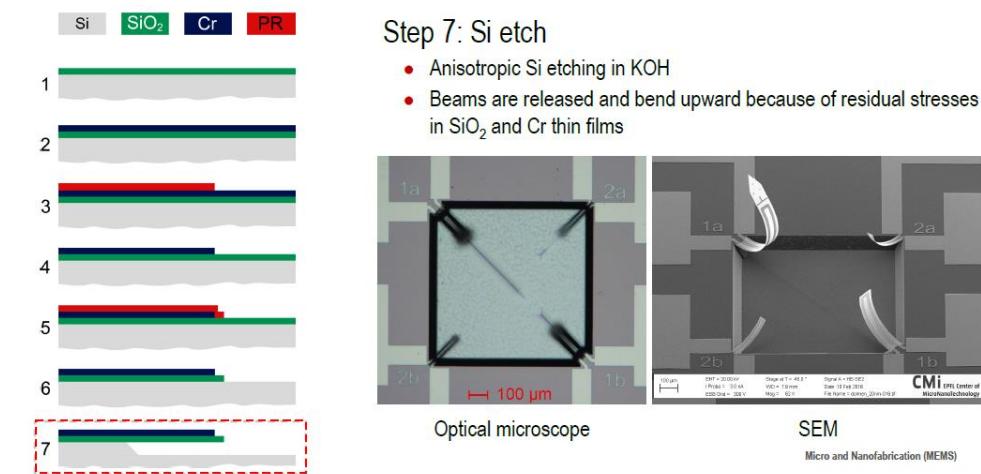
after a KOH etching process and one recognizes typically these V-shaped channels and holes. And this is the KOH etching bath. This Section shows the etching of a silicon wafer in a KOH solution. Initially, the wafer is in a beaker of deionized water and then transferred to the KOH solution. One observes the formation of hydrogen gas during etching. In principle, the etching can go on for hours if deep structures need to be etched. KOH etching was used also in the final step of our case study of the thermo-mechanical actuator. It was the process step that released the cantilever beam from the wafer by anisotropic underetching of the silicon. While there are several options that can be used to underetch, such as dry plasma etching, and isotropic silicon etching, anisotropic etching of silicon was used here due to its simplicity and efficiency for this type of structure. The inclined side walls of the etched hole immediately make it clear that we used an anisotropic etching process. Also so-called alkaline organic baths are used for anisotropic silicon etching. A well known example is the ethylenediamine bath



- Anisotropic etching possible in alkaline aqueous solutions like KOH, NaOH, LiOH, CsOH, NH₄OH
- Aqueous KOH is most 'popular' etchant, a typical bath is composed of 20 wt% KOH, 16 wt% propanol and 64 wt% water. The bath is operated under agitation at 80 °C
- The etching anisotropy ratio for different Si planes is (111):(110):(100) ≈ 1:600:400
- The bath is relatively safe and non-toxic

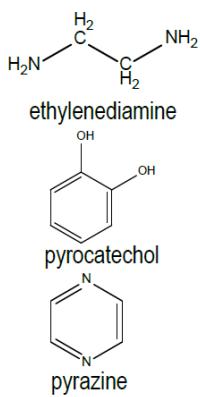
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with addition of pyrocatechol molecules, so-called EDP bath.

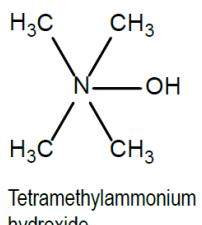


- Alkaline organics also result in anisotropic etching.
Examples: ethylenediamine pyrocatechol (water) (EDP) and tetra-methyl ammonium hydroxide (TMAH)
- A typical EDP bath is composed of 75 wt% ED, 13.5 wt% of the chelating compound pyrocatechol, 0.5 wt% of the ‘smoothener’ pyrazine and 11 wt% water. The bath is operated at 70-100 °C
- Ionization of ED produces OH^- ions
 $\text{NH}_2(\text{CH}_2)_2\text{NH}_2 + \text{H}_2\text{O} \rightarrow \text{NH}_2(\text{CH}_2)_2\text{NH}_3^+ + \text{OH}^-$
- The etching anisotropy ratio for different Si planes is
 $(111):(110):(100) \approx 8:50:200$

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It is composed typically of 75 percent of ethylenediamine, 13.58 percent of pyrocatechol, a half percent of pyrazine, and 11 percent of water. Ionization of the ethylenediamine produces this ion and the hydroxyl ion. That is why it becomes an alkaline bath. Pyrocatechol is a chelating molecule. Two of such molecules with these fingers can grab a silicon atom and transport it into solution. We also present here, the etching anisotropy rates for different silicon planes using this bath. So the ratio of the etching rate for example, of a (111) plane and a (100) plane is 8:200.



- A typical TMAH bath is composed of 38 wt% TMAH (25% solution in water), 4 wt% of Si powder and 58 wt% water. The bath is operated at 90 °C
- The Si serves for seasoning the bath and provides protective compounds for Al contacts during etching, for example
- The bath can be used in transistor fabrication, as it does not contain alkali metals like Na and K
- The etching anisotropy ratio for different Si planes is
 $(111):(100) \approx 1:10$

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A third popular bath is the tetramethylammonium hydroxide bath or TMAH bath which produces good results by adding a few weight percent of silicon powder in the bath during etching. This is a so-called seasoning of the bath and it results in better aluminium contacts that are preserved during the etching.

The etching anisotropy is lower than for the two other baths. In this lesson, we have discussed the anisotropic etching of silicon. We gave a reminder of real and reciprocal space vectors whereby a reciprocal space vector is characterizing a crystal plane. We explained the anisotropic etching mechanism which is due to a difference in bond strength for a silicon atom on a different plane. We found that a (111) plane etches very slowly. Finally, we discussed different alkaline etching baths like KOH, EDP and TMAH.

Summary

- Real and reciprocal space
- Anisotropic etching mechanism
 - Different bond strength for a Si atom in a different plane
 - (111) plane etches very slow
- Different alkaline etching baths
 - KOH
 - EDP
 - TMAH

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Practice quiz anisotropic wet etching of silicon in alkaline baths

Questions:

1. Which one is an adequate bath for anisotropic Si wet etching?

- A pure HF bath
- An alkaline organic bath like EDP
- A low concentration H_2SO_4 bath
- A KOH bath with over 95% of KOH concentration in water

2. Assuming that a Si wafer is immersed in a wet anisotropic etchant, which of the following is correct regarding the Si anisotropic etching process?

- A Si atom in a (111) plane has 2 backbonds and 2 dangling bonds
- A Si atom in a (100) plane has 3 backbonds and 1 dangling bond
- The etch rate for Si atoms in (100) and (111) planes are temperature-independent
- A Si atom in a (100) plane has a higher etching rate than a Si atom in a (111) plane

Etch stop techniques for thin membrane microfabrication and bulk micromachining

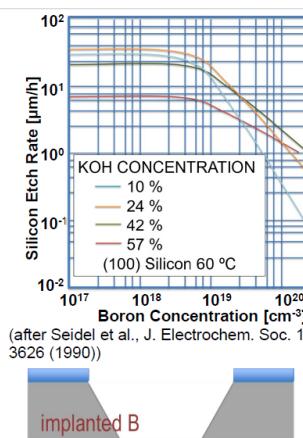


In this lesson we will explain two techniques for stopping the etching in a very controlled way, allowing the microfabrication of very thin membranes.

- Etch stop techniques for thin membrane microfabrication
- Bulk micromachining

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Then we will illustrate the potential of this technique for bulk micromachining, which is microfabrication by etching through bulk parts of a wafer. In our introductory lesson on wet etching we already mentioned that one can make a very thin silicon membrane by implanting it with boron. And if one etches, then, in KOH solution, the etching stops when one reaches this boron-doped membrane. We can now understand this. The figure shows the silicon etching rate as a function of the boron concentration for different KOH concentrations in the etching bath. For boron concentrations above 10^{19} atoms/cm³, the etch rate drops, and note that this is a logarithmic scale.



- For KOH-based solutions, significant reduction in etch rate for B concentrations in Si above 10^{19} cm⁻³
- At high B concentration, the Si Fermi level drops and the electrons tunnel into the valence band, where they recombine with holes, rather than staying at the Si surface for regeneration of new OH⁻ ions
- Hence the etching stops
- Other anisotropic etching baths show similar effect upon B implantation in Si
- This property is used for making thin membranes

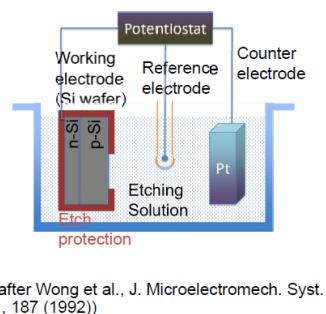
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This is due to the following mechanism: at high boron concentration, the silicon Fermi level drops and the electrons that originate from the negative hydroxyl ions tunnel directly into the valence band rather than staying on the silicon surface for regeneration of new hydroxyl ions from the water. Therefore the etching simply stops as these hydroxyl ions cannot be regenerated. A disadvantage of the boron etch stop is that we have to use very high boron concentrations. And these are not compatible with standard microelectronic devices, and also these compromise the crystal quality of the silicon. Therefore an interesting alternative for making a thin membrane, is the so-called electrochemical etch stop. In this case, we take a lightly p-doped silicon substrate and one deposits on top of that, a lightly doped silicon layer with n-type impurities. Then one brings this substrate in the etching solution, in the KOH solution.

- Disadvantages of B etch-stop

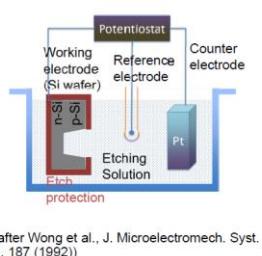
- Very high B concentrations are not compatible with standard CMOS or bipolar microelectronic devices
- High B concentrations compromise the crystal quality (stress, slip planes)
- Alternative: lightly doped p-n junction is used by applying a bias voltage between the wafer and a reference electrode in the etchant
- The p-n junction can be formed by epitaxial growth of an n-type layer (P -doped 10^{15} cm^{-3}) on a lightly B(p)-doped substrate



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So the red part is protection against etching and this part of the wafer is seeing (is in contact with) the etching solution. The end result of the etching is shown here. We have etched through the p-doped silicon, and we recognize the (111) planes here. But when we have reached the n-type doped silicon, the etching stops, and in this way we can make here a thin membrane. How does this work? Two mechanisms are involved. First, we apply a positive potential here, which produces holes at the silicon solution interface, and these attract hydroxyl ions and form silicon dioxide. A competitive process is the dissolution of this silicon dioxide forming this complex ($\text{SiO}_2(\text{OH})_x$) that goes into the solution.

- Applying a positive potential to the wafer produces holes h^+ at the Si/solution interface
- Two mechanisms involved
 - SiO_2 formation: $\text{Si}-\text{OH}$ and $\text{Si}-\text{OH}$ form passivating SiO_2 at surface, splitting off H_2O
 - SiO_2 dissolution by $\text{SiO}_2(\text{OH})_x$ complex formation.
- At V below the passivation potential: oxide is formed and etched away
- Above the passivation potential: complete passivation and all etching stops
- The passivation potential depends on dopant type

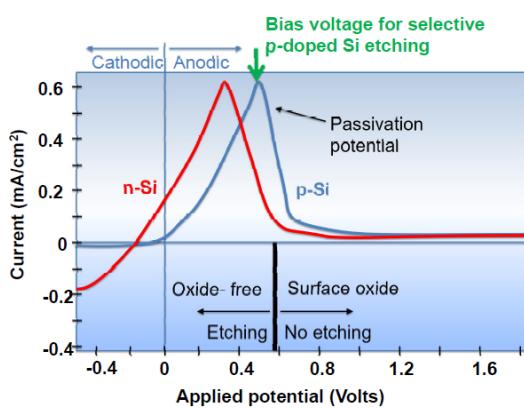


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If the voltage that is applied to the wafer is below the so-called passivation potential, the oxide will be formed and will be dissolved, will go into the solution. So there is continuous oxidation, continuous removal of silicon, so that means etching. Above this passivation potential there will be complete passivation by oxidation and all etching stops. Why does it stop at the interface with the n-type doping? That is because this passivation potential changes and depends on the doping type. This shows a typical current-voltage characteristic for p-doped silicon. Below the passivation potential, that is on this side, there is a current flowing. As holes get transported to the substrate, where they oxidize the silicon, after which the oxide is removed by formation of the complex, which is an etching process. Above the passivation potential, the

current drops as the surface is covered with an oxide and no etching occurs. Here we have added the current-voltage characteristic of n-doped silicon. It has a similar behavior but the passivation potential is different. So this shows where we have to put the bias voltage. It's where there is the green arrow. When this is the voltage we apply, we will have high etching of p-doped silicon, and zero or very little etching of n-doped silicon. And then when reaching the membrane with n-type doping, the etching will stop. We now give examples of bulk micromachining of a (100) oriented silicon wafer in a KOH bath. We draw the wafer with the four vectors indicating the norms to the respective (111) planes. We have covered the wafer with a mask with a rectangular opening, which is oriented along the <110> direction in real space. The picture below shows a cross section of the etching, where one recognizes the typical V-shape for a rectangular opening. If the <110> direction is in this direction, the (111) planes, indeed, are oriented with these facets. After etching, potassium salt residues originating from the KOH bath, may remain on the etched structure. These deposits can be removed by immersing the wafer in an HCl bath. We have again drawn the same (100) wafer but now we have deposited a mask with a circular opening, like given by this dashed line. If we look through a circular opening after etching, we see, again, four (111) planes. And we see that the mask is underetched, so a complete inverted pyramid is present underneath the circular mask. The contour of the basis of this pyramid is shown by this dashed line. The end result of such a microfabrication step is a square or more generally a rectangular structure, which encompasses all extremities of the mask. That is because for this situation, all (111) planes are perfectly protected by the mask and no chemical attack via etching of other crystal planes are possible to remove the silicon atoms on a (111) plane. The picture here shows, again, an arbitrary mask and underneath, one sees indeed again, these V-shaped underetched structures. This example shows the etching of a (100) wafer where we have here a U-shaped mask. We know already that the final structure that will be etched will be an inverted pyramid, the basis of which encompasses all extremities of the mask opening. So the pyramid will be like that. However, before reaching this end result, the etching bath will etch rectangular openings, like shown here, and at this stage the etched structure is stable, and has (111) planes that are not attackable via other crystal planes, except for these two ridges, indicated by the green lines. At the top of these ridges, the silicon atoms that are fixed there, have less than three backbonds to the silicon, which is the reason why they are not so strongly bound and why these get attacked in the KOH bath. Therefore at the ridges, the etching continues, and the etching front proceeds underneath the mask creating this suspended mask structure. At the same time, the etching proceeds also in the vertical direction so that the pyramidal hole gets deeper and deeper.



- Current-voltage characteristic of p-doped Si
- Current-voltage characteristic of n-doped Si
- By selecting the bias voltage at high p-Si etch rate and zero(low) n-Si etch rate, one can selectively remove the p-Si

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This picture shows the situation when the etching under such a beam is proceeding. So here we have a mask beam. These are (111) planes, which are not attacked, but here there is attack on these planes. So this feature is magnified here. So you see here that the (111) planes will disappear at the end because the attack is going on by these planes here, and the complete silicon underneath the beam will be etched away like that. A last example of bulk micromachining is one in which one has again, a (100) wafer with a rectangular mask that has now been oriented along an in-plane <100> direction. That means that this rectangle has been

re-oriented over an in-plane angle of 45-degrees, with respect to the initial rectangular mask we considered. So this is the mask, this is the <110> direction, and we know that the end result will be an inverted pyramid like that. From the beginning of the etching, the (111) planes in these four corners will immediately appear and will not be attacked. However, an interesting intermediate etching result appears, which is sketched in this cross section. Here one sees a hole that is etched, and a vertical plane, and this vertical plane, during etching, is going further and further underneath the mask. How can we understand this? We have here a (100) orientation of the wafer. If we orient the square in the mask like this, this direction will be a (010) plane, and this will be a (001) plane. So that means that the planes are identical in the vertical and in the horizontal direction. So exactly the same etching rate, which will give such a rectangular hole. And these vertical walls, we see it here, and progressively the vertical holes will move in this direction to the extreme directions. At the end, one will reach a (111) plane and if one waits long enough, there will be only the (111) facets of the inverted pyramid which are visible. In this lesson we have discussed two etch stop techniques by which one can make very thin membranes. One etch stop technique was due to a heavy boron-doping, and the second technique was the electrochemical etch stop exploiting the junction between lightly p- and n-doped silicon. Finally, we gave examples of bulk micromachining based on the orientation and shape of the mask on a (100) silicon wafer.

Practice quiz etch stop techniques for thin membrane microfabrication and bulk micromachining

Questions:

1. The etch stop by B implantation in Si, using B concentrations above 10^{20} atoms/cm³, is a technique used to create thin membranes from Si wafers. What is a disadvantage of this process?

- The technique requires the application of a positive potential to the wafer that produces holes at the Si/solution interface
- Very high B concentrations are not compatible with standard CMOS devices and they may compromise the crystal quality
- The silicon crystal orientation has a high influence on the implantation profile and hence it creates its proper B distribution
- The SiO₂ layer on top of the Si wafer does not provide a good B filtering and hence B implantation might extend more than the desired area

2. What is the reason why a mask with arbitrary shape cannot be replicated accurately into the substrate by anisotropic wet etching of the bulk of the substrate?

- A V-shaped structure appears under the mask because the etch rate in the (100) direction is slower than the etch rate in (111) direction
- Using a mask with arbitrary curved structures results in different etching speeds, with deeper holes etched where the radius of curvature of the mask is higher
- Etching stops only when the etchant arrives at (111) planes, which ultimately results in an inverted-roof rectangular structure when viewed from the top
- The opening that is etched underneath the mask is at an angle of 45° with respect to the mask itself

Supercritical drying for realization of suspended structures; test microstructures for quantifying stress in thin layers

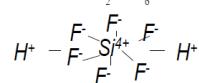
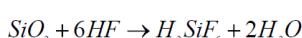


In our introductory lesson on Wet Etching, we have already introduced the concept of surface micromachining which consisted in removing a silicon dioxide thin film from underneath a polysilicon layer

- Supercritical drying
- Microstructures for quantifying stress in thin layers

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so that the latter becomes a suspended functional structure. In this lesson, we will present an issue with this technique that is related to the surface tension of the drying etching liquid which exerts a force on the suspended silicon structure so that the latter can be permanently deformed. Supercritical drying is a technique in which such collapse of the functional silicon structure can be avoided. Another major issue with surface micromachining is the existence of stress in the functional layer which becomes apparent after removal of the sacrificial layer and results in undesirable deformed microstructures. Here, we will introduce some test microstructures that are dedicated for quantifying stress in thin layers.



- Surface machining requires removing a sacrificial layer beneath a functional layer
- Step 1: patterning of SiO_2 sacrificial layer
- Step 2: deposition of polySi layer (for example by LPCVD)
- Step 3: wet etching of SiO_2 in a HF bath forming fluorosilicic acid (H_2SiF_6) and water

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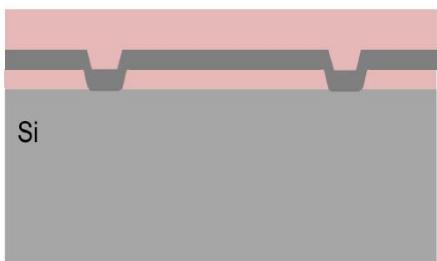
We sketch here again a typical surface micromachining sequence. In surface micromachining, one needs to remove the sacrificial layer from beneath the functional layer. Step one of such a process is the patterning of the silicon dioxide sacrificial layer. So we have patterned it, and there are two parts where the silicon dioxide has been removed. Step two is the deposition of a polysilicon layer, which is a deposition that is conformal to the texture which is already present on the substrate, and it can be performed, for example, by a low-pressure chemical vapor deposition step.



- Reality may be different from the ideal case: during drying of the etching or rinsing solution, the microstructure is pulled down by capillary forces, often leading to unwanted permanent deformation
- Solution to this problem: **supercritical point drying**

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Etching in the HF liquid is based on the formation of the fluorosilicic acid, schematically represented here, that goes into the solution. The drawing here is shown after removal of the wafer out of the etching bath and after rinsing in deionized water. This is the ideal case where everything worked out fine. However, in reality, the situation may be different. During drying of the etching or rinsing solution, a limited amount of liquid underneath the functional structure can pull down the latter towards the substrate by capillary forces. Often, after such collapse, the functional structure cannot be released again and can, hence, not be used in the application. A solution to avoid such problem is the technique of supercritical point drying. In this technique we etch the sacrificial layer in HF bath as schematically illustrated here. Then we replace the HF by deionized water, whereby, the liquid is replaced by a liquid, and no drying is involved. In the next step, in a similar way, we replace the water by ethyl alcohol, which is a liquid with lower surface tension and higher vapor pressure than water. This wafer is then placed in a closed chamber that can be filled with CO₂ gas, to which one can apply high pressure so that the gas is condensed in liquid CO₂ that will occupy, then, also, the space between the functional layer and the substrate. So this will be replaced, this liquid, by liquid CO₂. The picture shows the stainless steel pressurizable vessel in which the wafer is positioned.



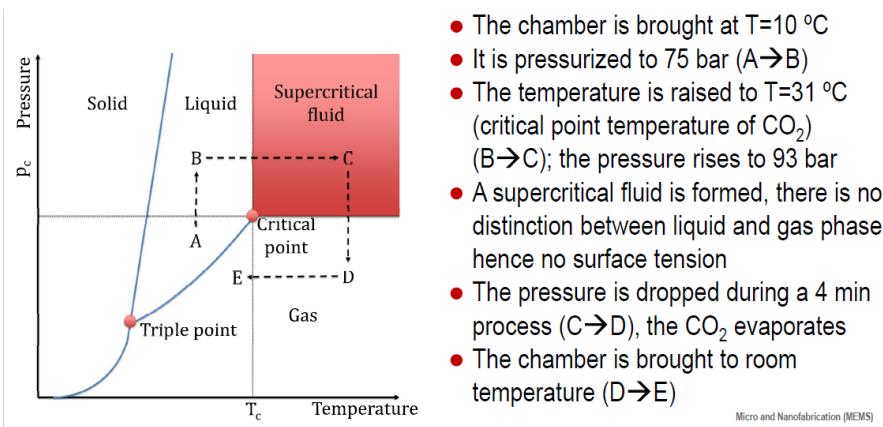
- Sacrificial layer is etched in **HF bath**
- HF is replaced by **deionized water**
- Water is replaced by **ethyl alcohol**
- The wafer is placed in a closed chamber that is filled with **CO₂ gas**, which will be condensed into a liquid



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Here we show a phase diagram for CO₂. On the x-axis, there is the temperature, and on the y-axis, the pressure. At high temperature and low pressure, the CO₂ is in the gas state, while at low temperature, the CO₂ is in the solid state, and in the intermediate temperature range, the CO₂ is in the liquid state. At low pressure there can be transfer from the solid to the gas phase by sublimation.

Let us now discuss the supercritical point drying process. The chamber is brought to 10 degrees Celsius



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and then the chamber is pressurized to 75 bar. This means we go from A to B in the phase diagram. Then we raise the temperature to 31 degrees Celsius, which is the critical point temperature of CO_2 , this temperature. This means that we go from B to C in the diagram, and, in fact, our point C is just above this critical point temperature. Due to this heating, the pressure rises further to 93 bar in the chamber. As when it's just above the critical point of CO_2 , a supercritical fluid is formed in which there is no distinction between the liquid and gas phase anymore and, hence, there is no surface tension. Then one releases the pressure and one brings the CO_2 in the gas phase going from C to D, during which, the CO_2 evaporates. Finally, after removal of all CO_2 , the chamber is brought to room temperature going from D to E, this region. We have now avoided the evaporation of CO_2 from the liquid phase during the drying process, and we have removed all CO_2 . Another issue in surface micromachining is the presence of stress in the surface machined microstructures. This results from the fact that the polysilicon layer is deposited at a high temperature, and that, when cooling down to room temperature, the thermal expansion coefficient of the thick substrate and the thin deposit layer is not the same. The stress becomes most apparent after removal of the sacrificial layer and it is visible by deformed membranes and beam structures. The stress may be compressive, and this happens when the substrate, during cooling, shrinks down more than the thin film, resulting in the type of structure shown here in the schematic diagram. The stress can also be tensile, and this happens when the thin film would like to shrink down more than the substrate, but it's kept under tension by the contact with the substrate at these two points. In such case, it may be that one cannot see the tensile stress because it will result in a straight beam or straight membrane, just like a microstructure without stress.



- Deposition of the polySi layer is done at elevated temperature (for example by LPCVD)
- When cooling down to room temperature and after release of the sacrificial layer, due to different thermal dilatation between film and substrate, stress may develop
- or **tensile**, which is less visible, but eventually the microstructure breaks
- Stress is to be avoided → adaptation of thin film process needed

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Only in case the stress is so high that catastrophic failure of the thin film occurs, it becomes visible. Hence, generally, it is hard to detect tensile stress as it is less easy to observe. Suppose one can detect stress, then this information will be used to fine-tune the deposition process, vary parameters,

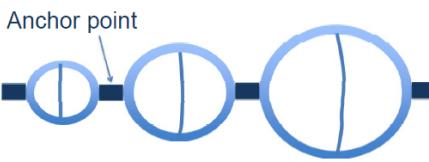
and eventually do annealing treatments of the structures to reduce the stress. So-called ring crossbar test structures are very useful for detecting and quantifying the stress in the thin film material.



- Series of suspended microstructures made in polySi (the functional material in general) and of increasing size, each fixed to the substrate by two anchor points
- If there is no stress in the polySi, the microstructures stay completely flat after removal of the sacrificial layer underneath

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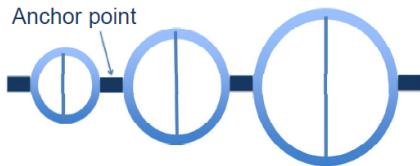
The size of these structures is in the range of between tens of microns to several hundreds of microns and one designs them typically in a row of structures of increasing size. The microstructures consist of a ring with connecting crossbar that are suspended because one has removed the sacrificial layer underneath. Fixation on the substrate is achieved by two anchor points for each ring. If there is no stress in the suspended polysilicon ring crossbar structure, and if one removes the sacrificial layer underneath, the structures stay nicely flat. If these structures are under tensile stress, all suspended materials want to shrink down. The ring is fixed at two anchor points, hence, will shrink down more than the crossbar in the y-direction. So the shrinkage of the x-direction is, in a way, transferred to the y-direction. A result is that the crossbar in the middle will be deformed. It will shrink down too, but not as much as the ring structure in this direction.



- **Tensile stress:** the ring shrinks down, but is fixed at the two anchor points, hence shrinks down more than the crossbar in the y-direction
- Both the ring and crossbar are deformed
- The bigger the microstructure, the more easy deformation is. The size at which deformation occurs allows quantifying the tensile stress

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Planar microstructures are easily recognizable as such when looking through a microscope. Also, the bigger the microstructure, the more easy deformation is. That is why one makes a series of microstructures of increasing size, to look at the size of the ring crossbar structure where deformation will first develop. In this case, this ring. This ring is okay, and here, this is the first ring which shows deformation.



- **Compressive stress:** the ring expands, but is fixed at the two anchor points, hence expands more than the crossbar in the y-direction
- The ring is deformed but the crossbar remains straight
- The bigger the microstructure, the more easy deformation is. The size at which ring deformation occurs allows quantifying the compressive stress

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This allows quantifying the tensile stress. We draw here again the test structures without stress. If these structures are under compressive stress, all suspended materials want to expand. The ring is again fixed at the two anchor points, hence, it will expand more than the crossbar in the y-direction. A result is that the crossbar will stay straight while the ring will be non-planar. The bigger the microstructure, the more easy deformation is. That is why one makes, again, this series of microstructures: to look at the size of the ring crossbar structure where deformation will first develop, and this allows quantifying the compressive stress. The ring crossbar test structure, hence, is a universal detector of stress that can either be of tensile or compressive nature. In this lesson we have explained the technique of supercritical drying using CO₂ by which evaporation from the liquid phase underneath a functional microstructure can be avoided, leading to surface micromachine structures that do not collapse towards a substrate because of the absence of surface tension-driven bending forces. Also, we introduced the phenomenon of intrinsic stress in the functional thin film materials and explained how ring crossbar microstructures can be used for diagnosis of both tensile and compressive stress.

Summary

- Mechanism of supercritical drying using CO₂ for avoiding collapse of surface-micromachined structures
- Ring crossbar structures for diagnosis of tensile or compressive stress in surface-micromachined functional layers

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Practice quiz supercritical drying for realization of suspended structures; test microstructures for quantifying stress in thin layers

Questions:

1. Why is supercritical point drying used after HF etching of a SOI wafer?

- To provide a smooth wafer surface for proceeding to next fabrication steps
- To completely remove HF molecules on the surface in order to prevent any hazardous consequences during wafer handling
- To prevent collapse of free-standing Si structures on the wafer surface by capillary forces
- To remove any organic residues remaining on the wafer surface after etching

2. Which of the following steps is essential in a supercritical point drying cycle?

- CO₂ in the closed chamber is condensed into a liquid
- HF is replaced by cold H₂SO₄
- HF is filled back again in the chamber for one last removal
- Water is replaced by high-pressure acetone

3. Which of the following is true for surface-machined microstructures?

- Stress may develop due to the different thermal dilation between the film and the substrate, while cooling down to room temperature after the release of the sacrificial layer
- Stress can only be compressive
- The compressive stress is less visible than tensile stress in simple beam test structures, as the test structures remain perfectly flat, until they eventually break
- Ring-crossbar test structures can be fabricated to only investigate the tensile stress

Conclusion and summary

We have learned how etching in a liquid bath works. Both anisotropic and isotropic wet etching baths of silicon exist and we have seen how thin membranes can be fabricated using wet etching too. We also discussed the hydrofluoric acid or HF bath for silicon dioxide and glass wet etching. Moreover, we discussed applications of wet etching, like wafer cleaning and removal of sacrificial layers underneath a functional layer to realize free-standing structures. Also we introduced electrochemical etching of silicon substrates for making porous silicon. Here are a few important key points you should remember.

Wet etching of silicon

- An anisotropic etching bath for Si is a potassium hydroxide or KOH solution. Four hydroxyl groups bind progressively to a silicon atom in the 100 plane by injecting four electrons into the valence band of silicon. These interact with water molecules to regenerate four hydroxyl ions, so that there is no charging of the silicon and the etching continues. This etching works for atoms on a 100 plane with two dangling bonds pointing into the etching solution, while, to first order, there is no or very little etching of atoms on a 111 plane, as they have just one dangling bond pointing into the etching solution. Such etching bath can be used for bulk micromachining of silicon substrates.
- A wet etching bath for the isotropic etching of silicon is the so-called HNA bath, consisting of nitric acid, HF, and acetic acid. The HNA bath has three components, two of which are active in the etching, namely the nitric acid and the HF. The acetic acid is a diluent for reducing and controlling the etching rate. The silicon is etched from the substrate and transported into the etching solution via the reaction product fluorosilicic acid, while nitric acid and HF are consumed.
- Silicon can be made micro or nanoporous by etching the wafer in an HF bath under a positive voltage bias onto the silicon wafer with respect to a counter electrode is put into the conducting HF solution. Doing so, one creates unidirectional pores that provide a large effective surface area on the wafer surface.
- A very thin silicon membrane can be made via KOH etching by doping the silicon with boron. The etching stops when the bath reaches the doped layer. An interesting alternative etch-stop technique for making a thin membrane is the so-called electrochemical etch stop. Taking a lightly p-doped substrate, one deposits a lightly n-doped thin layer on top of it. One brings then the substrate in a KOH solution and applies a positive voltage to it, so that the p-doped material is etched away and the thin n-layer stays.

Wet etching of glass and oxides

- Wet etching of glass in an HF bath proceeds by chemisorption of an HF molecule to the SiO network. There is a combined action of the hydrogen on the oxygen atom and of the fluorine to the silicon atom, which weakens the bond between silicon and oxygen atom, the so-called siloxane bond, leading to bond breakage. Gold masks are typically used.
- An etching bath that is frequently used for glass etching, is one in which adds the non-etching ammonium fluoride to the HF bath. The etching rate goes down by addition of the ammonium fluoride. A mix of 40 weight percent ammonium fluoride and 49 weight percent of HF in a ratio from 6 to 1 to 10 to 1 is called buffered oxide etch or buffered HF. The use of buffered HF produces a slower and less aggressive etch, so that photoresist masks can be used, while the latter are strongly degraded in pure HF baths.
- Wet etching permits to make thin membranes by removal of a sacrificial layer by the wet etching bath from beneath a functional layer. The first step in this process is the deposition and patterning of a sacrificial layer like silicon dioxide. The next step in the process is deposition of a functional layer, poly-silicon in our example. The final step in the process is the wet etching of silicon dioxide using an

HF bath, forming fluorosilicic acid as a reaction product. Such process, where one makes a very thin membrane on top of a wafer is an example of so-called surface micro-machining. The membrane fabrication can incorporate a supercritical drying step to avoid collapse of the thin membrane to the substrate.

Wet etching of metals and organic layers

- The iodine-iodide system, which is made by adding iodine and potassium iodide to an aqueous solution, is used to etch gold films. During etching, a gold atom then forms with two iodide ions a complex that goes into the solution under release of an electron.
- A piranha solution consists of a mixture of concentrated sulphuric acid and hydrogen peroxide. It is used for removal of organic residues, like photoresists from wafer surfaces. The organic residue first is attacked by the sulphuric acid, which violently dehydrates the organic molecules. Subsequently, a second reaction starts. The sulphuric acid reacts with the hydrogen oxide to produce atomic oxygen which can dissolve elemental carbon.



Introduction and objectives

Inspection and metrology

This module describes methods of inspection and metrology based on four technique categories: optical, mechanical, charged beam and electrical. Physical principles, setup configurations, advantages and limitations are introduced and discussed for various inspection and metrology methods. The MEMS bi-morph thermal actuator introduced in the first week is taken as the example for a demonstration of each method. In addition, the comparison of measurement or inspection results obtained from different methods is also presented.

At the end of this week, you should be able to:

- Name the different metrology methods and list their main advantages and limitations.
- Describe how the different metrology tools operate and what the important physical principles are that enable each method.
- Classify the different metrology methods according to the working principles and the physical quantities measured.
- Compare different metrology methods. Determine which metrology method should be used for a specific application.

Intro quiz

Questions:

1. Which of the following statements regarding inspection and metrology are true?

- The inspection and metrology should be minimized because they are time consuming and costly.
 - The inspection and metrology are conducted in order to evaluate the processes' performance and to make sure that they are properly conducted.
 - The inspection and metrology can only be done at the end of the process flow to check the MEMS' performance.
 - Some inspection and metrology methods are invasive, therefore possible effects on the device under study must be taken into consideration.
2. What can we do to avoid or minimize the measurement error?
- Periodic calibration of the metrology tool
 - Statistical analysis of the measurement results
 - Assure that the sample is in proper condition for the specific measurement
 - Comparison of the results obtained from different measurement approaches



Inspection and metrology I

Optical microscopy: Inspection and dimension measurement

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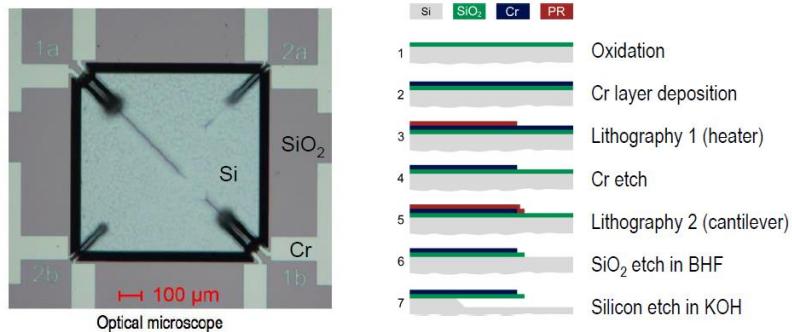
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In the past lessons, we have seen the basics of micro Nano fabrication in a clean room. In the following lessons, I will show you how you can inspect and measure the fabricated structures with various methods.

- Optical microscopy variations
 - Bright field (BF) and Dark field (DF)
 - Differential Interference Contrast (DIC)
 - Others
- Inspection under different modes
- Dimension measurement (XY & Z)
- Calibrated metrology

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I will start by introducing how you can use the optical microscope in different imaging modes to visually inspect the device surface. I will also show you how you can use the optical microscope to quantitatively measure "xy" lateral dimensions and to some extents also film thickness and vertical features in the "z" direction. I will briefly mention the important concerns of calibration.



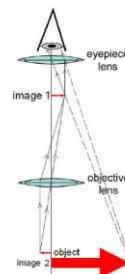
How to check the process result?

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So let's inspect the bi-morph actuator that we use as a case study in this book. Let us see how we can inspect it in order to validate that the fabrication process was successful. On the left, you see a photograph taken with a camera mounted on optical microscope. The scale bar, in red, is very important and serves as a reference to perform dimensional metrology. You certainly remember from the earlier lessons that the cantilevers are bent out of plane and consequently are not in focus. I will show later how focusing on the optical microscope can be used to determine the vertical extension of the micro fabricated MEMS device along the "z" axis.

- Compound lenses to magnify the object
- Total magnification = (magn. of eyepiece lens) x (magn. of objective lens)
- Magn. of eyepiece: 5x, 10x (the most common), 15x, 20x
- Magn. of objective lens: 5x-100x
- Transmitted light for transparent specimen
- Reflected light for opaque specimen



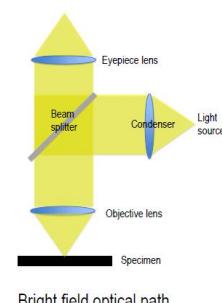
https://commons.wikimedia.org/w/index.php?title=File:Microscope_compound_diagram.png

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The optical microscope is projecting the magnified image of the object via several lenses onto the imaging plane which is either an eye piece or a camera. Modern microscopes have both modes available. Using the eye allows somewhat to get a quick overview and identify contrast mechanisms in the image quite fast .The camera is then better suited to record images and videos to perform metrology and to do image processing. Magnification of samples can go up to 1000 times, which allows seeing features as small as half a micrometer for high contrast samples. Light is either transmitted through transparent samples or is reflected from opaque surfaces.

- 1) Light source
- 2) Condenser
- 3) DIC polarizer slider
- 4) Bright/dark field knob
- 5) XYZ specimen stage
- 6) Objective lenses
- 7) Analyzer slider
- 8) Eyepieces
- 9) CCD camera
- 10) Focus knob
- 11) Controller

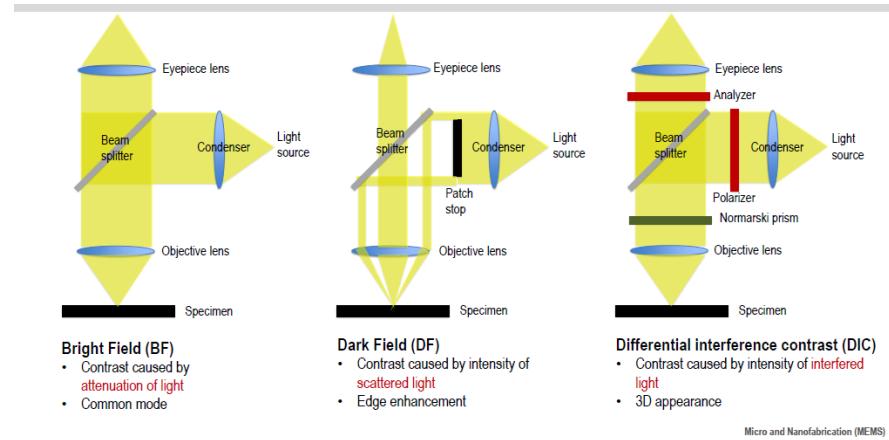


Bright field optical path

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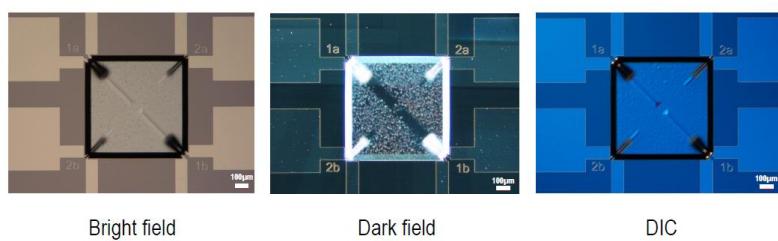
This photo shows a typical optical microscope which is installed in a clean room. The numbers 1 to 11 indicate the key components of the instrument that allow adjusting the microscope settings for various imaging modes and for the x, y, z positioning of the sample. The right side shows the light path coming from the light source going through the lenses into the sample and back to the eyepiece or camera. In this situation, the specimen is viewed in the so called bright field imaging mode. This means that, basically, all the light is used to image the surface. Here, you will see 3 possible and often used variations of optical inspections.



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Left, the already mentioned bright field imaging, in the center, the so called dark field imaging, and in the right hand side, it is the differential interference contrast mode. Let's first look at the difference between bright field and dark field. In dark field, there is a path stop introduced in the light path that blocks the central part of the illumination. Using only the peripheral part of the illumination greatly reduces the image brightness but enhances the detection of scattered light. This dark field imaging mode is therefore much darker, but it shows much better any irregularities on the surface such as edges, defects and dust. In the DIC mode, a Nomarski prism is introduced to split the incoming light into two beams that are shifted by about 200 nanometers. Any light path difference between these two beams caused by surface topography will result in interferences. Using linearly polarized light ensures that the two polarizations of the two split incident light beams are orthogonal to each other after passing through the prism.

- Bi-morph actuator optical microscope inspection



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This way, no interferences will occur until the reflected light from the sample is passing through the prism again, but the polarization of the split light beams is rotated back to the same direction. Interference between the lights from the 2 adjacent points allow quantifying the height difference on the sample surface which provides a 3d appearance of the image in the DIC mode. When we inspect the bi-morph device in these 3 modes, we can then see clearly how the images are different. The bright field image shows the true colors and gives a general overview of the sample surface and dimensions. The dark field is darker in general and highlights parts of the sample that scatters the light beside the bent cantilevers and the KOH etched

slopes in silicon, you can see in particular the sharp edges of the metal pattern, you can also small bright spots on the metal contact pads which shows some surface roughness due to processing. They could also be dust or contamination particles in case the sample was taken out of the clean room.

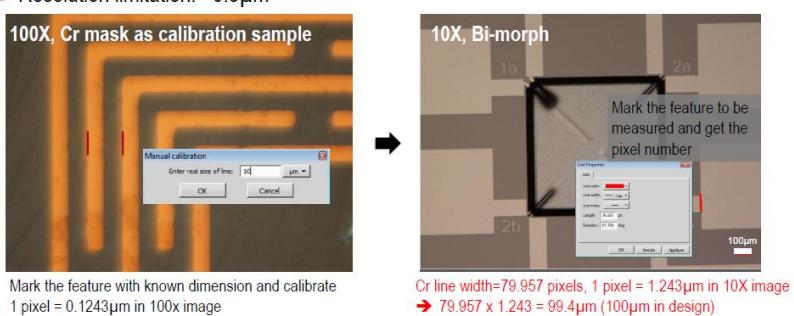
Method	Features	Main Areas of Use
Bright field	• The most common mode • Entire field illuminated	• Commonly used
Dark field	• Observing the scattered light • Edge enhancement	• Defect inspection
DIC	• Enhance the topography • 3D appearance	• Topographical inspection • 3D structure inspection
Phase contrast	• Contrast from interference due to phase shift	• Transparent sample • Live cells observation
Polarizing	• Contrast from specimen birefringence	• Mineral crystals observation
Fluorescence	• Observing fluorescent light	• Cells/tissues labeled with fluorescent dye • Auto-fluorescence

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The DIC image here on the right side reveals a sort of a 3D surface image as it highlights small surface topographic variations by the interference effects. All three imaging modes show complementary information if relevant, one should use them all to complete the inspection of a micro or a Nano structure surface. This table provides an overview of optical inspection variations along with the particular features and main areas of use. Besides the 3 modes already mentioned, the bright field, the dark field and the DIC modes, the table also lists other imaging modes that are not shown in detail in this course, but that are used depending on the sample nature. For instance, when imaging living biological cells that are transparent, one often uses a phase contrast mode to create contrast by interference of the light caused by phase shift inside the sample. Polarizing the light is another way to create contrast due to birefringence effects often used when imaging minerals crystal. And finally, an often used mode is to work with fluorescent material that allows labelling selectively part of the sample to create additional contrast.

- CCD camera → standard sample with known dimension → how many μm per pixel → calibrate the scale bar in the CCD image → use the scale bar as a ruler
- Resolution limitation: $\sim 0.5 \mu\text{m}$



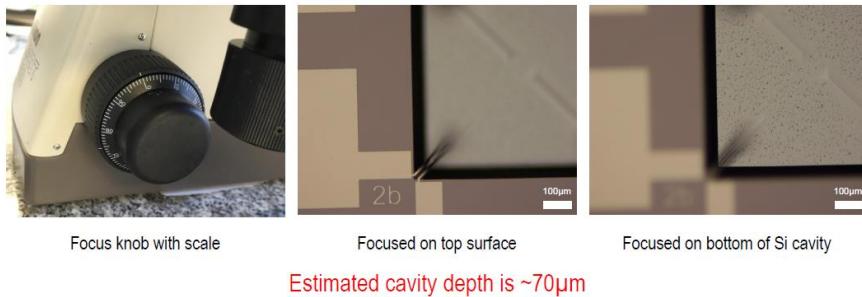
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Besides quality control by optical inspection, it is often necessary to measure dimensions. This is called metrology and is meant to quantify the device length, width and thickness. Modern optical microscopes have a scale bar on the screen as a reference for the lateral dimensions. To ensure accurate dimensions, one performs measurements on a well-known calibration sample. This allows converting the number of micrometers per image pixel into physical dimensions. Using the one handed x objective on a chrome mask calibration sample, one can see that 1 pixel corresponds to about 0.1243 micrometers. We now inspect the bi-morph device with a 10x objective to determine the lateral dimensions of the silicon dioxide beams and chrome wires by using the calibrated value of the pixel size. In this case, you measure the width of the

chrome wires to be 99.4 micrometers, which is slightly less than the 100 micrometers in the design. This deviation is most likely a result of telegraphy processes and chrome etching. Please also remember that the resolution here, is limited by diffraction to about 500 nanometers. To some extent, the optical microscope also allows measuring vertical dimensions.

- Calibrate the scale on focus knob → focused on top surface → focused on bottom surface → read the focus knob scale difference → estimate the Z-dimension



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This practice is simple to implement and allows for a first order of magnitude estimations. As we know, the depth of the focus in an optical microscope is shallow, particularly when using high numerical aperture objectives. If there are 3D surface features on the surface that touches bent cantilevers or etched holes, we can manually displace a sample up or down by along the z axis by the knob, and thereby going in or out of the optical focus. This knob here, has scales with 1 micrometer of resolution. If we focus on the top surface of the bi-morph, record the scale number and then shift focus to the bottom of the silicon cavity, we can read on this scale the travel of the sample and hence its radical extension. Here, we measure the focus displaced in z axis by about 70 micrometer, which is roughly the depth of the edge grooves. For more precise measurement, one should use another metrology tool such as an optical or mechanical profilometer, for instance, as shown later in this mooc class. In this lesson, I have shown you how the optical microscopy can be used, as convenient method for inspection, quality control and dimension measurements of micro fabricated systems. After every step in a micro and nano fabrication process, it is recommended to perform a visual analysis of the sample to detect any potential defect or mistake, before continuing the processing. The optical microscope is a workhorse instrument that provides much information on the device quality and dimensions. There is no need to contact the sample and it works for both opaque and transparent specimen. It is regarded as a fundamental and very important method which is used very frequently in R&D as well as in industrial production.

Summary

- Easy, fast and cost effective method for inspection and dimension measurement
- Multiple modes for specific purpose
- Non-contact, non-invasive
- Works for both opaque and transparent specimens
- Workhorse for sample inspection

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Optical microscopy: details in OM and DIC

Find below links for further information about optical microscope:

- [Detail description of optical microscope components](#) (Wikipedia webpage)
- [Illustration of optical path in a typical optical microscope](#) (Wikipedia webpage)
- [Details about DIC](#) (Wikipedia webpage)

Practice quiz Optical microscopy: inspection and dimension measurement

Questions:

1. A defined structure on a calibration sample has a width of 50 μm . Using the 50x objective, a corresponding number of 96 pixels is determined. How wide (in micrometer) is a sample that is 86 pixels wide using the 20x objective?

- 18 μm
- 112 μm
- 66 μm
- 413 μm

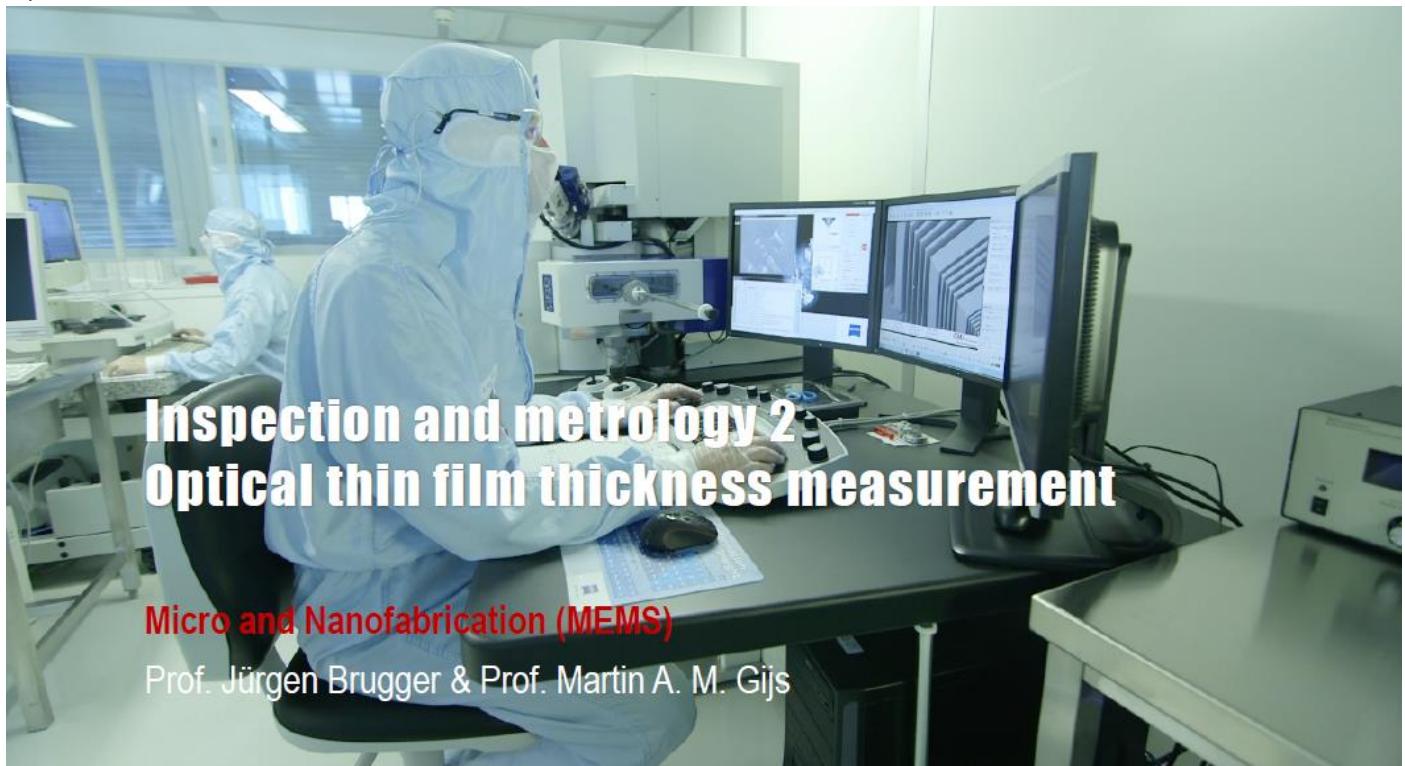
2. Which of the following parts are additionally necessary when performing differential interference contrast (DIC) mode imaging on an optical microscope operated in the bright field (BF) mode?

- Nomarski prism
- Polarizer
- Patch stop
- Aperture
- Analyzer
- Laser

3. Which of the following statements are true regarding the comparison of the bright field (BF) and dark field (DF) imaging mode in optical microscopy?

- An aperture in DF mode blocks the outer part of the light beam thereby decreasing the image brightness
- The DF mode enhances the detection of scattered light from the sample
- The BF mode shows surface irregularities better than DF
- BF images show the samples' true colors
- The microscope setup is exactly the same

- For the DF mode a different light source is needed
- BF and DF modes provide complementary information on the sample surface and thus both should be used for the investigation of MEMS surfaces



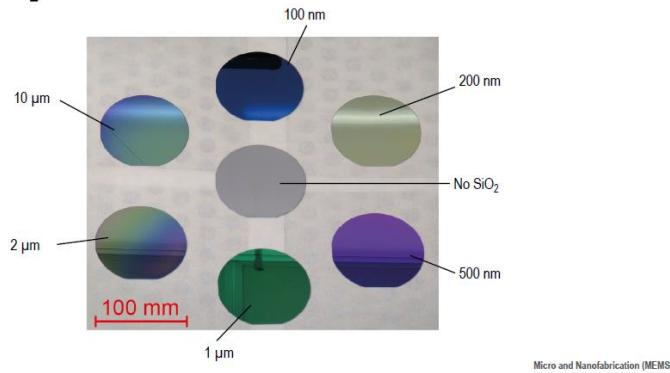
In wafer inspection, metrology and quality control, it is very important to determine the exact thickness of deposited thin films. Here in this lesson, I will show how we can precisely quantify the thickness of transparent films such as silicon dioxide or silicon nitrate using optical methods.

- Physical principle
- Variations
 - Reflectometer & transmittometer
 - Ellipsometer
- Bi-morph SiO₂ thickness measurement

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We will use again the bi-morph device as an example and determine the SiO₂ thickness. Remember, we have already seen these silicon dioxide coated silicon wafers in an earlier lesson. Pay again attention to the different colors appearance which is a function of the sio₂ layer thickness. This effect is due to the interference between the light reflected by the upper and lower boundaries of the transparent thin films. It allows already getting a first estimation of the SiO₂ thickness. For more precise value, we need specific tools. I will now show you how we can determine the SiO₂ layer thickness of the bi-morph device shown here again.

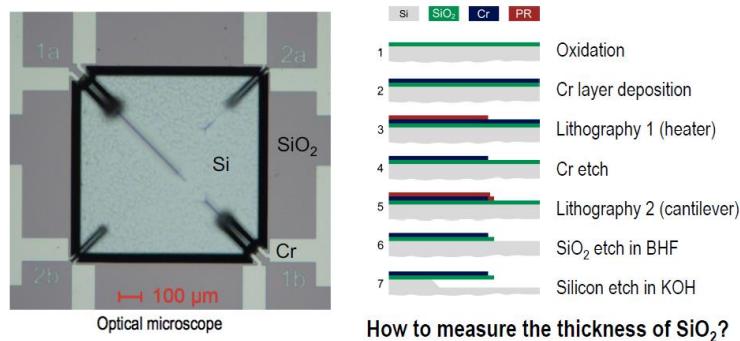
SiO_2 on silicon



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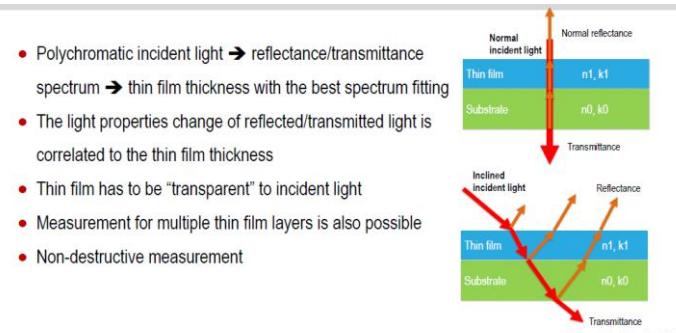
The SiO_2 layer not only defines the mechanical properties of the free standing bi-morph cantilever, over here, but it also delineates the mask layer for the KOH etching like here, here , here and here. Finally, the SiO_2 layer also serves as an electrical isolation between the conducting chrome wires and the underlying silicon substrate. There are 2 ways to perform optical measurements shown here and that use polychromatic light that is incident to the surface either normal or under an angle.



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The light is then reflected back to the instrument and by measuring intensity wavelength, or polarization of the reflected light, one can compute the thin film properties. For instance by knowing the film parameters of "n" and "k", where "n" is the refractive index, and "k" is the extinction coefficient respectively, one can precisely determine the SiO_2 layer thickness. It is also possible to measure multiple thin films. These techniques are entirely non-destructive to the sample. An equipment to measure the layer thickness of thin films using the normal incidence mode is called reflectometer or transmittometer as shown here on the right side. It is based on illuminating the surface with polychromatic light of wavelength between 200 and 1100nm. The reflectometer detects the change in intensity of the reflected light over the light source spectrum. Intensity variations are due to thin film interferences.

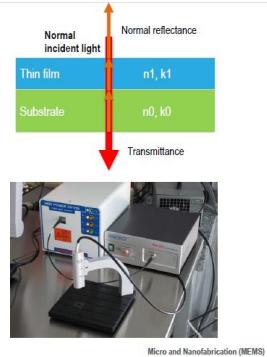


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The illumination spot is in the order of 1.5 mm as a consequence, only large film samples can be measured. The range of thickness measurement is between 1 nm and 40 μm . This is quite a wide range. This method is often used on photoresists, SiO_2 , silicon nitrate, glass, and polymer samples. It also allows determining "n" and "k" values, in case the thickness is already known. Please consult accompanying documents for more physics background of this measurement. Let us take again the wafer in process for the bi-morph device, shown here. You apply this method at the border of the wafer, here, where there is a large enough surface area to place the measurement spot. In this particular case, we measure the SiO_2 layer thickness after the KOH etching. Remember that the target value for the SiO_2 layer is 1.5 μm .

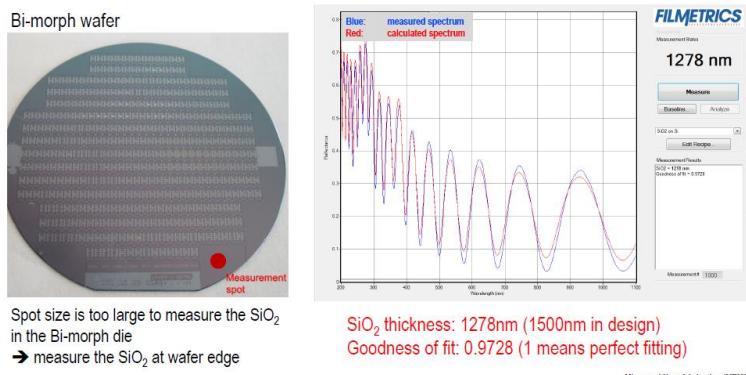
- Normal incidence
- Signal: change in intensity over the wavelength
- Light source: deuterium lamp + halogen lamp (wavelength: 200nm to 1100nm)
- Beam spot size: 1.5mm
- Film thickness range: 1nm to 40 μm
- Thin film material: photoresist, SiO_2 , Si_3N_4 and other polymer, dielectric films
- n, k measurement is also possible



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We also know that the SiO_2 serves as a mask for the KOH etching. But that the SiO_2 is also etched slowly in the KOH etch part. Hence, we expect to see a reduced thickness of the SiO_2 . Let's now verify this here. The curve here, shows the reflectance on the "y" axis as a function of the wavelength on the "x" axis. This spectrum shows a wavy curve as shown here, which is then fitted mathematically to determine the SiO_2 thickness. In our case, we get 1.278 μm which is with the goodness of fit of nearly 1. As expected, the thickness of SiO_2 has been reduced from our initial value of 1.5 μm to 1.278 μm . The 200 nm difference obtained is expected and is due to the loss of SiO_2 during the KOH silicon etch. Another often used tool is the spectroscopic ellipsometer.

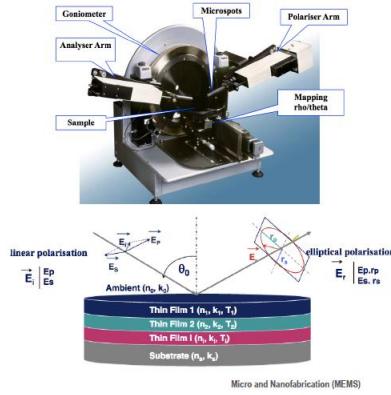


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Here, the angle of light incident is inclined which induces a polarization change after the reflection. The linear polarization of the incoming light is changed to elliptical polarization for the reflected light. The spot size of the light is in the order of 400 μm . And can be aligned to a microstructure if needed. The wavelengths can be varied between 190 nm and 2000 nm, which allows measuring film thickness from a few Amstrongs up to 50 μm thickness. The tool also allows determining to some extent the composition roughness and "n" and "k" values, where "n" is a real, and "k" is the imaginary part of the refractive index.

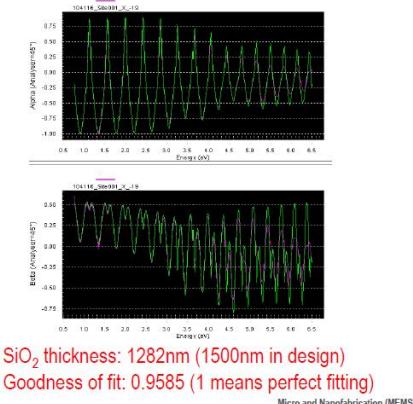
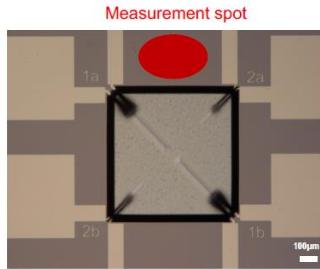
- Inclined incidence
- Change in polarization after reflection
- Spot size: $400\mu\text{m}$
- Wavelength range: 190nm to 2000nm
- Film thickness range: few Å to $50\mu\text{m}$
- Other properties of thin film:
 - Composition
 - Roughness
 - n, k value
- ZnO, PbS, PbSe, TiO_2 , Al, Ag, Au, SiN, SiC, Si, CdTe, CdS...



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It can be applied to a variety of dielectric optically transparent thin films, and even some metal thin films. Please consult the study material for further data on the basics behind this method. As before, I show you now how to use the ellipsometer to measure SIO₂ layer thickness in the bi-morph ship area.

- Use ellipsometer to measure SIO₂ in the Bi-morph die



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The spot size is small enough to measure the SIO₂ thickness at the border of the device like shown here. The two curves here, showing the "y" axis, the "Alpha" and the "Beta" parameter, for an angle of 45 degree and as a function of wavelength here shown in eV units. The parameters alpha and beta in y axis of the spectrum are called ellipse parameters. They are composed of the incident angle and some geometric factors that describe the shape of elliptically polarized light after the reflection. The measurement here results in 1282 nm, which agrees very well the data obtained from the reflectometer. In this module, I have introduced 2 optical techniques to determine the thin film thickness. The reflectometer allows us a quick and simple measurement. For more precise measurement, it is advised to use the ellipsometer. Both of them do not touch and damage the sample, and no sample preparation is required.

Summary

- Reflectometer & Transmittometer
 - Rapid measurement of thin film thickness
 - Large beam spot size
- Ellipsometer
 - Smaller beam size and higher accuracy
 - More complicated methodology
- Both are non-contact, non-invasive
- No sample preparation needed

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Thin film interference and ellipsometry

Find [here](#), a Wikipedia webpage about “thin film interference”, and [here](#), another Wikipedia webpage about “Fresnel equations”, both are principles behind reflectometers and transmittometers. If you are interested in the derivation of Fresnel equations, find [here](#), a literature from Dr. Alexander I. Lvovsky, Department of Physics and Astronomy, University of Calgary. You can also find [here](#), a reflectometer calculator provided by FILMETRICS, the vendor of the reflectometers and transmittometers installed in EPFL CMi. As for ellipsometry, find [here](#) for a Wikipedia webpage about the basic concept of ellipsometry, and [here](#), a document of introduction to ellipsometry from Dr. Jean-Philippe PIEL. You can also find out the concept of complex refractive index [here](#). (Wikipedia webpage)

Practice quiz Optical thin film thickness measurement

Questions:

1. In optical thin film metrology, which of the following statements are true with regards to the incident angle of light?

- Reflectometers and transmittometers operate under normal incidence
- Reflectometers and transmittometers operate under inclined incidence
- Ellipsometers operate under normal incidence
- Ellipsometers operate under inclined incidence

2. Is it possible to measure the thickness of the following thin film material by either reflectometry or transmittometry?

- ZnO
- SiO₂
- Si
- Photoresist
- Si₃N₄
- Dielectric films
- Au

Optical surface profile measurement

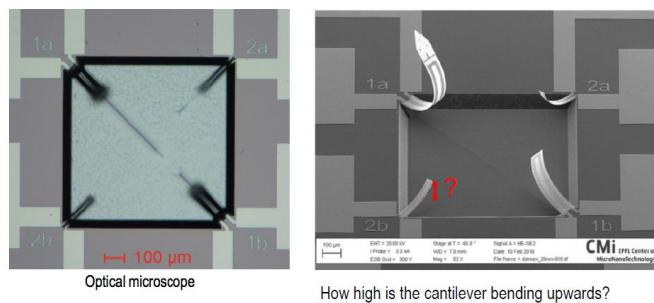


Two additional examples of optical inspection and metrology are a white light interferometer and the laser beam surface profiler.

- White light interferometric (WLI)
surface profiler
- Bi-morph measurement with WLI
- Laser beam surface profiler
- Thin film stress measurement

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They are particularly useful to determine the 3D aspect of MEMS surfaces as well as film stresses. We will use again our bi-morph example and will use both methods to determine the bending of substrate and the bending of cantilever devices.



How high is the cantilever bending upwards?

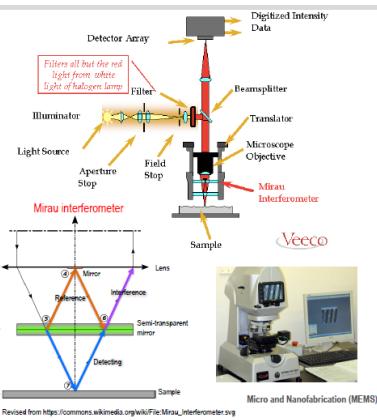
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Here you see again our well known bi-morph actuated devices, let us now quantify precisely how much actually a cantilever is bent upwards. Remember we could estimate this value by the focus control of an optical microscope like shown here. But, let's have a much more precise approach now. The principle of the

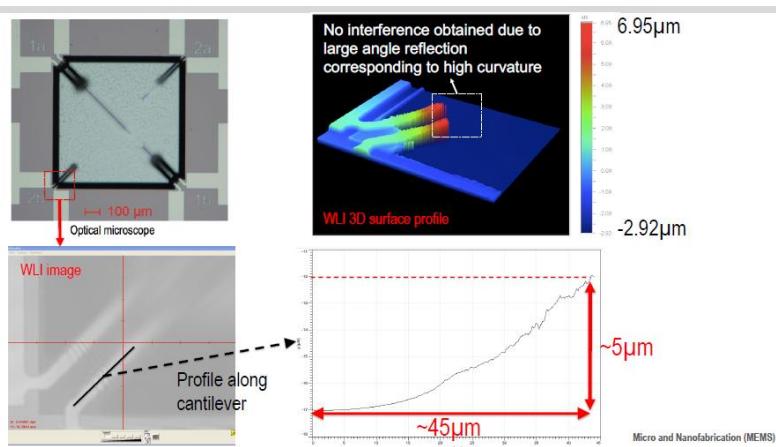
white light interferometer is shown here on the right side with a general overview of the setup, a zoom into the detail of interference part, and the photography of the system in our clean room. The white light interferometer system works as follows. The light coming into the mirau interferometer, is focused by the lens, and further split into 2 beams using a semi-transparent mirror. The reference beam is shown in orange, whilst the object beam is shown in blue. On a flat sample surface, the light path of the reference and the object beams are totally identical, which means the light path difference is 0 and hence constructive interference occurs. On the other hand, if the sample surface is not flat, the light path difference between the reference and the object beam is no longer 0.

- Mirau interferometer embedded objective lenses
- Surface topography → optical path change → interference change
- Scan in vertical direction to obtain 3D surface profile
- Field of view: up to 2.5mm x 1.9mm
- Vertical resolution: < 1nm
- Vertical scan range: 1mm
- Non-contact, non-destructive



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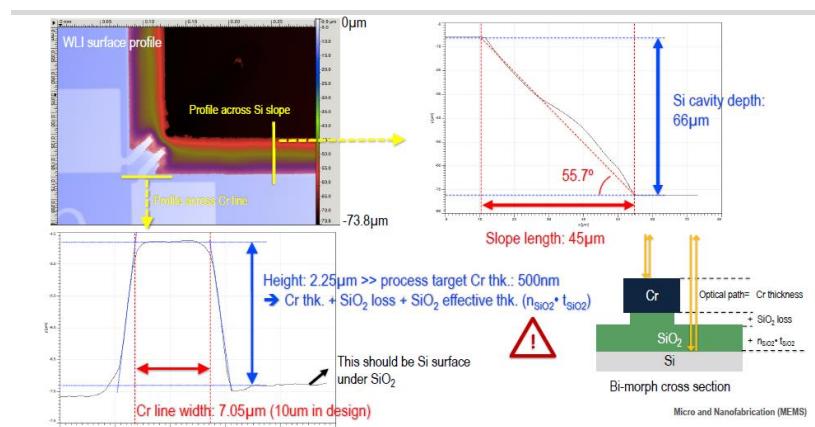
Instead, interference intensity as shown in purple here, will change accordingly and is detected by a light intensity detector. This way, the topographic information of the sample surfaces is obtained, typical values for field of view resolution and "z" scan range are listed here. On the left side, you see the bi-morph cantilever device imaged with the normal optical microscope. Inspecting the bi-morph under the white light interference gives us additional information. White light interference image delivers interference fringes that allow quantifying very precisely the out of plane bending of the cantilever. We can see these fringes here on the bent part of the cantilever. By creating a profile along the cantilever, you obtain the bending curve with quantitative values as shown here. Please notice that for high bending angles above 45 degrees, the system cannot detect any more interference fringes. This can be seen in the curve, by the noisy curve and bumps. The white light interference allows creating a 3D colored map on the high profile.



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Here, red means high, and blue means low. From a certain point the value and height cannot be extracted, because the bending curvature of the cantilever is too high. In this case, tilting the sample could be a solution. The white light interferometer also allows measuring the width of surface patterns and depth of edge grooves as shown here. In this example, let us assess the silicon slope that results from the anisotropic silicon etching in KOH. We know it should be about 54.7 degree, which is the angle between the 100 and 111 crystal

planes of the silicon. But let us measure it now. The data from the white light interferometer tells us that the silicon cavity is 66 um deep. And the silicon slope is 45 um long. With these two values, we calculate the angle to be 55.7 degree, which agrees very well with the theoretical value.



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We can also measure the width and the thickness of the chrome line here. But doing so, I also would like to draw your attention that each measurement should be accompanied with a thorough consideration of the sample condition, to be able to correctly interprets the measurement results. Here, the measured line width of the chrome pattern is 7.05 um. This is quiet in contrast to the design width of 10 um. This difference in values is most likely a result from a non-optimized lithography and chrome wet etch process, and should be improved for more critical devices. The thickness measurement indicates 2.25um as thickness. Remember that chrome thickness was designed to be 500 nm. So, how come that we measure 2.25 um now ? Let us have a look here at this drawing which shows the cross section at the point of interest. The white light interferometer actually detects the surface of silicon underneath the transparent silicon dioxide film. Here. Therefore, the optical path difference is the sum of both: the thickness of the chrome and the thickness of the silicon dioxide. In addition, we need to take into account that the SIO₂ has a reflective index of about 1.5. Which also changes the light propagation inside this medium. Therefore, since the height difference is detected by the light path difference between the reference and object beams, we have to consider the silicon dioxide thickness as effective thickness, which equals the refraction index of silicon dioxide multiplied by the thickness of silicon dioxide. Therefore, the measured total height difference is obviously larger than the true summation of 500 nm for the chrome thickness, and the true silicon dioxide thickness of about 1.3 um. If we take into account the thickness loss due to the KOH etching and which was already confirmed by the measurement result in the previous lesson. The situation here reminds us always not to trust a measurement result without reasonable evaluation. Remember in the "mooc" lesson on physical vapor deposition, we mentioned that the stress from the deposited thin film could lead to wafer and device bending.



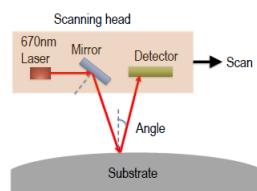
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The origin for this upward or downward pending can be either compressive or tensile stress. Here, I would like to introduce a methodology to determine a thin film stress level by measuring the wafer bending before

and after thin film coating. To this end, we use a laser beam surface profiler. It creates a line scan over the entire wafer surface and thereby determines the surface profile and radius of curvature.

- Laser beam to detect the entire wafer surface profile → curvature
- Too large wafer curvature will affect fabrication process
- Wafer curvature → thin film stress level
 - Stoney equation:

$$\sigma_f = \frac{E_s}{6(1-\nu_s)} \cdot \frac{t_s^2}{t_f} \left(\frac{1}{r_{sf}} - \frac{1}{r_s} \right)$$

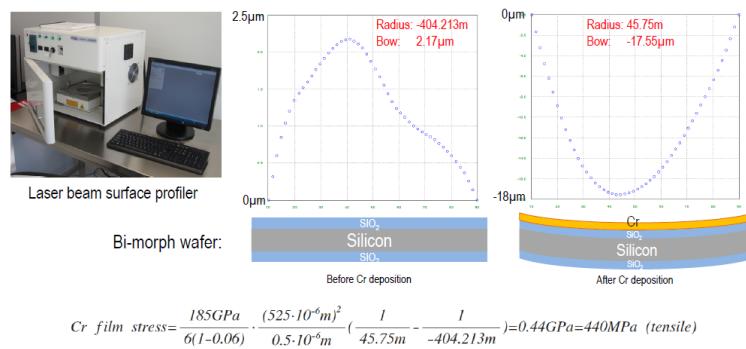


σ_f = stress in film in [Pa], by convention negative stresses are compressive
 E_s = substrate Young's modulus in [Pa]
 ν_s = Poisson ratio of the substrate
 t_f and t_s = film and substrate thickness in [m]
 r_{sf} = radius of curvature of the substrate with the thin film in [m]
 r_s = radius of curvature of the substrate before deposition in [m]

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The drawing here on the right side shows the principle. A laser beam is aligned to the wafer surface and then the reflected beam is detected. The scanning head incorporated both the laser source and the detector. The head is scanning across the entire wafer at a fixed height, and any bending of the wafer will induce changes in the angle of reflection. Therefore, the curvature profile of the entire wafer surface can be obtained. To determine any stress built up during fabrication, we measure the wafer curvature before and after the film deposition. Then we calculate the thin film stress values according to the Stoney equation shown here. You already know it from a previous lesson. Taking the wafer with bi-morph cantilever device as an example, let us now see how by adding the chrome film, the shape of the wafer changes.



$$Cr \text{ film stress} = \frac{185GPa}{6(1-0.06)} \cdot \frac{(525 \cdot 10^{-6}m)^2}{0.5 \cdot 10^{-6}m} \left(\frac{1}{45.75m} - \frac{1}{-404.213m} \right) = 0.44GPa = 440MPa \text{ (tensile)}$$

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The left curve shows the profile of the silicon wafer coated on both side with SIO₂. shown here... before chrome, the bow is 2.17 um which comes slightly from the wafer cutting and polishing. The right curve shows the same wafer after 500 nm thick chrome layer on one side. Now the bow is about -17.55 um. From these values, we calculate the chrome film stress to be 440 Mpa (Mega Pascal) in the tensile direction, based on this formula. Such values are typical and induce the resulting bending as a common artifact during thin film processing. The bow here in the measurement result, indicates the height difference between the peak and the valley of the surface profile. This concludes this lesson on optical surface analysis method for MEMS inspection and metrology. I have shown the white light interferometer and the laser beam surface profilometer. Both are non-contact and thus do not contaminate or damage the sample. They are simple to use, and allow for important in-process characterization of thin film and stress parameters.

Summary

- WLI surface profiler
 - XYZ dimension measurement
 - Released structure measurement
- Laser beam surface profiler
 - Wafer curvature
 - Thin film mechanical stress
- Non-contact, non-invasive
- No sample preparation needed

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Practice quiz Optical surface profile measurement

Questions:

1. What are the limitations or drawbacks of white light interferometric measurements?

- The lateral scanning of the surface profile makes this kind of measurement slow.
- The sample surface needs to be sufficiently reflective.
- Only rigid samples can be measured.
- Steep slopes on the sample surface cannot be measured.

2. Which of the following statements regarding optical surface profilers are true?

- Laser beam surface profiler is best suited to be used to measure the depth of a KOH etched silicon cavity.
- The laser beam surface profiler has the same measurement mechanism as the white light interferometer, but light sources are different.
- The profile measured by the laser beam surface profiler is only a line scan instead of a 3D surface profile.
- The white light interferometer cannot measure the profile at a very steep sidewall.

3. Why is it important to measure the stress of thin films that are used in a micro fabrication process?

- The stress of the thin film could induce a significant wafer bow, which might impact processes such as photolithography, wafer bonding, etc.
- In mechanically released moving parts in MEMS devices, the stress of thin films is correlated to the mechanical properties of the released part.
- By measuring the thin film stress, the adhesion force between the substrate and the thin film can also be obtained.
- By measuring the thin film stress, the performance of the thin film deposition process is monitored.

Mechanical surface profile measurement



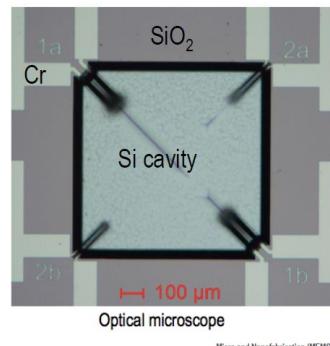
After the optical non-contact methods for wafer inspection, this lesson presents tools that rely on mechanically probing the surface of a wafer of a MEMS device.

- Mechanical surface profiler
- Bi-morph surface profile
measurement
- Atomic force microscopy
- Bi-morph surface roughness
measurement

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One example is the mechanical surface profiler for film thickness measurement. We will apply it to the wafer with the bi-morph cantilever to measure the thickness of the chrome thin films used to build the device. Then, I will show you how the atomic force microscope is used to characterize the surface properties in high resolution. We apply it here to quantify the roughness of the chrome and sio₂ surfaces in the bi-morph device.

- Cr thin film thickness
- Cr and SiO₂ thin film surface roughness

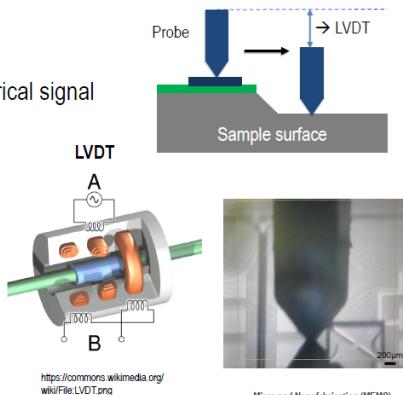


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The position where we intend to measure the chrome layer on top of the sio₂ layer is here. To determine the device property, we need to know precisely the thickness of the chrome film as well as the surface quality, because they influence the device performance. For the first measurement, we used the mechanical surface profiler, which is basically a diamond needle that scans along a linear path in contact with the device surface.

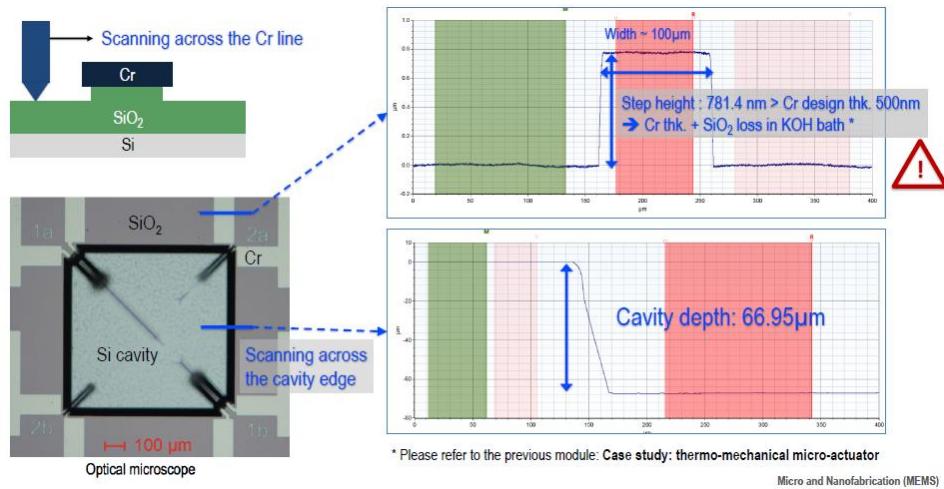
- Diamond probe scans the surface
- Surface height → probe position → electrical signal
- Resolution in Z: ~1nm
- Measurement range in Z: up to 1mm
- Scan length up to 55mm
- Risk to damage the probe or sample

LVDT = linear variable differential transformer



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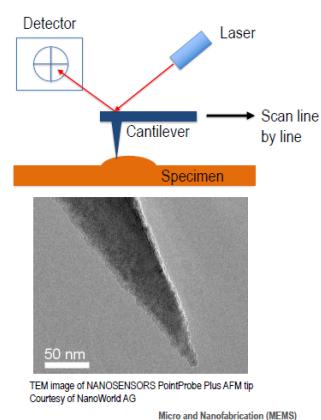
Here, we apply it to determine the thickness of the chrome, film thickness, and here, we apply it to measure the depth of the etched silicon part. Typically, a linear variable differential transformer or LVDT is used to measure the z displacement of the tip. Here, you can see an illustration of an LVDT device. This particular case is based on electromagnetic transducers. It is composed of a moving part in green, with a ferromagnetic material attached to it in blue, and a fix part with three coils embedded. Please see in the study documents how such LVDT is working in detail. You perform so well measurement down to 1 nm of resolution along the z axis. Typical maximum scan length are in the order 55 mm. which is a bit more than half a 4 inch wafer. Since the contact force is not well controlled, it may damage the surface of soft films and cannot be applied to elastic structures. The photo on the right side shows a screen shot from the camera on the tool in our clean room. It shows here the tip above and its shadow below. We can also see the bi-morph device here.



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Here, we see a schematic of the measurement that will be formed. On the surface, we have the pattern chrome, on the sio2 layer on silicon. The drawing is not to scale. We do this measurement after the KOH etching. As we know, KOH also etches to sio2 slowly. So we expect to see this in the profile. The tip is scanned over a chrome thin film pattern from left to right. The scan line is highlighted here in blue on the photo of the device. The diagram here shows the height profile on the z axis as a function of the scan location on the x axis. The measured step height is 781.4 nm which is as expected more than the targeted 500 nm chrome thickness. The additional step comes from the loss of sio2 during the KOH etching. The second curve here shows the scan across the KOH etch shown here on the photo. Here, the depth is about 67 um which agrees well with the design value and also with the optical measurement shown in the previous lesson. Please note while the surface profilometer is very accurate for vertical displacement, it has a poor lateral resolution due to the convolution of a relatively blunt tip. To overcome this resolution limit, we now consider the atomic force microscope or AFM. The AFM is a highly sensitive and high resolution mechanical surface scanner just like the surface profiler we introduced before. The key distinction of the AFM is that it operates in force feedback. By doing so, it reduces the contact force between tip and surface. Due to the high force sensitivity, it does not harm or scratch the surface and can be applied to very fragile surfaces. Very sharp tip is at the end of a flexible cantilever that bends when a force is applied to its end.

- A cantilever probe to touch and scan the surface
- Surface height → probe position → laser signal
- Probe is consumable
- Z resolution: ~ 0.1nm
- XY lateral resolution: < 10nm
- Nano scale 3D surface profile map
- Surface roughness measurement

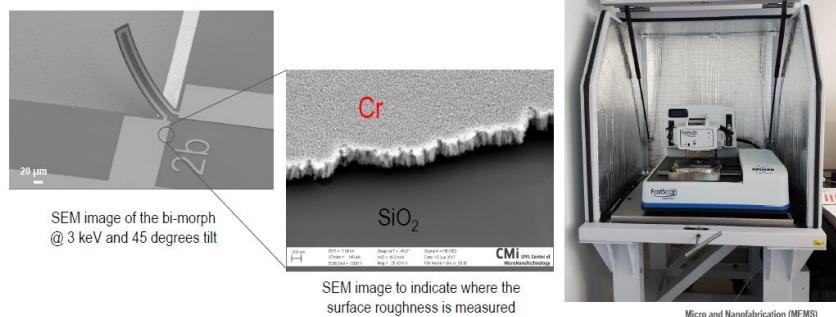


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The bending is measured by a laser beam deflection system as shown here. Here, the tip is a raster scanned with an area of interest and the vertical deflection is recorded for each x-y position. Thus providing a 3 d surface image. The z axis resolution is in the order of 1 Amstrong or below. Lateral resolutions are below 10 nm. Besides making 3d images of the surface at high resolution, it allows quantifying the surface roughness that is often playing a role for device performance. The image on the right side here shows a TEM image of

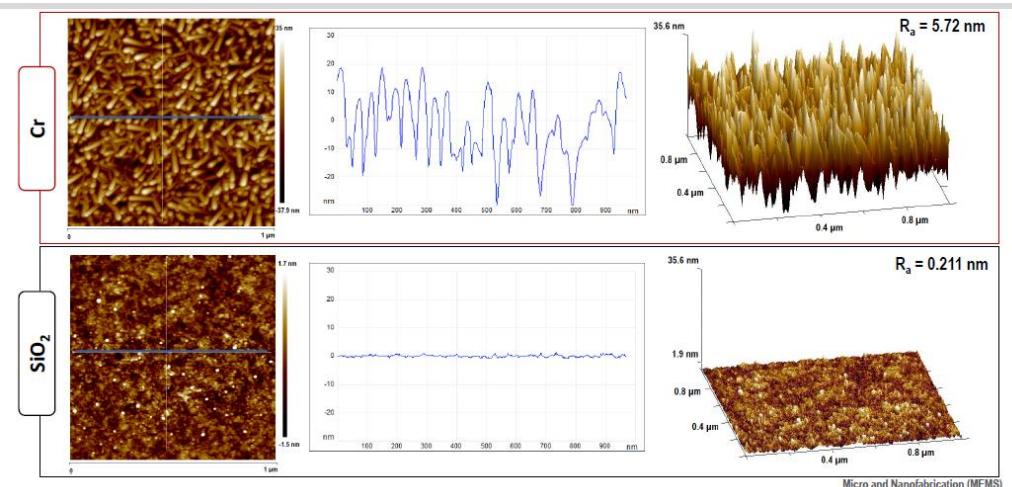
a commercial AFM tip, showing the very sharp epics that provides a higher lateral resolution. Let us now apply AFM to measure the surface roughness of the chrome, and sio₂ layer in the bi-morph device.

- To measure the surface roughness of Cr and SiO₂



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On the left side, you see an SEM image of one of the bi-morph cantilever. The circle here indicates the area of interest that we want to inspect in detail with the AFM. To this end, we mount the sample into an AFM system, and we align the AFM tip to scan the area here on the chrome, and here on the sio₂. A photo of the AFM setup in our clean room is shown here. This Section shows a sequence of screenshots recorded during a real AFM imaging of the chrome sample as discussed before. The Section is partially accelerated and edited to make it shorter.



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In reality, you should count for about 3 to 5 min to setup and prepare the measurements. And then, count about 3 min to record an entire image of about 500 by 500 nm in good resolution. First we locate the measurement site of interest with the aid of the integrated optical microscope. In this case, we aim to inspect a chrome surface on the bi-morph wafer which is the bright area on the image. The AFM cantilever tip is not in contact with the surface during the navigation. Once we are at the right spot to measure, we setup and check the measurement parameters such as the scan size, scan rate, and sampling rate, then we approach the tip to the surface and start scanning. The approach between the tip and the surface is done automatically while monitoring the cantilever response. After approaching the surface, the scanning begins. Here in this sequence, you see the image built up in real time with a real time topographical profile here at the bottom. Now we accelerate the video, in reality the entire image takes 3 min to build up. Please notice that the x and z axis are not in scale and the blue and red lines are the result of forward and backward scanning respectively. The scanning range here, again, is 500 by 500 nm. Here, are shown the AFM scan data of the chrome film here, and sio₂ here. The left shows the top few in color code with x y scan area and the z scale here in this color bar. The surface topography profile along the blue line is shown in the center where we see the chrome

has a roughness of about 5.72 nm in average. We also see that the sio₂ is much smoother and has a roughness of about 0.211 nm in average. To make this difference clear, we show these 2 scanned data with the same z-x value. Here and here. Images on the right are a tilted 3d view of the same scan as shown on the left. They allow for our eyes to see easier the surface nanoscale landscape. This lesson presented 2 mechanical surface profiler instruments. Remember that in some cases the physical contact between the tip and the surface can induce some damage. On the other hand, unlike the optical method seen before, we can also measure the thickness of opaque film which is not available with optical methods. Hence, we can also use AFM to obtain nanoscale images on both conducting and insulating materials. This is an advantage compared to methods using charged beams as you will see in the next lesson.

Summary

- Physical contact
- Opaque film thickness measurement
- AFM for nano scale image
- Conductive / non-conductive samples

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Linear variable differential transformer

Find [here](#) for a Wikipedia webpage of introduction to “linear variable differential transformer (LVDT), which is a key component in a mechanical surface profiler.

Practice quiz Mechanical surface profile measurement

Questions:

1. Which of the following samples are suitable for the use of a mechanical surface profilometer?

- Hard metallic or ceramic surfaces
- Soft organic and inorganic surfaces
- Solid polymeric surfaces
- Liquid samples

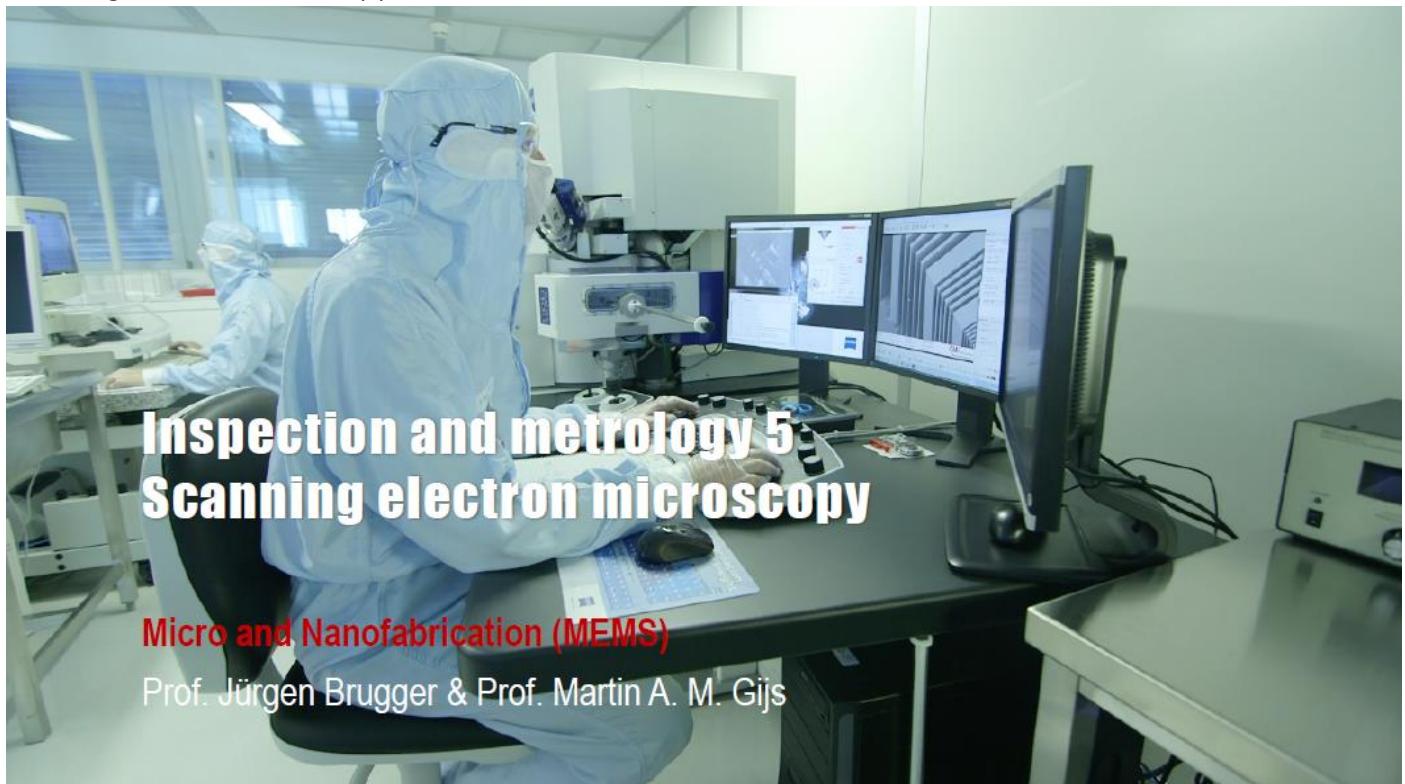
2. Is the mechanical surface profilometry introduced in the video suitable to measure the extent of undercut resulted by an isotropic etching process?

- Yes
- No

3. How is the cantilever deflection measured in an AFM?

- With a piezo actuator that keeps the cantilever at constant distance from the surface.
- With a laser focused onto the backside of the cantilever and a detector that measures the laser beam deflection.
- With the linear variable differential transformer (LVDT), which is attached to the cantilever.

Scanning electron microscopy



Now, I will show you how charged electrons in a scanning microscope can be used to perform inspection, quality control, and metrology.

- Physical principle
- Inspection with different electron signals
- Charging issue
- Dimension measurement

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First, I will remind you briefly how an electron microscope works and how electrons interact with matter. Then, I will list the various electron signals that I used to examine the sample. I will briefly mention the issue of electrons charging, and show how the SEM can be used to perform dimensional metrology at a nanometer scale. As a quick reminder to what we have already seen earlier in this “mooc”, in the chapter of electron beam lithography. We use a focused electron beam primarily to overcome the diffraction limit of optical systems that are typically in the order of lambda over 2, or around 300 nm for visible light. Remember that electrons can be associated to a wavelength, depending on the electron energy, the associated wavelength can be as small as a few pm. Please notice however that the resolution of a scanning electron tool is not limited by the electron wavelength, but by the focusing ability of the system and the electrons scattering, as we have already seen in the lithography lesson. As a thumb rule, remember that a SEM can resolve images of conducting samples down to a few nm, as we can clearly see on this electron microscope here, showing the bi-morph cantilever in very high resolution.

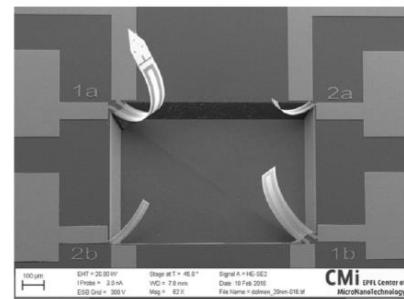
Why use electrons instead of photons?

- Overcome the optical diffraction limit:
 $\sim \lambda/2$
- Electron wavelength, De Broglie equation

kV	1	10	100
nm	0.038	0.012	0.0038

$$\lambda_e = \frac{h}{p}$$

λ : wavelength
h: Planck's constant
p: momentum



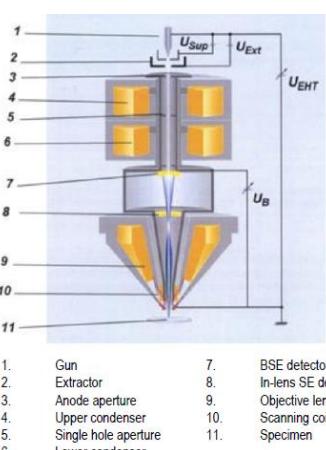
Using electron results in higher resolution compared to visible light

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In a scanning electron microscope, electrons are emitted from an electron gun here, and accelerated under high voltage to obtain momentum and travel through the chamber. Several electromagnetic lenses shape and steer the electron beam. In order to avoid unwanted scattering between electrons and atmospheric molecules, the entire system is working in a vacuum chamber. The electron beam is focused on the specimen surface down here and interacts with its atoms. Detectors and filters, here, number 7 and 8 collect the back scattered electrons. The brightness of each pixel is determined according to the number of collected electrons. The electron beam is deflected to scan the sample surface pixel by pixel and line by line to record an image. During the electron scanning process, negative charges will accumulate on the surface of dielectric material which reduces the image quality. Therefore, for high quality images, a conductive sample is required, or a non-conducting material has to be coated with a thin conducting film. Typically, in good conditions, a modern SEM system can reach resolutions down to about 1 nm and below. Different electron signals can be detected in a scanning electron microscope system. On the right side, you see possible electron atoms interaction. We call the incident electron as primary electron (PE). Mostly, when a PE hits an atom, it generates a secondary electron (SE). Which we can collect to have the secondary electron image or so called SE image. This is the most commonly used signaling in SEM which gives us a good contrast caused by the sample surface topographic structures. The SE detector is situated in the electron beam path as shown here in blue. And is called in lens SE detector which collects most of SE efficiently. Best scattered electrons (BSE) are primary electrons that are reflected or back scattered by elastic collisions with atoms. Atoms with higher atomic number generates higher BSE signals, which allows detecting material contrast. Another special detector is called Everhart- Thornley detector (ET detector). It is designed to collect both SE's and BSE's. Unlike the In-lens SE detector, the E-T detector is placed on the side in the SEM chamber as shown here in orange. To be able to collect SE and BSE with large angles with respect to the PE.

- System similar to EBL:
 - E-gun: 0.02 – 30 kV
 - Electromagnetic lenses
 - Vacuum system
- Electrons → detectors → image
- Morphology & compositional analysis
- Resolution: ~1nm
- Accuracy: +/-3%
- Conductive samples required for high quality imaging



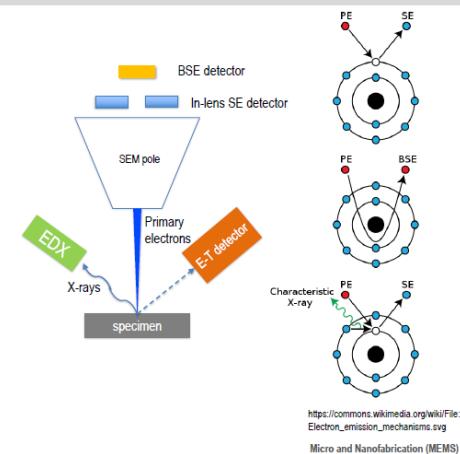
Zesis The GEMINI II column

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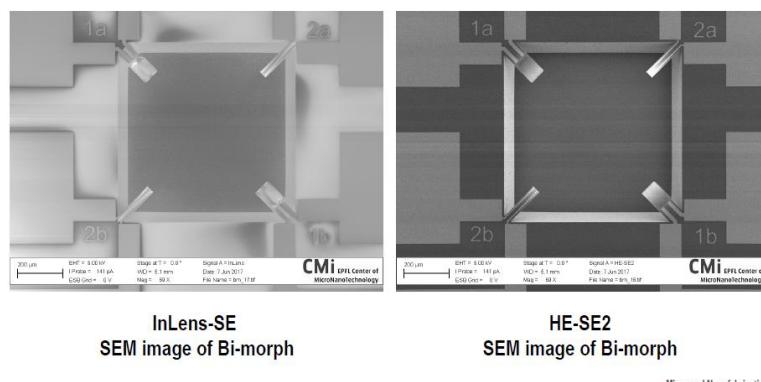
This enhances the image contrast for topographic and etch features. The signal generated from these detectors is called high efficiency SE imaging (HE-SE2) for the specific SEM model that we used during the demonstrations in this chapter. PE with high enough energy can also knock out inner shell electrons from the sample atoms. This causes an electron from a higher energy state to fill the empty state whereby a photon is released. This is the so called characteristic X-ray. By detecting the energy dispersive x ray, we can therefore, perform spectroscopic compositional analysis of the sample in other words, we can determine what material we are looking at, and this at a very high spatial resolution. Here, we can see 2 SEM image taken with different detectors. Both images are taken under same conditions such as electron energy and working distance. On the left side, we see the image taken by in-lens secondary electron detector. It is very bright because it collects most of SE. On the down side, the charging effect of the sio₂ layer on the bi-morph is also obvious. On the other hand HE-SE2 detector shown here on the right hand side provides better contrast and clearer edge definition in the case of the bi-morph device. For our purpose, the choice of this detector is thus preferred. In order to better demonstrate the material contrast of BSE image, here, we use a carbon Nano tube sample as an example.

- Secondary electron (SE) imaging
 - Surface structure
- Backscattered electron (BSE) imaging
 - Atomic number ↑, BSE ↑ → material contrast
- High efficiency SE (HE-SE2) imaging
 - Topography and edge enhancement
- Energy-dispersive X-ray (EDX)
 - X-ray detection
 - Spectroscopic compositional analysis



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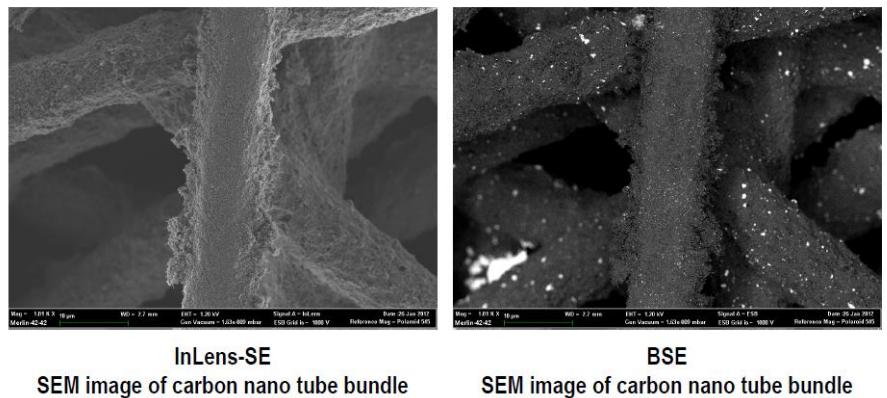
Such a sample is used to adjust and calibrate the SEM tool. Here are bundles of carbon Nano tubes. The scale bar is 10um. The InLens SE image on the left side, here we cannot distinguish the metal and cobalt catalytic nanoparticles that are used during the synthesis of carbon nano tubes. While in the BSE image on the right side, each catalytic particle are highlighted and can be easily detected.



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If there is one downside of charged particle imaging to mention, it is the problem of charging. If the electrons used to image the sample cannot be removed to ground, then, they will accumulate in the sample, which will deviate the trajectory of the next electrons. A direct consequence is a blurred image. The 3 SEM images here show photoresist which is insulating on sio₂ which is also insulating. One can see the charging effect in the left image that increases over time, in the middle. One remedy is to coat the sample with a very thin

conducting layer, either gold or chrome layer. The result can be seen here on the right. Notice that, of course, we are now imaging the gold layer on top of the sample.

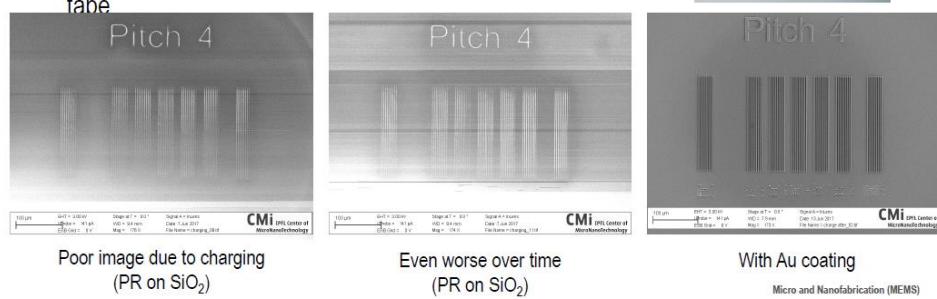
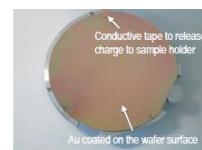


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But for many investigations in MEMS, this is not an issue, and allow seeing the surface quality of the device. To conduct the electron charges to ground, it is important to ensure a proper conduction path. For instance by means of a conducting tape as shown here. In order to perform a calibrated dimension measurement in an SEM, one needs to first ensure that the instrument is calibrated. This is done typically using a calibration with known dimensions. This will translate then, the conversion ratio between each pixel in the digital data acquisition and the sample dimensions in nm or um. This allows defining a scale bar which then can be used to measure the size of unknown samples with high accuracy. The calibration sample are typically made by electrons beam lithography. It is however also well known that, due to over exposure or under exposure, or over or under development, the exact pattern width is not perfectly predictable. That is why instead of using the pattern line width as calibration reference, one favors a periodic pattern where the pitch is highly accurate even if the individual pattern widths are not very precisely defined. The SEM image on the right shows the surface of the bi-morph device where the SEM is now used to measure the width of the chrome pattern.

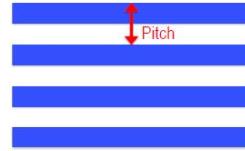
- Electron charges accumulate on the sample and repulse other electrons if the sample is not conductive
- Solution: metal coating (e.g. 20nm Au) + conductive tape



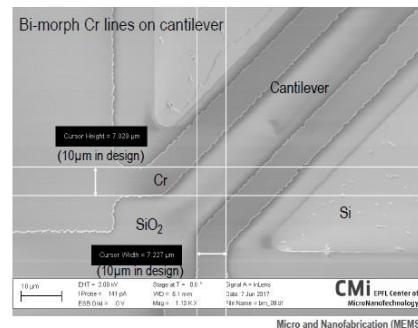
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The white lines are positioned on the SEM tool to accurately measure the chrome pattern. Here we confirm now that the value obtained before, that the chrome pattern is about 7.2 um wide, which is much less than the designed 10 um, and which is due to some lithography effects. Here you see how to inspect a MEM sample in a scanning electron microscope, we mount the sample holder with the silicon MEM sample on the transfer stage. A load lock maintains the high vacuum inside the SEM chamber during the sample transfer. After the sample transfer, we setup the right configuration of the system. The first step is to position the sample to a proper working distance with respect to the electron column and detector. Then, we use the

- Standard sample with known dimension → how many μm per pixel → scale bar calibration
- Use the scale bar to measure XY lateral dimensions



Periodic pattern fabricated by EBL as standard sample for calibration, the line width may vary but **the pitch** is highly accurate



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controller to tune the electron beam and the image. Here on the screen, you see the electron beam image made on a silicon sample with deep reactive ion etched grooves. You see how one can navigate around and zoom in and out. Here, we have seen how electrons, as charged particles in a SEM, can be used to inspect a MEM device surface. It allows for very high resolution in imaging, and allows for dimensional metrology. Remember that some materials might be damaged by the electron charges or heat generated.

Summary

- Magnification up to 500,000X
- Accurate dimensional measurement
- Nano scale inspection (tilting possible)
- Soft samples could be slightly damaged by high energy electrons

Practice quiz Scanning electron microscopy

Questions:

1. Why does scanning electron microscopy exhibit a higher spatial resolution than optical microscopy?

- Larger wavelength of electrons compared to photons
- Smaller wavelength of electrons compared to photons
- Electron is travelling in vacuum
- Lower energy of electrons compared to photons

2. Which of the following components are essential for a typical scanning electron microscope?

- Electron gun
- Ion source
- Electromagnetic lenses
- Vacuum chamber
- X-ray generator
- Electron detectors



Inspection and metrology 6 Focused ion beam: Local cross sectional inspection and measurement

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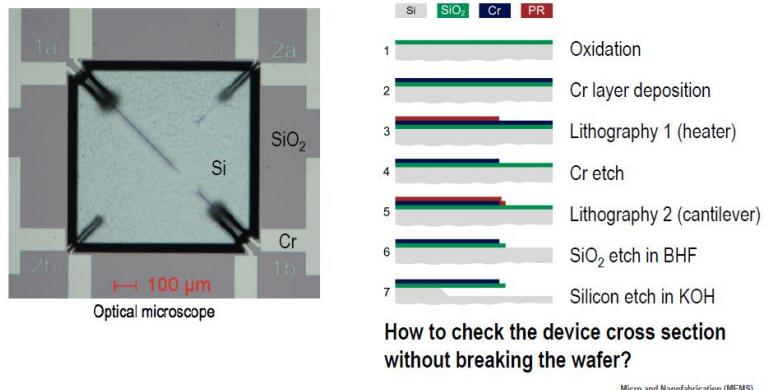
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MEMS processes like the ones shown in this “mooc”, involves layer by layer deposition processes similar to the fabrication of integrated micro electronic circuits.

- Basic principle
- Focused ion beam imaging
- Local cross sectional inspection
- Z-dimension measurement

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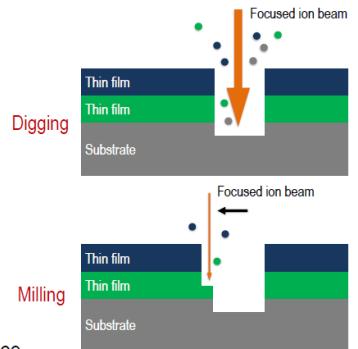
Once the fabrication is finished, it is sometimes necessary to check and characterize the sub surface structure, to perform a quality check, and eventually analyze when there is a device failure. One very useful tool enabling sub surface inspection is the focused ion beam or FIB. It allows removing locally material, and is therefore invasive. I will show you how a FIB system can be used to determine the z-axis dimension of the layers in the micro fabricated MEMS device. Here, we show again the bi-morph cantilever device, our case study, where we fabricated the bi-morph with a layer by layer micro fabrication process shown again here on the right side in cross section.



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In the previous lessons, the sio2 loss in the KOH path during the silicon etching in step 7 here, was already mentioned. We have already measured this by the mechanical and optical profilometer. Here, we will show you how to use the FIB to inspect and measure the amount of sio2 loss in more detail and without breaking the entire wafer.

- Ion imaging:
 - System similar to SEM: Ions (Ga^+) instead of e^-
 - Resolution: $< 10\text{nm}$
 - Damages the sample surface
- Sample sputtering & milling
 - Sub- μm spatial resolution
 - Depth up to hundreds of μm
 - Localized deposition
 - Embedded SEM (Dual-beam system)
 - Conductive samples for better performance

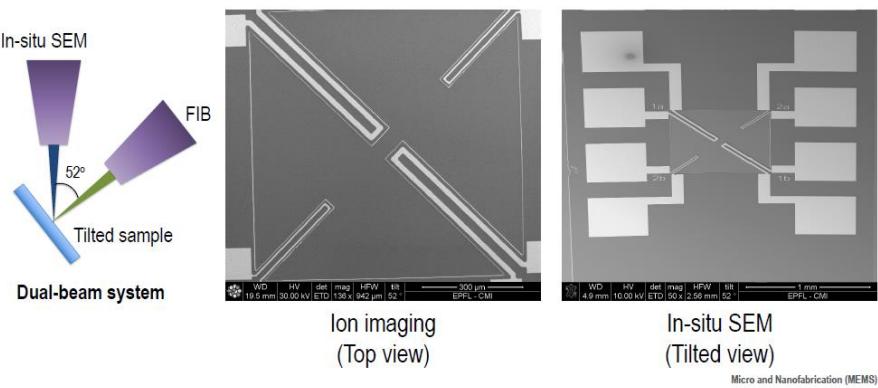


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An FIB system is like an electron beam system, and can also be used for both ion beam imaging and ion beam milling. Instead of using electrons with very small mass, we are now using positively charged ions. The liquid metal ion source is made of Gallium which is heavy, has low melting temperature and thus allows for convenient ion generation. Imaging with gallium plus ions also damages the surface during scanning. One can now utilize this fact to sputter material of the sample surface. The digging or sputtering mode removes material from the sample surface in a larger area and in a faster speed using high ion current. The milling mode removes material from the surface with slower rate and better spatial precision. It results in smoother cross section, and performs some polishing, which is essential to perform cross sectional inspection and dimension measurement. In order to have a well-defined cross section of the sample, there is a need to locally protect the surface from unwanted erosion by the milling. This function is integrated in the FIB system by local platinum deposition.

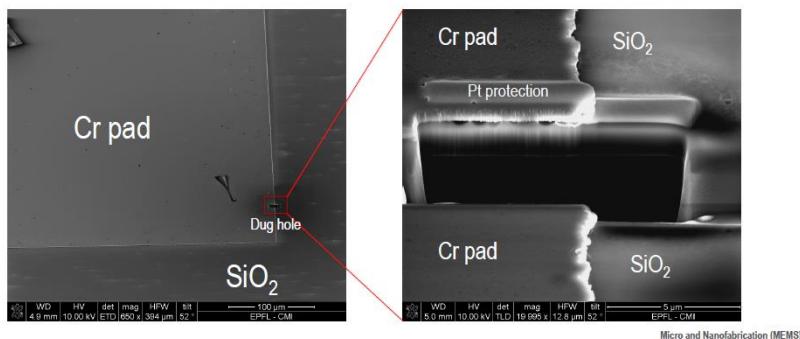
- Sample: bi-morph wafer before KOH wet etch (20nm Cr coated to reduce charging)



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Since ions are damaging the surface when imaging and modern systems is conflicted into a so called dual beam system. That incorporates both an ion beam and an electron beam column. As for the SEM, it is better to perform FIB on a conducting sample. In the dual beam system, the in-situ SEM and FIB columns are arranged at an angle of about 52 degree with respect to each other. In the FIB chamber, we usually tilt the sample so that it faces the ion beam in the normal direction, in order to obtain vertical cross section with respect to the sample surface. Therefore, the in-situ SEM image is taken at the tilting angle of 52 degree with respect to the surface. In order to have a better image quality for us to compare the ion imaging and SEM imaging, and avoid charging, we coat the bi-morph device with a 20 nm thick chrome layer. The sample here is at the process stage before the KOH wet etching of the silicon.

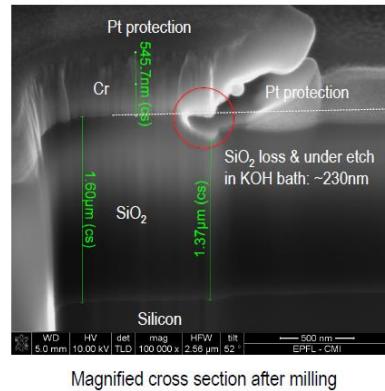
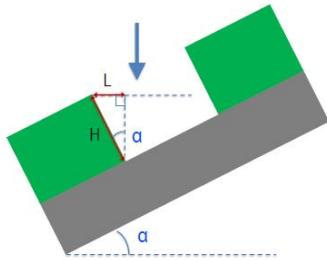
- Sample: Bi-morph wafer after KOH wet etch, without extra Cr coating
- In-situ Pt deposition → FIB digging → FIB milling



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You can see the image quality is quite comparable between ion imaging here, and the SEM electron imaging. So keep in mind however, that the surface is damaged by the ions in the left image. We will now use the FIB for what it is actually designed for, namely to inspect in detail the cross section in the area where the chrome pattern forms and etch on the sio2 layer, shown here. This time, we use the bio-morph wafer after the KOH etch. Remember we know that KOH that we used to etch the silicon, also etches the sio2, and now, we want to verify this etching in detail. We used the focused ion to drill a hole at the edge of the chrome pad. First we add a local layer of platinum protection shown here, in very fine details, by the focused ion beam induced deposition. This platinum layer, not only reduces the charging during FIB milling, but it also provides a smoother top surface to reduce ion scattering during digging and milling, and thus provides a smoother side wall. The photo on the right side shows the structure after the FIB has been used to mill the hole at the cross section between the chrome pad and the sio2.

- Sample tilting is needed for better cross sectional view
- Z dimension compensation: $H = L / \sin(\alpha)$



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The platinum protection here, and the hole created here that goes then deeper into the silicon. We now zoom into the area of interest, with the SEM after the ion milling, so now we don't damage the sample anymore. And for better measurement, we tilt the sample to see clearly into the cross section. We see the silicon substrate here. We see the sio2 which is 1.6um thick here. And we see the chrome layer 545 nm thick. We also see the Pt platinum protection layer here. We see in particular, the under etched sio2 layer that is about 230 nm under etch. Which is exactly the value that we expect from the KOH etching, from the values already obtained by the optical and mechanical surface metrology done in the previous lessons. In the additional study materials, you can find more details on FIB techniques for post process sample inspection and Feeler analysis, and to what one should pay particular attention. In this lesson, you have seen how to use FI to inspect the MEMS device with very high resolution. Remember that this technique is invasive and damages at least locally the devices. But it can be applied to a full wafer in mid process.

Summary

- Ion imaging will damage sample
- In-situ SEM
- Locally destructive cross sectional inspection & measurement

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Application of focused ion beam in failure analysis

Find [here](#), a document of introduction to FIB from Dr. Marco Cantoni, Centre Interdisciplinaire de Microscopie Electronique, EPFL. You can find some applications of FIB including failure analysis starting from page 19.

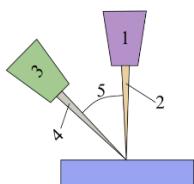
Practice quiz Focused ion beam: local cross sectional inspection and measurement

Questions:

1. Which of the following statements correctly describe the focused ion beam (FIB) technique?

- In the sputtering mode of the FIB, a high electron beam current is used to remove material from the sample.
- The milling mode is used to remove material with better spatial precision and slower rate.
- Unlike scanning electron microscopy, there is no need for a conductive surface for FIB imaging.
- FIB is a non-invasive technique, which allows inspecting a multilayer device in its z dimension.

2. The image below is a scheme of a dual-beam FIB/SEM system. Match the components with the corresponding description



1:

2:

3:

4:

5:



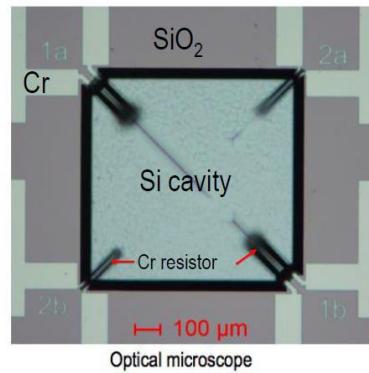
In this module, I will present methods to characterize the electrical properties of micro and nano fabricated devices and systems. I will first introduce how to measure the resistivity of thin films, and in particular provide measured details of the thin chrome film that we used for the bi-morph actuator.

- Resistivity meter
- Bi-morph Cr resistivity measurement
- Prober station
- Bi-morph actuation and measurement

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Then, I will show the functionalities of the prober station and show how to use it for electric characterization of the bi-morph actuator.

How to evaluate the Cr film quality
and determine the resistance of the
Cr heaters?



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Remember our case study of the bi-morph actuator that we used to run through the typical MEMS fabrication processes. We will now have a closer look how we can determine the resistivity of the deposited

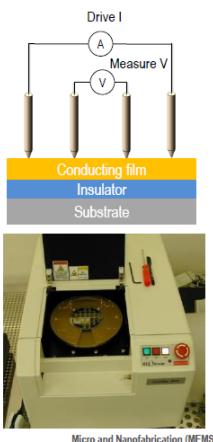
chrome thin film and show how we can calculate and measure the electrical resistance of the chrome heaters, that are used to induced their bending. A well-known and widely used method to determine the resistivity of a thin film is based on the so called Van der Pauw 4 point probe measurement. It is schematically shown here in this drawing. 4 needles with about 1 mm spacing in between are in contact with the thin film in yellow. A source applying a well-controlled current through the 2 outer probes induce a current flowing through the sample in thin film. The 2 inner probes are measuring the voltage difference. The strength of this method is that since we measure a voltage, and not a current, the contact resistance is not critical, and allows for more precise measurement of the resistivity. This method applies to conducting and semi-conducting thin films as well as to bulk samples not shown here in this lecture. With the measured values of voltage and current, we can use the Van der Pauw formulae as shown here, to calculate the sheet resistance.

- To evaluate the metal film quality
- Van der Pauw 4-point measurement
- Probe spacing: ~ 1mm
- Unpatterned film with known thickness on an insulator
- Accuracy: +/- 0.5%

$$\text{Van der Pauw formula for 4-point measurement: } R_s = \frac{\pi}{\ln 2} \cdot \frac{V}{I}$$

$$\text{Calculate resistivity: } \rho = R_s \cdot t$$

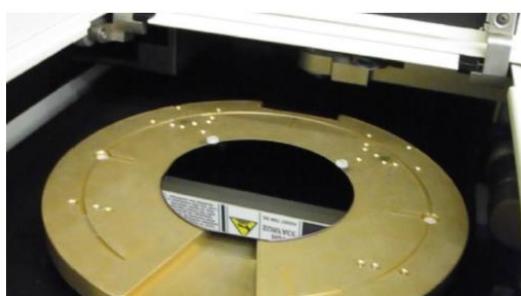
R_s : Sheet resistance (ohm/sq)
 V : Voltage (V)
 I : Applied current (A)
 ρ : Resistivity (ohm·m)
 t : Film thickness (m)



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The pi over log of 2 here, is the geometric factor aid for using 4-point measurement for thin film with a thickness that is negligible with regard to the spacing between the probes. We then can calculate resistivity by multiplying the sheet resistance with the thickness of the thin film. The photograph on the right shows the automatic 4-point probe tool in our clean room, which can measure the sheet resistance on multiple sites on a wafer automatically. Here is a video showing the operation of the resistivity meter in our clean room. The wafer we measure is a sio2 coated silicon wafer, after the 500 nm thick chrome deposition.

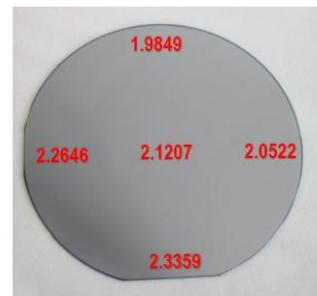


$$\rho = R_s \cdot t$$

$$R_s \text{ mean value} = 2.152 \text{ ohm/sq}$$

$$t_{Cr} = 500 \text{ nm}$$

$$\Rightarrow \text{The resistivity of Cr} = R_s \cdot t_{Cr} = 2.152 \times 500 \times 10^{-9} = 1.076 \times 10^{-6} \text{ ohm}\cdot\text{m}$$



5-sites R_s data (ohm/sq) of bi-morph wafer after Cr deposition

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Once the wafer is placed on the sample holder, and the measurement recipe is set up, the probing head carrying 4 needles will start measuring the sheet resistance from 5 sites on the wafer, automatically. Here we average the 5 sites sheet resistance, and calculate the resistivity of the chrome film on the bi-morph to be 1.076×10^{-6} ohm meter. This is a reasonable value for chrome film deposited on the silicon dioxide by means of thermal evaporation. The resistivity of the deposited metal film may have different values

depending on how the film is deposited. It also depends on the underlying material. Please notice that the resistivity meter can only measure the un-patterned thin film. In the bi-morph device, the chrome resistor is patterned by lithography to form a conducting path with a certain length L, and a width W, in a U shape as shown here, in this drawing.

$$R = \rho \frac{L}{tW} = R_s \cdot \text{sq. where } R_s \equiv \frac{\rho}{t} \quad \text{sq.} \equiv \frac{L}{W}$$

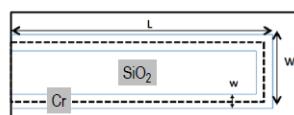
For Cr resistor:

$$R_s = 2.152 \text{ ohm/sq.}$$

$$L = L_{\text{eff}} = 640 \mu\text{m}$$

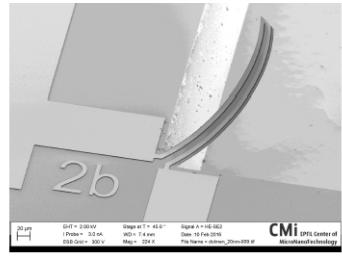
$$W = 7.13 \mu\text{m}$$

$$\text{The resistance of Cr} = 2.152 \times (640 / 7.13) = 193.2 \text{ ohm}$$



$$L_{\text{eff}} = 2\left(L - \frac{w}{2}\right) + W - w$$

R :	Resistance (ohm)
ρ :	Resistivity (ohm•m)
L :	Resistor length (m)
t :	Resistor thickness (m)
W :	Resistor width (m)
R_s :	Sheet resistance (ohm/sq.)
sq.:	Square number

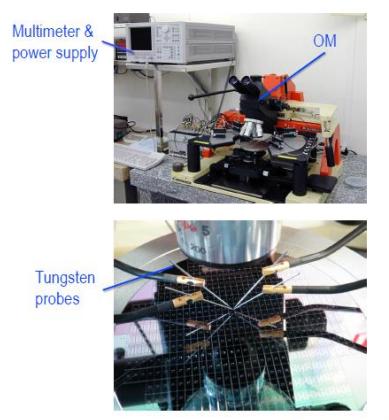


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Let us now calculate the resistance of the chrome heater. Resistance equals resistivity times the resistor length over the thickness and the width. The definition of sheet resistance = resistivity /resistor thickness and the squared number defined as resistor length / resistor width. The resistance = sheet resistance * sq. In this case, the sheet resistance of chrome film is obtained from resistivity meter as 2.152 ohm square. The effective length of the u shaped chrome resistor is defined as shown here, and the value is 640 um. The width of the chrome resistor is obtained by averaging sub measurements resulting in the previous chapter, about 7.13 um. All together we calculate the resistance of the chrome resistor to be 193.2 ohm. The tool to access to the inner parts of a MEMS and to apply electrical signals is often based on a prober, which is nothing else than fine needles that can be positioned with micrometer precision on a specific location of a MEMS device.

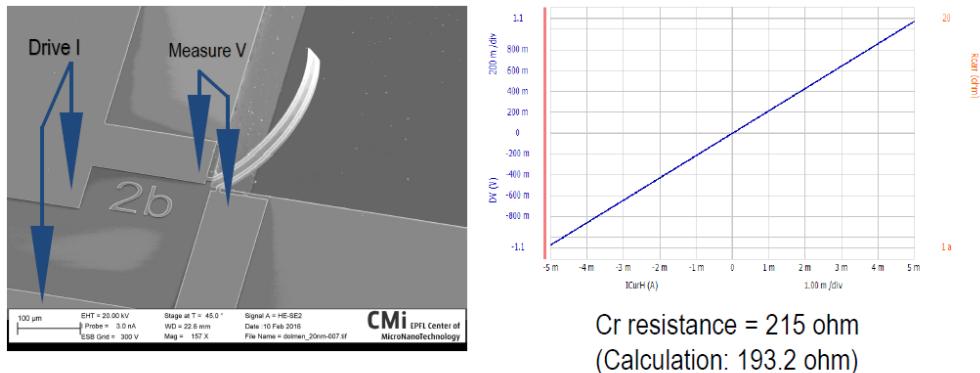
- OM + tungsten micro probes + multimeter & power supply
- Metal pads needed: $> 50 \times 50 \mu\text{m}^2$
- Electronics characterization
 - Current (0.1 fA – 1 A), voltage (0.5 µV – 200 V)
- I-V, C-V, C-f, C-t curves
- MEMS resonant frequency



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Tungsten needles can be controlled under an optical microscope, with micrometer precision and controlled electrical signals, such as voltage and current can be applied. A minimum contact area of 50 by 50 um is needed to position the needles properly. Typical curves that one can extract are IV, CV, C-f and C-t measurements. To some extent, also high frequency measurements can be done. In our case, we apply a DC voltage to determine the resistive value of our bi-morph MEMS device. Here you see now on the left side an SEM image, one of our chrome bi-morph actuator beams, the blue arrows show where we apply the prober needles. Here again, we use a 4 probe principle to inject the current here, and to measure the voltage here. The current will then flows through the cantilever in and out in this 'u' shaped wire. By doing so, we are not



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influenced by the contact resistances between the needles and the contact pads. Which is often not well defined and could induce some errors. The right plot here shows the resulting IV curve of the measurement. The applied current on the x axis and the resulting voltage on the y-axis. By calculating the slope, we can find that resistance of the bi-morph actuator is 215 ohms. It is about 10 % deviated from what we just calculated in the slides before. We have seen a few simple, but essential methods to determine the electrical properties of fabricated micro devices, it allows ultimately determining whether the process has been successful, and allows further to study new materials, and their electrical properties. This is very important to improve the device performance of new MEMS and MEMS. This last metrology and inspection lessons, closes the MEMS mooc lectures. On behalf of the entire mooc MEMS team, I would like to thank you for your interest and active participation. As always, we are eager to read your comments and feedback to further improve these lessons in upcoming sessions. Bye for now and enjoy the quizzes.

Summary

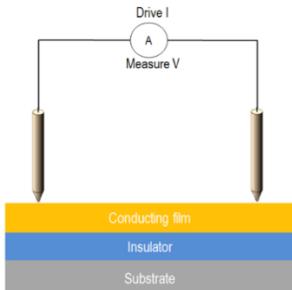
- Proper test pattern design
- Risk to burn out the device
- Always make the pads big enough
- Ohmic contact

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Practice quiz Electrical characterization

Questions:

1. Let us consider an electronic multimeter that has 1% accuracy and the possibility to work in both 2-point (see the following picture) and 4-point mode. Assuming the per-branch parasitic resistance is 1 Ohm, what is the minimum resistance you can measure with the 2-point approach? Consider a factor of 10 as error margin.



- 1 mOhm
 - 10 mOhm
 - 200 mOhm
 - 20 mOhm
2. Let us consider the metal connections in a bi-morph thermal actuator. Which of the following are good strategies to minimize the parasitic resistance and the capacitance of the metal connections?
- Increase the thickness of the metal connections.
 - Maximize the square number of the metal connections.
 - Reduce the overall area of the metal connections on the silicon substrate.
 - Increase the sheet resistance of the metal connections.

Conclusion and summary

In this chapter about inspection and metrology, you have learned the physical principles, the different setup configurations as well as the advantages and limitations of four different techniques which are optical, mechanical, charged beam and electrical techniques. You were also reminded how important it is to evaluate and analyze your measurement result. And how to decide which tools to use under different circumstances since some of them are invasive or even destructive to the sample. Here are a few important key points you should remember.

Inspection

- Optical microscopes are for dimensions larger than 0.5 um
- Scanning electron microscopes are for dimensions down to several nm
- Atomic force microscopes can be used to inspect nanoscale patterns on non-conducting samples, but rather time-consuming

Thin film thickness measurement

- The reflectometer / transmittometer is a simple and effective tool to measure dielectric films, better before the patterning since the spot is big
- The ellipsometer is a more powerful and complicated tool, requires practical experience to do the analytical measurement
- Surface profilometer can be also used to detect the film thickness on a patterned structure, but beware of the sample condition like thickness loss or transparency of underlying film or substrate

XY lateral dimension measurement

- Calibrated optical microscope and scanning electron microscope are usually used to measure lateral dimensions
- The mechanical surface profilometer is not recommended for lateral dimension measurement due to the convolution of the tip

Z dimension measurement

- The mechanical profilometer is used to avoid the potential optical issue on the sample
- The optical profilometer is used to obtain 3D map and to avoid the potential risk of damage on the sample surface
- Surface roughness can be obtained with an atomic force microscope
- Focus ion beam is used to have local cross-sectional inspection and Z dimension measurement without destructing the entire sample

Electrical characterization

- The resistivity is one of the physical quantities used to characterize conducting thin films and deposition processes
- Prober station can be used to measure various electrical properties. Make sure to design the conducting pads big enough and make sure you have the ohmic contact between probes and conducting pads.

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Links

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- [Thermo-mechanical micro actuator: dynamic response](#)
- [Thermal evaporation: materials and parameters](#)
- [Sputtering: plasma detailed explanation](#)

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