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BMS College of Engineering, Bangalore-560019

(Autonomous Institute, Affiliated to VTU, Belgaum)

July / August 2017 Supplementary Semester Examinations

Course: Elements of Electronics Engineering — Duration: **3 hrs**
Course Code: 14EC1ICEEE/14EC2ICEEE — Max Marks: **100**

Date: 28.07.2017

Instructions:

UNIT 1

1	a	Explain the working of n-p-n transistor with a neat diagram.	6
	b	Calculate the values of I_C, I_E, β_{dc} for a transistor with $\alpha_{dc} = 0.98$ and $I_B=120\mu A$	4
	c	Explain the working of voltage divider biasing circuit and Calculate V_{CE} and I_C for the circuit given $\beta=100$, for a silicon transistor. [Refer Fig. 1(c)]	10

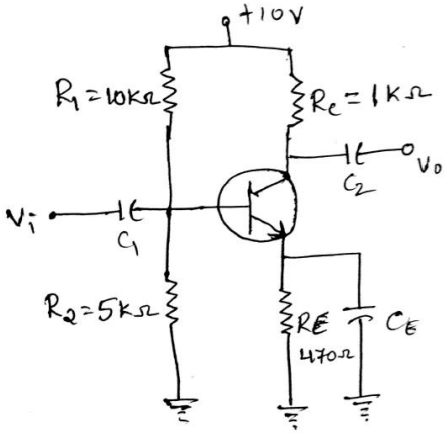

Fig. 1(c)

OR

2	a	Compare (i) FET and BJT (ii). NMOS and PMOS	8
	b	With neat sketch, Explain the construction of p-channel FET.	6
	c	Draw the circuit diagram to obtain the drain characteristics for n-channel JFET. Explain the characteristics.	6

UNIT 2

3	a	Mention the advantages of Negative Feedback	5
	b	Compare C_B, C_E, C_C Circuits.	5
	c	Explain classification of amplifiers	10

OR

4	a	Explain different types of feedback topologies.	10
	b	Explain re model of voltage divider bias configuration with necessary equations	10

UNIT 3

5	a	Explain Colpitt's oscillator with a neat circuit. Given $C_1=C_2=C$ and L=100µH, Frequency of oscillation is 500 kHz. Determine value of C.	10
	b	List the characteristics of ideal OPAMP. Calculate the output voltage of the circuit given below	10

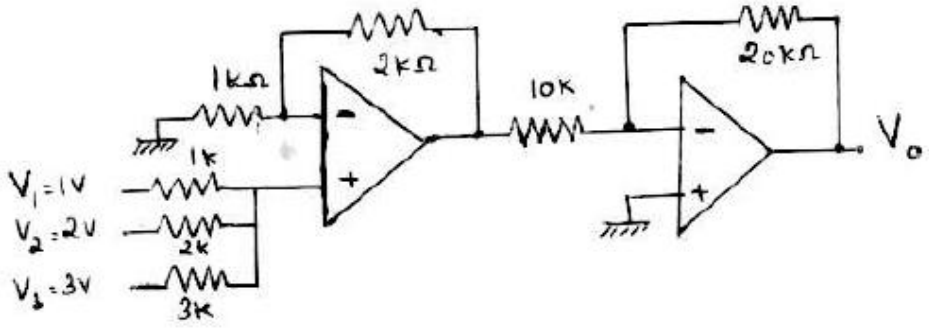

Fig. 5(b)

UNIT 4

6	a	Convert the following: (i). $(ABCD)_{16}$ = (?)$_2$ = (?)$_8$ = (?)$_{10}$ (ii). $(725.25)_8$ = (?)$_2$ = (?)$_{10}$	8
	b	Implement EX-OR gate using only NAND gates.	4
	c	Design full adder and Implement using two half adder and one OR gate.	8

UNIT 5

7	a	Explain the block Diagram of a Digital Communication System.	10
	b	Summarise the advantages and disadvantages of LED and LCD	10

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