

Digital Design and Computer Organisation Laboratory
3rd Semester, Academic Year 2025

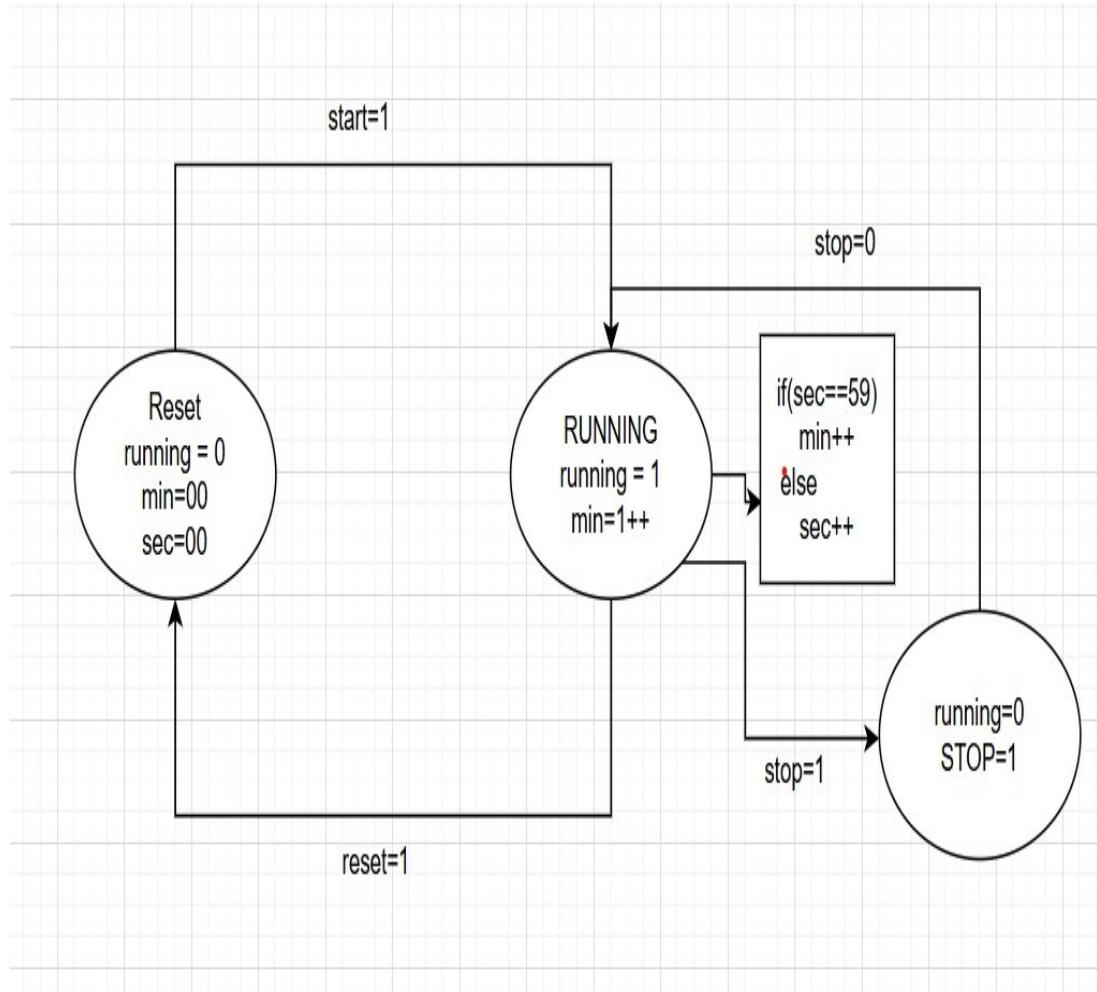
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TITLE: Stop Watch(Start, Reset, Stop)

Deliverables

- I. Verilog Code Screenshot
- II. Verilog VVP Output Screen Shot
- III. GTKWAVE Screenshot
- IV. Output Table to be completed and included

State Diagram



IVERLOG CODE

```
1 module stopwatch (
2     input clk,          // clock input (1 Hz or divided clock)
3     input reset,        // reset stopwatch
4     input start,        // start counting
5     input stop,         // stop counting
6     output reg [5:0] sec, // seconds (0-59)
7     output reg [5:0] min // minutes (0-59)
8 );
9
10    reg running; // keeps track if stopwatch is running
11
12    always @(posedge clk or posedge reset) begin
13        if (reset) begin
14            // Reset all values
15            sec <= 0;
16            min <= 0;
17            running <= 0;
18        end
19        else begin
20            // Control logic
21            if (start)
22                running <= 1;
23            else if (stop)
24                running <= 0;
25
26            // Time counting
27            if (running) begin
28                if (sec == 59) begin
29                    sec <= 0;
30                    if (min == 59)
31                        min <= 0;      // reset after 59:59
32                    else
33                        min <= min + 1;
34                end
35                else begin
36                    sec <= sec + 1;
37                end
38            end
39        end
40    end
41 endmodule
42
```

TEST BENCH

```
1 `timescale 1ns/1ps
2
3 module stopwatch_tb;
4     reg clk, reset, start, stop;
5     wire [5:0] sec, min;
6
7     // Instantiate the stopwatch
8     stopwatch uut (
9         .clk(clk),
10        .reset(reset),
11        .start(start),
12        .stop(stop),
13        .sec(sec),
14        .min(min)
15    );
16
17     // Clock generation: toggle every 5 ns -> 100 MHz
18     initial begin
19         clk = 0;
20         forever #5 clk = ~clk;
21     end
22
23     initial begin
24         // For GTKWave dump
25         $dumpfile("stopwatch.vcd");
26         $dumpvars(0, stopwatch_tb);
27
28         // Initialize signals
29         reset = 1; start = 0; stop = 0;
30         #20 reset = 0;      // Release reset after 20 ns
31
32         #20 start = 1;    // Start counting
33         #10 start = 0;    // Pulse style start button
34
35         // Let it run for a while
36         #600 stop = 1;    // Stop after ~600 ns
37         #10 stop = 0;
38
39         #100 start = 1;   // Start again
40         #10 start = 0;
41
42         #300 reset = 1;   // Reset stopwatch
43         #20 reset = 0;
44
45         #200 $finish;     // End simulation
46     end
47
48     // Display output on console
49     initial begin
50         $monitor("T=%0t | running=%b | min=
51         | sec=          $time, uut.running, min, sec);
52     ", end
53 endmodule
54
```

VVP OUTPUT

```

ibrahim@adu:~/Clie_mini/00C0> M>main> 21:16 vvp stopwatch.vvp
VCD info: dumpfile stopwatch.vcd opened for output.
T=0 | running=0 | min=0 | sec=0
T=45000 | running=1 | min=0 | sec=0
T=55000 | running=1 | min=0 | sec=1
T=65000 | running=1 | min=0 | sec=2
T=75000 | running=1 | min=0 | sec=3
T=85000 | running=1 | min=0 | sec=4
T=95000 | running=1 | min=0 | sec=5
T=105000 | running=1 | min=0 | sec=6
T=115000 | running=1 | min=0 | sec=7
T=125000 | running=1 | min=0 | sec=8
T=135000 | running=1 | min=0 | sec=9
T=145000 | running=1 | min=0 | sec=10
T=155000 | running=1 | min=0 | sec=11
T=165000 | running=1 | min=0 | sec=12
T=175000 | running=1 | min=0 | sec=13
T=185000 | running=1 | min=0 | sec=14
T=195000 | running=1 | min=0 | sec=15
T=205000 | running=1 | min=0 | sec=16
T=215000 | running=1 | min=0 | sec=17
T=225000 | running=1 | min=0 | sec=18
T=235000 | running=1 | min=0 | sec=19
T=245000 | running=1 | min=0 | sec=20
T=255000 | running=1 | min=0 | sec=21
T=265000 | running=1 | min=0 | sec=22
T=275000 | running=1 | min=0 | sec=23
T=285000 | running=1 | min=0 | sec=24
T=295000 | running=1 | min=0 | sec=25
T=305000 | running=1 | min=0 | sec=26
T=315000 | running=1 | min=0 | sec=27
T=325000 | running=1 | min=0 | sec=28
T=335000 | running=1 | min=0 | sec=29
T=345000 | running=1 | min=0 | sec=30
T=355000 | running=1 | min=0 | sec=31
T=365000 | running=1 | min=0 | sec=32
T=375000 | running=1 | min=0 | sec=33
T=385000 | running=1 | min=0 | sec=34
T=395000 | running=1 | min=0 | sec=35
T=405000 | running=1 | min=0 | sec=36
T=415000 | running=1 | min=0 | sec=37
T=425000 | running=1 | min=0 | sec=38
T=435000 | running=1 | min=0 | sec=39
T=445000 | running=1 | min=0 | sec=40
T=455000 | running=1 | min=0 | sec=41
T=465000 | running=1 | min=0 | sec=42
T=475000 | running=1 | min=0 | sec=43
T=485000 | running=1 | min=0 | sec=44
T=495000 | running=1 | min=0 | sec=45
T=505000 | running=1 | min=0 | sec=46
T=515000 | running=1 | min=0 | sec=47
T=525000 | running=1 | min=0 | sec=48
T=485000 | running=1 | min=0 | sec=44
T=495000 | running=1 | min=0 | sec=45
T=505000 | running=1 | min=0 | sec=46
T=515000 | running=1 | min=0 | sec=47
T=525000 | running=1 | min=0 | sec=48
T=535000 | running=1 | min=0 | sec=49
T=545000 | running=1 | min=0 | sec=50
T=555000 | running=1 | min=0 | sec=51
T=565000 | running=1 | min=0 | sec=52
T=575000 | running=1 | min=0 | sec=53
T=585000 | running=1 | min=0 | sec=54
T=595000 | running=1 | min=0 | sec=55
T=605000 | running=1 | min=0 | sec=56
T=615000 | running=1 | min=0 | sec=57
T=625000 | running=1 | min=0 | sec=58
T=635000 | running=1 | min=0 | sec=59
T=645000 | running=1 | min=0 | sec=60
T=655000 | running=1 | min=1 | sec=1
T=665000 | running=1 | min=1 | sec=1
T=675000 | running=1 | min=1 | sec=1
T=685000 | running=1 | min=1 | sec=1
T=695000 | running=1 | min=1 | sec=1
T=705000 | running=1 | min=1 | sec=1
T=715000 | running=1 | min=1 | sec=1
T=725000 | running=1 | min=1 | sec=1
T=735000 | running=1 | min=1 | sec=1
T=745000 | running=1 | min=1 | sec=1
T=755000 | running=1 | min=1 | sec=1
T=765000 | running=1 | min=1 | sec=1
T=775000 | running=1 | min=1 | sec=2
T=785000 | running=1 | min=1 | sec=3
T=795000 | running=1 | min=1 | sec=4
T=805000 | running=1 | min=1 | sec=5
T=815000 | running=1 | min=1 | sec=6
T=825000 | running=1 | min=1 | sec=7
T=835000 | running=1 | min=1 | sec=8
T=845000 | running=1 | min=1 | sec=9
T=855000 | running=1 | min=1 | sec=10
T=865000 | running=1 | min=1 | sec=11
T=875000 | running=1 | min=1 | sec=12
T=885000 | running=1 | min=1 | sec=13
T=895000 | running=1 | min=1 | sec=14
T=905000 | running=1 | min=1 | sec=15
T=915000 | running=1 | min=1 | sec=16
T=925000 | running=1 | min=1 | sec=17
T=935000 | running=1 | min=1 | sec=18
T=945000 | running=1 | min=1 | sec=19
T=955000 | running=1 | min=1 | sec=20
T=965000 | running=1 | min=1 | sec=21
T=975000 | running=1 | min=1 | sec=22
T=985000 | running=1 | min=1 | sec=23
T=995000 | running=1 | min=1 | sec=24
T=1005000 | running=1 | min=1 | sec=25
T=1015000 | running=1 | min=1 | sec=26
T=1025000 | running=1 | min=1 | sec=27
T=1035000 | running=1 | min=1 | sec=28
T=1045000 | running=1 | min=1 | sec=29
T=1055000 | running=1 | min=1 | sec=30
T=1065000 | running=1 | min=1 | sec=31
T=1075000 | running=1 | min=0 | sec=0
T=1070000 | running=0 | min=0 | sec=0
tb_stopwatch.v:45: $finish called at 12900000 (1ps)
ibrahim@adu: ~/Clie_mini/00C0> M>main> 21:16

```

GTKWAVE

