

Digital Design and Computer Organisation Laboratory
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TITLE: Stop Watch(Start, Reset, Stop)

Deliverables

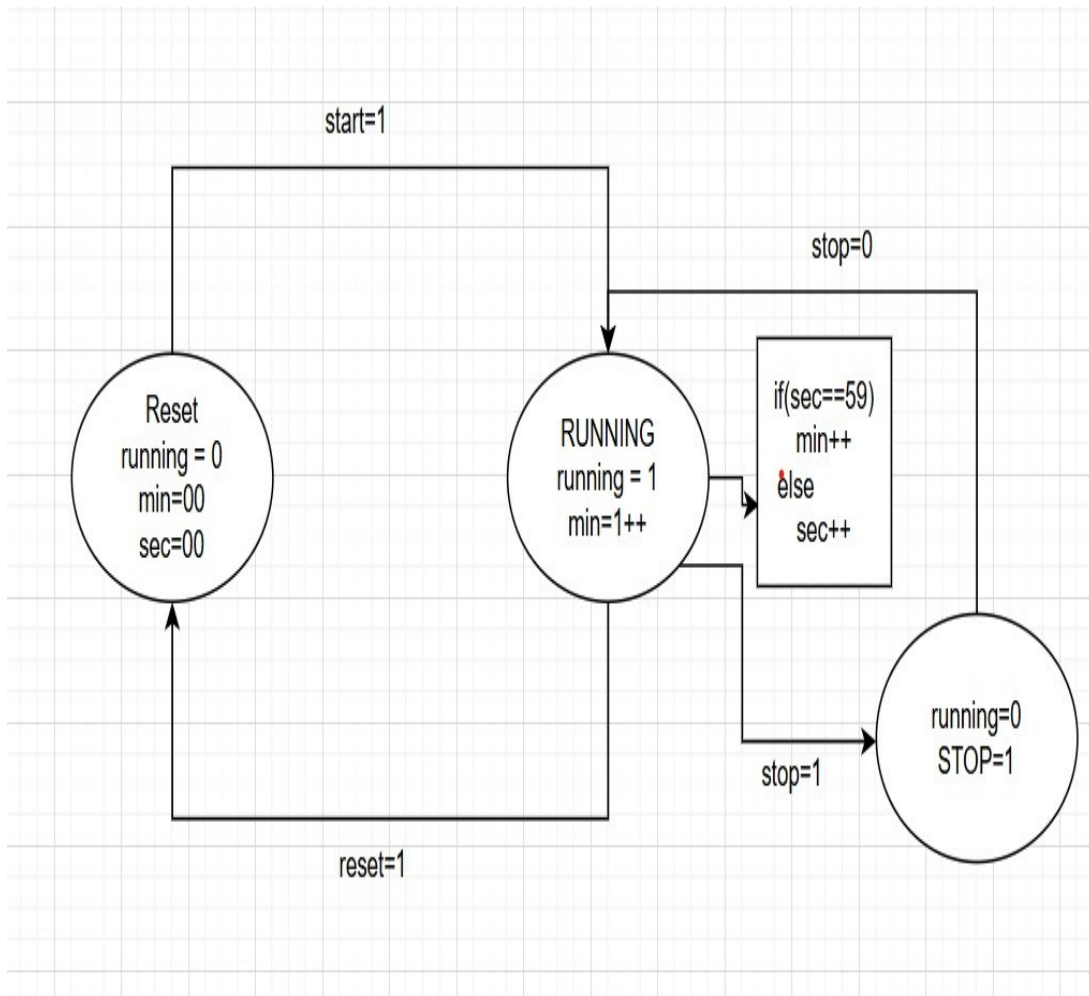
I. Verilog Code Screenshot

II. Verilog VVP Output Screen Shot

III. GTKWAVE Screenshot

IV. Output Table to be completed and included

State Diagram



IVERLOG CODE

```
1  module stopwatch (  
2      input clk,          // clock input (1 Hz or divided clock)  
3      input reset,        // reset stopwatch  
4      input start,        // start counting  
5      input stop,         // stop counting  
6      output reg [5:0] sec, // seconds (0-59)  
7      output reg [5:0] min  // minutes (0-59)  
8  );  
9  
10     reg running; // keeps track if stopwatch is running  
11  
12     always @(posedge clk or posedge reset) begin  
13         if (reset) begin  
14             // Reset all values  
15             sec <= 0;  
16             min <= 0;  
17             running <= 0;  
18         end  
19         else begin  
20             // Control logic  
21             if (start)  
22                 running <= 1;  
23             else if (stop)  
24                 running <= 0;  
25  
26             // Time counting  
27             if (running) begin  
28                 if (sec == 59) begin  
29                     sec <= 0;  
30                     if (min == 59)  
31                         min <= 0; // reset after 59:59  
32                     else  
33                         min <= min + 1;  
34                 end  
35                 else begin  
36                     sec <= sec + 1;  
37                 end  
38             end  
39         end  
40     end  
41 endmodule  
42
```

TEST BENCH

```
1 `timescale 1ns/1ps
2
3 module stopwatch_tb;
4     reg clk, reset, start, stop;
5     wire [5:0] sec, min;
6
7     // Instantiate the stopwatch
8     stopwatch uut (
9         .clk(clk),
10        .reset(reset),
11        .start(start),
12        .stop(stop),
13        .sec(sec),
14        .min(min)
15    );
16
17    // Clock generation: toggle every 5 ns -> 100 MHz
18    initial begin
19        clk = 0;
20        forever #5 clk = ~clk;
21    end
22
23    initial begin
24        // For GTKWave dump
25        $dumpfile("stopwatch.vcd");
26        $dumpvars(0, stopwatch_tb);
27
28        // Initialize signals
29        reset = 1; start = 0; stop = 0;
30        #20 reset = 0;    // Release reset after 20 ns
31
32        #20 start = 1;    // Start counting
33        #10 start = 0;    // Pulse style start button
34
35        // Let it run for a while
36        #600 stop = 1;    // Stop after ~600 ns
37        #10 stop = 0;
38
39        #100 start = 1;    // Start again
40        #10 start = 0;
41
42        #300 reset = 1;    // Reset stopwatch
43        #20 reset = 0;
44
45        #200 $finish;    // End simulation
46    end
47
48    // Display output on console
49    initial begin
50        $monitor("T=%0t | running=%b | min=
51        | sec=          $time, uut.running, min, sec);
52        ", end
53    endmodule
54
```

VVP OUTPUT

```
ibrahimfadu /C:/s.mini/0000 P main 21:16 vvp stopwatch.vvp
VCD info: dumpfile stopwatch.vcd opened for output.
T=0 | running=0 | min=0 | sec=0
T=45000 | running=1 | min=0 | sec=0
T=50000 | running=1 | min=0 | sec=1
T=60000 | running=1 | min=0 | sec=2
T=70000 | running=1 | min=0 | sec=3
T=80000 | running=1 | min=0 | sec=4
T=90000 | running=1 | min=0 | sec=5
T=100000 | running=1 | min=0 | sec=6
T=110000 | running=1 | min=0 | sec=7
T=120000 | running=1 | min=0 | sec=8
T=130000 | running=1 | min=0 | sec=9
T=140000 | running=1 | min=0 | sec=10
T=150000 | running=1 | min=0 | sec=11
T=160000 | running=1 | min=0 | sec=12
T=170000 | running=1 | min=0 | sec=13
T=180000 | running=1 | min=0 | sec=14
T=190000 | running=1 | min=0 | sec=15
T=200000 | running=1 | min=0 | sec=16
T=210000 | running=1 | min=0 | sec=17
T=220000 | running=1 | min=0 | sec=18
T=230000 | running=1 | min=0 | sec=19
T=240000 | running=1 | min=0 | sec=20
T=250000 | running=1 | min=0 | sec=21
T=260000 | running=1 | min=0 | sec=22
T=270000 | running=1 | min=0 | sec=23
T=280000 | running=1 | min=0 | sec=24
T=290000 | running=1 | min=0 | sec=25
T=300000 | running=1 | min=0 | sec=26
T=310000 | running=1 | min=0 | sec=27
T=320000 | running=1 | min=0 | sec=28
T=330000 | running=1 | min=0 | sec=29
T=340000 | running=1 | min=0 | sec=30
T=350000 | running=1 | min=0 | sec=31
T=360000 | running=1 | min=0 | sec=32
T=370000 | running=1 | min=0 | sec=33
T=380000 | running=1 | min=0 | sec=34
T=390000 | running=1 | min=0 | sec=35
T=400000 | running=1 | min=0 | sec=36
T=410000 | running=1 | min=0 | sec=37
T=420000 | running=1 | min=0 | sec=38
T=430000 | running=1 | min=0 | sec=39
T=440000 | running=1 | min=0 | sec=40
T=450000 | running=1 | min=0 | sec=41
T=460000 | running=1 | min=0 | sec=42
T=470000 | running=1 | min=0 | sec=43
T=480000 | running=1 | min=0 | sec=44
T=490000 | running=1 | min=0 | sec=45
T=500000 | running=1 | min=0 | sec=46
T=510000 | running=1 | min=0 | sec=47
T=520000 | running=1 | min=0 | sec=48
```

```
T=480000 | running=1 | min=0 | sec=44
T=490000 | running=1 | min=0 | sec=45
T=500000 | running=1 | min=0 | sec=46
T=510000 | running=1 | min=0 | sec=47
T=520000 | running=1 | min=0 | sec=48
T=530000 | running=1 | min=0 | sec=49
T=540000 | running=1 | min=0 | sec=50
T=550000 | running=1 | min=0 | sec=51
T=560000 | running=1 | min=0 | sec=52
T=570000 | running=1 | min=0 | sec=53
T=580000 | running=1 | min=0 | sec=54
T=590000 | running=1 | min=0 | sec=55
T=600000 | running=1 | min=0 | sec=56
T=610000 | running=1 | min=0 | sec=57
T=620000 | running=1 | min=0 | sec=58
T=630000 | running=1 | min=0 | sec=59
T=640000 | running=1 | min=1 | sec=0
T=650000 | running=0 | min=1 | sec=1
T=660000 | running=1 | min=1 | sec=1
T=670000 | running=1 | min=1 | sec=2
T=680000 | running=1 | min=1 | sec=3
T=690000 | running=1 | min=1 | sec=4
T=700000 | running=1 | min=1 | sec=5
T=710000 | running=1 | min=1 | sec=6
T=720000 | running=1 | min=1 | sec=7
T=730000 | running=1 | min=1 | sec=8
T=740000 | running=1 | min=1 | sec=9
T=750000 | running=1 | min=1 | sec=10
T=760000 | running=1 | min=1 | sec=11
T=770000 | running=1 | min=1 | sec=12
T=780000 | running=1 | min=1 | sec=13
T=790000 | running=1 | min=1 | sec=14
T=800000 | running=1 | min=1 | sec=15
T=810000 | running=1 | min=1 | sec=16
T=820000 | running=1 | min=1 | sec=17
T=830000 | running=1 | min=1 | sec=18
T=840000 | running=1 | min=1 | sec=19
T=850000 | running=1 | min=1 | sec=20
T=860000 | running=1 | min=1 | sec=21
T=870000 | running=1 | min=1 | sec=22
T=880000 | running=1 | min=1 | sec=23
T=890000 | running=1 | min=1 | sec=24
T=900000 | running=1 | min=1 | sec=25
T=910000 | running=1 | min=1 | sec=26
T=920000 | running=1 | min=1 | sec=27
T=930000 | running=1 | min=1 | sec=28
T=940000 | running=1 | min=1 | sec=29
T=950000 | running=1 | min=1 | sec=30
T=960000 | running=1 | min=1 | sec=31
T=970000 | running=1 | min=1 | sec=32
T=980000 | running=1 | min=1 | sec=33
T=990000 | running=1 | min=1 | sec=34
T=1000000 | running=1 | min=1 | sec=35
T=1010000 | running=1 | min=1 | sec=36
T=1020000 | running=1 | min=1 | sec=37
T=1030000 | running=1 | min=1 | sec=38
T=1040000 | running=1 | min=1 | sec=39
T=1050000 | running=1 | min=1 | sec=40
T=1060000 | running=1 | min=1 | sec=41
T=1070000 | running=0 | min=0 | sec=0
tb_stopwatch.v45: finish called at 1290000 (1ps)
ibrahimfadu /C:/s.mini/0000 P main 21:16
```

GTKWAVE

