**CSE 315 DIGITAL LOGIC DESIGN TERM PROJECT**

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1. Instruction Set

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | OPCODES | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AND | 0 | 0 | 0 | DST REG | | | | SRC1 REG | | | | 0 | 0 | 0 | SRC2 Reg | | | |
| ANDI | 0 | 0 | 0 | 1 | Immediate value | | | | | |
| OR | 0 | 0 | 1 | DST REG | | | | SRC1 REG | | | | 0 | 0 | 0 | SRC2 Reg | | | |
| ORI | 0 | 0 | 1 | 1 | Immediate value | | | | | |
| ADD | 0 | 1 | 0 | DST REG | | | | SRC1 REG | | | | 0 | 0 | 0 | SRC2 Reg | | | |
| ADDI | 0 | 1 | 0 | 1 | Immediate value | | | | | |
| XOR | 0 | 1 | 1 | DST REG | | | | SRC1 REG | | | | 0 | 0 | 0 | SRC2 Reg | | | |
| XORI | 0 | 1 | 1 | 1 | Immediate value | | | | | |
| LD | 1 | 0 | 0 | DST REG | | | | ADRESS 11 | | | | | | | | | | |
| STR | 1 | 0 | 1 | ADRESS 11 | | | | | | | | | | | DST REG | | | |
| JUMP | 1 | 1 | 0 | ADRESS 15 | | | | | | | | | | | | | | |
| BEQ | 1 | 1 | 1 | 0 | 1 | 0 | OP1 | | | | OP2 | | | | ADRESS 4 | | | |
| BGT | 1 | 1 | 1 | 0 | 0 | 1 | OP1 | | | | OP2 | | | | ADRESS 4 | | | |
| BLT | 1 | 1 | 1 | 1 | 0 | 0 | OP1 | | | | OP2 | | | | ADRESS 4 | | | |
| BGE | 1 | 1 | 1 | 0 | 1 | 1 | OP1 | | | | OP2 | | | | ADRESS 4 | | | |
| BLE | 1 | 1 | 1 | 1 | 1 | 0 | OP1 | | | | OP2 | | | | ADRESS 4 | | | |
|  |  |  |  | n | z | p |  |  |  |  |  |  |  |  |  |  |  |  |

2. Datapath

A. Program Counter

Program Counter holds a 18-bit value inside it. This value shows which address of the Instruction Memory should be read. If “PCWrite” signal is enabled, it loads the register with the data in “PCinDATA” in next clock rising edge. If “brachoper” enabled which is 17th16th15th bits f the given instruction. The mux befor the pc mux set to 1 and it allows to pass branch address given in the last four bit of the instructure. İf pc mux not set to 1 it allows to pass jump adress which is given in the instruction. Then If “JUMP” signal is not enabled, it increments by 1 in next clock rising edge.

B. Instruction Memory

Instruction Memory is a “18-bit data width, 18-bit address width” memory where only the instructions are stored.

C. Data Memory

Data Memory is a “18-bit data width, 10-bit address width” memory where the data resides. If “memStore” signal is supplied, it stores the value read from specified register adress.

D. ALU

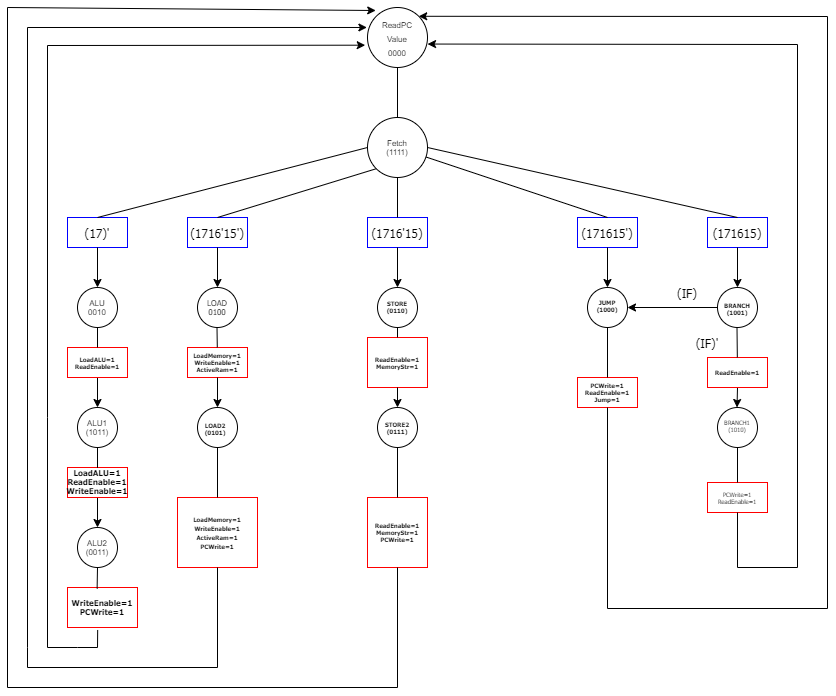
ALU is a component that performs the operations “ADD”, “AND”, “OR” and “XOR”. If “selectoper” is 10, it adds its inputs and ready for the writing specified register in the register file .If “selectoper” is 00, it “AND” it ‘Ands’ its inputs and ready for the writing specified register in the register file. If “selectoper” is 11, make ‘XOR’ operation with its inputs and ready for the writing specified register in the register file. If “selectoper” is 01, it “OR” it make ‘OR’ operation with its inputs and ready for the writing specified register in the register file.

E. Register File

Register file contains 16 18-bit registers. If “writeEnable” signal is supplied, it writes the data in the register with the address specified in “writeAdress”. If “ReadEnable” signal is supplied, it reads the data in the register with the address specified in “ReadAdress1” and “ReadAdress2”. Then it sends the read value from specified adresses to “ReadData1” and “ReadData2”. These outputs connected to the ALU and Comparator inputs. Alu’s mux’s select bit is get from 17th bit of the instructure.the other mux’s select bit gets from the “Branch or Jump” signal.

3.Control Unit

A.Control Unit Finite State Machine



B.Control Unit Truth Table

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **S0** | **S1** | **S2** | **S3** | **17** | **16** | **15** | **if** | **n0** | **n1** | **n2** | **n3** | **LoadALU** | **Read Enable** | **Write**  **Enable** | **Load**  **Memory** | **Memory Str** | **PC write** | **Jump** |  | **Active**  **Ram** |
| 0 | 0 | 0 | 0 | X | X | X | X | 0 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 | 0 | X | X | X | 0 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 | 1 | 0 | X | X | 0 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | X | 0 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | X | 1 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | X | 1 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 1 | 0 | X | X | X | X | 1 | 0 | 1 | 1 | 1 | 1 |  |  |  |  |  |  |  |
| 0 | 0 | 1 | 1 | X | X | X | X | 0 | 0 | 0 | 0 |  |  | 1 |  |  | 1 |  |  |  |
| 0 | 1 | 0 | 0 | X | X | X | X | 0 | 1 | 0 | 1 |  |  | 1 | 1 |  |  |  |  | 1 |
| 0 | 1 | 0 | 1 | X | X | X | X | 0 | 0 | 0 | 0 |  |  | 1 | 1 |  | 1 |  |  | 1 |
| 0 | 1 | 1 | 0 | X | X | X | X | 0 | 1 | 1 | 1 |  | 1 |  |  | 1 |  |  |  | 1 |
| 0 | 1 | 1 | 1 | X | X | X | X | 0 | 0 | 0 | 0 |  | 1 |  |  | 1 | 1 |  |  | 1 |
| 1 | 0 | 0 | 0 | X | X | X | X | 0 | 0 | 0 | 0 |  | 1 |  |  |  | 1 | 1 |  |  |
| 1 | 0 | 0 | 1 | X | X | X | 1 | 1 | 0 | 0 | 0 |  | 1 |  |  |  |  |  |  |  |
| 1 | 0 | 0 | 1 | X | X | X | 0 | 1 | 0 | 1 | 0 |  | 1 |  |  |  |  |  |  |  |
| 1 | 0 | 1 | 0 | X | X | X | X | 0 | 0 | 0 | 0 |  | 1 |  |  |  | 1 |  |  |  |
| 1 | 0 | 1 | 1 | X | X | X | X | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  |  |  |  |  |  |