Pipelined ARM Processor

Computer Architecture (CIE 439)

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System verilog modules used:

- ALU.sv
- ARM.sv
- CondCheck.sv
- Controller.sv
- DataPath.sv
- Dmem.sv
- Eqcmp.sv
- Flopenr.sv
- Extend.sv
- Flopenrc.sv
- Floprc.sv
- Hazard.sv
- Imem.sv
- Regfile.sv
- Testbench.sv
- Top.sv
- Mux2.sv
- Mux3.sv

Testbench

ADDR	PROGRAM	; COMMENTS	HEX CODE
00	MAIN SUB R0, R15, R15	; R0 = 0	E04F000F
04	ADD R2, R0, #5	; R2 = 5	E2802005
08	ADD R3, R0, #12	; R3 = 12	E280300C
0C	SUB R7, R3, #9	; R7 = 3	E2437009
10	ORR R4, R7, R2	; R4 = 3 OR 5 = 7	E1874002
14	AND R5, R3, R4	; R5 = 12 AND 7 = 4	E0035004

Testbench

```
18    ADD R5, R5, R4       ; R5 = 4 + 7 = 11             E0855004


1C    SUBS R8, R7, R2      ; R8=3-5=-2,set Flags         E0578002

20    ADDLT R7, R5, #1     ; R7 = 11 + 1 = 12            B2857001

24    SUB R7, R7, R2       ; R7 = 12 - 5 = 7             E0477002

28    STR R7, [R3, #84]    ; mem[12+84] = 7              E5837054

2C    LDR R2, [R0, #96]    ; R2 = mem[96] = 7            E5902060

30    ADD R12, R2, #114    ; R12 = 114 + 7 = 121         E282C072
```

Testbench

```
34        BIC R3, R12, R7       ; R3 = 121 & ~ 7 = 120   E1CC3007
38        EOR R5, R3, R12       ; R5 = 120 ^ 121 = 1     E023500C
```

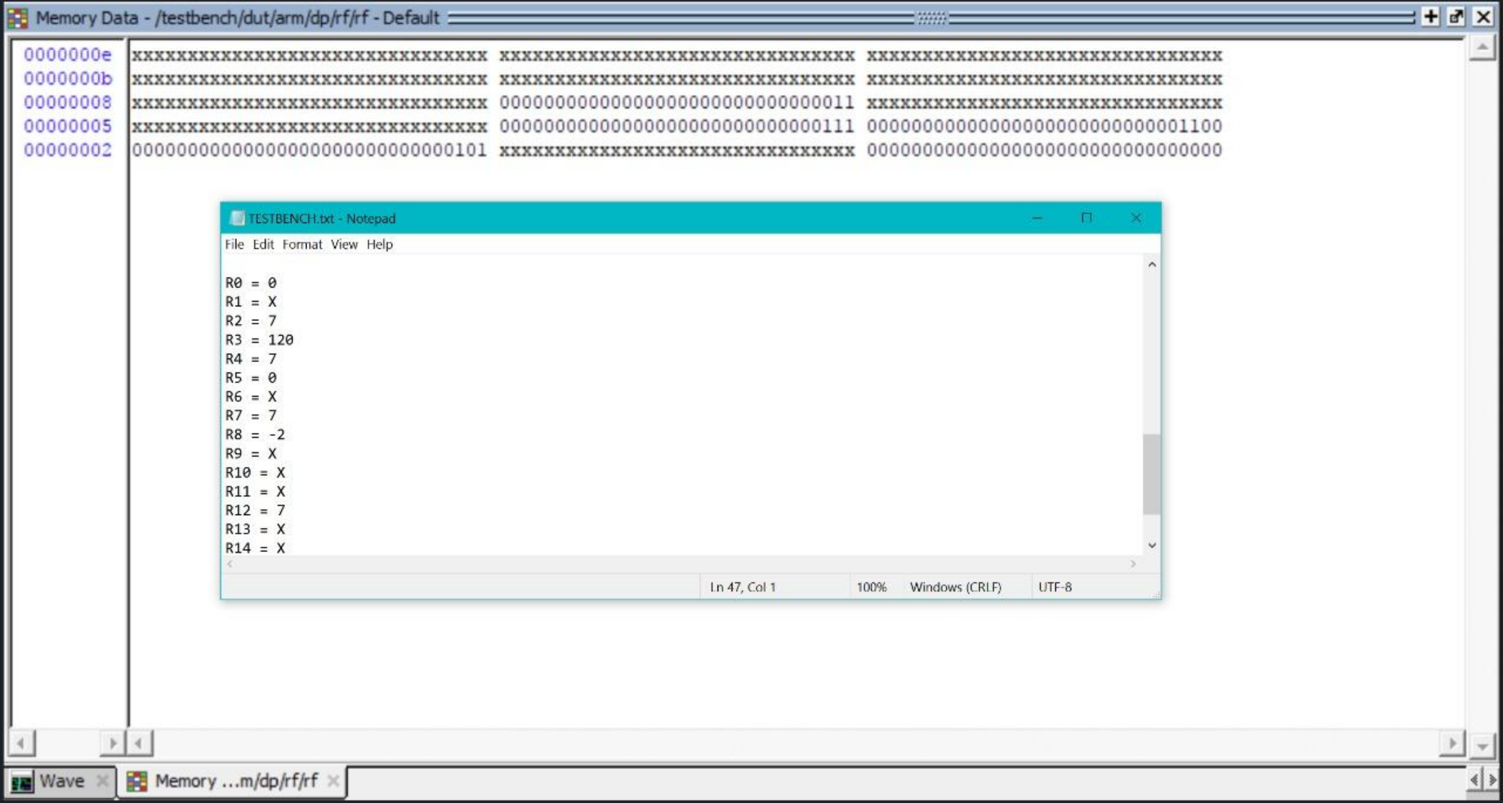
PCWRITE:

```
3C        ADD R15, R15, #0                     E28FF000
40        ADD R4 , R0, R0                      E2898005
44        ADD R5 , R0, R0                      E0805000
48        ADD R12 , R4, R5                     E084C005
```

Testbench

```
4C        B END                ; always taken       EA000001
50        ADD R2, R0, #13      ; shouldn't happen   E280200D
54        ADD R2, R0, #10      ; shouldn't happen   E280200A
58    END STR R2, [R0, #100]   ; mem[100] = 7       E5802064
```

RegFile after running the test bench

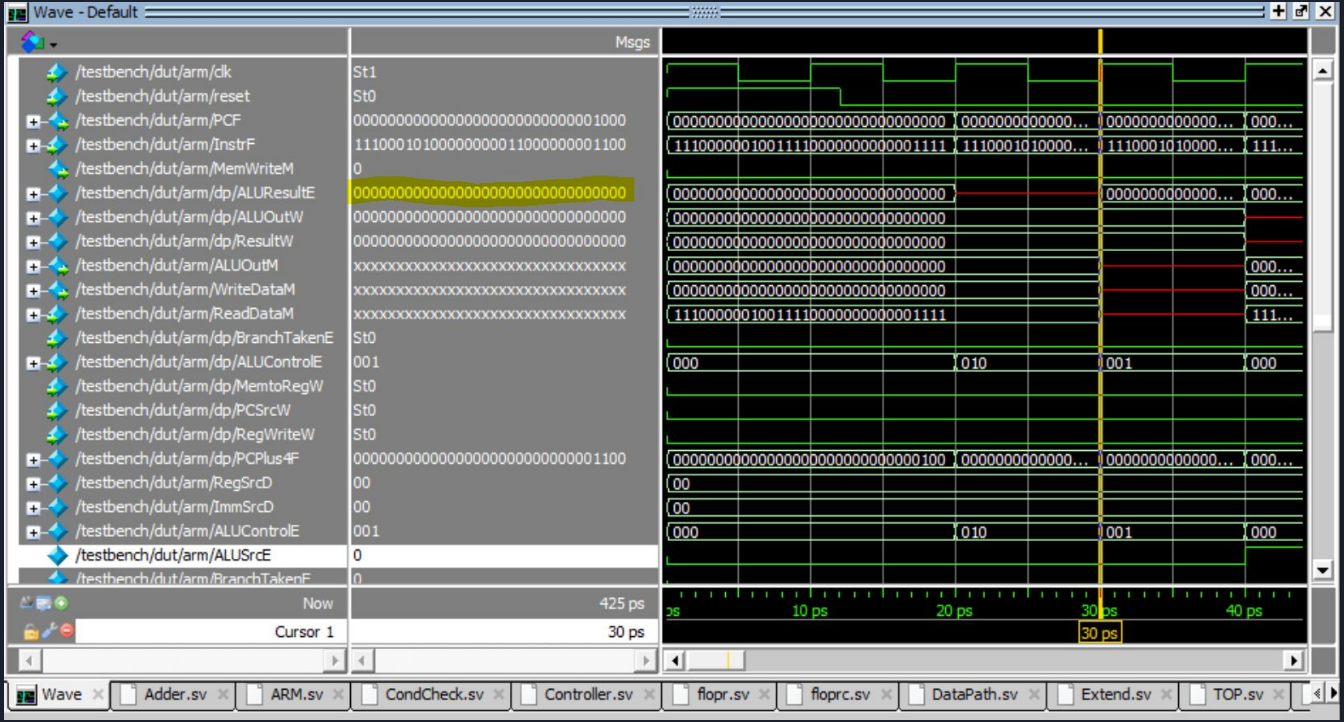


```
0000000e xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0000000b xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000008 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx 00000000000000000000000000000011 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000005 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx 00000000000000000000000000000111 00000000000000000000000000001100
00000002 00000000000000000000000000000101 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx 00000000000000000000000000000000
```

```
R0 = 0
R1 = X
R2 = 7
R3 = 120
R4 = 7
R5 = 0
R6 = X
R7 = 7
R8 = -2
R9 = X
R10 = X
R11 = X
R12 = 7
R13 = X
R14 = X
```

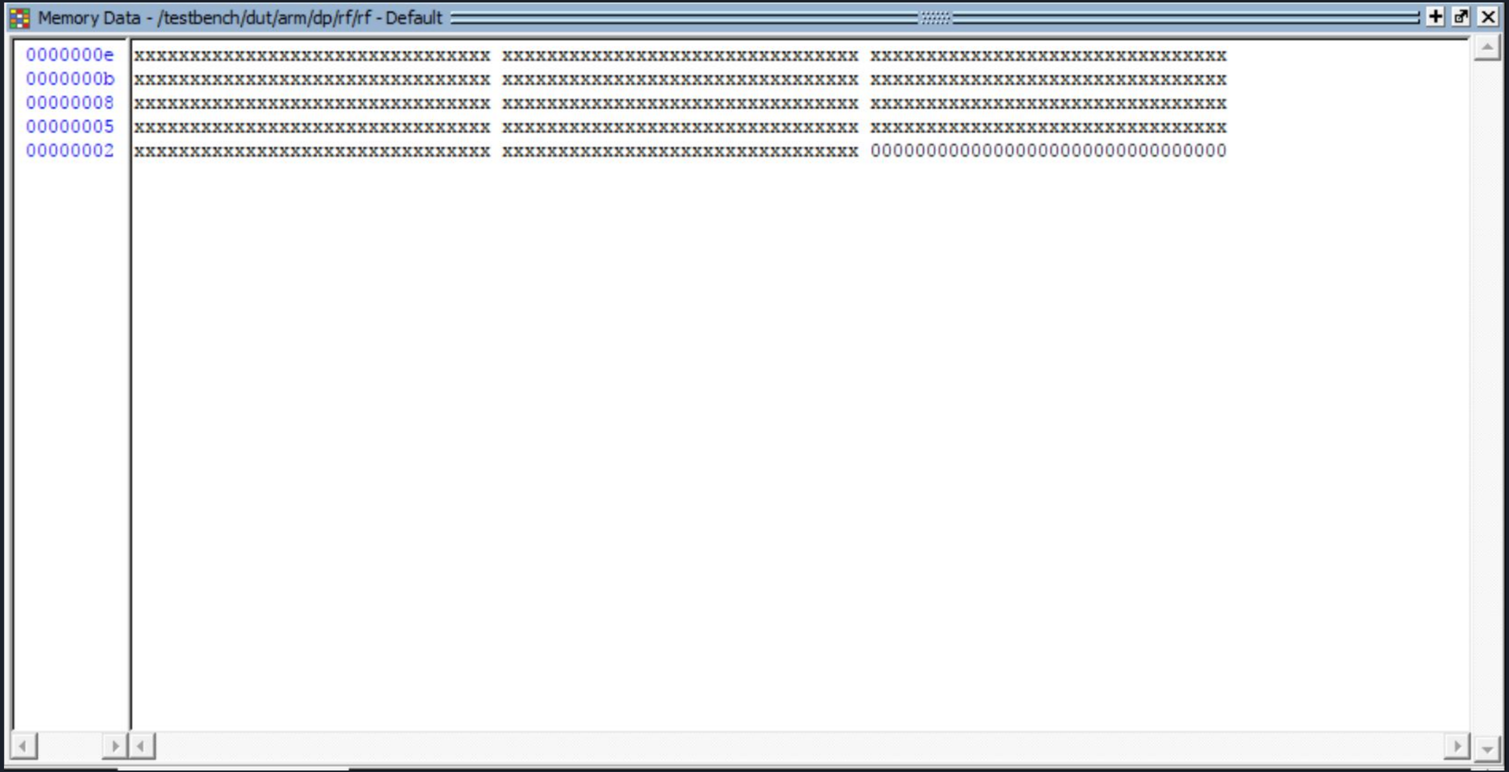
Simulation results

SUB R0, R15, R15   ; R0 = 0



```
                                       Msgs
/testbench/dut/arm/clk                 St1
/testbench/dut/arm/reset               St0
/testbench/dut/arm/PCF                 00000000000000000000000000001000
/testbench/dut/arm/InstrF              11100010100000000011000000001100
/testbench/dut/arm/MemWriteM           0
/testbench/dut/arm/dp/ALUResultE       00000000000000000000000000000000
/testbench/dut/arm/dp/ALUOutW          00000000000000000000000000000000
/testbench/dut/arm/dp/ResultW          00000000000000000000000000000000
/testbench/dut/arm/ALUOutM             xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
/testbench/dut/arm/WriteDataM          xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
/testbench/dut/arm/ReadDataM           xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
/testbench/dut/arm/dp/BranchTakenE     St0
/testbench/dut/arm/dp/ALUControlE      001
/testbench/dut/arm/dp/MemtoRegW        St0
/testbench/dut/arm/dp/PCSrcW           St0
/testbench/dut/arm/dp/RegWriteW        St0
/testbench/dut/arm/dp/PCPlus4F         00000000000000000000000000001100
/testbench/dut/arm/RegSrcD             00
/testbench/dut/arm/ImmSrcD             00
/testbench/dut/arm/ALUControlE         001
/testbench/dut/arm/ALUSrcE             0
/testbench/dut/arm/BranchTakenE        0
Now                                    425 ps
Cursor 1                               30 ps
```

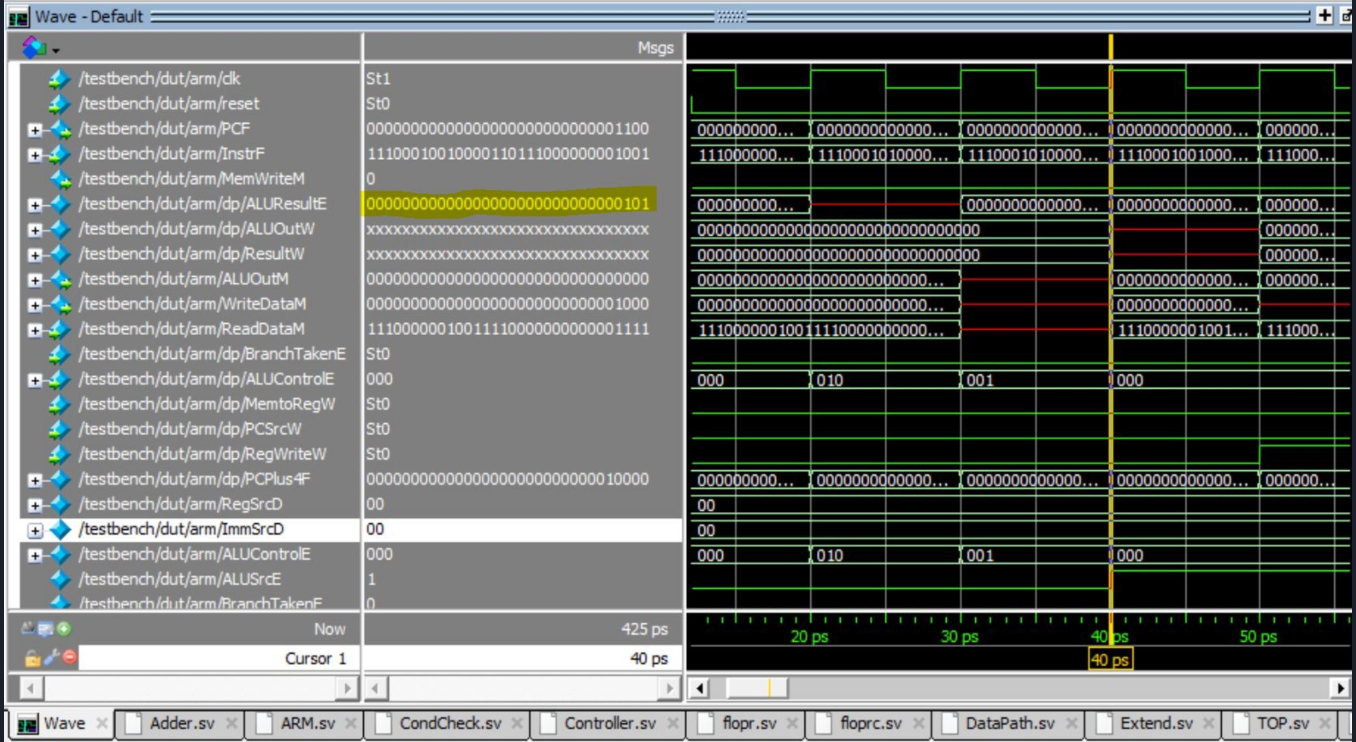
Register file at fifth cycle



Memory Data - /testbench/dut/arm/dp/rf/rf - Default

```
0000000e xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0000000b xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000008 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000005 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000002 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx 00000000000000000000000000000000
```

ADD R2, R0, #5   ; R2 = 5

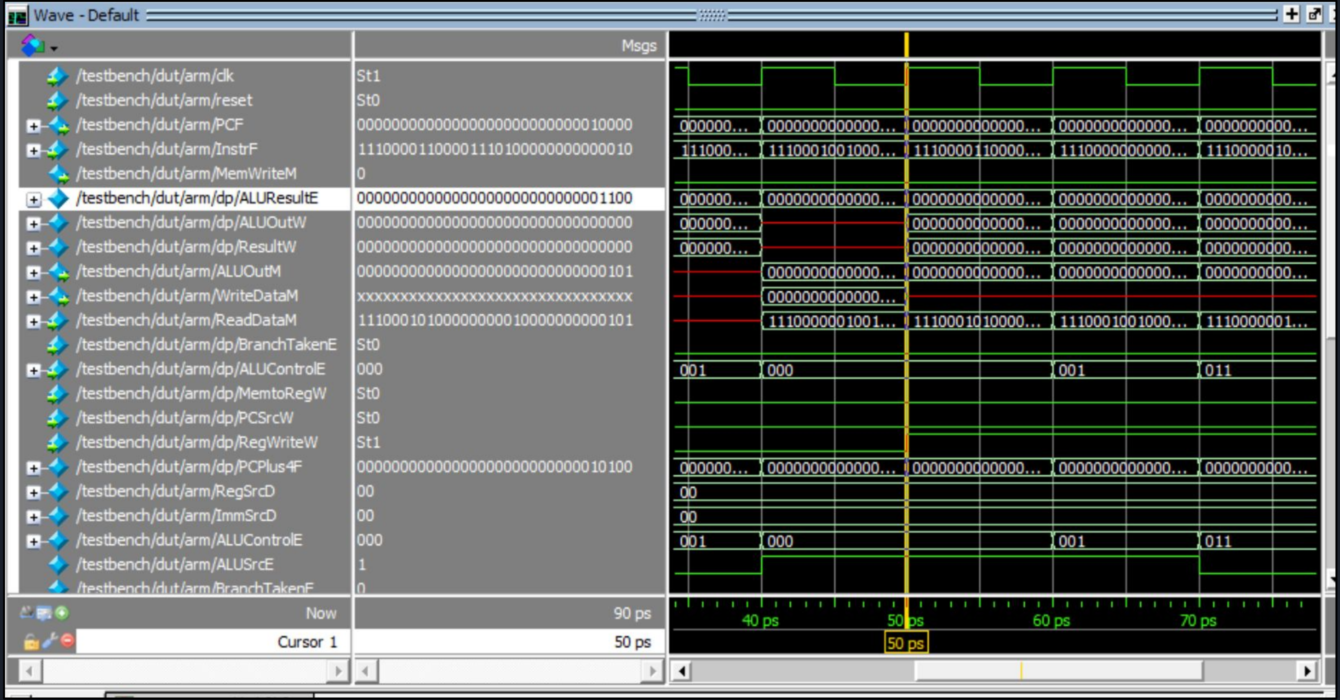


Wave - Default

```
                                        Msgs
/testbench/dut/arm/clk                  St1
/testbench/dut/arm/reset                St0
/testbench/dut/arm/PCF                  00000000000000000000000000001100
/testbench/dut/arm/InstrF               11100010010000110111000000001001
/testbench/dut/arm/MemWriteM            0
/testbench/dut/arm/dp/ALUResultE        00000000000000000000000000000101
/testbench/dut/arm/dp/ALUOutW           xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
/testbench/dut/arm/dp/ResultW           xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
/testbench/dut/arm/ALUOutM              00000000000000000000000000000000
/testbench/dut/arm/WriteDataM           00000000000000000000000000001000
/testbench/dut/arm/ReadDataM            11100000010011110000000000001111
/testbench/dut/arm/dp/BranchTakenE      St0
/testbench/dut/arm/dp/ALUControlE       000
/testbench/dut/arm/dp/MemtoRegW         St0
/testbench/dut/arm/dp/PCSrcW            St0
/testbench/dut/arm/dp/RegWriteW         St0
/testbench/dut/arm/dp/PCPlus4F          00000000000000000000000000010000
/testbench/dut/arm/RegSrcD              00
/testbench/dut/arm/ImmSrcD              00
/testbench/dut/arm/ALUControlE          000
/testbench/dut/arm/ALUSrcE              1
/testbench/dut/arm/BranchTakenE         0

Now                                     425 ps
Cursor 1                                40 ps
```

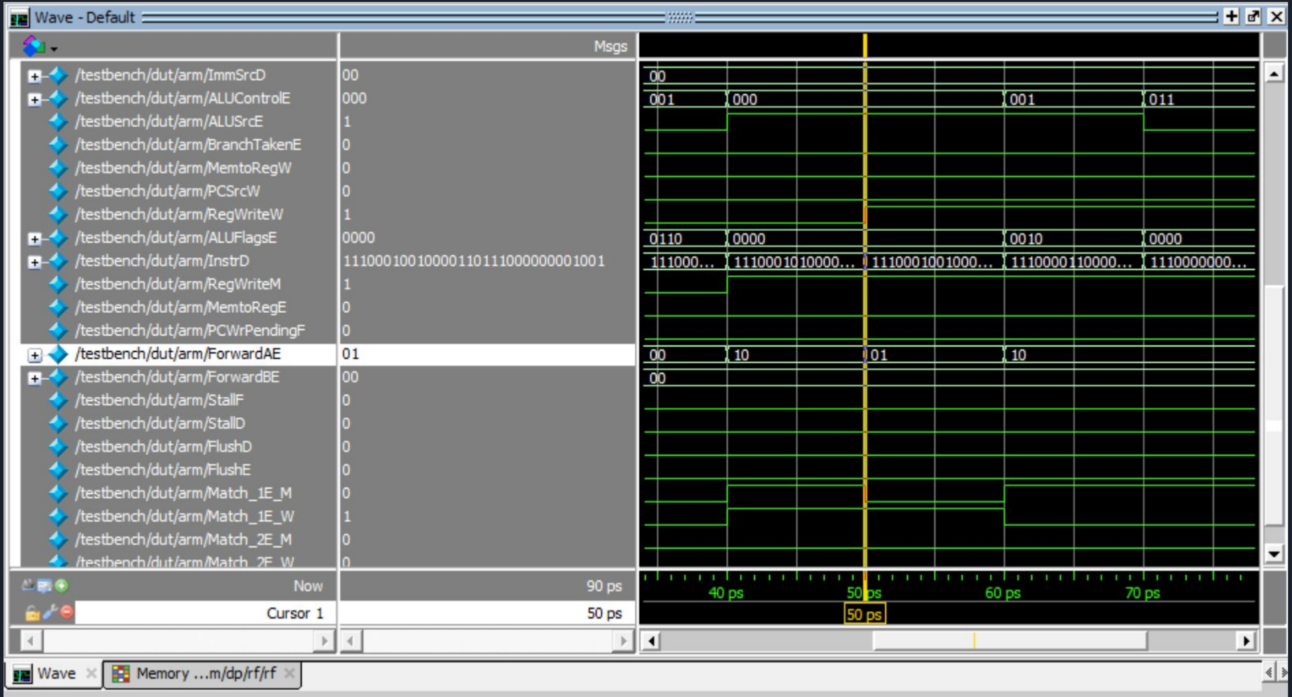
ADD R3, R0, #12 ; R3 = 12



Wave - Default

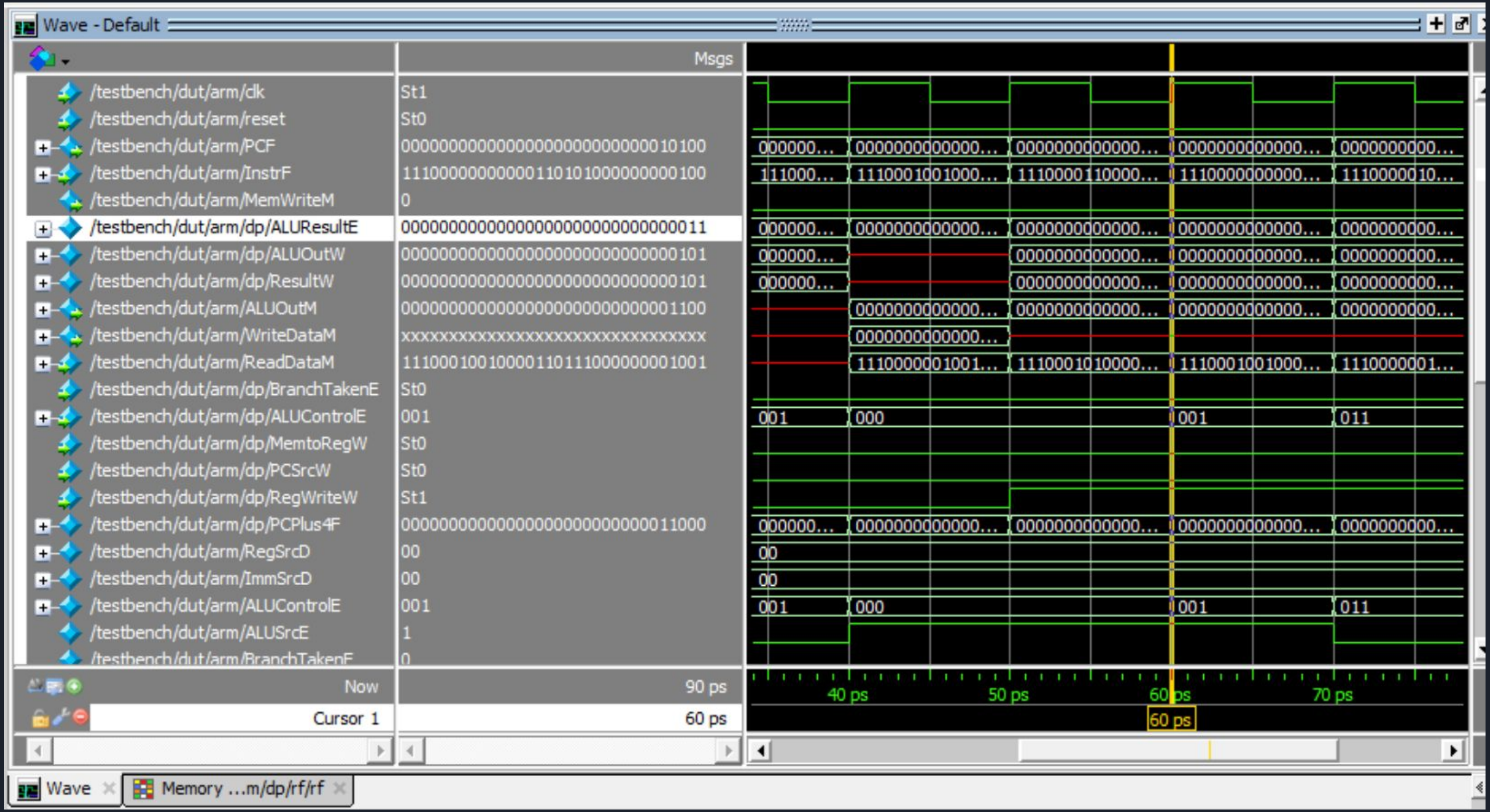
	Msgs
/testbench/dut/arm/clk	St1
/testbench/dut/arm/reset	St0
/testbench/dut/arm/PCF	00000000000000000000000000010000
/testbench/dut/arm/InstrF	11100001100000111010000000000010
/testbench/dut/arm/MemWriteM	0
/testbench/dut/arm/dp/ALUResultE	00000000000000000000000000001100
/testbench/dut/arm/dp/ALUOutW	00000000000000000000000000000000
/testbench/dut/arm/dp/ResultW	00000000000000000000000000000000
/testbench/dut/arm/ALUOutM	00000000000000000000000000000101
/testbench/dut/arm/WriteDataM	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
/testbench/dut/arm/ReadDataM	11100010100000000010000000000101
/testbench/dut/arm/dp/BranchTakenE	St0
/testbench/dut/arm/dp/ALUControlE	000
/testbench/dut/arm/dp/MemtoRegW	St0
/testbench/dut/arm/dp/PCSrcW	St0
/testbench/dut/arm/dp/RegWriteW	St1
/testbench/dut/arm/dp/PCPlus4F	00000000000000000000000000010100
/testbench/dut/arm/RegSrcD	00
/testbench/dut/arm/ImmSrcD	00
/testbench/dut/arm/ALUControlE	000
/testbench/dut/arm/ALUSrcE	1
/testbench/dut/arm/BranchTakenE	0
Now	90 ps
Cursor 1	50 ps

SUB R7, R3, #9 ; R7 = 3 **(Data dependency: solved by data forwarding)**



Wave - Default

	Msgs
/testbench/dut/arm/ImmSrcD	00
/testbench/dut/arm/ALUControlE	000
/testbench/dut/arm/ALUSrcE	1
/testbench/dut/arm/BranchTakenE	0
/testbench/dut/arm/MemtoRegW	0
/testbench/dut/arm/PCSrcW	0
/testbench/dut/arm/RegWriteW	1
/testbench/dut/arm/ALUFlagsE	0000
/testbench/dut/arm/InstrD	11100010010000110111000000001001
/testbench/dut/arm/RegWriteM	1
/testbench/dut/arm/MemtoRegE	0
/testbench/dut/arm/PCWrPendingF	0
/testbench/dut/arm/ForwardAE	01
/testbench/dut/arm/ForwardBE	00
/testbench/dut/arm/StallF	0
/testbench/dut/arm/StallD	0
/testbench/dut/arm/FlushD	0
/testbench/dut/arm/FlushE	0
/testbench/dut/arm/Match_1E_M	0
/testbench/dut/arm/Match_1E_W	1
/testbench/dut/arm/Match_2E_M	0
/testbench/dut/arm/Match_2E_W	0
Now	90 ps
Cursor 1	50 ps

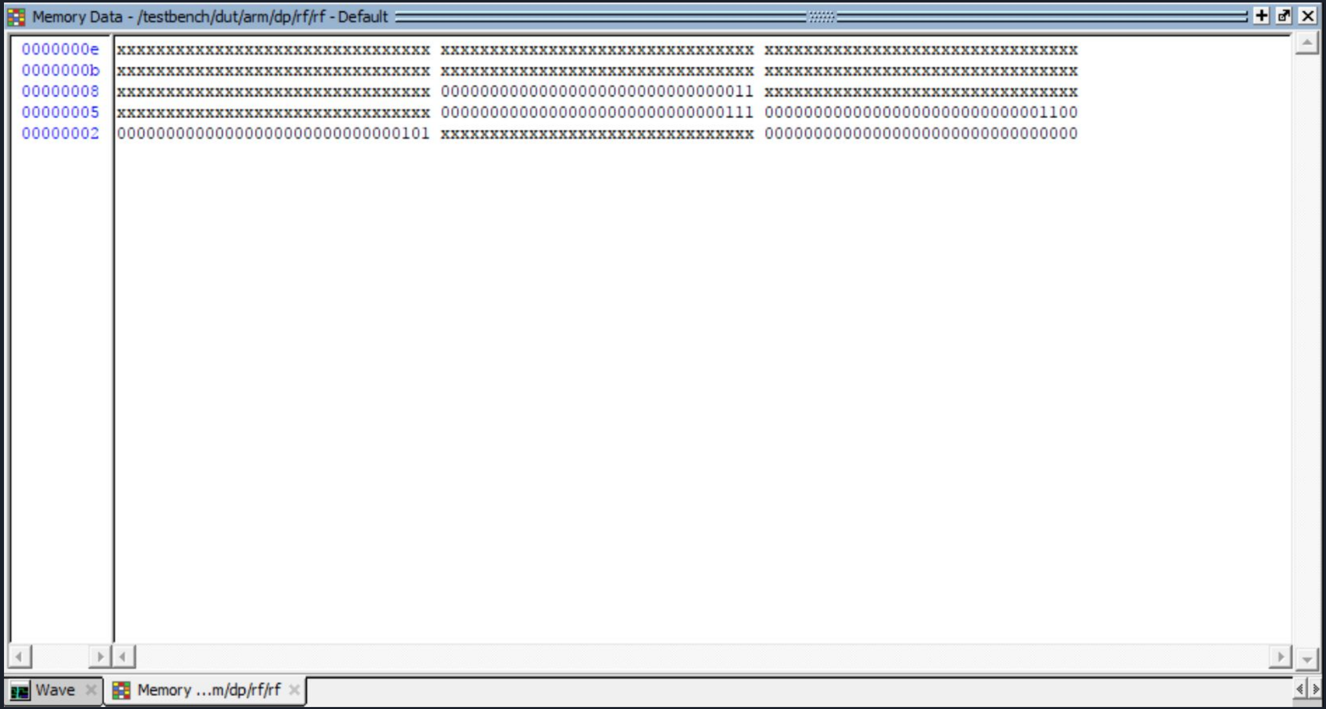


Wave - Default

```
                                             Msgs
/testbench/dut/arm/clk                       St1
/testbench/dut/arm/reset                     St0
/testbench/dut/arm/PCF                       00000000000000000000000000010100
/testbench/dut/arm/InstrF                    11100000000000110101000000000100
/testbench/dut/arm/MemWriteM                 0
/testbench/dut/arm/dp/ALUResultE             00000000000000000000000000000011
/testbench/dut/arm/dp/ALUOutW                00000000000000000000000000000101
/testbench/dut/arm/dp/ResultW                00000000000000000000000000000101
/testbench/dut/arm/ALUOutM                   00000000000000000000000000001100
/testbench/dut/arm/WriteDataM                xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
/testbench/dut/arm/ReadDataM                 11100010010000110111000000001001
/testbench/dut/arm/dp/BranchTakenE           St0
/testbench/dut/arm/dp/ALUControlE            001
/testbench/dut/arm/dp/MemtoRegW              St0
/testbench/dut/arm/dp/PCSrcW                 St0
/testbench/dut/arm/dp/RegWriteW              St1
/testbench/dut/arm/dp/PCPlus4F               00000000000000000000000000011000
/testbench/dut/arm/RegSrcD                   00
/testbench/dut/arm/ImmSrcD                   00
/testbench/dut/arm/ALUControlE               001
/testbench/dut/arm/ALUSrcE                   1
/testbench/dut/arm/BranchTakenE              0

Now                                          90 ps
Cursor 1                                     60 ps
```

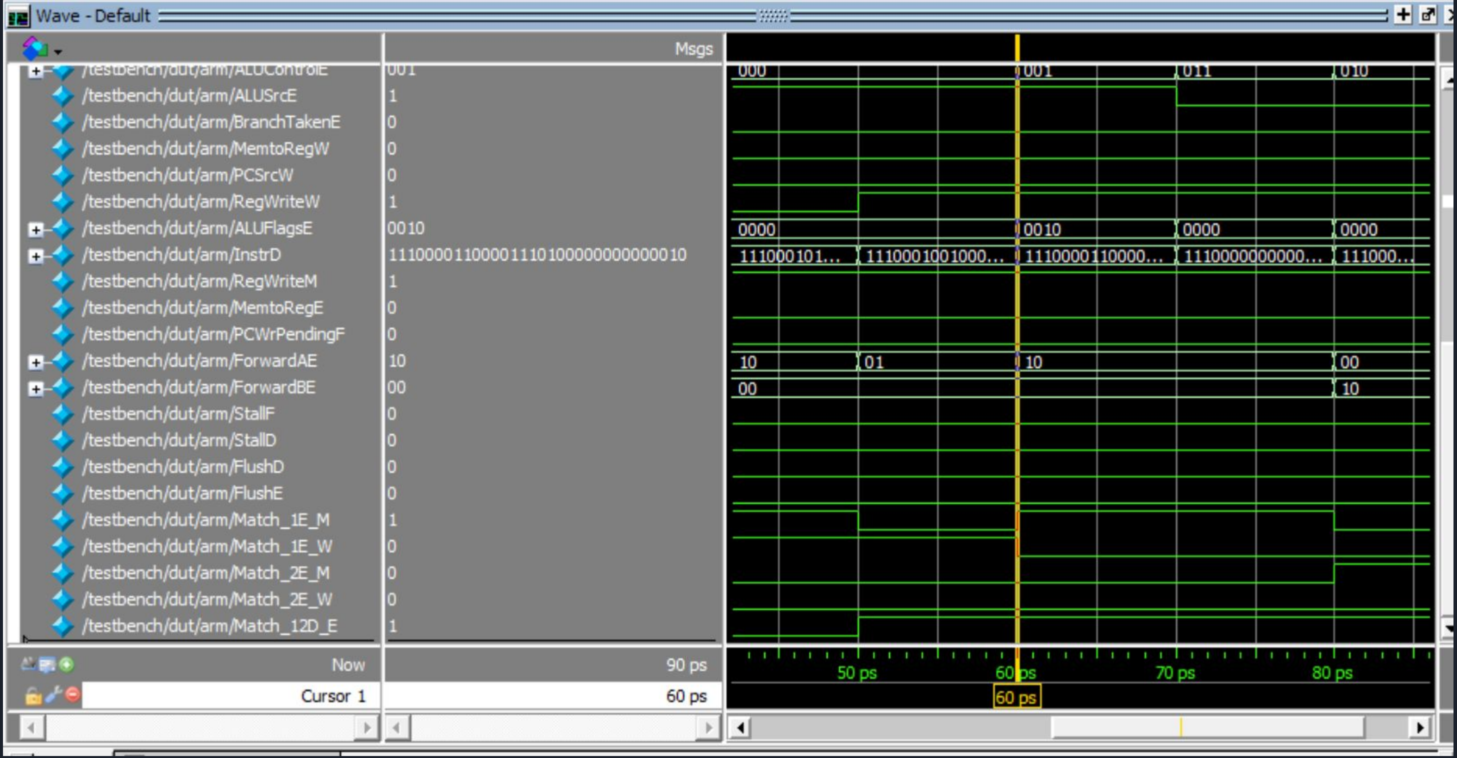
AND R5, R3, R4 ; R5 = 12 AND 7 = 4 E0035004



Memory Data - /testbench/dut/arm/dp/rf/rf - Default

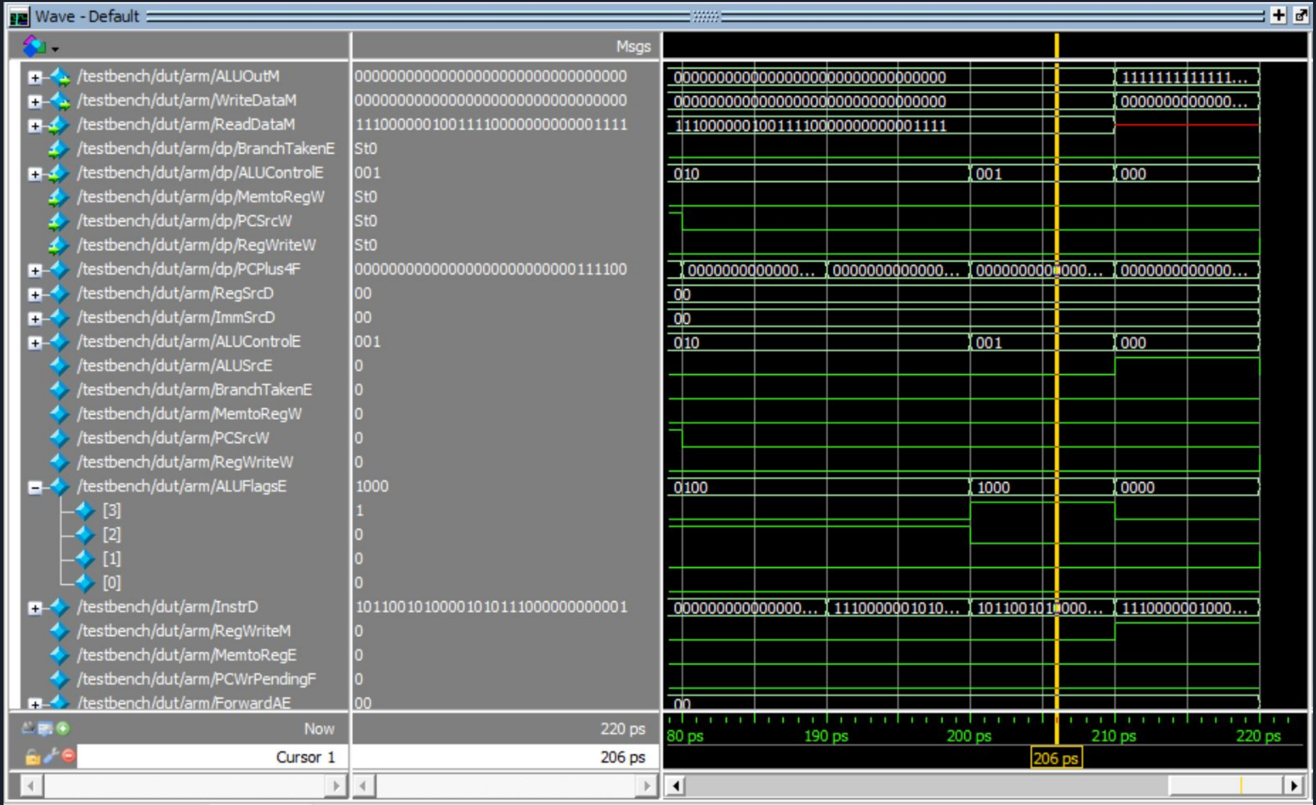
```
0000000e xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
0000000b xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000008 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx 00000000000000000000000000000011 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
00000005 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx 00000000000000000000000000000111 00000000000000000000000000001100
00000002 00000000000000000000000000000101 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx 00000000000000000000000000000000
```

ADD R5, R5, R4 ; R5 = 4 + 7 = 11 E0855004 (Data forwarding)



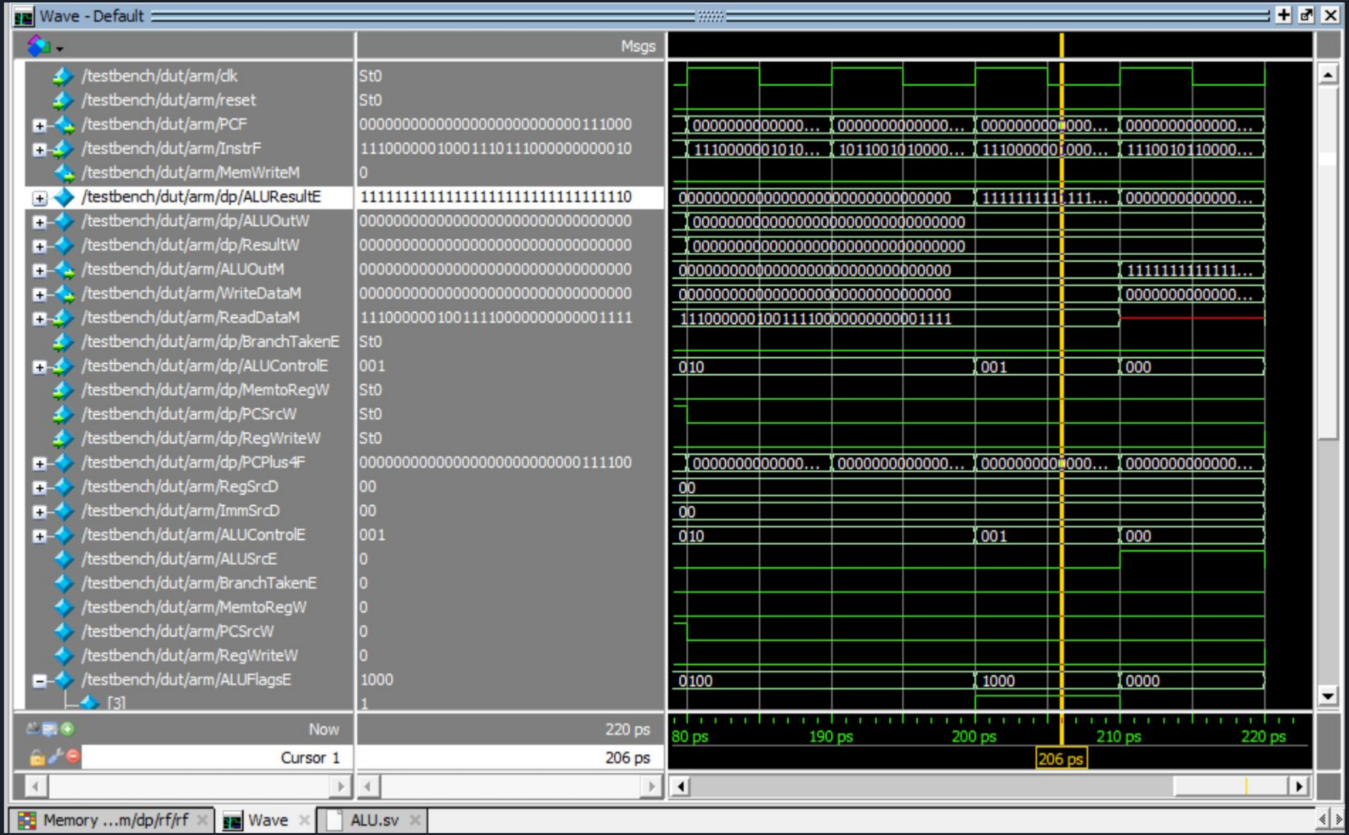
	Msgs
/testbench/dut/arm/ALUControlE	001
/testbench/dut/arm/ALUSrcE	1
/testbench/dut/arm/BranchTakenE	0
/testbench/dut/arm/MemtoRegW	0
/testbench/dut/arm/PCSrcW	0
/testbench/dut/arm/RegWriteW	1
/testbench/dut/arm/ALUFlagsE	0010
/testbench/dut/arm/InstrD	11100001100001110100000000000010
/testbench/dut/arm/RegWriteM	1
/testbench/dut/arm/MemtoRegE	0
/testbench/dut/arm/PCWrPendingF	0
/testbench/dut/arm/ForwardAE	10
/testbench/dut/arm/ForwardBE	00
/testbench/dut/arm/StallF	0
/testbench/dut/arm/StallD	0
/testbench/dut/arm/FlushD	0
/testbench/dut/arm/FlushE	0
/testbench/dut/arm/Match_1E_M	1
/testbench/dut/arm/Match_1E_W	0
/testbench/dut/arm/Match_2E_M	0
/testbench/dut/arm/Match_2E_W	0
/testbench/dut/arm/Match_12D_E	1
Now	90 ps
Cursor 1	60 ps

SUBS R8, R7, R2 ; R8=3-5=-2,set Flags E0578002 (n flag = 1)



Wave - Default

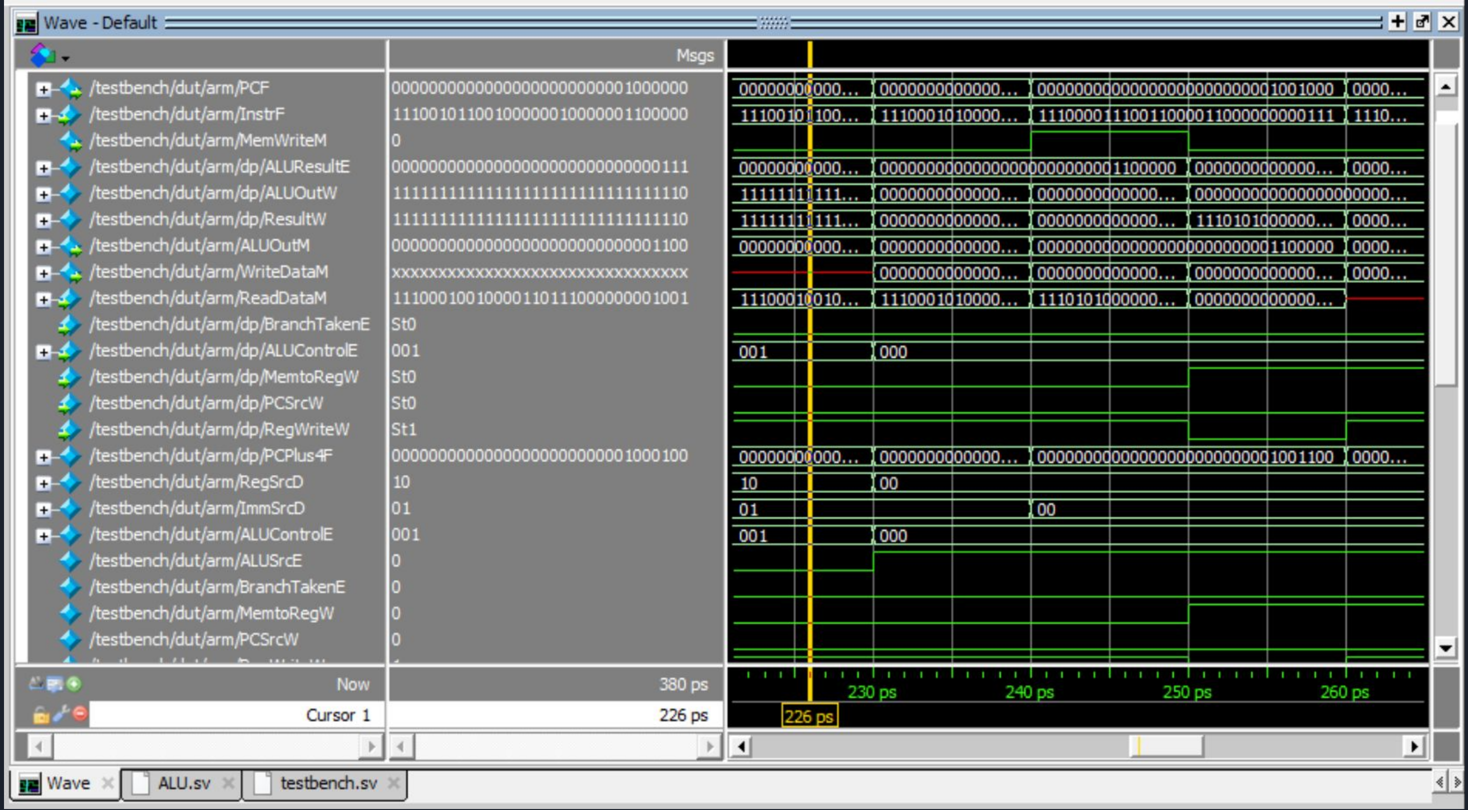
	Msgs
/testbench/dut/arm/ALUOutM	00000000000000000000000000000000
/testbench/dut/arm/WriteDataM	00000000000000000000000000000000
/testbench/dut/arm/ReadDataM	11100000010011110000000000001111
/testbench/dut/arm/dp/BranchTakenE	St0
/testbench/dut/arm/dp/ALUControlE	001
/testbench/dut/arm/dp/MemtoRegW	St0
/testbench/dut/arm/dp/PCSrcW	St0
/testbench/dut/arm/dp/RegWriteW	St0
/testbench/dut/arm/dp/PCPlus4F	00000000000000000000000000111100
/testbench/dut/arm/RegSrcD	00
/testbench/dut/arm/ImmSrcD	00
/testbench/dut/arm/ALUControlE	001
/testbench/dut/arm/ALUSrcE	0
/testbench/dut/arm/BranchTakenE	0
/testbench/dut/arm/MemtoRegW	0
/testbench/dut/arm/PCSrcW	0
/testbench/dut/arm/RegWriteW	0
/testbench/dut/arm/ALUFlagsE	1000
[3]	1
[2]	0
[1]	0
[0]	0
/testbench/dut/arm/InstrD	10110010100001010111000000000001
/testbench/dut/arm/RegWriteM	0
/testbench/dut/arm/MemtoRegE	0
/testbench/dut/arm/PCWrPendingF	0
/testbench/dut/arm/ForwardAE	00
Now	220 ps
Cursor 1	206 ps



```
/testbench/dut/arm/clk                St0
/testbench/dut/arm/reset              St0
/testbench/dut/arm/PCF                00000000000000000000000000111000
/testbench/dut/arm/InstrF             11100000010001110111000000000010
/testbench/dut/arm/MemWriteM          0
/testbench/dut/arm/dp/ALUResultE      11111111111111111111111111111110
/testbench/dut/arm/dp/ALUOutW         00000000000000000000000000000000
/testbench/dut/arm/dp/ResultW         00000000000000000000000000000000
/testbench/dut/arm/ALUOutM            00000000000000000000000000000000
/testbench/dut/arm/WriteDataM         00000000000000000000000000000000
/testbench/dut/arm/ReadDataM          11100000010011110000000000001111
/testbench/dut/arm/dp/BranchTakenE    St0
/testbench/dut/arm/dp/ALUControlE     001
/testbench/dut/arm/dp/MemtoRegW       St0
/testbench/dut/arm/dp/PCSrcW          St0
/testbench/dut/arm/dp/RegWriteW       St0
/testbench/dut/arm/dp/PCPlus4F        00000000000000000000000000111100
/testbench/dut/arm/RegSrcD            00
/testbench/dut/arm/ImmSrcD            00
/testbench/dut/arm/ALUControlE        001
/testbench/dut/arm/ALUSrcE            0
/testbench/dut/arm/BranchTakenE       0
/testbench/dut/arm/MemtoRegW          0
/testbench/dut/arm/PCSrcW             0
/testbench/dut/arm/RegWriteW          0
/testbench/dut/arm/ALUFlagsE          1000
  [3]                                 1

Now        220 ps
Cursor 1   206 ps
```

LDR R2, [R0, #96]   ; R2 = mem[96] = 7   E5902060



	Msgs
/testbench/dut/arm/PCF	00000000000000000000000001000000
/testbench/dut/arm/InstrF	11100101100100000010000001100000
/testbench/dut/arm/MemWriteM	0
/testbench/dut/arm/dp/ALUResultE	00000000000000000000000000000111
/testbench/dut/arm/dp/ALUOutW	11111111111111111111111111111110
/testbench/dut/arm/dp/ResultW	11111111111111111111111111111110
/testbench/dut/arm/ALUOutM	00000000000000000000000000001100
/testbench/dut/arm/WriteDataM	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
/testbench/dut/arm/ReadDataM	11100010010000110111000000001001
/testbench/dut/arm/dp/BranchTakenE	St0
/testbench/dut/arm/dp/ALUControlE	001
/testbench/dut/arm/dp/MemtoRegW	St0
/testbench/dut/arm/dp/PCSrcW	St0
/testbench/dut/arm/dp/RegWriteW	St1
/testbench/dut/arm/dp/PCPlus4F	00000000000000000000000001000100
/testbench/dut/arm/RegSrcD	10
/testbench/dut/arm/ImmSrcD	01
/testbench/dut/arm/ALUControlE	001
/testbench/dut/arm/ALUSrcE	0
/testbench/dut/arm/BranchTakenE	0
/testbench/dut/arm/MemtoRegW	0
/testbench/dut/arm/PCSrcW	0
Now	380 ps
Cursor 1	226 ps

THANK YOU !