**Zewail City of Science and Technology** **University of Science and Technology**

**Communications and Information Engineering Program**

**CIE 239, Digital Design and Computer Architecture, Fall 2022**

# Project Announcement

## I. Introduction:

In this project, you will work in teams of 2 to 4 students. You will be required to turn in both your code, hardware, and a detailed report for each phase documenting the work done step by step and results of your project. In addition, you are required to pass the final discussion session of your work as a team before the final exam. The project will be structured over two mandatory phases, where the detail of each phase is explained in the following sections.

## II. Project Outline:

In this project you will design, implement, and verify the functionality of a stopwatch system using HDL (SystemVerilog IEEE 1800-2017), the De0-Nano FPGA development platform, and the necessary supporting hardware. The result of this project should at least meet the main objectives below. Additional bonus objective(s) will also count as bonus coursework marks.

### Functional Requirements:

Create a special stopwatch that can count in both directions, up and down. The stopwatch must be able to display 4 digits, 2 for minutes and 2 for seconds: $M_1M_0{:}S_1S_0$ . The minimum starting value of the stopwatch is unusual, which is always 10:20. So, if the stopwatch is reset, it will be reset to this starting value. i.e., it must never display time values less than 10 minutes and 20 seconds. Same thing if the stopwatch is counting down, it stops at this minimum. Also, the maximum value of this stopwatch is 49:30. So, if it counts up to its maximum, it will stop at this value. i.e., it must never display time values greater than 49:30.

It has six inputs as follows:

- One **DIP switch** for starting and pausing the count operation. If paused while counting the counter will keep its latest value. The circuit can resume counting if start is pressed again later.
- One **DIP switch** for toggling between the count up and count down modes. The design must prevent the toggling of the **counting modes** if counting is ongoing. i.e., mode toggling is allowed only if the stopwatch is paused.

- One **DIP switch** for speeding up the watch rate i.e., the watch will count two digits each second.
- One **DIP switch** for slowing down the watch rate i.e., the watch will advance one digit each two seconds.
- One **push button** for resetting. When pressed, the time displayed is reset to the minimum starting value. Resetting is allowed while counting or while paused.
- One **push button** for adding (or subtracting) 2 minutes each time it is pressed (add2 button). The adding or subtracting is allowed while counting and while paused.
    - Count up mode: adding 2 minutes each time it is pressed.
    - Count down mode: subtracting 2 minutes each time it is pressed.

The system displays its outputs as BCD using 16 LEDs. Eight LEDs are built-in the Deo-Nano board for displaying the seconds. The other eight LEDs are to be connected externally for displaying the minutes.

**Optional Features:**

- Two special cases should be anticipated in the design of the stopwatch. Namely:
    - Error Code 1: The error code F3:F3 should flash twice in case the user attempts to change the **counting mode** while counting is in progress. For example, let's say the pre-change mode was "count up". In this case, while flashing, the counting up runs in the background, and once the flashing is done, correct counting will continue to be displayed as normal (up). If the counting mode is switched back, nothing changes, as we are already counting in the pre-change mode.
    - Error Code 2: The error code 55:55 should keep flashing in case the speed up and slow down modes are activated at the same time. The stopwatch must pause in this case. When the user deactivates either speed up or slow down mode, the flashing stops and the stopwatch resumes counting from its last value before the error in the correct mode.
- Displaying the output of the stopwatch using 4 external seven-segment-display units on a separate board (available in the lab).

**Main objectives:**

Phase 1

1- Identify more than one design approach.
   - e.g., with respect to the types of counters or the stopwatch control mechanism, etc.
2- Select the most suitable approach, given the system's functional requirements. Justify your decision.
3- Clearly design of the system building blocks hierarchically
   - Specifying each of its building blocks in detail.
   - The design must include the main units of the system, like multiplexers, decoders, adders, comparators, registers, counters, control unit, etc.
4- A simulation of each building block of the digital system working separately.
   - The units must be created using the structural style.
   - Document of the work done, the simulations, and the code.

Phase 2

1- Integrate the implemented modules into the whole stopwatch system, simulate the operation of the system using a **testbench** which must cover all the design states.
   - Document the work done, design details, simulations, and the code.
2- Implement the fully functioning stopwatch system using the FPGA development board (**DE0-Nano board**).

**Bonus objectives:**

- Error code 1
- Error code 2
- Seven segment display of the outputs

## III. Deliverables:

There are multiple steps to the final project, as follows:

### 1. Declaration of Teams:

- By the due date, one student from each team must declare the list of team members (name and ID).
- When selecting a team, keep in mind that all its members must be present in the final discussion. The absence of one member of the team from the final discussion may negatively impact the discussion mark of the others.
- Missing the due date of this step may result in 10% deduction of the project mark.

2. **Deliverables of Phase 1:**
   - Submit a progress report document describing the design, verification, and implementation steps of each implemented building block so far in detail.
   - Submit the project's HDL files by the deadline.

3. **Deliverables of Phase 2:**
   - Submit the final report document describing the design, verification, and implementation steps of the whole project in detail.
   - Submit the project's HDL files (and hardware) by the deadline.
   - You should confirm that your project works one week ahead of the phase 2 to give yourself time to finalize the project and the report.

**4. Discussion:**
   - During the discussion time each team must present a short demonstration of the hardware.
   - All team members must attend together in the assigned discussion time. If a team misses the discussion time, or if one member is absent, the discussion mark may be negatively impacted.

## IV. Important Notes:

- All modules must be built by the team members from scratch.
- Your code should include easy to understand comments.
- The progress reports must include a section for each team member that clearly outlines the individual work done by each team member.
- The reports must be presented well.
- For each phase, the report must explain and document every detail of the work done, including the block diagram(s), especially the system hierarchy and the state diagram, the components used, verification effort, etc.
- The code must run properly on the simulation tool. Similarly, the system must function properly on the development platform on the discussion day.