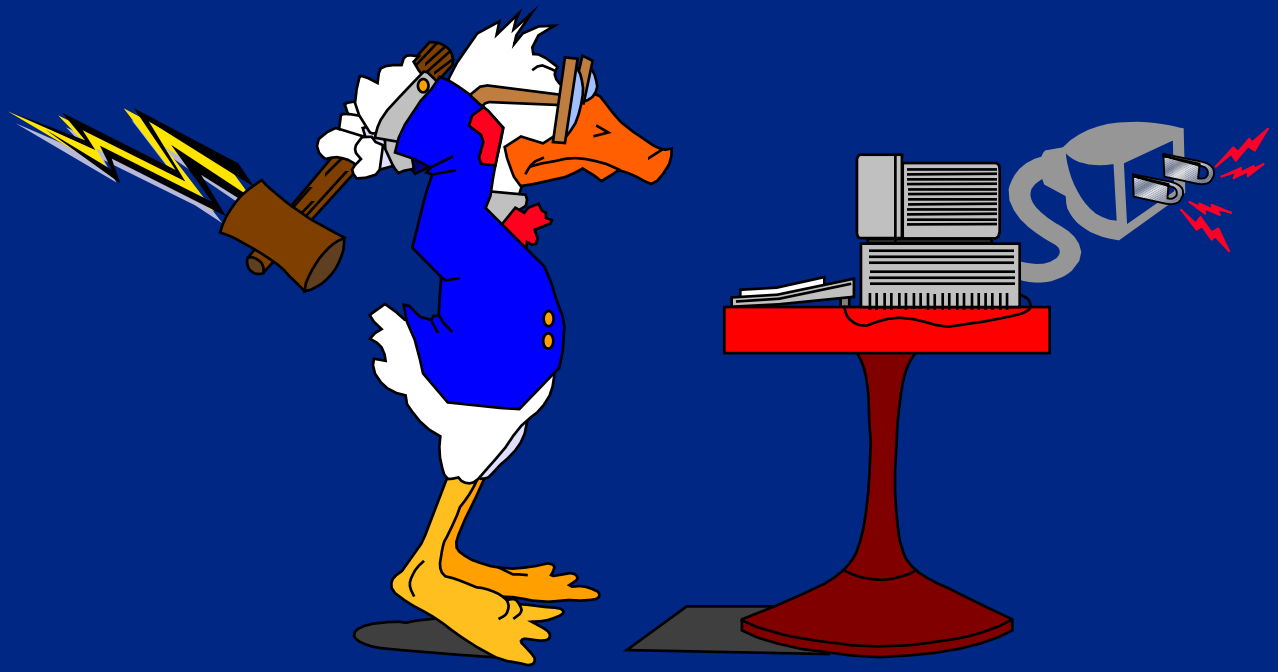
844 EMC

Designing PIC® Microcontroller Circuits for EFT/ESD Compatibility

Electro Magnetic Compliance

(ESD, EFT & Transformerless power supplies)



Overview of EMC

- EMC- Electromagnetic Compatibility
  - Capability of an electronic system to function compatibly with other electronic systems and not produce nor be susceptible to interference
  - A system is electromagnetically compatible if:
    - It does not cause interference with other systems
    - It is not susceptible to emissions from other systems
    - It does not cause interference with itself

Regulations

- FCC-Federal Communications Commission
- IEC - International Electrotechnical Commission
- Military
- Medical
- Vehicular
- Other

FCC

- Focus on emissions

  Any unintentional radiator (device or system) that generates and uses timing pulses at a rate in excess of 9000 pulses (cycles) per second and uses digital techniques…

- Defines two classes
  - Class A: marketed for use in commercial, industrial or business environments
  - Class B: marketed for use in residential environment, but includes use in commercial industrial or business environments

IEC

- International body that processes regulations to facilitate trade between countries
- Regulations focus on both emissions and immunity
- Standards include the IEC 61000-x-x
- Also include CISPR standards
  - International Special Committee on Radio Interference includes CISPR 11, 22
  - Two types of standards
    - Basic standard covers specific interference
    - Product standard covers specific products

Class Objectives

- Focus on EMC subgroups
  - "It is not susceptible to emissions from other systems"
    - Electrical Fast Transients (EFT)
    - Electro Static Discharge (ESD)
  - "It does not cause interference with itself"
    - Inductive Loads
    - Connectors/Cables

IEC Standards

- 60601 -> Medical electrical equipment
- 61000-3 -> Electromagnetic Compatibility
- **61000-4-2 -> Electro Static Discharge (ESD)**
- 61000-4-3 -> Radiated Electromagnetic Field
- **61000-4-4 -> Electrical Fast Transients (EFT)**
- 61000-4-5 -> Surge
- 61000-4-6 -> RF Field Conducted Disturbances
- 61000-4-11 -> Voltage dips and interruptions

Class Objectives

- Focus Applications
  - Cost-Sensitive Applications (Single/Two layer Printed Circuit Boards (PCB))
  - Typical Application
    - Uses microcontroller and some digital glue logic
    - Uses some analog blocks
    - Does power control through Relays/Triacs
    - May use transformerless power supply

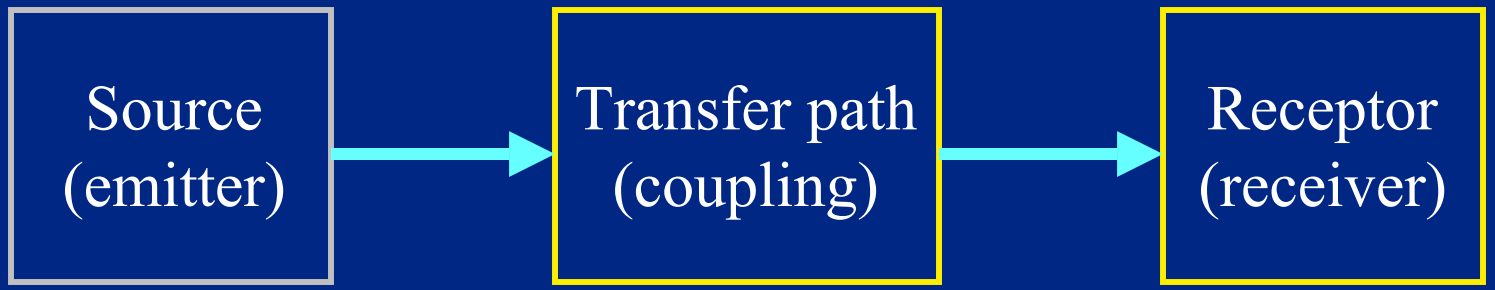
Class Objectives

- Procedure
  - Explain fundamentals
  - Provide simple low-cost Tips & Tricks for:
    - PCB layout & component placement
    - Use cheap (mainly passive) components
    - Component selection

Agenda

- EMC overview
- Noise fundamentals
- EFT standard - IEC 61000-4-4
- ESD standard - IEC 61000-4-2
- Transformerless power supplies
- PCB layout fundamentals
- Tips & tricks
- Component selection (Bonus)

Composition of EMC

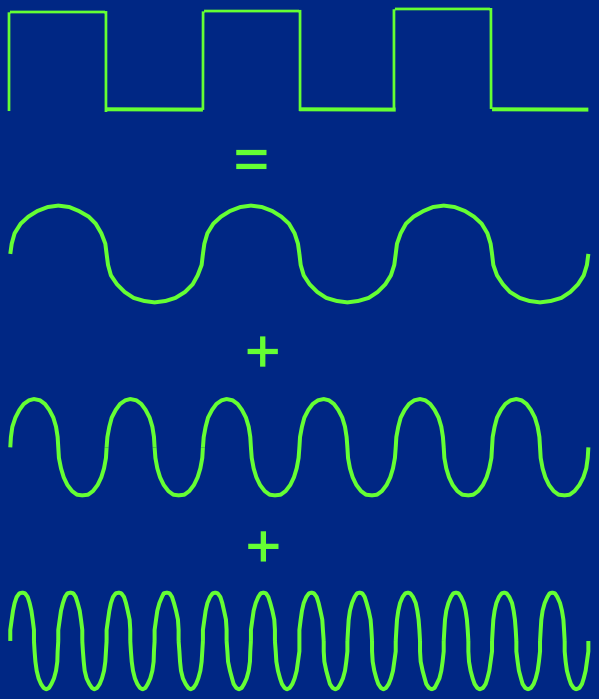


Interference Sources

- External
  - Electro-Static Discharge (ESD)
  - Electrical Fast Transients (EFT)
- Internal
  - Digital
    - Microcontroller/Microprocessor
    - Discrete logic
  - Power Electronics
    - Relays, SCR, Triac

Interference Sources

- Internal
  - Switching (for Gaussian system 3dB $BW = \frac{0.35}{t_r}$)



Radiated Noise: B-Field

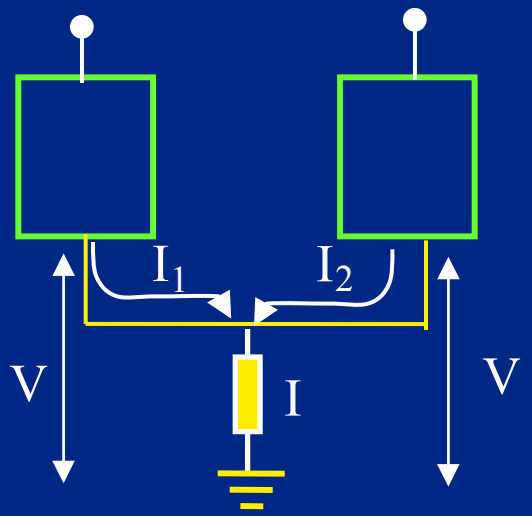
- Sources
  - On board transformers
  - Switching regulators
  - External noise
- Victims (Receivers)
  - Single-ended, high-impedance inputs
  - Traces that form a circle
    - Classic example: Ground loop
    - Signal loop
  - Long traces (acts like an antenna)

Reducing Radiated Noise

- Identify capacitive coupling problems
- Reduce all trace distances where possible
- Reduce the number of corners with Sensitive traces
- Eliminate all ground loops
- Use GROUND planes
  - One plane
  - Two planes, Analog and Digital

Conducted Noise

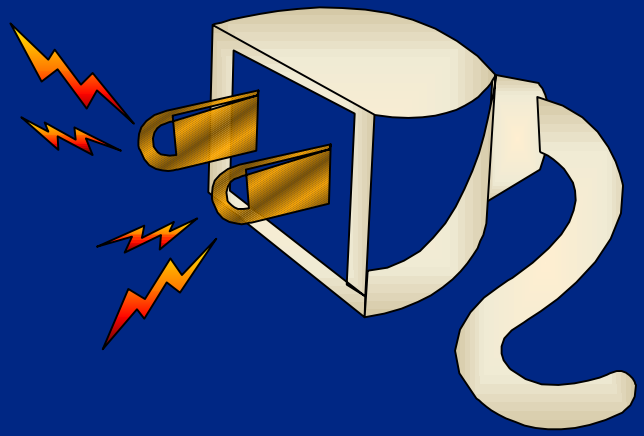
- Ground and Power
  - 60 or 50 Hz
  - Digital switching
  - Ground current return paths
  - Supply current return paths
- Signal path
  - Digital switching
  - Noise generated by previous device



Noise Reduction Tools

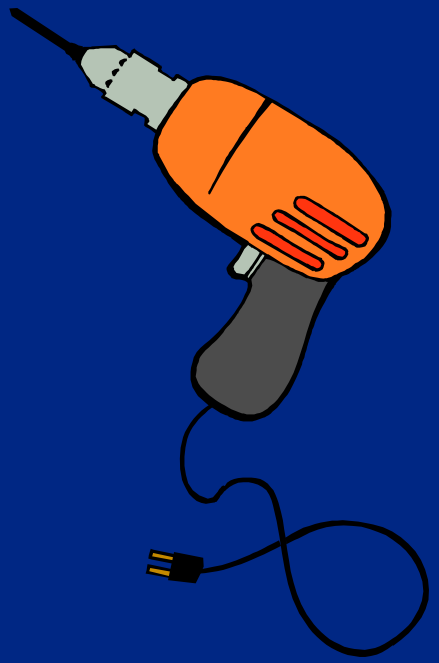
- Ground and Power Supply
  - Bypass capacitors
  - R/C filters
  - Low-impedance ground and power planes
  - Ferrite beads
  - Component placement on the board
- Signal path
  - Analog and digital filters
  - Analog differential signal path
  - Component placement on the board

Electrical Fast Transients (EFT) IEC 61000-4-4



Why EFT?

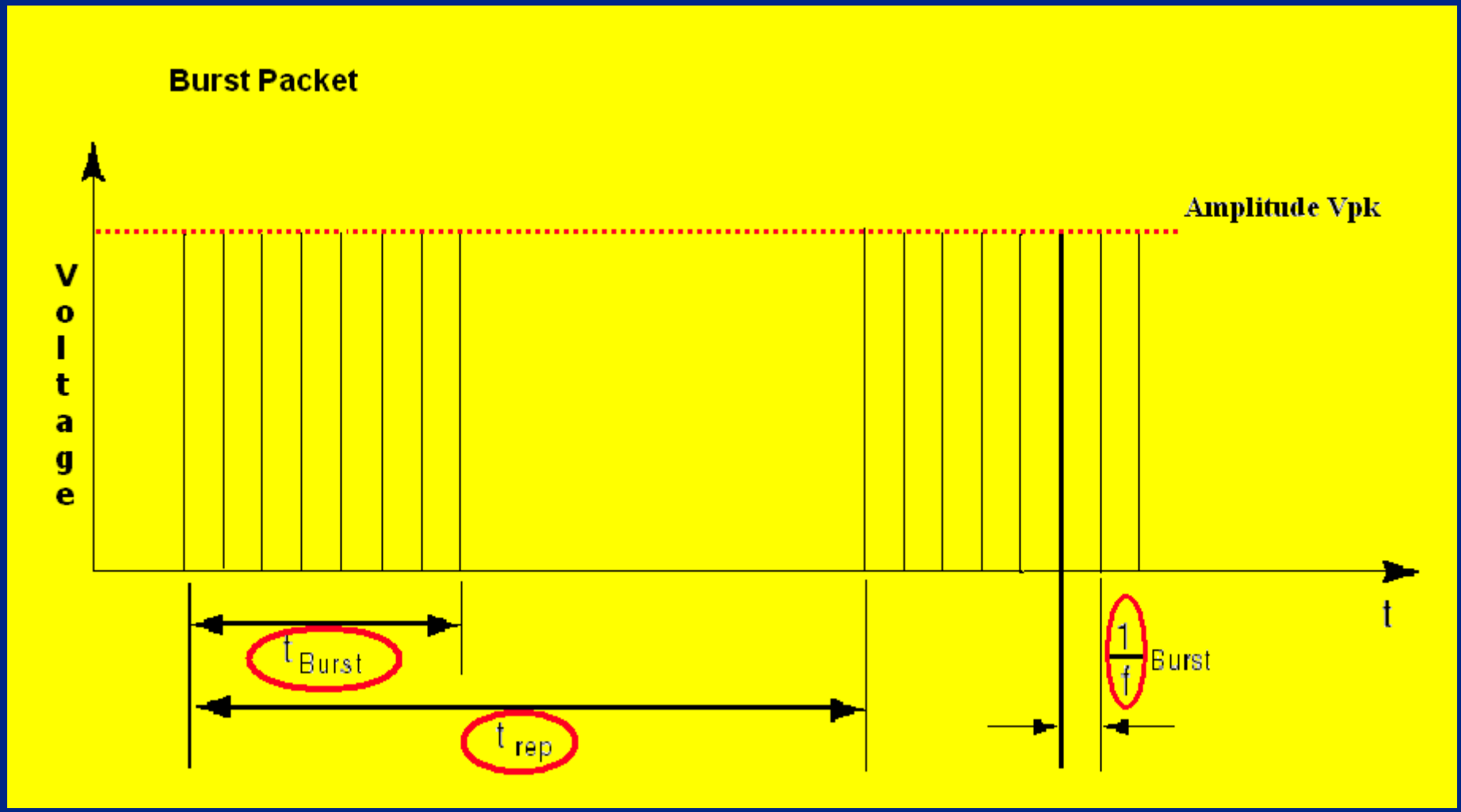
- Bursts of interference pulses simulates inductively loaded switches



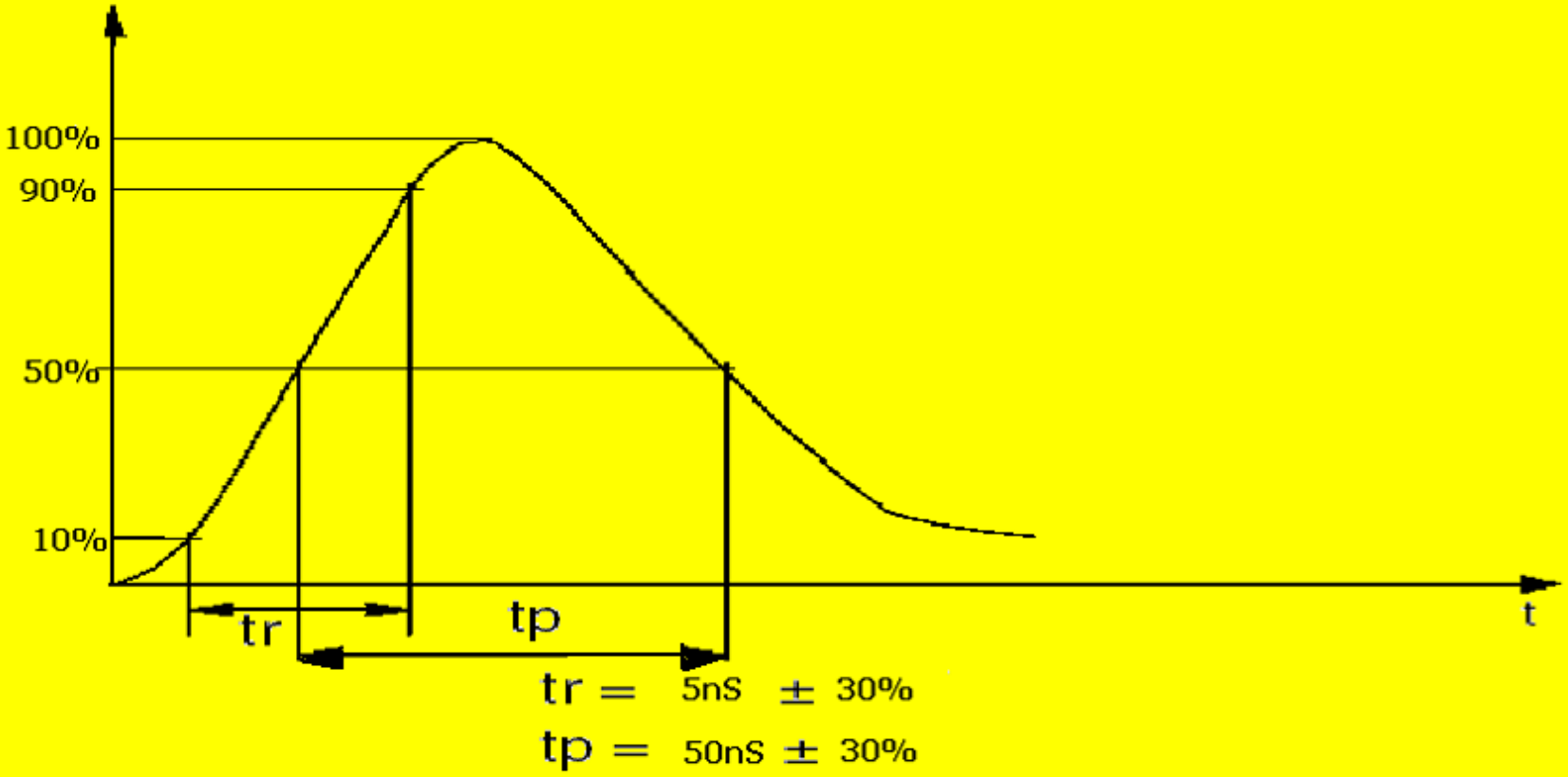
IEC 61000-4-4

- The “System Level” standard defines
  - Test voltage waveform
  - Range of test levels
  - Test equipment
  - Test set-up
  - Test procedure

IEC 61000-4-4
Test waveform



IEC 61000-4-4
Test waveform



IEC 61000-4-4
Test Levels

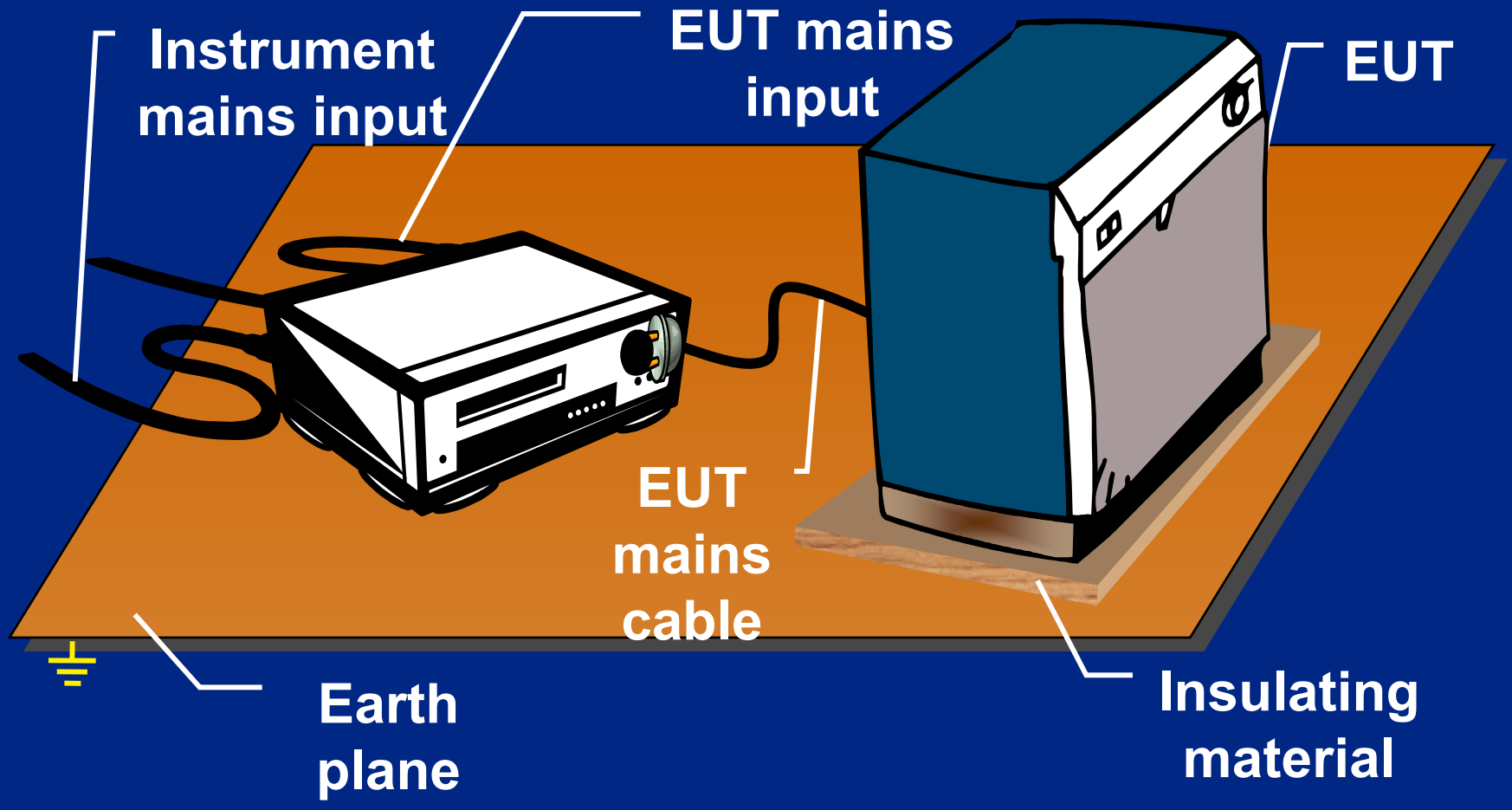
Level	Power Supply Ports		I/O signal, data and control Ports	
	Voltage Peak kV	Repetition rate kHZ	Voltage Peak kV	Repetition rate kHZ
1	0.5	5	0.25	5
2	1	5	0.5	5
3	2	5	1.0	5
4	4	2.5	2.0	5
X	Special	Special	Special	Special

IEC 61000-4-4
Test equipment

- Polarity: Positive/Negative
- Asynchronous to power supply
- Coupling
  - Power supply ports
    - Internal: Asymmetric: L, N, PE, L-N, L-PE,
    - N-PE, L-N-PE, 3phase
  - I/O and communication ports
    - Capacitive coupler

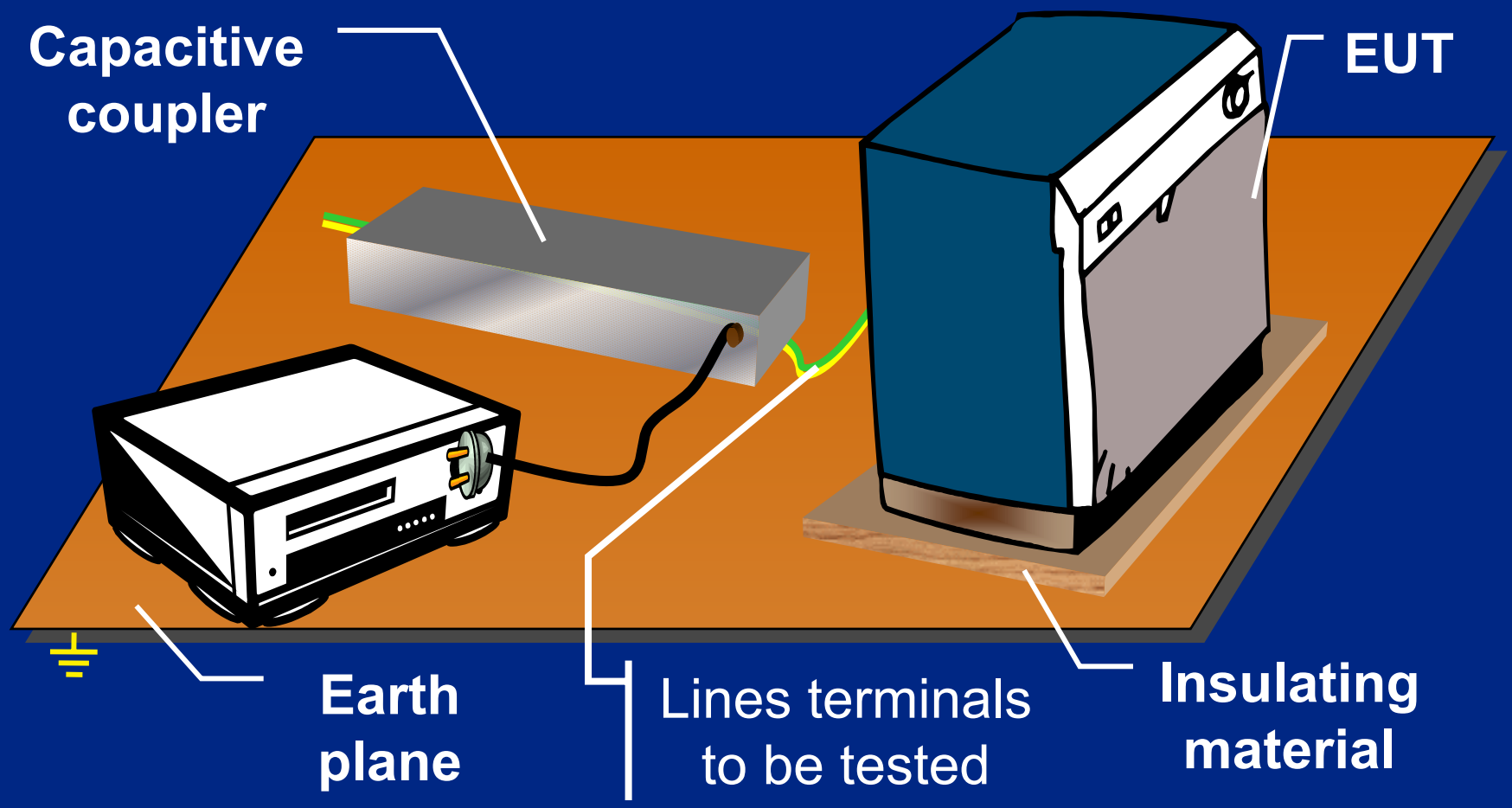
IEC 61000-4-4

Test set-up (Power Supply ports)



IEC 61000-4-4

Test set-up (Power Supply ports)

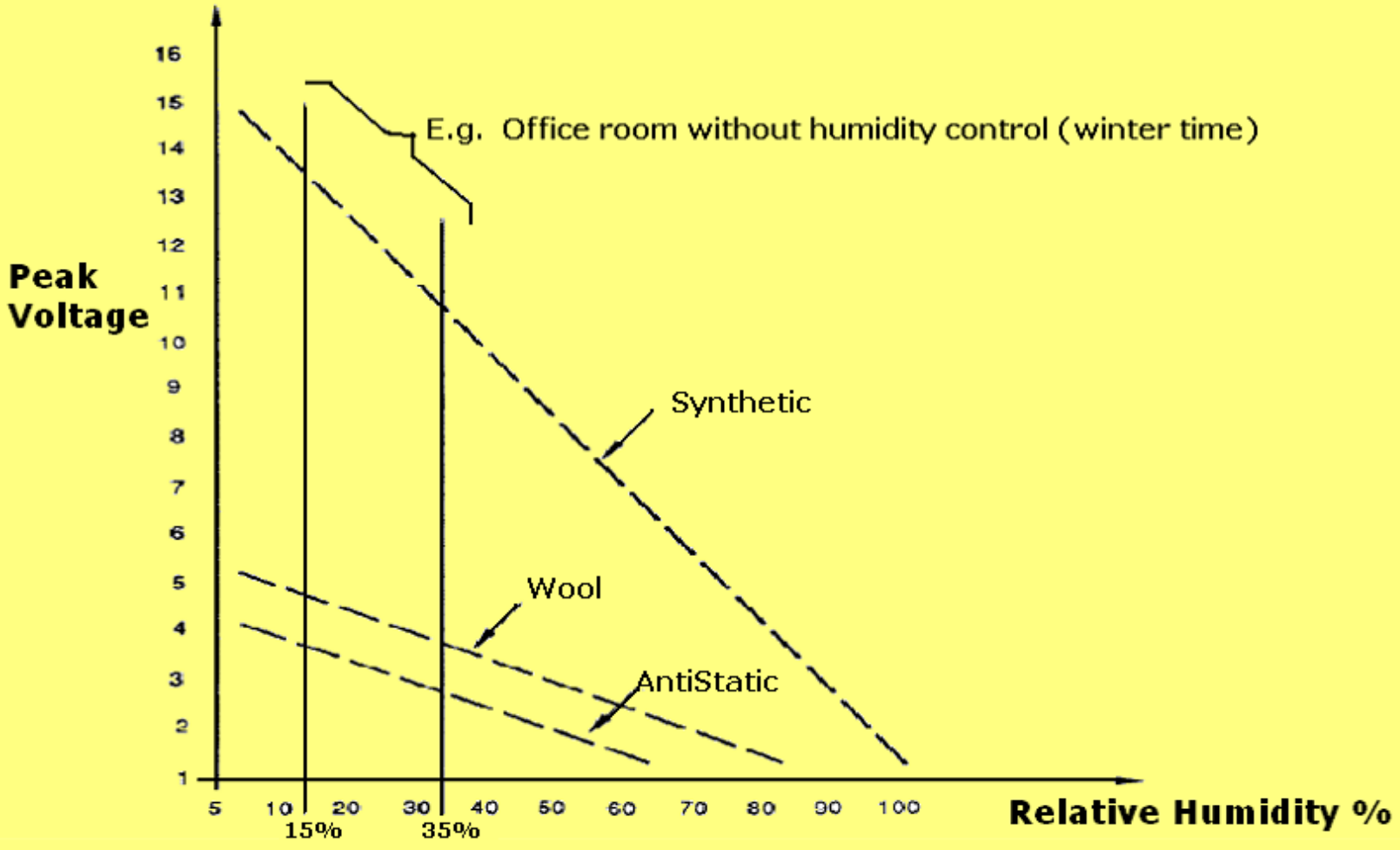


Electro-Static Discharge (ESD)
IEC 61000-4-2

Why ESD?

- Static Discharge
- ESD a “Context Sensitive” issue
  - Semiconductor
  - Manufacturing
  - End user

Why ESD?



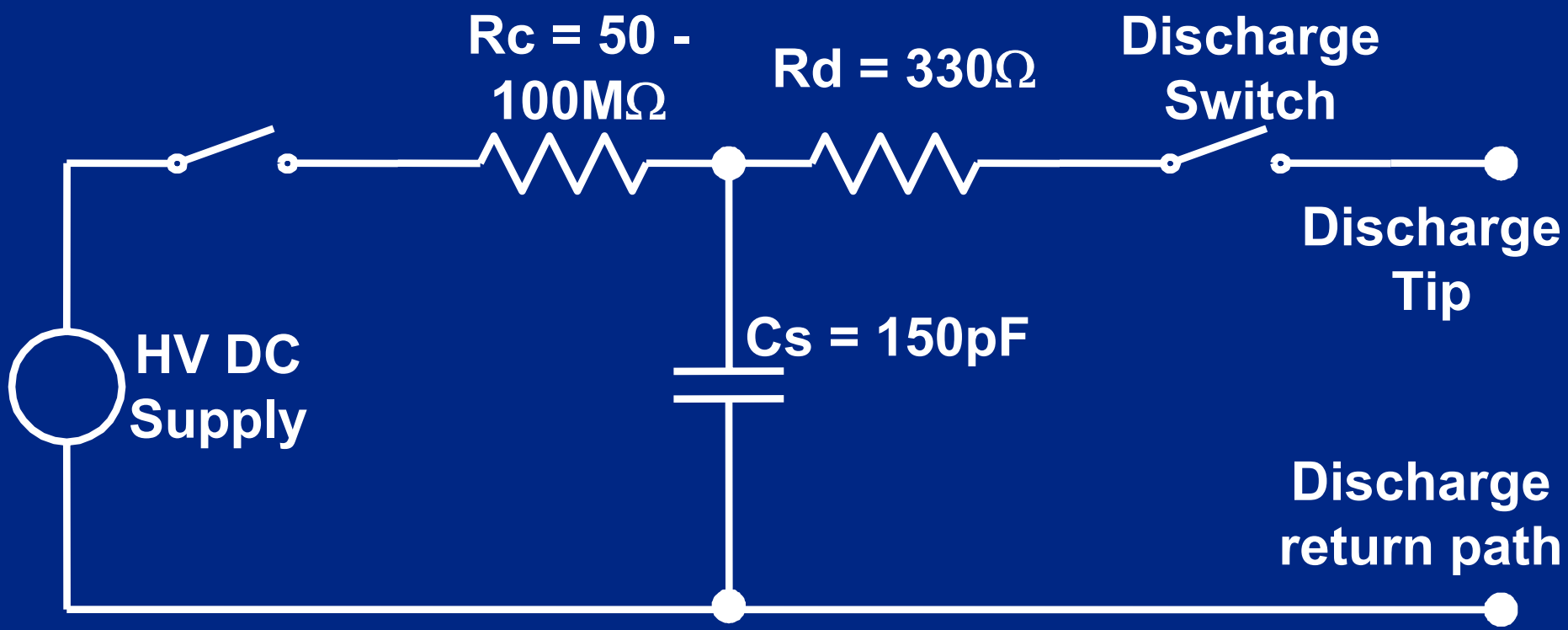
ESD

- Semiconductor perspective
  - JESD22-A114B for HBM
  - JESD22-A115A for MM
  - Microchip corporate guidelines are 4000V-HBM and 400V-MM.
- Manufacturing perspective
  - Anti static work station
  - Wrist band
  - Grounded systems

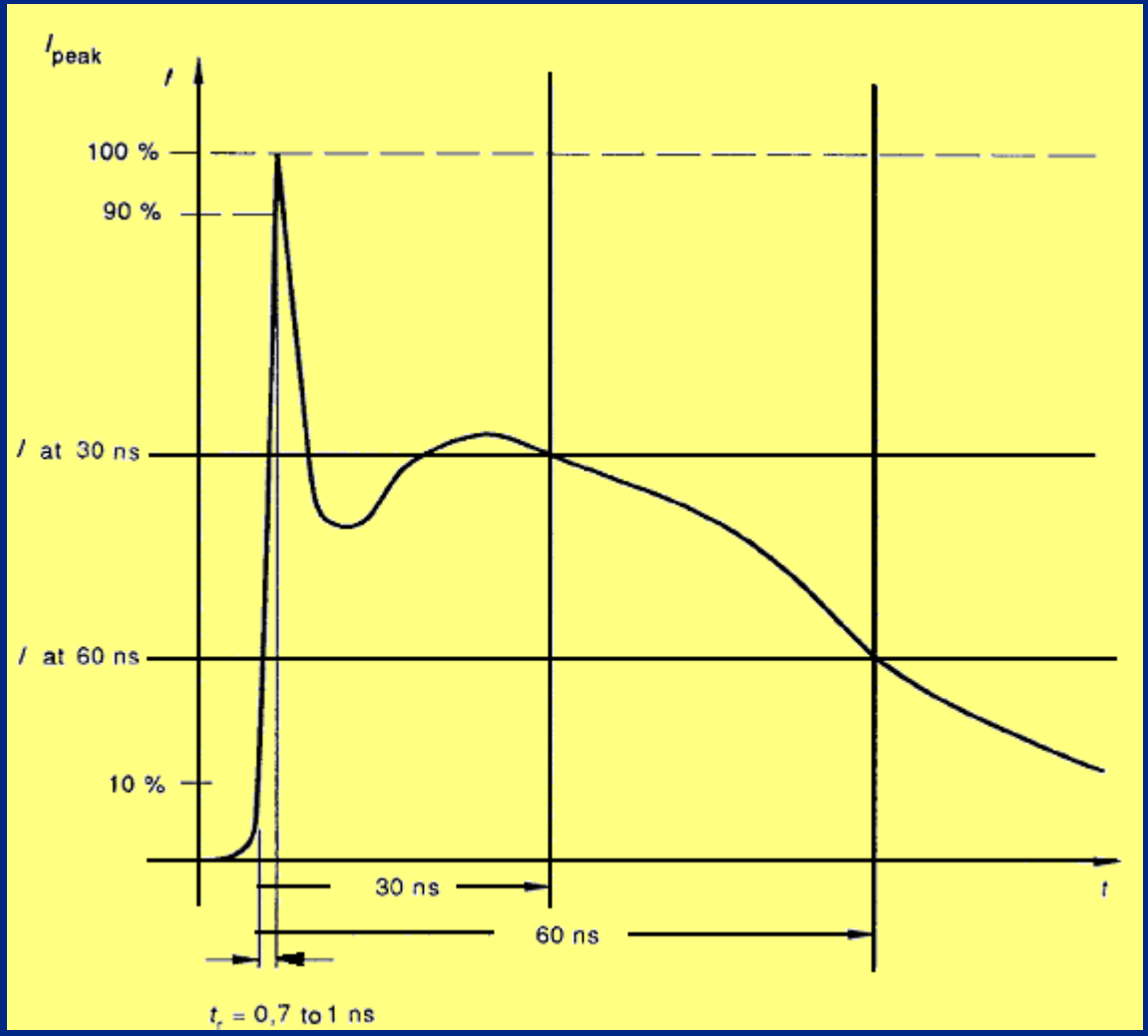
IEC 61000-4-2

- End User perspective
- The “System Level” standard defines:
  - Test voltage waveform
  - Range of test levels
  - Test equipment
  - Test set-up
  - Test procedure

IEC 61000-4-2
Test equipment



IEC 61000-4-2
Test waveform



IEC 61000-4-2
Test Levels

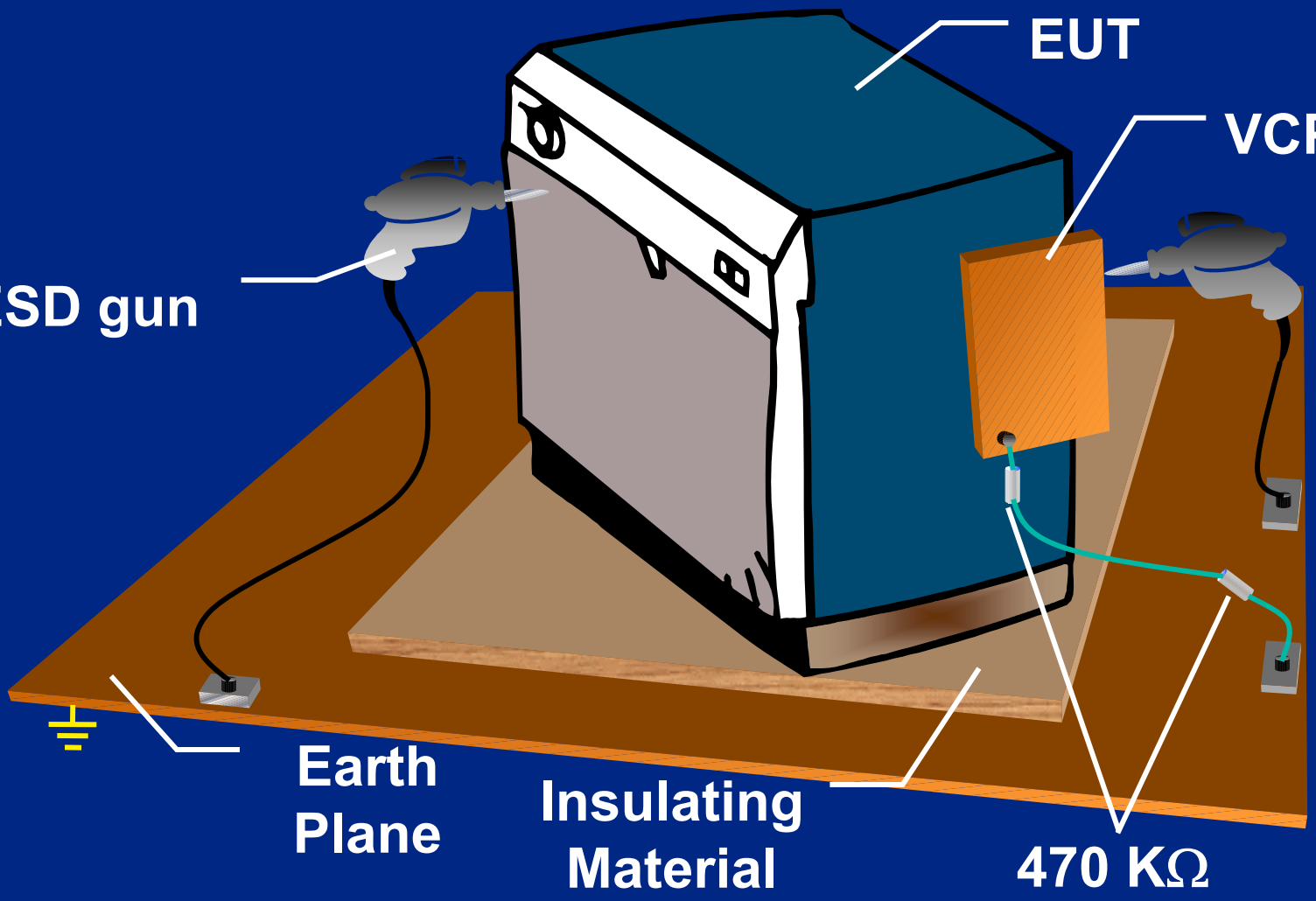
Contact Discharge		Air Discharge	
Level	Test Voltage (kV)	Level	Test Voltage (kV)
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
X	Special	X	Special

IEC 61000-4-2
Waveform Parameters

Level	Voltage (kV)	First Peak Current (A)	Rise time tr nS	Current at 30nS (A)	Current at 60nS (A)
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

IEC 61000-4-2

Test set-up (Floor Standing Equipment)



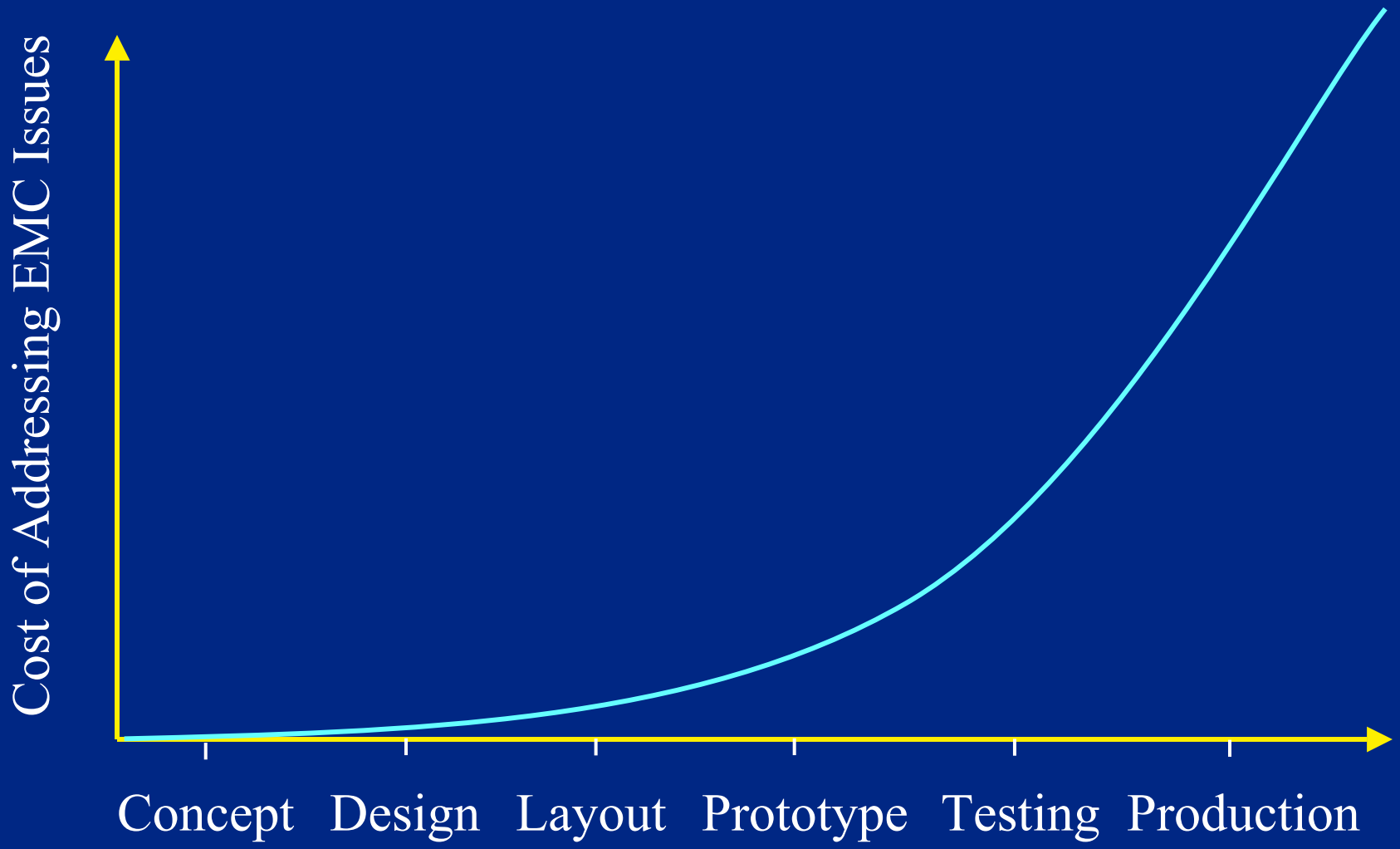
IEC 61000-(4-2 Vs 4-4)

Characteristics	ESD (4-2)	EFT (4-4)
Max Voltage	Up to 15kV	Up to 4kV
Energy	<10mJ	<= 300mJ
Rep Rate	Single Impulse	Multiple Pulses @ 5KHz
Spectrum	~1GHz	~100MHz

EMC Testing

- Pre-compliance testing
  - Get data on engineering prototypes
  - Emphasis on quick results
- Compliance testing
  - Test production prototypes
  - Verify compliance to specific standard
  - Requires accuracy and reliability
  - Requires comprehensive testing
  - Requires comprehensive documentation

Cost of Addressing EMC



Failure Mechanism

- **Common Failure mechanism**
  - Code runs away
  - Reset occurs
  - Port I/O abnormal operation
  - Device hangs, Interrupt/reset can recover
  - Devices latch-up

Latch-up

- Inherent characteristics of CMOS
  - High current flow
  - Destructive
- Prevention
  - Decoupling
  - Current limit (Power supply, I/O)
  - Low-impedance ground

Modern Electronics & EMC

- Smaller Geometry
  - Faster electronics
  - Lower max voltage

EFT Strategy

- Line filters
- Transient protectors
- Isolation transformers
- Voltage regulators
- Isolated high-power circuit

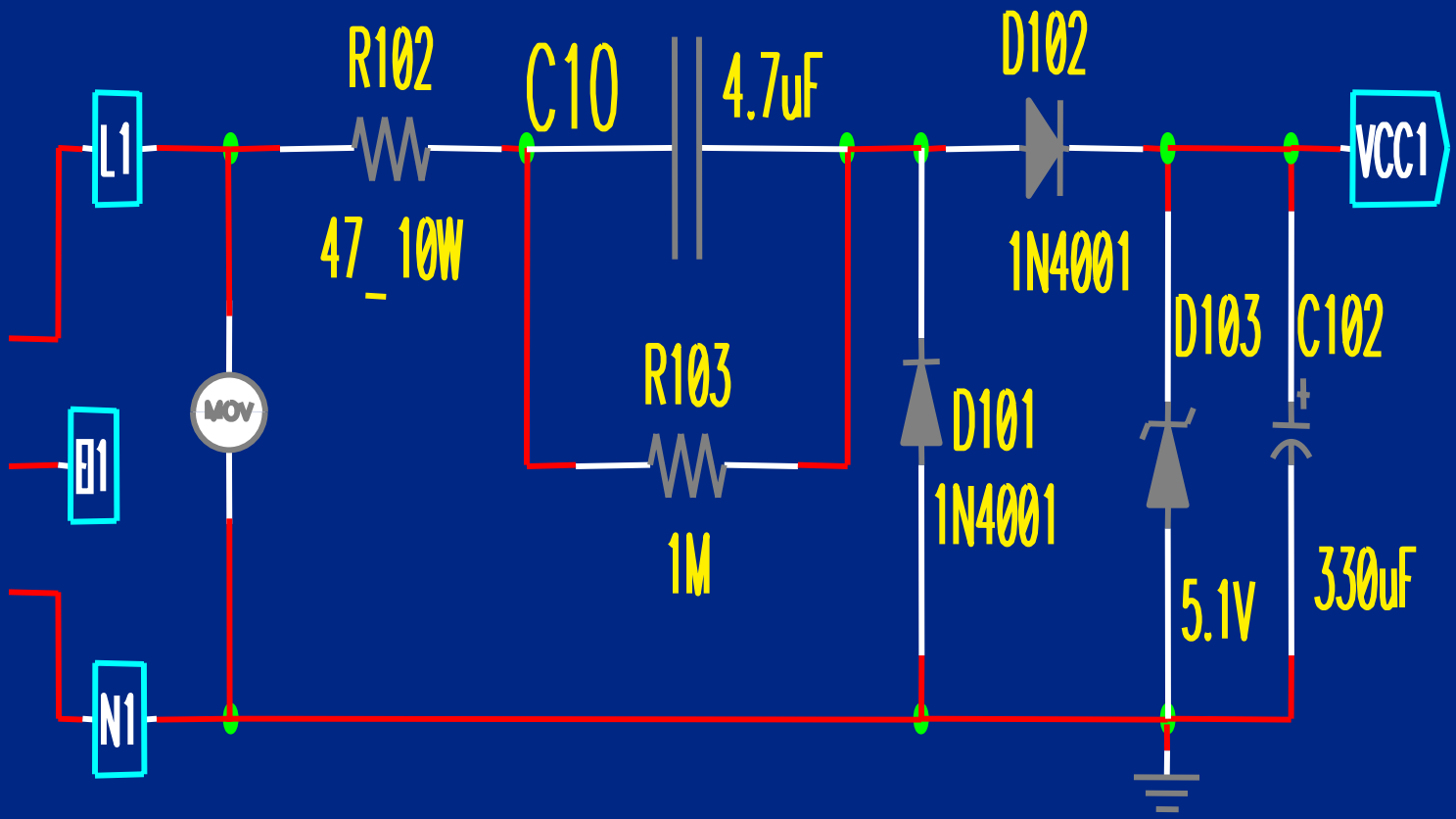
ESD Strategy

- Determine first point of contact
- Limit the current
- Low- inductance ground

Transformerless Power Supplies

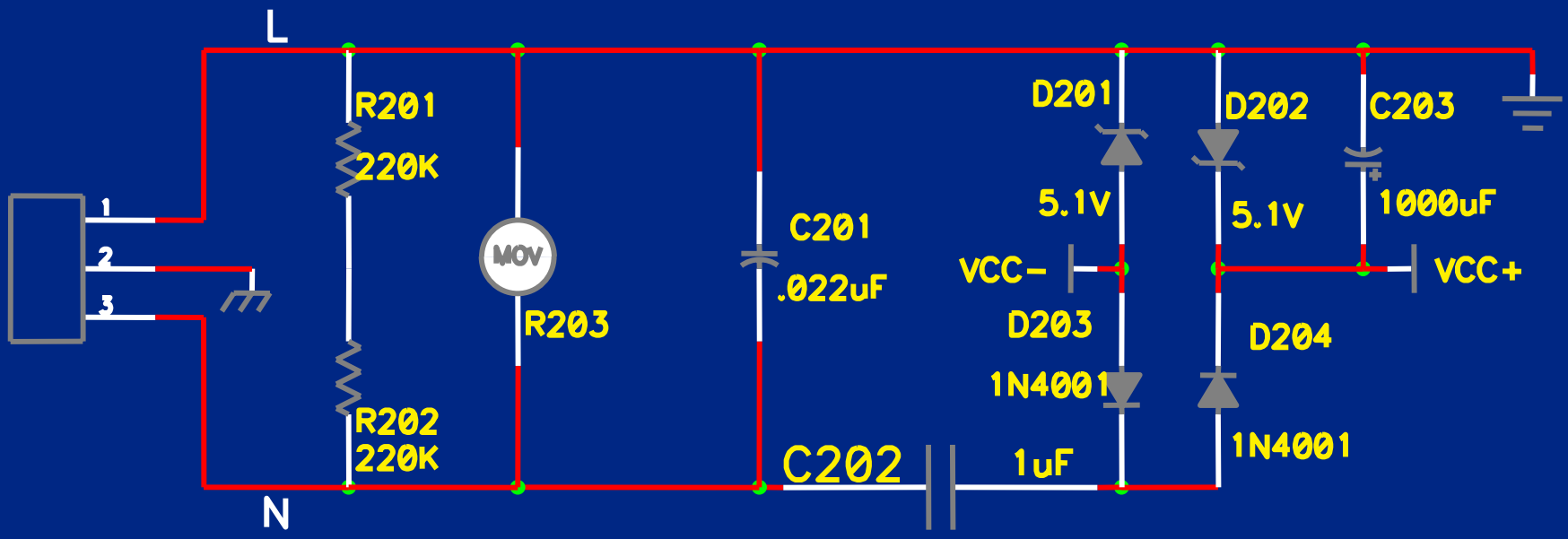
Type I

- Neutral -> Circuit ground



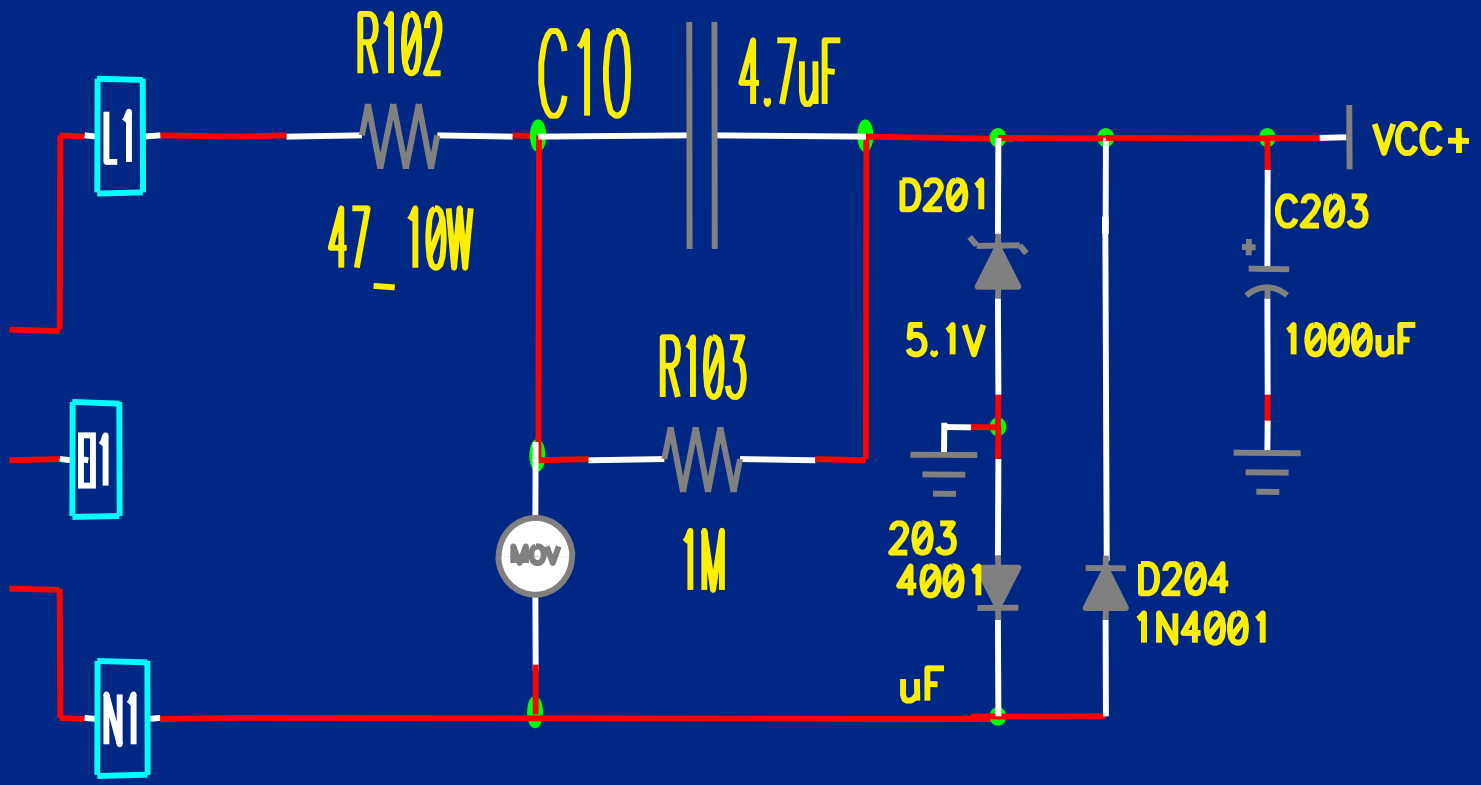
Type II

- Line -> Circuit ground

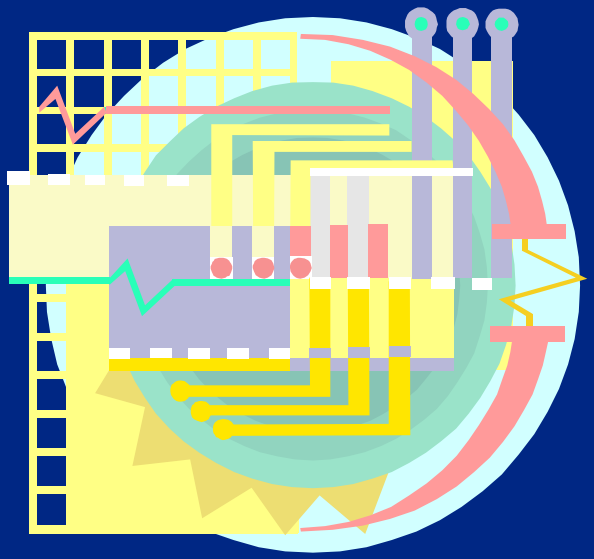


Type III

- Preferred approach
  - Virtual ground



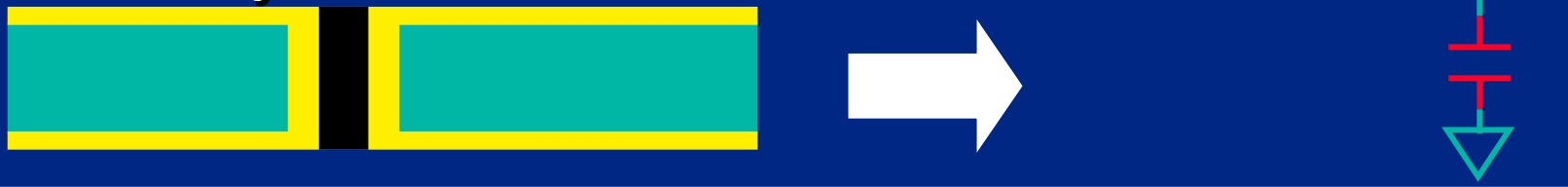
PCB Layout Fundamentals



PCB Layout
Fundamentals

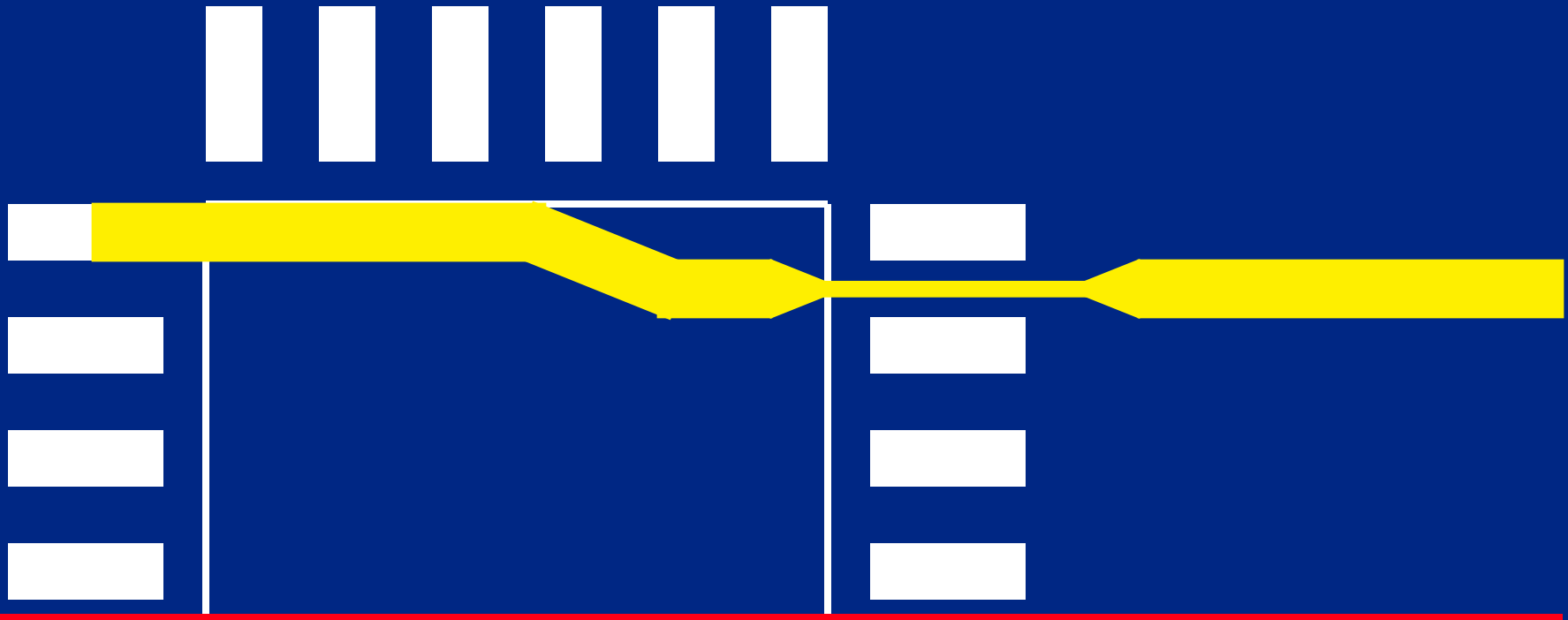
- Primary Goal
  - Connect nodes
- Track

  - Low freq. = Wire; High freq. = Inductor
- Vias
  - Each via introduces ~2 nH & ~0.5 pF
  - Causes impedance mismatches and signal delays



PCB Layout
Fundamentals

- Track Width
  - Any variation causes impedance mismatches (Can be helpful for some cases)



PCB Layout
Trace Resistance

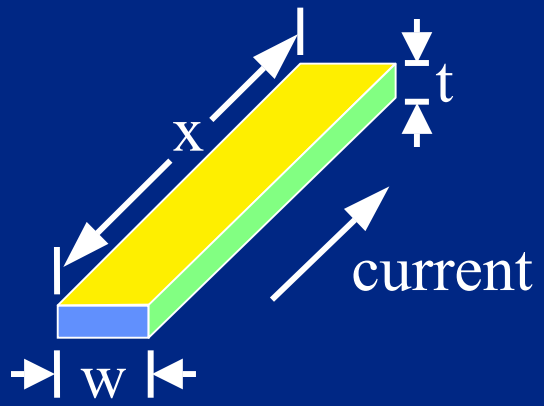
- Trace resistance is based on:
  - Trace length (x)
  - Trace thickness (t)
  - Trace width (w)

ρ = Resistivity

≈ 680 (nΩ-in), Cu (copper)

$t \approx 0.00137$ in/oz, Cu

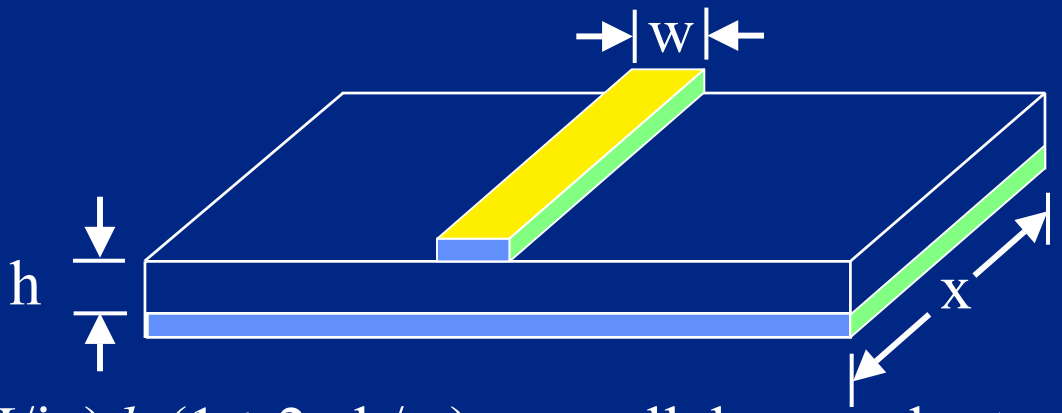
$$R \approx \frac{x}{w} \cdot (0.50\ m\Omega/\square), \quad 1\ oz\ Cu$$



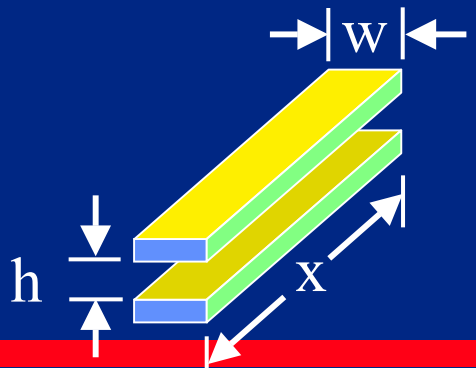
PCB Layout
Trace Inductance

- For PCB traces

$$L \approx x\,(5\ \text{nH/in})\ ln(1 + 2\pi\, h/w), \quad \text{with ground plane}$$



$$L \approx x\,(10\ \text{nH/in})\ ln(1 + 2\pi\, h/w), \quad \text{parallel ground return trace}$$



PCB Layout
Vias

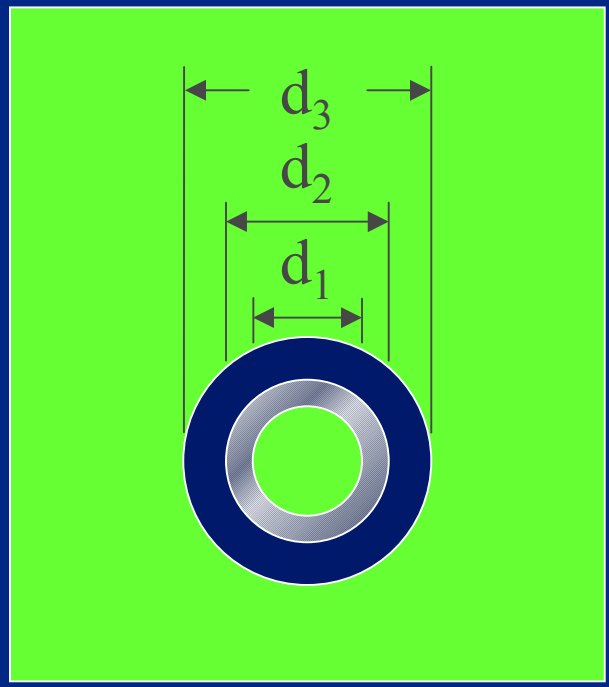
- Via impedances are quite important

d_1 = via diameter
d_2 = via pad diameter
d_3 = ground clearance hole diameter
h = height of via (e.g., board thickness)

$$R \approx \frac{h\,(870\ n\Omega\text{-in})}{d_1^{\,2}}$$

$$C \approx \frac{h\,d_2\,\varepsilon_r\,(1.4\ pF/in)}{d_3 - d_2}$$

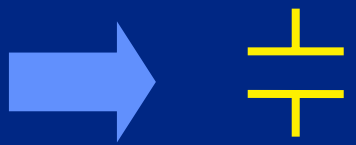
$$L \approx h\,(5\ nH/in)\,ln(1 + 4\,h/d_1)$$



PCB Layout
Fundamentals

- PCB Capacitor
  - Two conductors separated by dielectric
  - Low-inductance capacitor

Two Layer PCB

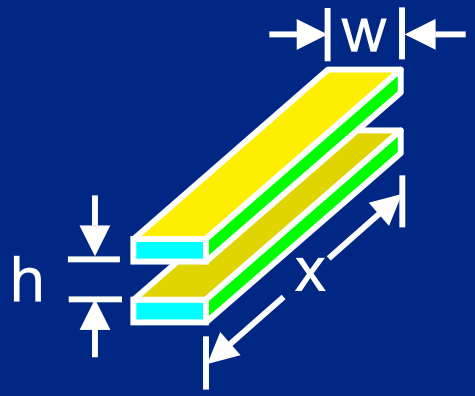


PCB Layout
Trace Capacitance

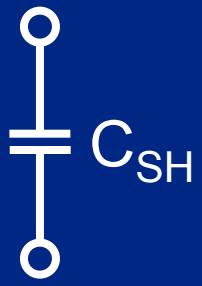
- Capacitance
  - Is caused by an electric field between two conductors
  - Depends on
    - Geometry
    - Separation
    - Dielectric (ε_r)

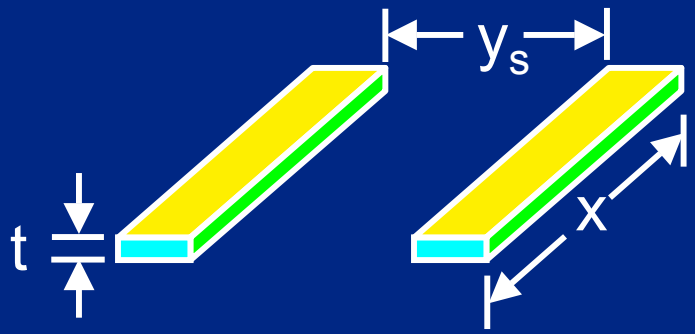
PCB Layout
Trace Capacitance

- Without ground plane



$$C_{SH} \approx \frac{x\,\varepsilon_r\,(0.71\ \text{pF/in})}{ln(1+\pi\,h/w)}, \quad x >> w,h$$

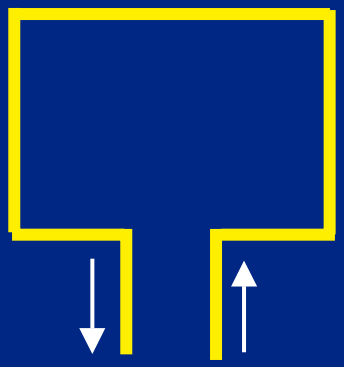




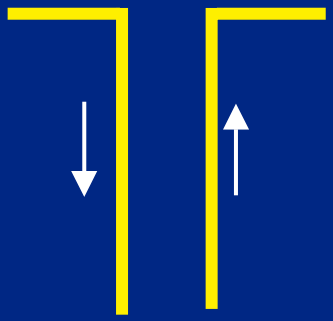
$$C_M \approx \frac{x\,\varepsilon_r\,(0.71\ \text{pF/in})}{ln(1+\pi\,y_s/t)}, \quad x >> t,y_s$$

PCB Layout
Fundamentals

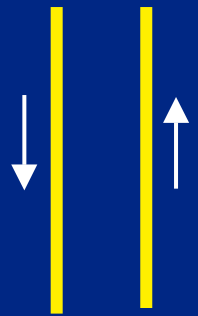
- Watch out for these antennas



Loop antenna



Dipole antenna



Transmission line

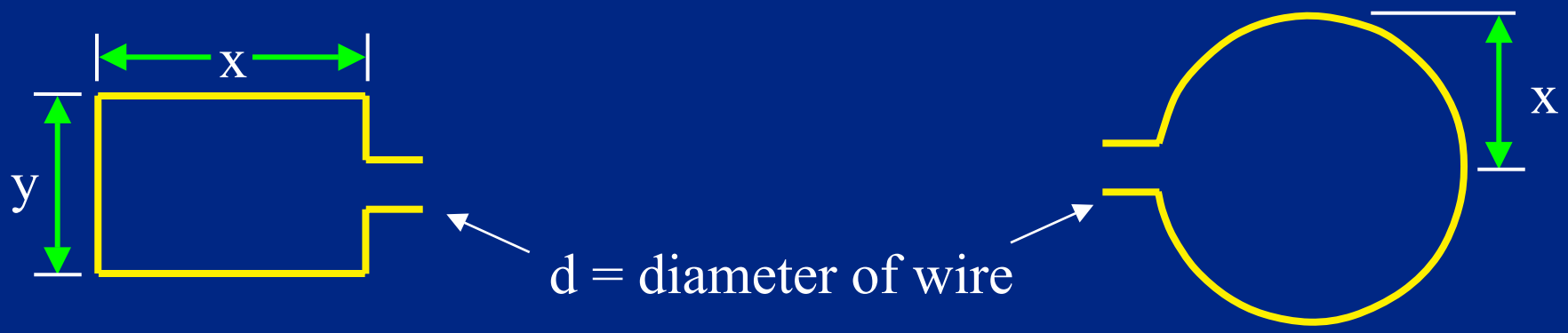
Radiation depends on A, L, I & *f*

PCB Layout
Loop Inductance

- Inductance Is Based on Magnetic Flux
  - Loop Area
  - Geometry

$$L \approx (5\ \text{nH/in})\,(2\ x\ ln(2\ y/d) + 2\ y\ ln(2\ x/d)\,),\quad \text{single rectangular loop}$$

$$L \approx 2\pi\ x\ (5\ \text{nH/in})\,(ln(16\ x/d) - 2),\quad \text{single circular loop}$$

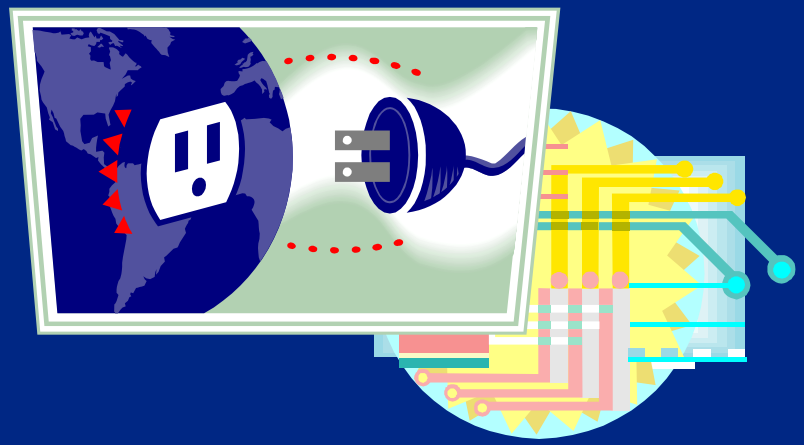


PCB Layout

- Main Goal
  - Connect nodes
- For EMC performance
  - Minimize impedance in intended path
  - Maximize impedance in unintended path

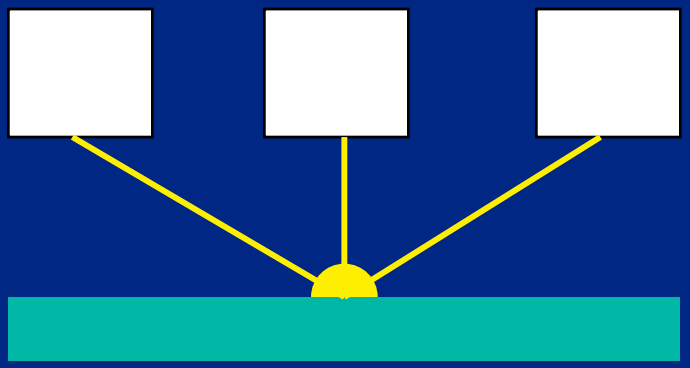
Tips & Tricks

Power, Ground & PCB Layout



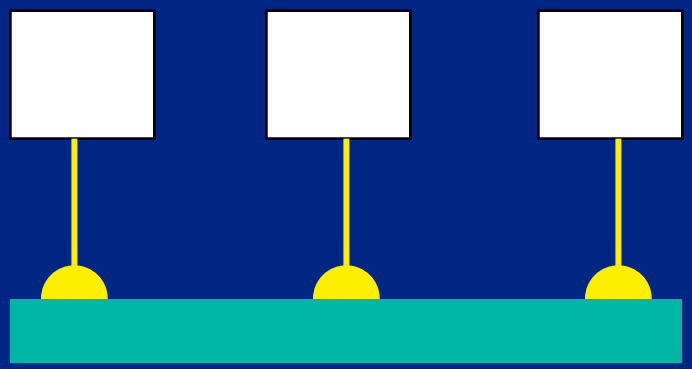
PCB Layout
Grounding

- Two most used grounding techniques
  - **Single Point**



- **Preferred for low frequency**
- **No ground loops**

  - **Multi Point**

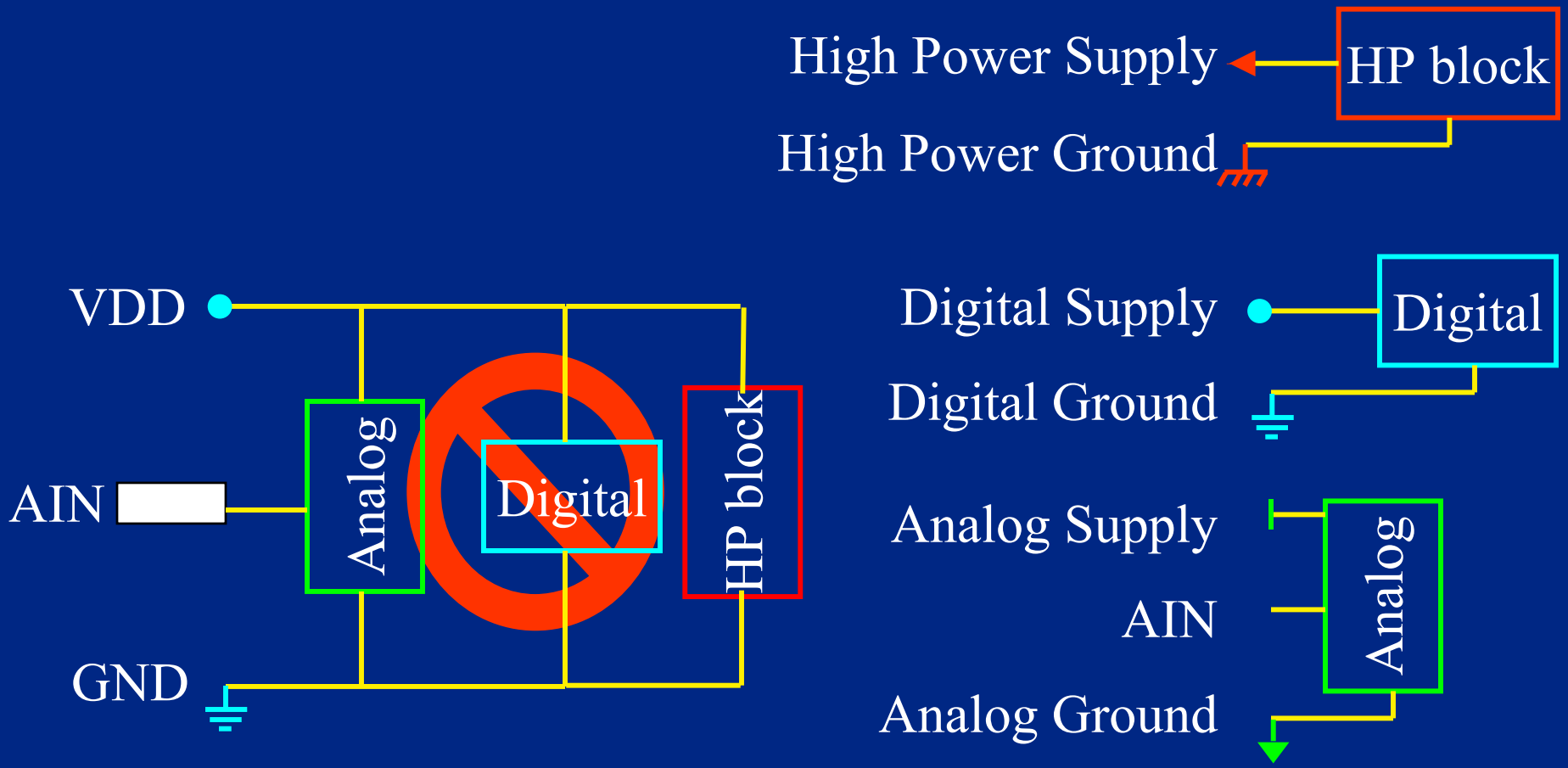


- **Preferred for high frequency**
- **Lesser parasitic inductance & capacitance**

Tip #1
PCB Layout - Hybrid Grounding

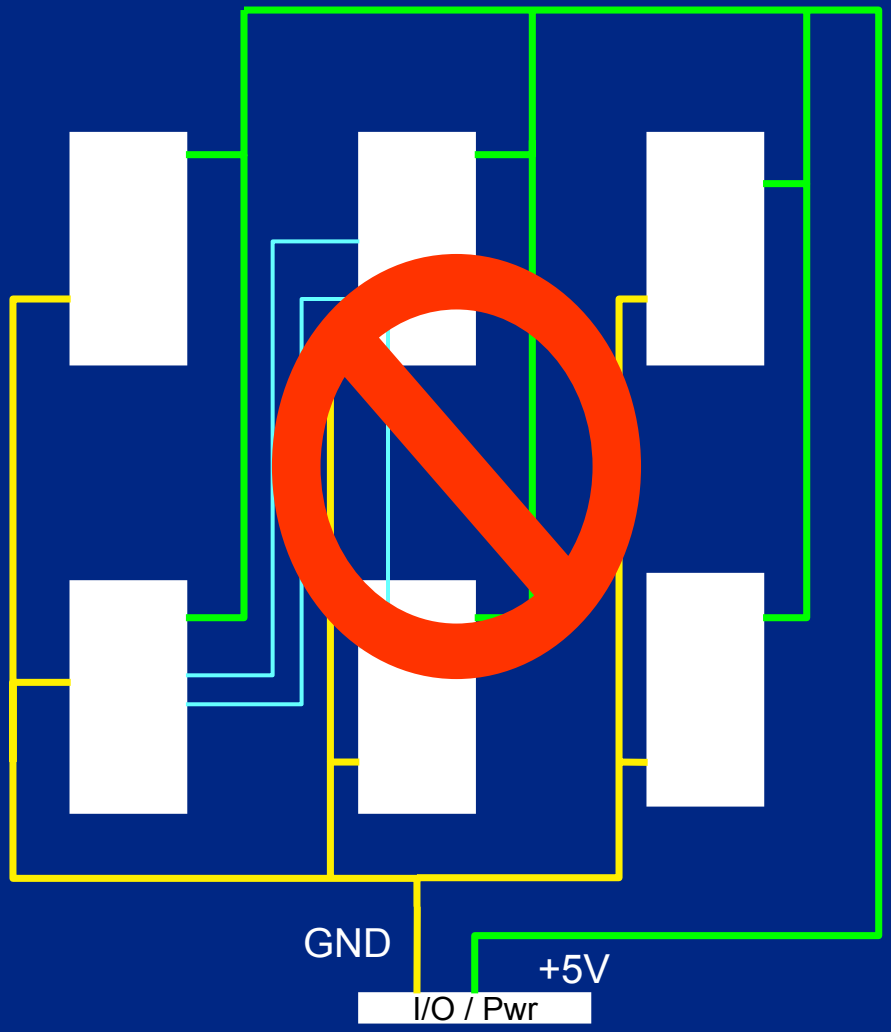
- Hybrid Ground
  - Single-point ground for analog system
  - Multi-point ground/grid for digital system
  - Capacitor for high frequency only ground
  - Inductor for low frequency only ground

Tip #2
PCB Layout - Grounding

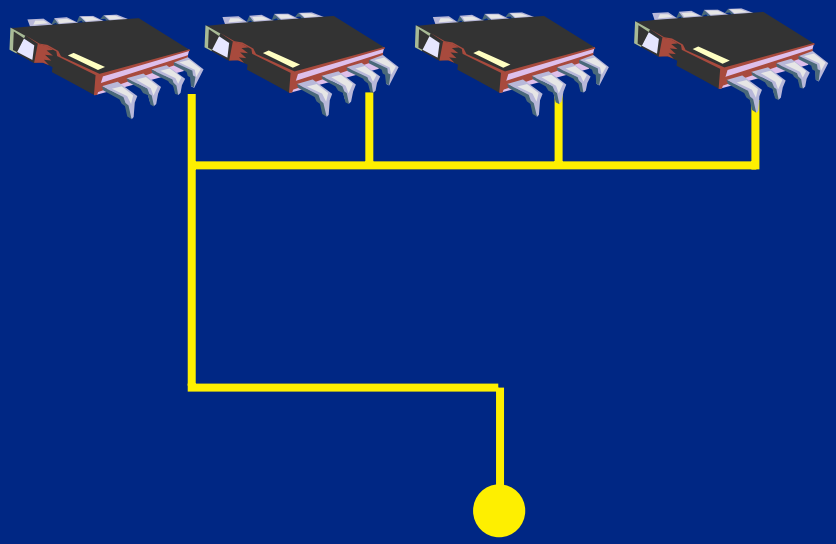


PCB Layout
Power Traces

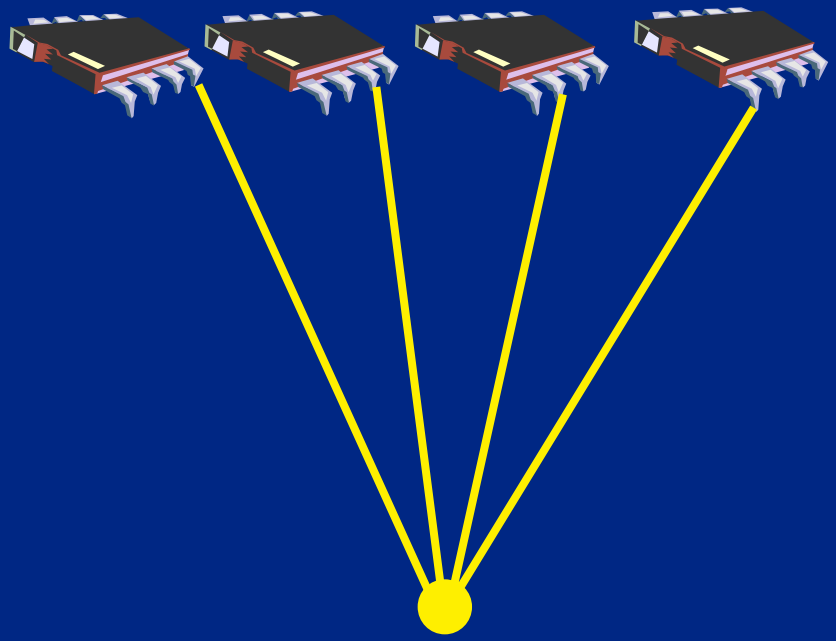
- Power Traces
  - No loops
  - Verify return paths



PCB Layout
Power lines



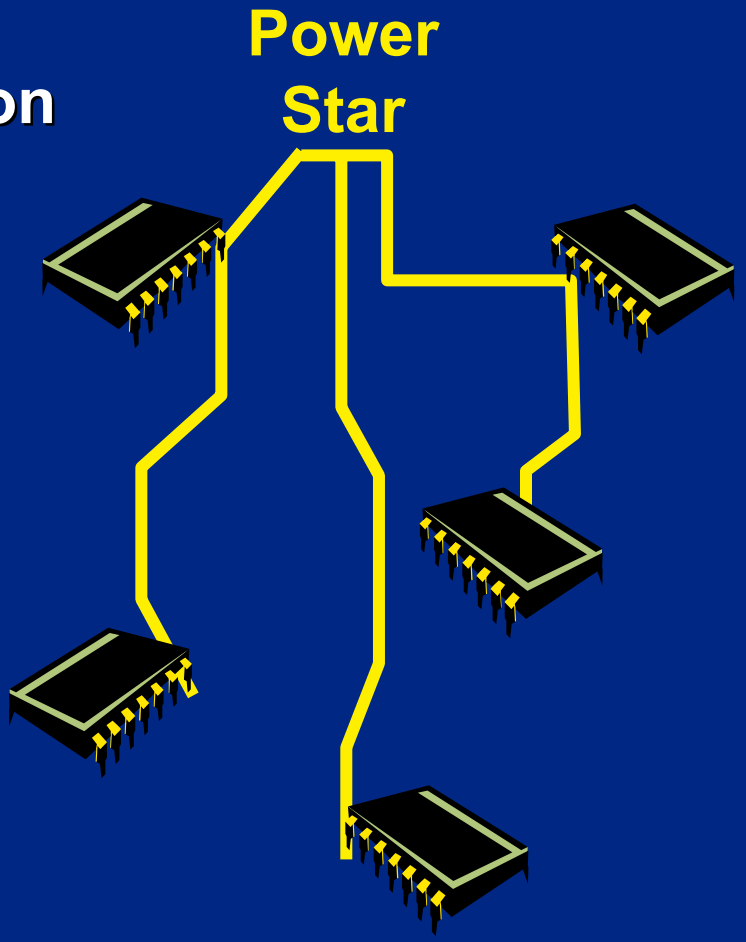
Poor- Daisy Chain



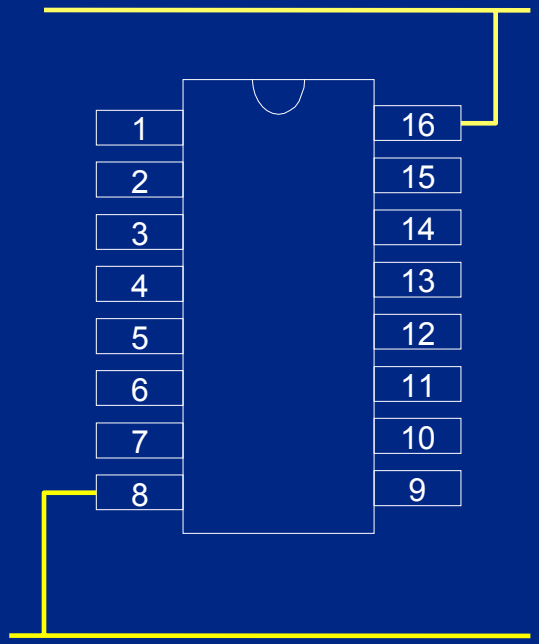
Best- Single Point

PCB Layout
Tip #3 Power Lines

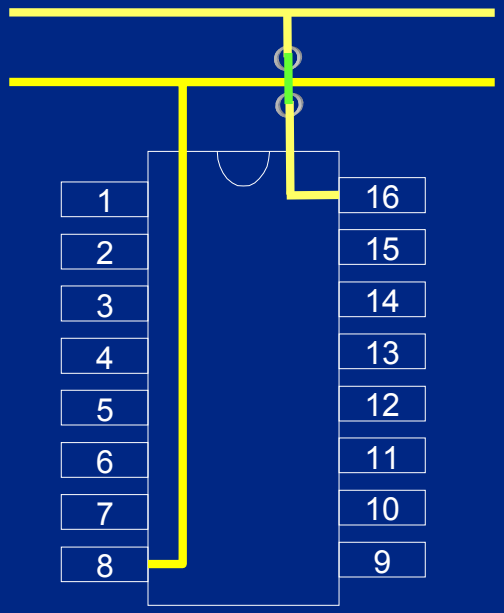
Better, Practical Solution



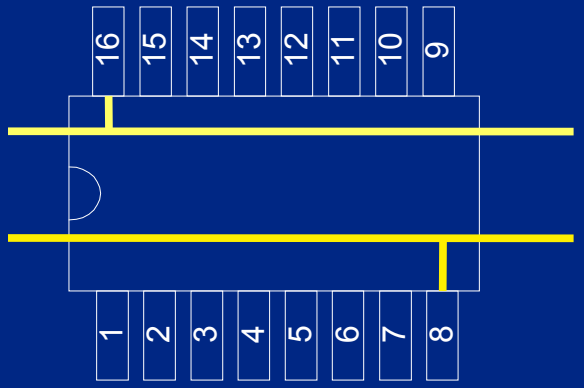
PCB Layout
Tip #4 Power Traces



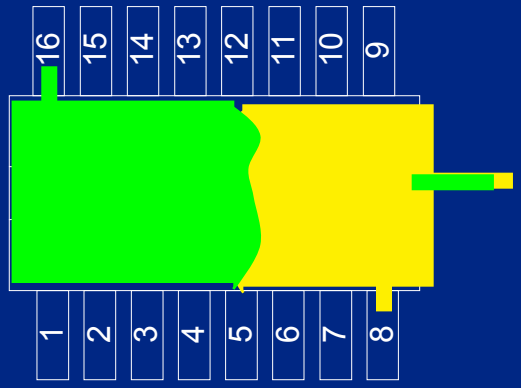
Poor



Good

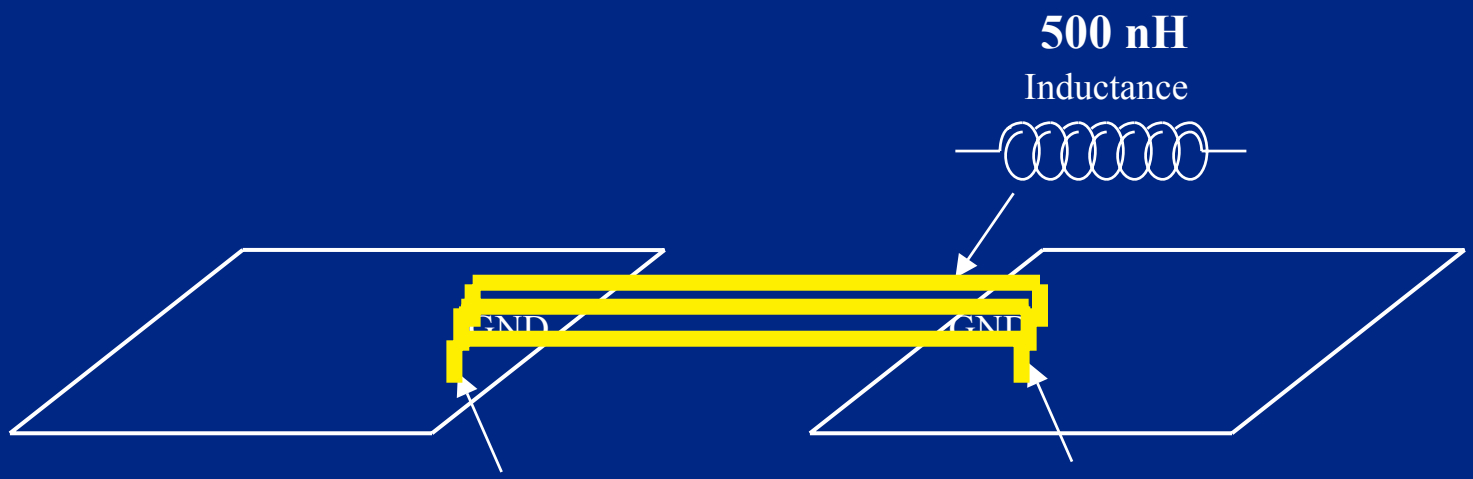


Better



Best

PCB Layout
Tip #5 Grounding
(Inter-board connection)

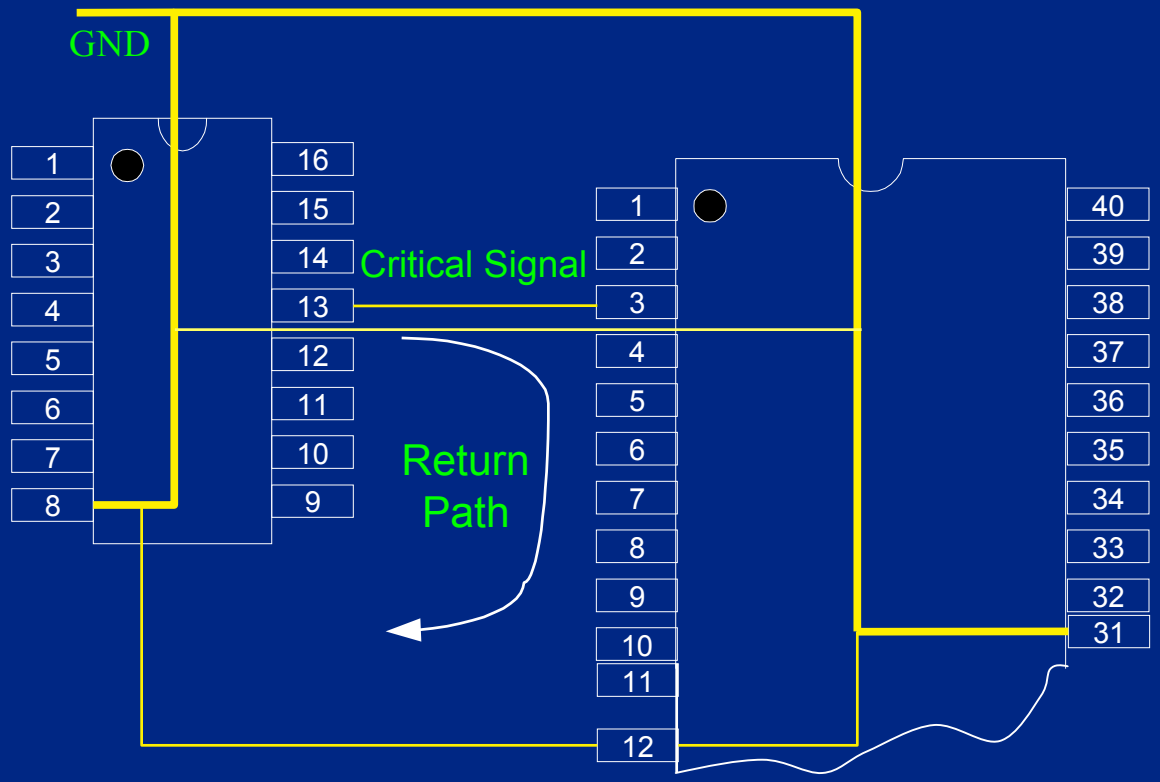


V = L di/dt

L = 500 nH, I = 10 mA, t= 5ns

V = 1 volts

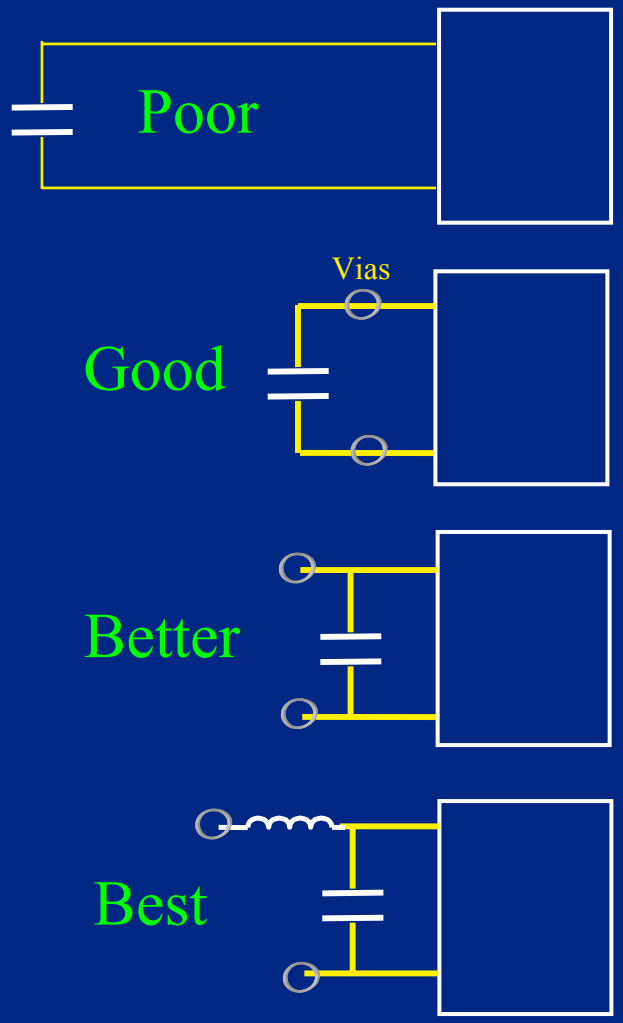
PCB Layout
Tip #6 Signal Return



Carefully route the return path of critical signal

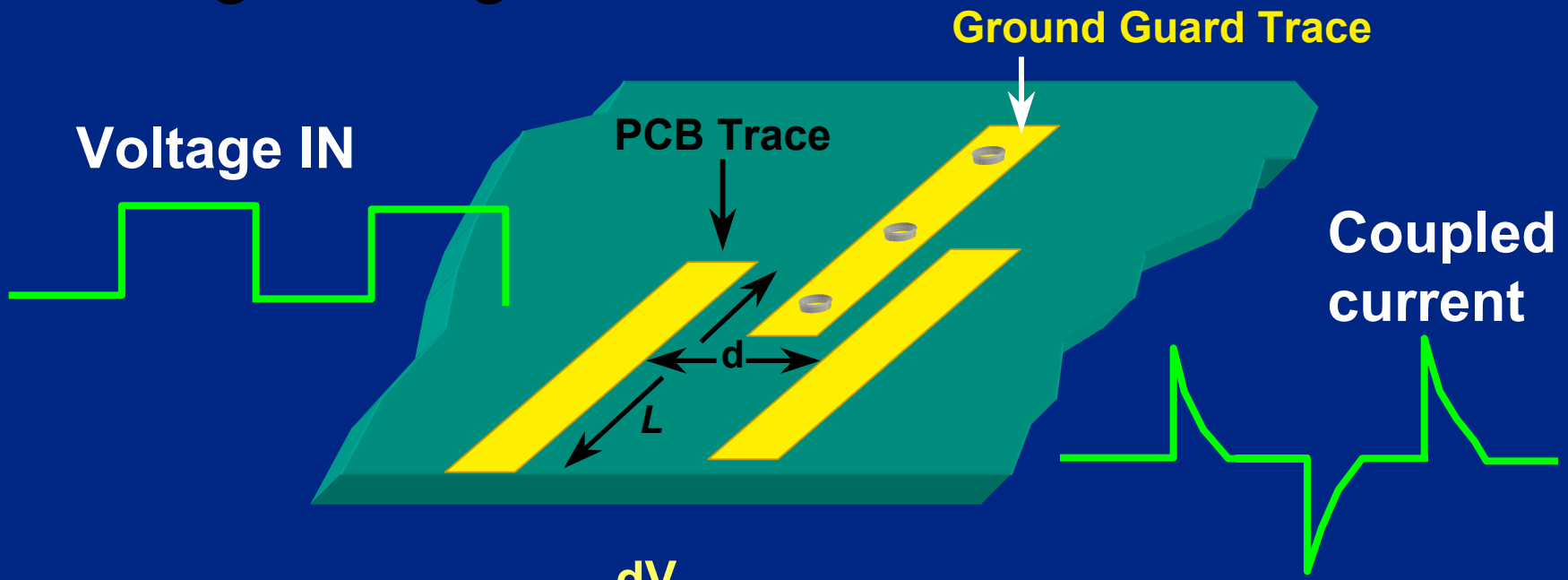
Tip #7

- Power supply decoupling



PCB Layout Tip #8 Coupling Noise

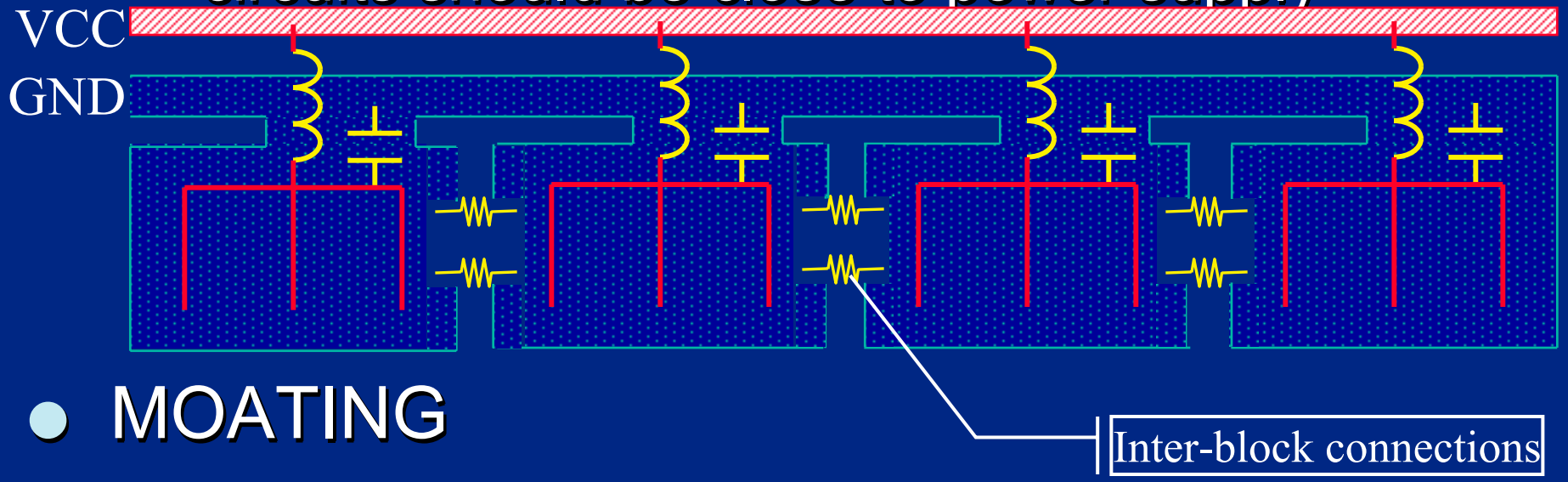
- Decrease “L” or increase “d” $C = \frac{w \cdot L \cdot e_o \cdot e_r}{d}$ pF
- Put ground guard between traces



$$I = C \frac{dV}{dt} \text{ (amps)}$$

Tip #9
PCB Layout - Circuit Segmentation

- Circuit Segmentation
  - Physically separate circuits to reduce coupling
  - High current or high switching frequency circuits should be close to power supply



- MOATING
  - Guard ring of ground

PCB Layout
Floor Planning

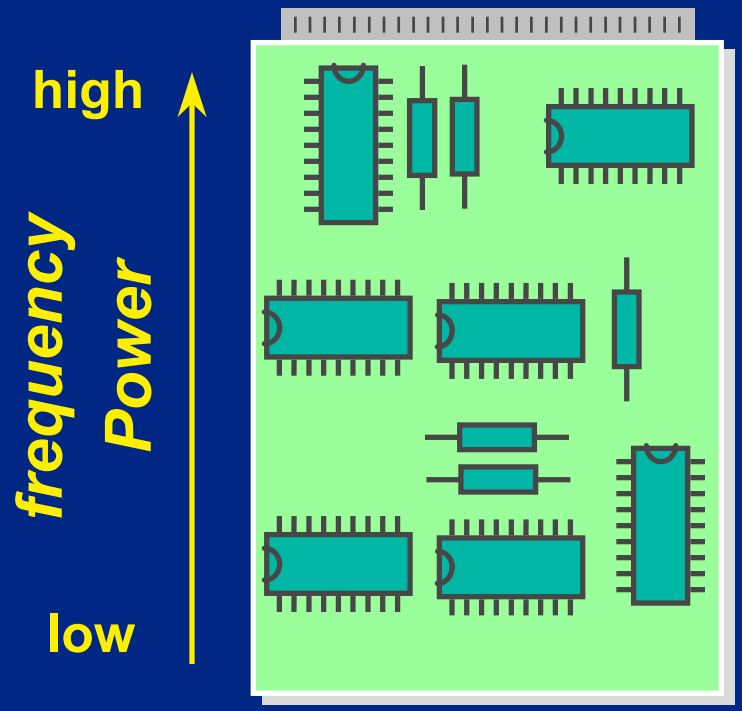
- Partition into functional areas
  - Separate different signals
    - Low frequency Vs. high frequency
    - Low power Vs. high power
  - Separate different functions
    - Analog Vs. digital
    - Supply Vs. signal
    - Power driver Vs. signal conditioning

PCB Layout
Floor Planning

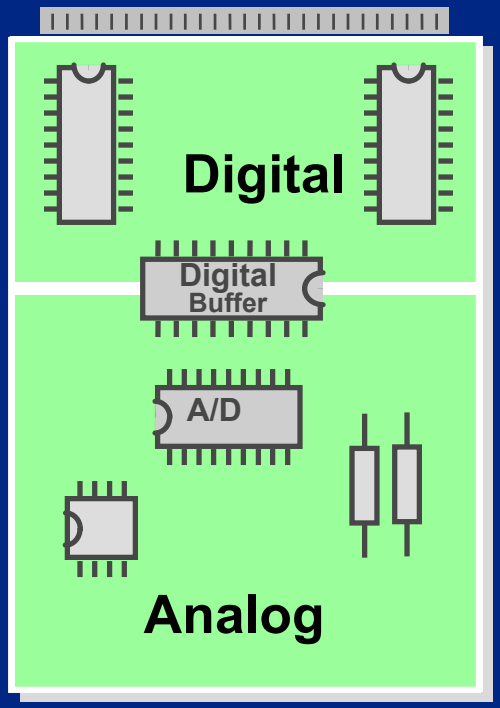
- Add isolation
  - Make high frequency signal paths
    - Short
    - Near the PCB edge connector
  - Use guard rings and traces
  - Add spacing between sections
- Do **not** use auto routers for analog/power sections

PCB Layout Tip #10 Floor Planning

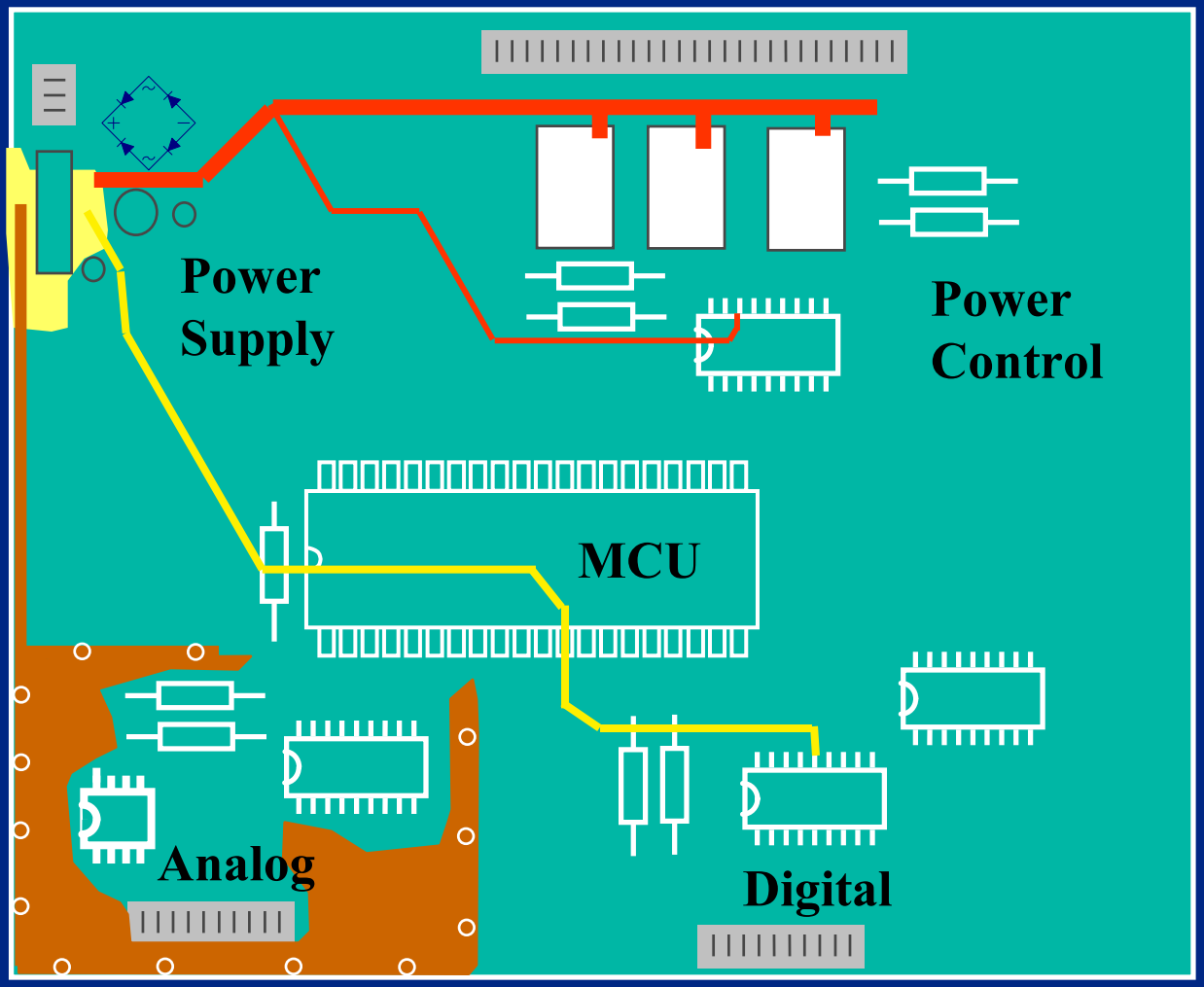
High Power/Frequency Components Placed Near Connector



Separate Digital and Analog Portions of the Circuit



Tip #11
Functional Block Placement



Tip #12a

- Use Multi-layer boards
  - One or more surface dedicated to power and ground
  - Minimizes loop areas
  - Minimizes signal return path (Lower impedance)
  - Minimizes cross talk
  - May provide 10x to 1000x improvement

Tip #12b
Two-Layer Board

- Two-layer board can achieve 95% effectiveness of Multi-layer board
  - Route GND/V_{DD} traces carefully
  - Ground plane in selective area
  - Routing of critical signals
    - Return path for critical signals
- May provide optimum Cost/Performance ratio

Tip #13
Board Design Approach

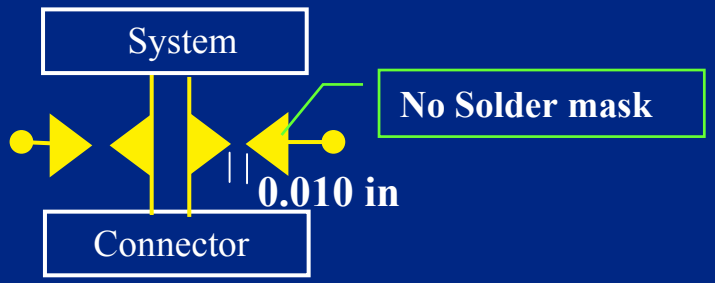
- Identify the power/ground sources and critical signals
- Partition layout into functional blocks
- Position all components with critical signal adjacent to each other
- Route power and ground traces
- Route critical signals and their return paths
- Route rest of the board

Tips & Tricks

Power Electronics

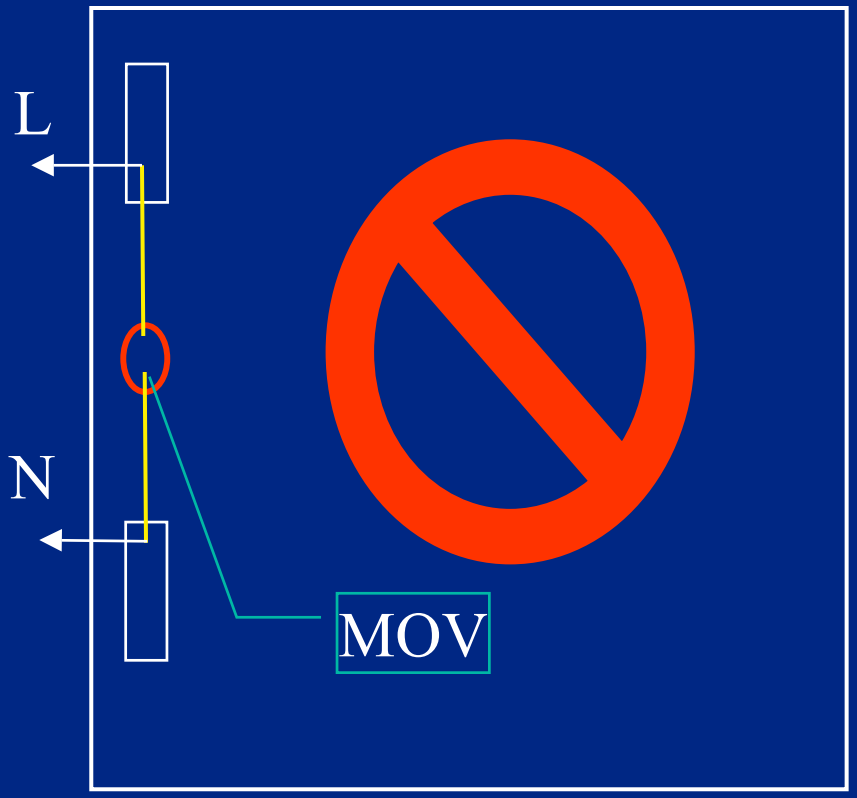
Tip #14

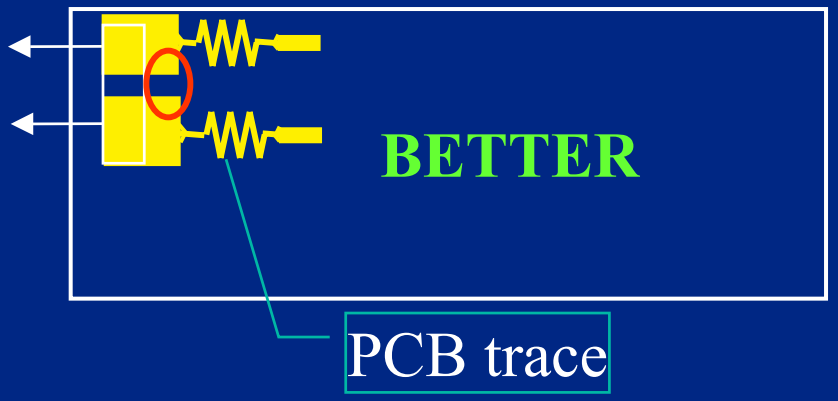
- Use a transient suppressor device
  - Large geometry zeners (TVS) are fastest
  - Multi-layer MOV works well
  - Ferrite + capacitor or RC combination can be used
  - Spark gaps



Tip #15

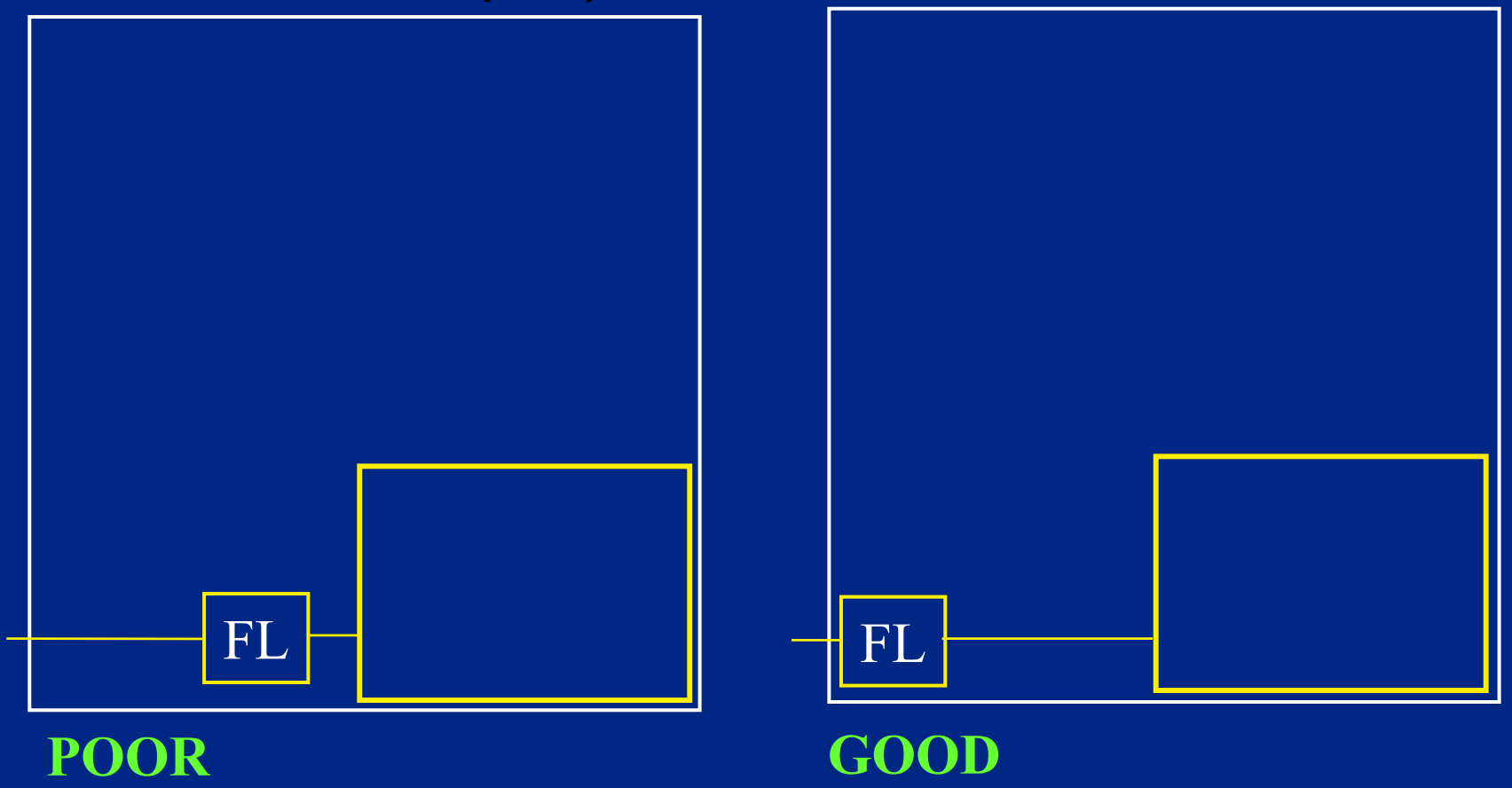
- Power entry & MOV (TS) location





Tip #16

- Power filter (FL) location



Inductive Loads

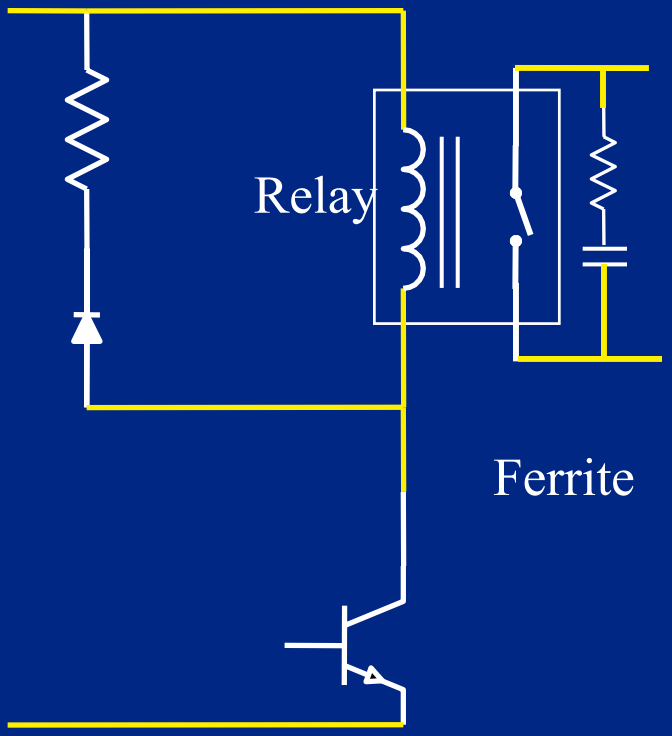
- Voltage across Inductor

$$V = L\left(\frac{di}{dt}\right)$$

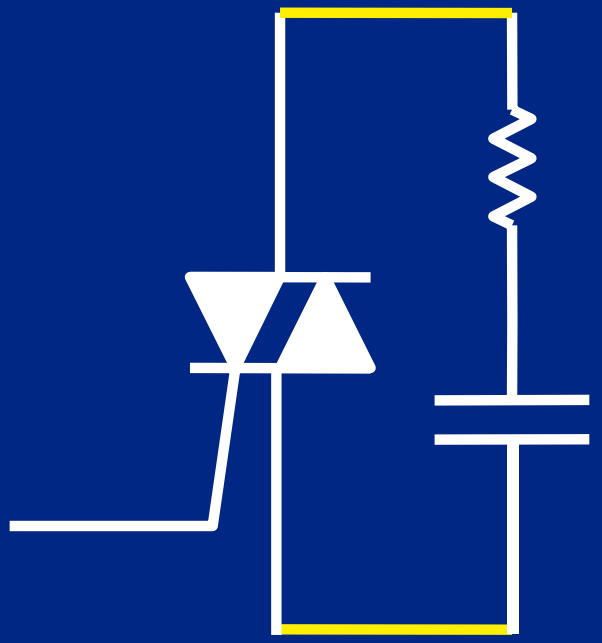
- "Inductive kick" or "Flyback"

Tip #17

- Use Snubber

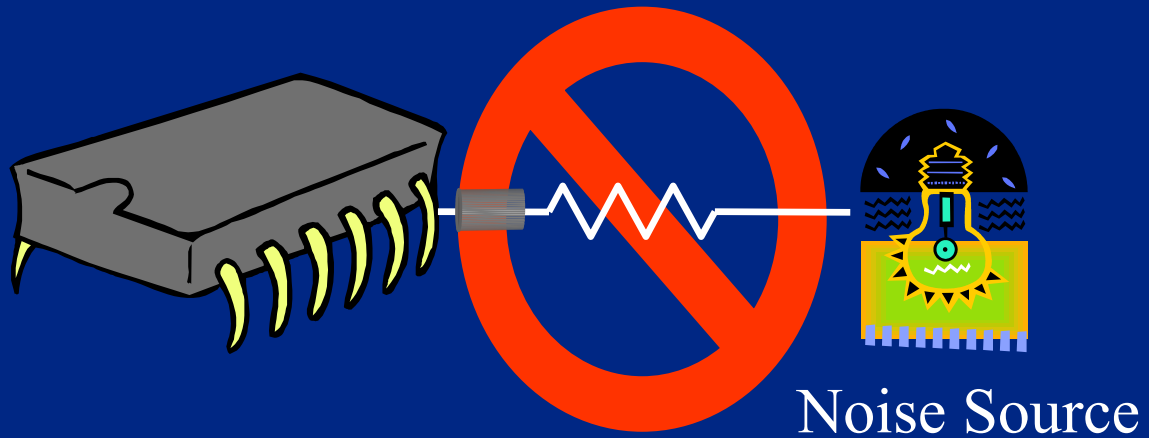


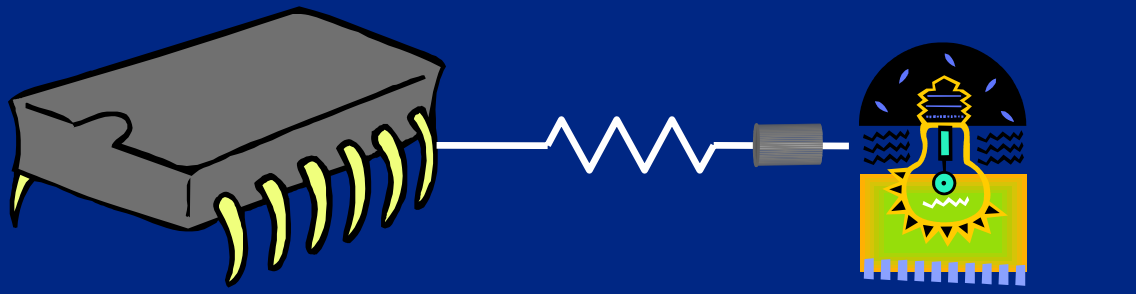
Voltage Snubber with Relay



Voltage Snubber with Triac

Tip #18
Ferrite Bead Placement



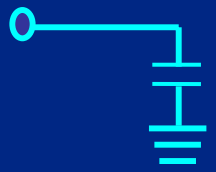


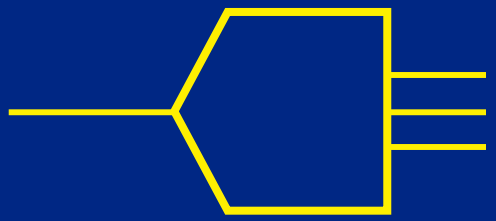
Tips & Tricks

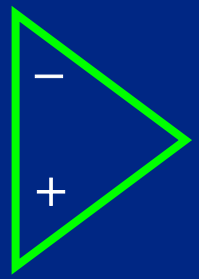
Analog

Device Noise

- Passive devices
  - Resistors
  - Capacitors
  - Inductors
  - Ferrite Beads
- Active devices
  - Operational amplifiers
  - Voltage references
  - Voltage regulators
  - A/D and D/A Converters







Passive Device Noise

- Resistors
  - Johnson or Thermal Noise
  - $V_{RN} = \sqrt{4KTR(BW)}$ {Vrms}
    - K = Boltzman's Constant = 1.38e -23 JK^{-1}
    - T = Temperature in Kelvin
    - R = Resistance in Ohms
    - (BW) = Noise Bandwidth in Hz
- Capacitors - Negligible
- Inductors - Negligible
- Ferrite Beads - Negligible

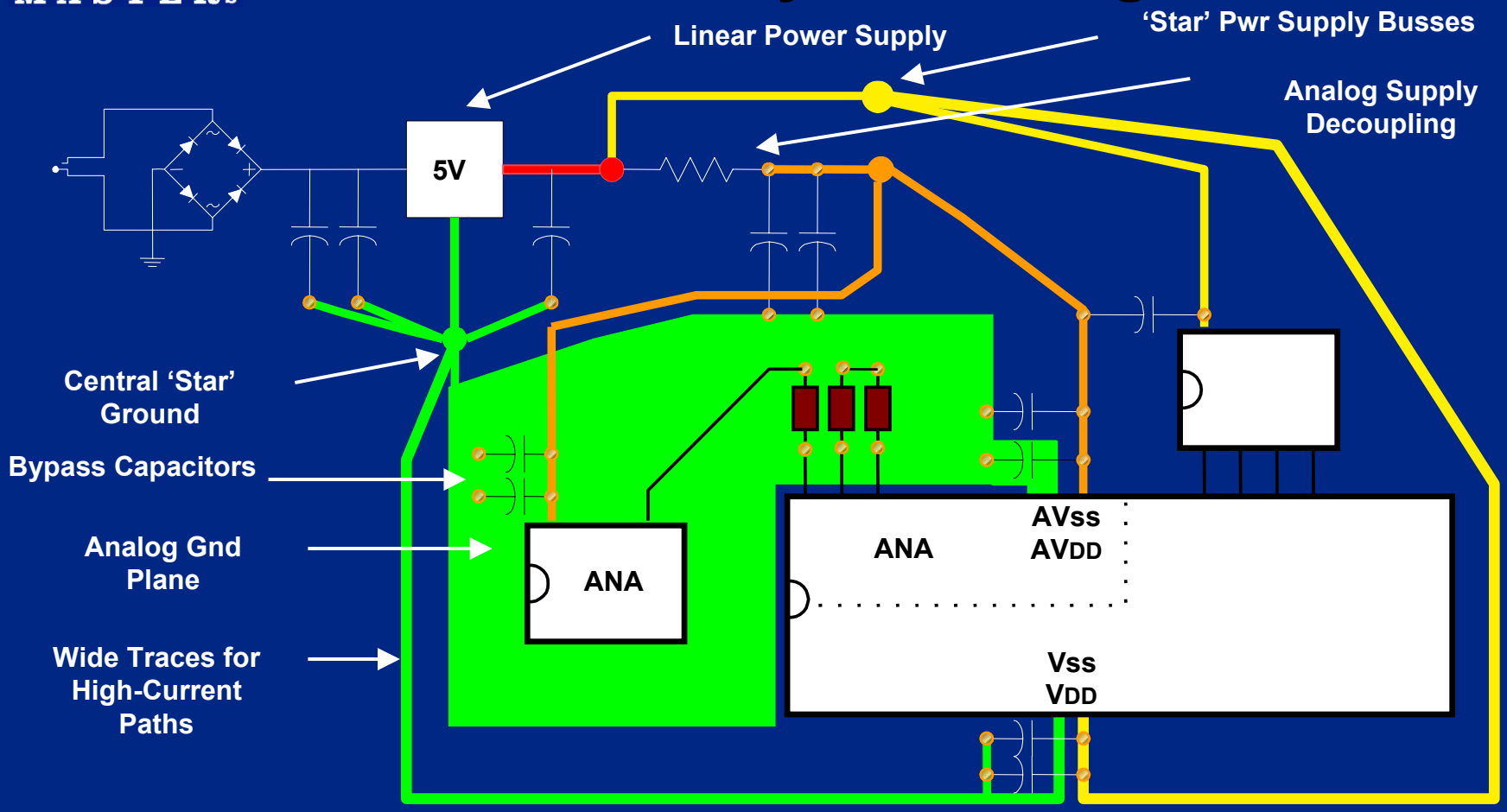
Tip #19
Reducing Device Noise

- Passive Devices
  - Resistor- Choose lower value resistors
- Op Amps
  - Use lower noise devices if needed
- A/D Converters
  - Select a converter with higher accuracy
    - Remember accuracy vs. resolution issues
  - Keep input frequency bandwidth below one quarter of the sampling frequency

Tip #20

- Use a Shield Cable for sensors & sensitive signals
  - Suggested ground for sensor I/P

Tip #21
PCB Layout Analog Section

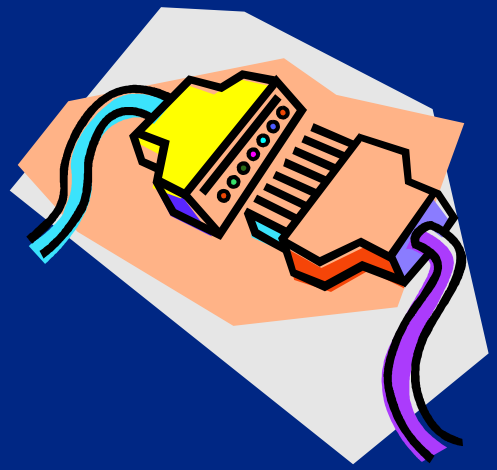


Noise in the Analog World

- The Noise will NEVER be Equal to Zero
  - Implement Your Layout Wisely
  - Choose Your Devices Carefully
  - Know the Environment
- Noise Reduction Rules of Thumb
  - Bypass, Bypass, Bypass!!!!!!
  - Always Implement a Ground Plane
  - Examine Current Return Paths
  - Choose Resistors Less than 100K
  - Band Limit the Analog below Nyquist/2

Tips & Tricks

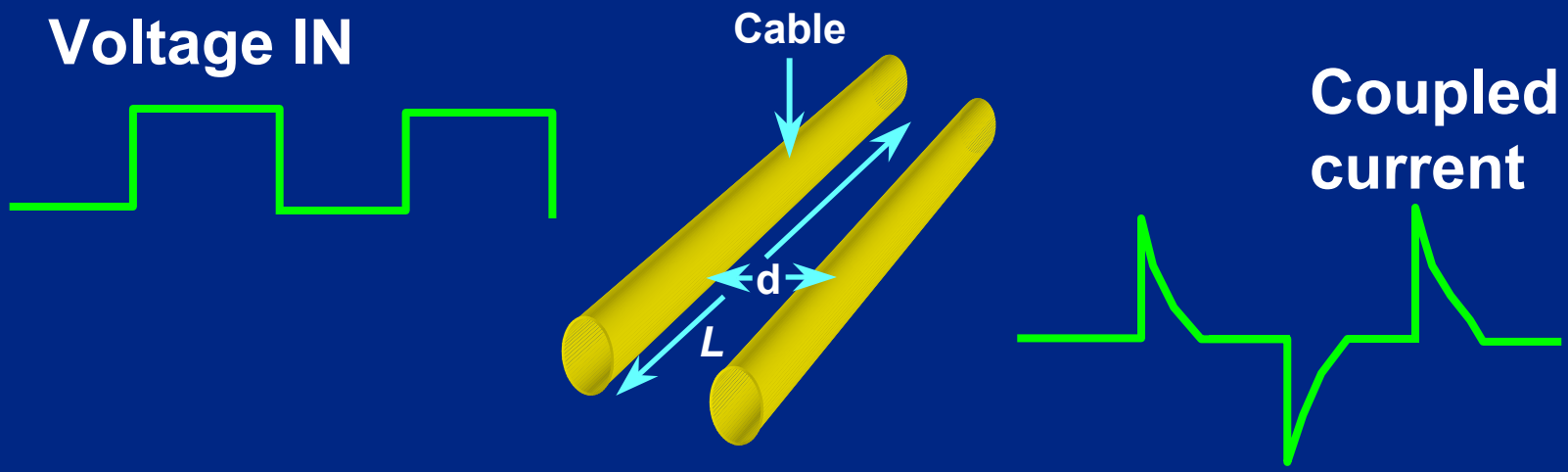
Connectors



Tip #22
Cable Harness Coupling Noise

- Decrease “L” or increase “d”

$$C = \frac{w \cdot L \cdot e_o \cdot e_r}{d} \quad pF$$



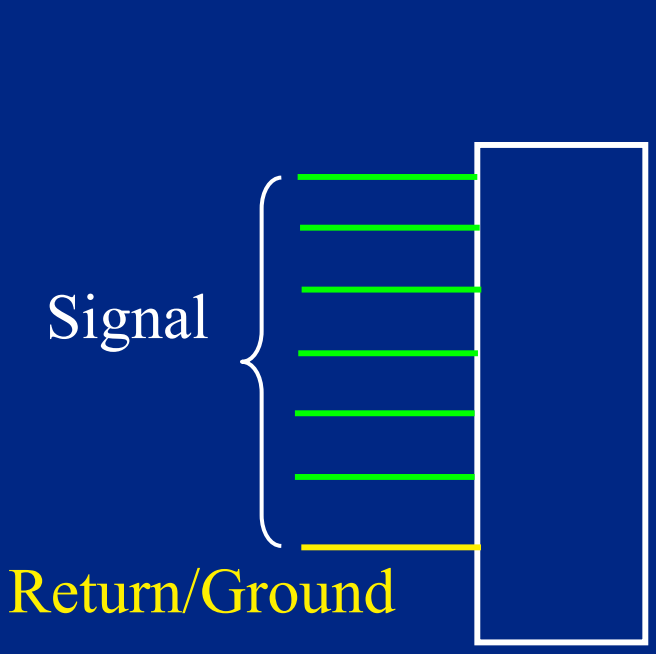
$$I = C \frac{dV}{dt} \text{ (amps)}$$

Tip #23
Cable Harness

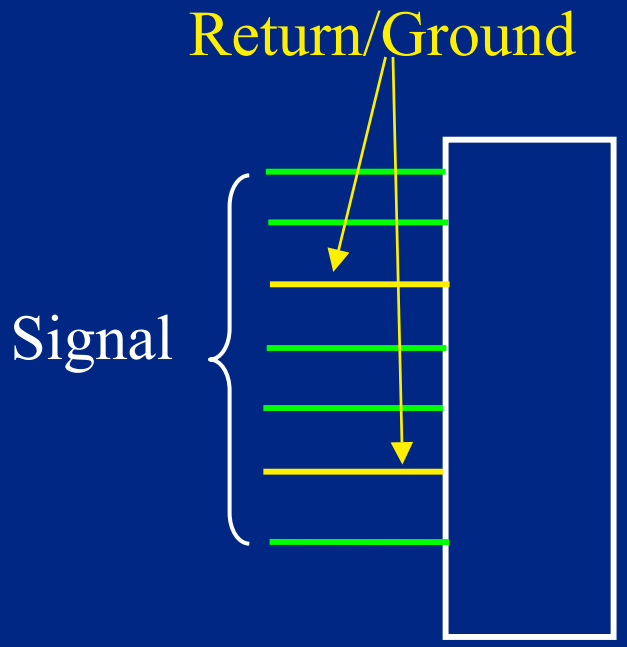
- Shield wires for sensitive signals
- Twisted wire pairs for analog
- Separate cable harness
  - Analog and inputs
  - Power control signals
- Ground return wires

Tip #24

- Connector
  - Total # of return line depends on speed



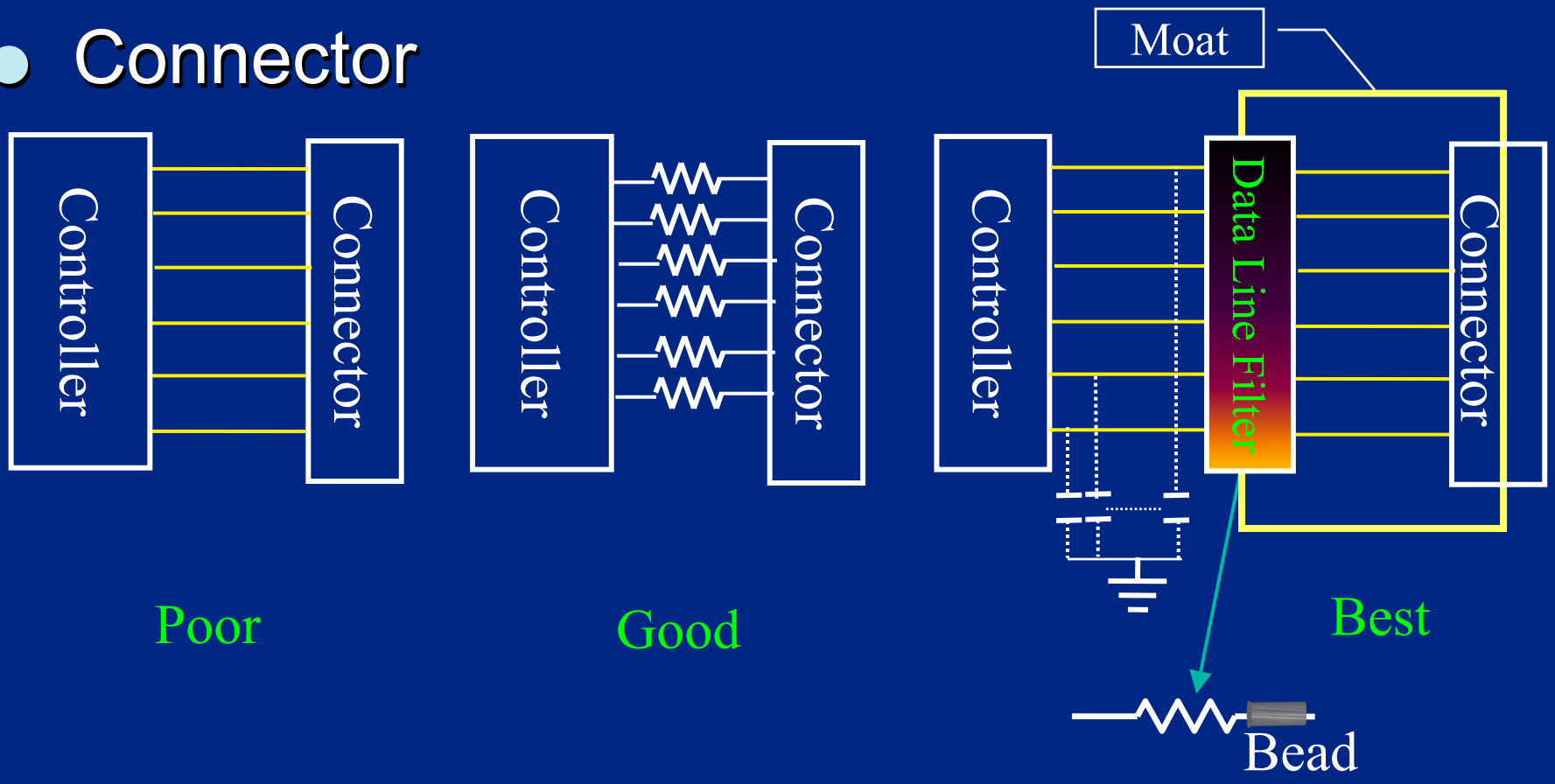
Poor



Better

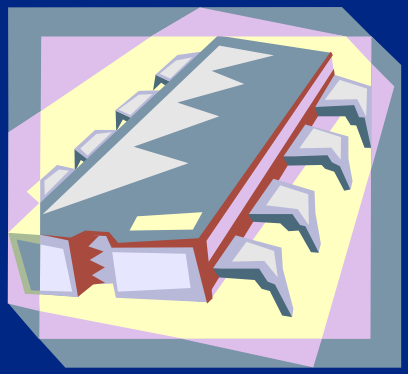
Tip #25

- Connector



Tips & Tricks

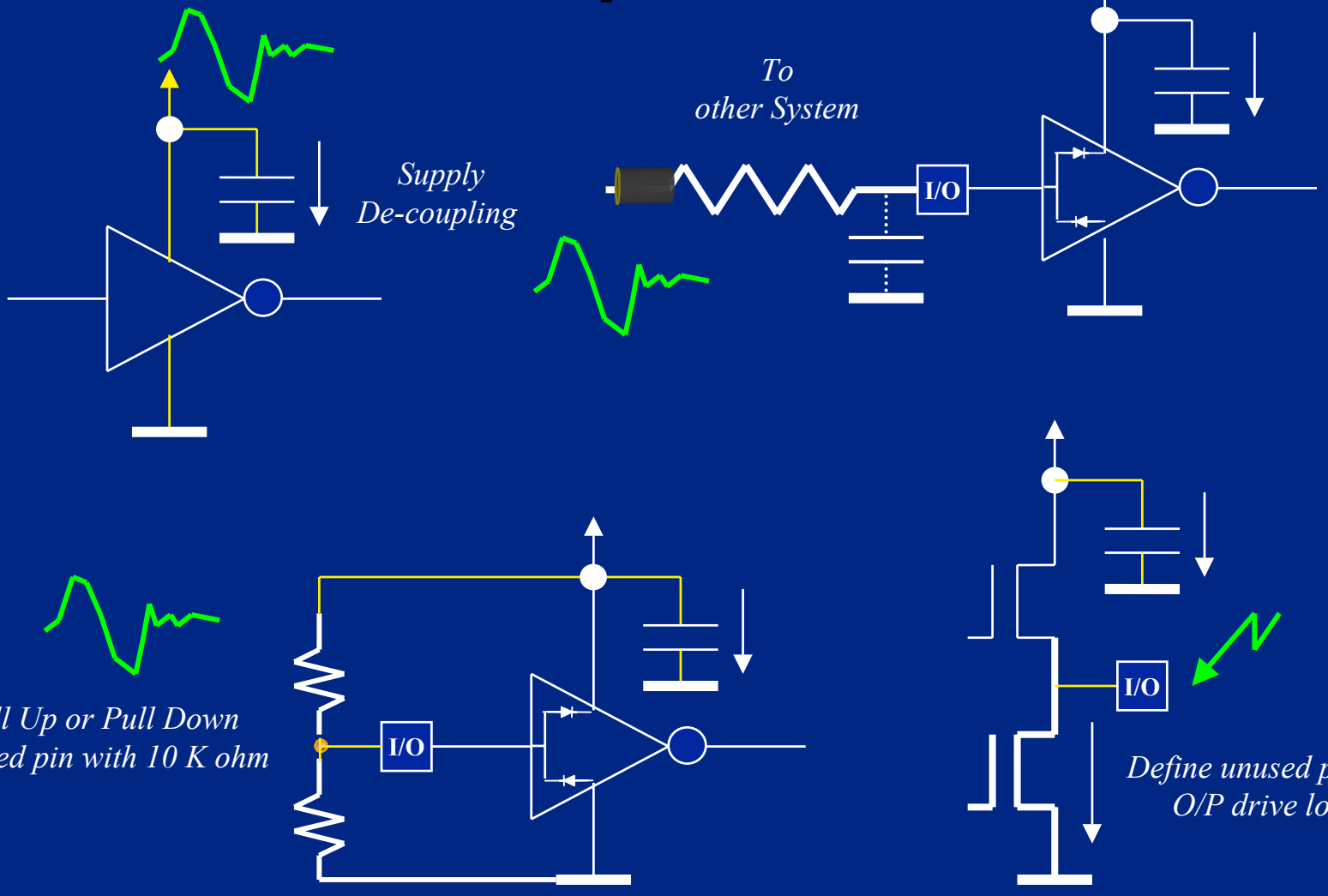
Microcontroller Circuits



Microcontroller Circuits

- I/O pins
- Interrupt pins
- Reset pin
- Power supply
- Oscillator
- Brown Out Reset (BOR)
- Watch Dog Timer (WDT)

Microcontroller Circuits
Tip #26 I/O Pins



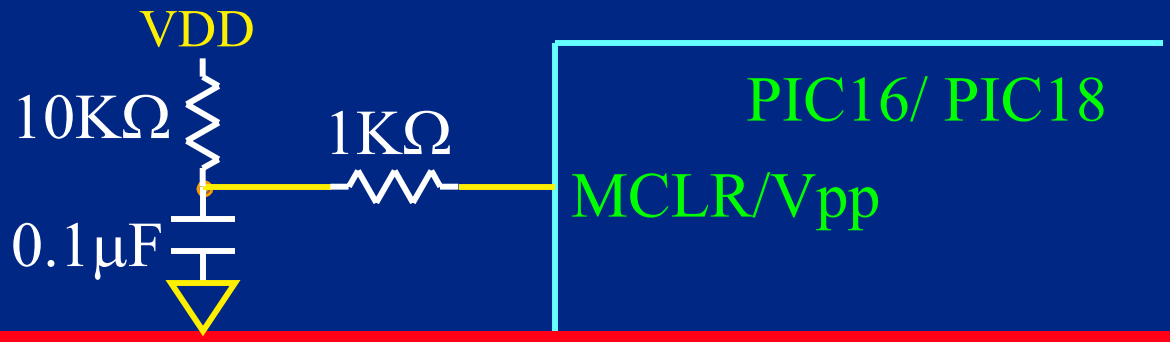
Microcontroller Circuits
Tip #27

- Interrupt Pins
  - Edge triggered interrupts susceptible to noise
  - Use level triggered type or sample interrupt pin inside ISR

  - Use line terminations to reduce reflections, ringing or overshoot which can cause false interrupts
  - Carefully route connections to interrupt traces/pins to reduce cross-talk

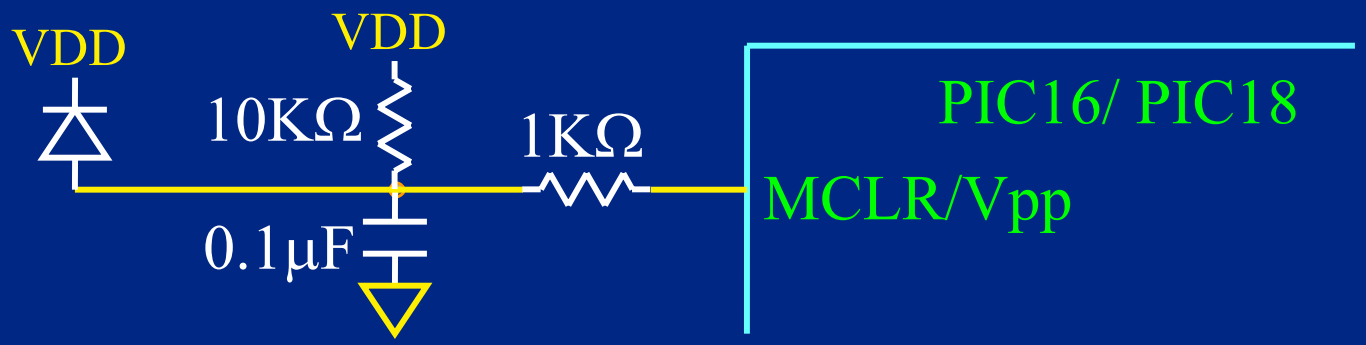
Microcontroller Circuits
Tip #28

- Reset Pins
  - A series resistor to limit the amount of current entering the MCLR pin due to ESD or EOS
  - A decoupling capacitor to attenuate high-frequency noise
  - Recommends pull-up resistor to VDD of <40 KΩ



Microcontroller Circuits

- Reset Pins
  - MCLR is also VPP for programming
  - If not performing In-circuit Serial Programming™ of the device in circuit, add diode to VDD for additional ESD protection

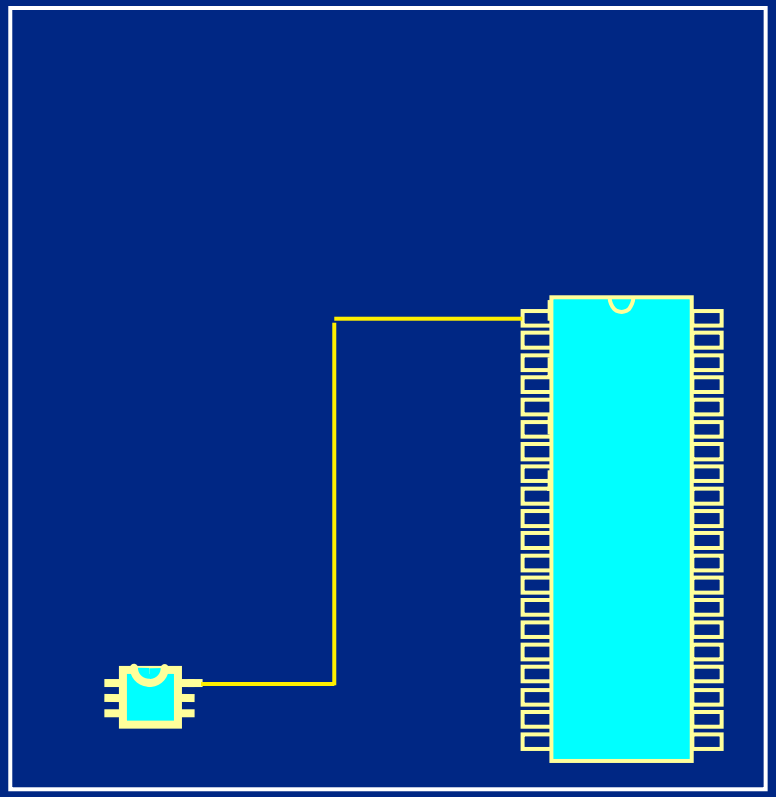


Microcontroller Circuits

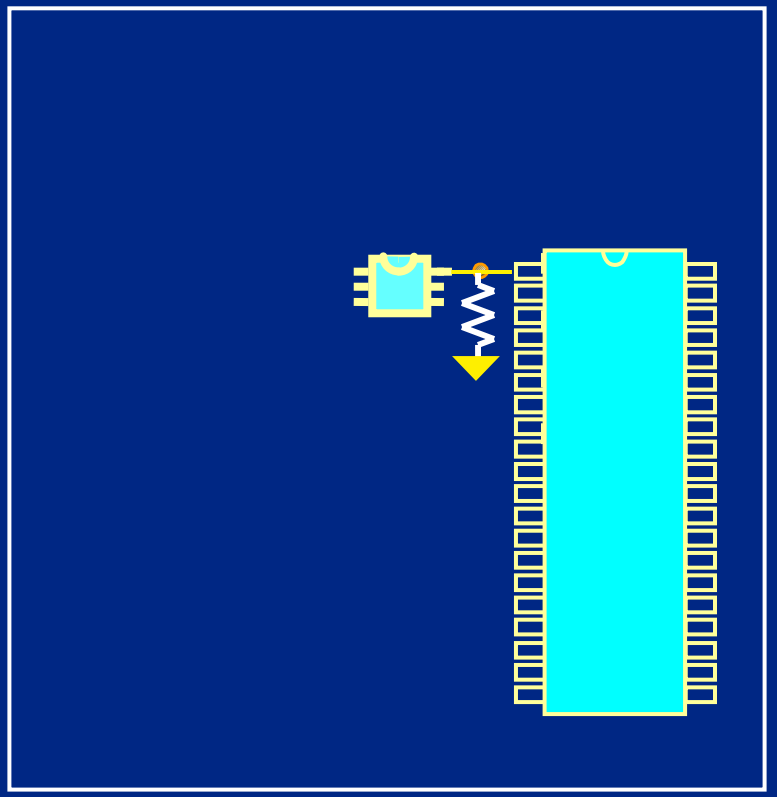
- Reset Pins
  - Some devices have a fuse setting to disable MCLR
  - If MCLR functionality is not required then disable it
  - If MCLR disabled then...

Microcontroller Circuits Tip #29

- External Watch Dog/Reset Control



POOR



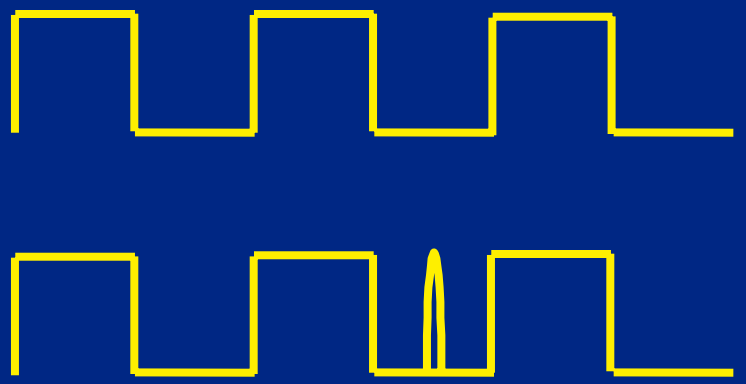
GOOD

Microcontroller Circuits

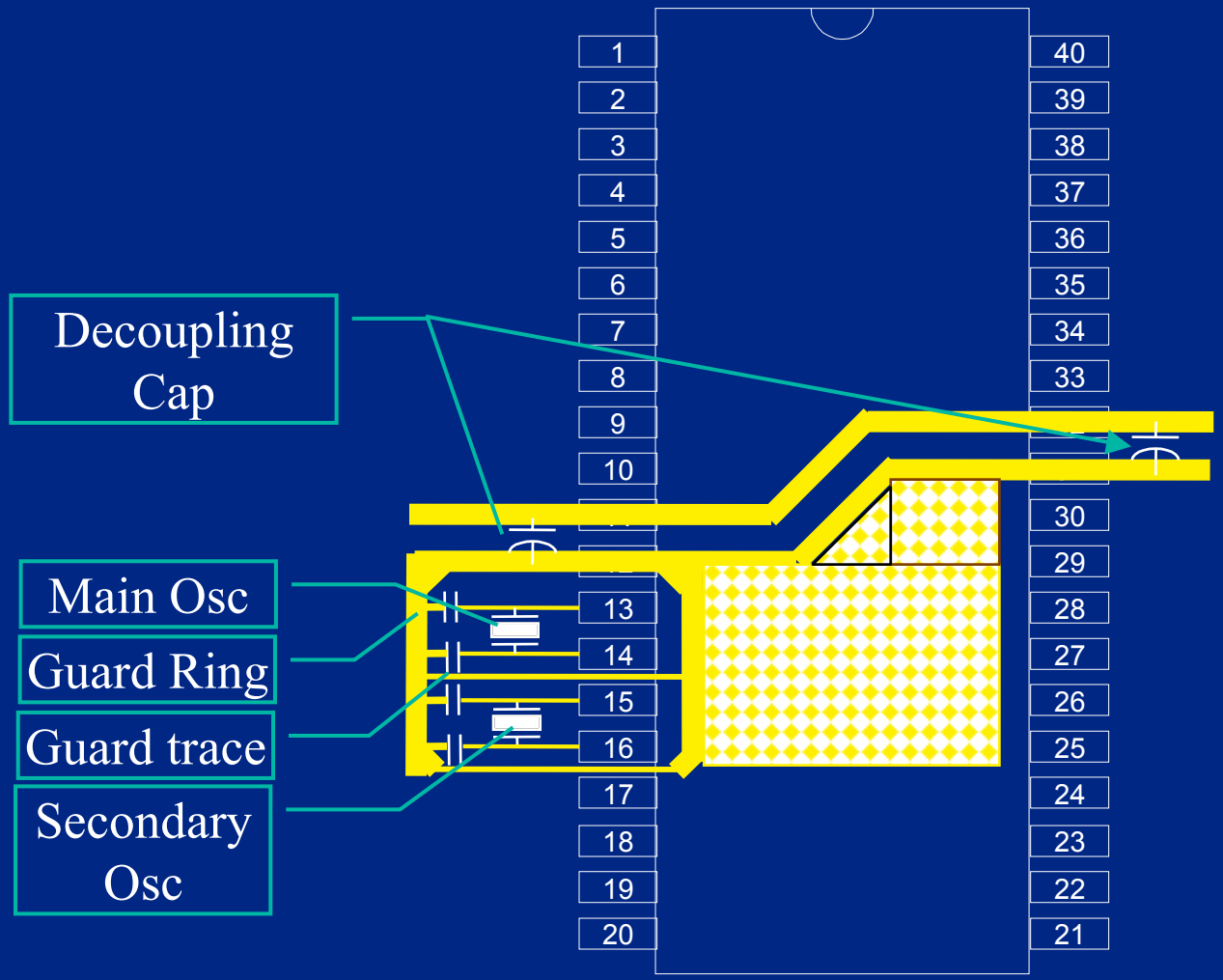
- Power Supply
  - Any noise on the power supply will enter all circuits on the board
  - Must have adequate decoupling caps AND bulk charge storage caps

Microcontroller Circuits
Oscillator

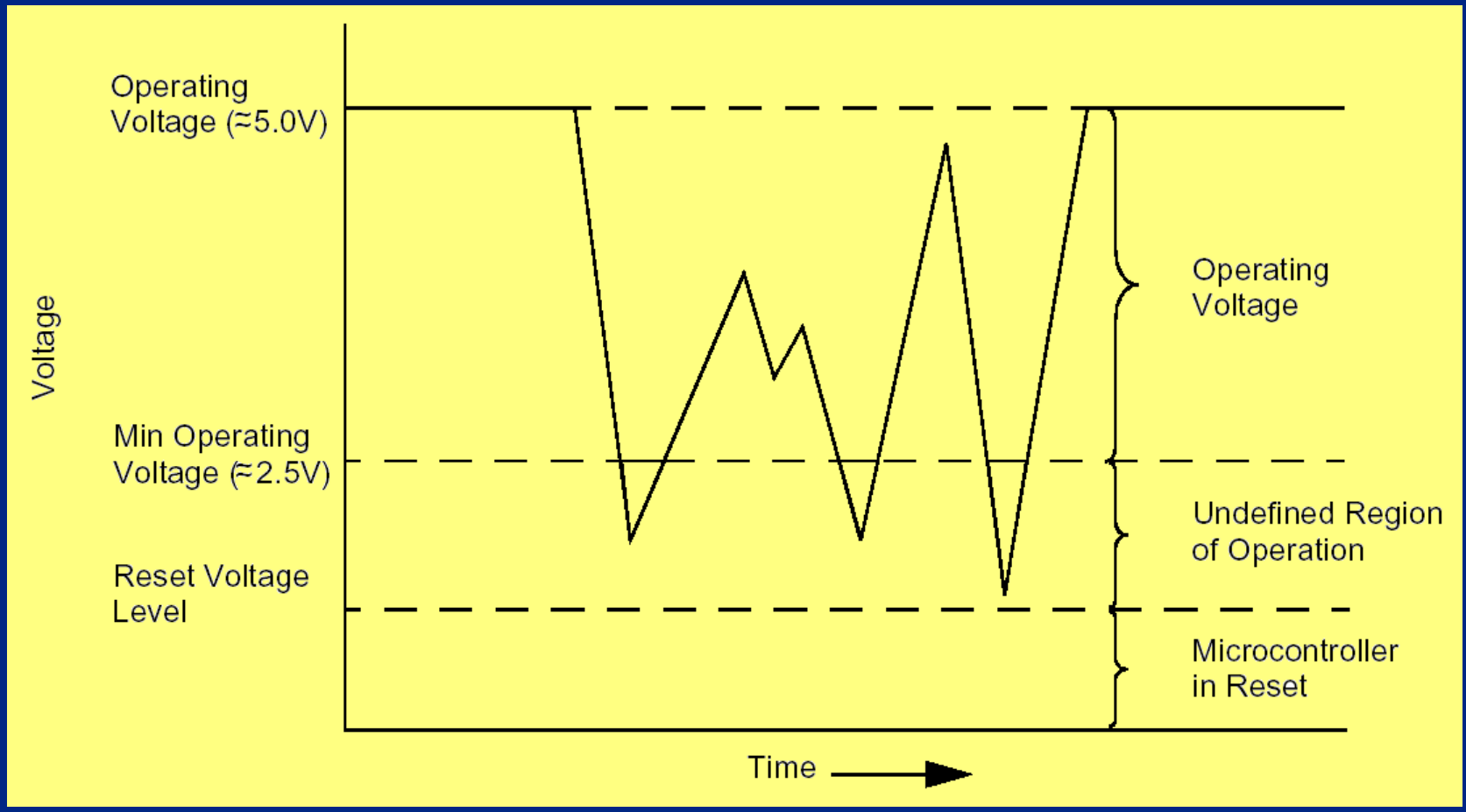
- Oscillator
  - Oscillator circuits are generally high-impedance
  - Susceptible to high-frequency signal cross-talk or noise
    - Can induce jitter, out of spec duty cycle or complete oscillator failure



Suggested Layout for PICmicro® MCU, Tip#30



Brown-Out Condition



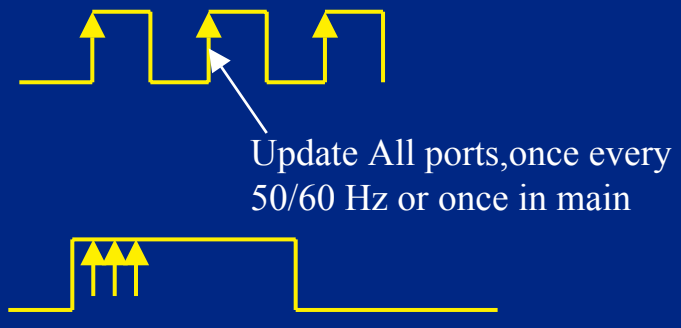
WDT protection from Brown Out

- Enable WDT
- Reset system only through WDT reset
- Use CLRWDT instruction once, and only once
- Fill all unused locations with "`goto $`" traps

Defensive Software

Tip #31

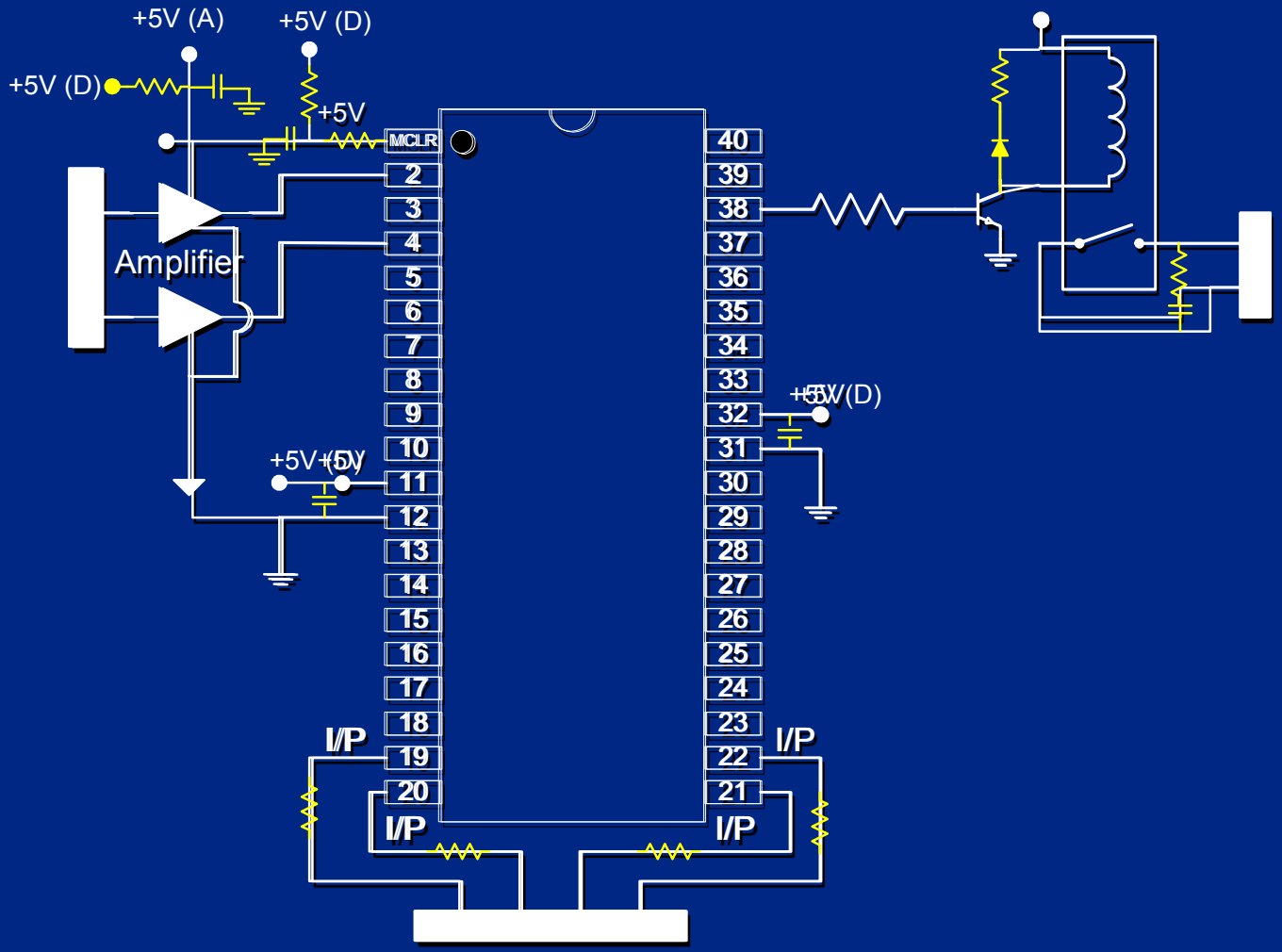
- Periodic refresh of ports
- Polling inputs
- “Noise Proof” input scan
- Token passing or subroutine counters
- Reset based recovery
  - Simple State Machine



Defensive Software
Tip #32

- Use the watchdog timer
  - Known reset loop
  - Fill unused memory with "`goto $`"
- Calculate program memory checksums

Putting it together...



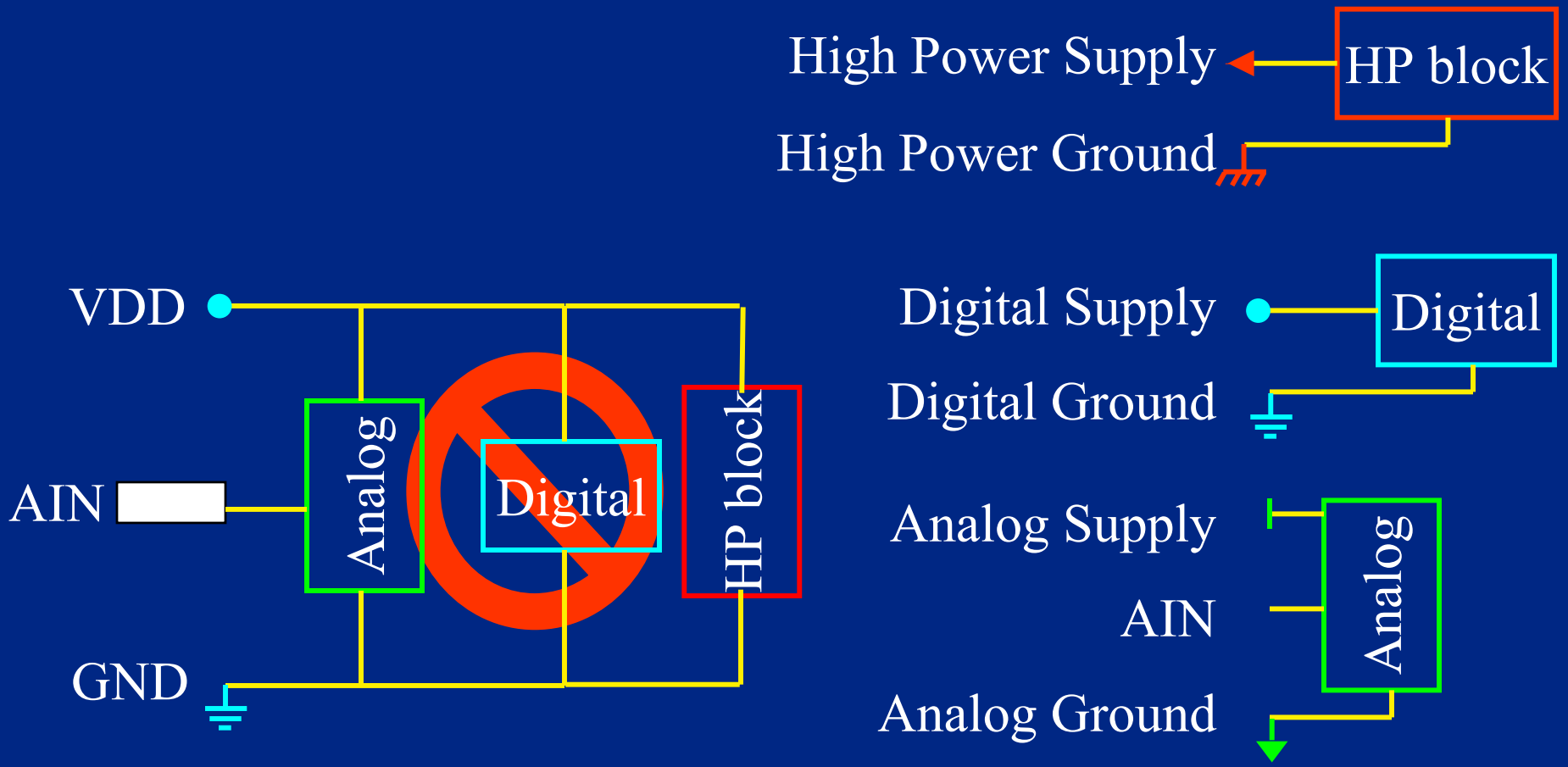
Summary

- IEC 61000-4-4 is a common system-level standard for EFT/ Burst
- IEC 61000-4-2 is a common system-level standard for ESD
- Many other standards are similar to this
- Various systems require various levels of protection

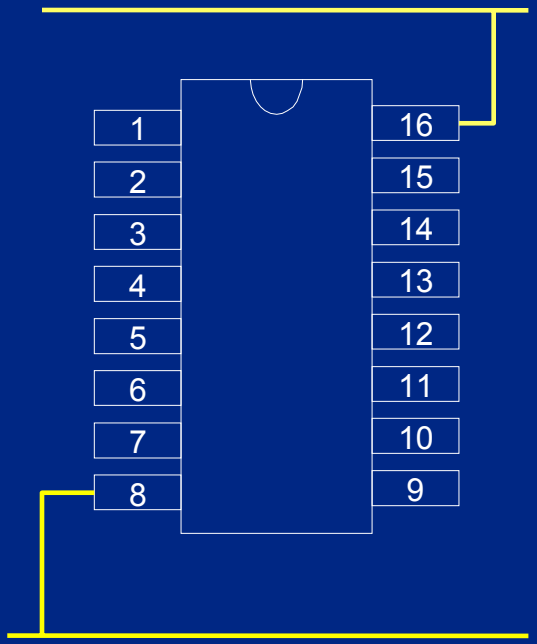
Summary

- Reviewed tips & tricks to improve the system susceptibility against EFT/ESD
- PCB layout and component selection is very important
- Many fixes for EFT & ESD helps for other EMC issues

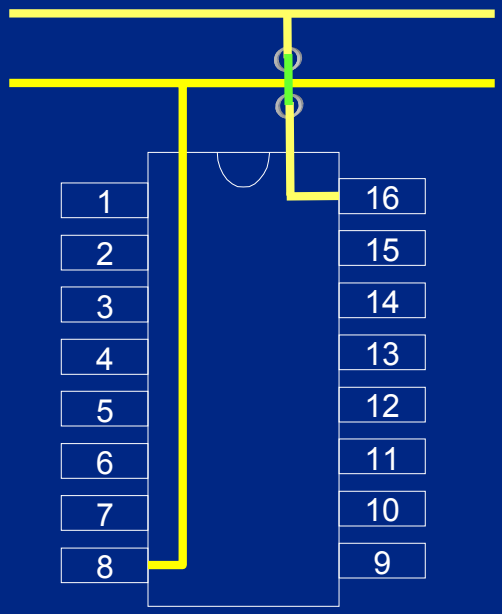
Top Fixes
PCB Layout - Grounding



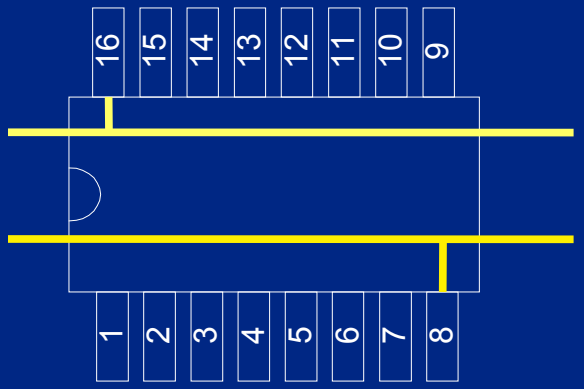
Top Fixes
Power Traces



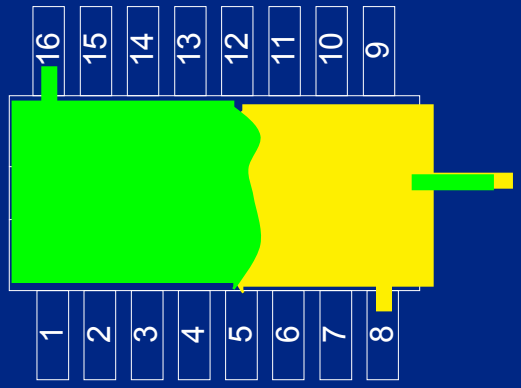
Poor



Good

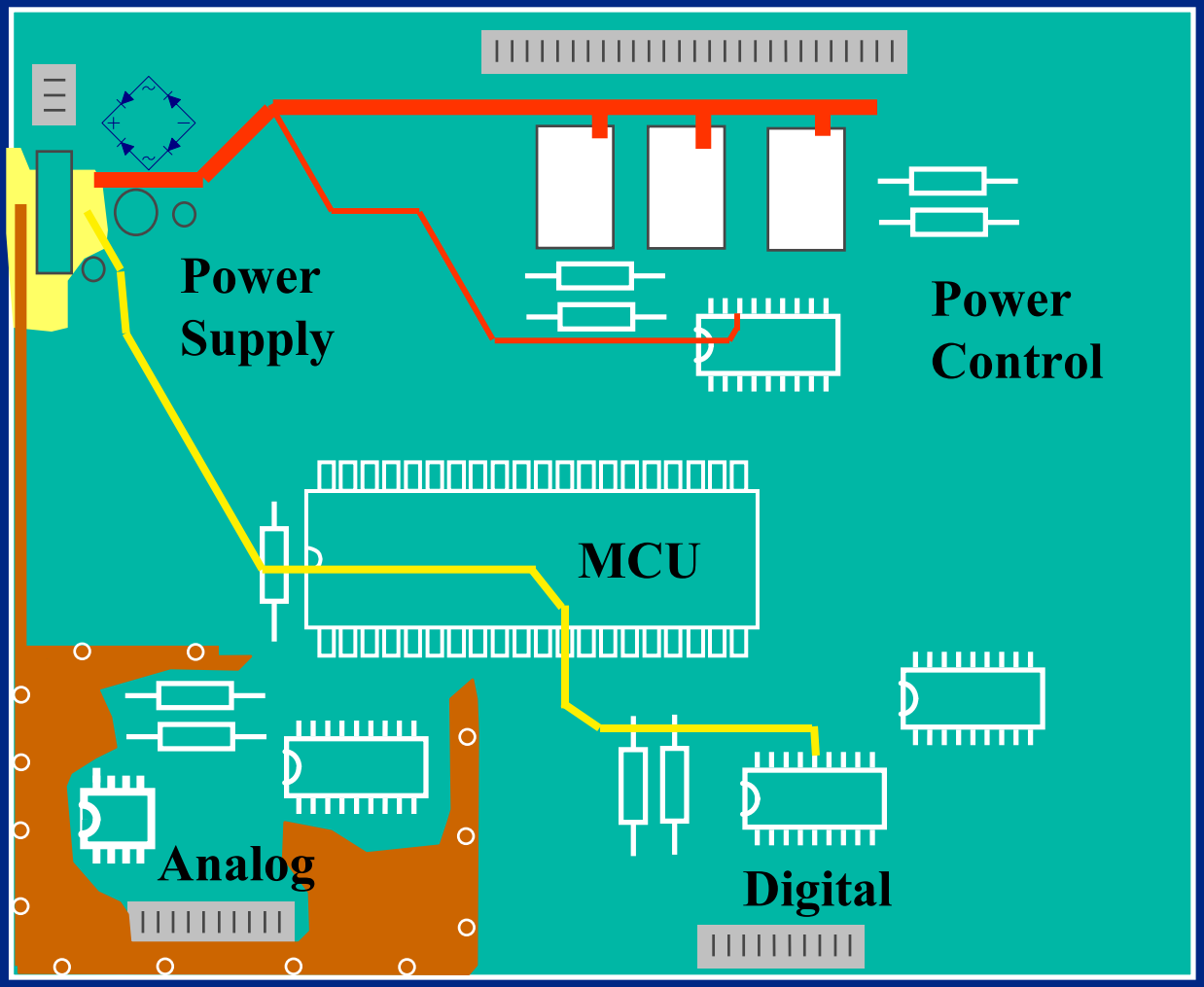


Better



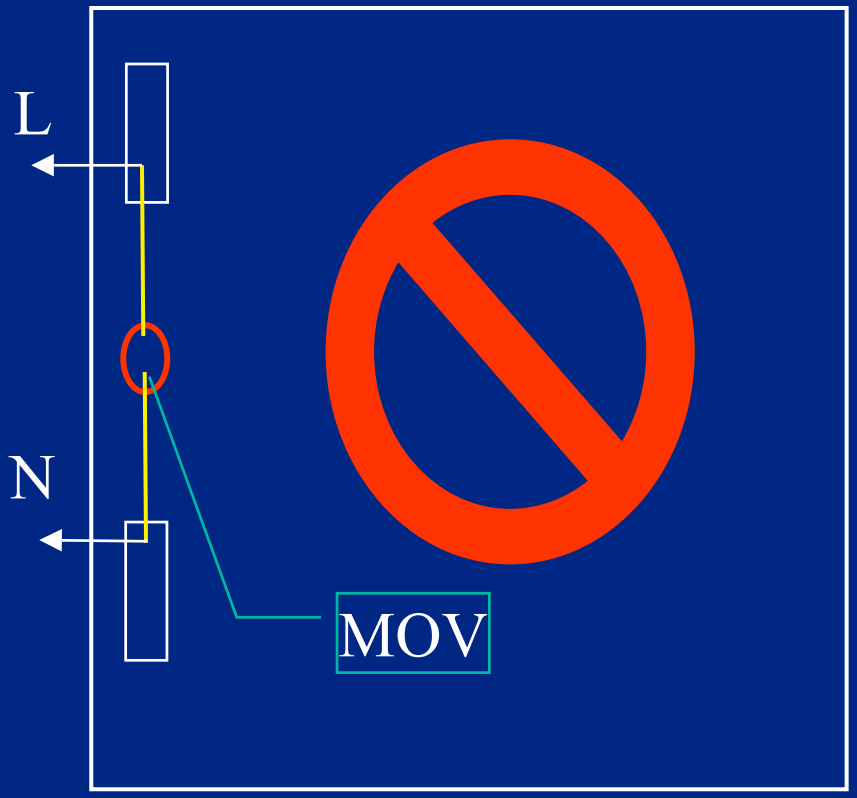
Best

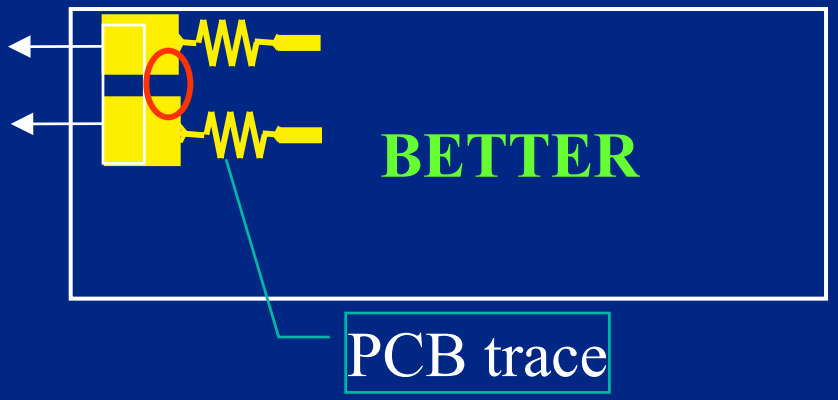
Top Fixes
Functional Block Placement



Top Fixes

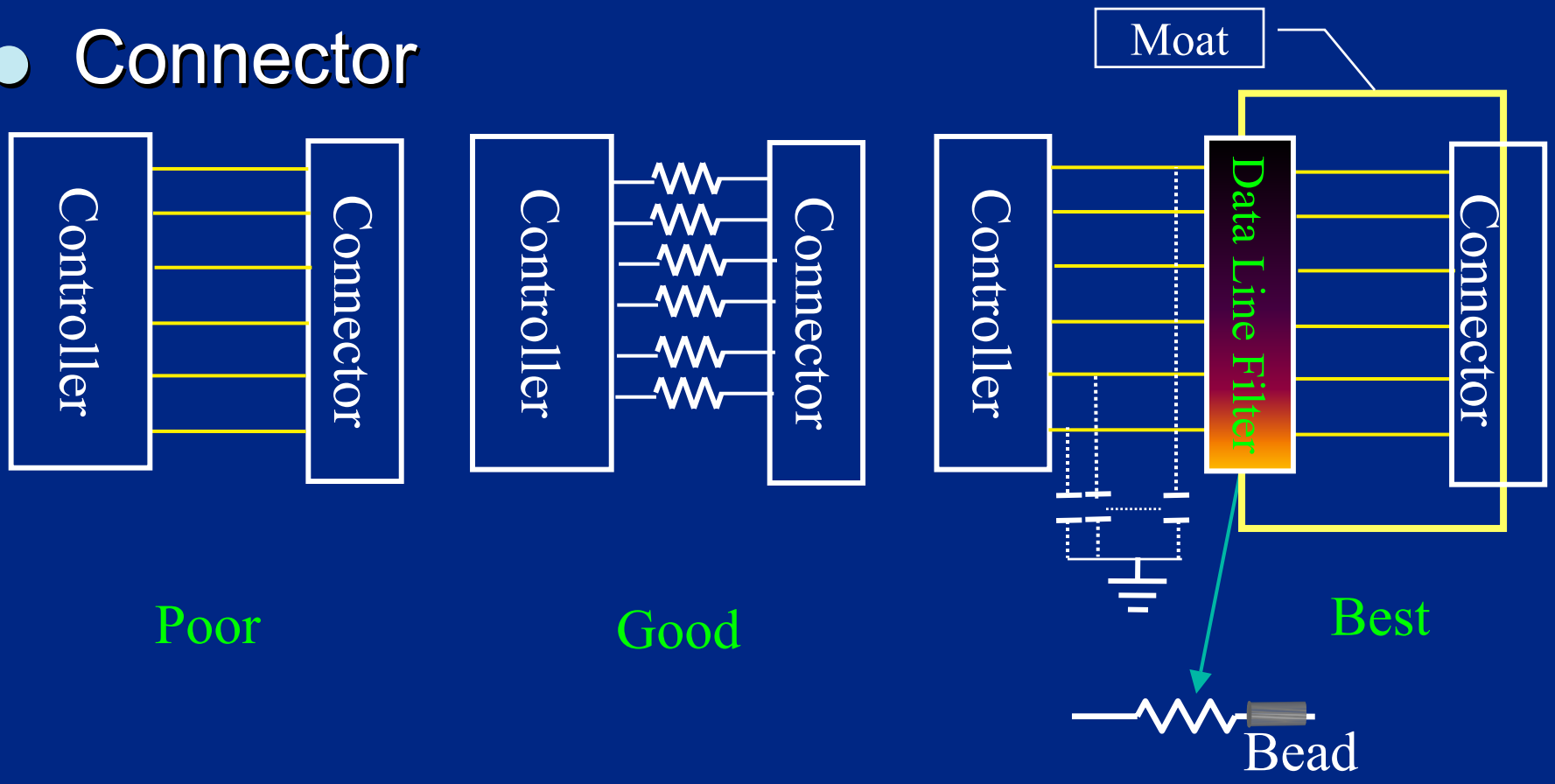
- Power entry & MOV (TS) location





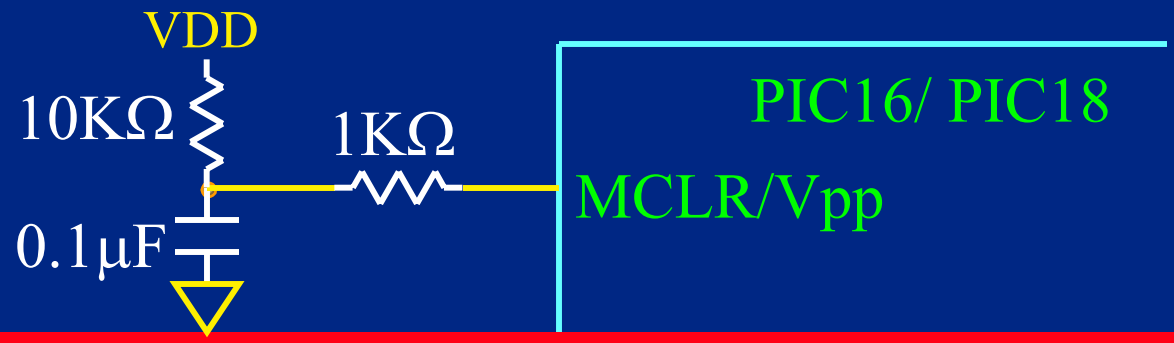
Top Fixes

- Connector



Top Fixes Microcontroller Circuits

- Reset Pins
  - A series resistor to limit the amount of current entering the MCLR pin due to ESD or EOS
  - A decoupling capacitor to attenuate high-frequency noise
  - Recommends pull-up resistor to VDD of <40KΩ



EMC References

- *The Designer's Guide to Electromagnetic Compatibility*
  by Daryl Gerke and Bill Kimmel
  EDN (www.ednmag.com)
- *Noise Reduction Techniques in Electronic Systems*
  Henry W. Ott
- *Printed Circuit Board Design Techniques for EMC Compliance*
  Mark I. Montrose

Standards Web Site

- Federal Communications Commission
  www.fcc.gov
- International Electrotechnical Commission
  www.iec.ch
- MIL Standards (military)
  www.mil-standards.com
- Society of Automotive Engineers
  www.sae.org

BONUS
Component Selection

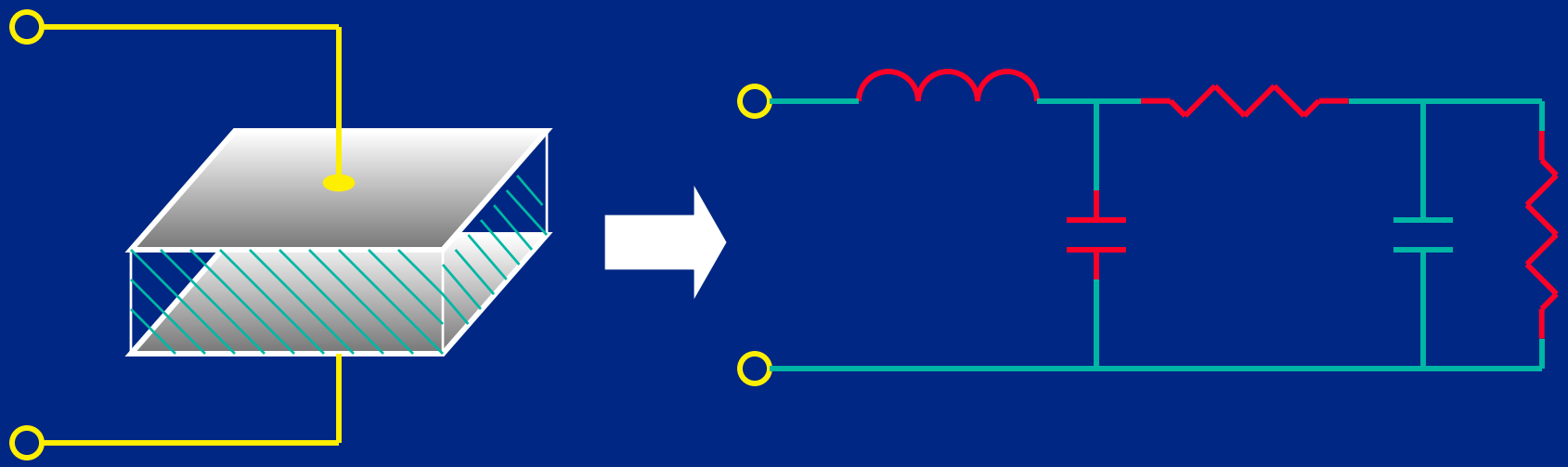
Resistors

- SMT & Thin film resistors
  - Good for high-frequency response
  - Not good for ESD protection. May arc around resistor
- Metal film suitable for high power density or high accuracy circuits
- Wire wound resistors suitable for high power handling circuits
  - Don’t use in high-frequency sensitive circuits

Capacitors - Construction

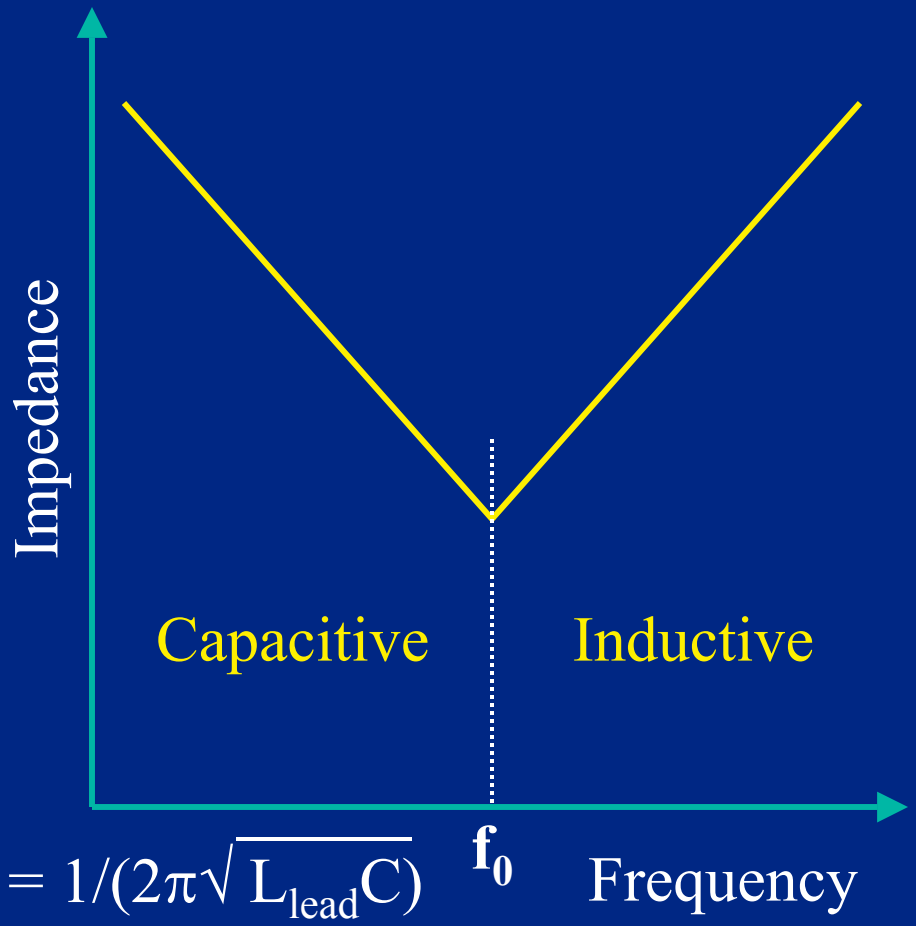
- Electrolytic- winds metal foil spirally between thin layer of dielectric
- Tantalum- block of dielectric with plates and pins attached
- Ceramic- multiple parallel metal plates in a ceramic dielectric
- Ceramic & tantalum dominate for EMC suppression
  - Low inductance & low ESR

Capacitors - Construction



Capacitors

- Self Resonance (f_0)
  - Impedance of inductor equals that of capacitor
  - Magnitudes of the impedance are same but opposite in sign
  - Net impedance of the circuit is the resistance



Capacitors

- Self resonance of various capacitance

Capacitor Value	Leaded	SMT
1.0 µF	2.5 MHz	5 MHz
0.1 µF	8 MHz	16 MHz
0.01 µF	25 MHz	50 MHz
1000 pF	80 MHz	160 MHz
100 pF	250 MHz	500MHz
10 pF	800 MHz	1.6 GHz

Bigger is not always better

Capacitors

Type	Approx. Max Frequency
Electrolytic	100 kHz
Tantalum	1 MHz
Paper	5 MHz
Mica	500 MHz
Ceramic	1 GHz

Capacitors
Tip #33

- To provide low impedance for shunting or diverting noise currents to ground
  - Frequency content must be below self-resonance frequency
- Sometimes multiple capacitors are needed to provide wider frequency filtering
- Frequent mistake is to make capacitance bigger to fix problem

Capacitors

- Ceramic capacitors
  - Smaller values of capacitance
  - Maintain ideal behavior up to much higher frequencies
  - Mid- to high-frequency filtering

Capacitors

- Electrolytic & Tantalum
  - Higher capacitance values
  - Low-frequency filtering
  - Used for bulk charge storage
- Electrolytic have high inductance
- Tantalum have low ESR
  - Lower ESR capacitors have better attenuation to signals

Capacitors
Tip #34

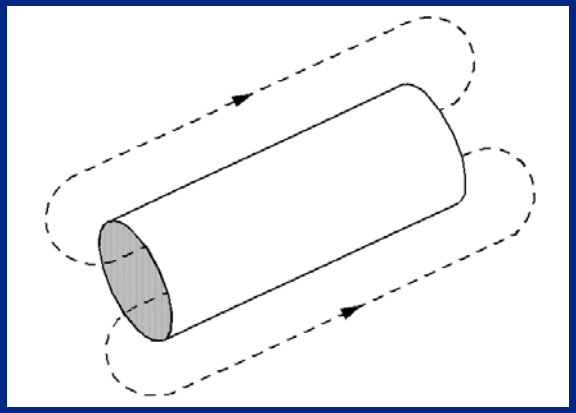
- Bypass
  - Shunts undesirable frequencies before they reach susceptible circuits
  - Watch self-resonance frequency as well as high-impedance circuits
  - Low-impedance loads draw energy away from bypass capacitor
  - Usually larger capacitance from electrolytic or tantalum capacitors

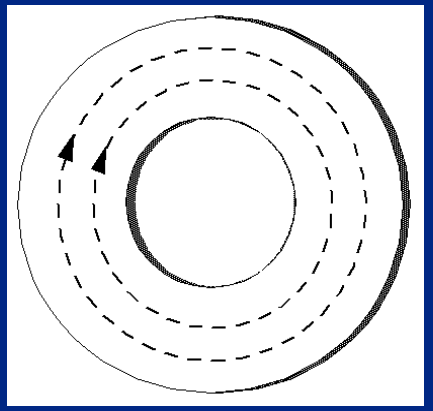
Capacitors
Tip #35

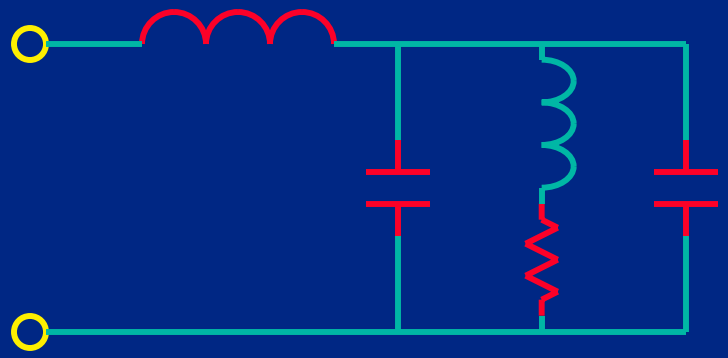
- Decoupling
  - Devices that are switching couple noise onto the power supply (V_{DD} & GND)
  - Decoupling capacitors filter high-frequency noise on power supply entering a device
  - Should be placed as close to the power pins on the device
  - Ceramic capacitors are usually used for decoupling because of the fast rise and fall times and their low ESR

Inductors

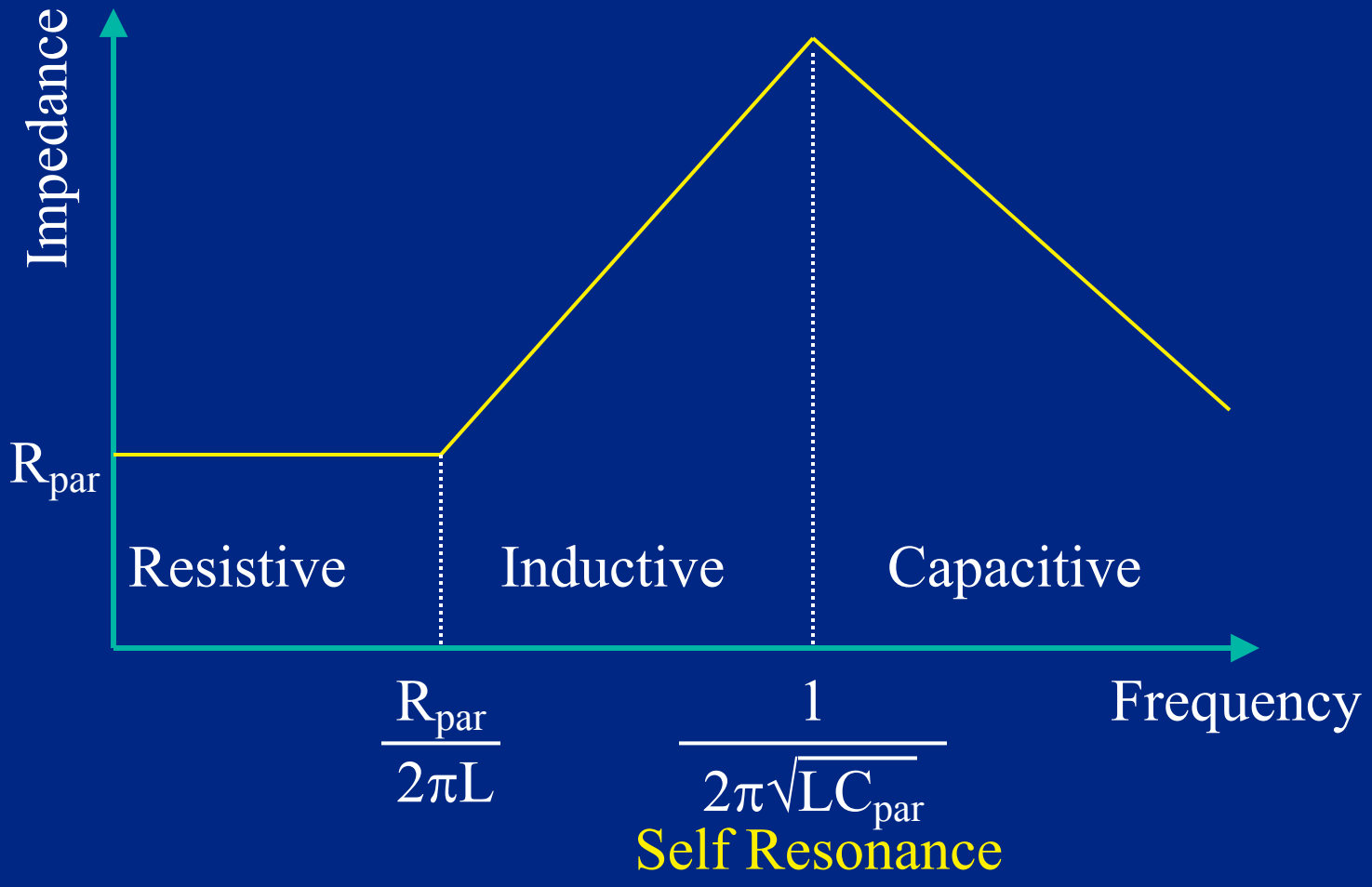
- Open-loop: rod inductor
  - Magnetic field passes through air
- Closed-loop: toroid
  - Magnetic field passes through core
- No parasitic inductance
  - No difference between leaded & SMT







Inductors

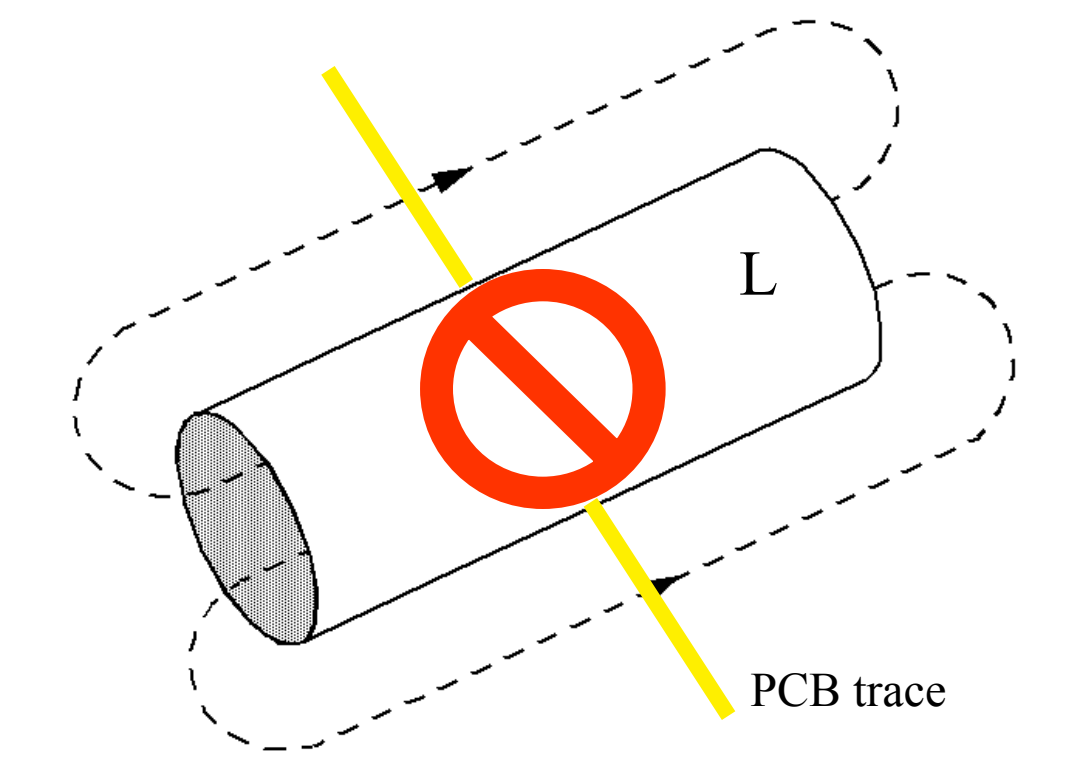


Inductors

- Open-loop inductors increase EMI
- Closed-loop inductors have very little susceptibility to external noise
- Two types of core material
  - Iron: useful for low frequency (kHz)
  - Ferrite: useful for high frequency (MHz)

PCB Layout - Inductive Coupling
Tip #36

- Noise Coupling



Inductors
Tip #37

- When using inductors to solve EMC issues
  - Usually only useful on signals that are DC or change infrequently
  - Impedance of load circuit is low
    - Parallel capacitors are better for high impedance loads
- Ferrite bead is basically a single turn inductor
  - Provide ~10 dB attenuation at high frequencies
  - Low attenuation or resistive at low frequencies

Component Selection
Transient Voltage Suppression (TVS) Device Comparison

Device	V/I curve	Speed	Energy cap..	Loss	Follow -on	Cost
Ideal	Sharp/ Flat	Fast	Infinite	None	None	Free
MOV	Sharp/ Non-Lin	Med	High	High	None/ High	Low
SAD	Sharp/ Flat	Fast	Low	Low	None/ High	Mod
GDT	Erratic/ Non-Lin	Slow	High	Low	High	Mod
Thyristor	Sharp/ Flat	Med	High	Low	None/ High	Mod
Spark Gap	Erratic/ Non-Lin	Slow	High	Low	None	Low

Component Selection
MOV

- Voltage Dependant Resistor
- Higher capacitance (Typ 1500 pF)
- High power handling capability
  - E.g. 6500 Amps @ 8 X 20 µS Pulse for 20 mmMOV
- Short- If fails
- Higher Leakage E.g. 5 mA @ operating V
- Performance degrades with transients

Hybrid TVS

- Hybrid TVS
  - Secondary Protection
  - Used to improve the V/I characteristics or speed
  - Higher Reliability (Back-up)