MCA Course (chapters and sections to learn)

- MCA Course book - Computer Architecture: A Quantitative Approach
  - Chapter 1 — Fundamentals of Quantitative Design and Analysis
    - Section 1.1 - Introduction
    - Section 1.2 - Classes of Computers
    - Section 1.3 - Defining Computer Architecture
    - Section 1.4 - Trends in Technology
    - Section 1.5 - Trends in Power and Energy in Integrated Circuits
    - Section 1.6 - Trends in Cost
    - Section 1.7 - Dependability
    - Section 1.8 - Measuring, Reporting, and Summarising Performance
    - Section 1.9 - Quantitative Principles of Computer Design
    - Section 1.10 - Putting it All Together
    - Section 1.11 - Fallacies and Pitfalls
    - Section 1.12 - Concluding Remarks
      - Not exam material, but interesting read
  - Chapter 2 — Memory Hierarchy Design
    - Section 2.1 - Introduction
    - Section 2.2 - Memory Technology and Optimizations
    - Section 2.3 - Ten Advances Optimizations of Cache Performance
    - Section 2.4 - Virtual Memory and Virtual Machines
      - Virtual Machines is not exam material
    - Section 2.5 - Cross-cutting Issues: The Design of Memory Hierarchies
    - Section 2.6 - Putting all Together: Memory Hierarchies in the ARM Cortex-A53 and Intel Core i7 6700
      - Not exam material, but interesting read
    - Section 2.7 Fallacies and Pitfalls
    - Section 2.8 - Concluding Remarks: Looking Ahead
      - Not exam material, but interesting read
  - Chapter 3 — Instruction-level Parallelism and Its Exploitation
    - Section 3.1 - Instruction-Level ParallelismL Concepts and Challenges
    - Section 3.2 - Basic Compiler Techniques for Exposing ILP
    - Section 3.3 - Reducing Branch Costs with Advanced Branch Prediction
    - Section 3.4 - Overcoming Data Hazards with Dynamic Scheduling
    - Section 3.5 - Dynamic Scheduling: Examples and the Algorithm
    - Section 3.6 - Hardware-based Speculation
    - Section 3.7 - Exploiting ILP using Multiple Issue and Static Scheduling
    - Section 3.8 - Exploiting ILP using Dynamic Scheduling, Multiple Issue, and Speculation
    - Section 3.9 - Advances Techniques for Instruction Delivery and Speculation
    - Section 3.10 - Cross-cutting Issues
    - Section 3.11 - Multithreading: Exploiting Thread-leve Parallelism to Improve Uni-processor Throughput
    - Section 3.12 - Putting it All Together: The Core i7 6700 and ARM Cortex-A53
      - Not exam material, but interesting read
    - Section 3.13 - Fallacies and Pitfalls

        - Section 3.14 - Concluding Remarks: What’s Ahead?
            - Not exam material, but interesting read
    - Chapter 4 — Data-level Parallelism in Vector, SIMD, and GPU Architectures
        - Section 4.1 - Introduction
        - Section 4.2 - Vector Architecture
        - Section 4.3 - SIMD Instruction Set Extensions for Multimedia
        - Section 4.4 - Graphics Processing Units
        - Section 4.5 - Detecting and Enhancing Loop-level Parallelism
            - Not exam material, but interesting read
        - Section 4.6 - Cross-cutting Issues
        - Section 4.7 - Putting It All Together: Embedded Versus Server GPA and Tesla Versus Core I7
            - Not exam material, but interesting read
        - Section 4.8 - Fallacies and Pitfalls
        - Section 4.9 - Concluding Remarks
    - Chapter 5 — Thread-level parallelism
        - Section 5.1 - Introduction
        - Section 5.2 - Centralized Sharing-memory Architectures
        - Section 5.3 - Performance of Symmetric Shared-memory Multiprocessors
        - Section 5.4 - Distributed Shared-memory and Directory-based Coherence
        - Section 5.5 - Synchronization: The Basics
            - Not exam material, but interesting read
        - Section 5.6 - Models of Memory Consistency: An Introduction
            - Relaxed Consistency Models are not exam material, but interesting read
        - Section 5.7 - Cross-cutting Issues
            - Not exam material, but interesting read
        - Section 5.8 - Putting it All Together: Multicore Processors and Their Performance
            - Not exam material, but interesting read
        - Section 5.9 - Fallacies and Pitfalls
        - Section 5.10 - The Future of Multicore Scaling
        - Section 5.11 - Concluding Remarks