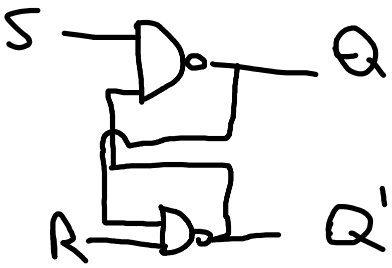
İSTANBUL TEKNİK ÜNİVERSİTESİ

1773

DIGITAL SYSTEM DESIGN APPLICATION PROJECT 5

SR LATCH WITH NAND GATE

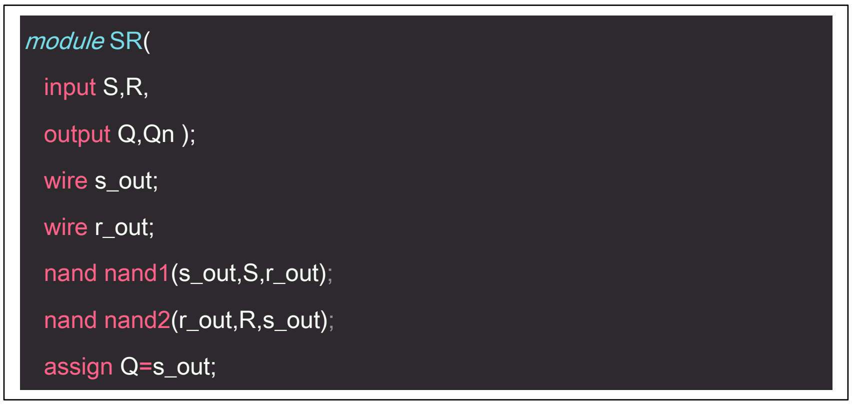
- Truth table and Circuit diagram



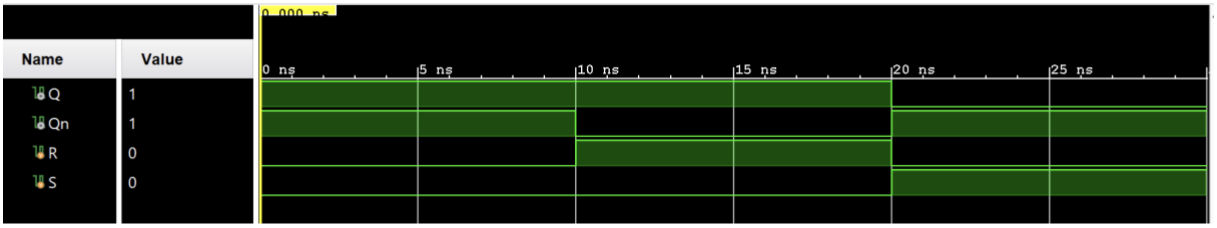
S	R	Qnext
0	0	No change
0	1	Q=0
1	0	Q=1
1	1	1 0

Characteristic and inverse characteristic functions

- Verilog code and Simulation results

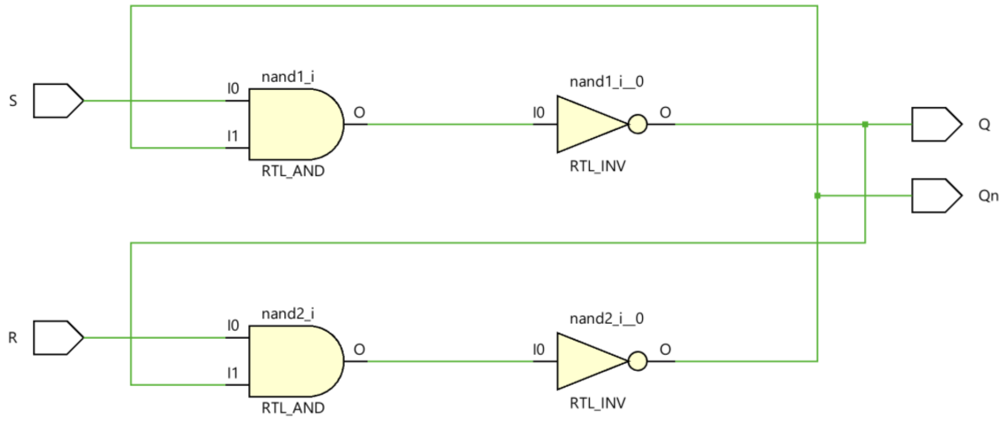


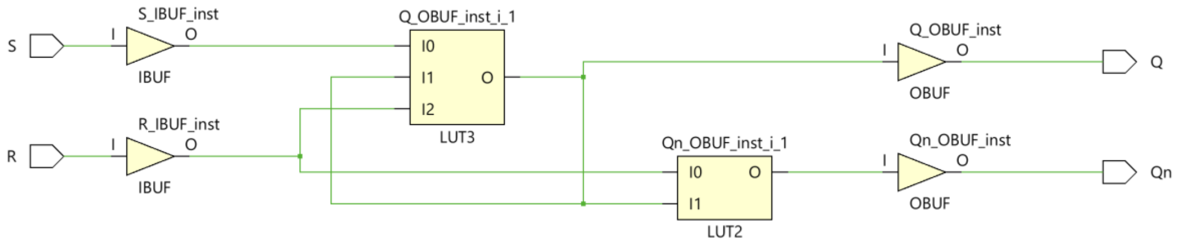
```
module SR(
   input S,R,
   output Q,Qn );
   wire s_out;
   wire r_out;
   nand nand1(s_out,S,r_out);
   nand nand2(r_out,R,s_out);
   assign Q=s_out;
```



Name	Value
Q	1
Qn	1
R	0
S	0

RTL and Technology Schematics

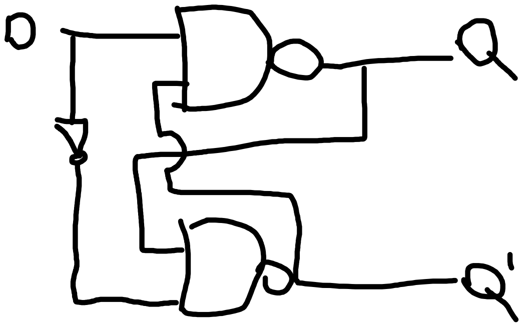




We done SR latch. SR latch have mermory so we can create sequential circuit with SR latch. We can do SR latch with nor gate this is other section. Our circuit not include enable input but we can do this.

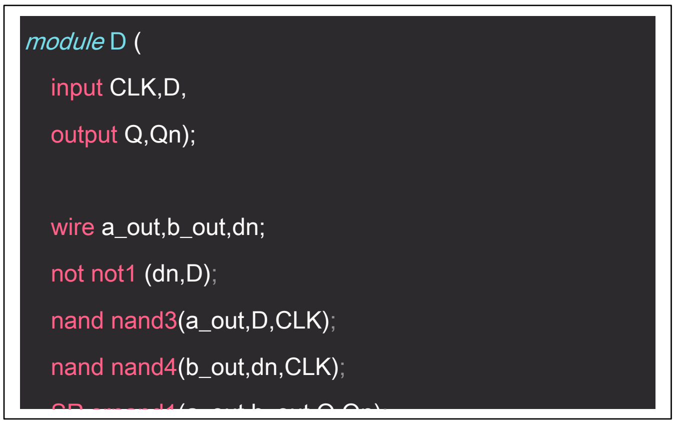
D FLIP FLOP

- Truth table and Circuit diagram,

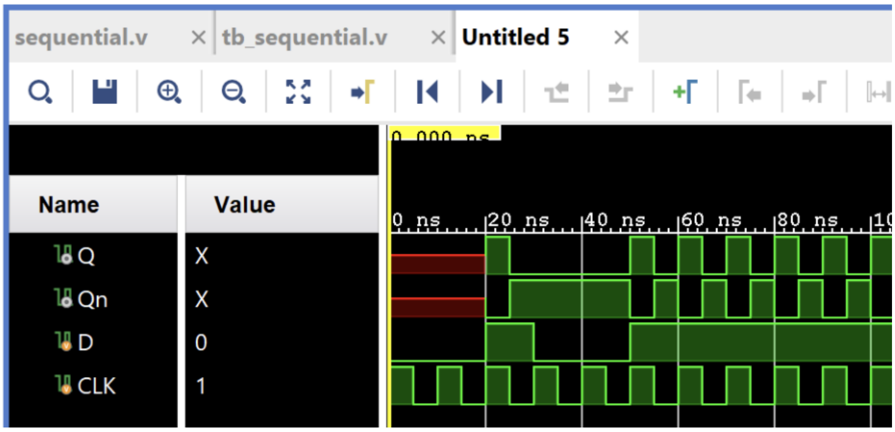


D	Qnext
0	Q=0
1	Q=1

- Characteristic and inverse characteristic functions,
- Verilog code and Simulation results

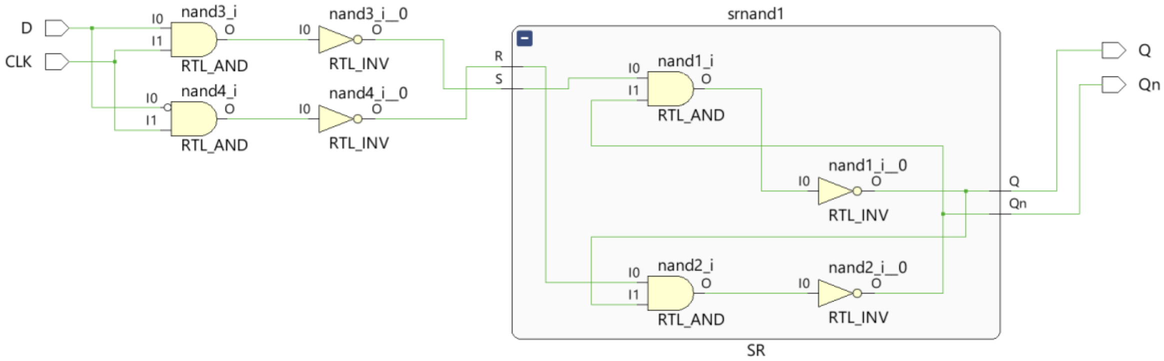


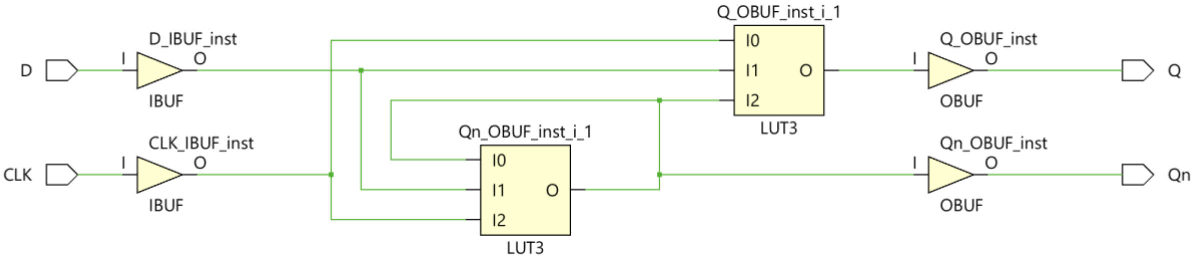
```
module D (
   input CLK,D,
   output Q,Qn);


   wire a_out,b_out,dn;
   not not1 (dn,D);
   nand nand3(a_out,D,CLK);
   nand nand4(b_out,dn,CLK);
   SR srnand1(a_out,b_out,Q,Qn);
```



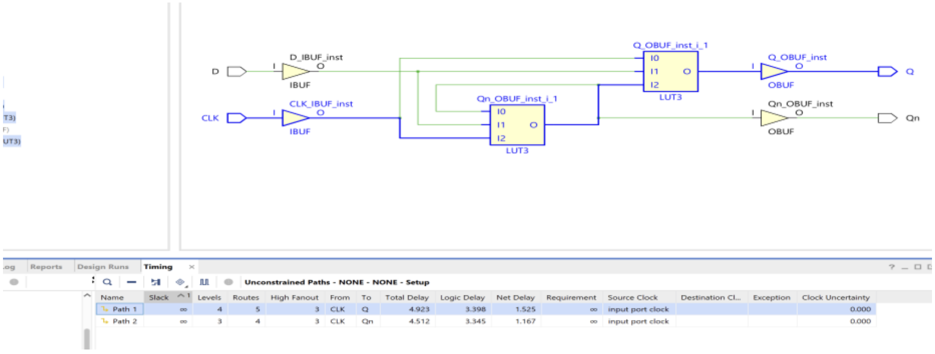
Name	Value
Q	X
Qn	X
D	0
CLK	1

• RTL and Technology Schematics





• Path with the longest delay and its delay time Explain



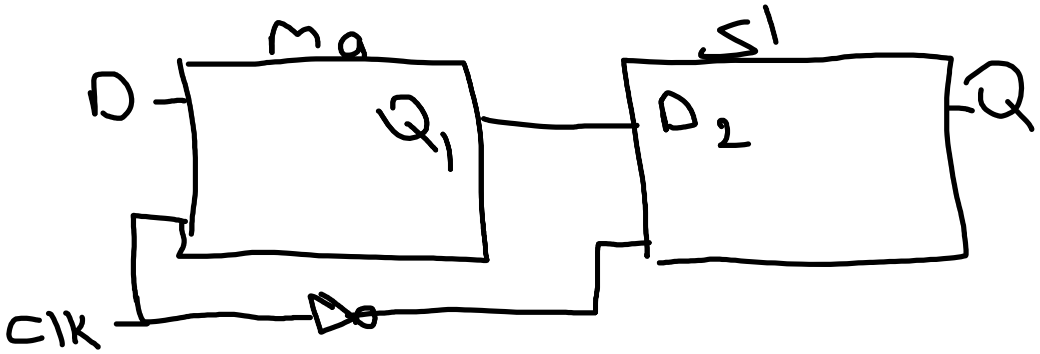
Unconstrained Paths - NONE - NONE - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Cl...	Exception	Clock Uncertainty
Path 1	∞	4	5	3	CLK	Q	4.923	3.398	1.525	∞	input port clock			0.000
Path 2	∞	3	4	3	CLK	Qn	4.512	3.345	1.167	∞	input port clock			0.000

We 4 path. This path delay time 4.923. this path delay is longest. Because this path ways longest long wire = delay.

MASTER -SLAVE D FLİP FLOP

- Add the circuit diagram to your report.



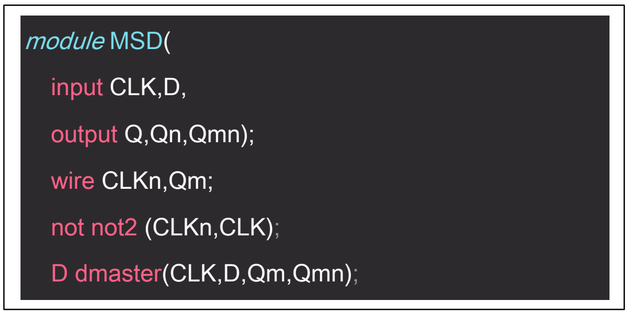
- Explain how Master-Slave D-Flip Flop works. What is the difference from the previous D-FF.

Master slave have 2 D flip flop. And one input D other is clock. Clock what gives first gives other inverse. So we can understand that posede or negede trigger.

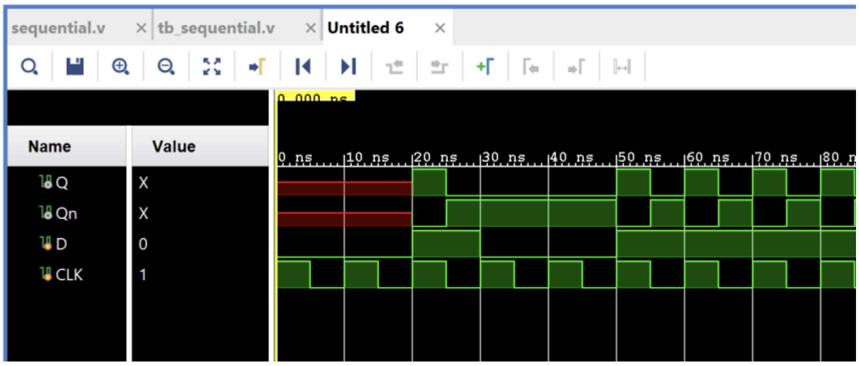
- Which edge of the clock signal affects the output? Explain.

Negative. Because when clock 1 master flip flop Works and D2 is 1 but clock sent 0 to slave flip flop so dont work.but negative edge from 1 to 0 clk sent slave flip flop 1 and slave flip flop work with previous D .

- Verilog code and Simulation results.



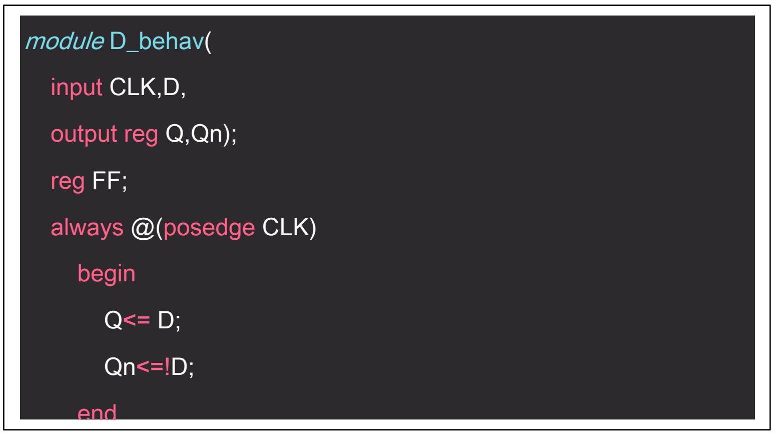
```
module MSD(
    input CLK,D,
    output Q,Qn,Qmn);
    wire CLKn,Qm;
    not not2 (CLKn,CLK);
    D dmaster(CLK,D,Qm,Qmn);
```



Name	Value
Q	X
Qn	X
D	0
CLK	1

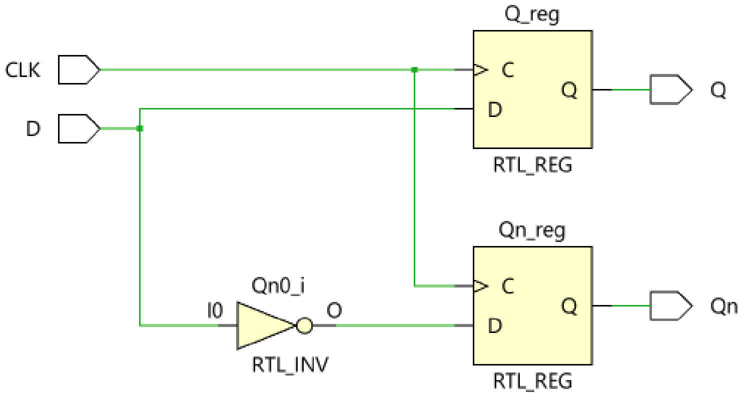
D FLIP FLOP BEHAVİORAL DESIGN

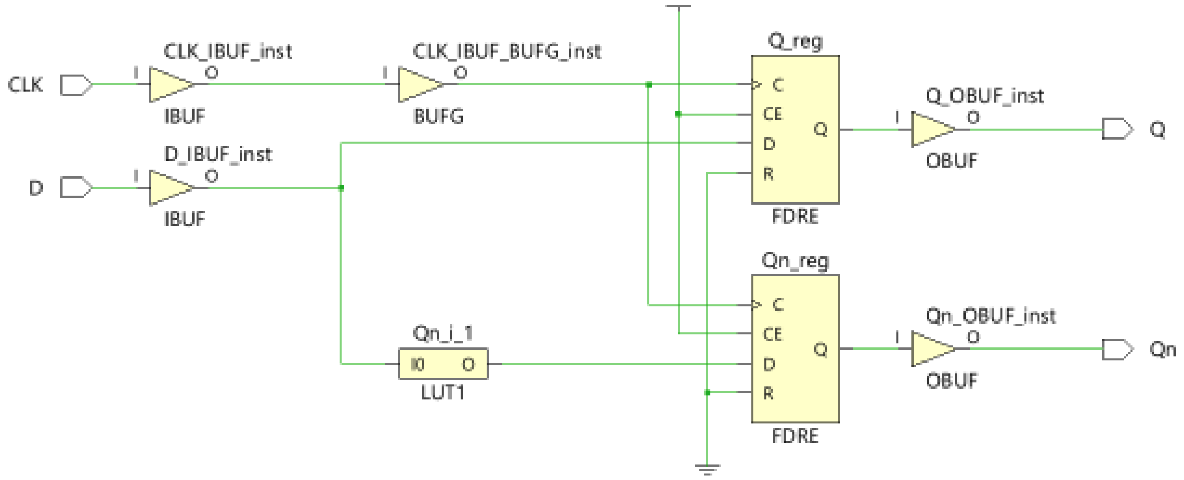
Verilog code



```
module D_behav(
  input CLK,D,
  output reg Q,Qn);
  reg FF;
  always @(posedge CLK)
    begin
      Q<= D;
      Qn<=!D;
    end
```

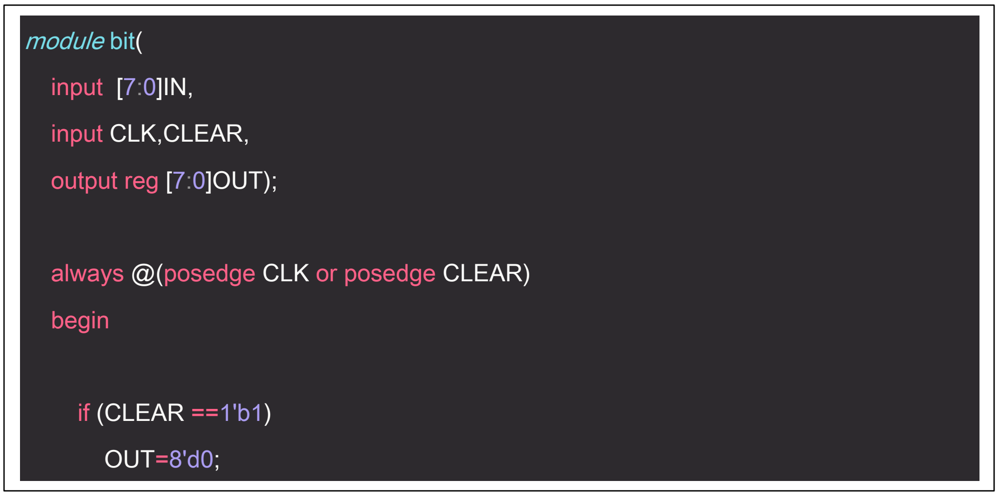
Rtl and technology schemaics



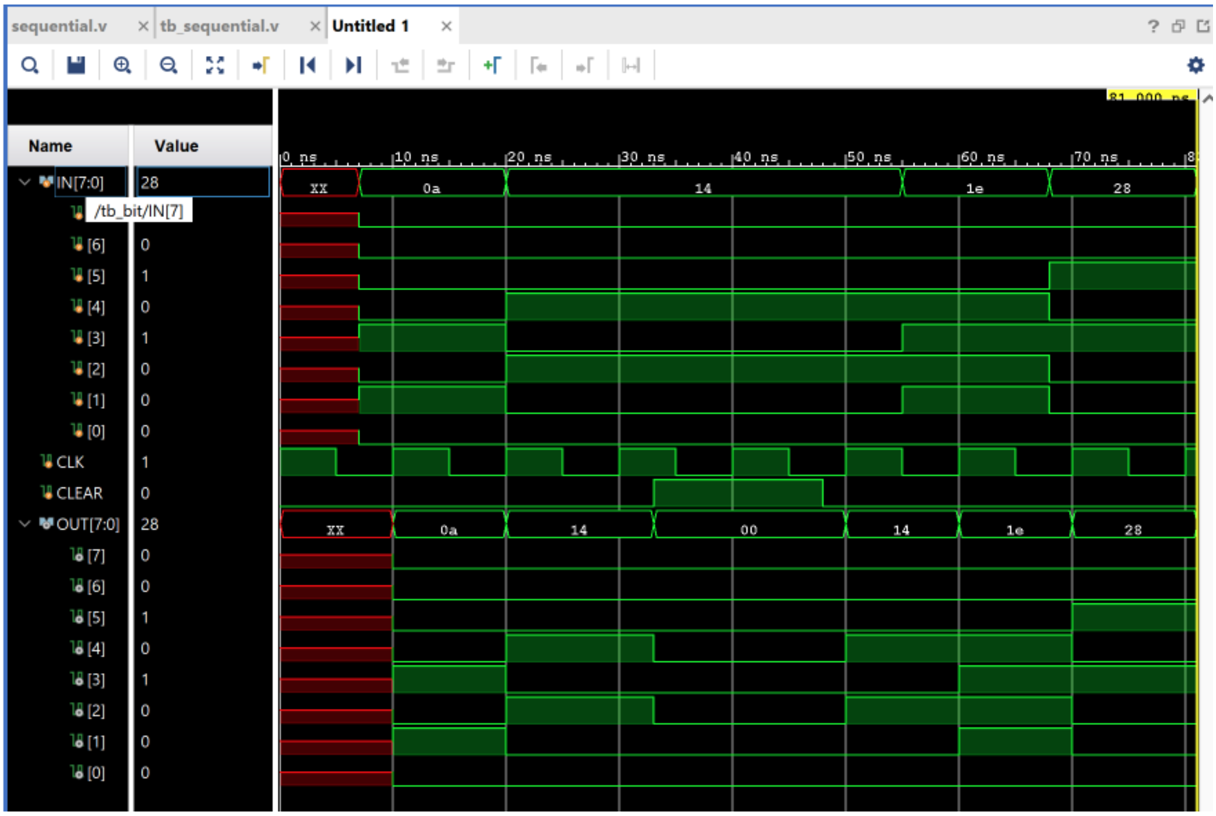


8-BIT REGISTER

- Verilog code and Simulation results.

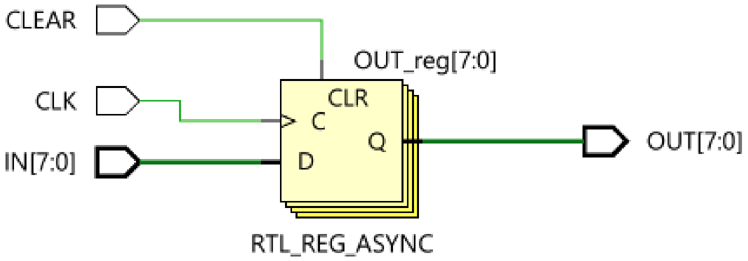


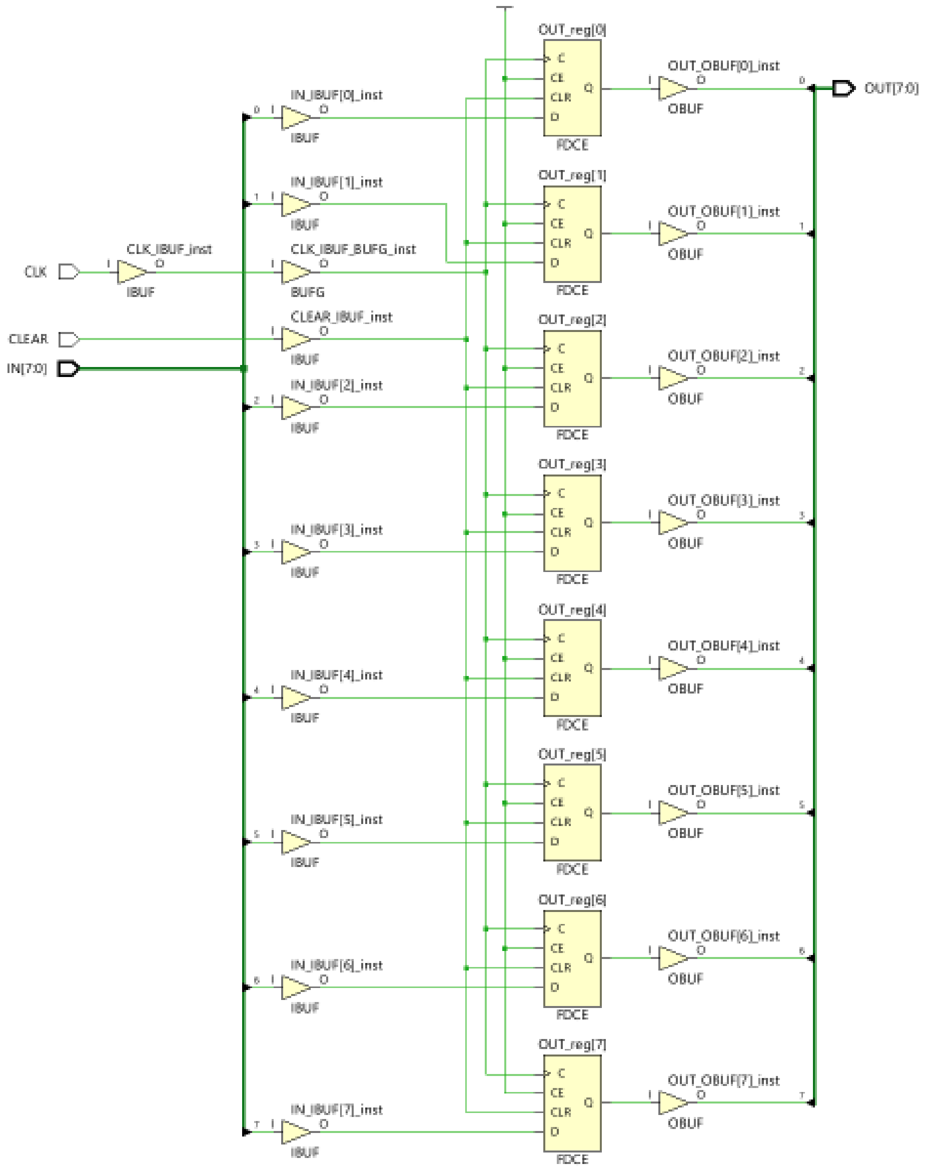
```
module bit(
   input  [7:0]IN,
   input CLK,CLEAR,
   output reg [7:0]OUT);

   always @(posedge CLK or posedge CLEAR)
   begin

      if (CLEAR ==1'b1)
          OUT=8'd0;
```



Name	Value
IN[7:0]	28
[6]	0
[5]	1
[4]	0
[3]	1
[2]	0
[1]	0
[0]	0
CLK	1
CLEAR	0
OUT[7:0]	28
[7]	0
[6]	0
[5]	1
[4]	0
[3]	1
[2]	0
[1]	0
[0]	0

RTL and Technology Schematics





Explain how you define a 4x8-bit register array in Verilog.

BLOCK RAM

- Verilog code and Simulation results.

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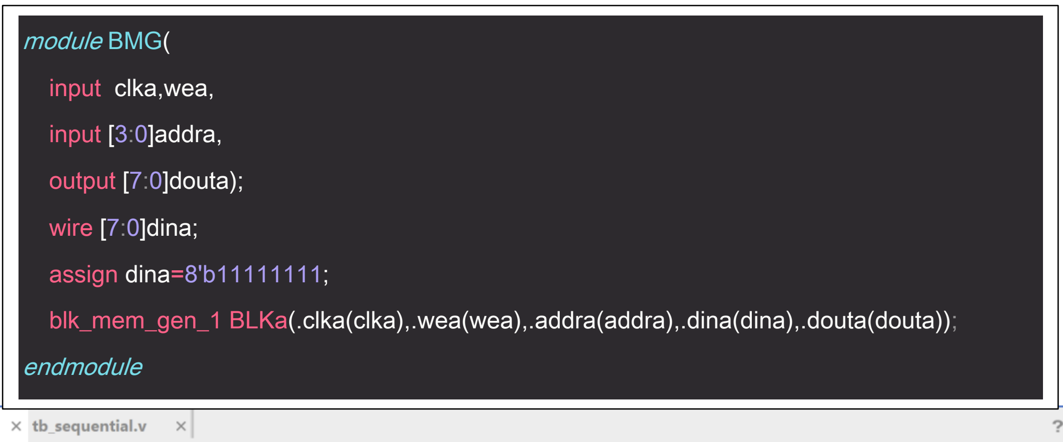
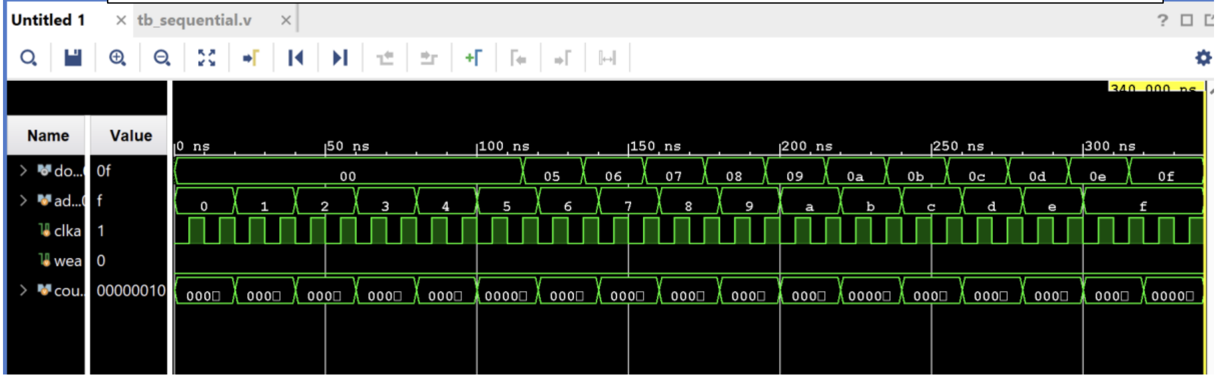


```
module BMG(
    input  clka,wea,
    input [3:0]addra,
    output [7:0]douta);
    wire [7:0]dina;
    assign dina=8'b11111111;
    blk_mem_gen_1 BLKa(.clka(clka),.wea(wea),.addra(addra),.dina(dina),.douta(douta));
endmodule
```

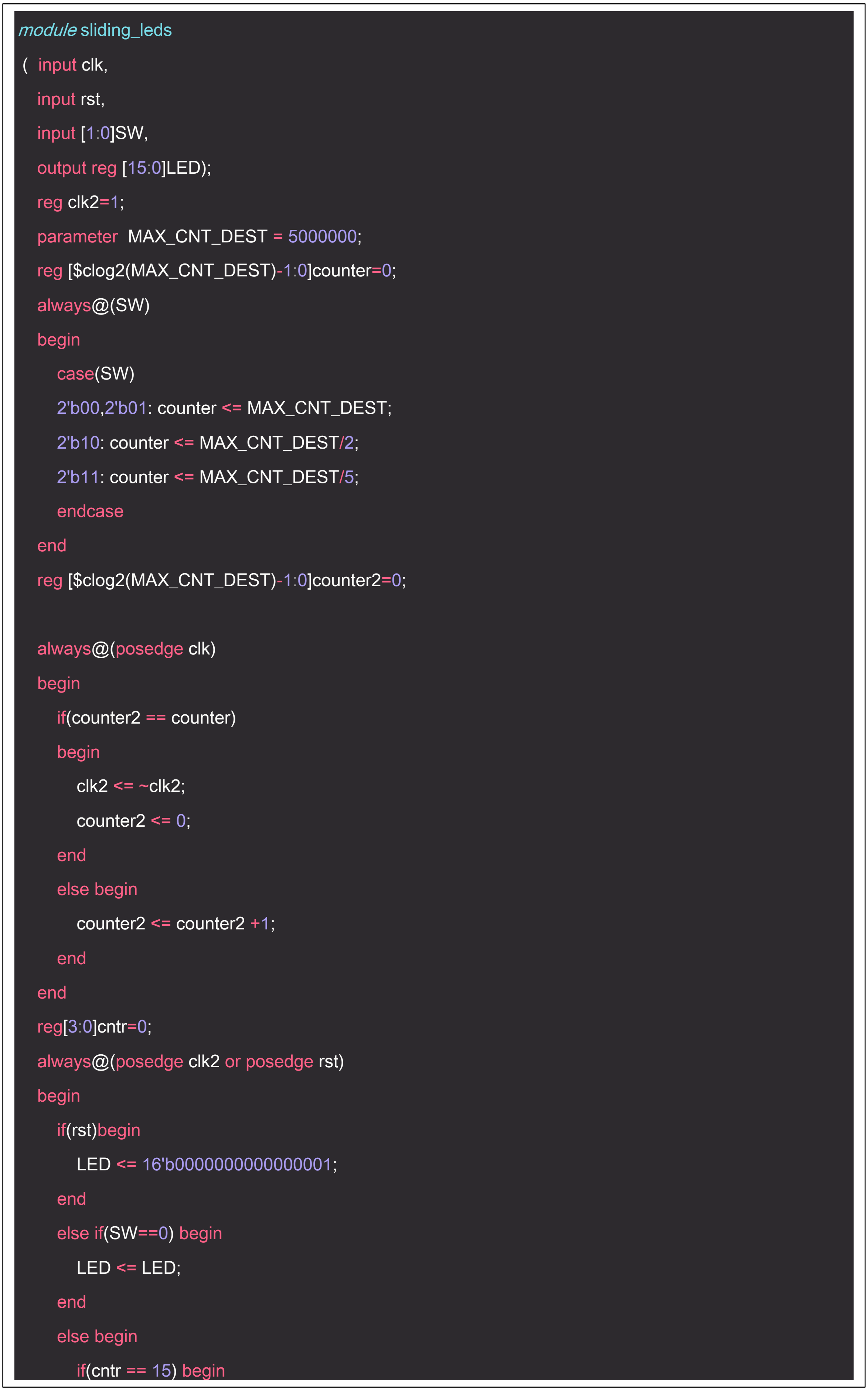


Investigate and explain the Block RAM ports.

- Investigate and explain the structure of .coe file.

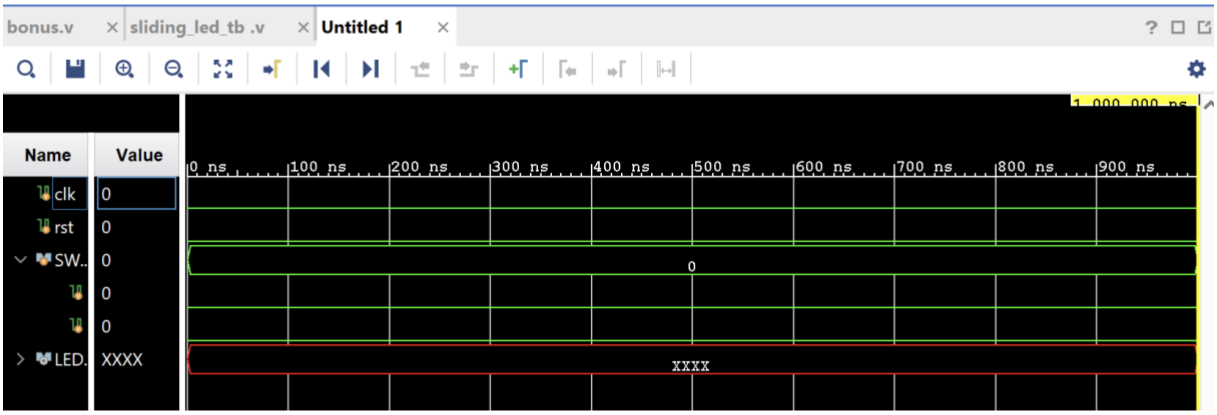
SLIDING LEDS

Verilog code and Simulation results.



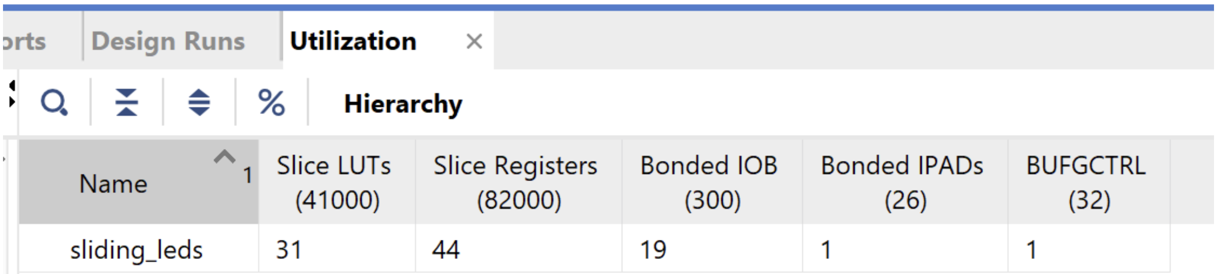
```
module sliding_leds
(  input clk,
   input rst,
   input [1:0]SW,
   output reg [15:0]LED);
   reg clk2=1;
   parameter  MAX_CNT_DEST = 5000000;
   reg [$clog2(MAX_CNT_DEST)-1:0]counter=0;
   always@(SW)
   begin
      case(SW)
      2'b00,2'b01: counter <= MAX_CNT_DEST;
      2'b10: counter <= MAX_CNT_DEST/2;
      2'b11: counter <= MAX_CNT_DEST/5;
      endcase
   end
   reg [$clog2(MAX_CNT_DEST)-1:0]counter2=0;

   always@(posedge clk)
   begin
      if(counter2 == counter)
      begin
         clk2 <= ~clk2;
         counter2 <= 0;
      end
      else begin
         counter2 <= counter2 +1;
      end
   end
   reg[3:0]cntr=0;
   always@(posedge clk2 or posedge rst)
   begin
      if(rst)begin
         LED <= 16'b0000000000000001;
      end
      else if(SW==0) begin
         LED <= LED;
      end
      else begin
         if(cntr == 15) begin
```

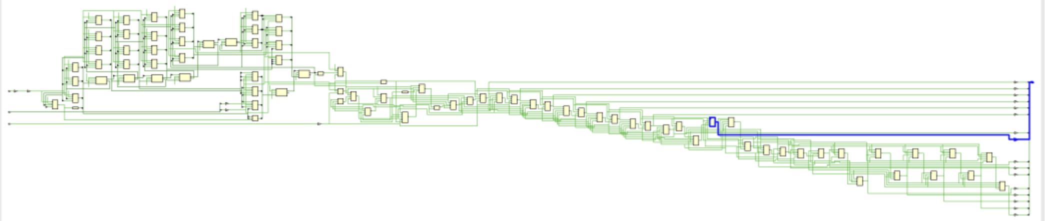


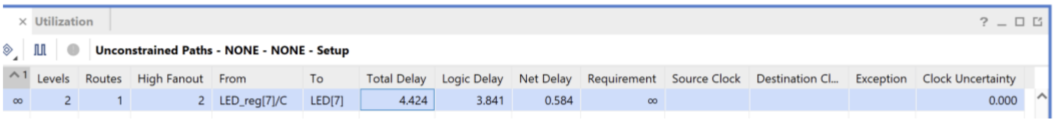
Name	Value
clk	0
rst	0
SW..	0
	0
	0
LED.	XXXX

- Utilization report and critical path slack.



Name	Slice LUTs (41000)	Slice Registers (82000)	Bonded IOB (300)	Bonded IPADs (26)	BUFGCTRL (32)
sliding_leds	31	44	19	1	1





Unconstrained Paths - NONE - NONE - Setup

1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Cl...	Exception	Clock Uncertainty
∞	2	1	2	LED_reg[7]/C	LED[7]	4.424	3.841	0.584	∞				0.000