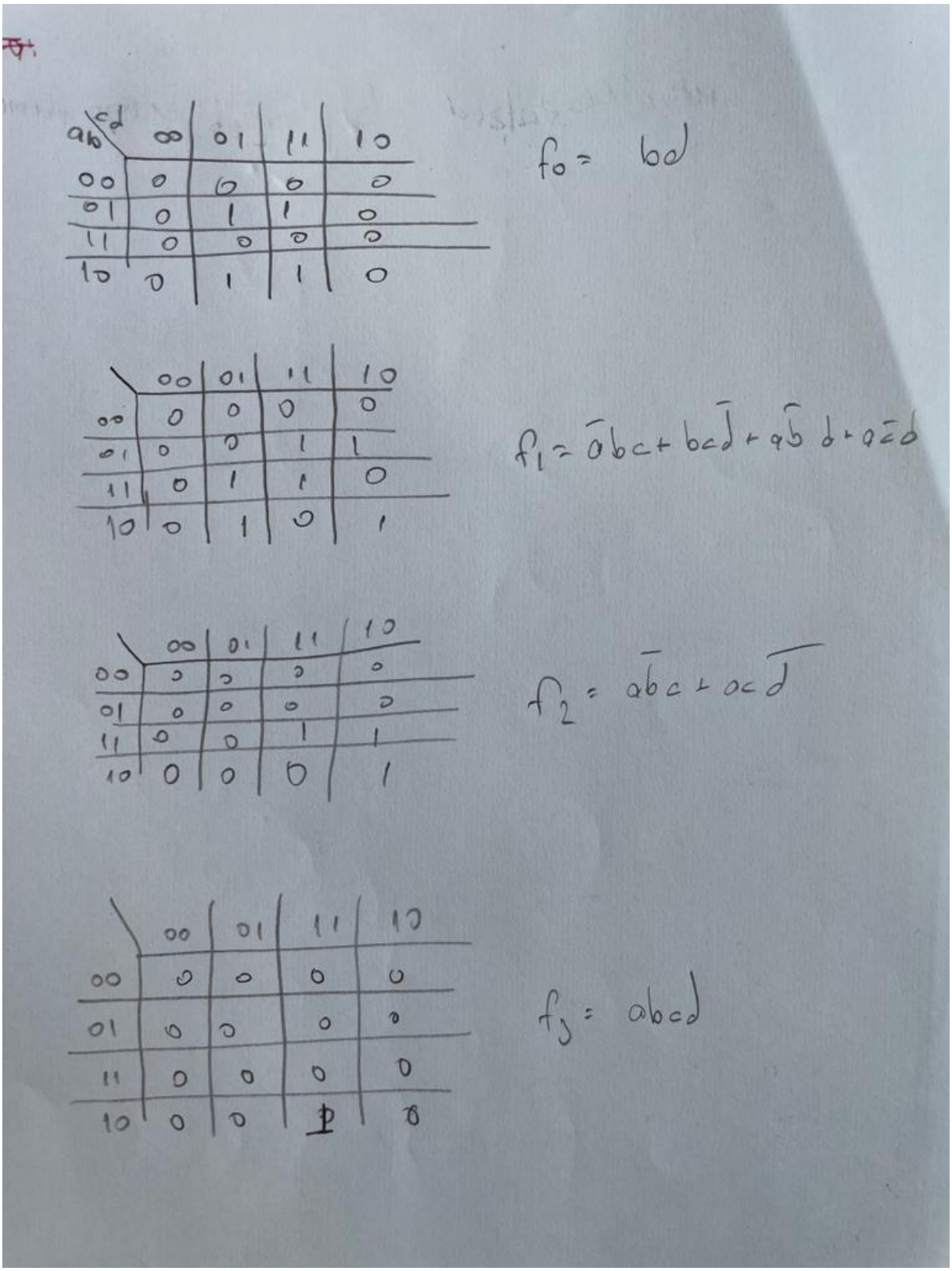
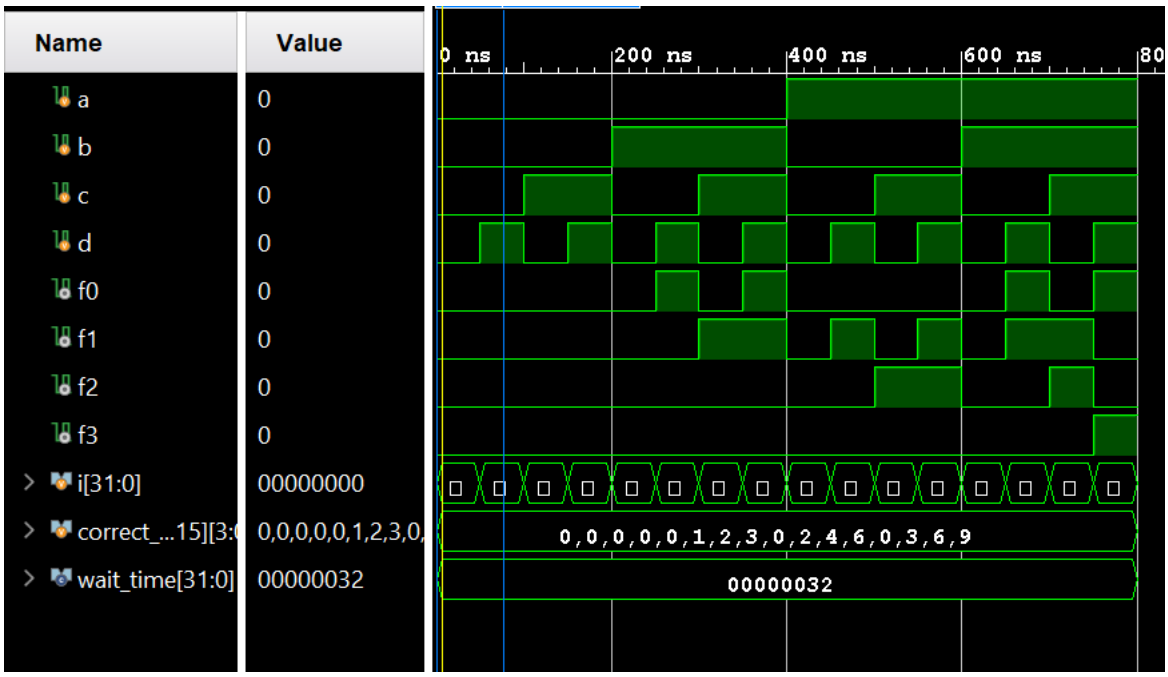
DIGITAL SYSTEM DESIGN APPLICATION PROJECT 3

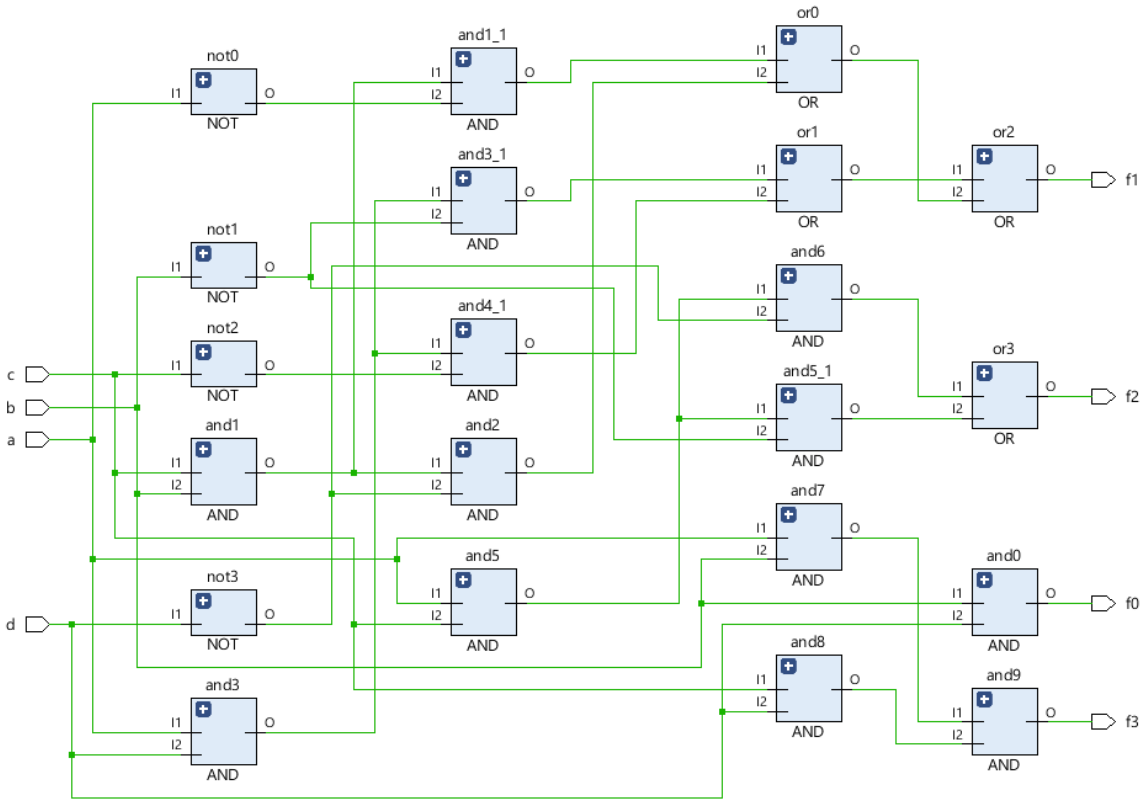
With SSI:


ab \ cd
00 01 11 10
00 0 0 0 0
01 0 1 1 0
11 0 0 0 0
10 0 1 1 0
$f_0 = bd$
00 01 11 10
00 0 0 0 0
01 0 0 1 1
11 0 1 1 0
10 0 1 0 1
$f_1 = \bar{a}bc + b\bar{c}d + a\bar{b}d + 0\bar{c}\bar{d}$
00 01 11 10
00 0 0 0 0
01 0 0 0 0
11 0 0 1 1
10 0 0 0 1
$f_2 = a\bar{b}c + ac\bar{d}$
00 01 11 10
00 0 0 0 0
01 0 0 0 0
11 0 0 0 0
10 0 0 1 0
$f_3 = abcd$

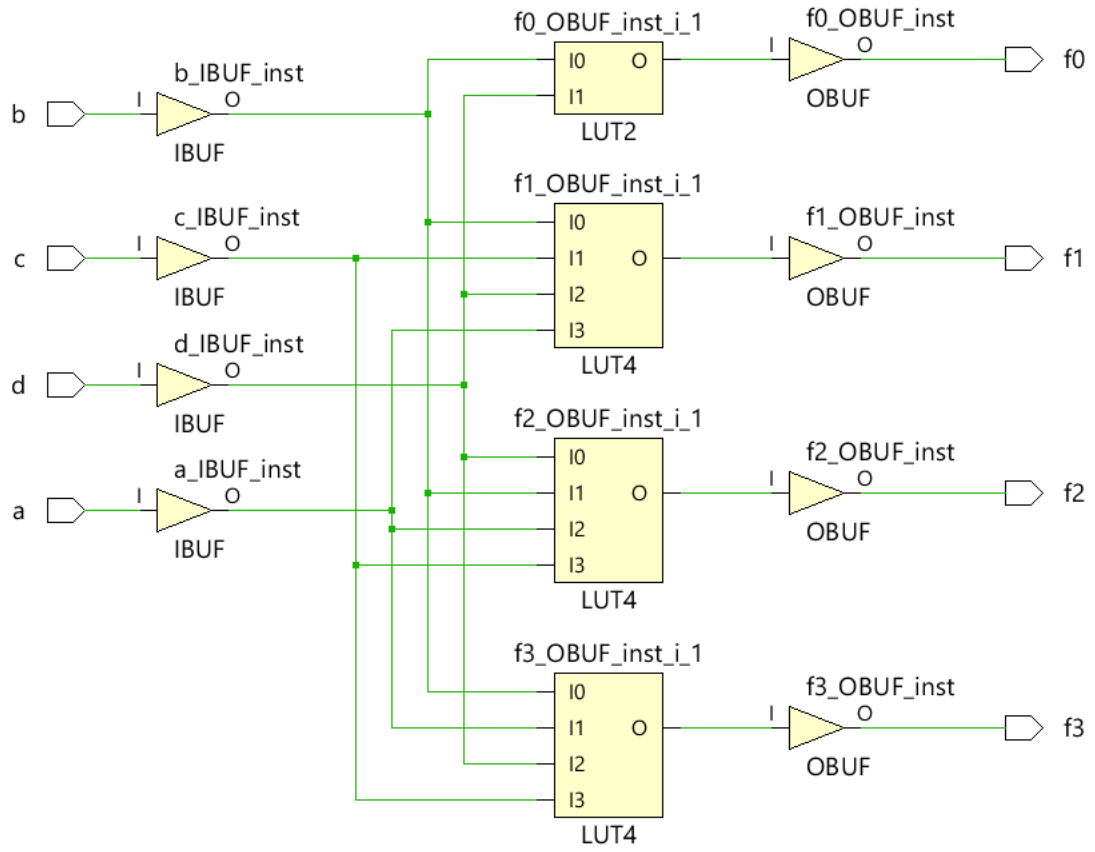
BEHAVIORAL SIMULATION



RTL SHEMATIC



SHENTHESYZ TECHNOLOGY SHEMATIC



PAD TO PAD NO TIMING

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f1	7.311	SLOW	2.444	FAST
a	f2	6.977	SLOW	2.343	FAST
a	f3	7.112	SLOW	2.396	FAST
b	f0	6.661	SLOW	2.240	FAST
b	f1	6.790	SLOW	2.288	FAST
b	f2	6.490	SLOW	2.183	FAST
b	f3	6.663	SLOW	2.258	FAST
c	f1	6.977	SLOW	2.335	FAST
c	f2	6.646	SLOW	2.233	FAST
c	f3	7.029	SLOW	2.383	FAST
d	f0	6.739	SLOW	2.234	FAST
d	f1	6.879	SLOW	2.294	FAST
d	f2	6.547	SLOW	2.195	FAST
d	f3	6.707	SLOW	2.259	FAST

PAD TO PAD MAX TIMING

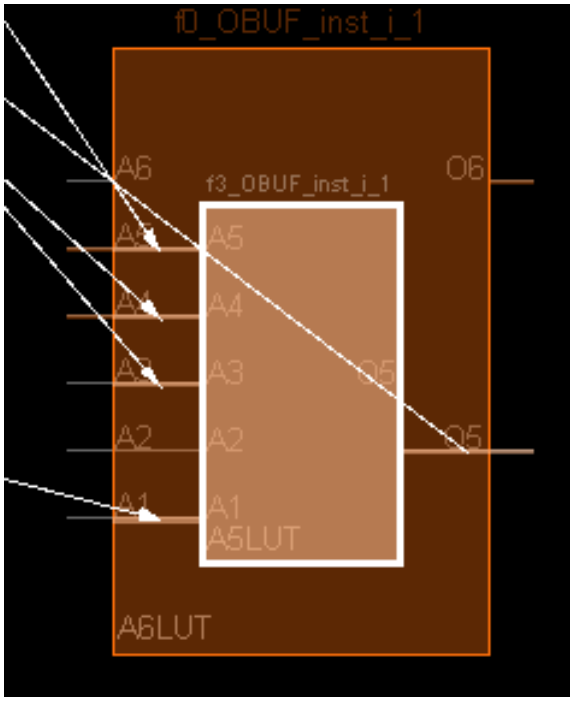
Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f1	9.132	SLOW	2.783	FAST
a	f2	9.291	SLOW	2.899	FAST
a	f3	8.899	SLOW	2.728	FAST
b	f0	9.427	SLOW	2.861	FAST
b	f1	8.893	SLOW	2.642	FAST
b	f2	9.050	SLOW	2.756	FAST
b	f3	8.660	SLOW	2.585	FAST
c	f1	8.116	SLOW	2.385	FAST
c	f2	8.307	SLOW	2.495	FAST
c	f3	7.928	SLOW	2.335	FAST
d	f0	9.420	SLOW	2.877	FAST
d	f1	8.876	SLOW	2.646	FAST
d	f2	9.033	SLOW	2.760	FAST
d	f3	8.652	SLOW	2.603	FAST

PAD TO PAD WITH-OUT LOC

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f1	8.881	SLOW	2.725	FAST
a	f2	8.852	SLOW	2.722	FAST
a	f3	10.132	SLOW	3.265	FAST
b	f0	10.569	SLOW	3.473	FAST
b	f1	8.716	SLOW	2.587	FAST
b	f2	8.655	SLOW	2.586	FAST
b	f3	10.358	SLOW	3.423	FAST
c	f1	8.919	SLOW	2.669	FAST
c	f2	8.858	SLOW	2.672	FAST
c	f3	10.773	SLOW	3.551	FAST
d	f0	10.971	SLOW	3.662	FAST
d	f1	9.283	SLOW	2.817	FAST
d	f2	9.220	SLOW	2.819	FAST
d	f3	10.728	SLOW	3.613	FAST



TIMING AND WITHOUT LOC

Combinational Delays

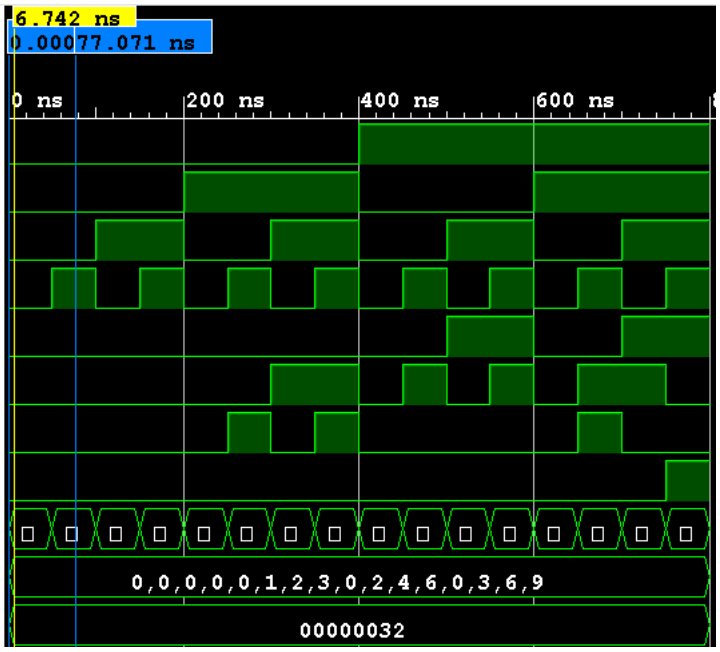
From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f1	8.881	SLOW	2.725	FAST
a	f2	8.852	SLOW	2.722	FAST
a	f3	10.132	SLOW	3.265	FAST
b	f0	10.569	SLOW	3.473	FAST
b	f1	8.716	SLOW	2.587	FAST
b	f2	8.655	SLOW	2.586	FAST
b	f3	10.358	SLOW	3.423	FAST
c	f1	8.919	SLOW	2.669	FAST
c	f2	8.858	SLOW	2.672	FAST
c	f3	10.773	SLOW	3.551	FAST
d	f0	10.971	SLOW	3.662	FAST
d	f1	9.283	SLOW	2.817	FAST
d	f2	9.220	SLOW	2.819	FAST
d	f3	10.728	SLOW	3.613	FAST

DECODER

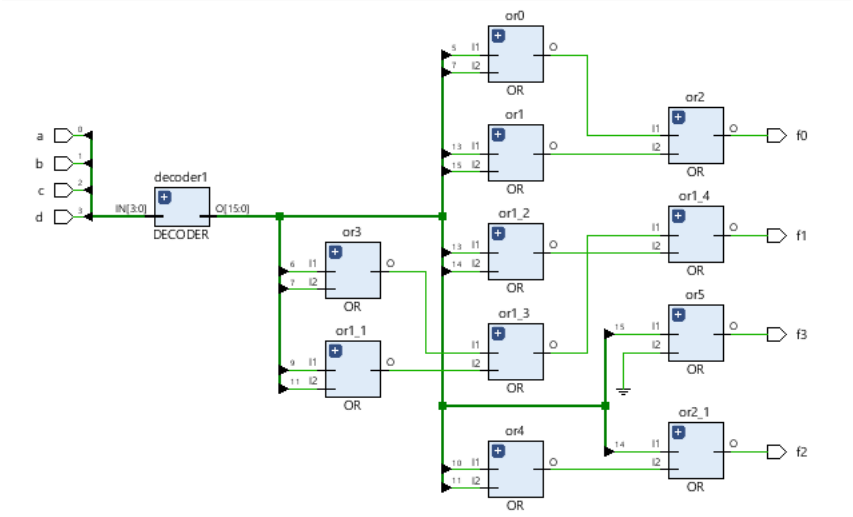
DECODER 4-16 SHEMA

DECODER SUM OF PRODUCT

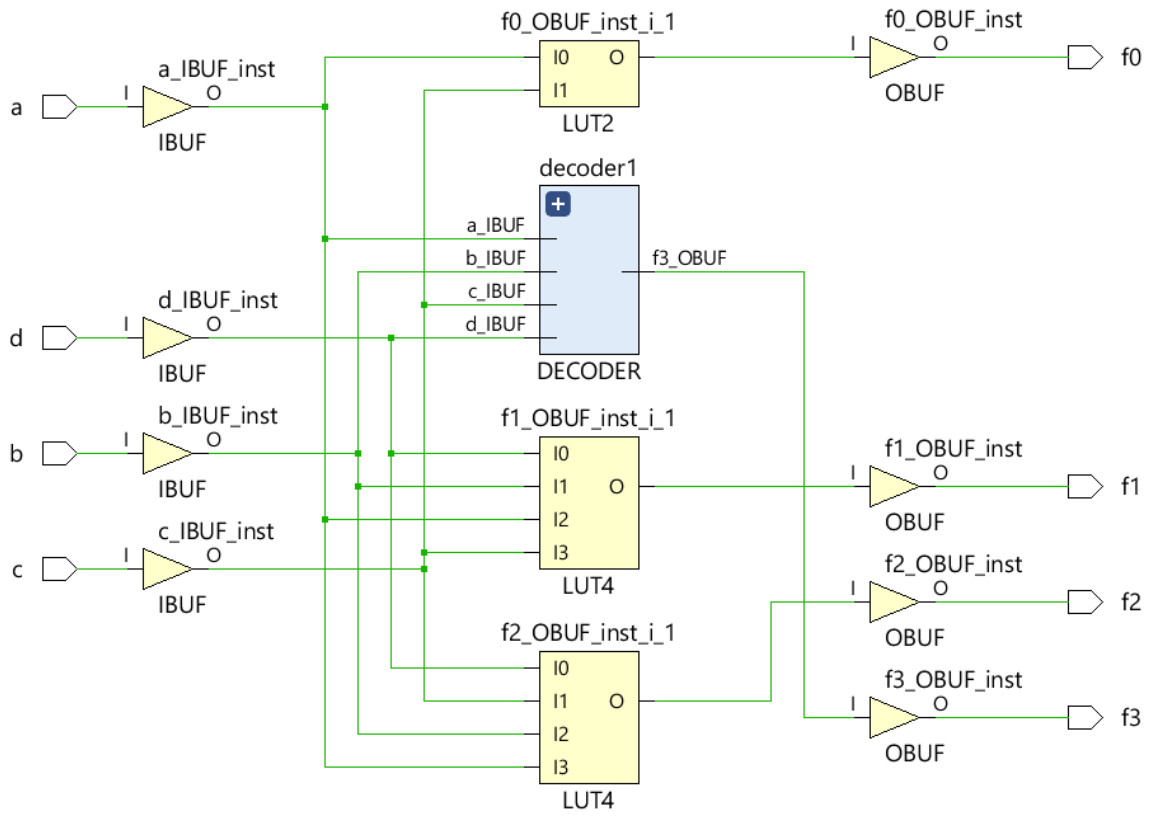
BEHAVİORAL



RTL SHEMATIC



TECHNOLOGY SHEMATIC

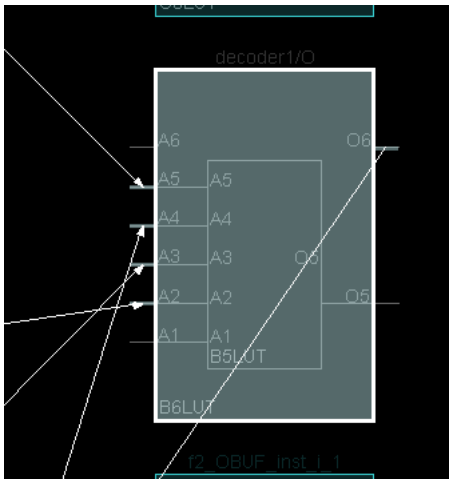


PAD TO PAD

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f0	9.785	SLOW	3.067	FAST
a	f1	9.422	SLOW	2.894	FAST
a	f2	9.496	SLOW	2.978	FAST
a	f3	9.236	SLOW	2.852	FAST
b	f1	8.805	SLOW	2.629	FAST
b	f2	8.881	SLOW	2.715	FAST
b	f3	8.636	SLOW	2.587	FAST
c	f0	9.128	SLOW	2.752	FAST
c	f1	8.556	SLOW	2.521	FAST
c	f2	8.632	SLOW	2.603	FAST
c	f3	8.609	SLOW	2.563	FAST
d	f1	8.545	SLOW	2.558	FAST
d	f2	8.653	SLOW	2.638	FAST
d	f3	8.419	SLOW	2.522	FAST

DEVICE



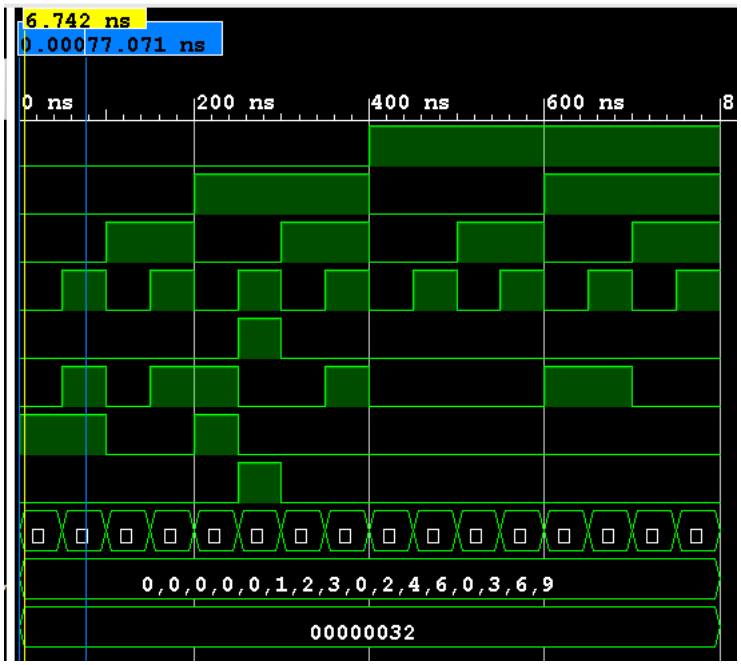
PAD TO PAD

Combinational Delays

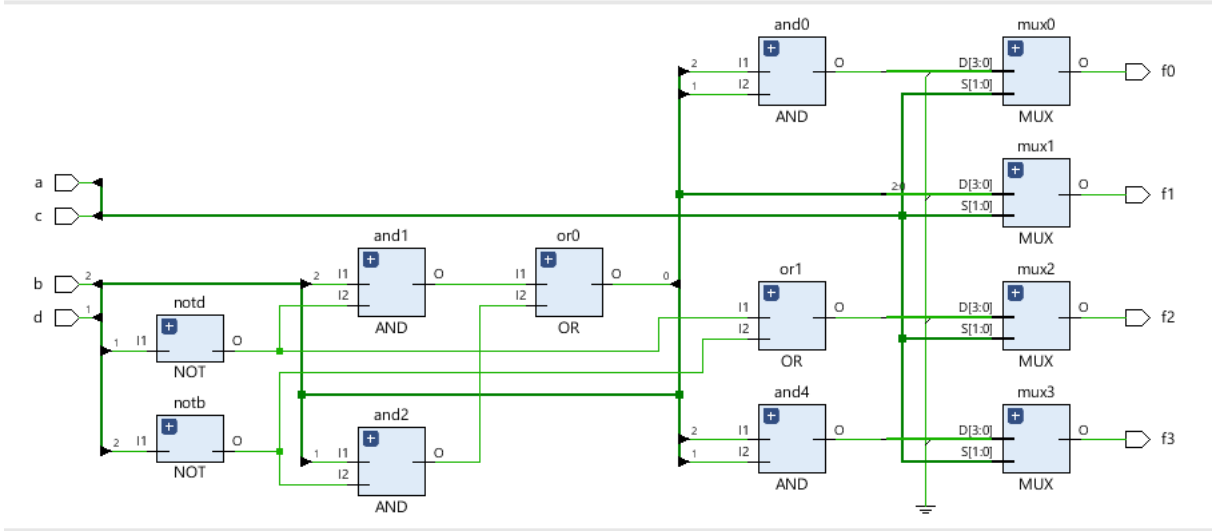
From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f0	9.785	SLOW	3.067	FAST
a	f1	9.422	SLOW	2.894	FAST
a	f2	9.496	SLOW	2.978	FAST
a	f3	9.236	SLOW	2.852	FAST
b	f1	8.805	SLOW	2.629	FAST
b	f2	8.881	SLOW	2.715	FAST
b	f3	8.636	SLOW	2.587	FAST
c	f0	9.128	SLOW	2.752	FAST
c	f1	8.556	SLOW	2.521	FAST
c	f2	8.632	SLOW	2.603	FAST
c	f3	8.609	SLOW	2.563	FAST
d	f1	8.545	SLOW	2.558	FAST
d	f2	8.653	SLOW	2.638	FAST
d	f3	8.419	SLOW	2.522	FAST

MUX

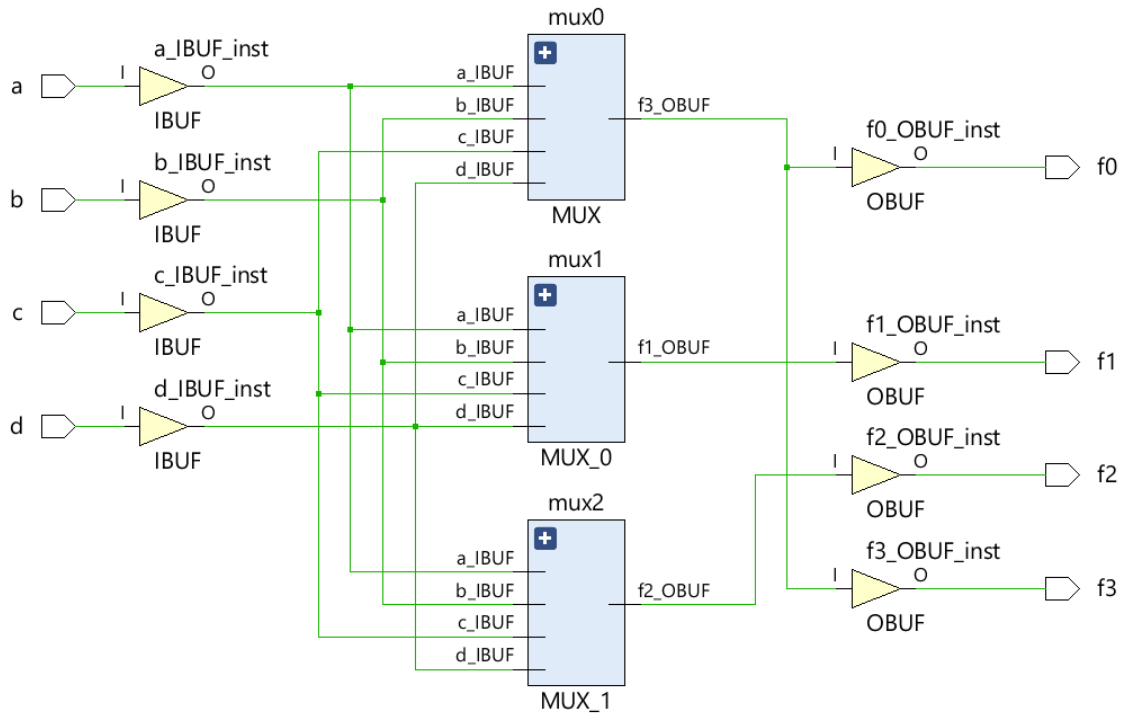
BEHAVIORAL SHEMA



RTL SHEMA



TECHNOLOGY SHEMA

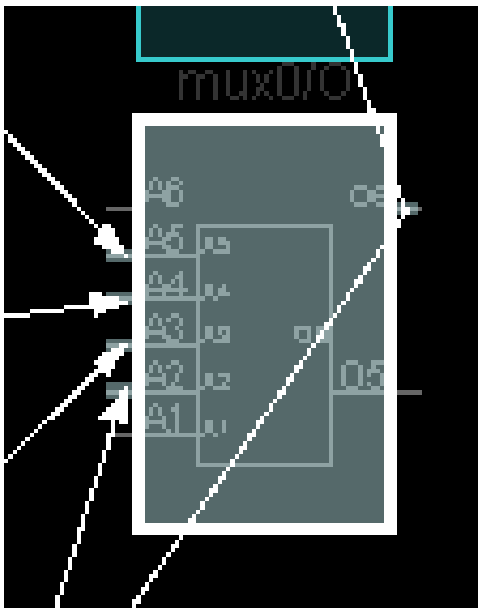


PAD TO PAD

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f0	9.472	SLOW	2.952	FAST
a	f1	9.022	SLOW	2.769	FAST
a	f2	9.728	SLOW	3.059	FAST
a	f3	9.275	SLOW	2.872	FAST
b	f0	8.866	SLOW	2.697	FAST
b	f1	8.431	SLOW	2.513	FAST
b	f2	9.077	SLOW	2.781	FAST
b	f3	8.669	SLOW	2.618	FAST
c	f0	8.608	SLOW	2.577	FAST
c	f1	8.395	SLOW	2.481	FAST
c	f2	8.903	SLOW	2.679	FAST
c	f3	8.411	SLOW	2.497	FAST
d	f0	8.638	SLOW	2.620	FAST
d	f1	8.214	SLOW	2.448	FAST
d	f2	9.037	SLOW	2.754	FAST
d	f3	8.441	SLOW	2.540	FAST

Device



PAD TO PAD MAX DELAY

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f0	9.472	SLOW	2.952	FAST
a	f1	9.022	SLOW	2.769	FAST
a	f2	9.728	SLOW	3.059	FAST
a	f3	9.275	SLOW	2.872	FAST
b	f0	8.866	SLOW	2.697	FAST
b	f1	8.431	SLOW	2.513	FAST
b	f2	9.077	SLOW	2.781	FAST
b	f3	8.669	SLOW	2.618	FAST
c	f0	8.608	SLOW	2.577	FAST
c	f1	8.395	SLOW	2.481	FAST
c	f2	8.903	SLOW	2.679	FAST
c	f3	8.411	SLOW	2.497	FAST
d	f0	8.638	SLOW	2.620	FAST
d	f1	8.214	SLOW	2.448	FAST
d	f2	9.037	SLOW	2.754	FAST
d	f3	8.441	SLOW	2.540	FAST