“ADD_SHIFT_MULTIPLIER” TASK SOLUTION NOTES

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I attempted the task by going through the following steps.

1) I understand the flow of signals by drawing block diagram comprises of “AXI_stream” interfaces for Master and Slave and Multiplier dut.

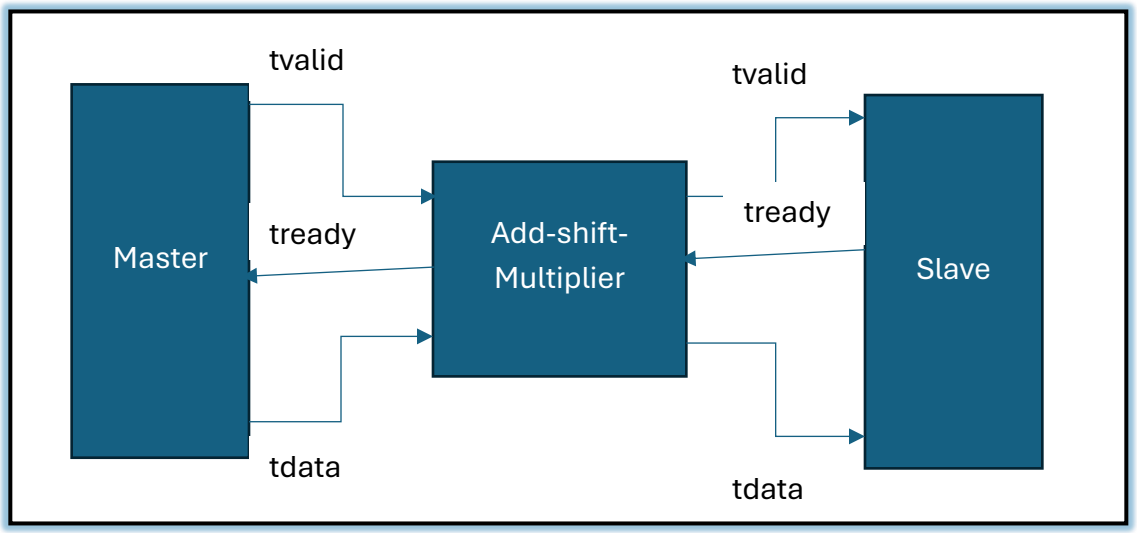

Fig 01: Block Diagram

2) I write the direct testbench and check the behavior of DUT and analyze it through waveform viewer. The direct test bench calculates the result correctly. (note: the direct testbench is shown in comments in the code for reference).

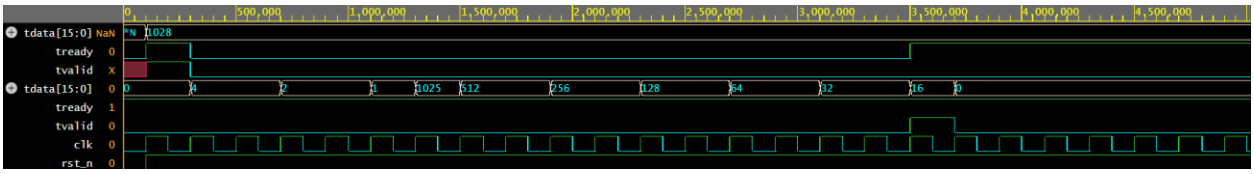

Fig 01: Direct testbench waveform

3) I make the verification plan by listing all the possible testcases.
4) I write the uvm testbench by writing all the required classes (e.g. seq_item, sequence, driver, monitor, scoreboard, coverage etc).
5) The uvm testbench behave just as direct testbench behaves.

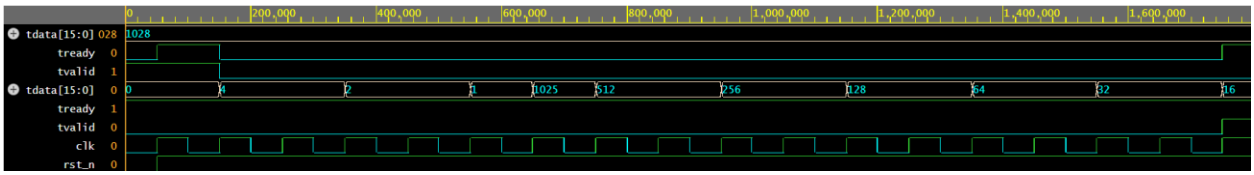

Fig 02: UVM testbench waveform

6) I also point out the bug in the DUT. Which explanation is as below.
   Bug 1: the "iteration" was not properly initialized and reset.
   Bug 2: The FSM may not correctly make transition toward the "output" state.
   Bug 3: The "output" state was not waiting for "tready" before getting back.
   Note: I have resolved these issues by making changes in the code. I have mentioned in the code (with word "Edited" in the comments) where I made change.
7) I have not used "Assertions" in my code because I have not studied and practice in deep, as it is part of formal verification.
8) Verification Plan is attached with this document in the same email.
9) The "EDA playground" link for task is given below.

https://edaplayground.com/x/qwms