UNIVERSITY OF GHANA

BSc. INFORMATION TECHNOLOGY, FIRST SEMESTER EXAMINATIONS 2021/2022

DEPARTMENT OF DISTANCE EDUCATION

CSIT 307: DIGITAL AND LOGIC DESIGN (3 CREDITS)

INSTRUCTIONS:

Answer ALL Questions in section A

Answer any two (2) Question from section B

TIME ALLOWED:

TWO (2) HOURS

SECTION A [30 Marks]

Answer ALL questions in this section.

1. Explain the theory of computation and state its significance in the design of digital logic systems [5 Marks]
2. Give a formal definition of a finite state automata with output [4 Marks]
3. In the design of ALU of a particular modern CPU, a combinational logic circuit is required to perform arithmetic difference of any single bit input from the memory to the CPU. Design a combination logic circuit that would accomplish this task Show truth tables, logic equations and circuit diagram [13 Marks]
4. Explain the T-Flip flop and state its significance in logic circuit design [4 Marks]

A5. Describe the behavior of sequential and combinational logic circuits. [4 Marks]

SECTION B [70 Marks]

Answer <u>ANY TWO (2)</u> Questions in this section

1.

(a) Design an encoder that takes Hexadecimal input signal and encode it to generate corresponding binary output signal. [10 Marks]

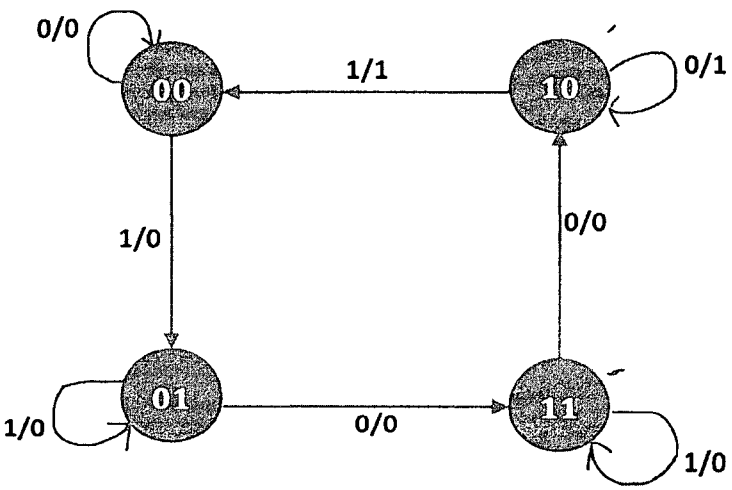
(b) Design a BCD to 7-segment decoder, which takes a BCD input, and display the corresponding decimal number. Your solution should include the truth table and the circuit diagram. [10 Marks]

(c) Describe the behavior of a NAND JK Flip Flop using characteristic table and show how this can be used to design a digital circuit that requires D Flip Flop. [15 Marks]

2.

(a) Design clock sequential logic circuit that would recognize the input string `1101` using D flip-flops. Assuming the input string is `1101101100101101100` with overlap allowed. You are required to derive Mealy state diagram, state tables, state equation and draw the resultant sequential circuit diagram. [20 Marks]

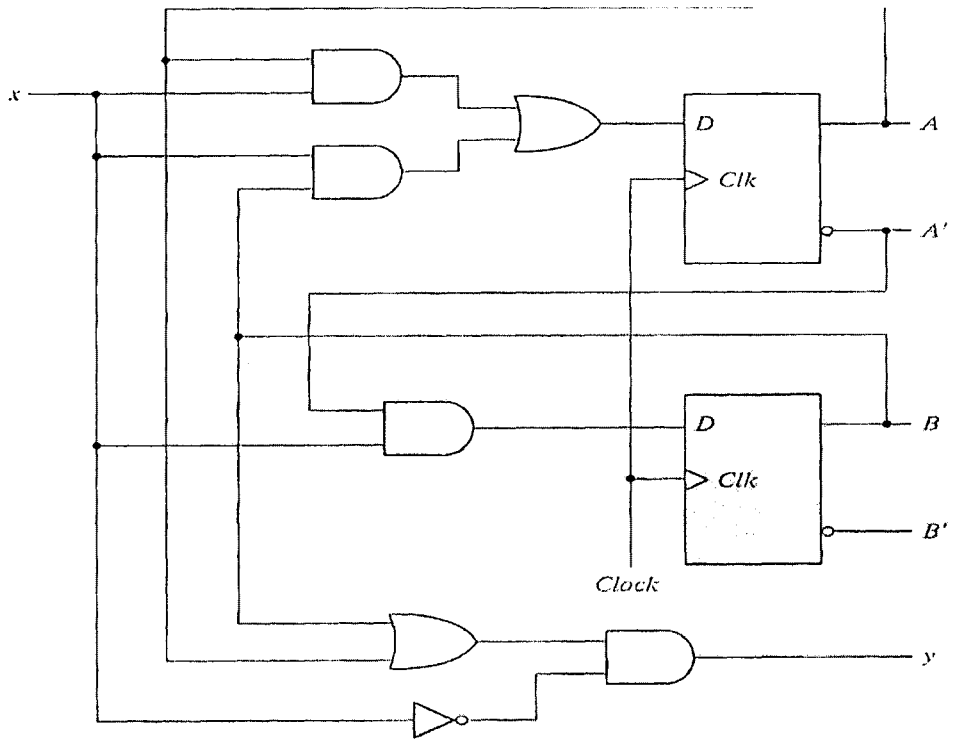
(b) Given the state diagram below, construct, derive the state table and state equations. Based on the state equations, construct the appropriate circuit diagram modeled by the state diagram. [15 Marks]



3.

(a) Implement the function f (a, b, c) =∑m(2, 3, 5, 6) with a 4-to-1 MUX and selection inputs a, b [15 Marks]

(b) Obtain the state equation, state table and state diagram that models the behavior of the circuit diagram presented below. [20 Marks]



(c) Design a combinational logic circuit diagram that can perform arithmetic sum of three input bits. Show truth tables, logic equations and circuit diagram. [12 Marks]