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UNIVERSITY OF GHANA

B.SC INFORMATION TECHNOLOGY, FIRST SEMESTER EXAMINATIONS: 2016/2017

CSCD 211: COMPUTER ORGANISATION AND ARCHITECTURE (3 CREDITS)

INSRUCTIONS

SECTION A:

ANSWER ALL QUESTIONS IN THIS SECTION

NB: ALL QUESTIONS THAT INVOLVE CALCULATION, YOU ARE REQUIRED TO SHOW ALL STEPS USED IN ARRIVING AT THE FINAL ANSWER.

SECTION B:

ANSWER ANY ONE (1) QUESTION FROM THIS SECTION

TIME ALLOWED:

TWO AND A HALF (2½) HOURS

SECTION A [50 MARKS]

QUESTION 1[14 marks]

a. Explain the main characteristics of the Von Neumann Architecture that makes its choice less desirable compared to the Harvard Architecture **[3 marks]**
b. Explain how the memory hierarchy helps in solving the design constraint of computers' memory **[2 marks]**
c. Explain the concept of byte addressability **[2 marks]**
d. What is Bi-endian Processor?. **[2 mark]**
e. Describe the motivation of the CISC architecture that would make its choice paramount over the RISC architecture **[2 marks]**
f. State the purpose of the memory buffer register (MBR) **[1 marks]**
g. Explain why SRAM is faster than DRAM **[2 mark]**

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QUESTION 2[15 marks]

a. Write a RISC-style program that accomplishes the expression below using 2-address instruction with Register –Memory Architecture:

   $A = (X + Y * Z)/(K - M * N)$ **[4 marks]**

b. Given a 32-bit word represented by the hexadecimal equivalent **0x0A050C08**, stored in memory location K.

   i. Show how this word would be stored with byte-addressability using little-endian **[2 marks]**

   ii. State the consecutive memory addresses where each byte of data would be stored **[2 marks]**

c. Explain the condition under which word locations in memory are considered as having *aligned addresses*? **[2 marks]**

d. What is an advantage of a 3-operand ISA over a 2-operand ISA?**[3 mark]**

e. Explain indirect addressing mode given example **[2 mark]**

QUESTION 3 [21 marks]

a. Compute the expression $A7CF_{16}$- 122020_8 in hexadecimal and leave your answer in binary **[2 marks]**

b. Computer the expression -4197_{10}-1812_{10} in 9's compliment and leave your final answer in hexadecimal. **[3 marks]**

c. Compute 345_{10}+865_{10} in BCD leaving your final answer in decimal **[3 marks]**

d. Compute 1101110101_2 *1111100011_2*1101001_2 and leave your final answer in octal. **[3 marks]**

e. Compute $23EF_{16}$*$1F49_{16}$+$EAB4_{16}$ leaving your answer in binary **[3 marks]**

f. Write 147.625 in its hexadecimal representation in IEEE-754 floating-point format. **[4 marks]**

g. Convert the following numbers into their respective equivalent

   i. 5613.90625_{10} to binary **[1 mark]**

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ii. $4740.625 * 10^{-2}{}_{10}$ to binary **[1 mark]**

iii. 1110011011010.0011_2 to denary **[1 mark]**

SECTION B:
ANSWER ANY ONE (1) QUESTION FROM THIS SECTION

QUESTION1 [20 marks]

a. Use Boolean algebra to simplify the following expression, then draw a logic gate circuit for the simplified expression using only NAND gate

$f = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + A\,\overline{B}\,\overline{C} + A\,\overline{B}C + \overline{D}$ **[4 marks]**

b. A program runs in 10 sec on MIPS Processor, which has a 400MHz clock. We are trying to design a new Processor AZIPRO processor with faster clock rate so as to reduce the execution time to 6 sec. The increase of clock rate will affect the rest of the CPU design, causing B to require 1.2 times as many clock cycles as the MIPS Processor for this program. What clock rate should AZIPRO be?

[3 marks]

c. A new CPU executed 10GB of instruction with a average of 2.5 cycles for each instruction. The clock cycle rate is 200MHz with a clock cycle of 5 nano second. What is the execution time for this program? **[4 marks]**

d. Given the function below [6 marks]

F (w, x, y, z) = Σ(2, 3, 10, 11, 12, 13, 14, 15)

a. Write the function in disjunctive normal form
b. Simplify the expression using k-map
c. Indicate the gate count

d. Construct a block diagram of a ripple Look Ahead binary subtractor which uses Full substactor to illustrate the computation of 5-bit binary expression
11010_2-11011_2 **[3 marks]**

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QUESTION2[20 marks]

a. What is instruction pipelining of the processor and how it affect performance [**2 marks]**

b. Given each instruction, what is the single-cycle datapath? **[2 marks]**

c. In the a particular super scalar machine the 50% of the program instructions is executed with 3 parallel issues, while the fraction of remaining instructions (50%) is executed with one issue. **[4 marks]**

i. How much is the **SpeedUp** from the case (1) to the case (2)?

ii. How much is the **Throughput2** expressed in MIPS?

d. You are required to write a program segment that can perform the operation C →A+ B where each of A and B represents a set of 100 memory locations each storing a value such that the set of values represented by A are stored starting at memory location 1000 and those represented by B are stored starting at memory location 2000.
The results should be stored starting at memory location 3000. The above operation is to be performed using each of the following instruction classes. **[6 marks]**

h. A machine with one-address instructions
i. A machine with two-address instructions
j. A machine with three-address instructions

e. Suppose a program spends 80% of its time in a square root routine. How much must you speed up square root to make the program run 5 times faster? **[2 marks]**

f.

g. In a certain system the main memory access time is 100 ns. The cache is 10 times faster than the main memory and uses the write though protocol. If the hit ratio for read request is 0.92 and 85% of the memory requests generated by the CPU are for read, the remaining being for write; what is the average time consideration both read and write **[4 marks]**