Test Object - Device Settings

Substation/Bay:

Substation:	Substation address:
Bay:	Bay address:

Device:

Name/description:	OCP relay - UMZ10	Manufacturer:	ABB
Device type:	REF615	Device address:	
Serial/model number:			
Additional info 1:	Yazan Eissa, lawal ibrahim		
Additional info 2:	s0574690,s0596159		

Hardware Configuration

Test Equipment

Type	Serial Number
CMC156	NC693N

Hardware Check

Performed At	Result	Details
19.11.2024 13:39:07	Passed	

Ramping:

Test Settings

General

No. of ramp states:	2
Total steps per test:	102
Total time per test:	10,200 s
No. of test executions:	1
Input Mode:	Direct
Fault Type:	

Ramped Quantities

I L1; L2; L3 / Magnitude

Ramp States

Ramp	Ramp 1	Ramp 2
I L1	900,0 mA 0,00 ° 50,000 Hz	1,400 A 0,00 ° 50,000 Hz
I L2	900,0 mA -120,00 ° 50,000 Hz	1,400 A -120,00 ° 50,000 Hz
I L3	900,0 mA 120,00 ° 50,000 Hz	1,400 A 120,00 ° 50,000 Hz
Force abs. Phases	No	No
Sig 1 From	900,0 mA	1,400 A
Sig 1 To	1,400 A	900,0 mA
Sig 1 Delta	10,00 mA	-10,00 mA

Sig 1 d/dt	100,0 mA/s	-100,0 mA/s
dt per Step	100,0 ms	100,0 ms
Ramp Steps	51	51
Ramp Time	5,100s	5,100s
Trigger	Bin	Bin
Trigger Logic	OR	OR
Trip	X	X
Start	1	0
Step back	No	No
Delay Time	0,000 s	0,000 s

Test Module

Name:	OMICRON Ramping	Version:	4.31
Test Start:	19-Nov-2024 15:19:19	Test End:	19-Nov-2024 15:19:23
User Name:		Manager:	
Company:			

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pick-up	Ramp 1	Start 0->1	I L1; L2; L3	1,000 A	1,010 A	15,00 mA	15,00 mA	10,00 mA	+	13,60
Drop-off	Ramp 2	Start 1->0	I L1; L2; L3	950,0 mA	960,0 mA	15,00 mA	15,00 mA	10,00 mA	+	56,30

Assess: + .. Passed   x .. Failed   o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed   x .. Failed   o .. Not assessed

Calculation Results

Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
Drop-off/Pick-up	X/Y	Drop-off	Pick-up	0,9500	0,9505			0,0005000	+

Assess: + .. Passed   x .. Failed   o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed   x .. Failed   o .. Not assessed
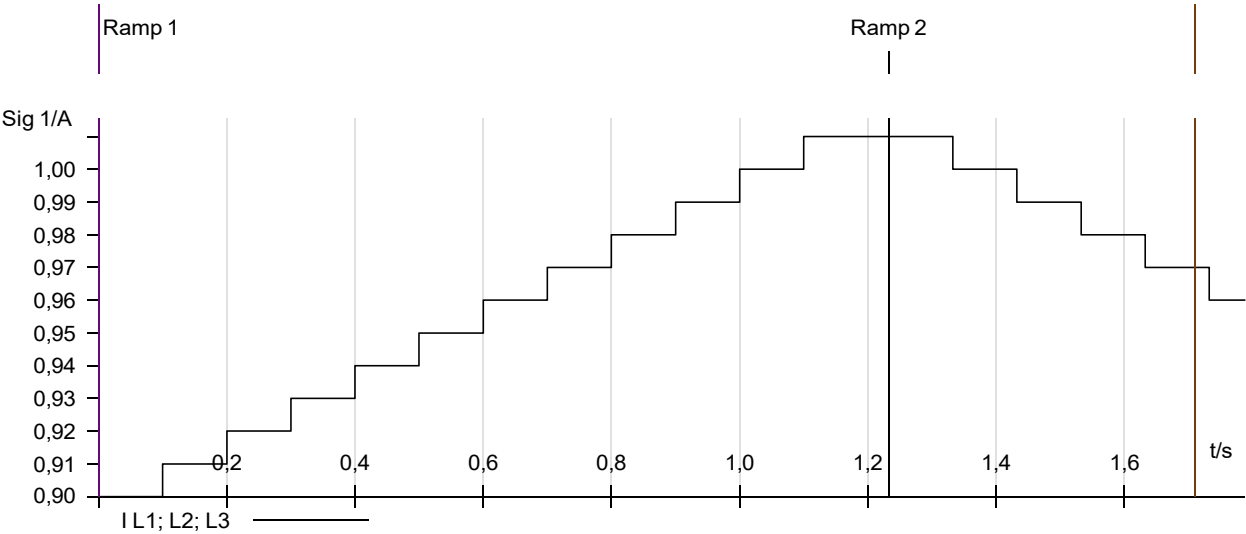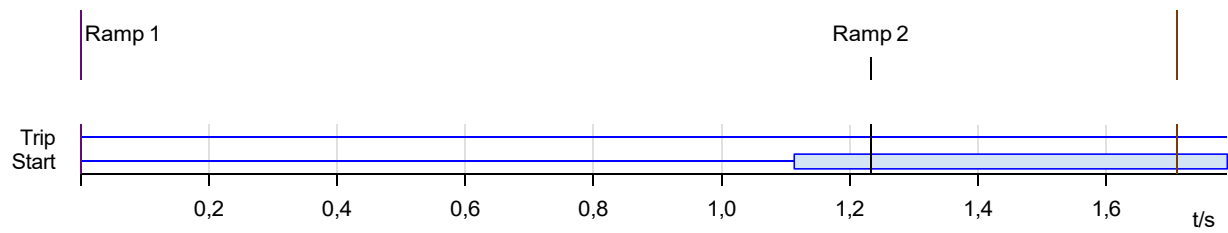
Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	\<none\>	n/a
Cursor 2	1,711 s	\<none\>	n/a
C2 - C1	1,711 s		n/a

Test State:
  Test passed

2A Pulse Ramping:

Test Settings

Ramp parameters

Outputs	Quantity	From	To	Δ	TFault	TReset	Steps	Duration
I L1;I L2;I L3	Magnitude	1,700 A	2,600 A	30,00 mA	1,100 s	300,0 ms	31	43,50 s

States

State	Reset State	Fault State
I L1	0,000 A 0,00 ° 50,00 Hz	1,700 A 0,00 ° 50,00 Hz
I L2	0,000 A -120,00 ° 50,00 Hz	1,700 A -120,00 ° 50,00 Hz
I L3	0,000 A 120,00 ° 50,00 Hz	1,700 A 120,00 ° 50,00 Hz
Diagrams		

Test Conditions:

Start Test:	Immediately
Prefault time:	100,0 ms
Stop ramp on assessment:	Yes
Delay after assessment:	0,000 s

Fault Calculator:

Table Inputmode	Parameters		
Direct	I L1	1,700 A	0,00 °	50,00 Hz
	I L2	1,700 A	-120,00 °	50,00 Hz
	I L3	1,700 A	120,00 °	50,00 Hz

Comment

Test Module

Name:	OMICRON Pulse Ramping	Version:	4.31
Test Start:	19-Nov-2024 15:10:39	Test End:	19-Nov-2024 15:10:57
User Name:		Manager:	
Company:			

Test Results

Threshold	Assess on	Nom	Tol+	Tol-	Act	Dev	Assess
Magnitude I L1;I L2;I L3	Trip 0>1	2,000 A	1,5 %	1,5 %	2,030 A	1,5 %	+

Assess: + .. Passed   x .. Failed   o .. Not assessed

Time at assessment: 917,9 ms

Ramped output/A

I L1 ——   I L2 ——   I L3 ——

CMC156 Current/A

I L1 ——   I L2 ——   I L3 ——

Trip
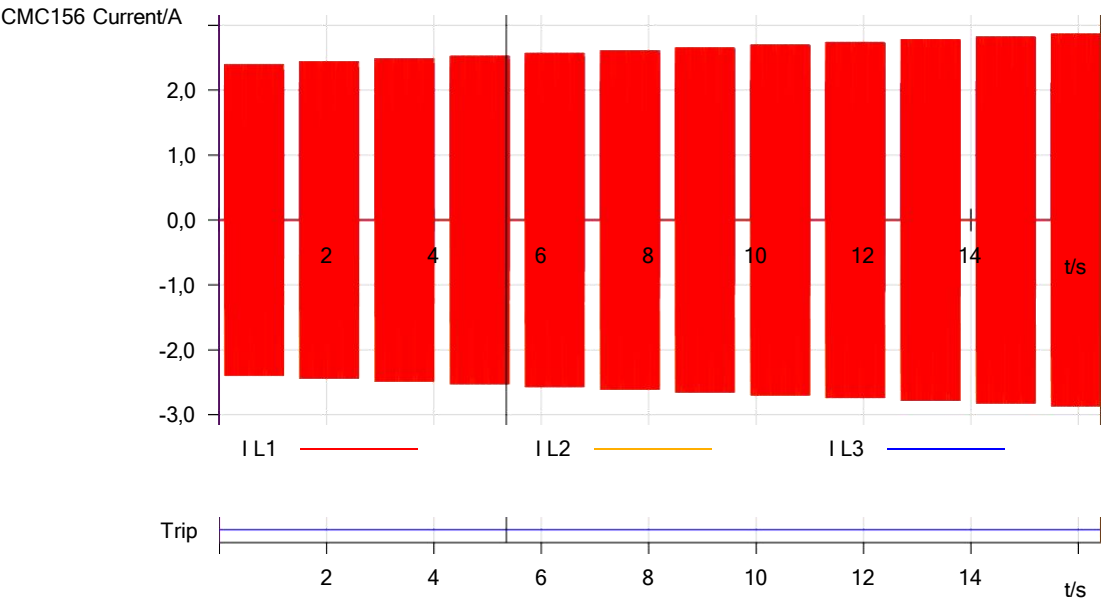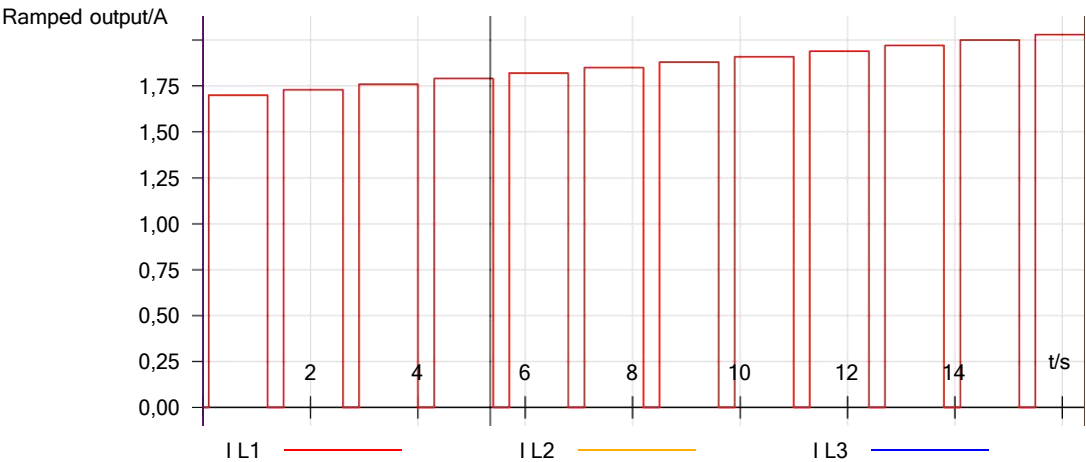
Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	16,42 s	<none>	n/a
C2 - C1	16,42 s		n/a

8A Pulse Ramping:

Test Settings

Ramp parameters

Outputs	Quantity	From	To	Δ	TFault	TReset	Steps	Duration
I L1;I L2;I L3	Magnitude	6,400 A	9,600 A	35,00 mA	500,0 ms	150,0 ms	93	60,55 s

States

State	Reset State	Fault State
I L1	0,000 A 0,00 ° 50,00 Hz	6,400 A 0,00 ° 50,00 Hz
I L2	0,000 A -120,00 ° 50,00 Hz	6,400 A -120,00 ° 50,00 Hz
I L3	0,000 A 120,00 ° 50,00 Hz	6,400 A 120,00 ° 50,00 Hz
Diagrams		

Test Conditions:

Start Test:	Immediately
Prefault time:	100,0 ms
Stop ramp on assessment:	Yes
Delay after assessment:	0,000 s

Fault Calculator:

Table Inputmode	Parameters			
Direct	I L1	6,400 A	0,00 °	50,00 Hz
	I L2	6,400 A	-120,00 °	50,00 Hz
	I L3	6,400 A	120,00 °	50,00 Hz

Comment

Test Module

Name:	OMICRON Pulse Ramping	Version:	4.31
Test Start:	19-Nov-2024 15:16:33	Test End:	19-Nov-2024 15:17:04
User Name:		Manager:	
Company:			

Test Results

Threshold	Assess on	Nom	Tol+	Tol-	Act	Dev	Assess
Magnitude I L1;I L2;I L3	Trip 0>1	8,000 A	1,5 %	1,5 %	7,975 A	-0,3125 %	+

Assess: + .. Passed   x .. Failed   o .. Not assessed

Time at assessment: 408,4 ms
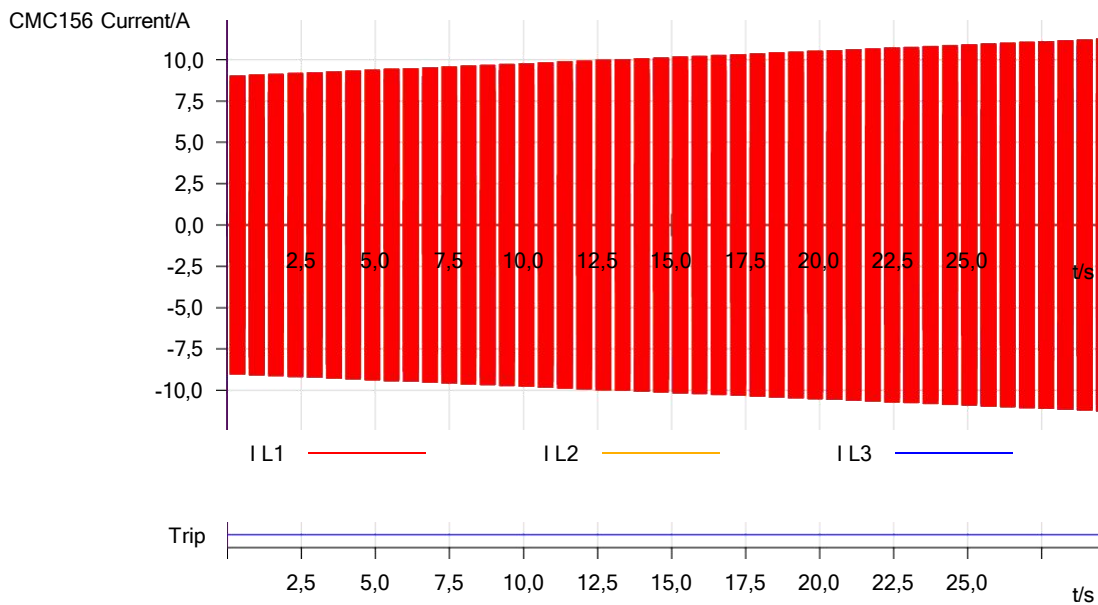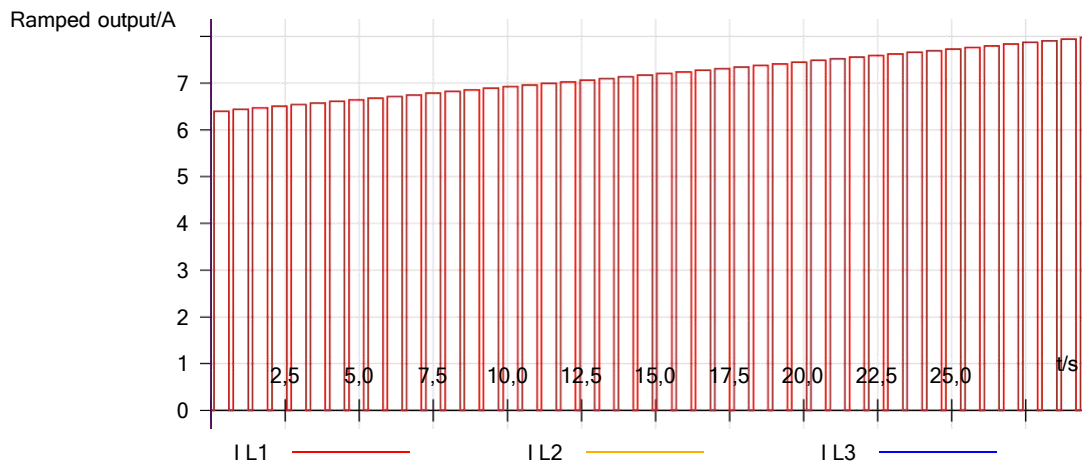
Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	\<none\>	n/a
Cursor 2	29,76 s	\<none\>	n/a
C2 - C1	29,76 s		n/a

Test State:
   Test passed

Overcurrent:
Test Object - Overcurrent Parameters

General - Values:

TimeTolAbs:	0,04 s	VT connection:	n/a
TimeTolRel:	5,00 %	CT starpoint connection:	n/a
CurrentTolAbs:	0,05 Iref		
CurrentTolRel:	5,00 %		
Directional:	No		

Elements - Phase:

Active	Name	Tripping characteristic	I Pick-up	Time	Reset Ratio	Direction
Yes	I >	IEC Definite Time	1,00 Iref	1,50 s	0,95	Non Directional
Yes	I >>	IEC Definite Time	2,00 Iref	0,90 s	0,95	Non Directional
Yes	I >>>	IEC Definite Time	8,00 Iref	0,40 s	0,95	Non Directional

Elements - Residual:

Active	Name	Tripping characteristic	I Pick-up	Time	Reset Ratio	Direction
Yes	I E>	IEC Definite Time	0,20 Iref	0,50 s	0,95	Non Directional

Test Module

Name:	OMICRON Overcurrent	Version:	4.31
Test Start:	19-Nov-2024 15:04:06	Test End:	19-Nov-2024 15:04:41
User Name:		Manager:	
Company:			

Test Settings:

Fault Model:

Time reference:	Fault inception
Load current:	0,000 A
Load angle:	n/a
Prefault time:	100,0 ms
Abs. max time:	3,000 s
Post fault time:	500,0 ms
Rel. max time:	100,0 %
Enable voltage output:	No
Fault voltage LN (for all but two phase faults):	n/a
Fault voltage LL (for two phase faults):	n/a
Decaying DC active:	No
Time constant:	n/a
CB char min time:	50,00 ms
Thermal reset active:	No
Thermal reset method:	n/a
Thermal reset message:	n/a

Shot Test:

Type	Relative To	Factor	Magnitude	Angle	tnom	tmin	tmax
L1-E	I >	800,0 m	800,0 mA	n/a	500,0 ms	460,0 ms	540,0 ms
L1-E	I >>	1,100	2,200 A	n/a	500,0 ms	460,0 ms	540,0 ms
L1-E	I >>>	800,0 m	6,400 A	n/a	500,0 ms	460,0 ms	540,0 ms
L2-E	I >	1,100	1,100 A	n/a	500,0 ms	460,0 ms	540,0 ms
L2-E	I >>	800,0 m	1,600 A	n/a	500,0 ms	460,0 ms	540,0 ms
L1-L2	I >	1,100	1,100 A	n/a	1,500 s	1,425 s	1,575 s
L1-L2	I >>	800,0 m	1,600 A	n/a	1,500 s	1,425 s	1,575 s
L1-L2	I >>>	1,100	8,800 A	n/a	400,0 ms	360,0 ms	440,0 ms
L2-L3	I >	800,0 m	800,0 mA	n/a	No trip	No trip	No trip
L2-L3	I >>	1,100	2,200 A	n/a	900,0 ms	855,0 ms	945,0 ms
L2-L3	I >>>	800,0 m	6,400 A	n/a	900,0 ms	855,0 ms	945,0 ms
L3-L1	I >	800,0 m	800,0 mA	n/a	No trip	No trip	No trip
L3-L1	I >>	1,100	2,200 A	n/a	900,0 ms	855,0 ms	945,0 ms
L3-L1	I >>>	800,0 m	6,400 A	n/a	900,0 ms	855,0 ms	945,0 ms
L3-L1	I >>	1,000	2,000 A	n/a	900,0 ms	855,0 ms	1,575 s
L3-L1	I >>>	1,300	10,40 A	n/a	400,0 ms	360,0 ms	440,0 ms
L3-E	I >>>	1,300	10,40 A	n/a	400,0 ms	360,0 ms	440,0 ms

Binary Inputs:

Trigger Logic: And

Name	Trigger State
Trip	1
Start	X

Shot Test Results:

Type	Relative To	Factor	Magnitude	Angle	tnom	tact	Deviation	Overload	Result
L1-E	I >	800,0 m	800,0 mA	n/a	500,0 ms	502,6 ms	0,5200 %	No	Passed
L1-E	I >>	1,100	2,200 A	n/a	500,0 ms	500,8 ms	0,1600 %	No	Passed
L1-E	I >>>	800,0 m	6,400 A	n/a	500,0 ms	501,0 ms	0,2000 %	No	Passed
L2-E	I >	1,100	1,100 A	n/a	500,0 ms	502,8 ms	0,5600 %	No	Passed
L2-E	I >>	800,0 m	1,600 A	n/a	500,0 ms	501,3 ms	0,2600 %	No	Passed
L1-L2	I >	1,100	1,100 A	n/a	1,500 s	1,517 s	1,120 %	No	Passed
L1-L2	I >>	800,0 m	1,600 A	n/a	1,500 s	1,512 s	0,7667 %	No	Passed
L1-L2	I >>>	1,100	8,800 A	n/a	400,0 ms	411,6 ms	2,900 %	No	Passed
L2-L3	I >	800,0 m	800,0 mA	n/a	No trip	No trip	n/a	No	Passed
L2-L3	I >>	1,100	2,200 A	n/a	900,0 ms	916,0 ms	1,778 %	No	Passed
L2-L3	I >>>	800,0 m	6,400 A	n/a	900,0 ms	903,9 ms	0,4333 %	No	Passed
L3-L1	I >	800,0 m	800,0 mA	n/a	No trip	No trip	n/a	No	Passed
L3-L1	I >>	1,100	2,200 A	n/a	900,0 ms	917,2 ms	1,911 %	No	Passed
L3-L1	I >>>	800,0 m	6,400 A	n/a	900,0 ms	903,8 ms	0,4222 %	No	Passed
L3-L1	I >>	1,000	2,000 A	n/a	900,0 ms	1,510 s	67,77 %	No	Passed
L3-L1	I >>>	1,300	10,40 A	n/a	400,0 ms	409,1 ms	2,275 %	No	Passed
L3-E	I >>>	1,300	10,40 A	n/a	400,0 ms	410,2 ms	2,550 %	No	Passed

Charts for Fault Types:

Type	Angle
L1-E	n/a
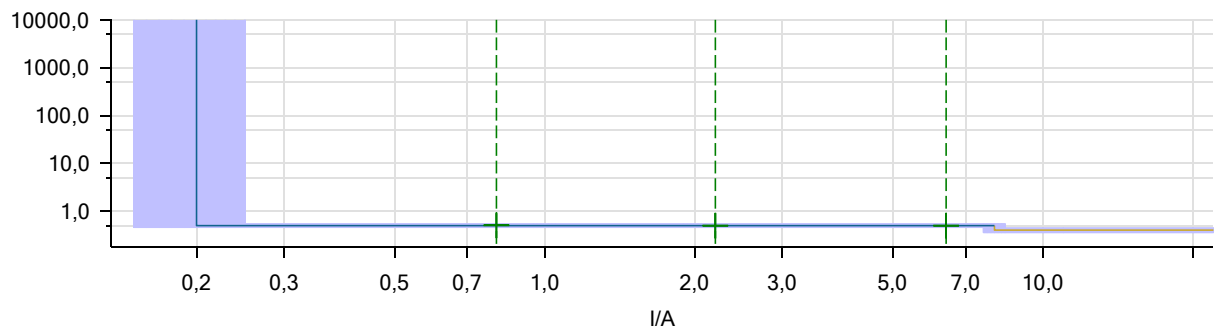
Charts for Fault Types:

Type	Angle
L2-E	n/a
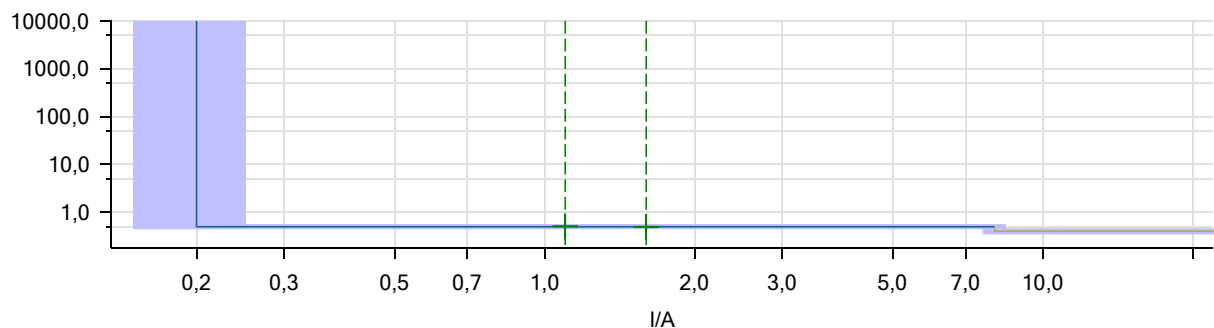
Charts for Fault Types:

Type	Angle
L1-L2	n/a
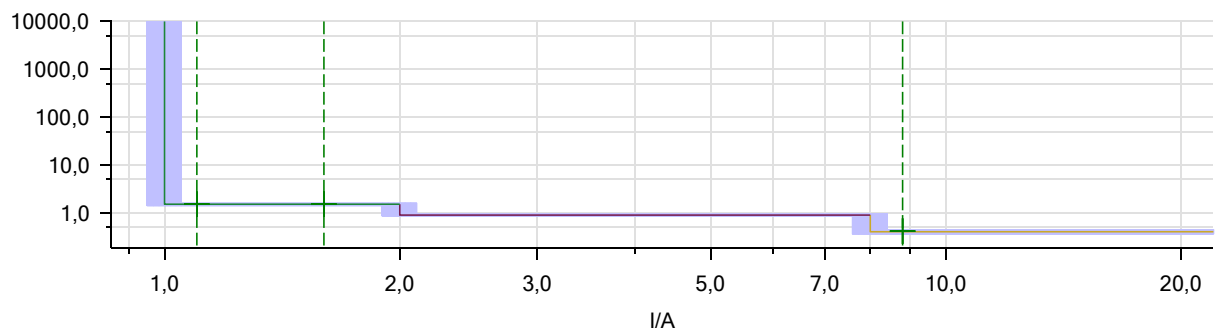
Charts for Fault Types:

Type	Angle
L2-L3	n/a
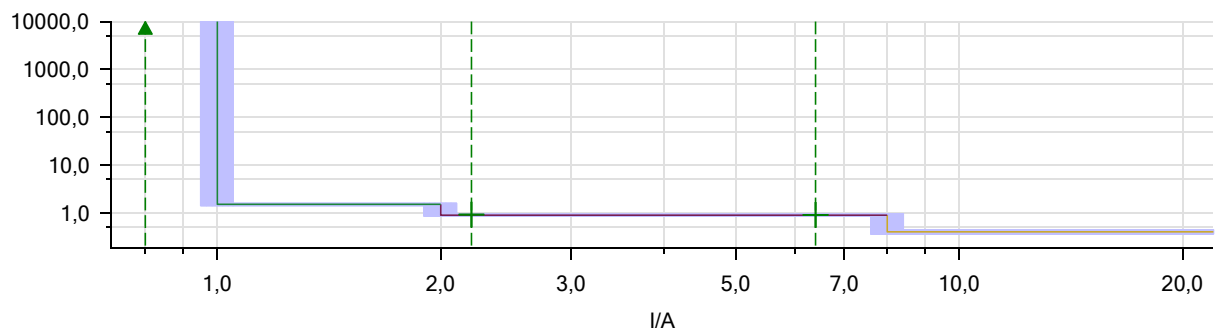
Charts for Fault Types:

Type	Angle
L3-L1	n/a
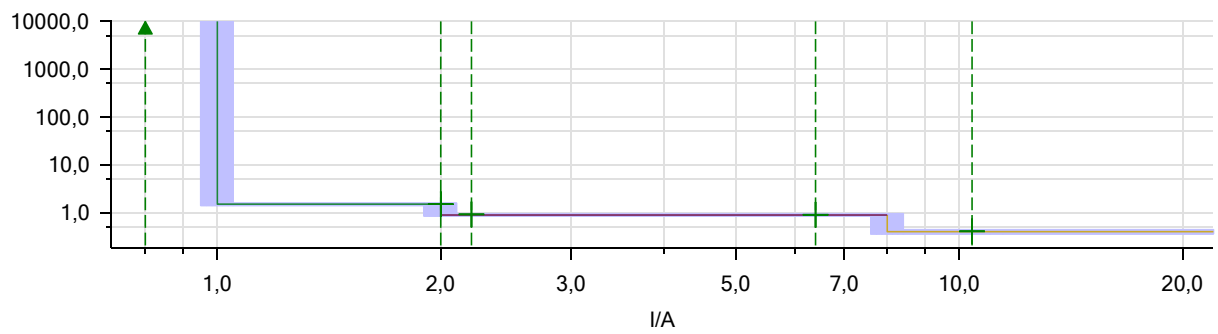
Charts for Fault Types:

Type	Angle
L3-E	n/a
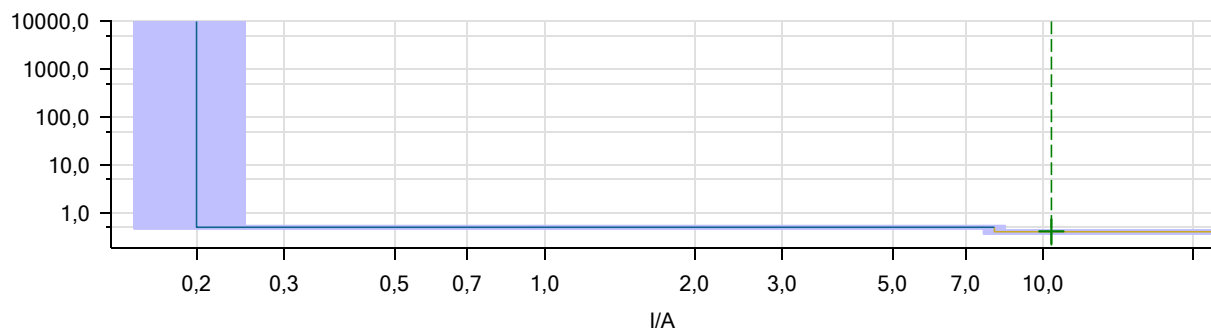
Test State:
17 out of 17 points tested.
17 points passed.
0 points failed.

Test passed

Earth Ramping:

Test Settings

General

No. of ramp states: 2
Total steps per test: 182
Total time per test: 18,200 s
No. of test executions: 1

Input Mode: Direct
Fault Type:

Ramped Quantities

I L1 / Magnitude

Ramp States

Ramp	Ramp 1	Ramp 2
I L1	170,0 mA 0,00 ° 50,000 Hz	260,0 mA 0,00 ° 50,000 Hz
I L2	0,000 A -120,00 ° 50,000 Hz	0,000 A -120,00 ° 50,000 Hz
I L3	0,000 A 120,00 ° 50,000 Hz	0,000 A 120,00 ° 50,000 Hz
Force abs. Phases	No	No
Sig 1 From Sig 1 To Sig 1 Delta Sig 1 d/dt	170,0 mA 260,0 mA 1,000 mA 10,00 mA/s	260,0 mA 170,0 mA -1,000 mA -10,00 mA/s
dt per Step Ramp Steps Ramp Time	100,0 ms 91 9,100s	100,0 ms 91 9,100s
Trigger	Bin	Bin
Trigger Logic Trip Start	OR X 1	OR X 0
Step back Delay Time	No 0,000 s	No 0,000 s

Test Module

Name: OMICRON Ramping   Version: 4.31
Test Start: 19-Nov-2024 15:28:55   Test End: 19-Nov-2024 15:29:01
User Name: Manager:
Company:

Test Results

Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Pick-up	Ramp 1	Start 0->1	I L1	200,0 mA	200,0 mA	3,000 mA	3,000 mA	0,000 A	+	37,50
Drop-off	Ramp 2	Start 1->0	I L1	190,0 mA	192,0 mA	3,000 mA	3,000 mA	2,000 mA	+	19,40

Assess: + .. Passed   x .. Failed   o .. Not assessed

Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed   x .. Failed   o .. Not assessed

Calculation Results

Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
Drop-off/Pick-up	X/Y	Drop-off	Pick-up	0,9500	0,9600			0,01000	+

Assess: + .. Passed   x .. Failed   o .. Not assessed

Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess

Assess: + .. Passed   x .. Failed   o .. Not assessed
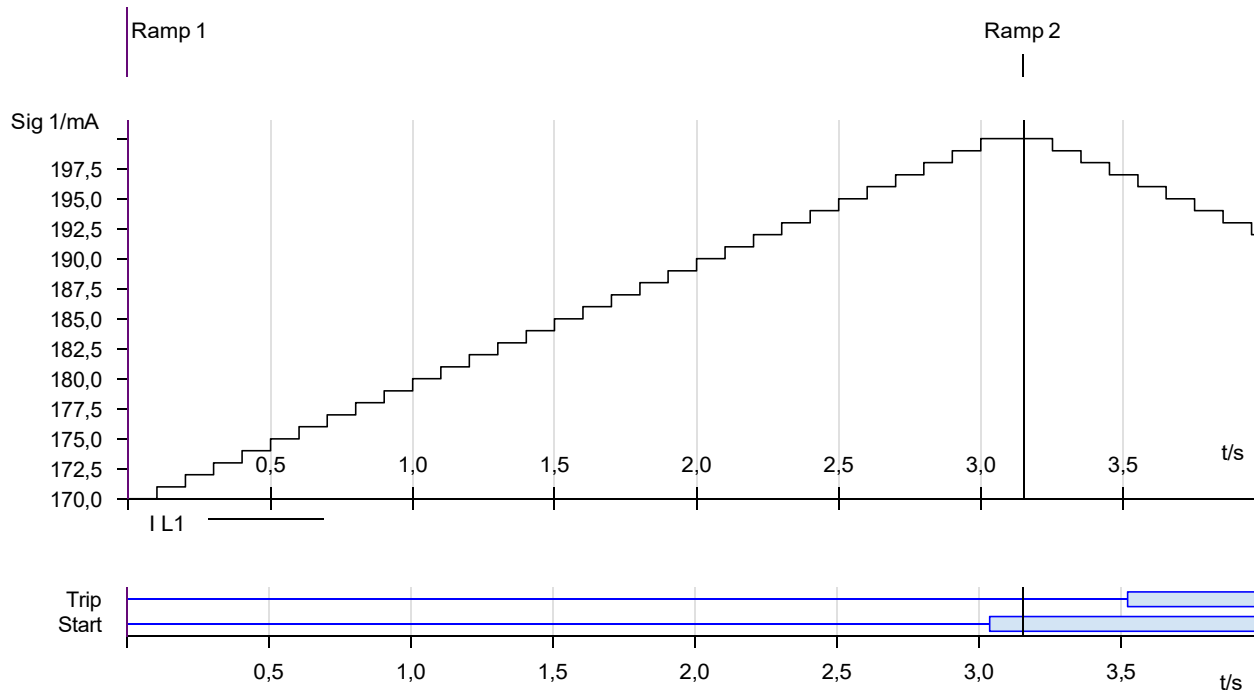
Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	3,973 s	<none>	n/a
C2 - C1	3,973 s		n/a

Pulse Ramping:

Test Settings

Ramp parameters

Outputs	Quantity	From	To	Δ	TFault	TReset	Steps	Duration
I L1	Magnitude	160,0 mA	240,0 mA	20,00 mA	600,0 ms	100,0 ms	5	3,600 s

States

State	Reset State	Fault State
I L1	0,000 A 0,00 ° 50,00 Hz	160,0 mA 0,00 ° 50,00 Hz
I L2	0,000 A -120,00 ° 50,00 Hz	0,000 A -120,00 ° 50,00 Hz
I L3	0,000 A 120,00 ° 50,00 Hz	0,000 A 120,00 ° 50,00 Hz
Diagrams		

Test Conditions:

Start Test:	Immediately
Prefault time:	100,0 ms
Stop ramp on assessment:	Yes
Delay after assessment:	0,000 s

Fault Calculator:

Table Inputmode	Parameters			
Direct	I L1	160,0 mA	0,00 °	50,00 Hz
	I L2	0,000 A	-120,00 °	50,00 Hz
	I L3	0,000 A	120,00 °	50,00 Hz

Comment

Test Module

Name:	OMICRON Pulse Ramping	Version:	4.31
Test Start:	19-Nov-2024 15:34:22	Test End:	19-Nov-2024 15:34:26
User Name:		Manager:	
Company:			

Test Results

Threshold	Assess on	Nom	Tol+	Tol-	Act	Dev	Assess
Magnitude I L1	Trip 0>1	200,0 mA	1,5 %	1,5 %	200,0 mA	0 %	+

Assess: + .. Passed   x .. Failed   o .. Not assessed

Time at assessment: 519,6 ms
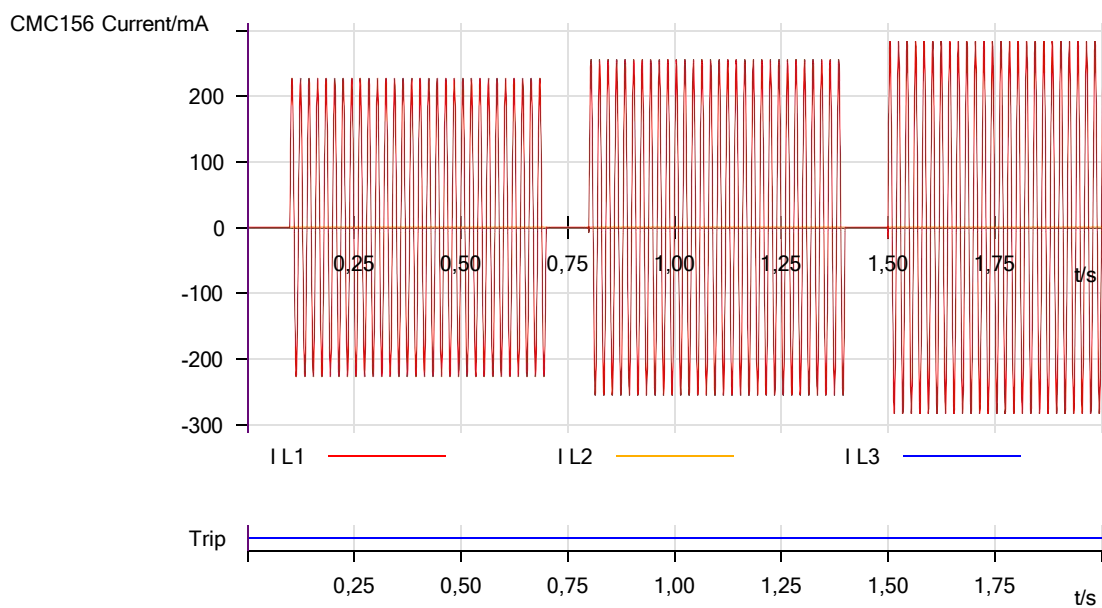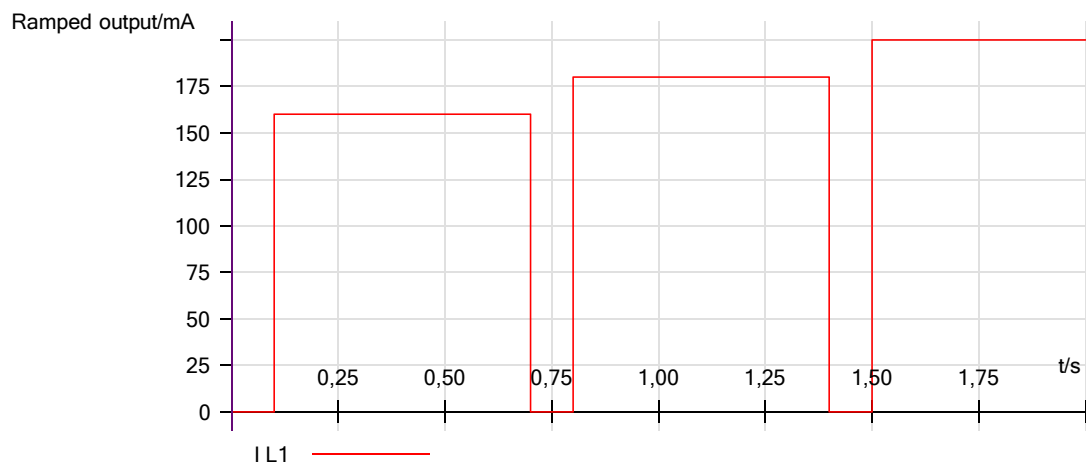
Cursor Data

	Time	Signal	Value
Cursor 1	0,000 s	<none>	n/a
Cursor 2	2,020 s	<none>	n/a
C2 - C1	2,020 s		n/a

Test State:
   Test passed

Challenges Faced:

1. **Binary Input Identification of CMC156 (NC693N):**
   During the initial ramping test, we encountered an issue where the start and trip responses were incorrect. After further investigation, we discovered a discrepancy between the hardware settings and the binary input configuration on our CMC156 (NC693N) device. Specifically, in our hardware settings, the first binary input was designated as "start" and the second as "trip." However, on the CMC156 (NC693N), these signals were reversed—the first input was configured for "trip" and the second for "start." This mismatch necessitated a reconfiguration of the binary inputs on our Omicron device to align with the expected functionality.

2. **Trigger and Stop Condition:**
   After correcting the binary input configuration, we noticed that the test results were still incorrect. Further examination revealed that the triggering state of the ramping test was also incorrectly set were both start and trip conditions configured as (1, 1). This meant that the "start condition" transitioned as (Start 1 -> 0) in both Ramp 1 and Ramp 2, which was inaccurate. While the pick-up condition was correct, the drop-out condition was not in the result of the ramping . We adjusted these settings accordingly, ensuring the proper triggering states for each ramp I.e Ramp 1 for (Start 1 -> 0) and Pramp 2 for (Start0-> 1) , which ultimately led to the successful completion of the ramping test.

3. **Tolerance Percentage Testing:**
   To achieve a precise drop-out and pick-up ratio, we experimented with different tolerance percentages, including 5%, 1.5%, and 1%. During these trials, the system tripped at 0.5%. After consulting the datasheets, we confirmed that for currents less than 10A, a tolerance of 1.5% is recommended. Since all the currents in our tests were below 10A, we adopted a 1.5% tolerance across all our tests to ensure consistent and accurate results.

4. **Earth Ramping and Earth Pulse Ramping:**
   The initial Earth ramping and Earth pulse ramping tests were conducted in three phases, but the results were incorrect. After adjusting the test to a single-phase setup, the test was successful, indicating that our Earth testing requires a single-phase configuration rather than a three-phase setup for accurate results.

5. **Overall Test Status:** The final assessment indicates that all major tests, including Ramping, pulse ramping, overcurrent, and Earth ramping, were completed successfully, with each passing the set thresholds and tolerances. This consistent pass across tests suggests that the adjustments made in the configuration and tolerance levels were effective, ensuring that each component performed as expected under the conditions tested.