VOLTAGE SOURCE CONVERTER

Submitted by:
Ibrahim Okikiola Lawal

Supervise by: Prof. Marc Cheah Mañé

Department of Electrical Engineering
Universitat Politecnica de Catalunya

Contents

List of Figures

List of Tables

Chapter 1

VOLTAGE SOURCE CONVERTER MODEL (VSC)

Voltage Source Converters (VSC) are a pivotal technology in the field of power electronics, enabling the efficient conversion between alternating current (AC) and direct current (DC) in a variety of applications, particularly in high-voltage direct current (HVDC) transmission systems. Their ability to manage active and reactive power independently makes them integral to modern electric grids, enhancing stability, and facilitating the integration of renewable energy sources. VSCs are comprised of semiconductor devices, usually Insulated Gate Bipolar Transistors (IGBTs) or similar, which can be switched on and off at high frequencies to control the direction and flow of electrical power. In contrast to Line Commutated Converters (LCC), VSCs do not require a strong AC system for commutation and are capable of generating an almost perfect sinusoidal AC voltage from a DC power source.

1.1 Applications of VSC in Power Systems

VSCs are utilized in various power system applications, including but not limited to:

1. **HVDC Transmission:** For long-distance power transmission with low losses and controlled power flows.
2. **Renewable Energy Integration**: To connect renewable energy sources with variable output, such as wind or solar, to the grid with the capability to control power quality.
3. **Grid Stability and Support**: Offering services like voltage regulation, frequency control, and reactive power support to maintain grid stability.
4. **Microgrids and Remote Areas:** Enabling reliable power supply in isolated regions and microgrids where grid stability is essential.

1.2 Average Models of a Voltage source converters

Average models, often used in simulations, represent the mean behavior of a system over time, abstracting the details of switching actions in power electronic converters. For a VSC, the fast-switching actions of devices like IGBTs or MOSFETs are replaced by their average effect over one or several switching periods. This simplification is particularly useful for studying the system's dynamics over longer periods where the switching details are less relevant compared to the overall system behavior. The key advantage of using average models in simulations is the reduction in computational complexity and simulation time. This is because the model does not need to compute the state of the system at each switching event, which can occur thousands of times per second. This model does not account for any losses, although is possible to add them. The active power equilibrium is ensured , which states that the DC power and active AC power must be always equal. $PDC = PAC$

1.3 SCHEMATIC REPRESENTATION OF THE AVERAGE MODEL

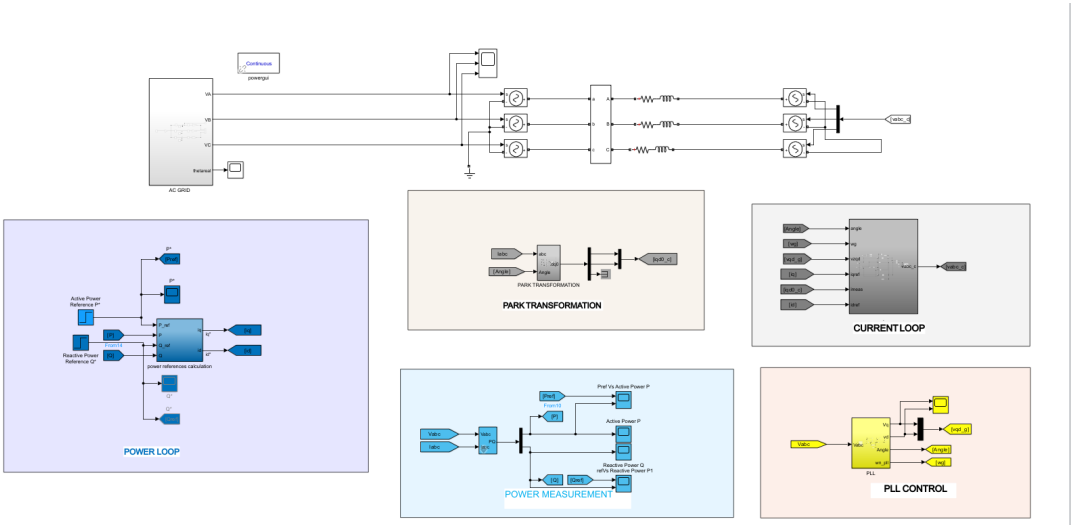

FIGURE 1.1:
MATLAB SIMULATION OF AVERAGE MODEL VSC AND CONTROL

1.4 AC Grid Block

This block serves as the AC voltage source for the converter. Within the average model, the sinusoidal AC source is typically not influenced by switching actions, and its parameters define the grid voltage level and frequency. For the VSC in question, these parameters include a nominal AC voltage (Ucn) of 690 volts and a nominal frequency (fg) of 50Hz, which are typical for many grid-connected systems. These values remain constant or follow a predetermined variation over time to simulate different grid conditions.

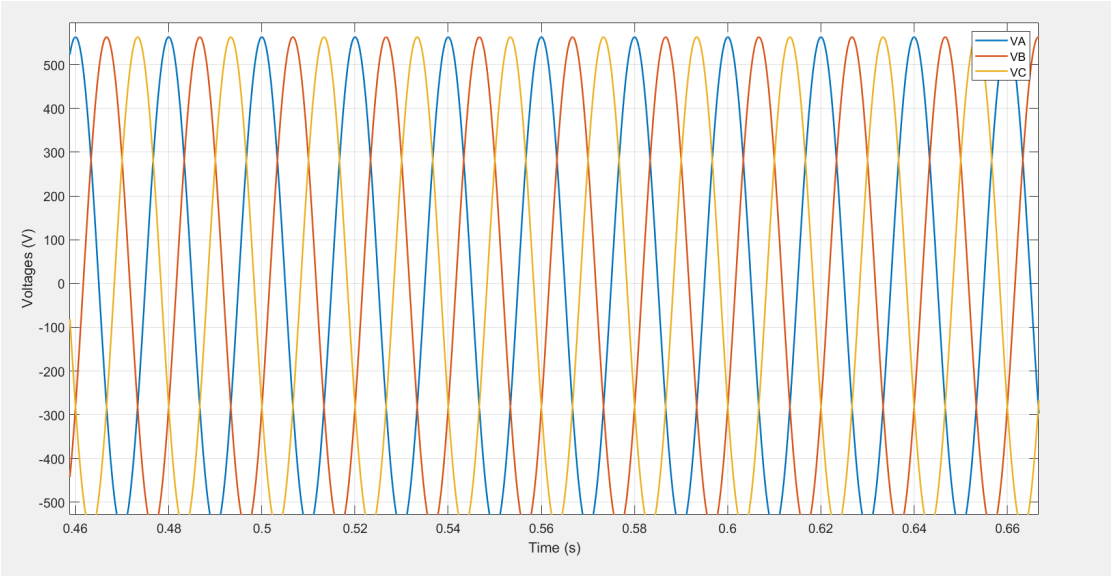

FIGURE 1.2: **Three phase voltage source**
The graph above displays the three-phase AC voltage for a VSC, with a stable grid voltage of 690V and a frequency of 50Hz, which are typical values for grid-connected systems. The sinusoidal waveforms indicate a consistent AC source, essential for the VSC's operation under various grid conditions.

1.5 VSC Block

The average model of a VSC captures the essential function of converting between AC and DC. Instead of modeling each switch, it uses a mathematical representation, like a controlled voltage or current source whose output is based on the average value expected from the real switching devices. Control inputs for this block include reference voltages or currents, which are derived from the control strategy implementing, for example, a PID controller or a more complex algorithm like Model Predictive Control.

1.6 Inductors and Filters

In a typical two-level VSC setup, inductors act like buffers that smooth out any sudden changes in the current, ensuring a steady and clean flow of electricity. They're a bit like the shock absorbers in a car, helping to provide a smooth ride by ironing out the bumps. In our model, these inductors are imagined as perfect components that perform this smoothing job without adding any complications. They have a value of 30.31 microhenries (µH), which is a measure of their ability to manage these current changes and keep the electricity flowing smoothly.

1.7 Control Systems

Control systems are the brain of the Voltage Source Converters, tasked with ensuring that the conversion from AC to DC and back again happens smoothly, matching the precise electricity shapes needed. These systems are smart, set up to quickly adapt to what's happening on the power grid at any moment. They can handle unexpected

events without interrupting power and actively manage the balance of power to keep everything running efficiently. In simulations using average models, these control systems are represented by algorithms that mimic these real-time adjustments without getting into the nitty-gritty of every single switch flip inside the converters. Controls of converters include :

1. **PLL Control**: A Phase-Locked Loop (PLL) is used to synchronize the converter with the grid voltage, It tracks the phase and frequency of the grid voltage and provides a reference angle for the Park Transformation.Proper PLL control is essential for stable operation of the converter, especially under grid disturbances.

2. **Current Loop**: The current loop works inside the power loop and is responsible for the fast control of the converter currents to the reference values calculated by the power loop. This is implemented using Park Transformation, which transforms three-phase quantities into a two-dimensional rotating reference frame (dq0), simplifying the control of three-phase systems.

3. **Power Loop**: This controls the real (P) and reactive (Q) power of the converter. It usually consists of reference settings for P and Q (Pref and Qref), which are compared with the measured P and Q values. The error is then processed through control algorithms (PI controllers are common) to adjust the converter's output to match the desired power flow.

1.8 Measurement Blocks

In the configuration of Voltage Source Converters, measurement blocks serve a dual purpose. Not only do they monitor the current flowing through each phase, indicated by the current (i) symbols, but they also keep tabs on the voltage levels. This dual-functionality is crucial for the feedback control mechanisms of the VSC. By tracking both current and voltage in real time, these blocks provide the detailed electrical information necessary for the control systems to fine-tune the converter's operations, ensuring that both voltage and current waveforms are precisely regulated for stable and efficient system performance.

Chapter 2

VOLTAGE SOURCE CONVERTER CONTROL

Voltage Source Converter (VSC) control is essential for the operation of modern electric power systems, especially those incorporating HVDC transmission and renewable energy sources. The control system in a VSC is responsible for managing the power conversion from DC to AC and vice versa, while ensuring that the conversion process is efficient, stable, and meets the quality standards of the electrical grid.

The main objectives of VSC control include:

1. **Synchronization**: VSC control ensures that the output frequency and phase match the AC grid, which is crucial for the integration of the converter with the power system.
2. **Efficiency**: Advanced control strategies optimize the switching of power electronic devices to minimize losses and improve the overall efficiency of power transmission.
3. **Grid Stability and Support:** Offering services like voltage regulation, frequency control, and reactive power support to maintain grid stability.
4. **Renewable Integration:** VSC control is integral to the integration of intermittent renewable energy sources, helping to balance supply and demand effectively.
5. **Fault Management:** Control systems can rapidly detect and respond to grid disturbances, protecting the converter and maintaining grid reliability

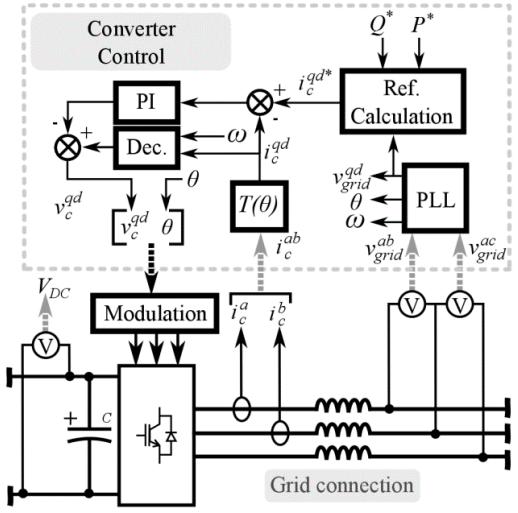

FIGURE 2.1: **Voltage Source Converter Control**

2.1 The control block diagram of a common control strategy for a Voltage Source Converter (VSC) in power systems include the following :

1. **Converter Control Block**: This is the central hub for the control system of the VSC. It interprets the reference signals for active power (P*) and reactive power (Q*) and adjusts the converter's output to match these references.

2. **Reference Calculation:** This module computes the desired current components in a synchronous reference frame (dq-frame) based on the power references. It essentially translates the power commands into current commands that the converter can follow.

3. **Decoupling** : This component accounts for the coupling between the d and q axes in the AC system due to inductance and the changing magnetic field. Decoupling ensures accurate control of the VSC.

4. **Transformation Block (T(theta))**: This block applies the Park transformation to convert the control signals between the synchronous dq-frame and the stationary abc-frame, aligning them with the grid's phases.

5. **Modulation**: The modulation block takes the voltage commands from the control system and modulates them to generate the gating signals for the power electronic switches in the converter. This typically involves pulse-width modulation (PWM) techniques.

6. **DC Voltage Source**: This represents the DC side of the VSC, providing the power to be converted. It's typically connected to an energy storage system, a DC transmission line, or a renewable energy source.

7. **Grid Connection**: This is where the VSC interfaces with the AC grid. The VSC injects or absorbs power through this connection, fulfilling its role in power conversion and grid support functions.

8. **Voltage and Current Measurement**: These measurement devices (represented by the V and I symbols) monitor the grid voltages (v_{grid}^{ac}, v_{grid}^{ab}) and currents (i_c^a, i_c^b) to provide feedback to the control system for real-time adjustments.

2.2 PHASE LOCKED LOOP

The Phase-Locked Loop (PLL) is a crucial component in the control system of a VSC. In an average model, which simplifies the power electronics by abstracting away the high-frequency switching actions, the PLL still plays a critical role in synchronizing the converter's output with the grid. The PLL works by taking the AC voltage input, often in three-phase form (Vabc), and transforming it into a two-phase orthogonal representation (dq-frame) using the Park Transformation. Once in the dq-frame, the PLL locks onto the phase of the grid voltage by adjusting its internal oscillator to match the grid's frequency and phase. The PLL's output includes the grid's angular frequency $\omega(g)$ and the angle θ. These are fed into the control system of the VSC to ensure that the power conversion aligns with the grid's voltage waveform, in terms of both frequency and phase.

In an average VSC model, the PLL allows the control system to generate the appropriate commands for the voltage source, ensuring that the VSC can properly inject or absorb power from the grid in a manner that supports the grid's stability and power quality.

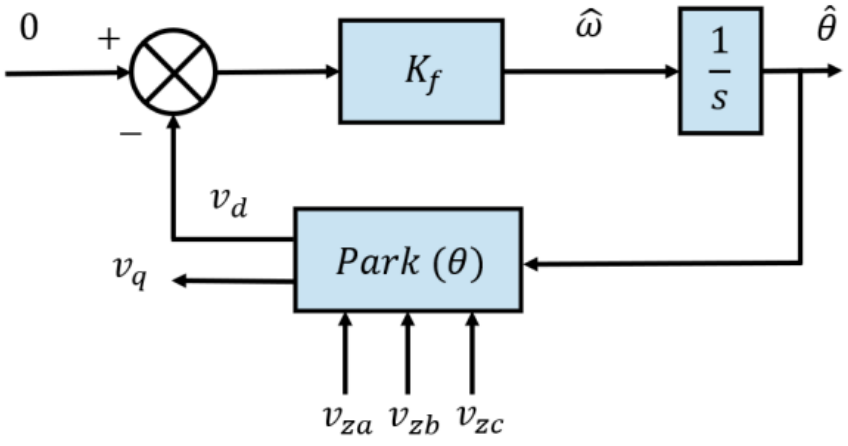

FIGURE 2.2: **PLL implementation structure**

The Phase-Locked Loop PLL takes in the grid voltages, denoted by Vzabc, and processes them to provide the grid's phase angle, θ, as its output. the PLL's role extends beyond just aligning the qd reference frame; it also guarantees that the Vd component is zero. This permits the discrete management of active power P through the iq component and

reactive power Q through the id component, thereby streamlining the overall control strategy.

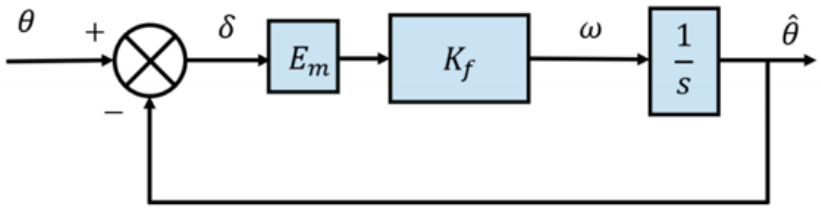

FIGURE 2.3: **PLL design structure**

$$K_f(s) = G_c(s) = \frac{K_p s + K_i}{s}$$

2.2.1 In the given parameters for a Phase-Locked Loop (PLL) used in an engineering application:

1. $xi_p ll$: represents the damping ratio, set here to $\frac{\sqrt{2}}{2}$. It's a unitless value that affects how quickly and smoothly the PLL can lock onto the grid frequency.

2. '$omega_p ll$': is the natural frequency of the PLL in radians per second, calculated here as 2π times the grid frequency (50 Hz in this case), which is standard for many power systems.

3. '$kp_p ll'$: (the proportional gain) is determined by the product of the damping ratio, twice the natural frequency, and the reciprocal of the peak AC voltage. This gain influences the responsiveness of the PLL to phase errors.

4. '$tau_p ll$': is the time constant for the PLL, computed as twice the damping ratio divided by the natural frequency. It's related to how fast the PLL responds to changes in the input signal.

5. '$ki_p ll'$: (the integral gain) is derived from the proportional gain divided by the time constant, shaping how the PLL eliminates the steady-state error over time.

2.2.2 PARK TRANSFORMATION

Park transformations play a pivotal role in the management of Voltage Source Converters (VSCs). Even though control can technically be executed in the abc or $\alpha\beta$ frames following the Clarke transformation, the qd frame is preferred for its simplicity and familiarity. The qd frame transforms the multi-dimensional system into one where only a single constant magnitude needs to be managed, facilitating the application of traditional control techniques and widely-understood control frameworks.

In the context of VSC control, three key transformations are involved:

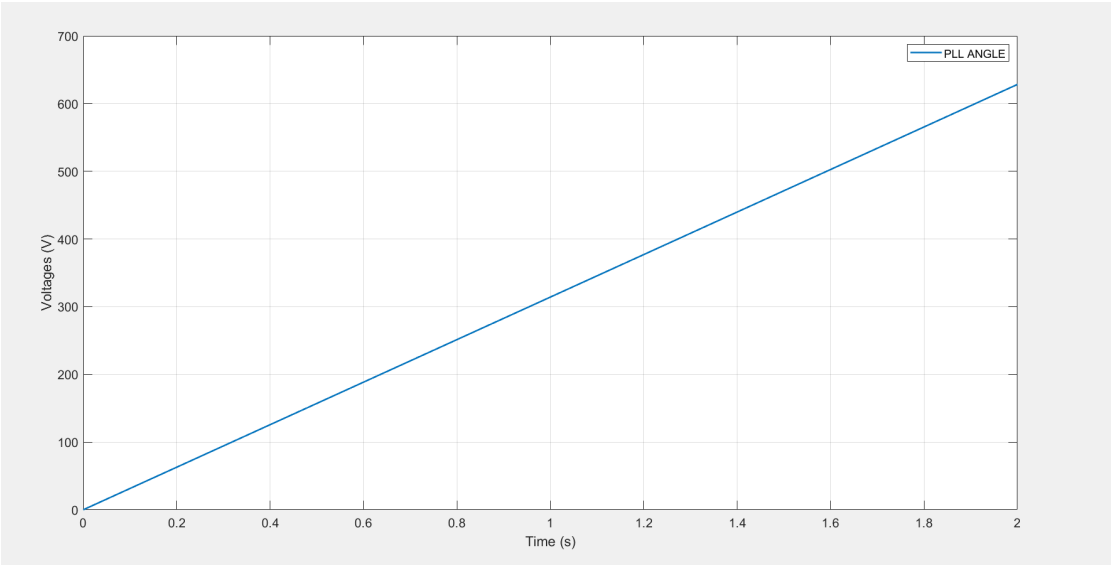

FIGURE 2.4: **PLL ANGLE**

The graph depicted that the Phase-Locked Loop (PLL) angle shows a linear increase over time, which signifies a constant angular velocity and thus stable operation of the PLL. This steady slope indicates that the PLL has locked onto the target frequency and is maintaining synchronization without any phase errors or corrections. The lack of fluctuations or transients shows that the graph captures the behavior after initial locking has occurred. Given a grid frequency of 50 Hz, the PLL's angle increases at a rate determined by the angular frequency.

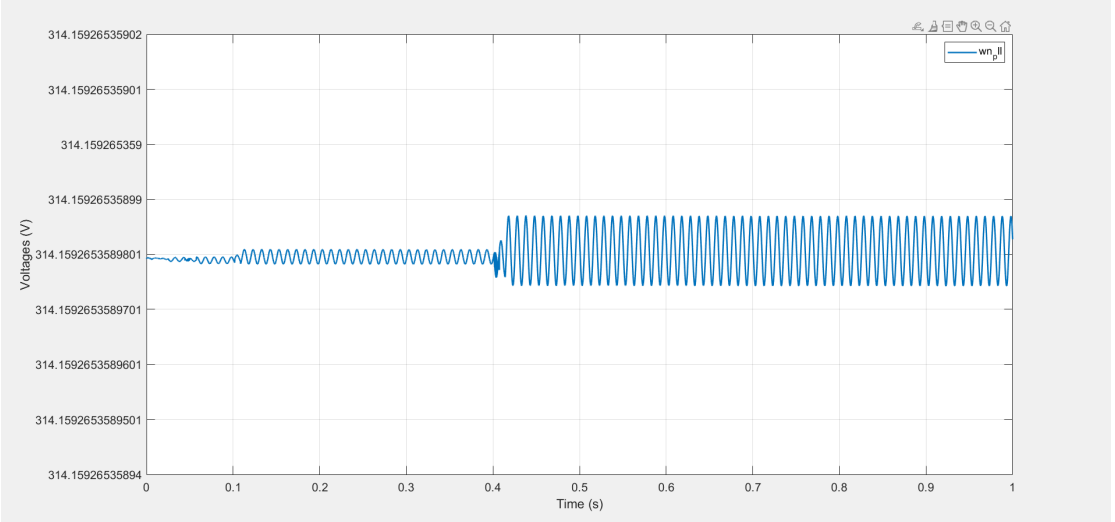

FIGURE 2.5: **Angular Velocity**

The angular velocity graph of the PLL initially shows a stable state before a transient response occurs, the PLL is trying to align with the input signal's phase and frequency. The graph then enters an oscillatory phase, with the angular velocity fluctuating as the system overshoots and undershoots while attempting to lock on to the input frequency. This behavior is likely influenced by the loop's proportional and integral gains. Eventually, the PLL appears to stabilize, indicating that it has locked onto the input signal frequency. The steady-state angular velocity reached by the PLL can be expressed as $2 * pi * fg$, where fg is the grid frequency of $50hz$. Thus, the steady-state angular velocity value that the PLL is aiming to achieve is a 314.16 rad/s.

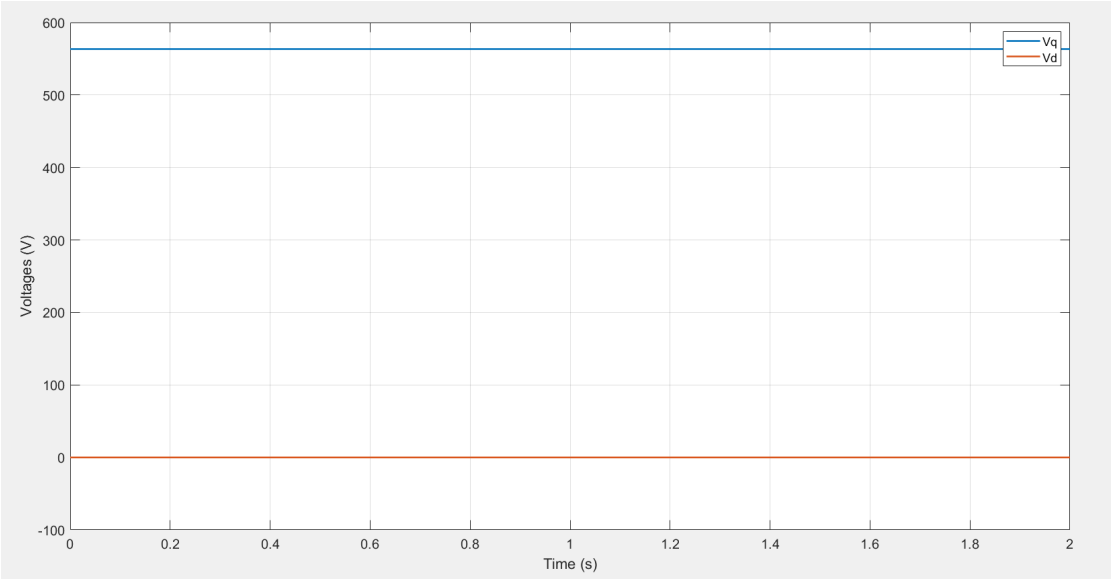

FIGURE 2.6: **Vd and Vq graph**

As shown in the graph below, In the Park transformation applied within PLL control for VSC, a zero V_D value shows that the PLL is properly synchronized with the grid, aligning the d-axis with the voltage vector perfectly. Conversely, the V_Q value, when not zero, indicates the active component of the voltage, which is pivotal for the control of power within the system. This distinction is critical for the effective operation and stability of VSCs in power applications.

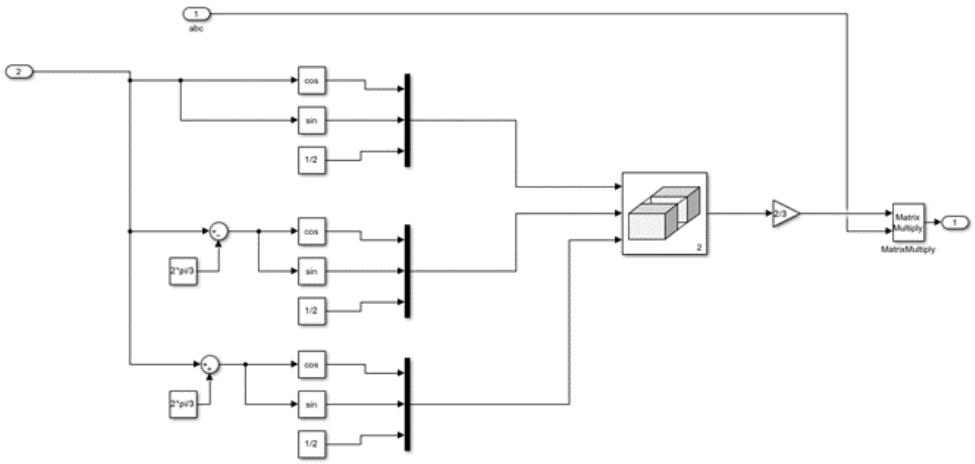

FIGURE 2.7: PARK TRANSFORMATION IN SIMULINK

1. The grid voltage is shifted from the abc frame to the qd frame, which is then utilized by the PLL to synchronize the converter's output with the grid.

2. current flowing to or from the grid is also converted from the abc to the qd frame. This transformation is essential for nearly all control elements within the VSC structure, as it allows for the streamlined control of power delivery and quality.

2.3 CURRENT LOOP CONTROL

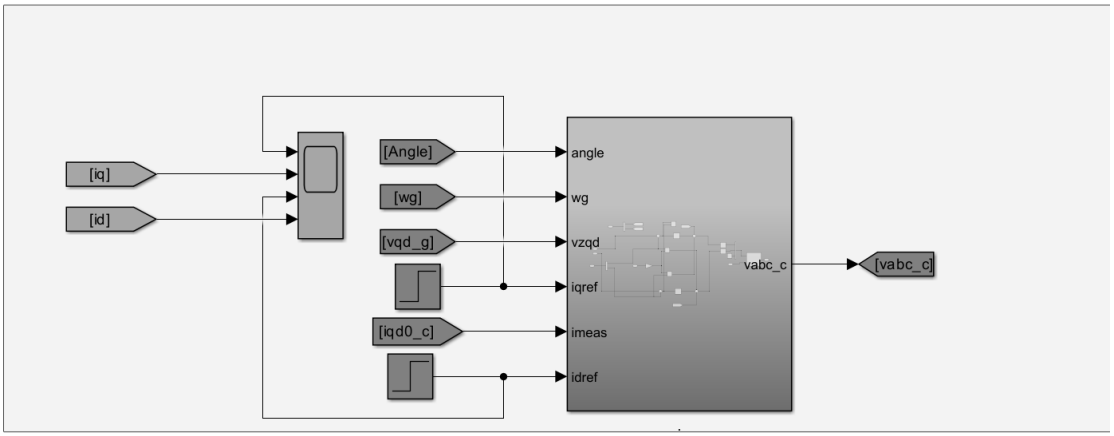

FIGURE 2.8: **CURRENT CONTROL LOOP**

The current loop is a critical component in the control of Voltage Source Converters (VSC). It's designed to manage the flow of current from the converter to the electrical grid. Among the various strategies used to control this current, the one that is most widely adopted operates on the principle of the synchronous reference frame. This method focuses on the independent regulation of q and d components of the current, which correspond to active and reactive power, respectively. A well-executed design of this control scheme can set the dynamic response rate of the control loop, ultimately influencing the converter's behaviour at fundamental levels. This helps ensure that the power delivery can be finely tuned to provide a balance between efficiency and performance.

The system equation :

$$\begin{bmatrix} v_{za} \\ v_{zb} \\ v_{zc} \end{bmatrix} - \begin{bmatrix} v_{ua} \\ v_{ub} \\ v_{uc} \end{bmatrix} - (v_{o1} - v_{o2}) \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} = \begin{bmatrix} r_i & 0 & 0 \\ 0 & r_i & 0 \\ 0 & 0 & r_i \end{bmatrix} \begin{bmatrix} \dot{i}_a \\ \dot{i}_b \\ \dot{i}_c \end{bmatrix} + \begin{bmatrix} l_i & 0 & 0 \\ 0 & l_i & 0 \\ 0 & 0 & l_i \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

In compact form (without neutral):

$$v_{abc} - v_{labc} = \begin{bmatrix} r_l & 0 & 0 \\ 0 & r_l & 0 \\ 0 & 0 & r_l \end{bmatrix} i_{abc} + \begin{bmatrix} l_l & 0 & 0 \\ 0 & l_l & 0 \\ 0 & 0 & l_l \end{bmatrix} \frac{d}{dt} i_{abc}$$

The decoupling loop can be defined by:

$$\begin{bmatrix} v_q \\ v_d \end{bmatrix} = \begin{bmatrix} -\dot{v}_q + v_{zq} - l\omega_e i_d \\ -\dot{v}_d + l\omega_e i_q \end{bmatrix}$$

Which leads to a completely decoupled system, in which it can be controlled:

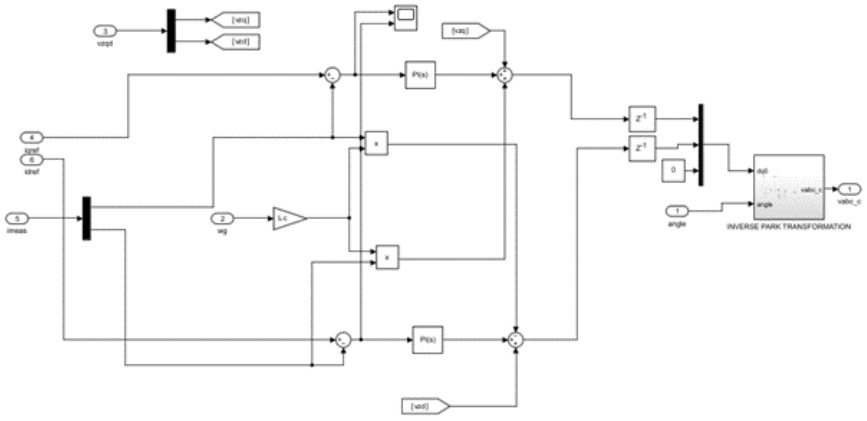

FIGURE 2.9: **INTERNAL STRUCTURE OF CURRENT LOOP CONTROL SUBSYSTEM**

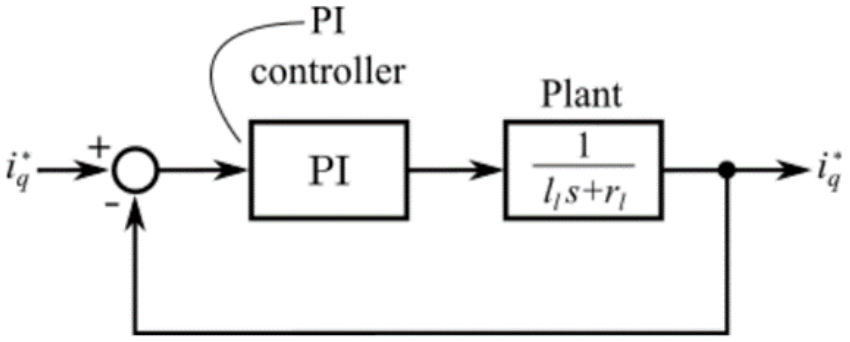

FIGURE 2.10: **CURRENT LOOP DESIGN STRUCTURE**

1. Current in the q-axis with the q-axis voltage
2. Current in the d-axis with the d-axis voltage

$$K(s) = \frac{K_p s + K_i}{s}$$

$$K_p = \frac{l}{\tau}$$

$$K_i = \frac{r_l}{\tau}$$

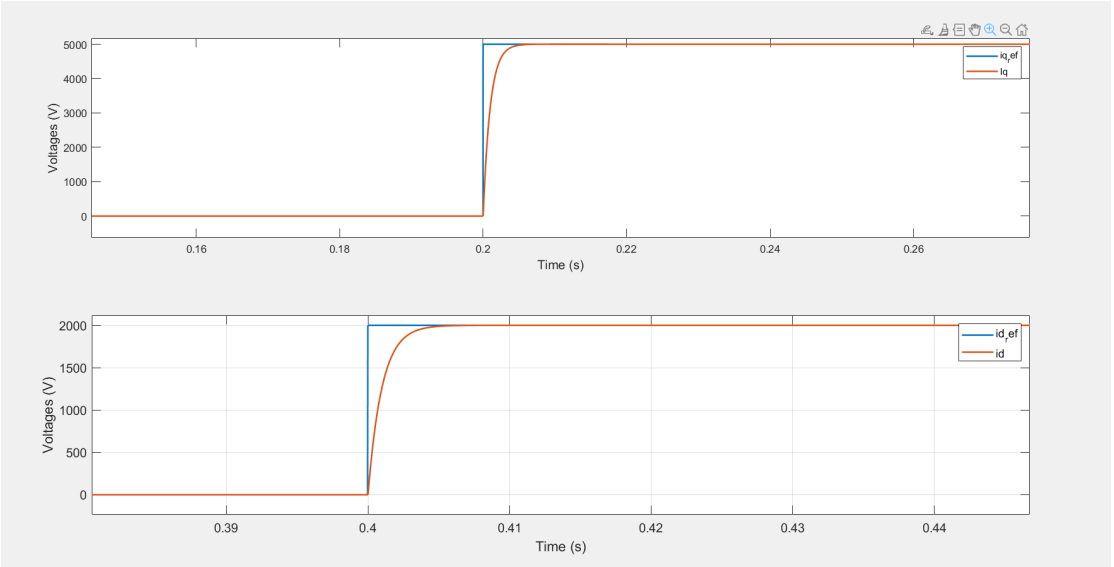

FIGURE 2.11: **Iqref, Iq, Idref,Id graph**

The graph shows the performance of a current control loop, specifically for the iq (quadrature-axis current) and id (direct-axis current) components in relation to their respective reference values, iqref and idref. In the upper plot, representing the iq and iqref, the current iq closely follows iqref, showing that the control loop is effectively managing the quadrature-axis current to align with the reference. This indicates robust control dynamics, as the actual current swiftly reaches and maintains the reference value without significant overshoot or oscillation. The lower plot shows id in relation to idref. The near-perfect overlap of the id current with its reference idref demonstrates the control system's precision in maintaining the direct-axis current at the desired level. This is indicative of a well-tuned controller that ensures the direct-axis current component remains stable and at the setpoint, which is critical for optimal performance of the system the controller is part of.

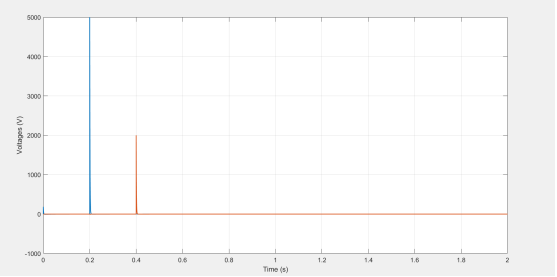

FIGURE 2.12: **Transient Response and Stabilization of Current Control Loop Before PI Controller**

2.3.1 Transient Response and Stabilization of Current Control Loop Before PI Controlle

The graph below indicates a transient error at the beginning of the simulation, which is a common occurrence when the system is responding to initial conditions or a step change in the reference signal. The swift reduction to zero signifies that the control system, specifically the PI controller that follows this measurement point, is responding appropriately to correct the error. The quick convergence to zero and the maintenance

of this value suggest the PI controller downstream is effectively bringing the system into the desired state and regulating the current as intended. This performance indicates a properly functioning current control loop, where the PI controller compensates for the initial discrepancy, resulting in a stable process control.

2.4 POWER LOOP

In the domain of Voltage Source Converters (VSC), the significance of power references, namely active (P*) and reactive (Q*) power, is paramount for the computation of reference currents on the q-axis (iq) and d-axis (id). The conversion process of these power commands into their respective current references, highlighting the role of the q-axis grid voltage(vq) in these calculations, especially under the condition where the d-axis voltage (vd) is zero.

2.4.1 Active Power and q-axis Current Reference

The equation

$$i_q^* = \frac{2}{3} \cdot \frac{P^*}{v_q}$$

serves as a foundational principle in converting the active power setpoint (P*) to the q-axis current reference (iq*), with vq denoting the q-axis component of the grid voltage. This relation underscores the transformation of active power into the q-axis current component.

2.4.2 Reactive Power and d-axis Current Reference

The conversion of reactive power (Q*) to the d-axis current reference (id) parallels that of active power to the q-axis current, but it traditionally involves the reactive power setpoint. However, the initial formulation provided

$$i_d^* = \frac{2}{3} \cdot \frac{Q^*}{v_q}$$

, appears misaligned with standard practices in VSC control. The direct correlation between reactive power and current in the d-q frame suggests a more nuanced approach to deriving id from Q*, particularly under specific operational conditions such as vd =0.

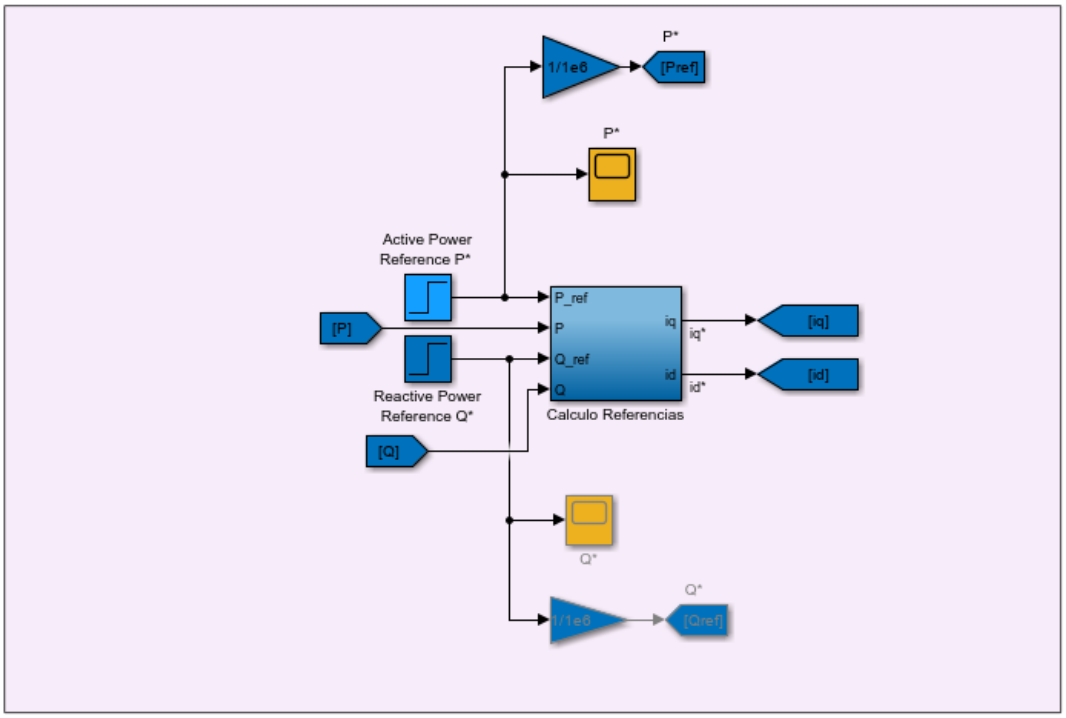

FIGURE 2.13: **Power Control Loop**

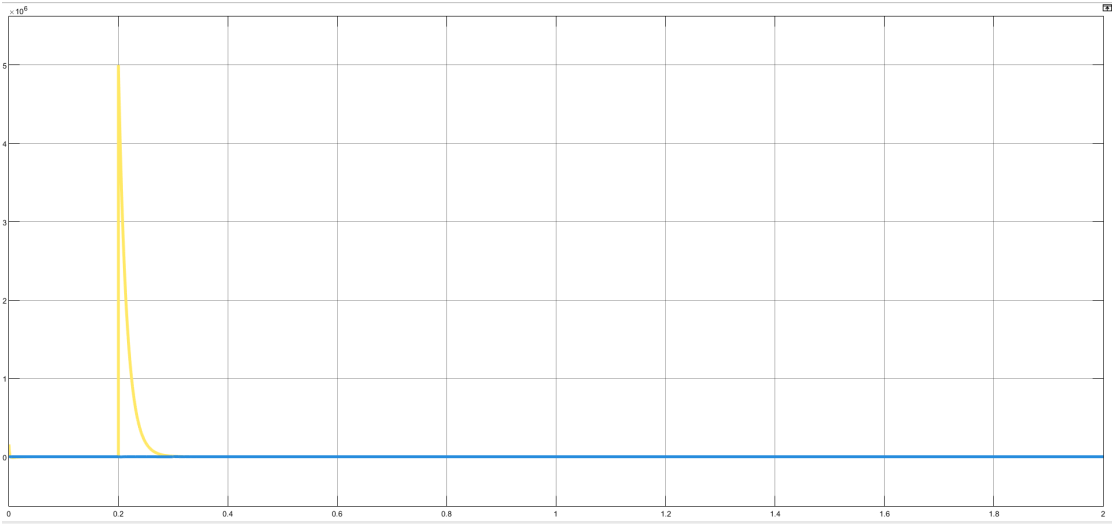

FIGURE 2.14: **Transient Response and Stabilization of Current Control Loop Before PI Controller**

The graph below shows an initial transient error in the power control loop, quickly corrected by the PI controller. This rapid convergence to zero error demonstrates effective current regulation and a stable control system.

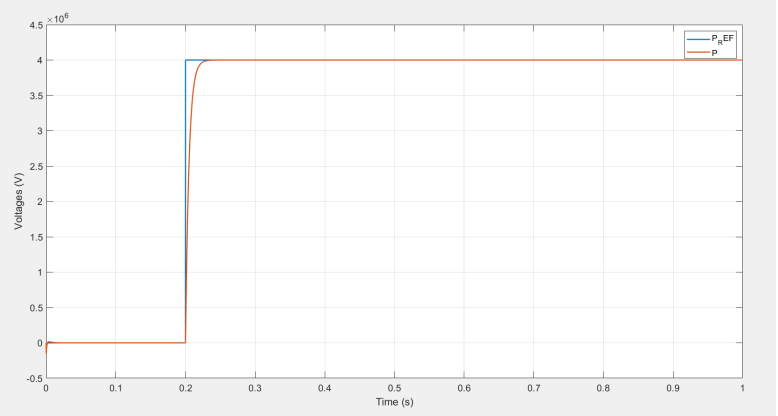

FIGURE 2.15: **Pref and activepower of the power control when time response is 5ms**

CASE 1: Time Response of 5ms

In the first case with a 5 ms time response, the actual power swiftly escalates to meet the power reference, illustrating the control system's quick responsiveness. The speed at which the actual power reaches and holds steady at the power reference level showcases a system that's efficiently tuned for fast action. The steady state is achieved almost instantly without any overshoot or oscillation, which is indicative of a stable system. While this mirrors the stability one would expect from a first-order system, the rate at which it stabilizes is notably quicker than the gradual, exponential rise typically seen in a first-order response.

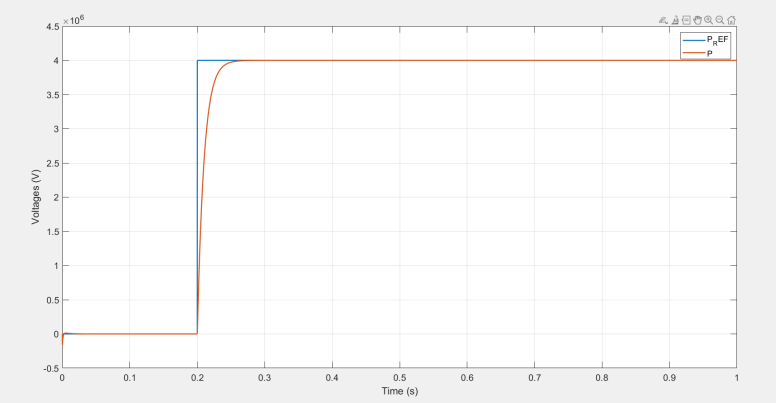

FIGURE 2.16: **Pref and activepower of the power control when time response is 10ms**

CASE 2: Time Response of 10ms

For the second case, with a 10 ms time response, the actual power responds to the input fastly, although not as fast as in the 5 ms scenario. It ascends more gradually to the power reference and maintains a stable output thereafter. This performance is consistent with the stability traits of a first-order system which is characterized by no overshoot . However, similar to the first case, the response is more immediate than the conventional first-order response, which suggests a faster-acting control system than the classical first-order model would predict.

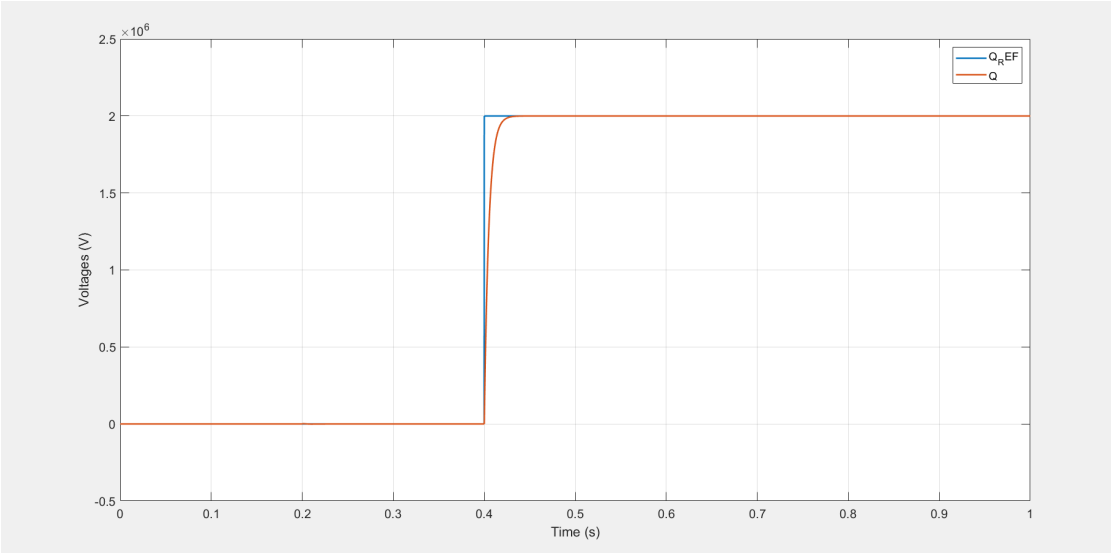

FIGURE 2.17: **Qref and REACTIVEpower of the power control when time response is 5e-3**

CASE1:5 ms Time Response

For the 5 ms response, the graph shows the reactive power (Q) quickly jumping to meet the set reference (Qref). This quick response means the system is tuned to react without delay. Once it reaches the reference level, it stays there, showing a stable and controlled reaction. While this fast stabilization is something one will see in a first-order system, the system here gets to the settled state quicker than the usual first-order response, which generally rises more slowly.

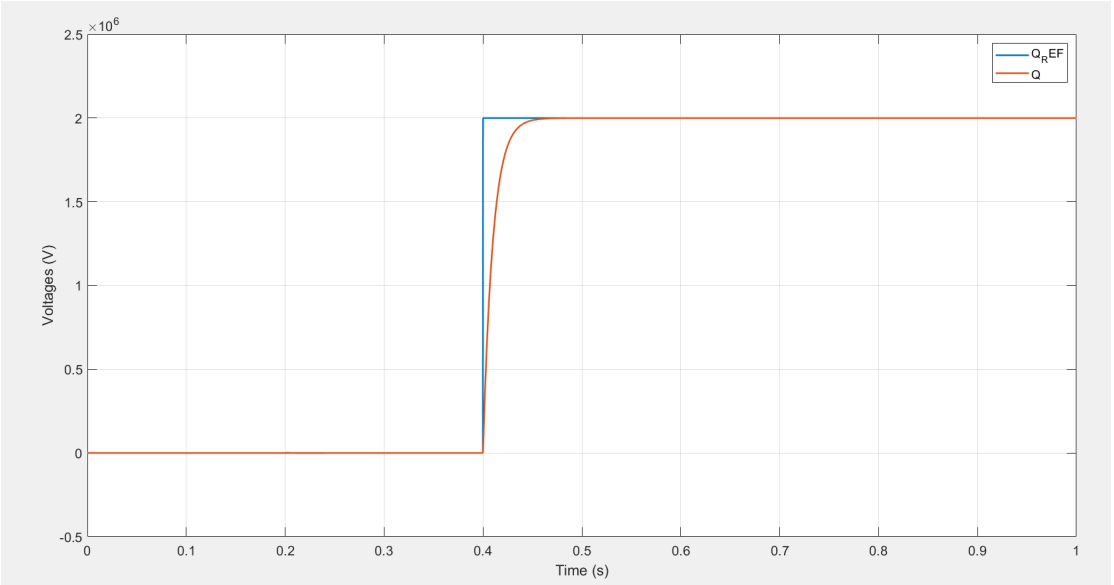

FIGURE 2.18: **Qref and REACTIVEpower of the power control when time response is 10e-3**

CASE2:10 ms Time Response:

With a 10 ms time response, the reactive power (Q) still moves to the reference (Qref) quite fast, but not as sharply as in the 5 ms case. The rise is smooth and hits the reference level without overshooting. The system shows a steady and predictable reaction, again reminiscent of a first-order system, but reaching the steady state faster than a typical first-order system would.

Chapter 3

GRID IMPENDANCE

Grid impedance is added to the average model of a Voltage Source Converter **(VSC)**,it plays a crucial role in defining the interaction between the converter and the AC grid. It essentially comprises two components: resistance **Rg** and inductance **Lg**, which together make up the Thevenin equivalent impedance as seen from the **VSC** side.

The resistance component **Rg** represents the energy losses as the current flows through the grid. These losses typically manifest as heat . The inductance component **Lg**, on the other hand, represents the grid's opposition to changes in the current flow. This inductive reactance impacts the phase angle between the voltage and current, a critical aspect when considering the power factor and the efficient operation of the grid.

Grid impedance is not only a parameter for consideration during steady-state operation but also a critical factor during transients, such as faults or switching operations, where the impedance determines how these events propagate through the system. Modeling the grid impedance accurately is thus vital for the analysis, design, and control of VSCs in power systems.

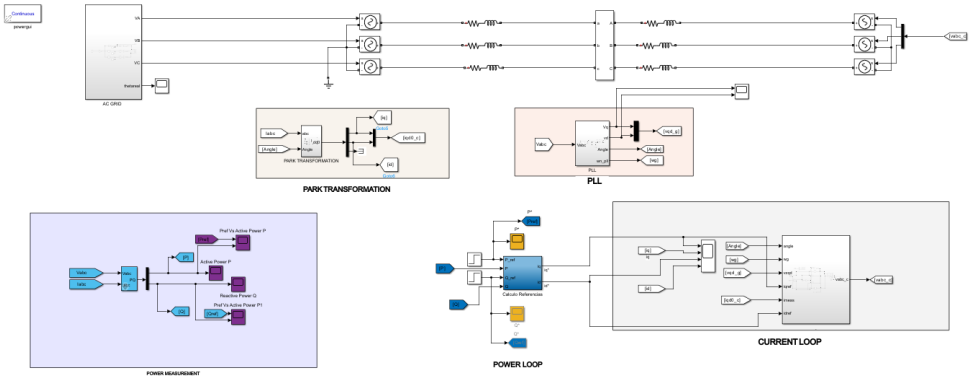

FIGURE 3.1: **MATLAB SIMULATION OF AVERAGE MODEL with GRID IMPENDANCE**

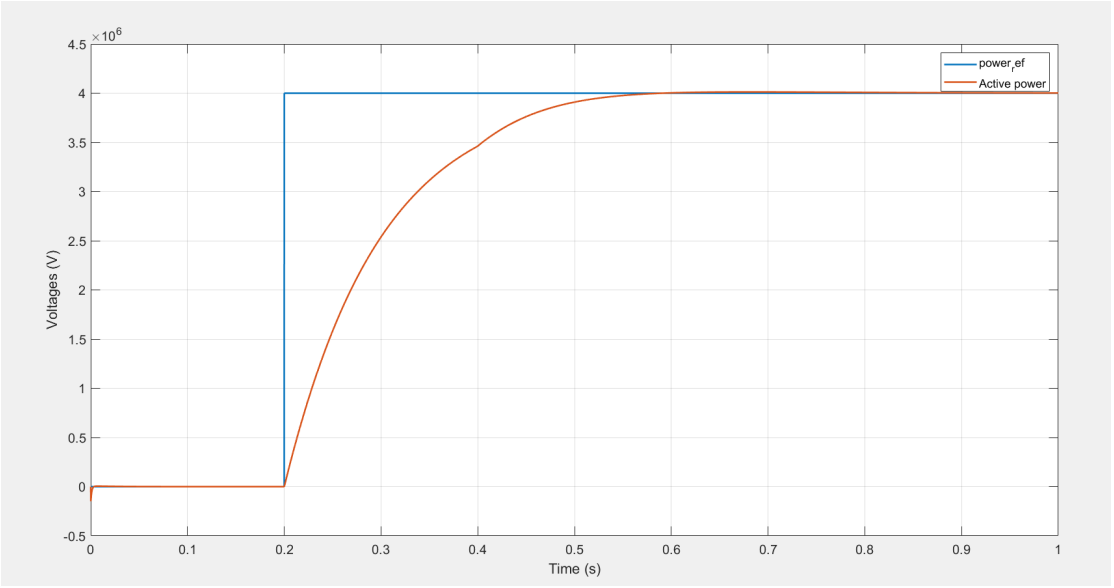

FIGURE 3.2: **GRAPH OF PREF AND P WHEN SRC IS 5 AND Taup is 100ms**

Grid impendance effect when taup=100ms and SRC=5

The graph reflects the active power response of a system with a grid impedance, considering a Short-Circuit Ratio (**SCR**) of 5. The steep rise in active power without overshooting suggests an effective control system, optimized to handle grid impedance effects. The high **SCR** value indicates a strong grid that can handle five times the system's nominal current, providing a stable backdrop for the **VSC** to quickly match its power output to the reference value. Grid impedance acts as a filter for the power fluctuations, and the **SCR** indicates the grid's capacity to sustain short-circuits, directly influencing the VSC's ability to rapidly and stably respond to changes in power demand.

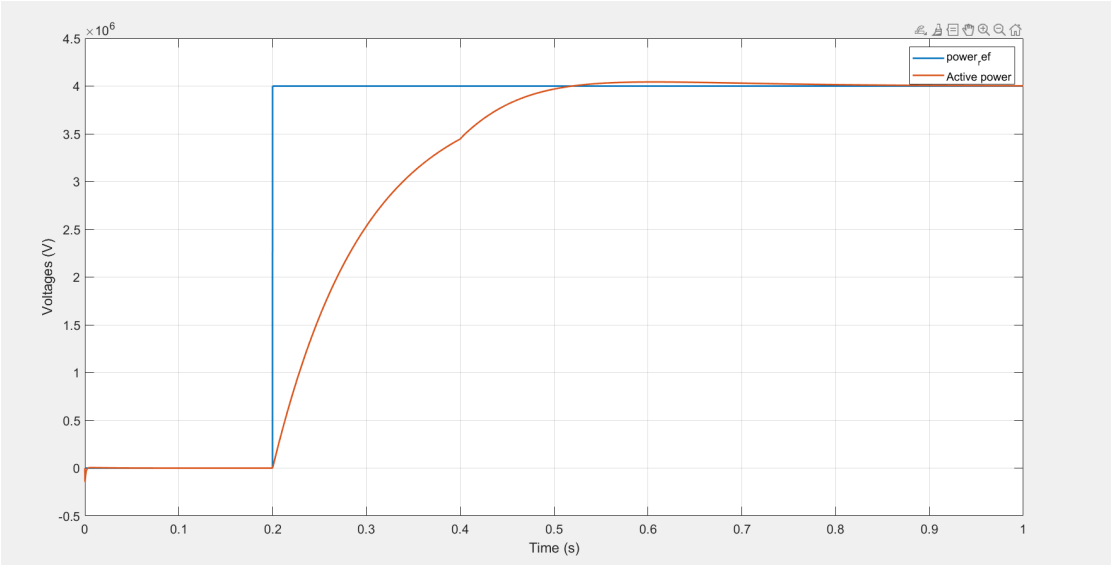

FIGURE 3.3: **GRAPH OF PREF AND P WHEN SRC IS 3 AND Taup is 100ms**

Grid impendance effect when taup=100ms and SRC=3

The graph shows a system's active power response with an **SCR** of 3, leading to a slower rise to the power reference, indicative of a less robust grid. The system demonstrates a conservative response, smoothly tracking the reference due to a lower **SCR** which requires more reliance on internal control for stability amid less grid support and greater impact from grid impedance.

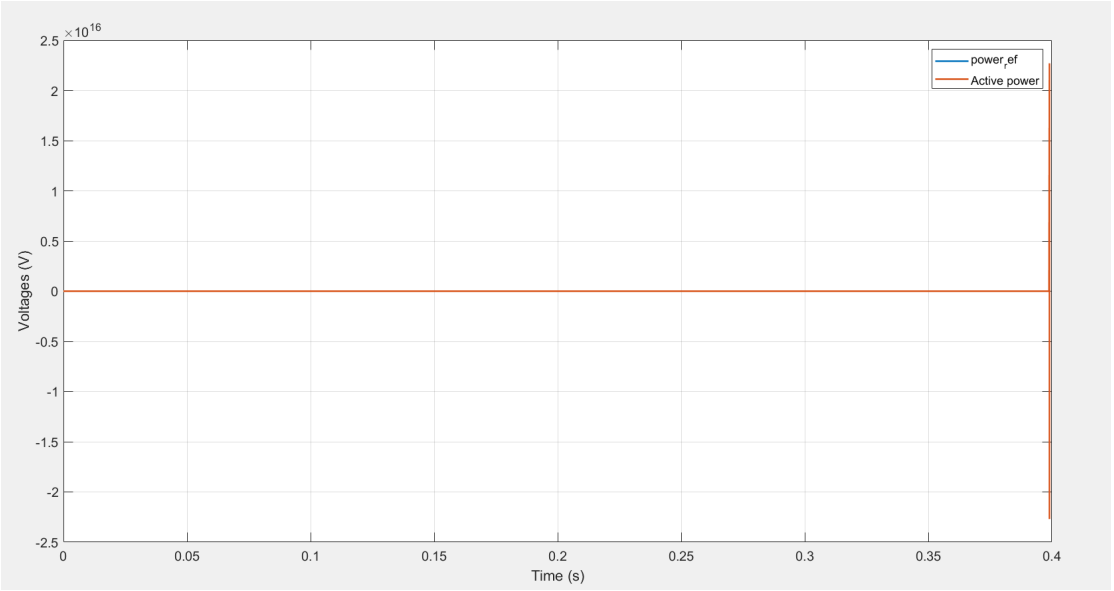

FIGURE 3.4: **Grid impendance effect when taup=100ms and SRC=3**

Grid impendance effect when taup=100ms and SRC=1

In this graph, with an **SCR** of 1, the active power remains constant and does not follow the power reference, which sharply increases. An **SCR** of 1 shows a grid with very limited capacity, equal to the system's nominal current. This limitation could will prevent the active power from responding to the reference, indicative of a grid that cannot support additional load demands or sudden changes in power. It's a situation often associated with a high risk of instability and voltage collapse in the grid.

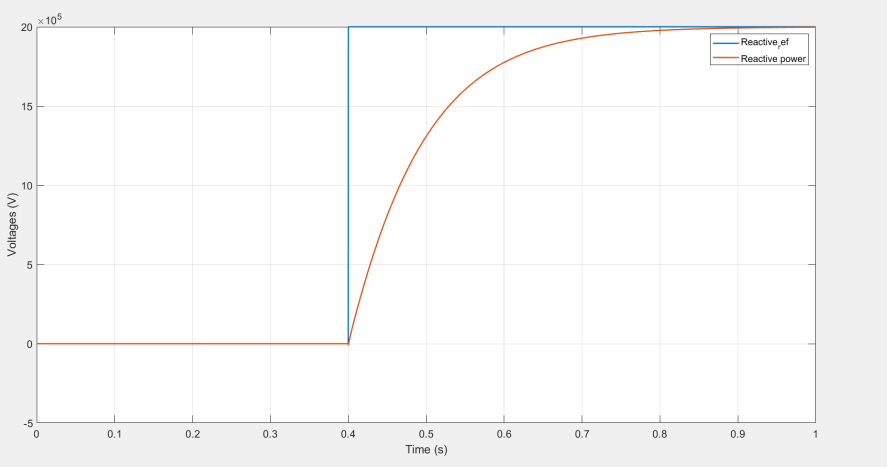

FIGURE 3.5: **Grid impendance effect when taup=100ms and SRC=5**

Grid impendance effect when taup=100ms and SRC=5 on the reactive reference and reactive power

In this graph with an SCR of 5, the reactive power closely follows the reactive power reference after an initial sharp rise, indicating a strong grid capacity. The VSC adjusts reactive power effectively, showing good control system performance and grid support that can handle rapid changes in reactive power demands. The alignment between the actual and reference reactive power demonstrates the system's ability to maintain voltage stability and power quality, which is essential in scenarios involving reactive power control, such as power factor correction or voltage regulation.

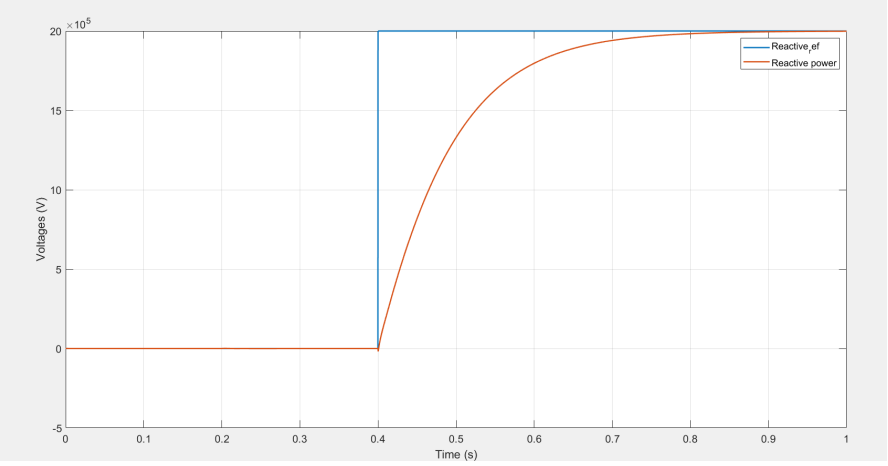

FIGURE 3.6: **Grid impendance effect when taup=100ms and SRC=3**

Grid impendance effect when taup=100ms and SRC=3 on the reactive reference and reactive power

In the graph where the SCR is 3, the reactive power still successfully tracks the reference, but the curve suggests a slightly delayed response compared to an SCR of 5. This indicates a weaker grid that is less capable of handling the reactive power changes, yet still manages to provide sufficient support for the VSC to adjust its output to the new conditions. The overall system stability seems maintained, with the reactive power reaching the reference value without overshoot, highlighting an effective control despite a less robust grid environment.

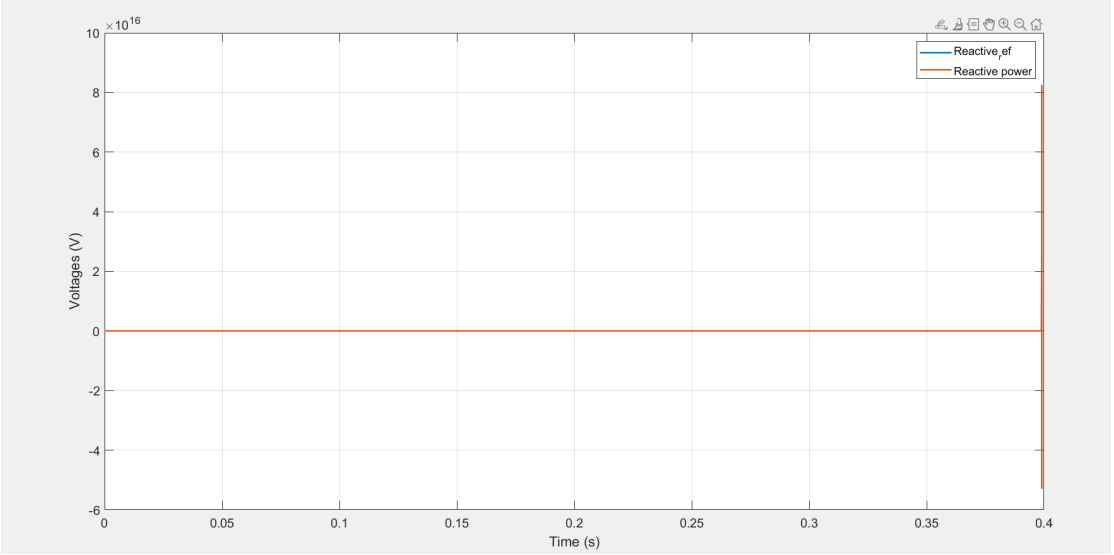

FIGURE 3.7: **Grid impendance effect when taup=100ms and SRC=1**
With an SCR of 1, the reactive power is flat and unresponsive to the reference, which signifies a grid that's at its capacity, providing only as much current as the system's nominal level. This can lead to an inability to handle reactive power changes, risking voltage stability and potentially leading to grid failure during higher demand or disturbances.