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Design of Digital 100-Base-TX Ethernet Receiver System

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***Abstract*—The objective of this project is to design the Digital 100-Base TX Ethernet Receiver System. A binary sequence as input signal is generated from the source. Through sampler, filter, equalizer and decision device, the output signal is distributed on three levels by three symbols. Additional methods are outlined that slicer reduces the impact of error propagation and alleviates intersymbol interferences (ISI), and time recovery adjusts sampling phase to achieve symbol synchronization.**

***Key Words*—Digital communications, ethernet receiver, sampler, filter, blind equalizer, time recovery, intersymbol interferences (ISI), slicer (decision device), feedforward equalizer (FFE), feedback equalizer (FBE) and decision feedback equalizer (DFE) slicer.**

I. INTRODUCTION

Ethernet system is a computer networking technology that commonly used in local area networks (LAN), metropolitan area networks (MAN) and wide area networks (WAN) to support higher bit rates and longer link distances.

In this work, an applied Digital 100-Base TX Ethernet Receiver System is introduced to conduct signal and separate them close to three symbols -1, 0, and 1 respectively, as shown in Fig 1.

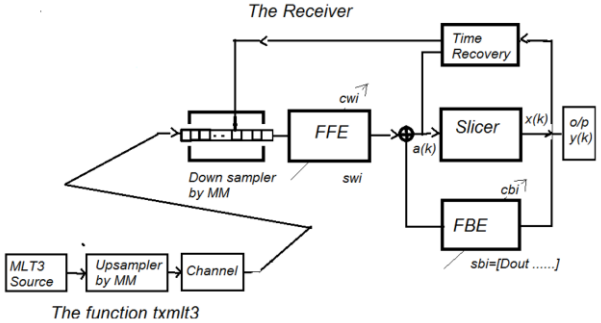


Fig. 1

Specifically, MLT3 Source creates the NRZ sequence beginning with the idle sequence and scrambled NRZ data and encodes the scrambled NRZ data to generate a binary sequence. The binary sequence is sampled through upsampler to MM (MM=16) samples per symbol. Convolve with a rectangular filter to approximate the DAC output. Then the waveform is transmitted through the channel and downsampler by MM (MM=16) times. Feedforward equalizer (FFE) acts as an FIR filter and pre-distorts transmitted pulse in order to invert channel distortion. It corrects the received waveform with information about the waveform itself and not information about the logical decisions made on the waveform. FFE is only concerned with correcting voltage levels in the waveform. Feedback equalizer (FBE) makes logical decisions (whether a bit is 0 or 1) and then feeds that information back to help determine whether the current bit is 1 or 0.

In this system, the design part are slicer function and time recovery. A simple modification of the decision feedback equalizer (DFE) slicer is proposed to reduce the effect of error propagation. An example is the transmission of high data rates over a linear channel causing intersymbol interferences (ISI) which can be compensated on the receiver side by a DFE. One of the major disadvantages of DFE is the effect of error propagation. In the present letter, a simple modification of the decision device is proposed to achieve better system performance [1]. Regarding time recovery, it is the process of extracting timing information from a serial data stream to allow the receiving circuit to decode the transmitted symbols in serial communication of digital data. Time recovery from the data stream is expedited by modifying the transmitted data. Wherever a serial communication channel does not

transmit the clock signal along with the data stream, the clock must be regenerated at the receiver, using the timing information from the data stream. Some digital data streams, especially high-speed serial data streams (Ethernet) are sent without an accompanying clock signal. The receiver generates a clock from an approximate frequency reference, and then phase-aligns the clock to the transitions in the data stream with a phase-locked loop (PLL) [2]. In general, time recovery aims to obtain symbol synchronization. The receiver clock must be continuously adjusted in its frequency and phase to optimize the sampling instants of the received data signal and to compensate for frequency drifts between the oscillators used in the transmitter and receiver clock circuits [3].

II. PROBLEM FORMULATION

1. *Slicer Function*

The slicer plays a role as decision device which distribute information to three distinct symbols (-1, 0, and 1). A symbol is defined if the value of the corresponding sample is in specific zone under the threshold. After defining the slicer function and array of all ones of output, execute statements if conditions expression is used as follows:

$$\begin{cases} x < -0.5, \ y = -1 \times y, \ symbol\ "-1" \\ -0.5 \le x < 0.5, \ y = 0 \times y, \ symbol\ "0" \\ x \ge 0.5, \ y = 1 \times y, \ symbol\ "1" \end{cases}$$

The Fig 2. and Fig 3. indicate the output separation to three symbols. If output is larger than or equal to 0.5, the output multiplies by one. Else if output is less than -0.5, the output multiplies by negative one. Else the output is zero.

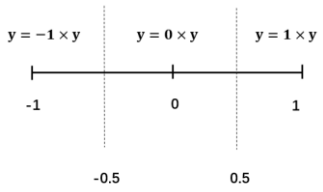


Fig 2.

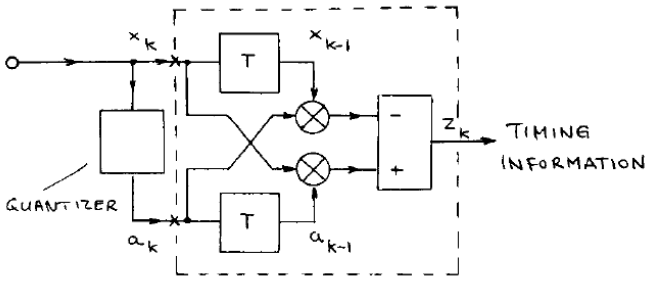
```
function y=slicmlt3(x);
    y=ones(1,length(x));
    if x>=0.5
        y=1*y;
    elseif x<-0.5
        y=-1*y;
    else
        y=0*y;
    end
```
Fig 3.

2. *Time Recovery*

For time recovery, sampling frequency and sampling phase must be determined by the receiver to achieve symbol synchronization. Sampling frequency requires estimating the symbol period (samples can be taken at correct rate), quantity should be known. Sampling phase determines the correct time within a symbol period to take a sample, sampling the symbol at the center of the symbol period (peak) results in the best signal-to-noise-ratio (SNR) and will ideally eliminate intersymbol interference [4]. The sample time is recorded by applying the algorithm of time recovery as follows:

$$\theta_{k+1} = \theta_n + \tau[a(k)x(k-1) - a(k-1)x(k)]$$

Where θ_{k+1} is new phase, θ_n is previous phase, and τ is coefficient usually around 0.1-0.5. This algorithm is based on Fig 4. block diagram about time recovery implementation of type A system [3].




```
%in the following you can perform your Time Recovery when k>=2
  if k>=2;
      sample_time= phase+0.1*((a(k)*x(k-1))-(a(k-1)*x(k)));
      phase=round(sample_time);
  end
```
Fig. 4

III. RESULTS

The simulations evaluate the output in terms of slicer organization and time recovery performance. From observing Fig. 5 below, the system output y(k) is clearly distributed on three symbol levels after a duration of time.

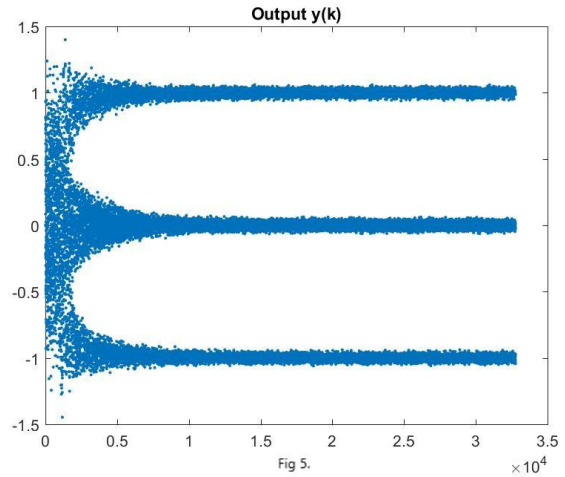


Fig 5.

As shown in Fig. 6, four kinds of coefficient are analyzed to test the performance of time recovery through around 2,000 samples. The larger coefficient τ, the less dispersion of sample times around phase

(-7) are generated. As matter of fact, more sample times are synchronized in terms of time recovery.

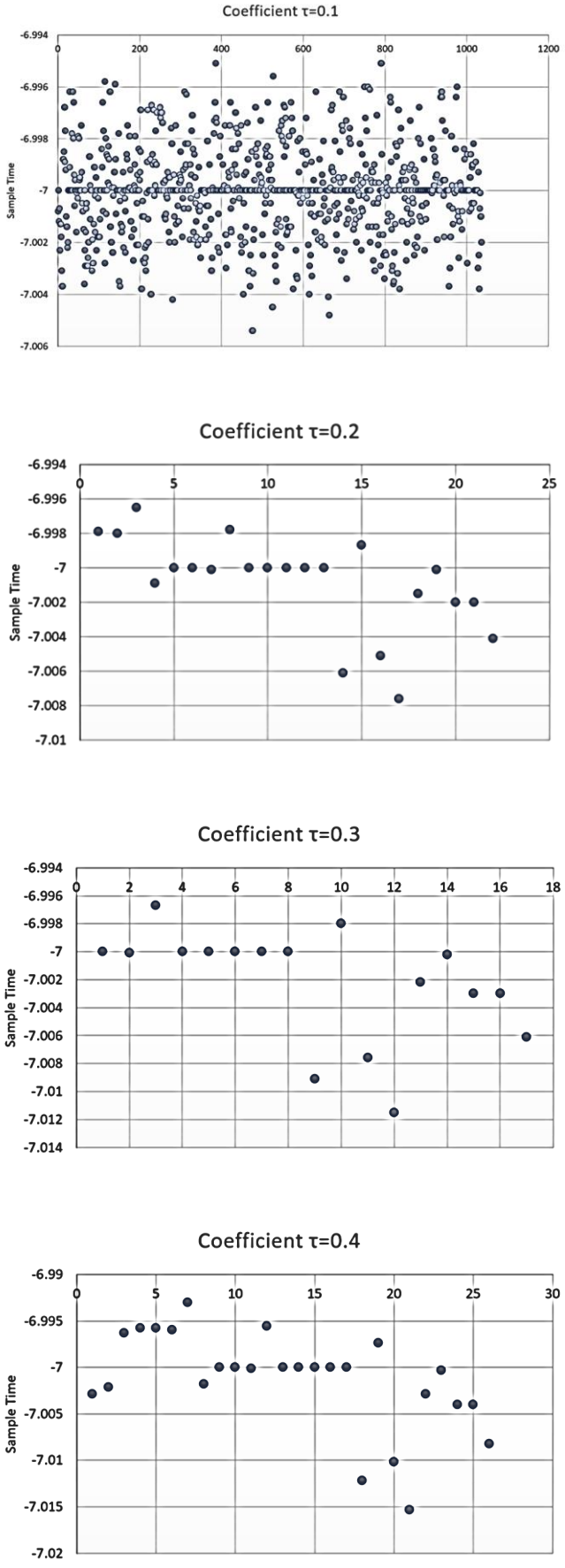


Fig. 6

IV. CONCLUSION

In the Digital 100-Base TX Ethernet Receiver System, the slicer function and time recovery are critical parts to reduce the effect of error propagation, alleviate intersymbol interferences (ISI), and optimize symbol synchronization. The simulations and results indicate the output distribution and symbol synchronization status, resulting in an improvement in performance during the data transmission.

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