Ibrahin Burk Tarribulu 21827852 Level of Parallelism Example Architecture Class 01-Single processor. (MIPS) Instruction level parallelism Single Instruction Single Data GPU (VMIPS) Onta level parallelism Single Instruction Multiple Data Multicore processors. (Pertium) Multiple Instanction Multiple Outa Thread level parallelism Q2- a) $speedup = \frac{1}{(1-0.6)+(\frac{0.6}{6})} = \frac{1}{0.55} = 1.81$ b) speedup = $2 = \frac{1}{0.5} = \frac{1}{(1-0.6)+(\frac{0.6}{x})}$ We need 6 processors. x = 6 a) CL BCS Address Data Address BCS Cache hit. Oate Write to cache. 0×20 0 M 0x20 14 Invalidate others. 5 3 DXID Core I writes the value 14 to the altress 0x20. CL BCS Adress Data 6) Private cache not hit, BCS Allress CL Data 0 I 0x20 1 5 0x10 Fetch from shared menery. M 0x 20 14 Oxlo 3 Core O reads from Headdress 0x10. c) CL BCS Address Data Cache hit but invalidated. CL BCS Address Onta 0.20 14 Fetch from others via BUS. 0 14 0×20 1 0x10 3 0×10 3 Core O reads from the address 0x20. d) CL BCS Address Ciche hit. CL BCS Address Data Write to cache. 0 x 20 14 0 x 20 Invalidate others. 0×10 6 0x10 Core O writes the value 6 to address 0x10. Cache hit e) CL BCS Adress Duta CL BCS Aldress Outa Write to cache 5 5 0x20 0,20 14 0 14 In validate others. M 0x10 12 OXIO Core 0 writes the value 12 to the address 0x10. f) CL/BCS Address Oata CL BCS Address On to Cache hit. 14 5 0,20 5 0×20 Read from cache. 0 14 M 0x10 12 0×10 Core 1 reads from the address 0x20.

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A[o] = - B[o]; for (i=0; i=99; i=i+1) { B[i+1] = 2* c[i]; A[i+1] = - B[i+1]; B[100] = 2*C[99];