

BBM233 Logic Design Lab

Fall 2019

Guide to Verilog Lab Experiments - Getting Started With Verilog Projects

November 25, 2019

Installing Xilinx Vivado Design Suite on Windows

To install Vivado Design Suite WebPACK edition download **Vivado Unified Installer** from the Xilinx's website: <https://www.xilinx.com/support/download.html>.

You will need to create a Xilinx account. You can use your school e-mail address.

Vivado Design Suite - HLx Editions - 2019.2

Important Information

Vivado Design Suite 2019.2 is now available.


- Introducing UVM 1.2 support in Vivado Simulator(XSIM)
- Improved layer visibility in IP Integrator
- Physical Optimization and other QoR improvement features
- 10% reduction in design compilation runtime
- New high bandwidth ICAP IP for enhancing Dynamic Function eXchange

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.


Please see [Installer Information](#) for details.

Note: Download verification is only supported with Google Chrome and Microsoft Internet Explorer web browsers.


Download Includes	Vivado Design Suite HLx Editions (All Editions)
Last Updated	Nov 12, 2019
Answers	2019.x - Vivado Known Issues
Documentation	Release Notes OS Support Update What's New in Vivado
Support Forums	Installation and Licensing

 **Xilinx Unified Installer 2019.2: Windows Self Extracting Web Installer (EXE - 65.5 MB)**

MD5 SUM Value : 9ad7d499f520f6a762f52bd273f4cc7a

 **Xilinx Unified Installer 2019.2: Linux Self Extracting Web Installer (BIN - 115.4 MB)**


MD5 SUM Value : b8d415a14a84241bdbae1f6a8a6e9a11

Download Verification 


Digests

Signature

Public Key

 **Vivado HLx 2019.2: All OS installer Single-File Download (TAR/GZIP - 26.55 GB)**

MD5 SUM Value : e2b2762964ef5f014591b13d77d823ab

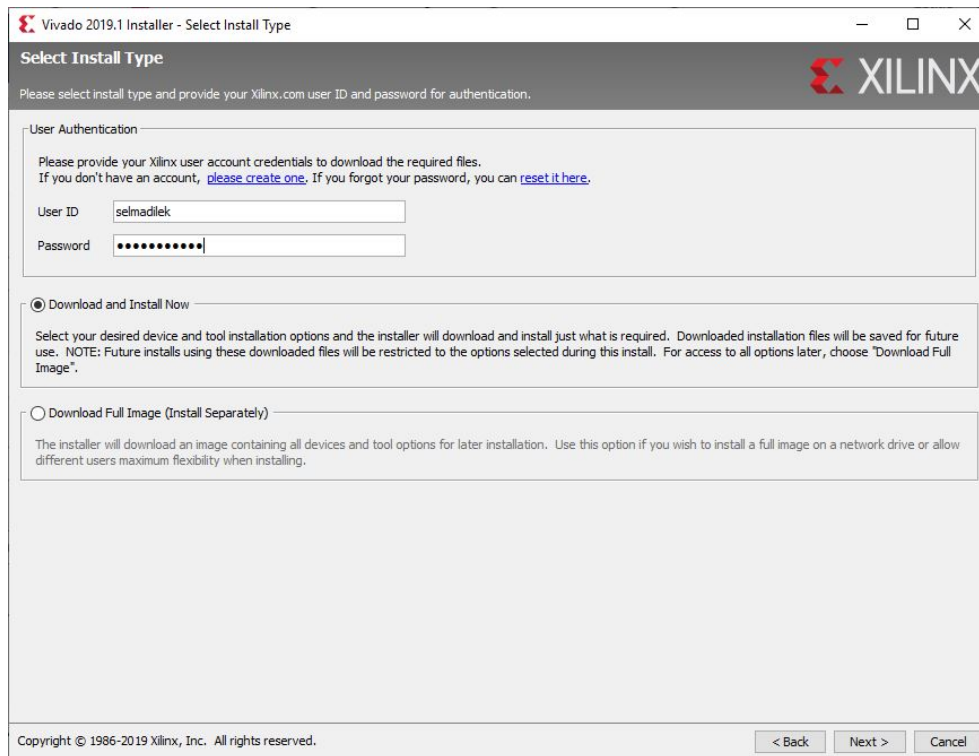
Download Verification 

Digests

Signature

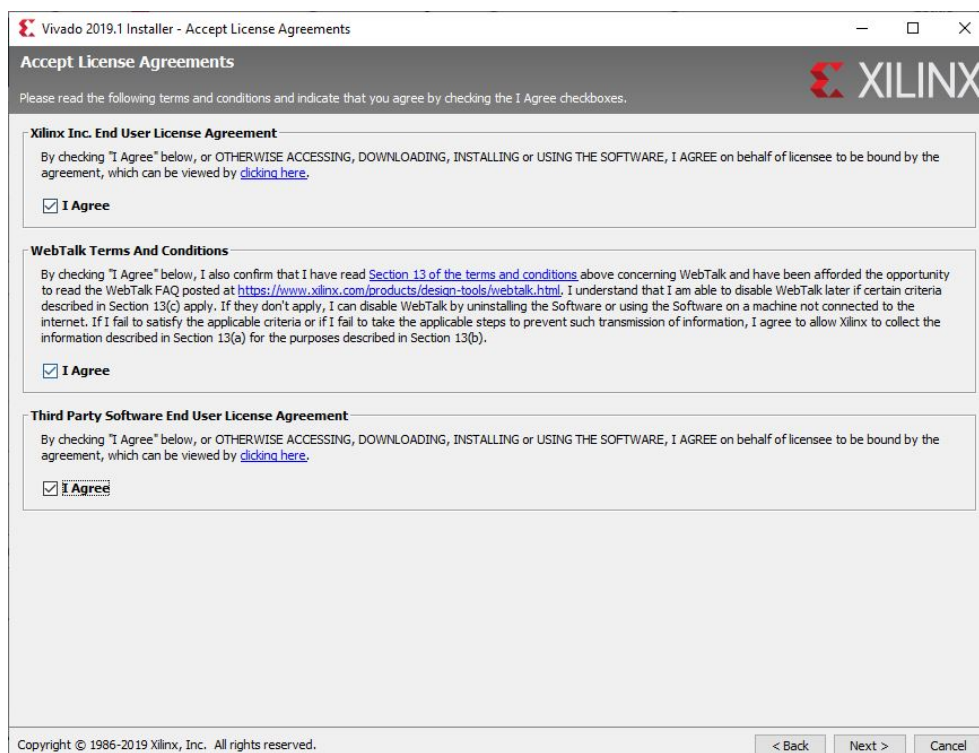
Public Key

After clicking the first Next button, you will be prompted to enter your Xilinx account user ID and Password.



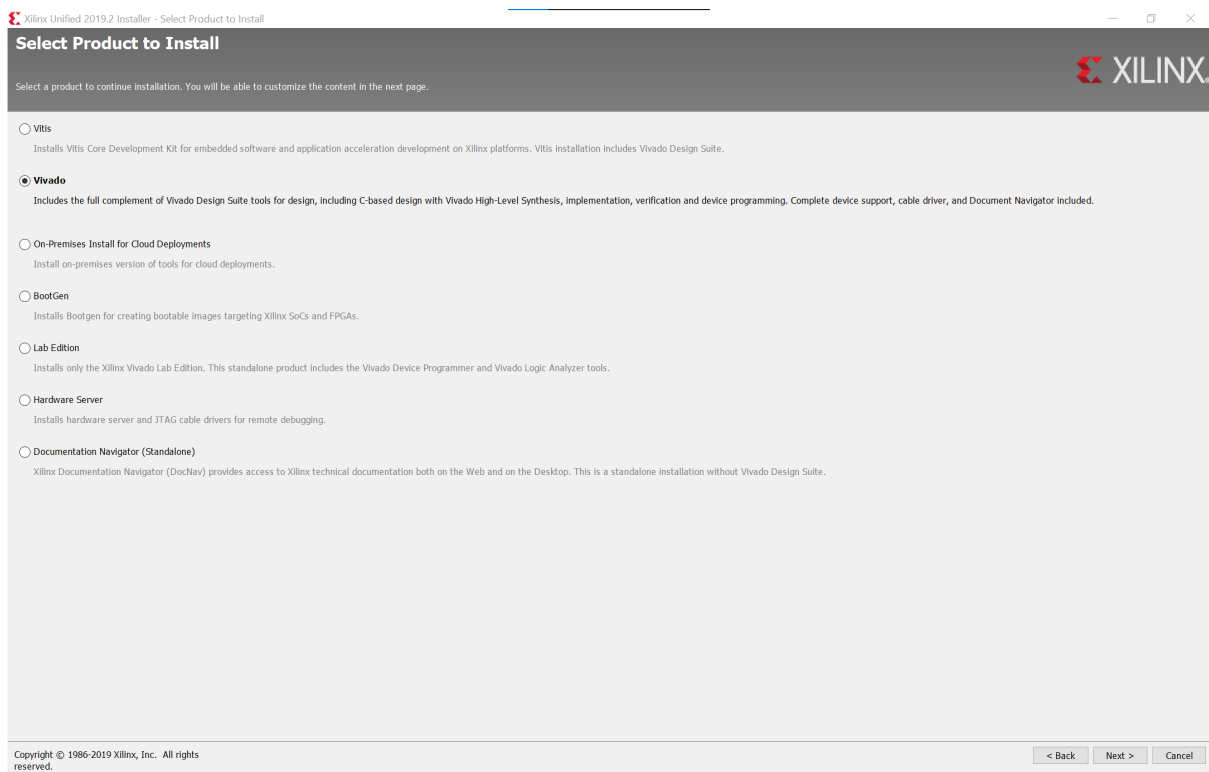
The screenshot shows the 'Vivado 2019.1 Installer - Select Install Type' window. It features the Xilinx logo in the top right corner. The main heading is 'Select Install Type'. Below it, a sub-heading reads 'Please select install type and provide your Xilinx.com user ID and password for authentication.' The window is divided into two main sections. The first section, 'User Authentication', contains a text prompt: 'Please provide your Xilinx user account credentials to download the required files. If you don't have an account, [please create one](#). If you forgot your password, you can [reset it here](#).' Below this are two input fields: 'User ID' with the text 'selmadilek' and 'Password' with masked characters. The second section contains two radio button options. The first option, 'Download and Install Now', is selected and includes a detailed description: 'Select your desired device and tool installation options and the installer will download and install just what is required. Downloaded installation files will be saved for future use. NOTE: Future installs using these downloaded files will be restricted to the options selected during this install. For access to all options later, choose "Download Full Image".' The second option, 'Download Full Image (Install Separately)', is unselected and includes a description: 'The installer will download an image containing all devices and tool options for later installation. Use this option if you wish to install a full image on a network drive or allow different users maximum flexibility when installing.' At the bottom of the window, there is a copyright notice: 'Copyright © 1986-2019 Xilinx, Inc. All rights reserved.' and three buttons: '< Back', 'Next >', and 'Cancel'.

Select **Download and Install Now** and click **Next**. On the next page agree to all Terms, Conditions and Agreements and click **Next**.

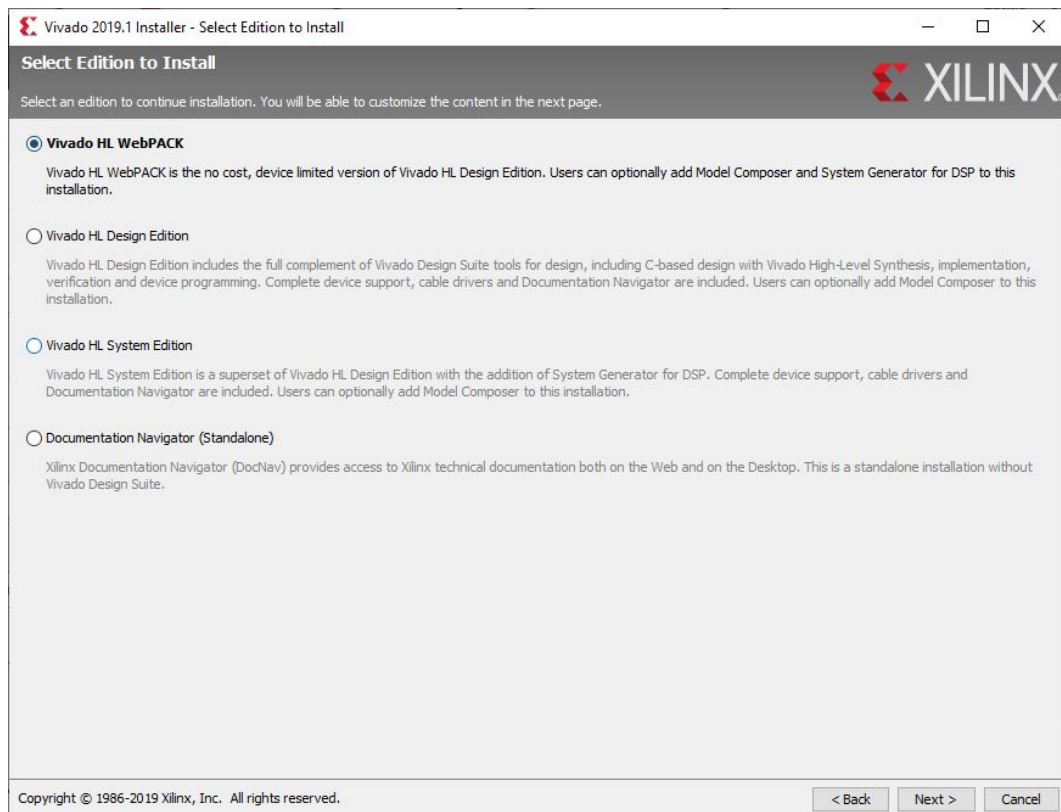


The screenshot shows the 'Vivado 2019.1 Installer - Accept License Agreements' window. It features the Xilinx logo in the top right corner. The main heading is 'Accept License Agreements'. Below it, a sub-heading reads 'Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.' The window is divided into three sections, each with a checkbox labeled 'I Agree'. The first section, 'Xilinx Inc. End User License Agreement', includes the text: 'By checking "I Agree" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, I AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).' The second section, 'WebTalk Terms And Conditions', includes the text: 'By checking "I Agree" below, I also confirm that I have read [Section 13 of the terms and conditions](#) above concerning WebTalk and have been afforded the opportunity to read the WebTalk FAQ posted at <https://www.xilinx.com/products/design-tools/webtalk.html>. I understand that I am able to disable WebTalk later if certain criteria described in Section 13(c) apply. If they don't apply, I can disable WebTalk by uninstalling the Software or using the Software on a machine not connected to the internet. If I fail to satisfy the applicable criteria or if I fail to take the applicable steps to prevent such transmission of information, I agree to allow Xilinx to collect the information described in Section 13(a) for the purposes described in Section 13(b).' The third section, 'Third Party Software End User License Agreement', includes the text: 'By checking "I Agree" below, or OTHERWISE ACCESSING, DOWNLOADING, INSTALLING or USING THE SOFTWARE, I AGREE on behalf of licensee to be bound by the agreement, which can be viewed by [clicking here](#).' At the bottom of the window, there is a copyright notice: 'Copyright © 1986-2019 Xilinx, Inc. All rights reserved.' and three buttons: '< Back', 'Next >', and 'Cancel'.

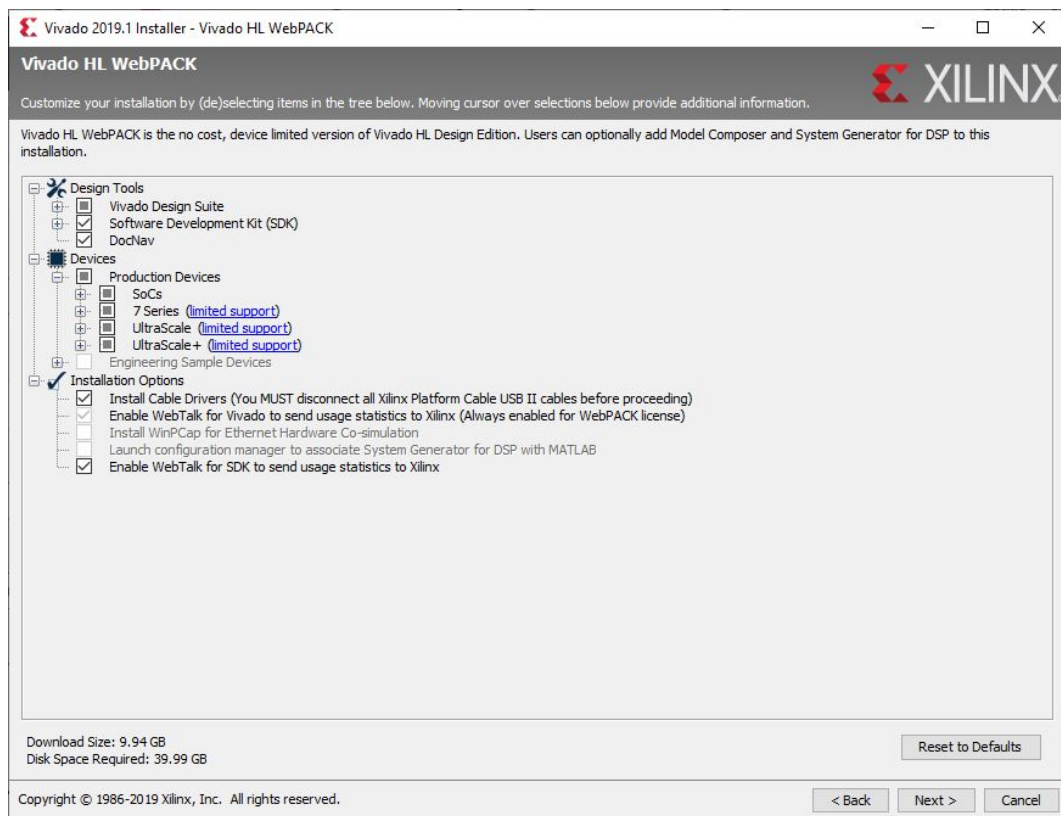
Select **Vivado** and click **Next**.



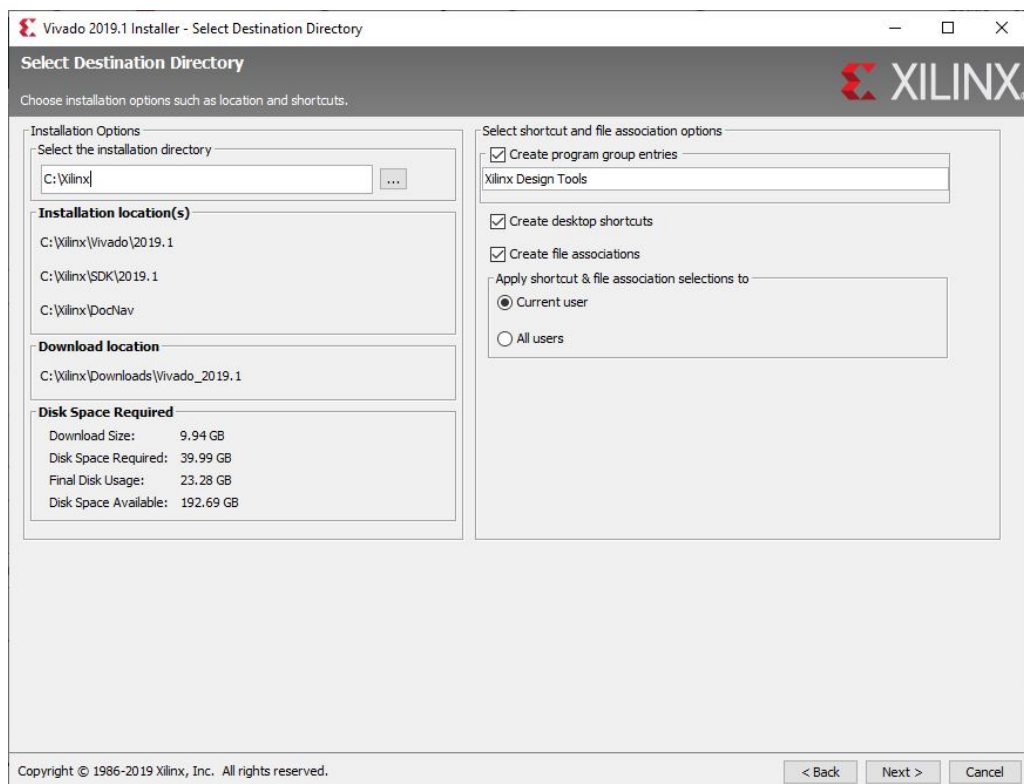
Select **Vivado HL WebPACK** and click **Next**.



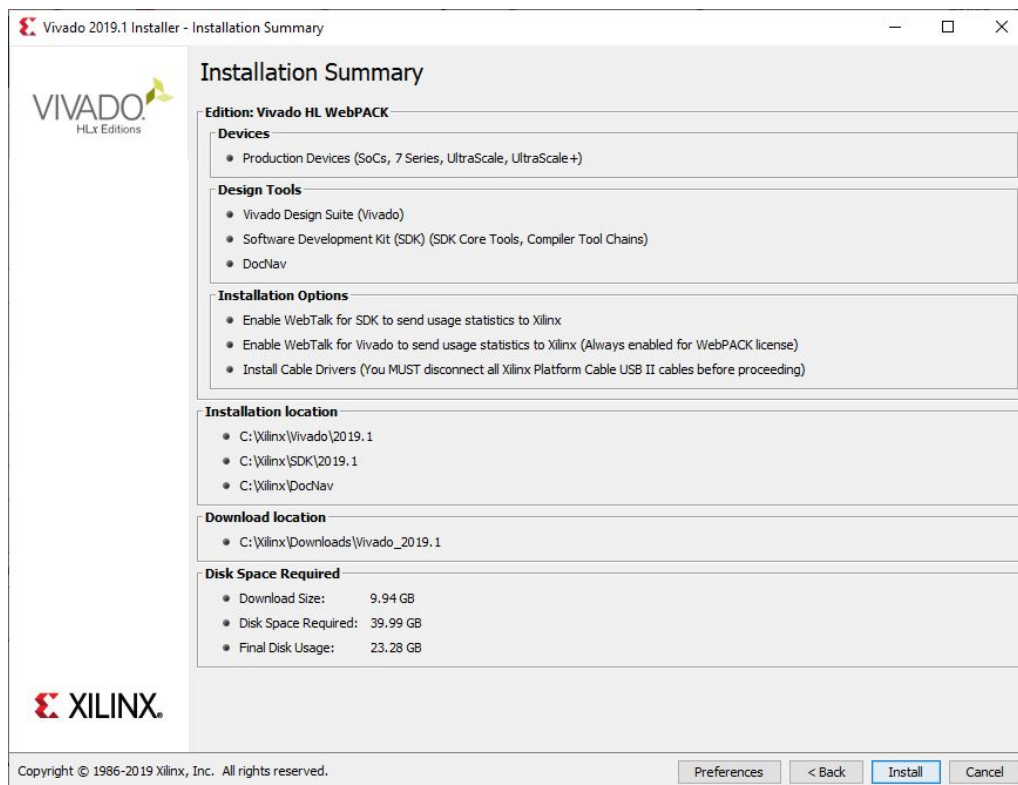
Don't change anything here, just click **Next**.



Here you can choose your installation directory.



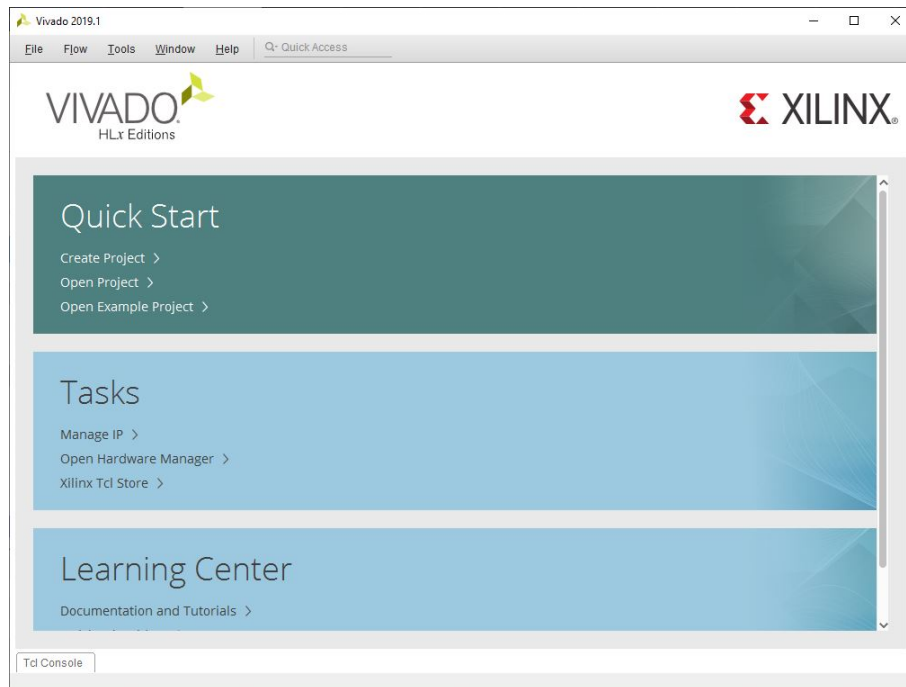
Click on **Install**.



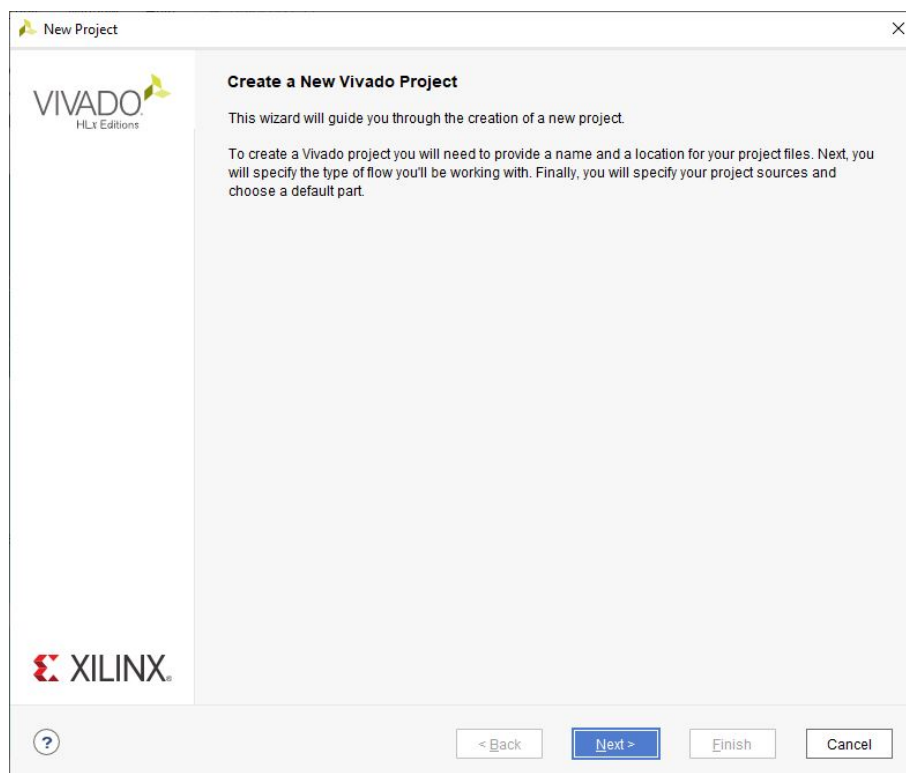
Installation will probably take a bit long. Once it is completed you may try to open your first Verilog project. Check the next page for the instructions.

Getting Started With Xilinx Vivado Design Suite

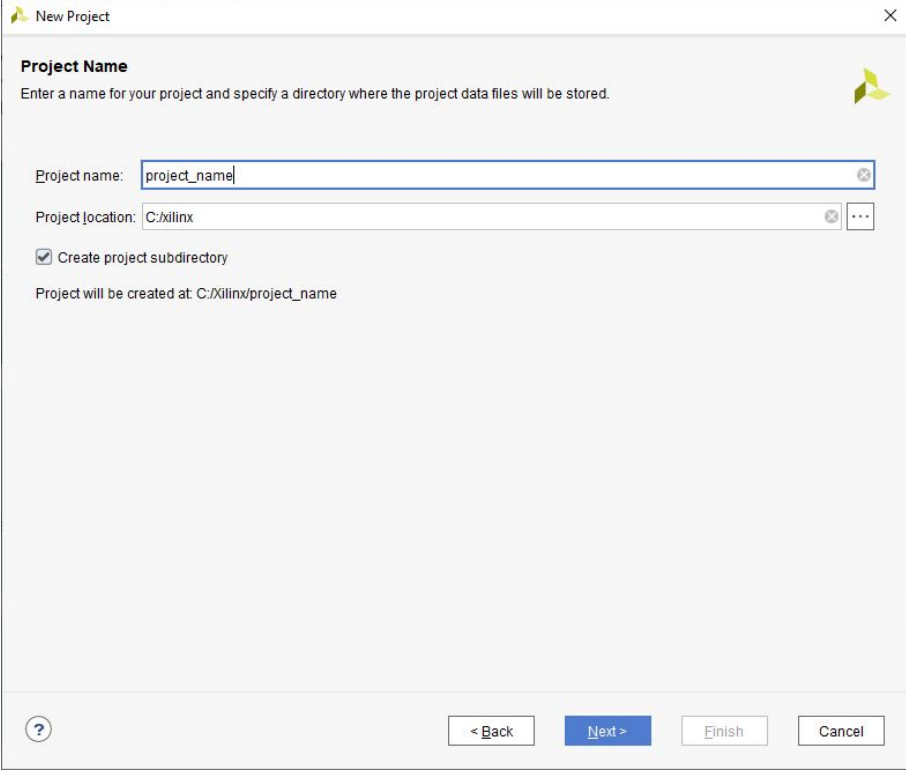
Once you have installed Vivado, you can create your first Verilog project. Click on **Create Project**.



Then click **Next**.



Give a name to your project and choose the location for your project files.



The 'New Project' dialog box is shown at the 'Project Name' step. The title bar says 'New Project' with a close button. The main area has a heading 'Project Name' and a sub-heading 'Enter a name for your project and specify a directory where the project data files will be stored.' Below this, there is a text field for 'Project name:' containing 'project_name' and a browse button. Below that is a text field for 'Project location:' containing 'C:/xilinx' and a browse button. A checkbox 'Create project subdirectory' is checked. Below the checkbox, it says 'Project will be created at: C:/Xilinx/project_name'. At the bottom, there is a help icon, a '< Back' button, a 'Next >' button, an 'Finish' button, and a 'Cancel' button.

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

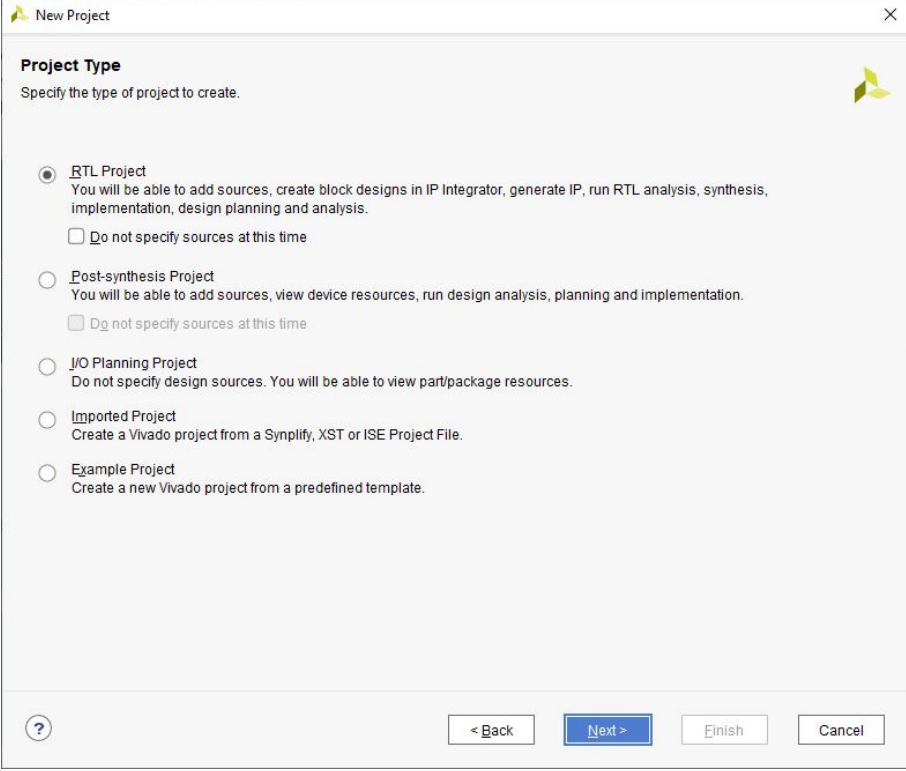
Project location:

☒ Create project subdirectory

Project will be created at: C:/Xilinx/project_name

[?](#) [< Back](#) [Next >](#) [Finish](#) [Cancel](#)

For project type, select **RTL Project**.



The 'New Project' dialog box is shown at the 'Project Type' step. The title bar says 'New Project' with a close button. The main area has a heading 'Project Type' and a sub-heading 'Specify the type of project to create.' Below this, there are five radio button options. The first option, 'RTL Project', is selected. The other options are 'Post-synthesis Project', 'I/O Planning Project', 'Imported Project', and 'Example Project'. At the bottom, there is a help icon, a '< Back' button, a 'Next >' button, an 'Finish' button, and a 'Cancel' button.

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.

☐ Do not specify sources at this time

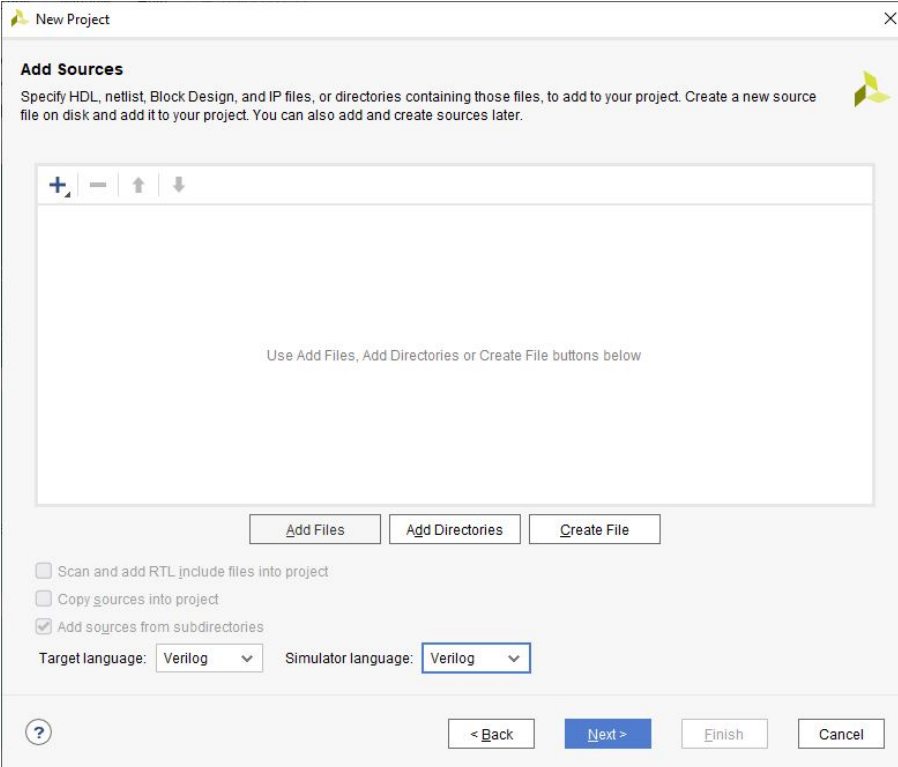
☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

[?](#) [< Back](#) [Next >](#) [Finish](#) [Cancel](#)

Since you will create your project from scratch, you don't need to add any sources or constraints at this stage. Just click **Next** at the following two pages.



New Project

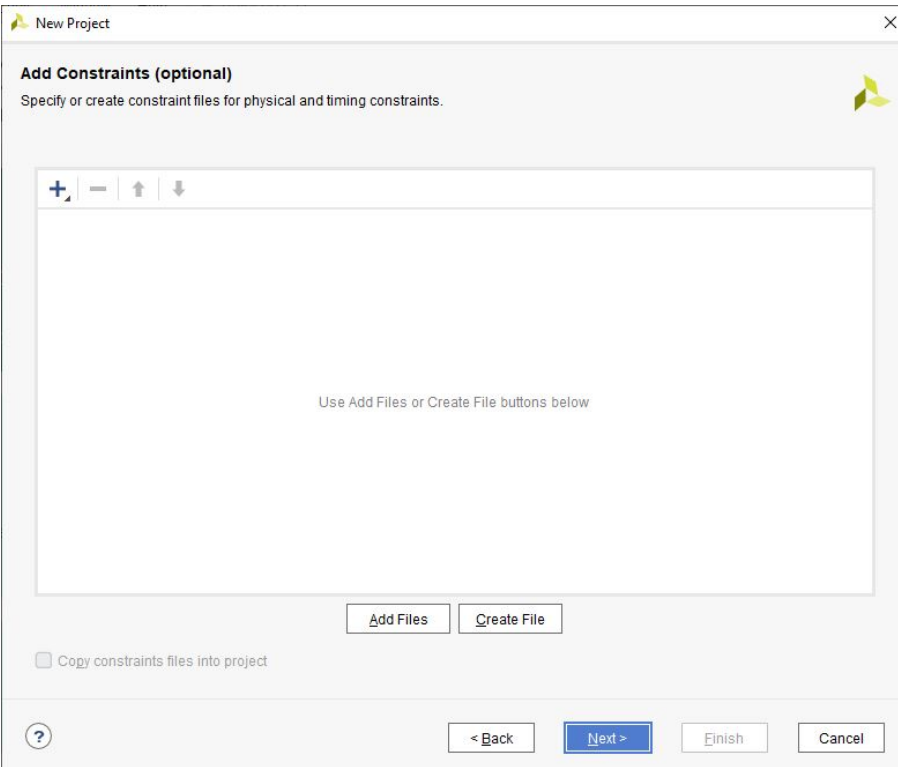
Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories

Target language: Verilog Simulator language: Verilog



New Project

Add Constraints (optional)

Specify or create constraint files for physical and timing constraints.

Use Add Files or Create File buttons below

☐ Copy constraints files into project

Select a board for your project. Choose **xc7a35tcpg236-1** from **Artix-7** family if you wish to make your simulations on the FPGA that we have in our lab. Click **Next** and then **Finish**.

New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category: All Package: All Remaining Temperature: All Remaining
Family: Artix-7 Speed: All Remaining Static power: All Remaining

Search: (4 matches)

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gt
xc7a35tcpg236-3	236	106	20800	41600	50	0	90	2
xc7a35tcpg236-2	236	106	20800	41600	50	0	90	2
xc7a35tcpg236-2L	236	106	20800	41600	50	0	90	2
xc7a35tcpg236-1	236	106	20800	41600	50	0	90	2

Navigation: ? < Back Next > Finish Cancel

New Project

VIVADO
HLS Editions

New Project Summary

- 1 A new RTL project named 'starter_project' will be created.
- 2 No source files or directories will be added. Use Add Sources to add them later.
- 3 No constraints files will be added. Use Add Sources to add them later.
- 4 The default part and product family for the new project:
Default Part: xc7a35tcpg236-1
Product: Artix-7
Family: Artix-7
Package: cpg236
Speed Grade: -1

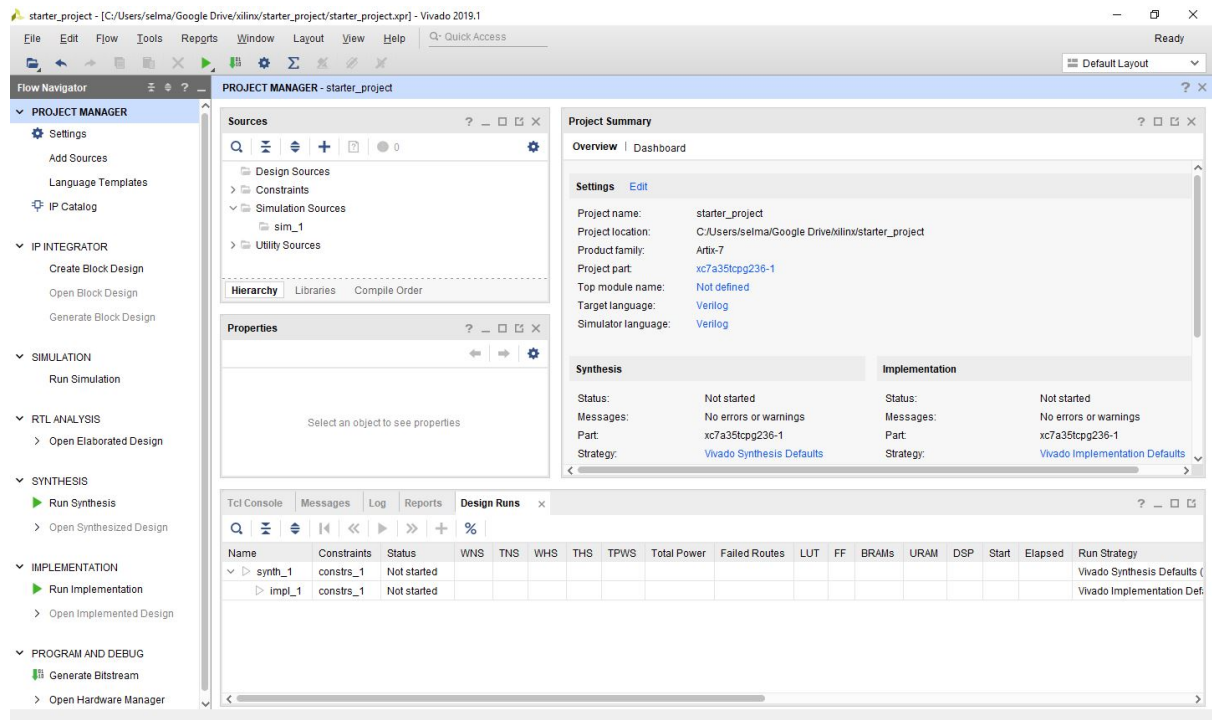
XILINX

To create the project, click Finish

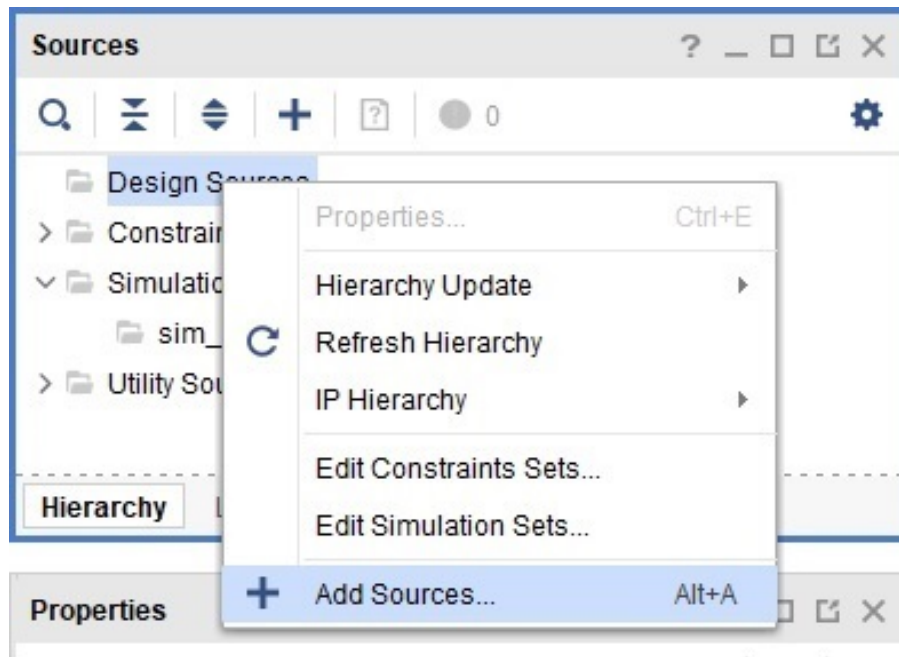
Navigation: ? < Back Next > Finish Cancel

A **Project Manager** will open, where you can see the following windows:

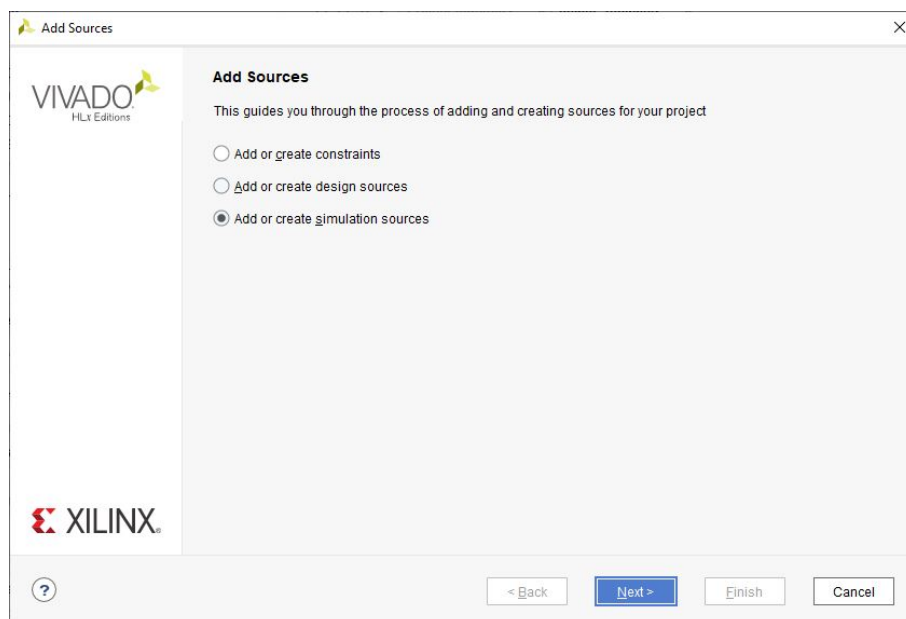
- **Flow Navigator:** Operations such as simulation, analysis, synthesis, etc. can be accessed from this menu.
- **Sources:** You can see your source files and the connection between them here.
- **Editor:** You will write your HDL code in this window. Also, circuit schematics, waveforms, etc. can be viewed in this window.
- **Status:** Console, messages, logs, etc. that indicate the status of your implementation will be shown here.



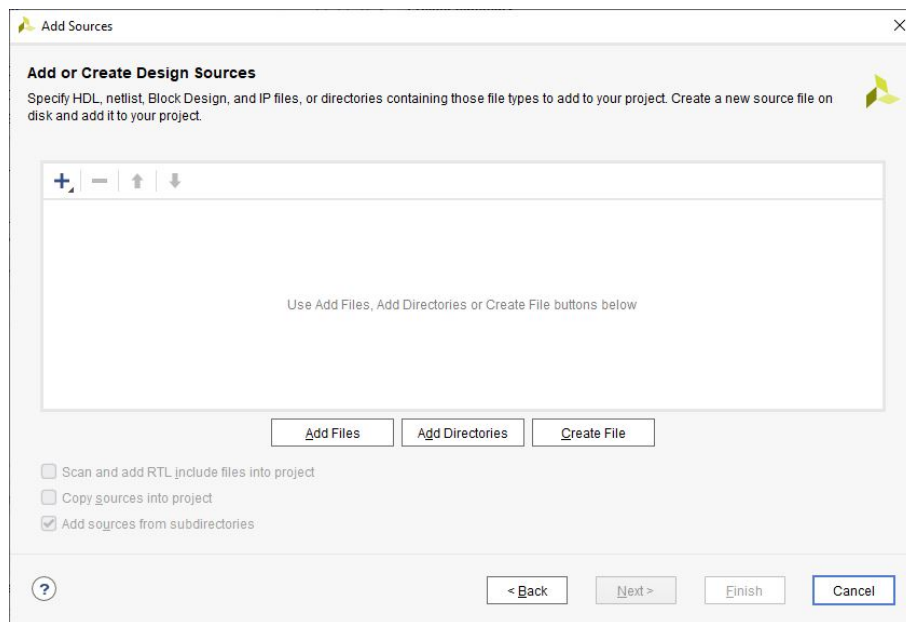
To add a Verilog source file to your project, right click on **Design Sources** in the **Sources** window and click on **Add Sources...**



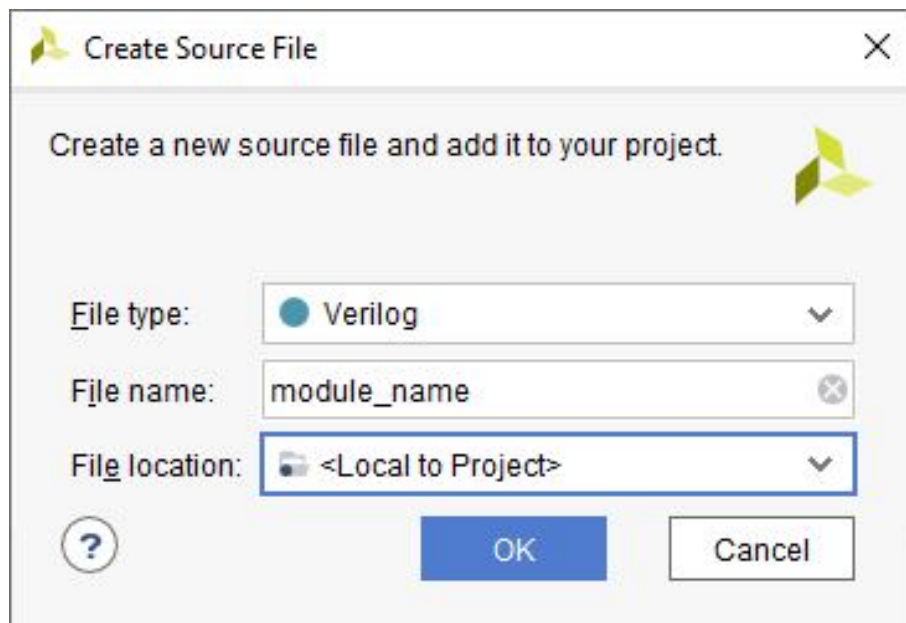
Select **Add or Create simulation sources** and click in **Next**.



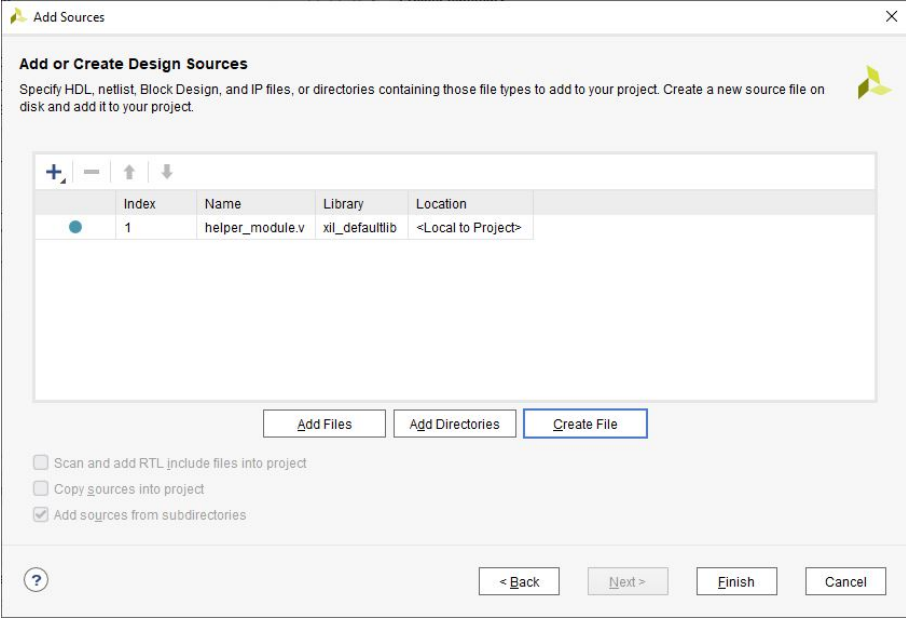
Click on **Create File**.



Select **Verilog** as File type and give a name to your file.



Click on **Finish** to get prompted to define your module.



Add Sources

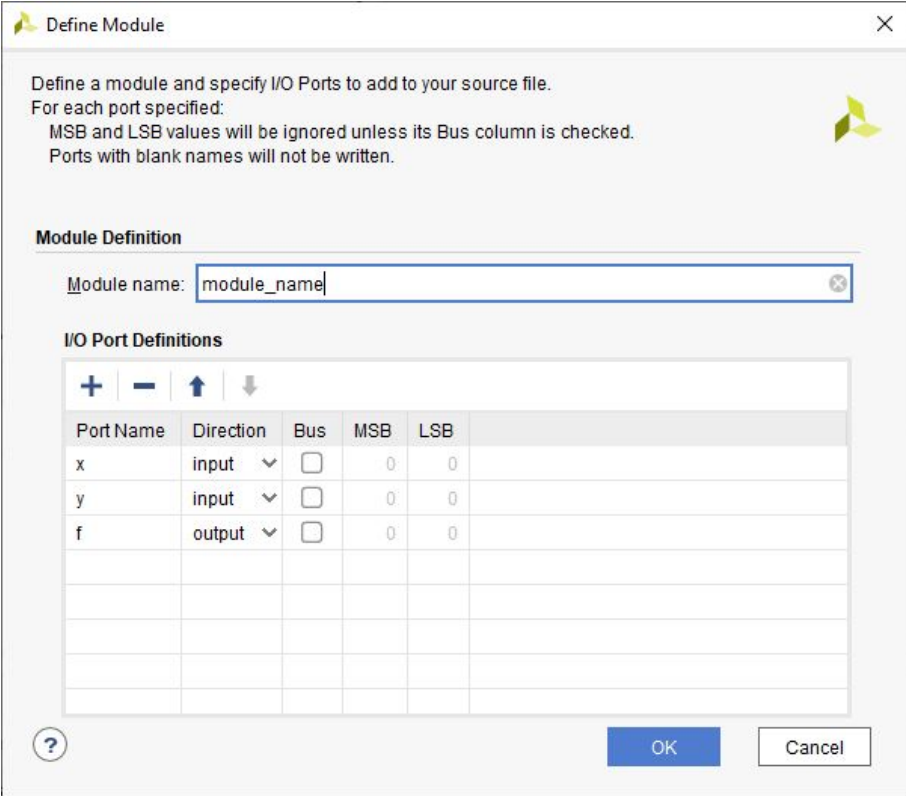
Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

	Index	Name	Library	Location
	1	helper_module.v	xil_defaultlib	<Local to Project>

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories

You can specify your input and output ports here, but it is not mandatory. You can specify them later in your HDL code.



Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

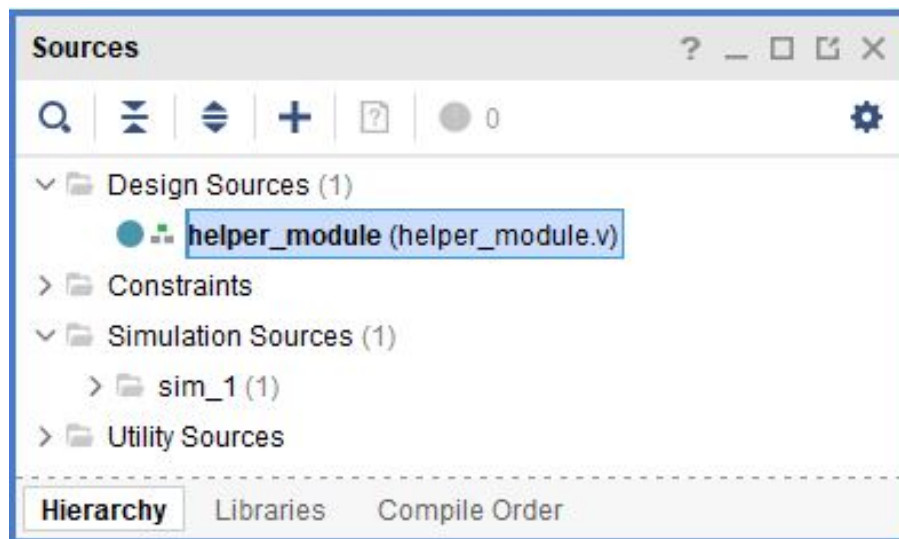
Module Definition

Module name:

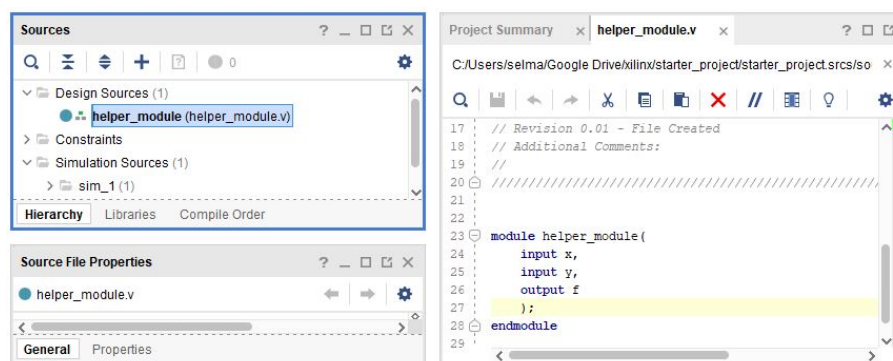
I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
x	input	<input type="checkbox"/>	0	0
y	input	<input type="checkbox"/>	0	0
f	output	<input type="checkbox"/>	0	0

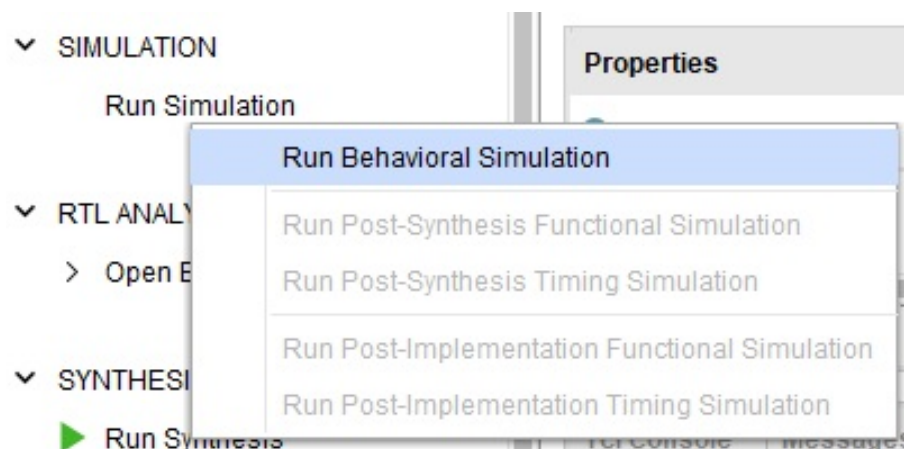
After this step, you will be able to see your module in the **Sources** window.



Vivado will create a starter code for you in the **Editor**.



After you have written your modules and a testbench you can simulate your design to verify it is working correctly. To do that, click on **Run Simulation** within the **Flow Navigator** and select **Run Behavioral Simulation**.



You can inspect the waveform of your simulation to verify the correctness of your design.

