BBM233 Logic Design Lab
Fall 2019

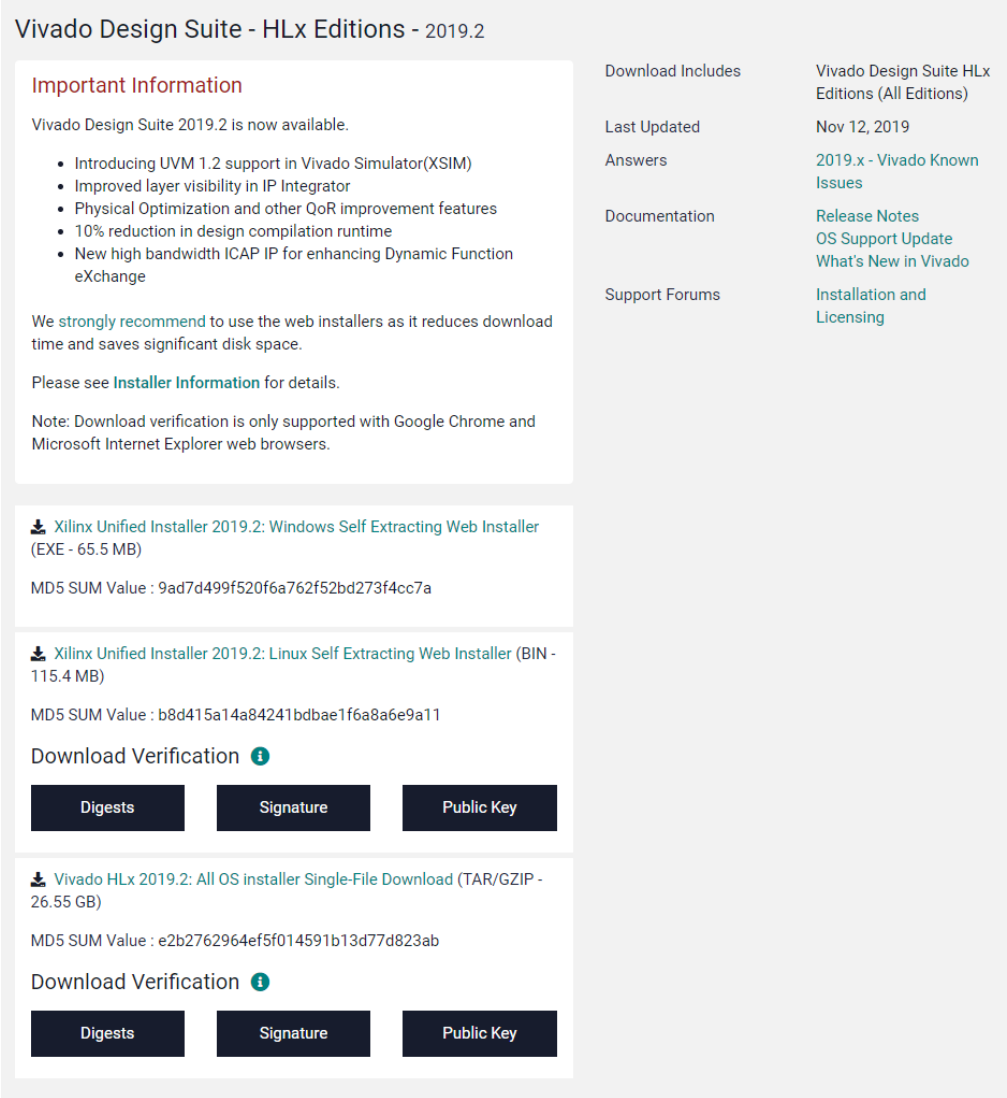
Guide to Verilog Lab Experiments - Getting Started With Verilog Projects

November 25, 2019

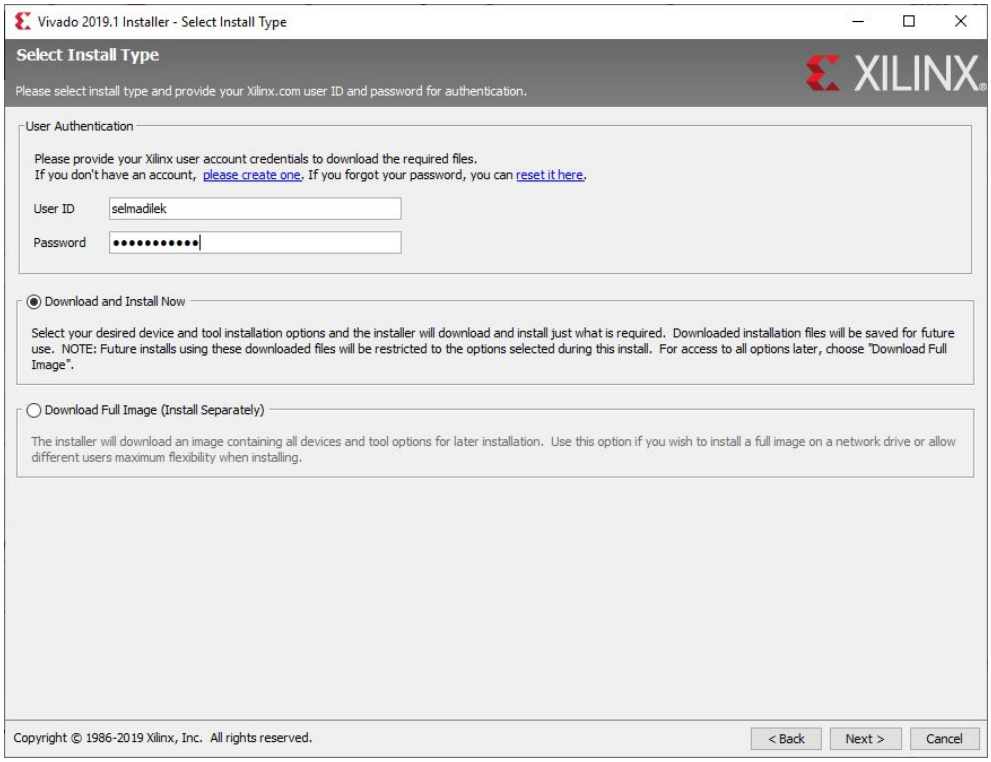
Installing Xilinx Vivado Design Suite on Windows

To install Vivado Design Suite WebPACK edition download **Vivado Unified Installer** from the Xilinx's website: `https://www.xilinx.com/support/download.html`.

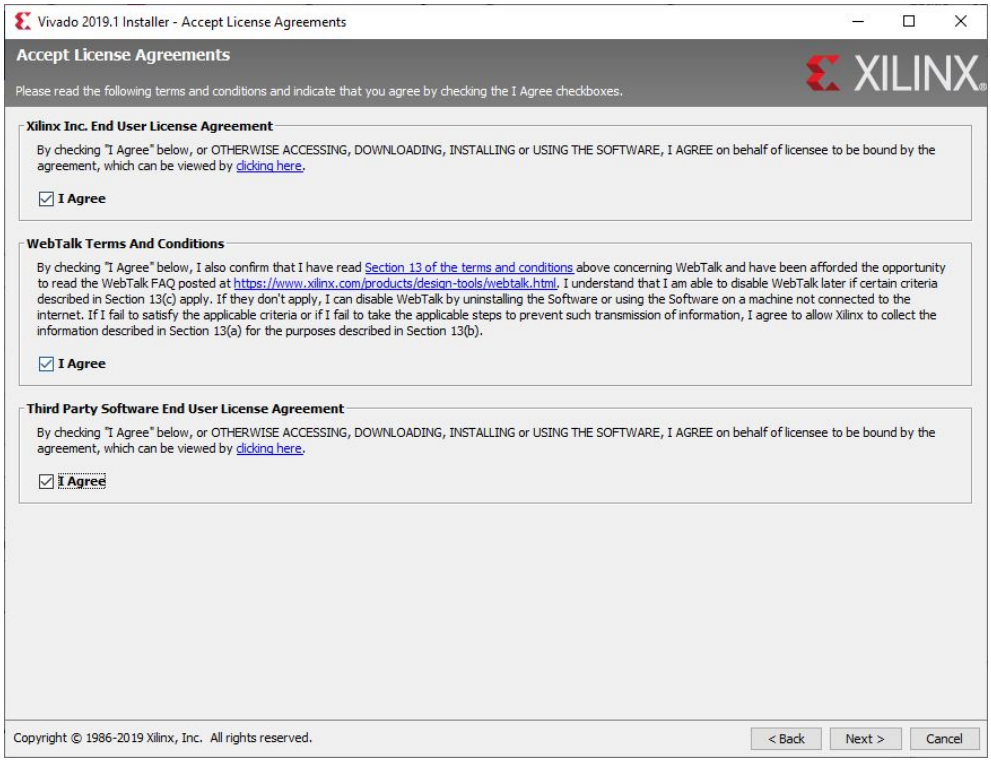
You will need to create a Xilinx account. You can use your school e-mail address.



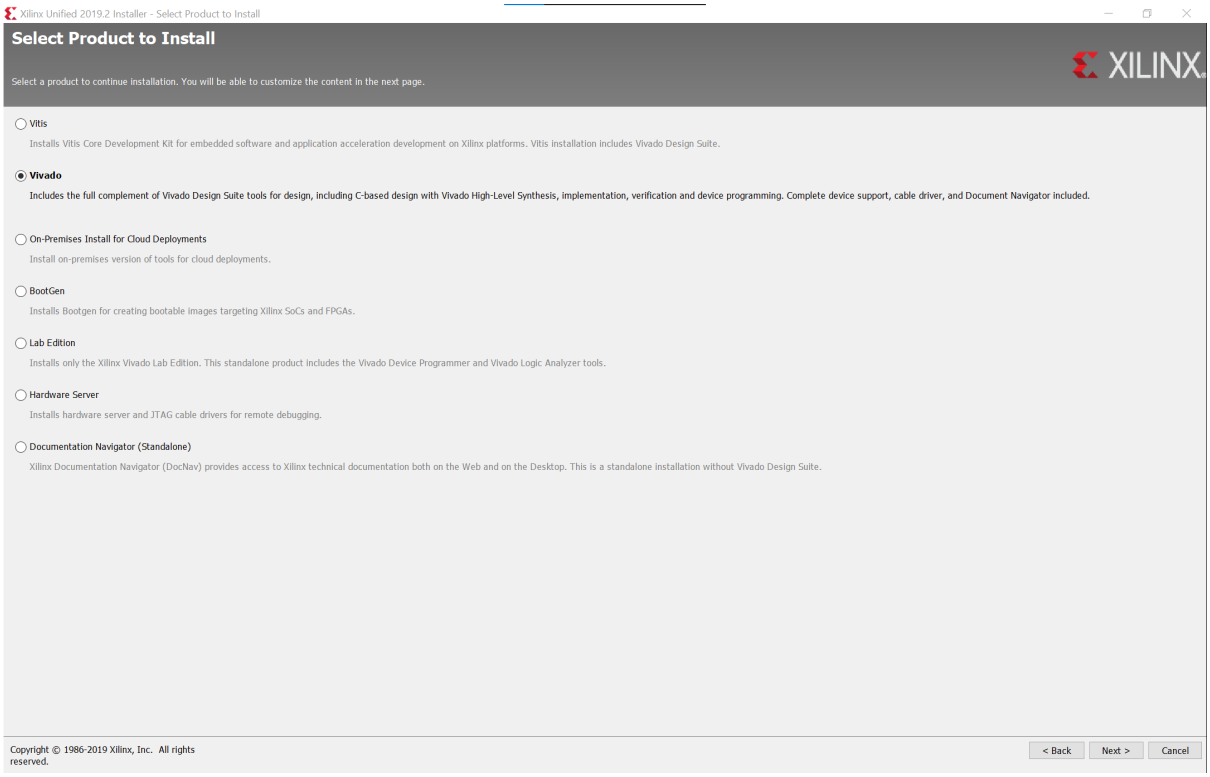
After clicking the first Next button, you will be prompted to enter your Xilinx account user ID and Password.



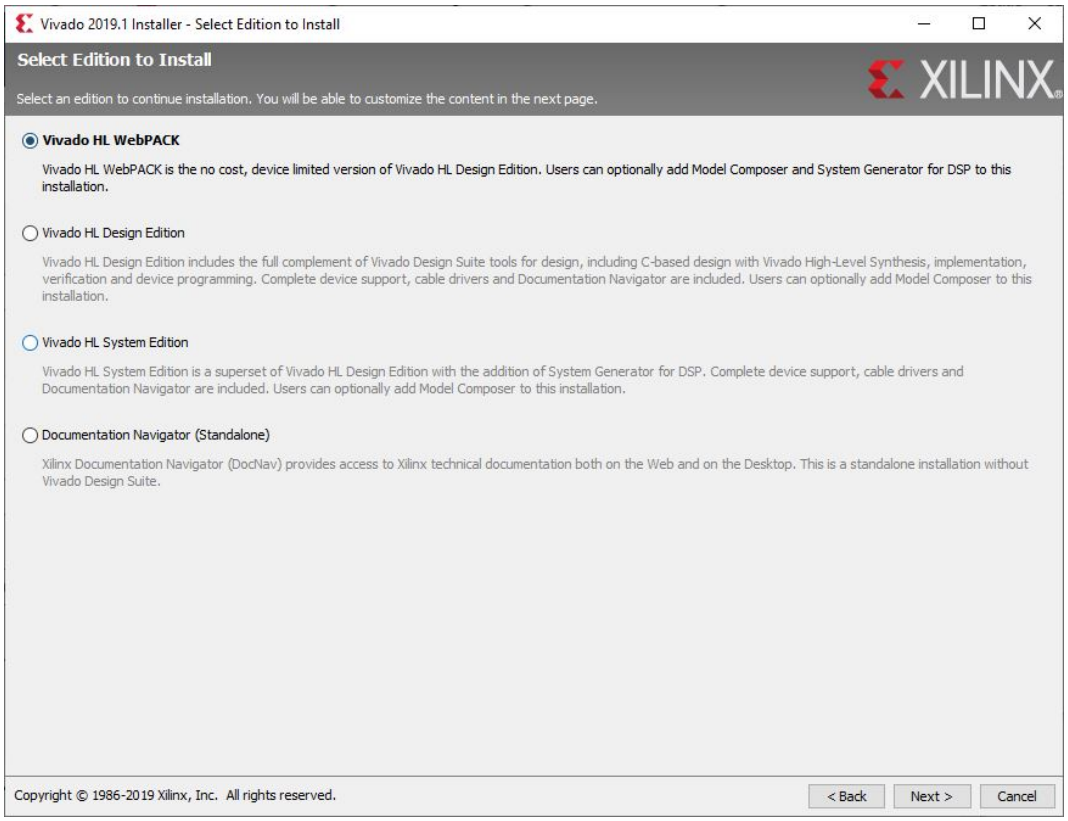
Select **Download and Install Now** and click **Next**. On the next page agree to all Terms, Conditions and Agreements and click **Next**.



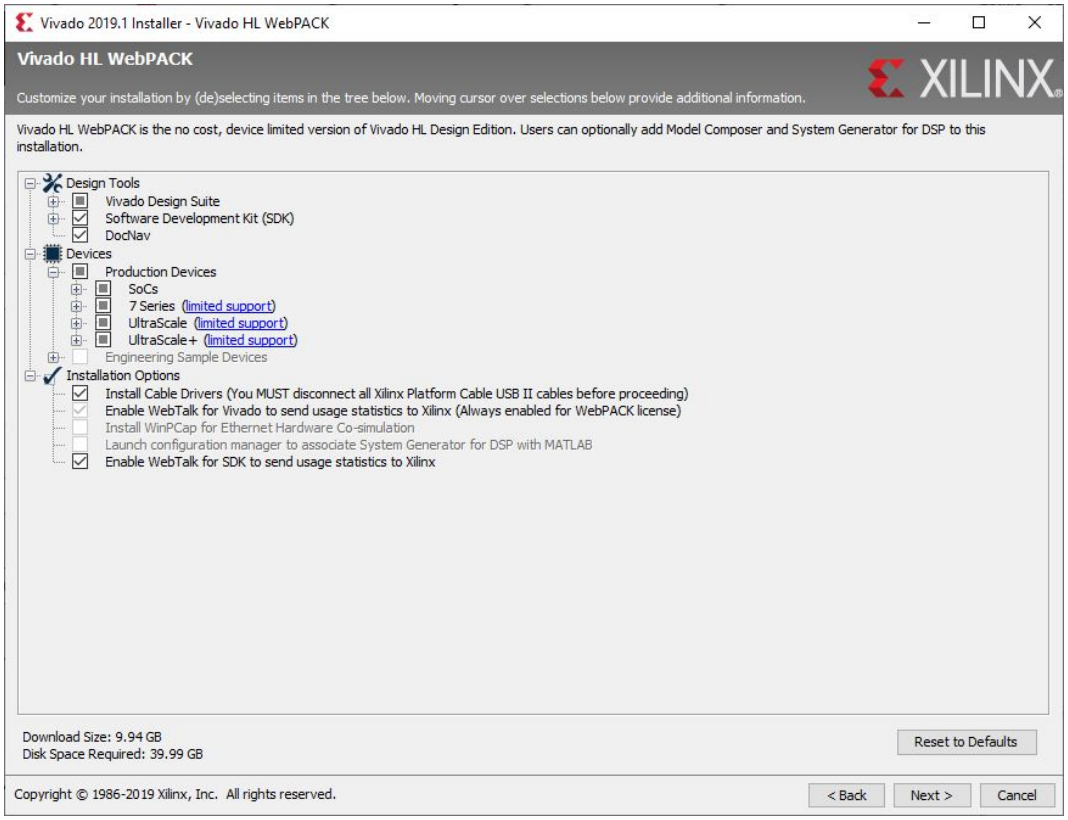
Select **Vivado** and click **Next**.



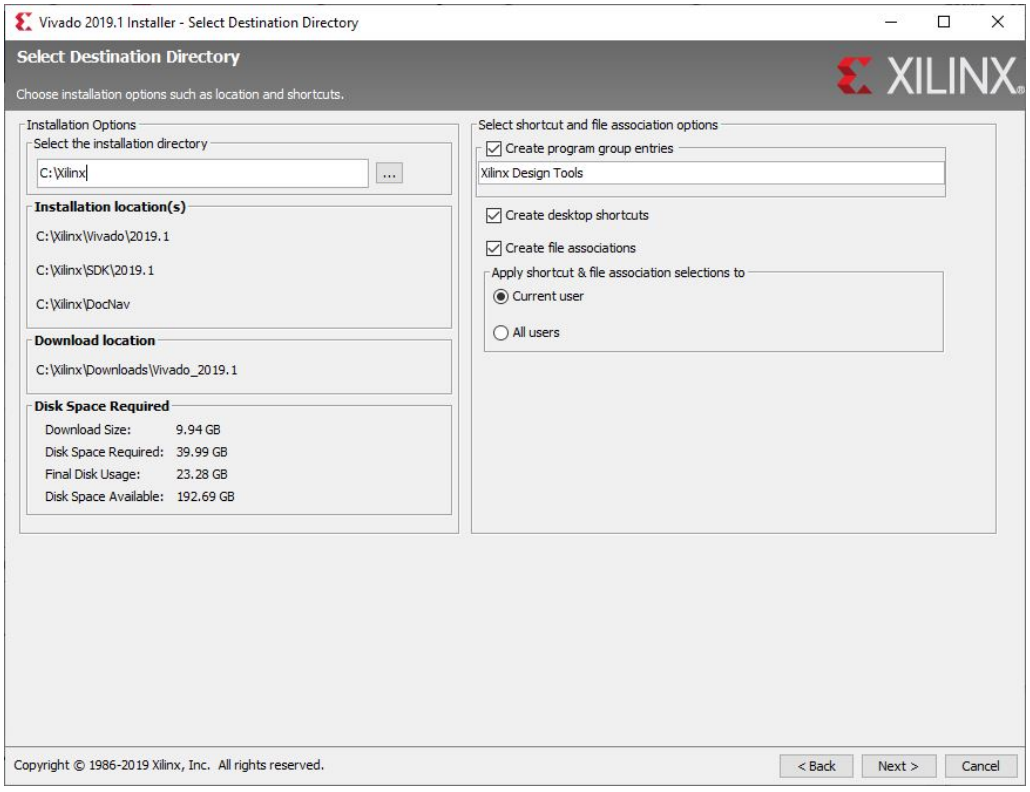
Select Vivado HL WebPACK and click **Next**.



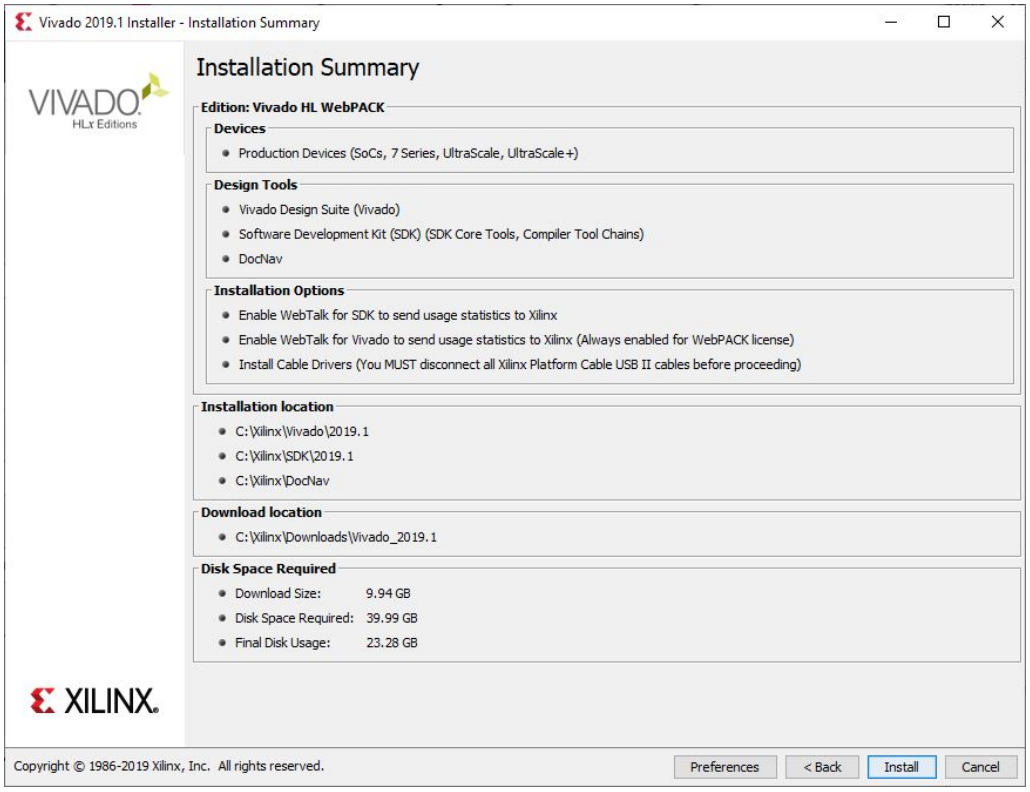
Don't change anything here, just click **Next**.



Here you can choose your installation directory.



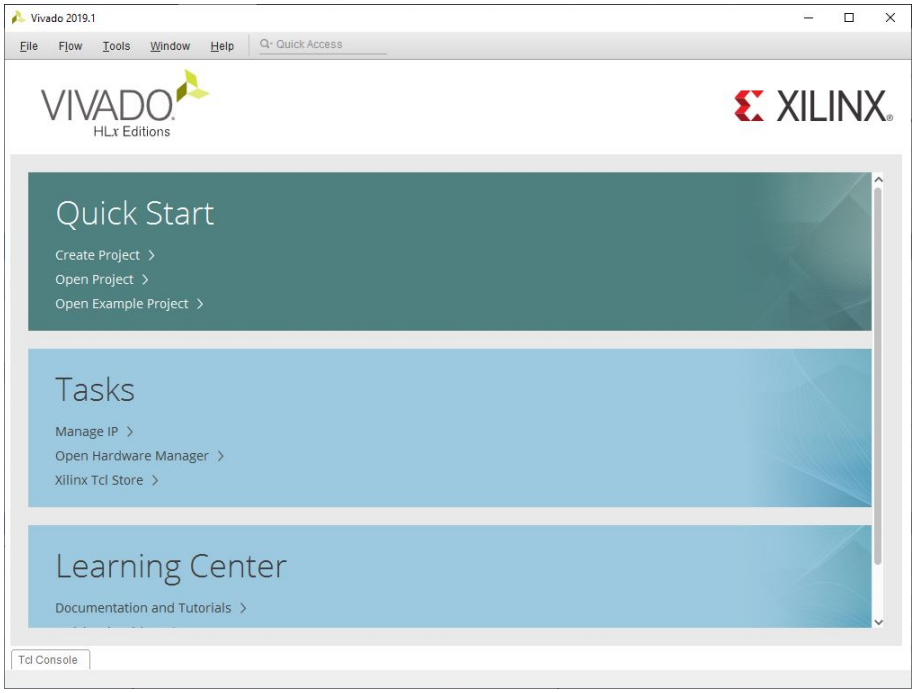
Click on **Install**.



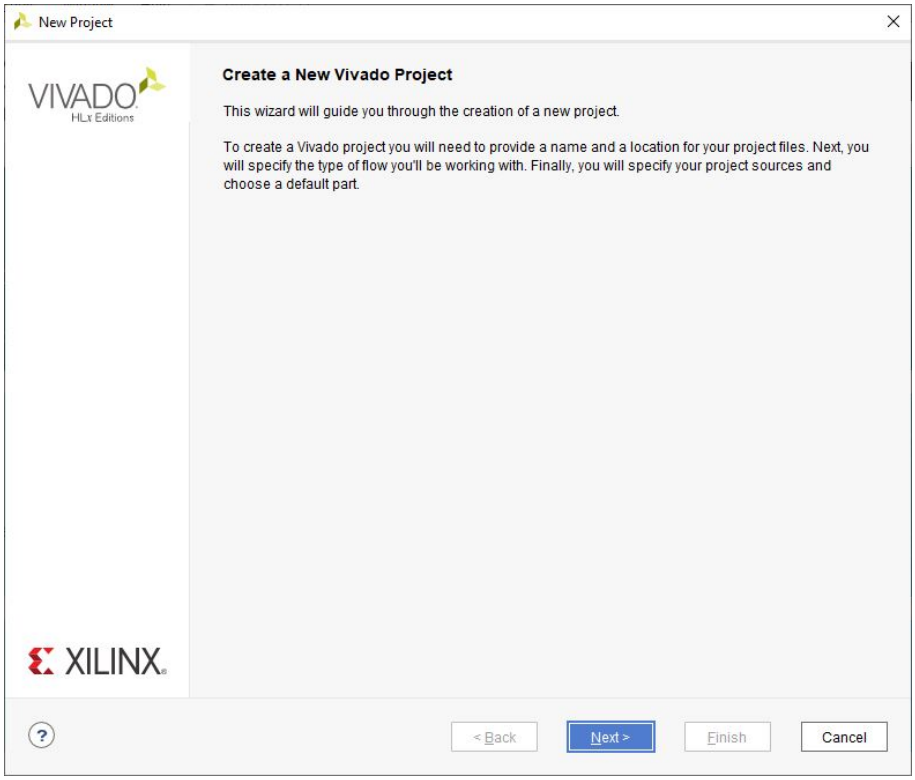
Installation will probably take a bit long. Once it is completed you may try to open your first Verilog project. Check the next page for the instructions.

Getting Started With Xilinx Vivado Design Suite

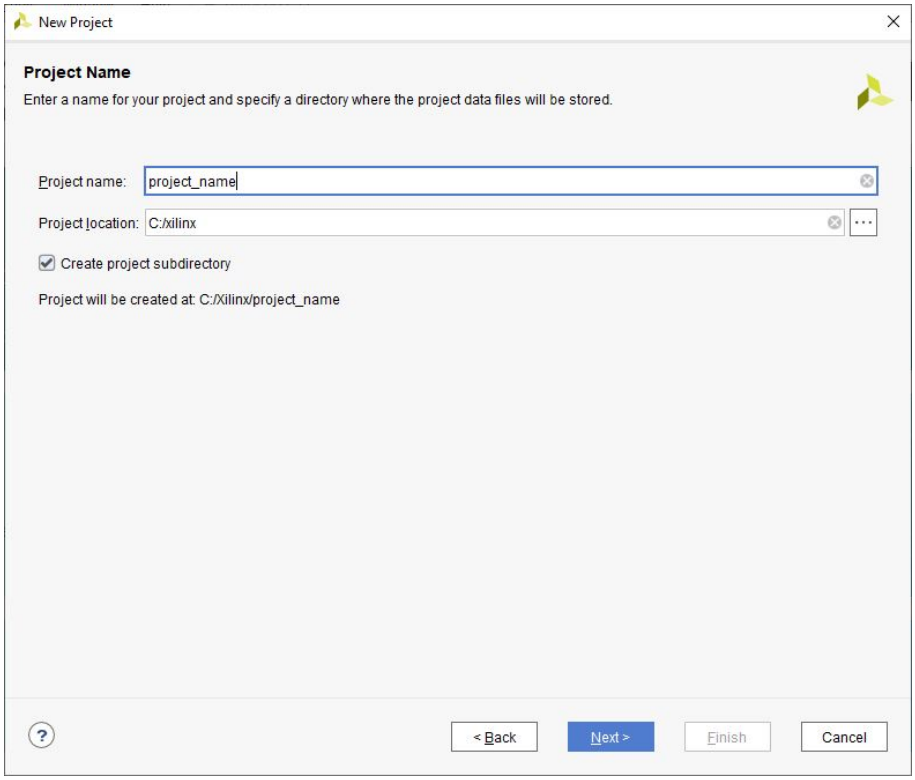
Once you have installed Vivado, you can create your first Verilog project. Click on **Create Project**.



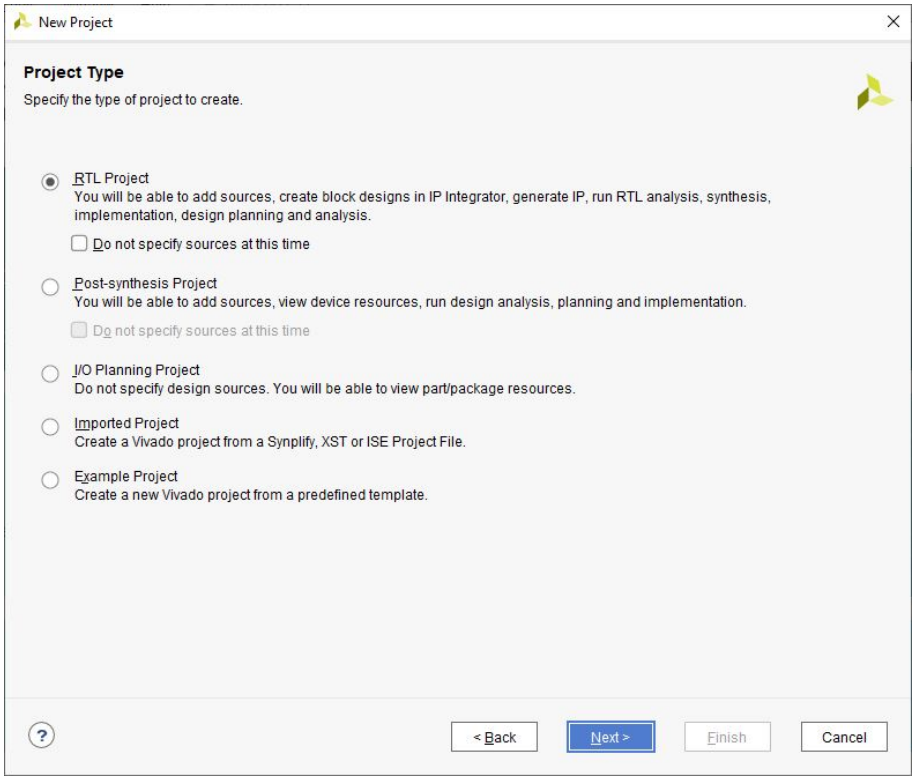
Then click **Next**.



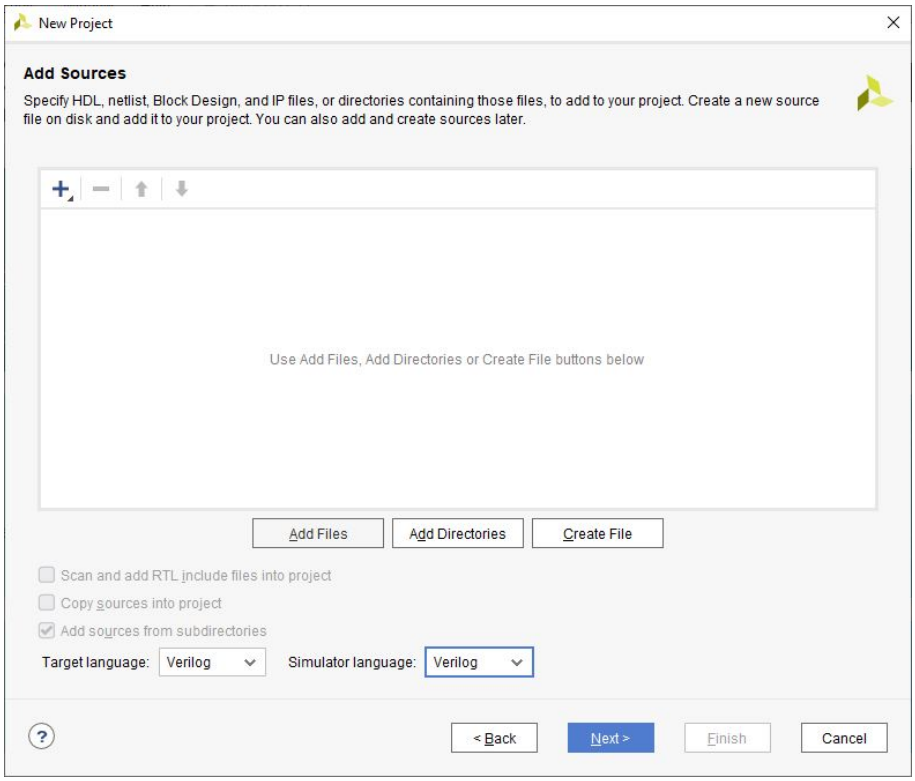
Give a name to your project and choose the location for your project files.

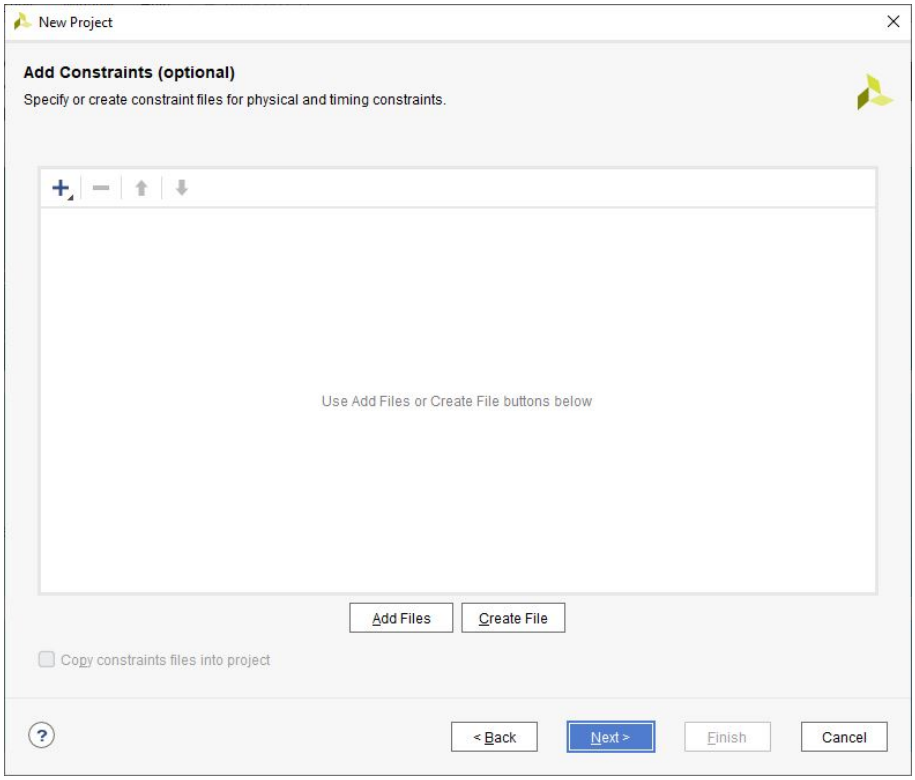


For project type, select **RTL Project**.

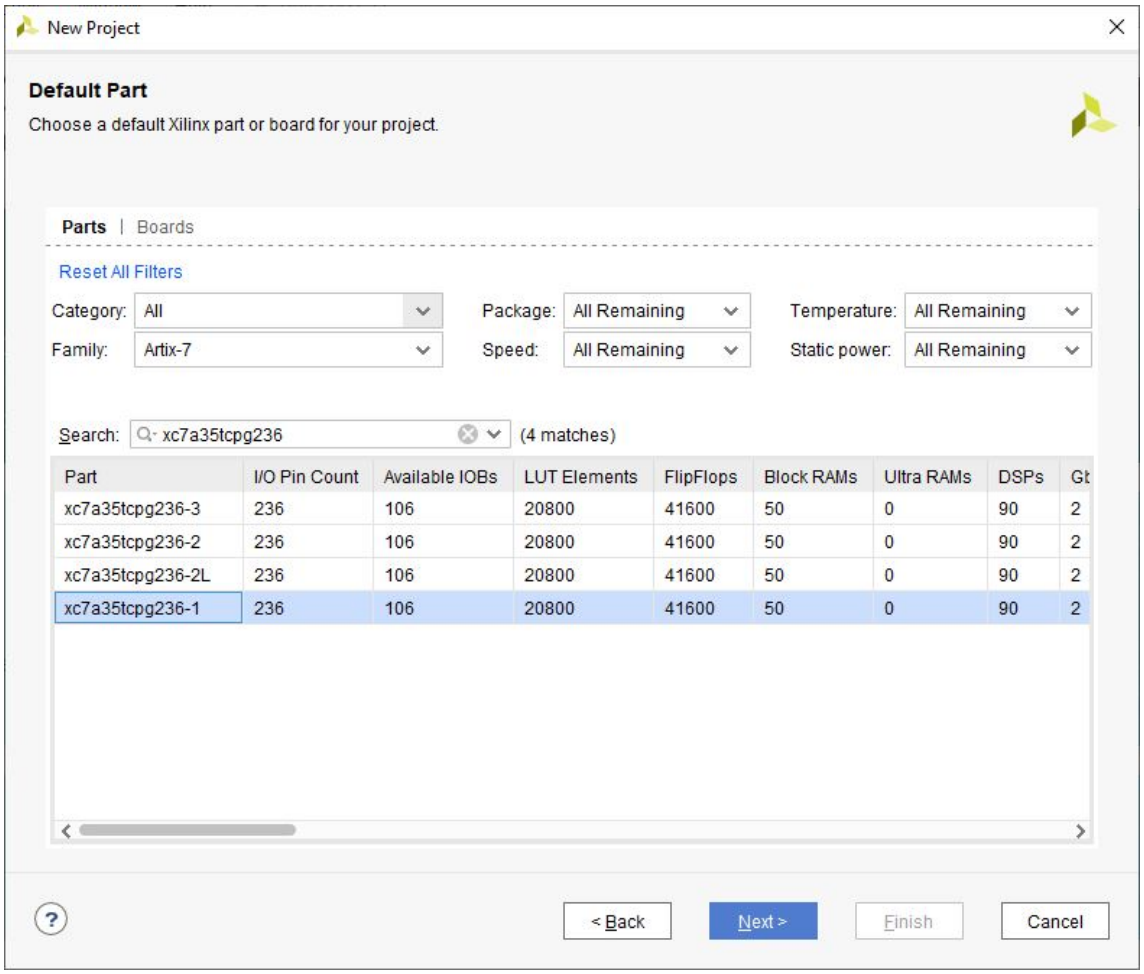


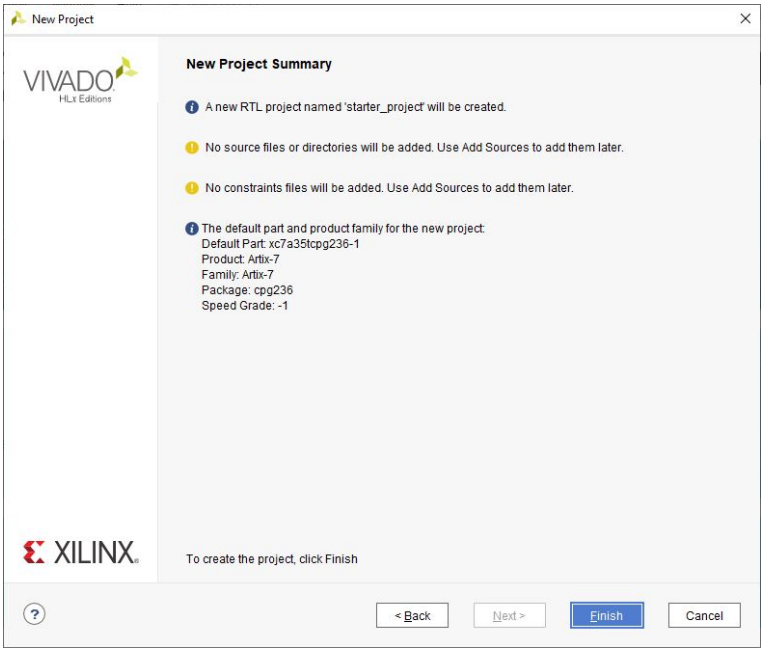
Since you will crate your project from scratch, you don't need to add any sources or constraints at this stage. Just click **Next** at the following to pages.





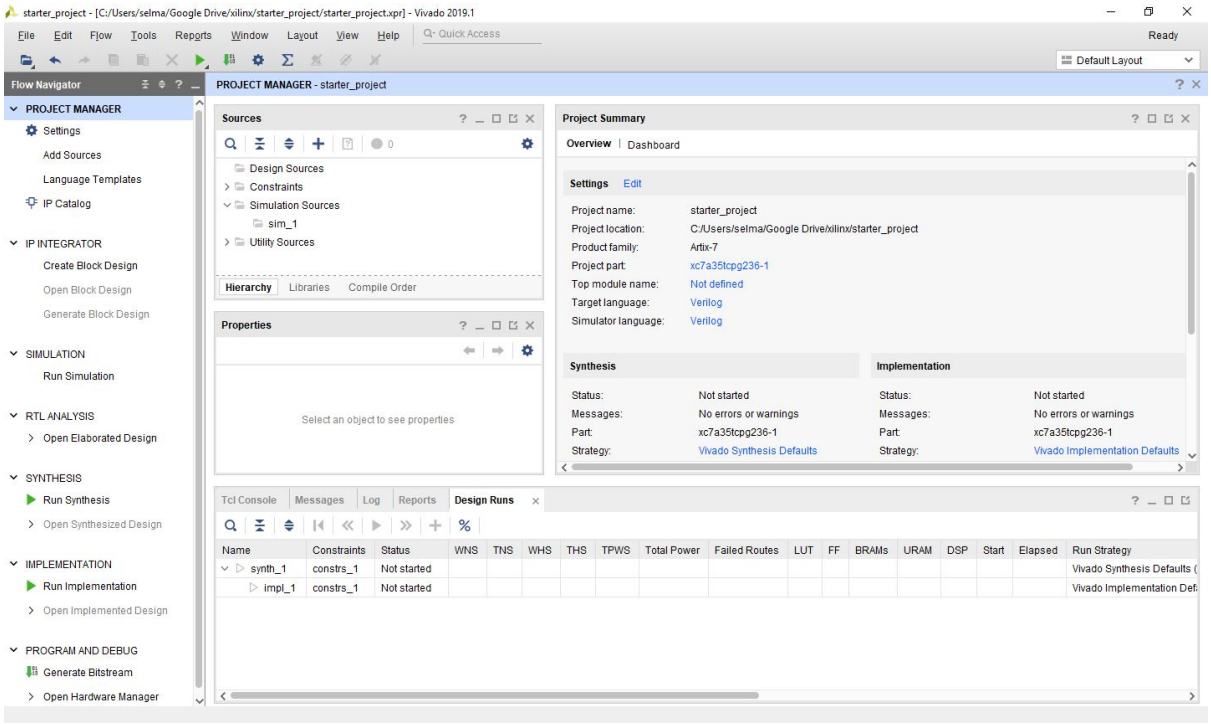
Select a board for your project. Choose **xc7a35tcpg236-1** from **Artix-7** family if you wish to make your simulations on the FPGA that we have in our lab. Click **Next** and then **Finish**.



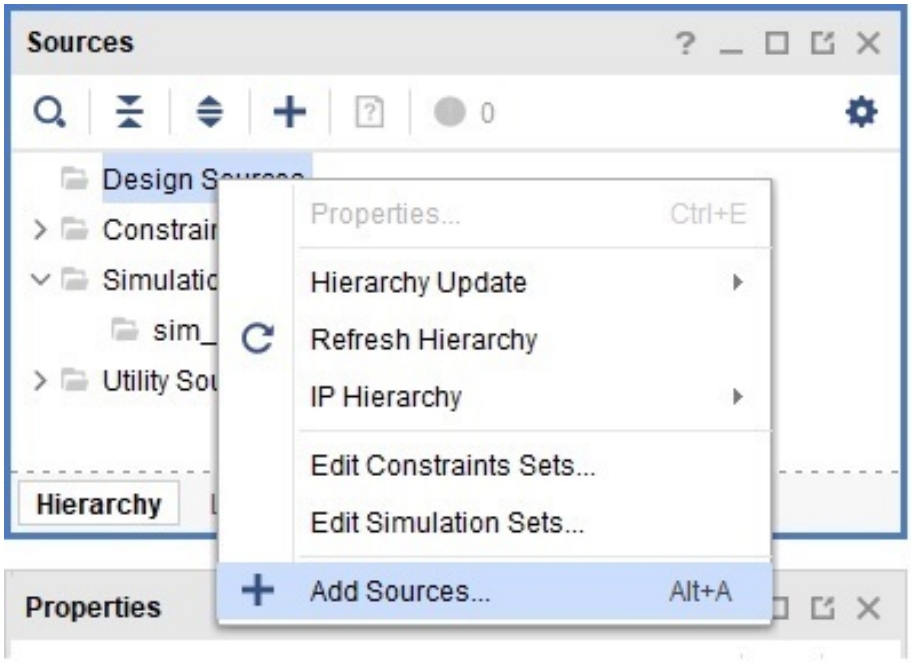


A **Project Manager** will open, where you can see the following windows:

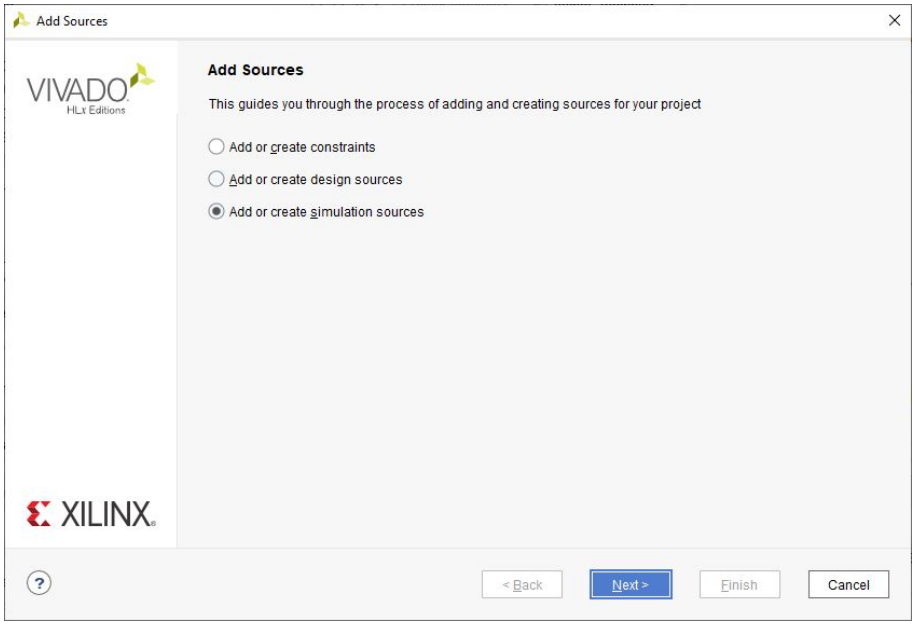
- **Flow Navigator:** Operations such as simulation, analysis, synthesis, etc. can be accessed from this menu.
- **Sources:** You can see your source files and the connection between them here.
- **Editor:** You will write your HDL code in this window. Also, circuit schematics, waveforms, etc. can be viewed in this window.
- **Status:** Console, messages, logs, etc. that indicate the status of your implementation will be shown here.



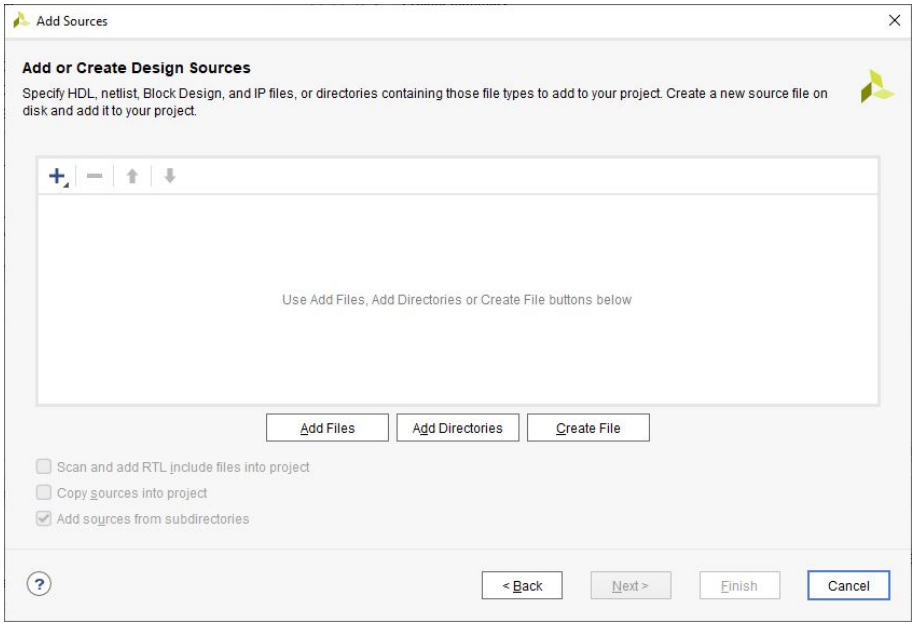
To add a Verilog source file to your project, right click on **Design Sources** in the **Sources** window and click on **Add Sources...**



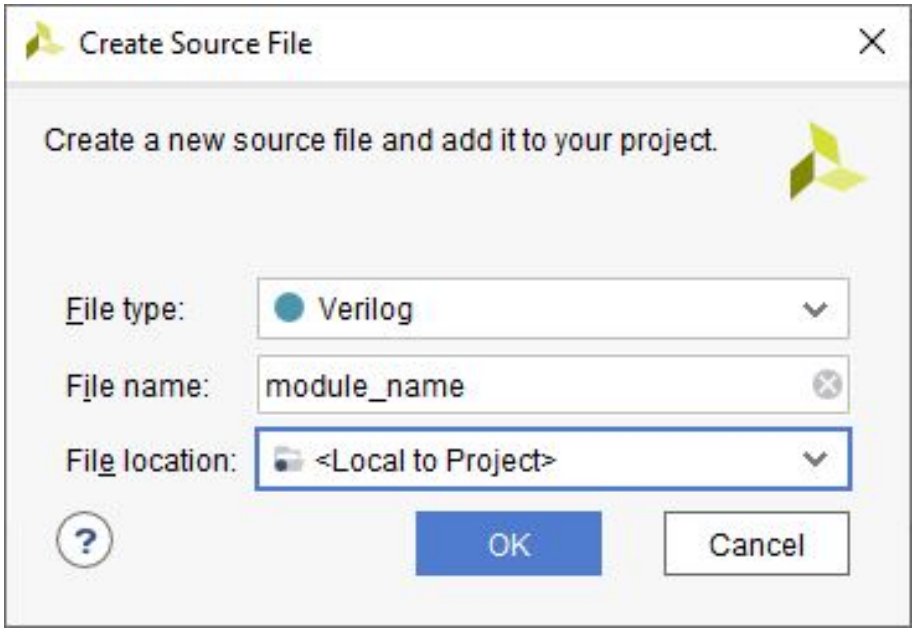
Select **Add or Create simulation sources** and click in **Next**.



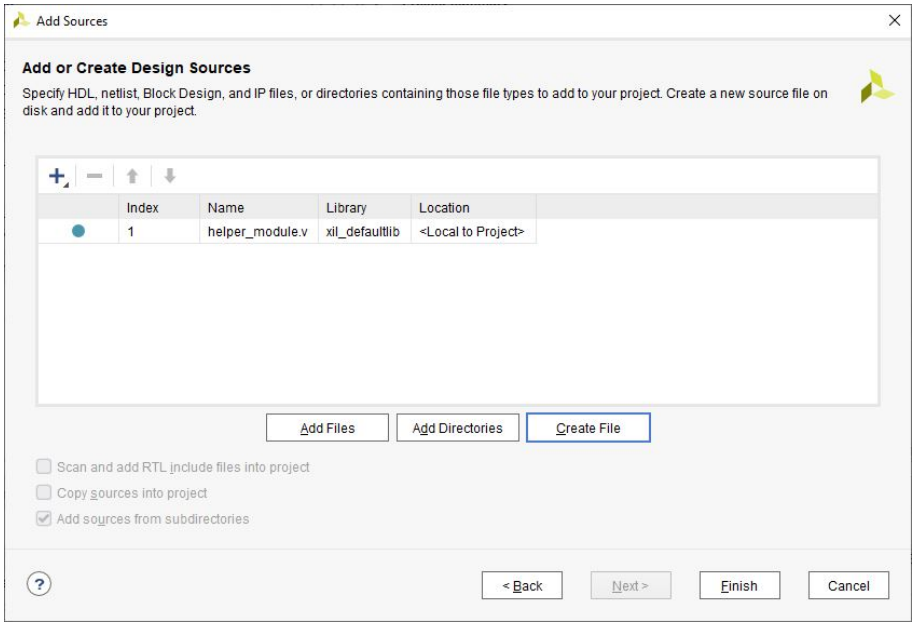
Click on **Create File**.



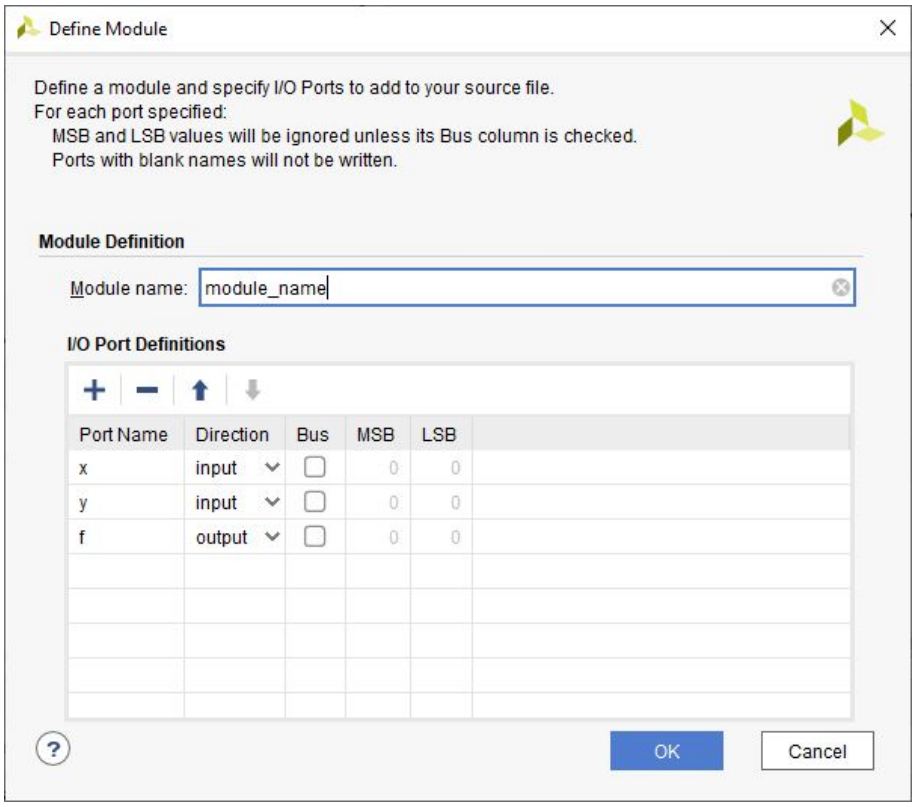
Select **Verilog** as File type and give a name to your file.



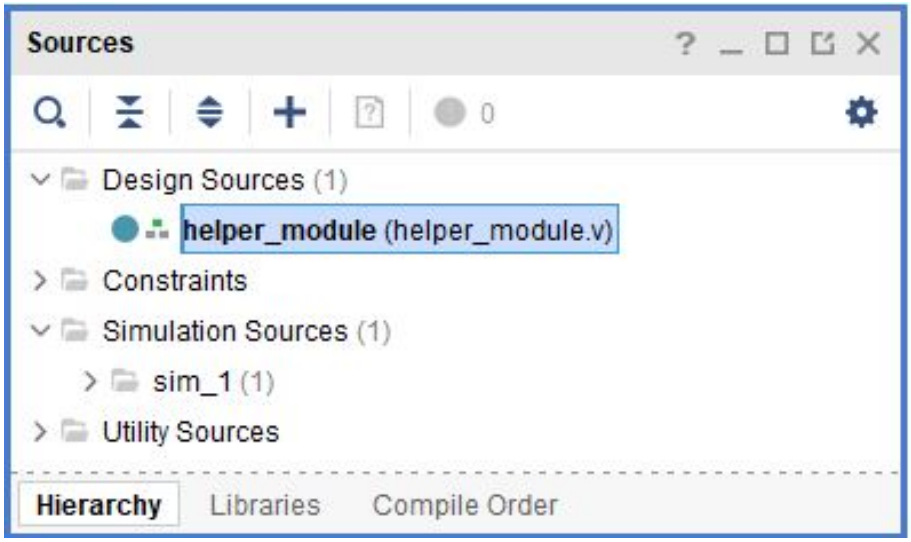
Click on **Finish** to get promted to define your module.



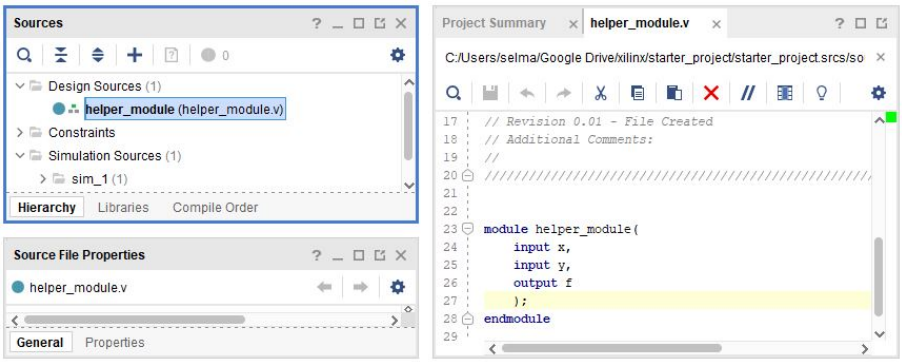
You can specify your input and output ports here, but it is not mandatory. You can specify them later in your HDL code.



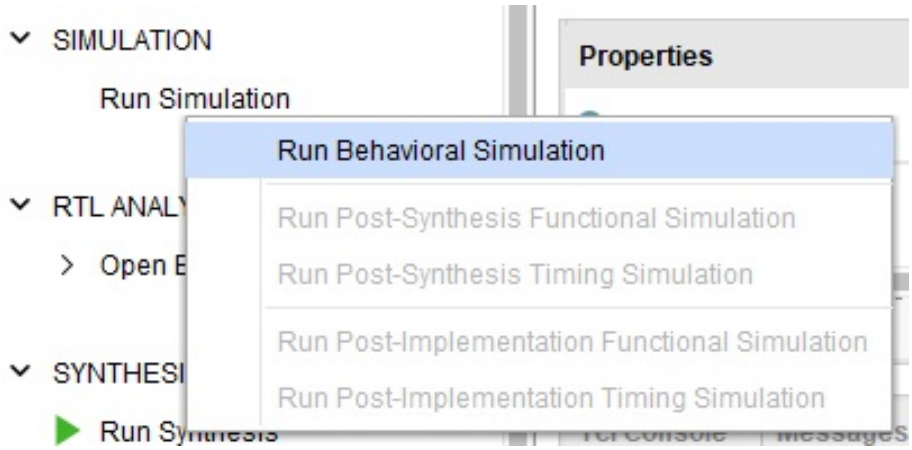
After this step, you will be able to see your module in the **Sources** window.



Vivado will create a starter code for you in the **Editor**.



After you have written your modules and a testbench you can simulate your design to verify it is working correctly. To do that, click on **Run Simulation** within the **Flow Navigator** and select **Run Behavioral Simulation**.



You can inspect the waveform of your simulation to verify the correctness of your design.