Name-Last Name: _____ **Student ID:** _____

Hacettepe University	Computer Engineering Department
BBM431-Advanced Computer Architecture	Instructor: Prof. Dr. Suleyman TOSUN
Final Exam	
Duration: 100 minutes	Exam Date: 20.01.2021

Questions	1	2	3	4	Total
Marks	25	25	40	10	100
Earned					

Make a single pdf of your answer sheets and send it to aca.odev@gmail.com.

Q1. Write the classes of parallel systems defined by Flynn's taxonomy. Write the "level of parallelism" that can be achieved by it. Finally, give an example system or architecture for each class.

Class	Level of parallelism	Example system/architecture

Q2. a) Suppose 40% of the program's code cannot be parallelized (must be sequential code) and remaining part can run in parallel. What is the speed up when this program runs on four processors instead of one? Show your calculations.

b) Assume that we would like to achieve at least the speed up of 2 for the same program. What is the minimum number of processors needed for this speed up?

Q3. Suppose we have the following memory and two private caches of cores 0 and 1 (C0 and C1). Columns from left to right show the cache line (CL), block coherence status (BCS), address, and data for each block. BCS can be in Shared (S), Modified (M) and Invalid (I) state.

Cache: Core 0 (C0)

CL	BCS	Address	Data
0	S	0x20	7
1	I	-	-

Cache: Core 1 (C1)

CL	BCS	Address	Data
0	S	0x20	7
1	S	0x10	3

Address	Data
0x20	7
0x10	3
0x00	0

Shared memory

Using snooping MSI protocol, sketch each private cache with necessary changes (if there is any) after the following memory accesses. You do not need to draw shared memory.

a) Core 1 writes the value 14 to the address 0x20.

Cache: Core 0 (C0)

CL	BCS	Address	Data
0			
1			

Cache: Core 1 (C1)

CL	BCS	Address	Data
0			
1			

b) Core 0 reads from the address 0x10.

Cache: Core 0 (C0)

CL	BCS	Address	Data
0			
1			

Cache: Core 1 (C1)

CL	BCS	Address	Data
0			
1			

c) Core 0 reads from the address 0x20.

Cache: Core 0 (C0)

CL	BCS	Address	Data
0			
1			

Cache: Core 1 (C1)

CL	BCS	Address	Data
0			
1			

d) Core 0 writes the value 6 to the address 0x10.

Cache: Core 0 (C0)

CL	BCS	Address	Data
0			
1			

Cache: Core 1 (C1)

CL	BCS	Address	Data
0			
1			

e) Core 0 writes the value 12 to the address 0x10.

Cache: Core 0 (C0)

CL	BCS	Address	Data
0			
1			

Cache: Core 1 (C1)

CL	BCS	Address	Data
0			
1			

f) Core 1 reads from the address 0x20.

Cache: Core 0 (C0)

CL	BCS	Address	Data
0			
1			

Cache: Core 1 (C1)

CL	BCS	Address	Data
0			
1			

Q4. You are given the following loop, which has dependency between two consecutive iterations. Dependency is on array B. B[i+1] in the current iteration is used as B[i] in the next iteration.

Transform the loop so that each iteration can be executed independently in parallel. Hint: You can move part of the iteration before or after the loop.

```
for (i=0; i<100; i=i+1) {
     A[i] = -B[i];
     B[i+1] = 2C[i];
}
```