Hacettepe University – Computer Engineering Dept.
BBM 231 Logic Design
2018-2019 Fall – MIDTERM II

Date : December 24, 2018 Duration : 120 Minutes

Full Name : Signature:
Student ID : BBM231 Section:

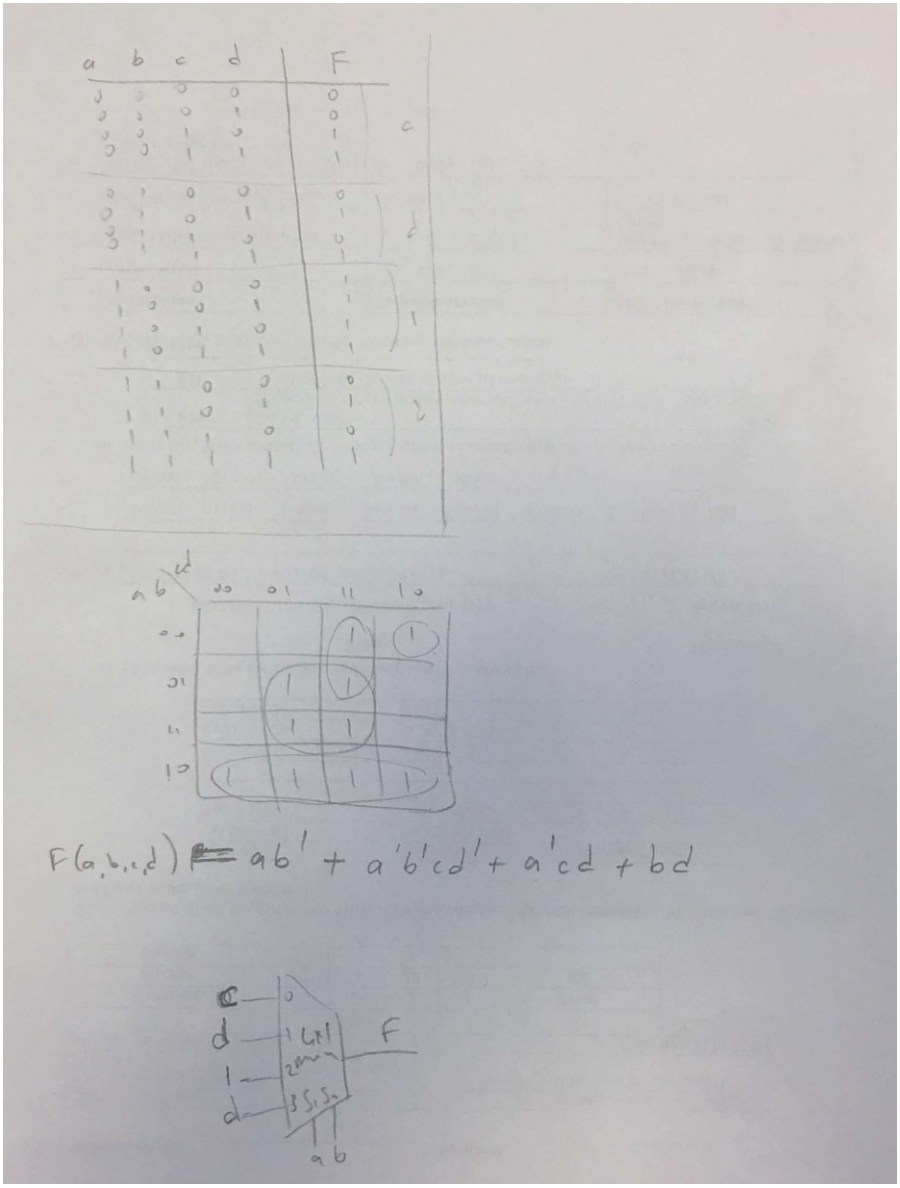
Ques.	1	2	3	4	Total
Points	20	25	35	20	100

Question 1 (20 points):

Implement the following function using nothing but a single 4x1 multiplexer.

F(a,b,c,d) = ab'+a'b'cd'+a'cd+bd

Show your solution in detail for full credit.



Question 2 (25 points):

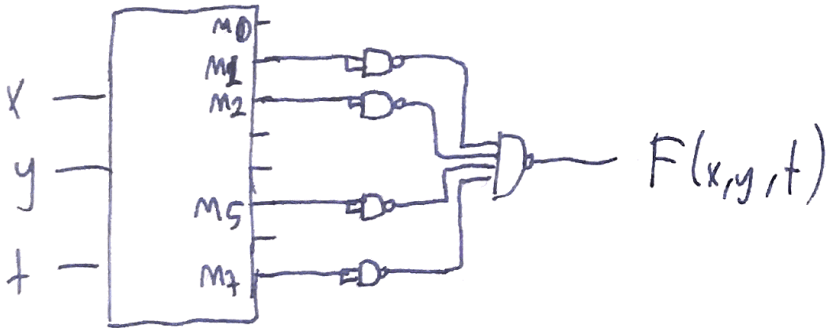
Implement $F(x, y, t) = (x \oplus t)'y + (x'y) \oplus t$ with one 3x8 decoder and NAND gates only. You must minimize the number of NAND gates as much as possible. You may use NAND gates with 2 or more inputs. Show your solution in detail for full credit.

$$F(x,y,t) = (x \oplus t)'y + (x'y) \oplus t$$

$$= (xt + x't')y + x'yt' + (x + y')t$$

$$= xyt + x'yt' + x'yt' + xyt + xy't + xy't + x'y't$$

$$= \Sigma(1, 2, 5, 7)$$



Question 3 (35 points):

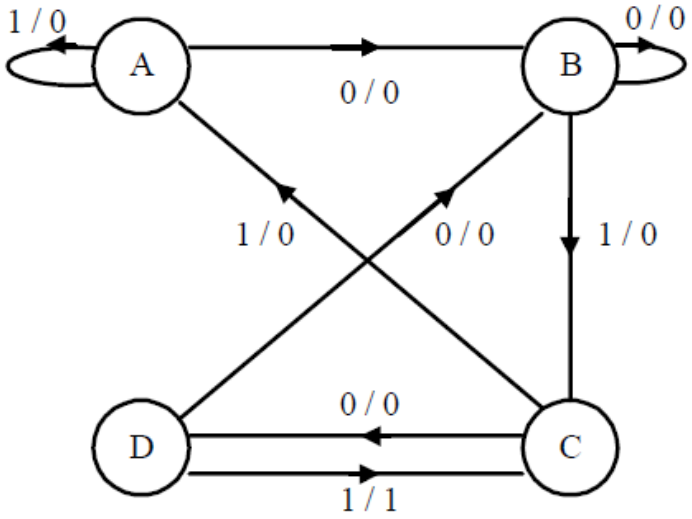
Design a one input one output circuit such that as the input is evaluated at every clock, when the input 0101 is detected, output becomes 1, otherwise it is 0. An example input-output sequence is given below.

Input (x)	0	0	1	0	1	0	1	1	1
Output (z)	0	0	0	0	1	0	1	0	0

In other words, design a Mealy type sequential circuit that detects the sequence 0101 using D-type flip flops and logic gates. Your circuit can have a maximum of 2 D-type flip flops.

a) (10) Draw the state diagram of the circuit
b) (5) Derive the complete state table from the state diagram
c) (10) Using Karnaugh-maps, find the most simplified Boolean expressions for flip-flop outputs and the circuit output
d) (10) Draw the complete circuit

State diagram:



A: Başlangıç durumu
B: 0 gelmiş durumu
C: 01 gelmiş durumu
D: 010 gelmiş durumu

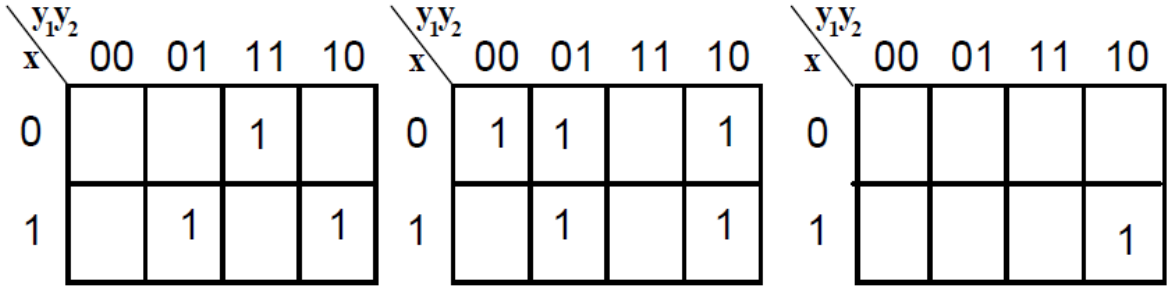
First assignment type:
Let A=00, B=01, C=10, and D=11.
Let y1 and y2 be present state and Y1 and Y2 be next state variables. We can fill the state table as follows:

x	y1	y2	Y1	Y2	z
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	1	1	0	1

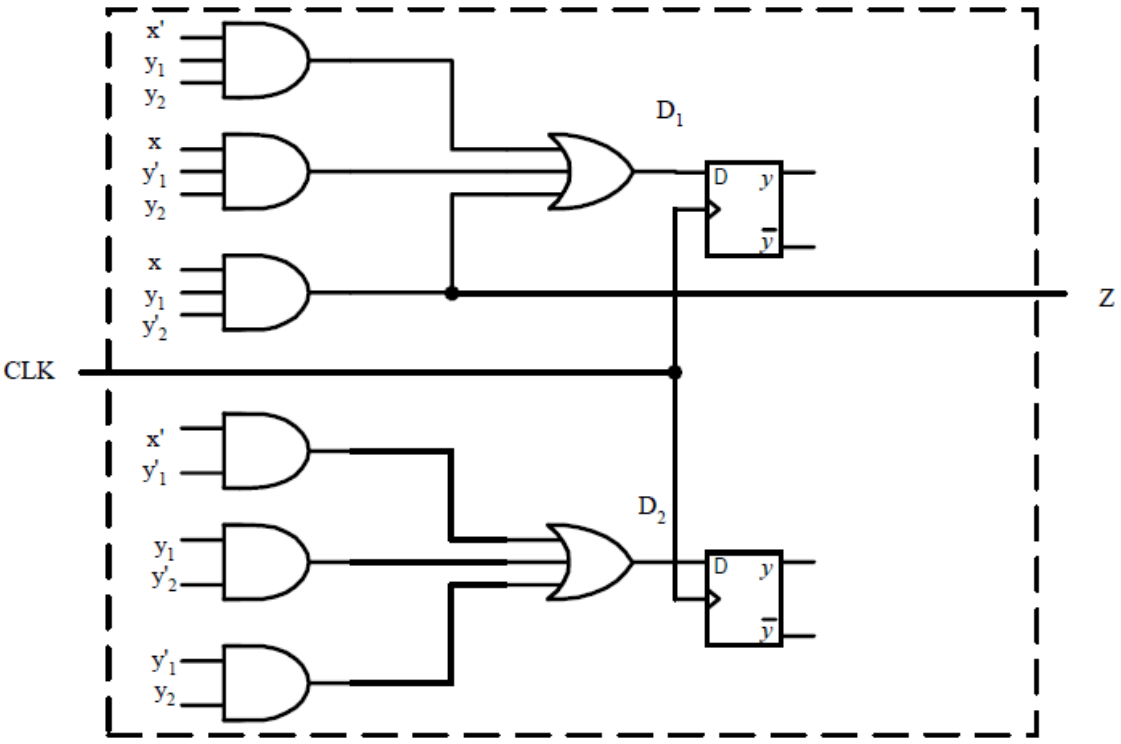
Z = xy1y2
Y1 = xy2 + x'y1y2'
Y2 = x'

Second assignment type:
Let A=00, B=01, C=11, and D=10.
Let y1 and y2 be present state and Y1 and Y2 be next state variables. We can fill the state table as follows:

x	y1	y2	Y1	Y2	z
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

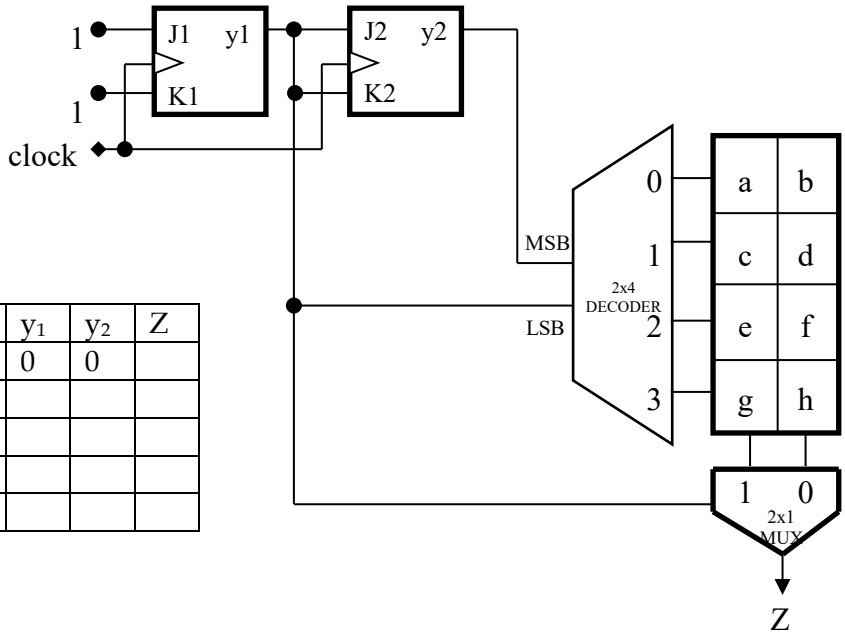


$D_1 = Y_1 = x\,'y_1\,y_2 + x\,y'_1\,y_2 + x\,y_1\,y'_2$ $D_2 = Y_2 = x\,'y'_1 + y'_1\,y_2 + y_1\,y'_2$ $Z = x\,y_1\,y'_2$

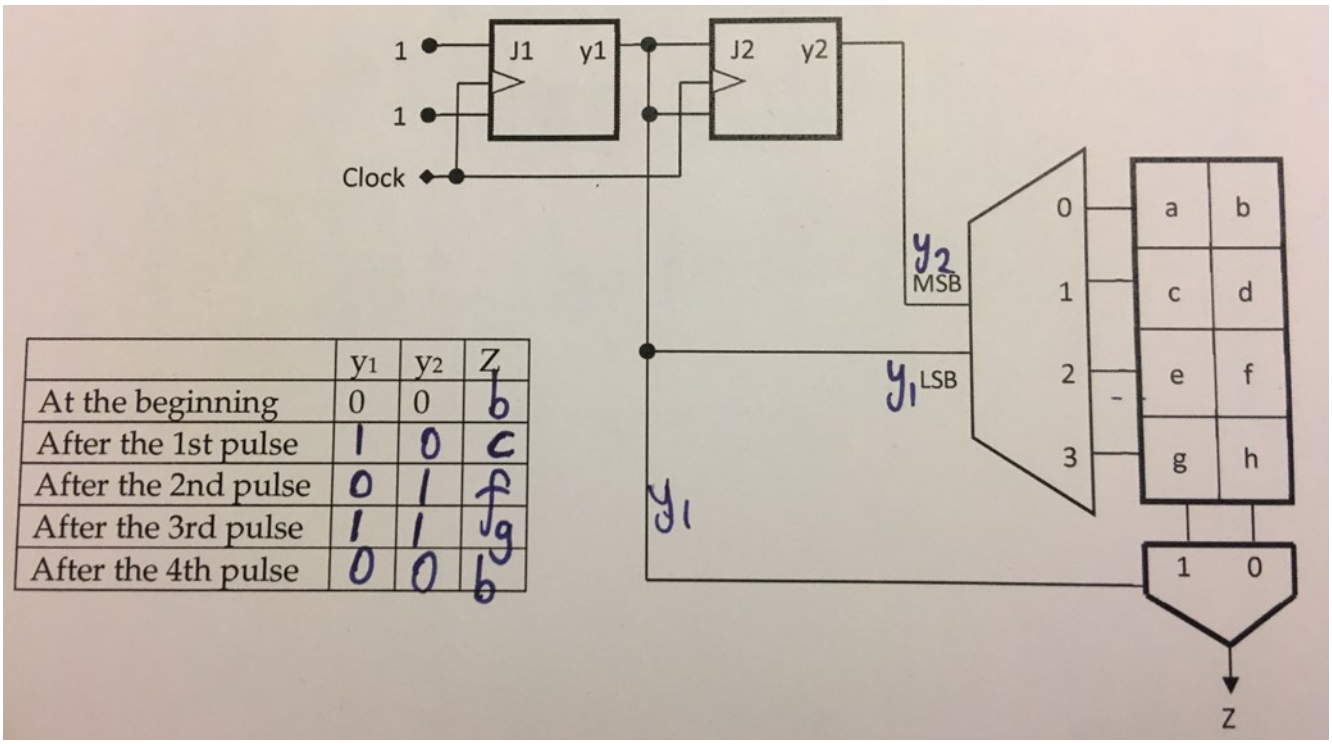


Question 4 (20 points):

For the circuit given below, at the beginning the clock signal is at 0 level and y_1=0, y_2=0. MSB: most significant bit. LSB: least significant bit. A rise of the clock signal to 1 level and a subsequent fall back to 0 level together constitute a **pulse**. Fill the rest of the table below for y_1, y_2 (which can be 0 or 1) and Z output (which can be one of the given 8 letters). Show your solution below the figure in detail for full credit.



	y_1	y_2	Z
At the beginning	0	0	
After the 1st pulse			
After the 2nd pulse			
After the 3rd pulse			
After the 4th pulse			



	y_1	y_2	Z
At the beginning	0	0	b
After the 1st pulse	1	0	c
After the 2nd pulse	0	1	f
After the 3rd pulse	1	1	g
After the 4th pulse	0	0	b