BBM436 Microprocessors Lab.
Fall 2020
Assignment 4
Memory Mapping

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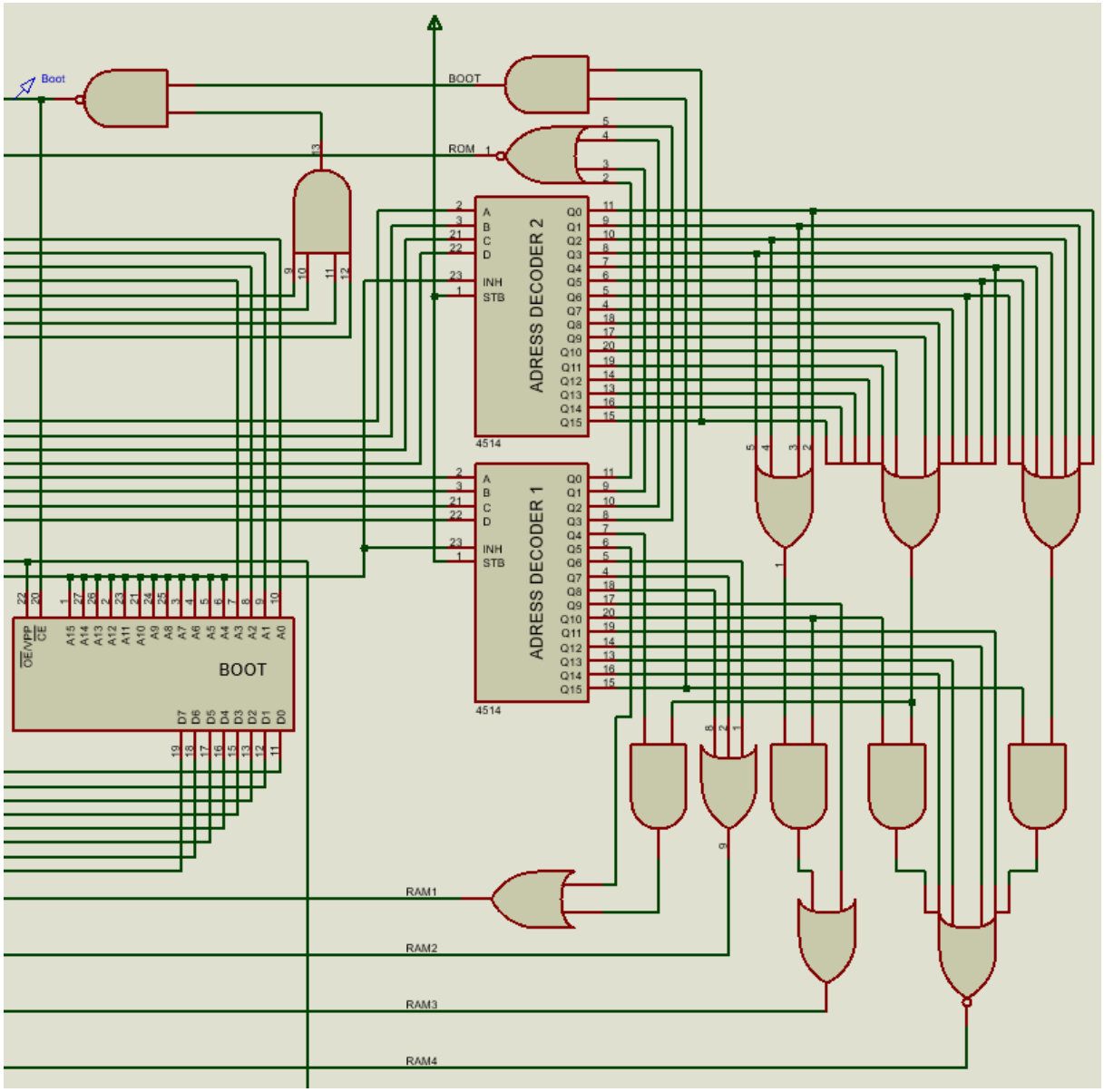
1 Memory address decoding

In this assignment, it is enough to use most significant 8 bits to addressing given memory chips. Thus i used 2 "4x16 decoder"s and a few logic gates for decoding. Firstly, lets make a table:

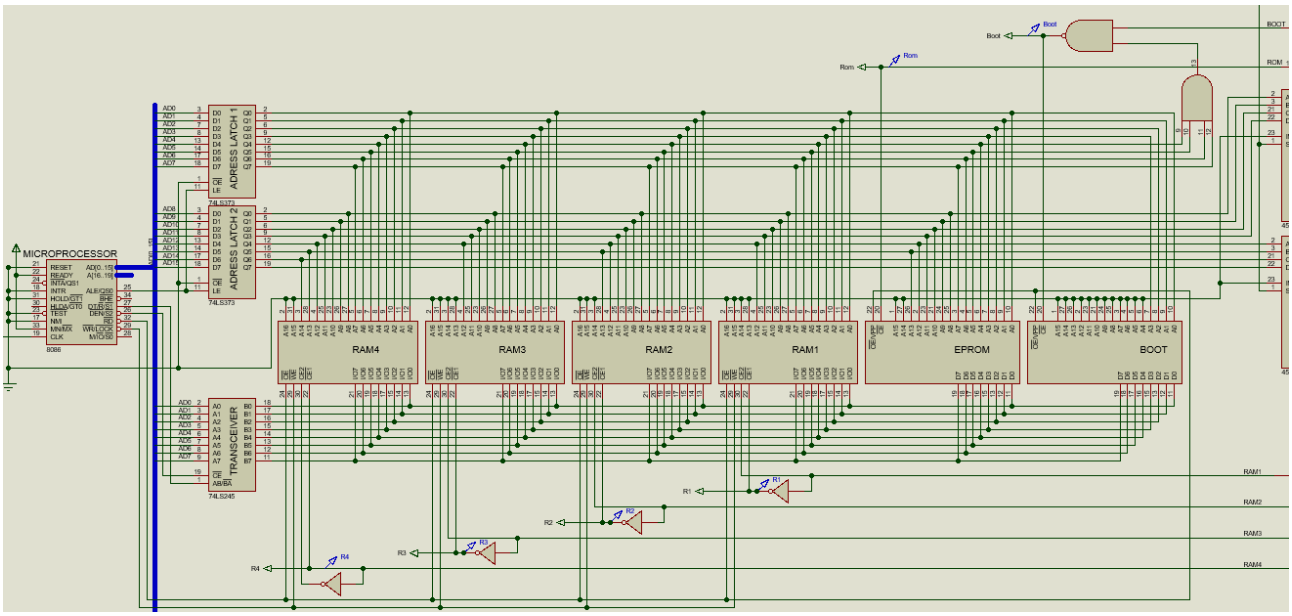
AD[8..15]	**AD[0..7]**	Chip Selection
00XX	XXXX	ROM
0100	00XX	NONE
0100	01XX	RAM1
0100	1XXX	RAM1
0101	XXXX	RAM1
011X	XXXX	RAM2
1000	XXXX	RAM2
1001	XXXX	RAM3
1010	00XX	RAM3
1010	01XX	RAM4
1010	1XXX	RAM4
1011	XXXX	RAM4
110X	XXXX	RAM4
1110	XXXX	RAM4
1111	0XXX	RAM4
1111	1XXX	NONE

We created our table. Now, we must do it with proteus. Figure below is my address decoder design. Also i added one more chip (BOOT) for first instruction fetch on 8086. Address for BOOT chip is 0xFFF0.


Boot
BOOT
ROM
ADRESS DECODER 2
4514
ADRESS DECODER 1
4514
BOOT
RAM1
RAM2
RAM3
RAM4

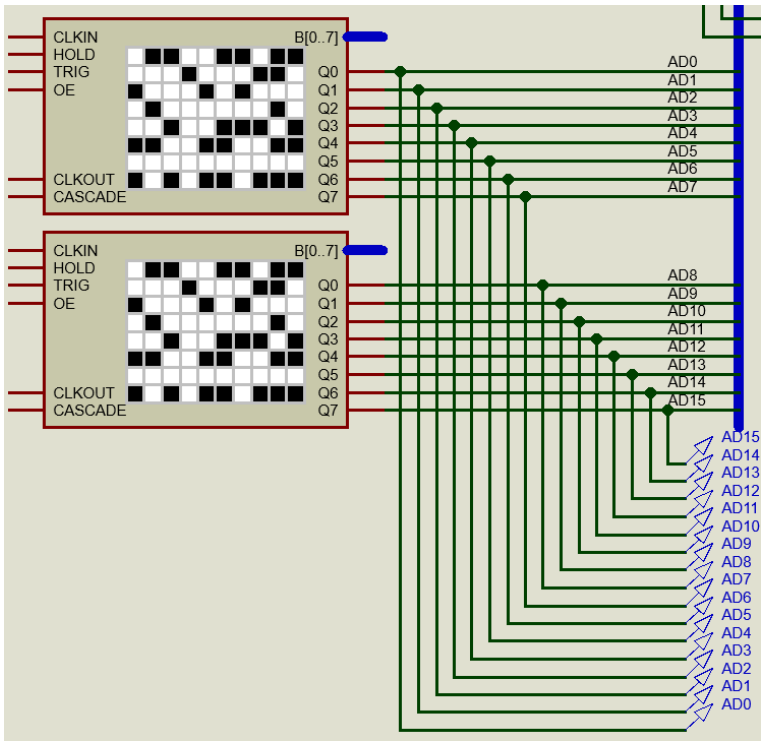
2 Creating system

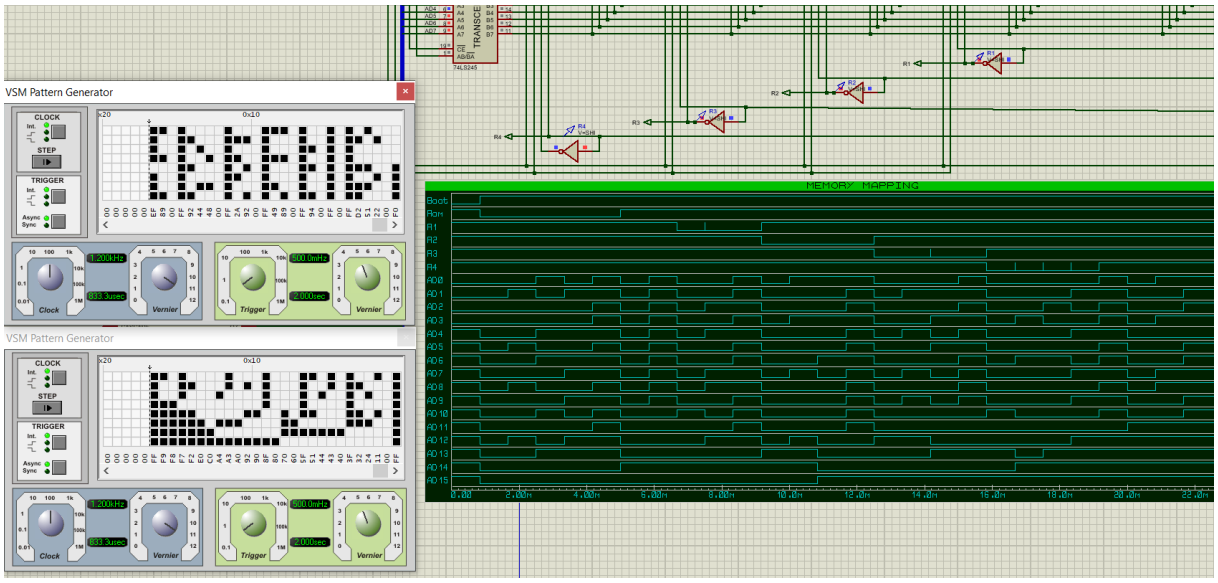
As i said before, i added one more memory chip. So there are 4 RAMs and 2 ROMs in this design. Outputs of address decoders are being chip select signal of these memory chips. Also there are 2 8-bit address latches for 16-bit addressing and there is 1 Transceiver for input-output data. Memory chip's sizes are less than 16 KB. Thus i didnt used some pins on these chips.



3 Logical graph

I used pattern generator for addresses. I couldn't do it with 8086 microprocessor itself. I connected 2 pattern generators for 16-bit addressing. Also used digital analysis graph for logical analysis. This graph takes inputs from probes as you can see near of the pattern generators or chip select units. There are chip select signals and address in this graph. I carefully fill pattern generator to clearly show all memory chips's starting address and ending address. if signal is 1, then this chip is not selected. There are some errors in this graph because of propagation delay of chip select unit (decode).


CLKIN
HOLD
TRIG
OE
CLKOUT
CASCADE
B[0..7]
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15


VSM Pattern Generator
MEMORY MAPPING