Name-Last Name: _____ **Student ID:** _____

Section No (1,2,3?): ____

Hacettepe University	Computer Engineering Department
BBM234 Computer Organization	Instructors: Assoc. Prof. Dr. Suleyman TOSUN Assist. Prof. Dr. Mehmet KOSEOGLU Dr. Hüseyin Temuçin
2nd Midterm Exam	
Duration: 120 minutes	Exam Date: 14.05.2019

Questions	**1**	**2**	**3**	**4**	**5**	**Total**
Marks	**20**	**20**	**20**	**20**	**20**	**100**
Earned						

Q1. You are given the following MIPS code. You have 5 stage pipelined MIPS processor running the code. If there is data hazard unit (data forwarding and early branch resolution hardware) in the MIPS processor, insert enough NOPs between the instructions to have correct execution of the code.

i. How many cycles does it take to execute all instructions if the branch (beq) is not taken?
ii. How many cycles does it take to execute all instructions if the branch (beq) is taken?
Show your calculations or explain how you found the cycle time.

 # MIPS assembly code

```
    lw  $s0, 0($0)

    lw  $s1, 4($0)

    addi $s1, $s1, 1

    beq $s0, $s1, L

    add $t0, $t0, $s0

    add $t1, $t1, $s1

    add $t2, $t0, $t1

L:  addi $t2, $t2, 1
```

Q2. The propogation delay of each stage for a CPU architecture is determined as shown in the table below. The delay of a pipeline register is found as 1ns. ($ns=10^{-9}$)

IF	ID	EX	MEM	WB
7ns	7ns	6ns	9ns	5ns

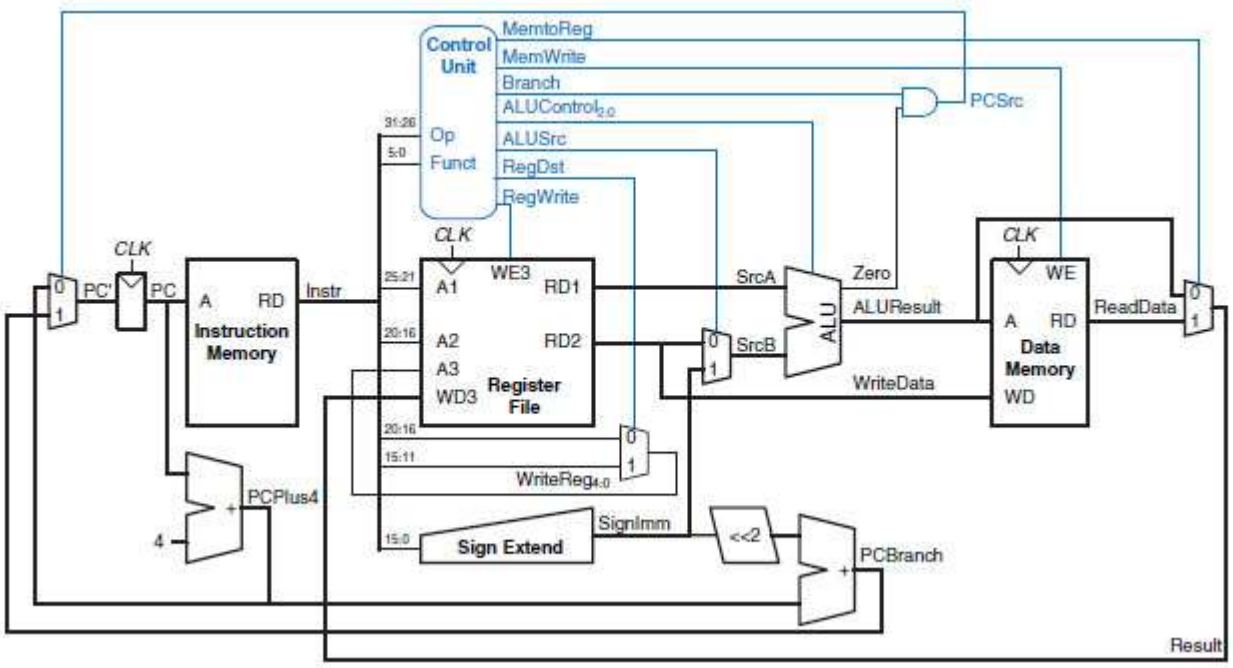
a) If we design a single-cycle processor, what would be the minimum clock cycle in ns?

b) What would be the clock cycle of a 5 stage pipelined processor? Assume register write and read operations take the whole clock cycle, not half of the cycle.

c) We would like to decrease the clock cycle of pipelined processor and we decided to divide one of the stages into two stages. Thus, the new pipelined processor will have 6 stages. Which stage would you divide to two? What would be the new clock cycle?

d) We would like run 1000 instrcutions on above specified processors. Assume there is no data and control hazards. What are the CPU times of these 1000 instruction on these three processors?

Q3. A single cycle microprocessor design is given below



a. Fill in the control bit table below, for the `addi $t1, 1000` command

MemtoReg	MemtoWrite	Branch	ALUControl	ALUSrc	RegDst	RegWrite

b. Fill in the control bit table below, for the `or $t1, $t2` command

MemtoReg	MemtoWrite	Branch	ALUControl	ALUSrc	RegDst	RegWrite

Q4. Benchmark values and Command dependency assumptions for a 5-starge pipelined MIPS processor is given.

- Benchmark:
  - 30% loads
  - 20% stores
  - 10% branches
  - 6% jumps
  - 34% R-type
- Assumptions:
  - 35% of loads used by next instruction
  - 20% of branches mispredicted
  - All jumps flush next instruction

a. What is CPI value for lw command ?

$CPI_{lw} =$

b. What is the average CPI ?

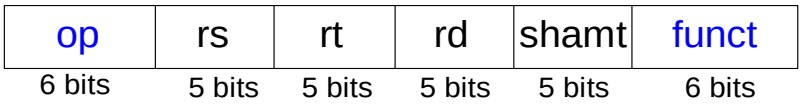
$CPI_{avg} =$

Q5.

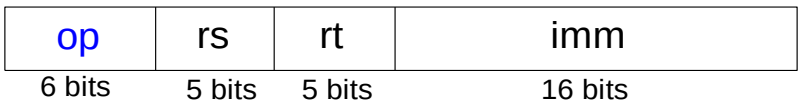
Good Luck ☺

MIPS CODE TYPES

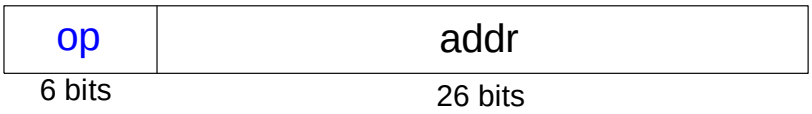
R-Type



I-Type



J-Type



ALU OPS

ALU	**Op Meaning**
00	Add
01	Substract
10	Look at funct field
11	n/a