Hacettepe University
Department of Computer Engineering
Advanced Computer Architecture Course
Homework 2

Assigned date: 06.12.2018
Due date: 13.12.2018

Answer the following questions and hand in your homework in class.

QUESTIONS

Q1: You are given a MIPS program below:

a) How many clock cycles does this program take to finish its execution on a 5-stage pipelined MIPS processor? Suppose the processor has data forwarding and early branch prediction (data hazard unit).[10]

```
        add $s0, $0, $0
        add $s1, $0, $0
        addi $t0, $0, 10
loop:   slt $t1, $s0, $t0
        beq $t1, $0, done
        add $s1, $s1, $s0
        addi $s0, $s0, 1
        j loop
done:   jr $ra
```

b) Unroll the program two times. How many cycles does it take now? [15]

Q2: We will compare some branch prediction methods by using the following MIPS code:

```
...
int i=0;
int a=2;
for (i=0, i<5, i++){
        if(i==a)
            a=0;
}
...
```

a) If we use a static branch predictor that predicts as always "branch taken (BT)", how many predictions will be correct? Show in the following table. (BT=Branch Taken, BNT=Branch Not Taken) [7]

Branch	For (i=0)	İf	For (i=1)	İf	For (i=2)	İf	For (i=3)	İf	For (i=4)	if	For (i=5)	Total
Result	BT	BNT										
Prediction												

b) Answer the same question for the branch predictor that predicts as always "branch not taken (BNT)". [6]

Branch	For (i=0)	İf	For (i=1)	İf	For (i=2)	İf	For (i=3)	İf	For (i=4)	if	For (i=5)	Total
Prediction												

c) Answer the same question for "1-bit branch predictor". Suppose initial state is BT. [6]

Branch	For (i=0)	İf	For (i=1)	İf	For (i=2)	İf	For (i=3)	İf	For (i=4)	if	For (i=5)	Total
Result												
Prediction												

d) Answer the same question for "2-bit branch predictor". Suppose initial state is BT. [6]

Branch	For (i=0)	İf	For (i=1)	İf	For (i=2)	İf	For (i=3)	İf	For (i=4)	if	For (i=5)	Total
Result												
Prediction												

Q3. The EX (Execute) clock cycles for a specific architecture is given in the following table.

Functional Unit	EX Clock Cycles
Integer ALU	1
Floating Point Add	4

a) For the following code segment, write the start and end times for each instruction for scoreboard and tomasulo. [15]

Instruction	Scoreboard		Tomasulo	
	Start	Finish	Start	Finish
LD F0, 0(R5)				
LD F2, 0(R6)				
ADDD F4, F0, F2				
SUBBD F6, F8, F10				
SD F4, 0(R5)				
SD F6, 0(R6)				

b) If there are any differences between two methods, write the reasons by explaining the main differences of these two methods. [10]

Q4:

a) What are the data hazard types that can be seen in out-of-order execution architectures? [5]

b) In the following table, you have the execution cycles for each instruction type in a 5-stage MIPS processor. Assume there is no forwarding in the architecture and it is in-order-fetch machine.

Functional Unit	EX Clock Cycles
Integer ALU	1
Floating Point Add	5
Floating/Point Load Store	2
Floating Point Multiply	3

What type of hazards can happen in the following code segment? Show them by listing the instructions that cause the hazards, the register names and type of the hazard. [10]

1: SUBF F1, F2, F3

2: ADDF F1, F4, F5

3: MULTF F6, F3, F1

4: SF F6, 100(R1)

5: LF F1, 0(R1)

6: ADDF F2, F1, F6

c) How many NOPS are necessary between instructions to remove hazards? Write them below. How many cycles does this code take to finish its execution now? [10]

SUBF F1, F2, F3

ADDF F1, F4, F5

MULTF F6, F3, F1

SF F6, 100(R1)

LF F1, 0(R1)

ADDF F2, F1, F6