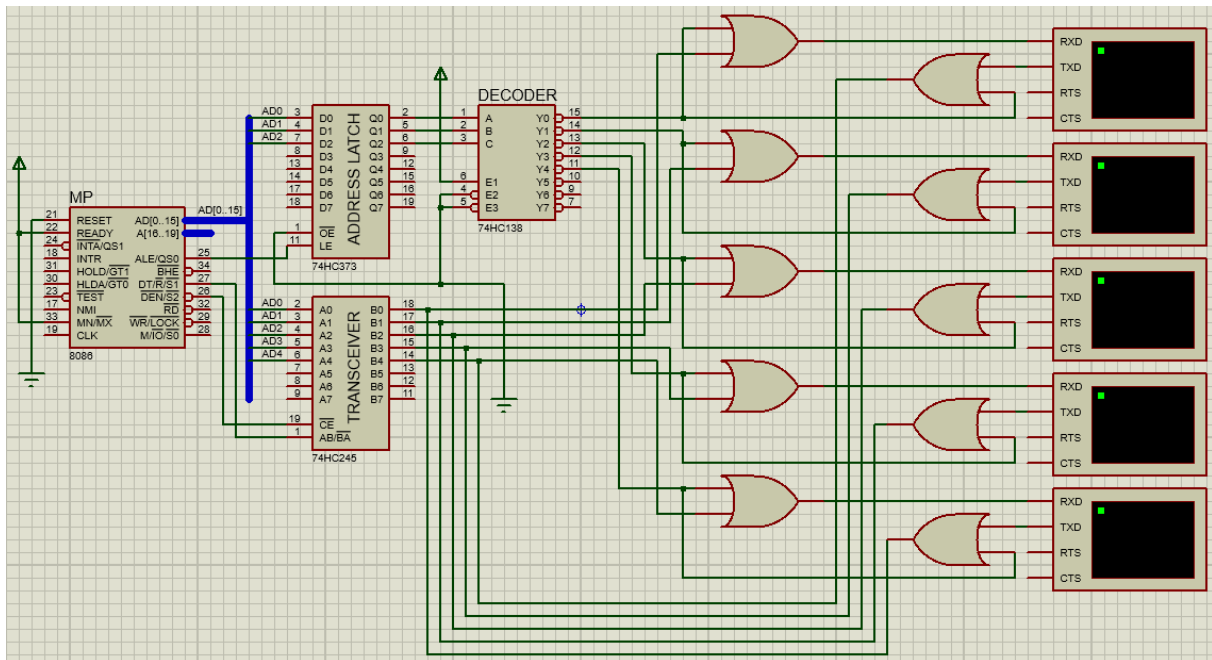


1-



I used address latch and decoder for mapping these terminals. I store address of target terminal in address latch. Then, decoding it. For example, 02H address for 3rd terminal. I used OR Gates as "Chip Enable". If a terminal is selected, then output of OR gate is data comes from transceiver/terminal. If a terminal is not selected, then output will be always 1(IDLE).

2-

START:

Microprocessor scans fastly to take an input.

(HW5)

If a terminal changes its state from IDLE,

(HW6-HW7)

then Microprocessor gets input by bit banging with interrupt.

(HW6-HW7)

Process this input, determines target terminal and its address.

(HW4)

Sends this data to target terminal with bit banging again.

(HW6-HW7)

Jump to START.

3-

Two terminals can be produce a output at the same time. So i need to scan while taking input too (Instead of delay subroutine, we can scan at this time.).

Instead of OR Gates, we can use small transceivers. OR gates blocks enabling two different chips.

For long transmissions, we can use synchronous communication.

4-

Adding transceivers instead of OR gates.

Synchronous communication instead of Asynchronous communication.

Instead of octal latches/transceivers, we can use smaller like 3to3 address latch / 5to5 transceivers.

