HACETTEPE UNIVERSITY
DEPARTMENT OF COMPUTER ENGINEERING
BBM436 MICROPROCESSORS LAB.
Assoc. Prof. Dr. Harun ARTUNER,
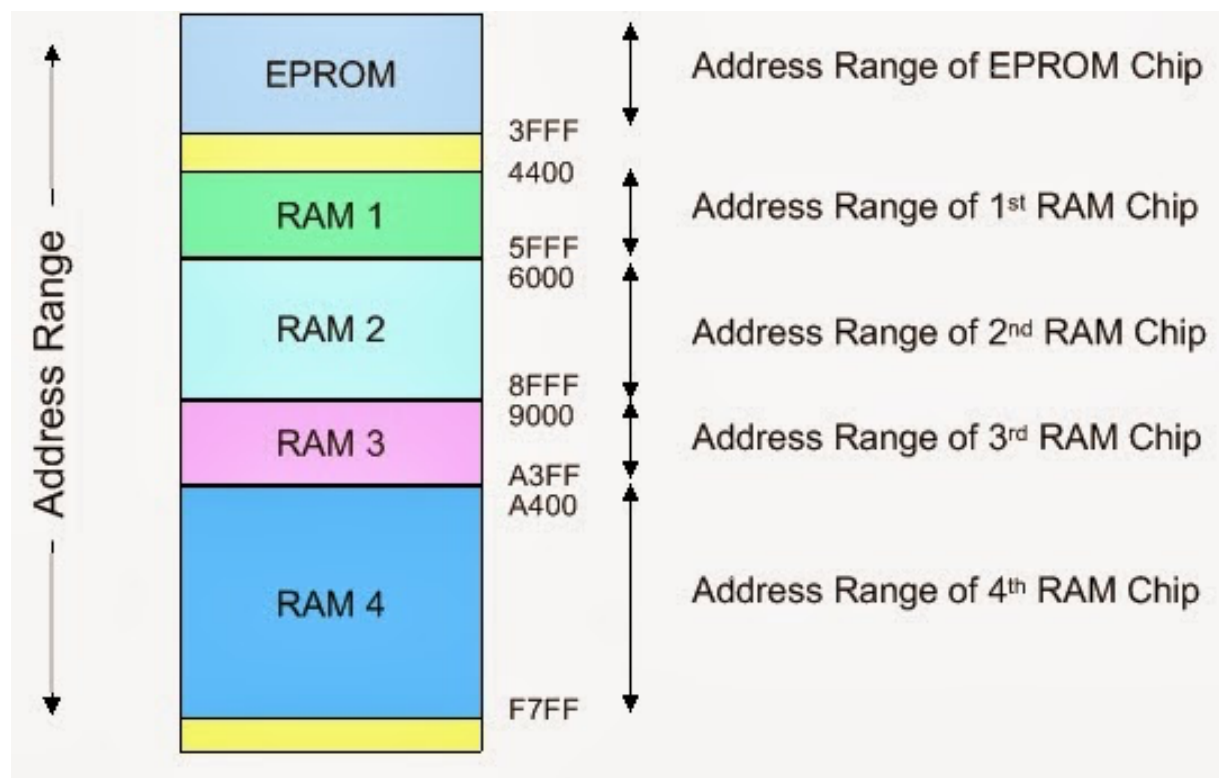Ali Osman SERHATOGLU, Burcu YALÇINER
17.11.2020

ASSIGNMENT 4

Topic

Submit your work file by attaching it to your report.

Phase 1
Perform the address map given below for the memory units you used in previous studies. Implement the necessary address decoding circuits on the proteus for this.

Phase 2
Create the necessary prerequisites for the system to work. Provide these in detail in your report.

Phase 3
Again, Draw the time plot of the address, data and control paths on the virtual logic analyzer in a setup.