Hacettepe University	Computer Engineering Department
BBM234 Computer Organization	Instructors: Suleyman TOSUN, Mehmet KOSEOGLU
Final Exam	
Duration: 90 minutes	Exam Date: 26.06.2020

Each question is 25 points.

Either print this page and write on them or write your solutions on a seperate sheets. Make it a single pdf. Submit your pdf 14:55. No late submissions will be accepted.

Q1.

a. Suppose the last digit of your student id is k. Write the register values in decimal after executing the following code. Draw the same table (all three rows). Fill only the second row.

```
        addi $t0, $0, k
        sll $t1, $t0, 2
        addi $t2, $0, 9
        addi $t3, $0, 2
        mult $t2, $t3
        mflo $t4
        slt $t5, $t1, $t4
        bne $t5, $0, skip
        addi $t6, $0, 1881
        add $t7, $t0, $t0
        j next
skip:   addi $t6, $0, 1938
        addi $t7, $t0, 1
next:   jr $ra
```

Register	**t0**	**t1**	**t2**	**t3**	**t4**	**t5**	**t6**	**t7**
Value								
Points	*1*	*3*	*1*	*1*	*3*	*3*	*5*	*3*

b. *(5 pts)* Bne instruction is an I-Type MIPS instruction. What is the value of its immediate part in its machine code? Write in hexadecimal.

opcode	**rs**	**rt**	**immediate**
bne	t5	0	???

Q2. A cache has the following parameters: *b*, block size given in numbers of words; *S*, number of sets; *N*, number of ways; and *A=32*, number of address bits. LRU replacement is used.

You are given the following MIPS code with the lw addresses given in hexadecimal. Suppose C=8 words and b=1 word. Assume the cache is initially empty. Answer the following questions.

For all questions, show where the addresses 0x24, 0x44, 0x20, and 0x40 are mapped on the figures.

```
# MIPS assembly code
        addi $t0, $0, 2
loop:   beq  $t0, $0, done
        lw   $t1, 0x24($0)
        lw   $t2, 0x44($0)
        lw   $t3, 0x20($0)
        lw   $t3, 0x40($0)
        addi $t0, $t0, -1
        j    loop
done:
```

a) *(1 pts)* How many data memory accesses (lw) do we have?

b) *(6pts)* If N=1 (direct mapped), what is the miss rate?

	Set 7 (111)
	Set 6 (110)
	Set 5 (101)
	Set 4 (100)
	Set 3 (011)
	Set 2 (010)
	Set 1 (001)
	Set 0 (000)

Miss Rate= ?

b) *(6pts)*If N=2, what is the miss rate

Way 1	Way 0	
		Set 3 (11)
		Set 2 (10)
		Set 1 (01)
		Set 0 (00)

Miss Rate=?

c) *(6pts)* If N=1 and b=2, what is the miss rate?

Block 1	Block 0	
		Set 3 (11)
		Set 2 (10)
		Set 1 (01)
		Set 0 (00)

Miss Rate= ?

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d) *(6pts)* If N=2 and b=2, what is the miss rate?

Way 1		Way 0		
Block 1	Block 0	Block 1	Block 0	
				Set 1 (1)
				Set 0 (0)

Miss Rate=

Q3. You are given the first 10 lines of page table, which is stored in the main memory. The page size is 4KB. Let the last digit of your student ID number is k.

a) (0 points) What is the last digit of your student ID number, k=_____

b) (15 points) Find the physical address corresponding to virtual address 0xkkkk.

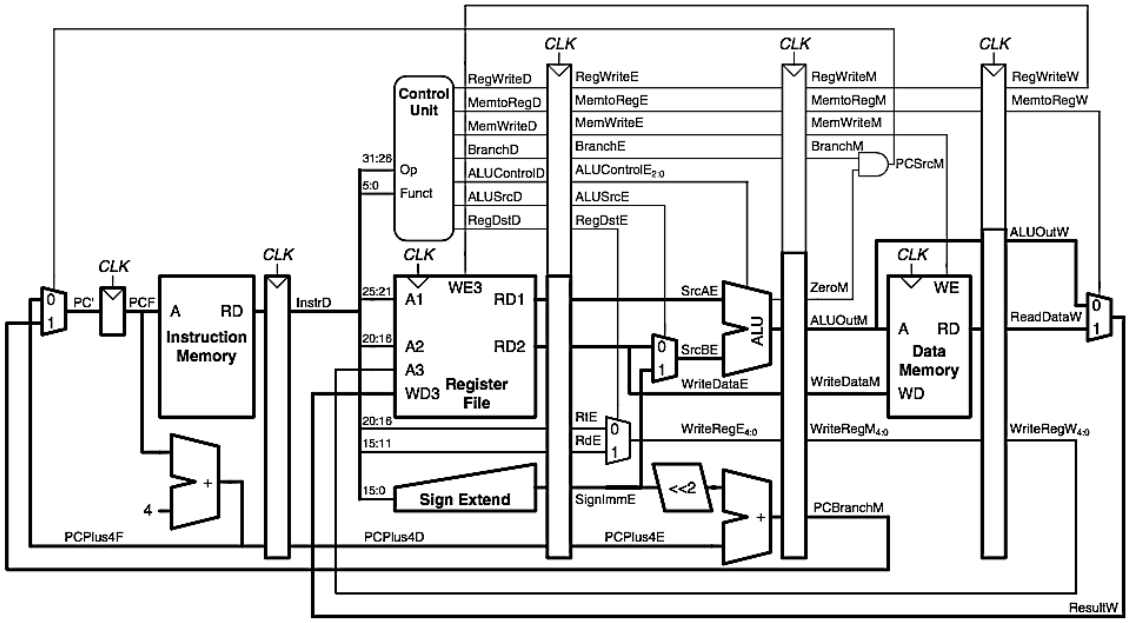
V	Physical Page Number (PPN)	Virtual Page Number (VPN)
.	..	..
1	0x18BC	9
1	0x46DE	8
1	0x94DE	7
1	0x63AB	6
1	0x52BC	5
1	0x61AB	4
1	0x90DE	3
1	0x40DE	2
1	0x10BC	1
1	0x00EF	0

c) (10 points) Assume the access time to TLB is 1cc and 10cc to main memory. Assume there is **no cache** in the architecture. Assume that we have a fully-associative 2-entry TLB. The TLB is initially empty.

Suppose the CPU accesses to the following virtual addresses in the given order:
0x04k, 0x08k, 0x0Ck, 0x202k, 0x202k.

What is the total access time (cc)?

Q4.



a) (0 points) What is the last digit of your student ID number, k=_____

b) (25 points) The MIPS program below is executed on the pipelined architecture given above. Replace k with the last digit of your student number. $tk indicates the temporary register k. For example, if the last digit of your ID number is k=5, $tk corresponds to $t5. Assume we have a forwarding unit in place, so the value written to tk by the `add` instruction is available to the `and` instruction. What are the values of the following signals?

Signal	Value
InstrD[20:16]	
MemWriteM	
ALUOutM	
ResultW	
WriteRegW	

MIPS program:

```
addi $t1, $0, k
add $tk, $t1, $t1 (Writeback)
and $s4, $tk, $tk (Memory)
sub $s5, $t2, $t3 (Execute)
sw  $s6, 20($tk) (Decode)
or  $s7, $t3, $t4 (Fetch)
```