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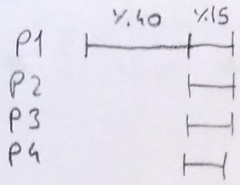
Q1-

Class	Level of Parallelism	Example Architecture
Single Instruction Single Data	Instruction level parallelism	Single processor. (MIPS)
Single Instruction Multiple Data	Data level parallelism	GPU (VMIPS)
Multiple Instruction Multiple Data	Thread level parallelism	Multi core processors. (Pentium)

Q2-

a)



$$speedup = \frac{1}{(1-0,6)+\left(\frac{0,6}{4}\right)} = \frac{1}{0,55} = 1,\overline{81}$$

b) $speedup = 2 = \frac{1}{0,5} = \frac{1}{(1-0,6)+\left(\frac{0,6}{x}\right)}$ $x = 6$ We need 6 processors.

Q3-

a)

CL	BCS	Address	Data
0	I	0x20	7
1	I	-	-

CL	BCS	Address	Data
0	M	0x20	14
1	S	0x10	3

Cache hit.
Write to cache.
Invalidate others.

Core 1 writes the value 14 to the address 0x20.

b)

CL	BCS	Address	Data
0	I	0x20	7
1	S	0x10	3

CL	BCS	Address	Data
0	M	0x20	14
1	S	0x10	3

Private cache not hit,
Fetch from shared memory.

Core 0 reads from the address 0x10.

c)

CL	BCS	Address	Data
0	S	0x20	14
1	S	0x10	3

CL	BCS	Address	Data
0	S	0x20	14
1	S	0x10	3

Cache hit but invalidated.
Fetch from others via BUS.

Core 0 reads from the address 0x20.

d)

CL	BCS	Address	Data
0	S	0x20	14
1	M	0x10	6

CL	BCS	Address	Data
0	S	0x20	14
1	I	0x10	3

Cache hit.
Write to cache.
Invalidate others.

Core 0 writes the value 6 to address 0x10.

e)

CL	BCS	Address	Data
0	S	0x20	14
1	M	0x10	12

CL	BCS	Address	Data
0	S	0x20	14
1	I	0x10	3

Cache hit
Write to cache
Invalidate others.

Core 0 writes the value 12 to the address 0x10.

f)

CL	BCS	Address	Data
0	S	0x20	14
1	M	0x10	12

CL	BCS	Address	Data
0	S	0x20	14
1	I	0x10	3

Cache hit.
Read from cache.

Core 1 reads from the address 0x20.

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Q 4-

```
A[0] = - B[0];
for (i=0; i<99; i=i+1) {
    B[i+1] = 2 * C[i];
    A[i+1] = - B[i+1];
}
B[100] = 2 * C[99];
```