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Q3-

```
        movl %edi, 3410H        ; I will store values here.
        movl %eax, 0            ; first element.
        movl [%edi], %eax       ; save first element
        movl %eax, 1            ; second element.
        addl %edi, 4            ; 32 bit = 4 byte
        movl [%edi], %eax       ; save second element
        movl %ecx, 341          ; iterate it 341 times.
Loop:   movl %eax, [%edi -4]    ; move (i-2)th element to ith element.
        addl %eax, [%edi]       ; add (i-2)th element and (i-1)th element
                                  move to ith element.
        addl %edi, 4            ; update address
        movl [%edi], %eax       ; save ith value to ith address.
        loop Loop               ; loop it 341 times (depends on ecx reg.)
```

Q4 - Let's say we iterate this loop n times.

In first iteration, there will be read miss. So cache fetches 4 values (16/4).

Then, second read will be hit and write will be also hit.

In second iteration, everything will be hit.

In third iteration, reads will be hit, but write will be miss. Thus cache will fetch another 4 values.

So, in every 3 iterations, cache will be refreshed.

1 read miss + 1 read hit + 1 write hit + 2 read hit + 1 write hit + 2 read hit + 1 write miss.

= 5 read hit 1 read miss + 2 write hit 1 write miss. = 7 hits 2 misses

Let say n=100, then 233 hit and 67 miss will be occurred.

% 77 hit rate.