# K4F661611C, K4F641611C

# CMOS DRAM

## 4M x 16bit CMOS Dynamic RAM with Fast Page Mode

## DESCRIPTION

This is a family of 4,194,304 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time ( -50 or -60) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. This 4Mx16 Fast Page Mode DRAM family is fabricated using Samsung′s advanced CMOS process to realize high band-width, low power consumption and high reliability.

## FEATURES

- **Part Identification**

  - K4F661611C-TC(5.0V, 8K Ref.)
  - K4F641611C-TC(5.0V, 4K Ref.)

- **Active Power Dissipation**

  Unit : mW

  | Speed | 8K | 4K |
  |-------|-----|-----|
  | -50 | 495 | 660 |
  | -60 | 440 | 605 |

- **Refresh Cycles**

  | Part NO. | Refresh cycle | Refresh time Normal |
  |----------|---------------|---------------------|
  | K4F661611C* | 8K | 64ms |
  | K4F641611C | 4K | 64ms |

  * Access mode & $\overline{RAS}$ only refresh mode
    : 8K cycle/64ms
  $\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
    : 4K cycle/64ms

- **Performance Range**

  | Speed | $t_{RAC}$ | $t_{CAC}$ | $t_{RC}$ | $t_{PC}$ |
  |-------|-----------|-----------|----------|----------|
  | -50 | 50ns | 13ns | 90ns | 35ns |
  | -60 | 60ns | 15ns | 110ns | 40ns |

- Fast Page Mode operation
- 2$\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL(5.0V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
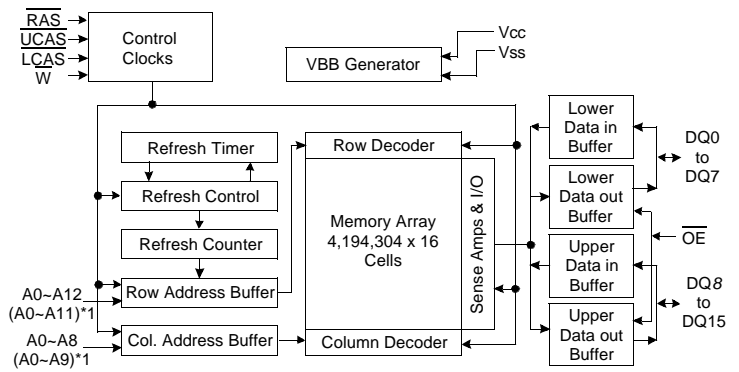- Available in Plastic TSOP(II) package
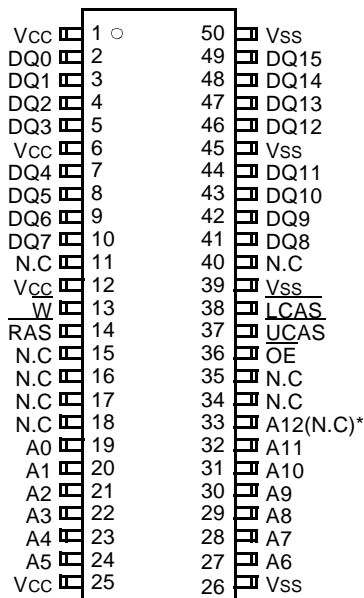- +5.0V±10% power supply

## FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

**SAMSUNG ELECTRONICS CO., LTD.** reserves the right to change products and specifications without notice.

## PIN CONFIGURATION   (Top Views)

• **K4F661611C-T**
• **K4F641611C-T**

```
        Vcc  1 ○      50   Vss
        DQ0  2         49   DQ15
        DQ1  3         48   DQ14
        DQ2  4         47   DQ13
        DQ3  5         46   DQ12
        Vcc  6         45   Vss
        DQ4  7         44   DQ11
        DQ5  8         43   DQ10
        DQ6  9         42   DQ9
        DQ7  10        41   DQ8
        N.C  11        40   N.C
        Vcc  12        39   Vss
          W  13        38   LCAS
        RAS  14        37   UCAS
        N.C  15        36   OE
        N.C  16        35   N.C
        N.C  17        34   N.C
        N.C  18        33   A12(N.C)*
         A0  19        32   A11
         A1  20        31   A10
         A2  21        30   A9
         A3  22        29   A8
         A4  23        28   A7
         A5  24        27   A6
        Vcc  25        26   Vss
```

(400mil TSOP(II))

*(N.C) : N.C for 4K Refresh Product

| Pin Name | Pin function |
|----------|--------------|
| A0 - A12 | Address Inputs(8K Product) |
| A0 - A11 | Address Inputs(4K Product) |
| DQ0 - 15 | Data In/Out |
| Vss | Ground |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{UCAS}$ | Upper Column Address Strobe |
| $\overline{LCAS}$ | Lower Column Address Strobe |
| $\overline{W}$ | Read/Write Input |
| $\overline{OE}$ | Data Output Enable |
| Vcc | Power(+5.0V) |
| N.C | No Connection |

### ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}, V_{OUT}$ | -1.0 to +7.0 | V |
| Voltage on Vcc supply relative to Vss | $V_{CC}$ | -1.0 to +7.0 | V |
| Storage Temperature | Tstg | -55 to +150 | °C |
| Power Dissipation | $P_D$ | 1 | W |
| Short Circuit Output Current | $I_{OS}$ Address | 50 | mA |

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, $T_A$= 0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.6 | - | $V_{CC}$+1.0[*1] | V |
| Input Low Voltage | $V_{IL}$ | -1.0[*2] | - | 0.7 | V |

*1 : $V_{CC}$+2.0V at pulse width≤20ns which is measured at $V_{CC}$

*2 : -2.0 at pulse width≤20ns which is measured at $V_{SS}$

### DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input Leakage Current (Any input 0≤$V_{IN}$≤$V_{CC}$+0.5V, all other pins not under test=0 Volt) | $I_{I(L)}$ | -5 | 5 | uA |
| Output Leakage Current (Data out is disabled, 0V≤$V_{OUT}$≤$V_{CC}$) | $I_{O(L)}$ | -5 | 5 | uA |
| Output High Voltage Level($I_{OH}$=-5mA) | $V_{OH}$ | 2.4 | - | V |
| Output Low Voltage Level($I_{OL}$=4.2mA) | $V_{OL}$ | - | 0.4 | V |

## DC AND OPERATING CHARACTERISTICS (Continued)

| Symbol | Power | Speed | Max | | Units |
|--------|-------|-------|------|------|-------|
| | | | K4F661611C | K4F641611C | |
| $I_{CC1}$ | Don't care | -50<br>-60 | 90<br>80 | 120<br>110 | mA<br>mA |
| $I_{CC2}$ | Normal | Don't care | 2 | 2 | mA |
| $I_{CC3}$ | Don't care | -50<br>-60 | 90<br>80 | 120<br>110 | mA<br>mA |
| $I_{CC4}$ | Don't care | -50<br>-60 | 60<br>50 | 70<br>60 | mA<br>mA |
| $I_{CC5}$ | Normal | Don't care | 1 | 1 | mA |
| $I_{CC6}$ | Don't care | -50<br>-60 | 120<br>110 | 120<br>110 | mA<br>mA |

$I_{CC1}$* : Operating Current ($\overline{RAS}$ and $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @$t_{RC}$=min.)

$I_{CC2}$ : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=$V_{IH}$)

$I_{CC3}$* : $\overline{RAS}$-only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=$V_{IH}$, $\overline{RAS}$, Address cycling @$t_{RC}$=min.)

$I_{CC4}$* : Fast Page Mode Current ($\overline{RAS}$=$V_{IL}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @$t_{PC}$=min.)

$I_{CC5}$ : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=$V_{CC}$-0.2V)

$I_{CC6}$* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{UCAS}$ or $\overline{LCAS}$ cycling @$t_{RC}$=min)

**\*Note :** $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ are dependent on output loading and cycle rates. Specified values are obtained with the output open. $I_{CC}$ is specified as an average current. In $I_{CC1}$, $I_{CC3}$ and $I_{CC6}$, address can be changed maximum once while $\overline{RAS}$=$V_{IL}$. In $I_{CC4}$, address can be changed maximum once within one fast page mode cycle time, $t_{PC}$.

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## CAPACITANCE (T$_A$=25°C, V$_{CC}$=5.0V, f=1MHz)

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input capacitance [A0 ~ A12] | C$_{IN1}$ | - | 5 | pF |
| Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$] | C$_{IN2}$ | - | 7 | pF |
| Output capacitance [DQ0 - DQ15] | C$_{DQ}$ | - | 7 | pF |

## AC CHARACTERISTICS (0°C≤T$_A$≤70°C, See note 1,2)

Test condition : V$_{CC}$=5.0V±10%, Vih/Vil=2.6/0.7V, Voh/Vol=2.4/0.6V

| Parameter | Symbol | -50 Min | -50 Max | -60 Min | -60 Max | Units | Note |
|---|---|---|---|---|---|---|---|
| Random read or write cycle time | t$_{RC}$ | 90 | | 110 | | ns | |
| Read-modify-write cycle time | t$_{RWC}$ | 133 | | 153 | | ns | |
| Access time from $\overline{RAS}$ | t$_{RAC}$ | | 50 | | 60 | ns | 3,4,10 |
| Access time from $\overline{CAS}$ | t$_{CAC}$ | | 13 | | 15 | ns | 3,4,5 |
| Access time from column address | t$_{AA}$ | | 25 | | 30 | ns | 3,10 |
| $\overline{CAS}$ to output in Low-Z | t$_{CLZ}$ | 0 | | 0 | | ns | 3 |
| Output buffer turn-off delay | t$_{OFF}$ | 0 | 13 | 0 | 13 | ns | 6 |
| Transition time (rise and fall) | t$_T$ | 1 | 50 | 1 | 50 | ns | 2 |
| $\overline{RAS}$ precharge time | t$_{RP}$ | 30 | | 40 | | ns | |
| $\overline{RAS}$ pulse width | t$_{RAS}$ | 50 | 10K | 60 | 10K | ns | |
| $\overline{RAS}$ hold time | t$_{RSH}$ | 13 | | 15 | | ns | |
| $\overline{CAS}$ hold time | t$_{CSH}$ | 50 | | 60 | | ns | |
| $\overline{CAS}$ pulse width | t$_{CAS}$ | 13 | 10K | 15 | 10K | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | t$_{RCD}$ | 20 | 37 | 20 | 45 | ns | 4 |
| $\overline{RAS}$ to column address delay time | t$_{RAD}$ | 15 | 25 | 15 | 30 | ns | 10 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | t$_{CRP}$ | 5 | | 5 | | ns | |
| Row address set-up time | t$_{ASR}$ | 0 | | 0 | | ns | |
| Row address hold time | t$_{RAH}$ | 10 | | 10 | | ns | |
| Column address set-up time | t$_{ASC}$ | 0 | | 0 | | ns | 13 |
| Column address hold time | t$_{CAH}$ | 10 | | 10 | | ns | 13 |
| Column address to $\overline{RAS}$ lead time | t$_{RAL}$ | 25 | | 30 | | ns | |
| Read command set-up time | t$_{RCS}$ | 0 | | 0 | | ns | |
| Read command hold time referenced to $\overline{CAS}$ | t$_{RCH}$ | 0 | | 0 | | ns | 8 |
| Read command hold time referenced to $\overline{RAS}$ | t$_{RRH}$ | 0 | | 0 | | ns | 8 |
| Write command hold time | t$_{WCH}$ | 10 | | 10 | | ns | |
| Write command pulse width | t$_{WP}$ | 10 | | 10 | | ns | |
| Write command to $\overline{RAS}$ lead time | t$_{RWL}$ | 15 | | 15 | | ns | |
| Write command to $\overline{CAS}$ lead time | t$_{CWL}$ | 13 | | 15 | | ns | 16 |
| Data set-up time | t$_{DS}$ | 0 | | 0 | | ns | 9,19 |
| Data hold time | t$_{DH}$ | 10 | | 10 | | ns | 9,19 |

## AC CHARACTERISTICS (Continued)

| Parameter | Symbol | -50 | | -60 | | Units | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Refresh period (4K, Normal) | $t_{REF}$ | | 64 | | 64 | ms | |
| Refresh period (8K, Normal) | $t_{REF}$ | | 64 | | 64 | ms | |
| Write command set-up time | $t_{WCS}$ | 0 | | 0 | | ns | 7 |
| $\overline{CAS}$ to $\overline{W}$ delay time | $t_{CWD}$ | 36 | | 38 | | ns | 7,15 |
| $\overline{RAS}$ to $\overline{W}$ delay time | $t_{RWD}$ | 73 | | 83 | | ns | 7 |
| Column address to $\overline{W}$ delay time | $t_{AWD}$ | 48 | | 53 | | ns | 7 |
| $\overline{CAS}$ precharge $\overline{W}$ delay time | $t_{CPWD}$ | 53 | | 60 | | ns | |
| $\overline{CAS}$ set-up time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh) | $t_{CSR}$ | 5 | | 5 | | ns | 17 |
| $\overline{CAS}$ hold time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh) | $t_{CHR}$ | 10 | | 10 | | ns | 18 |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | $t_{RPC}$ | 5 | | 5 | | ns | |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | | 30 | | 35 | ns | 3 |
| Fast Page mode cycle time | $t_{PC}$ | 35 | | 40 | | ns | |
| Fast Page mode read-modify-write cycle time | $t_{PRWC}$ | 76 | | 85 | | ns | |
| $\overline{CAS}$ precharge time (Fast Page cycle) | $t_{CP}$ | 10 | | 10 | | ns | 14 |
| $\overline{RAS}$ pulse width (Fast Page cycle) | $t_{RASP}$ | 50 | 200K | 60 | 200K | ns | |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{RHCP}$ | 30 | | 35 | | ns | |
| $\overline{OE}$ access time | $t_{OEA}$ | | 13 | | 15 | ns | |
| $\overline{OE}$ to data delay | $t_{OED}$ | 13 | | 13 | | ns | |
| Output buffer turn off delay time from $\overline{OE}$ | $t_{OEZ}$ | 0 | 13 | 0 | 13 | ns | 6 |
| $\overline{OE}$ command hold time | $t_{OEH}$ | 13 | | 15 | | ns | |
| Write command set-up time (Test mode in) | $t_{WTS}$ | 10 | | 10 | | ns | 11 |
| Write command hold time (Test mode in) | $t_{WTH}$ | 15 | | 15 | | ns | 11 |
| $\overline{W}$ to $\overline{RAS}$ precharge time (C-B-R refresh) | $t_{WRP}$ | 10 | | 10 | | ns | |
| $\overline{W}$ to $\overline{RAS}$ hold time (C-B-R refresh) | $t_{WRH}$ | 10 | | 10 | | ns | |
| $\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh) | $t_{RASS}$ | 100 | | 100 | | us | 20,21,22 |
| $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh) | $t_{RPS}$ | 90 | | 110 | | ns | 20,21,22 |
| $\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh) | $t_{CHS}$ | -50 | | -50 | | ns | 20,21,22 |

## TEST MODE CYCLE

( Note 11 )

| Parameter | Symbol | -50 | | -60 | | Units | Note |
|---|---|---|---|---|---|---|---|
| | | **Min** | **Max** | **Min** | **Max** | | |
| Random read or write cycle time | $t_{RC}$ | 95 | | 115 | | ns | |
| Read-modify-write cycle time | $t_{RWC}$ | 138 | | 160 | | ns | |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | | 55 | | 65 | ns | 3,4,10,12 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | | 18 | | 20 | ns | 3,4,5,12 |
| Access time from column address | $t_{AA}$ | | 30 | | 35 | ns | 3,10,12 |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 55 | 10K | 65 | 10K | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 18 | 10K | 20 | 10K | ns | |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 18 | | 20 | | ns | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 55 | | 65 | | ns | |
| Column Address to $\overline{RAS}$ lead time | $t_{RAL}$ | 30 | | 35 | | ns | |
| $\overline{CAS}$ to $\overline{W}$ delay time | $t_{CWD}$ | 41 | | 43 | | ns | 7 |
| $\overline{RAS}$ to $\overline{W}$ delay time | $t_{RWD}$ | 78 | | 88 | | ns | 7 |
| Column Address to $\overline{W}$ delay time | $t_{AWD}$ | 53 | | 58 | | ns | 7 |
| Fast Page mode cycle time | $t_{PC}$ | 40 | | 45 | | ns | |
| Fast Page mode read-modify-write cycle time | $t_{PRWC}$ | 81 | | 90 | | ns | |
| $\overline{RAS}$ pulse width (Fast Page cycle) | $t_{RASP}$ | 55 | 200K | 65 | 200K | ns | |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | | 35 | | 40 | ns | 3 |
| $\overline{OE}$ access time | $t_{OEA}$ | | 18 | | 20 | ns | |
| $\overline{OE}$ to data delay | $t_{OED}$ | 18 | | 18 | | ns | |
| $\overline{OE}$ command hold time | $t_{OEH}$ | 18 | | 20 | | ns | |

**NOTES**

1. An initial pause of 200$\mu$s is required after power-up followed by any 8 $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. $V_{IH}$(min) and $V_{IL}$(max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$(min) and $V_{IL}$(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL load and 100pF.

4. Operation within the $t_{RCD}$(max) limit insures that $t_{RAC}$(max) can be met, $t_{RCD}$(max) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$(max) limit, then access time is controlled exclusively by $t_{CAC}$.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. $t_{OFF}$(min)and $t_{OEZ}$(max) define the time at which the output achieves the open circuit condition and are not referenced $V_{oh}$ or $V_{ol}$.

7. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$ and $t_{AWD}$ are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

8. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

9. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{W}$ falling edge in read-modify-write cycles. Operation within the $t_{RAD}$(max) limit insures that $t_{RAC}$(max) can be met. $t_{RAD}$(max) is specified as a reference point only.

10. If $t_{RAD}$ is greater than the specified $t_{RAD}$(max) limit, then access time is controlled by $t_{AA}$. These specifications are applied in the test mode.

11. In test mode read cycle, the value of $t_{RAC}$, $t_{AA}$, $t_{CAC}$ is delayed by 2ns to 5ns for the specified values. These parameters

12. should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

## K4F64(6)1611C Truth Table

| $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{W}$ | $\overline{OE}$ | DQ0 - DQ7 | DQ8-DQ15 | STATE |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | Hi-Z | Hi-Z | Standby |
| L | H | H | X | X | Hi-Z | Hi-Z | Refresh |
| L | L | H | H | L | DQ-OUT | Hi-Z | Byte Read |
| L | H | L | H | L | Hi-Z | DQ-OUT | Byte Read |
| L | L | L | H | L | DQ-OUT | DQ-OUT | Word Read |
| L | L | H | L | H | DQ-IN | - | Byte Write |
| L | H | L | L | H | - | DQ-IN | Byte Write |
| L | L | L | L | H | DQ-IN | DQ-IN | Word Write |
| L | L | L | H | H | Hi-Z | Hi-Z | - |

13. $t_{ASC}$, $t_{CAH}$ are referenced to the earlier $\overline{CAS}$ falling edge.

14. $t_{CP}$ is specified from the later $\overline{CAS}$ rising edge in the previous cycle to the earlier $\overline{CAS}$ falling edge in the next cycle.

15. $t_{CWD}$ is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

16. $t_{CWL}$ is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

17. $t_{CSR}$ is referenced to the earlier $\overline{CAS}$ falling edge before $\overline{RAS}$ transition low.

18. $t_{CHR}$ is referenced to the later $\overline{CAS}$ rising edge after $\overline{RAS}$ transition low.
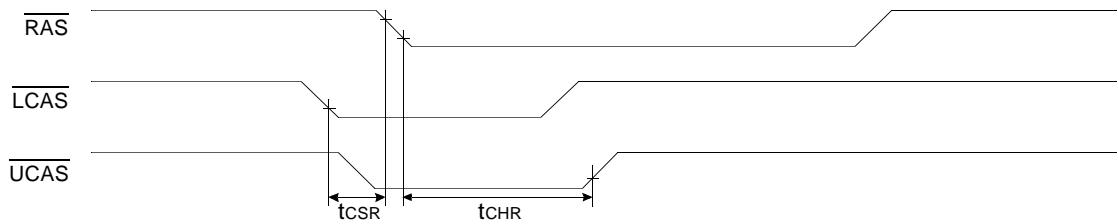


19. $t_{DS}$ is specified for the earlier $\overline{CAS}$ falling edge and $t_{DH}$ is specified by the later $\overline{CAS}$ falling edge.
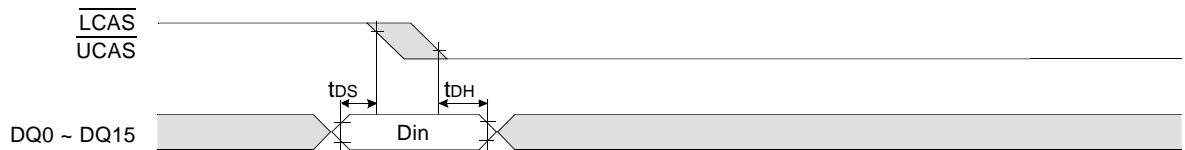


20. If $t_{RASS} \geq 100us$, then $\overline{RAS}$ precharge time must use $t_{RPS}$ instead of $t_{RP}$.

21. For $\overline{RAS}$-only refresh and burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096(4K/8K) cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

22. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval $\overline{CAS}$-before-$\overline{RAS}$ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

**WORD READ CYCLE**
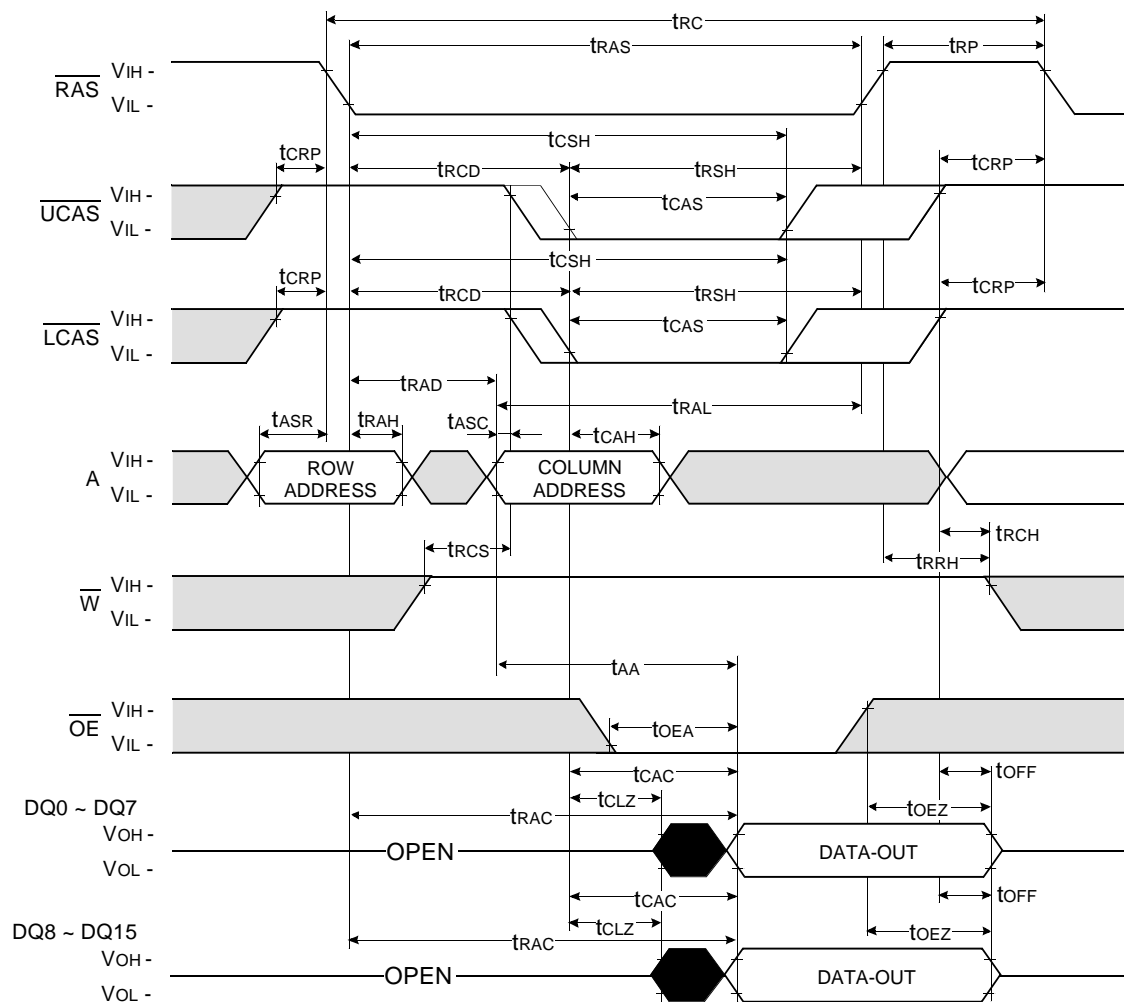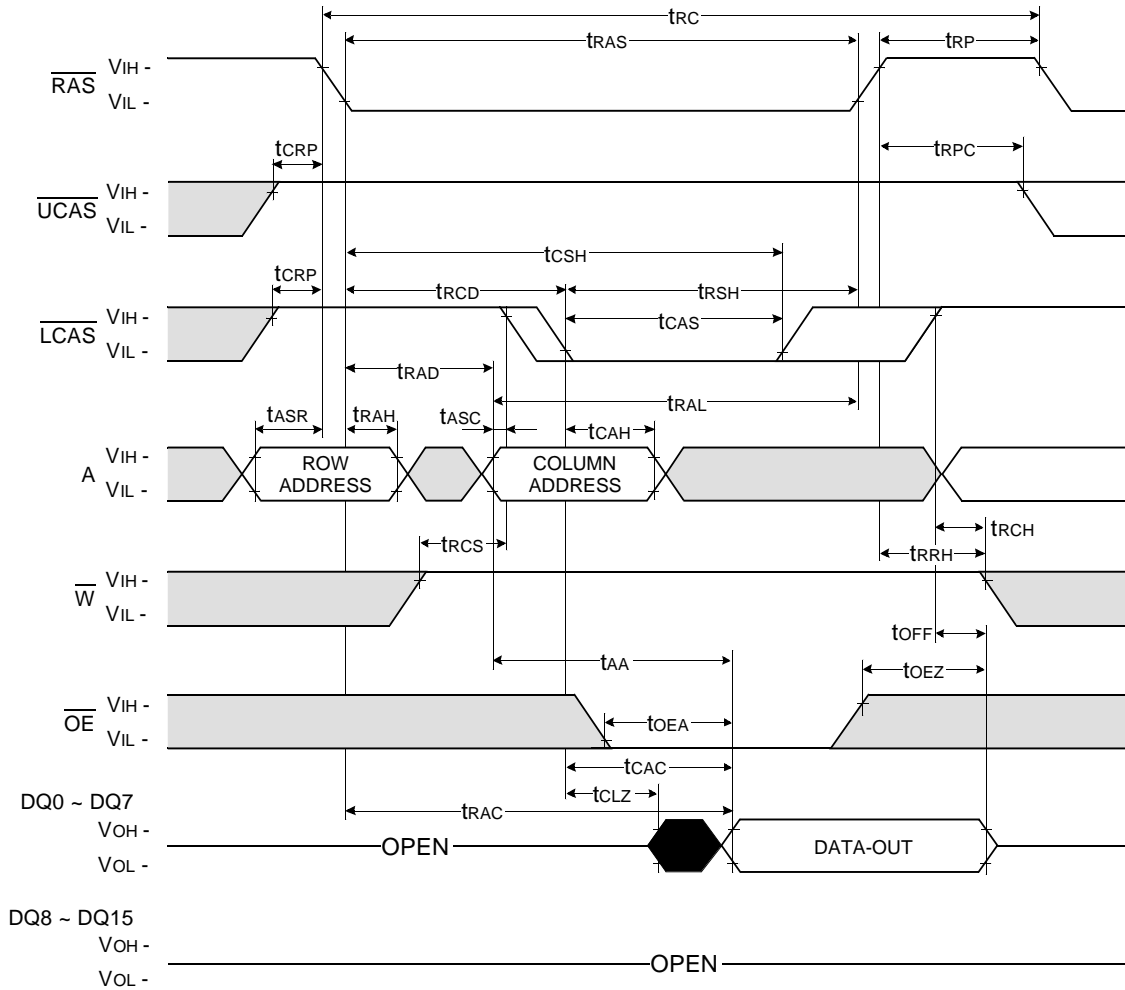


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## LOWER BYTE READ CYCLE

NOTE : $D_{IN}$ = OPEN



Don't care

Undefined

## UPPER BYTE READ CYCLE

NOTE : $D_{IN}$ = OPEN



| | |
|---|---|
| ▨ | Don't care |
| ■ | Undefined |
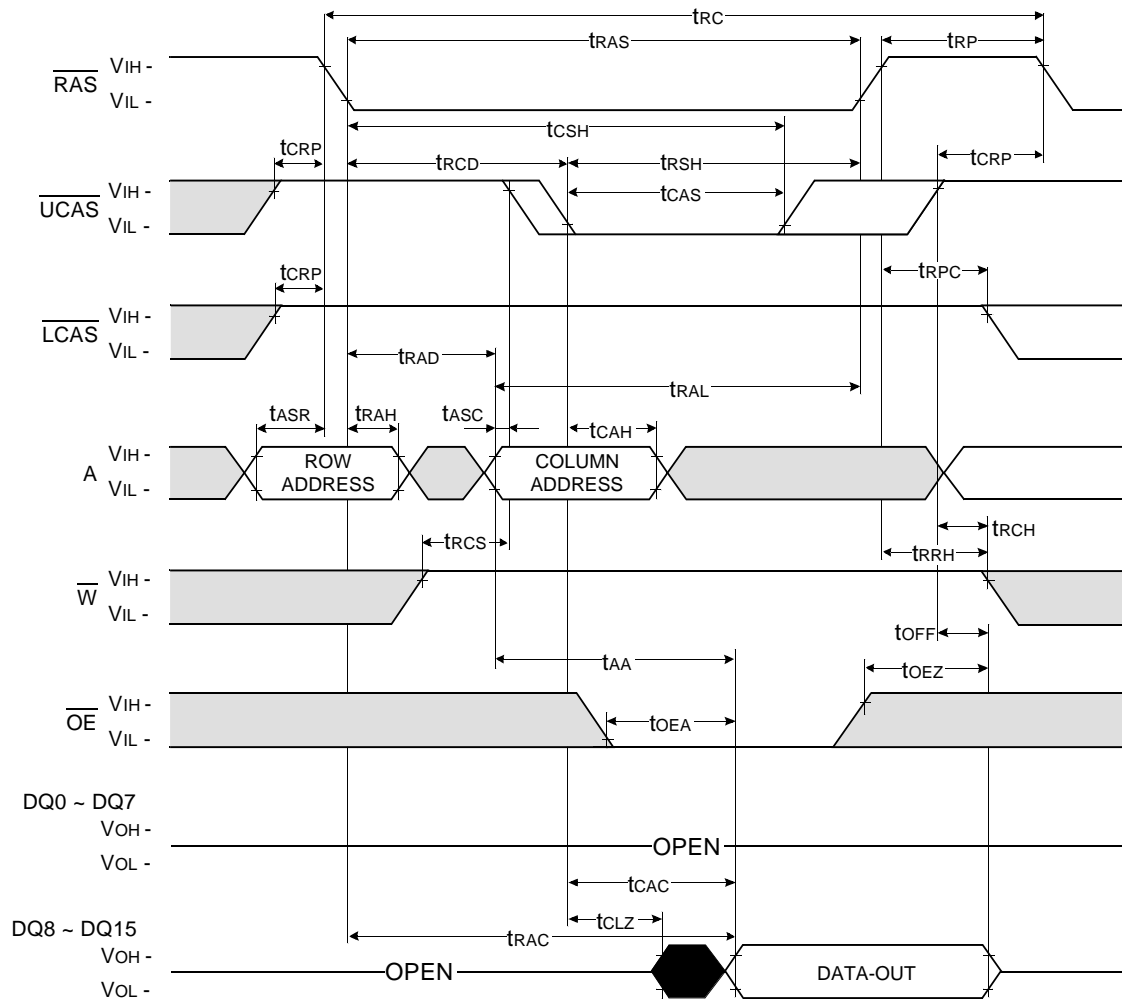
## WORD WRITE CYCLE ( EARLY WRITE )
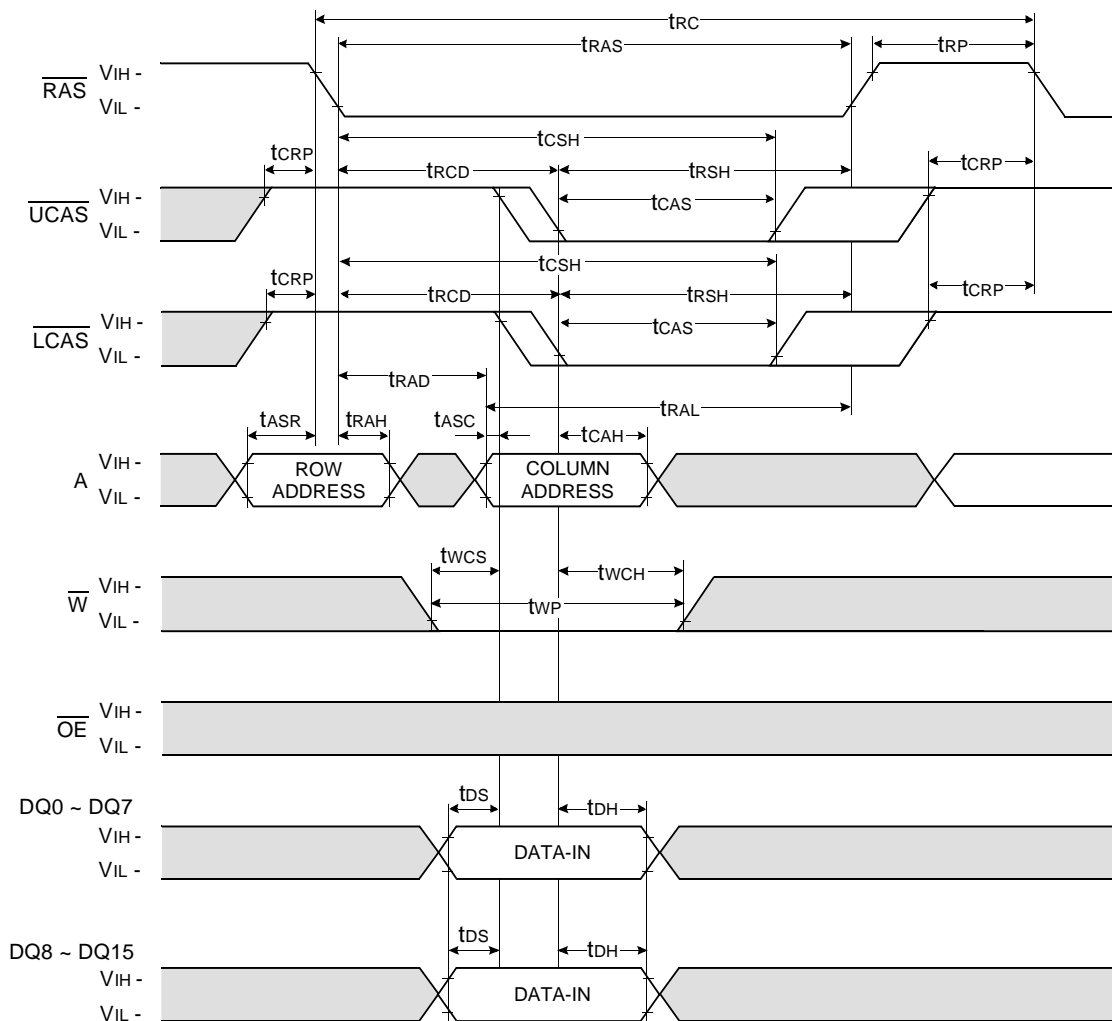
NOTE : D$_{OUT}$ = OPEN



Don't care

Undefined

## LOWER BYTE WRITE CYCLE ( EARLY WRITE )
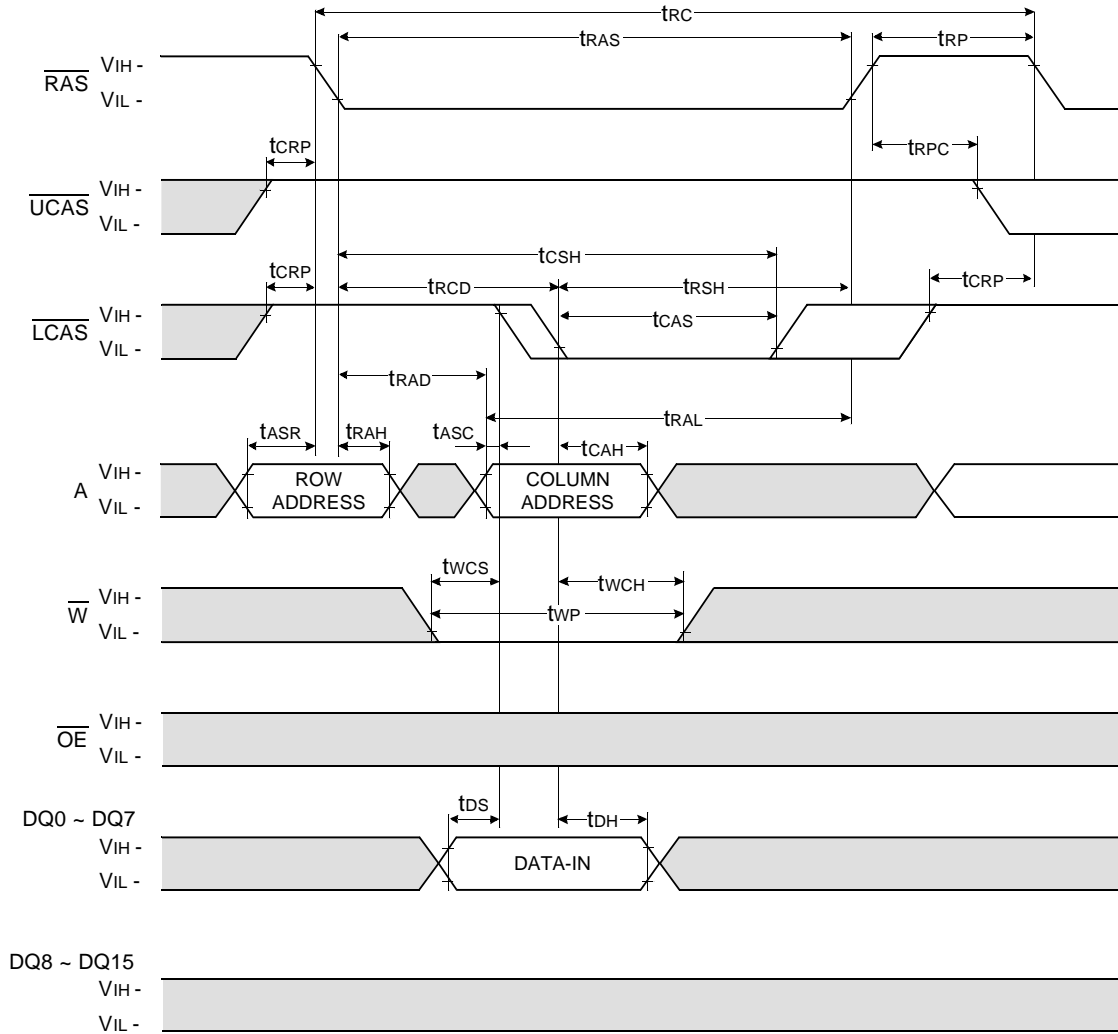
NOTE : $D_{OUT}$ = OPEN
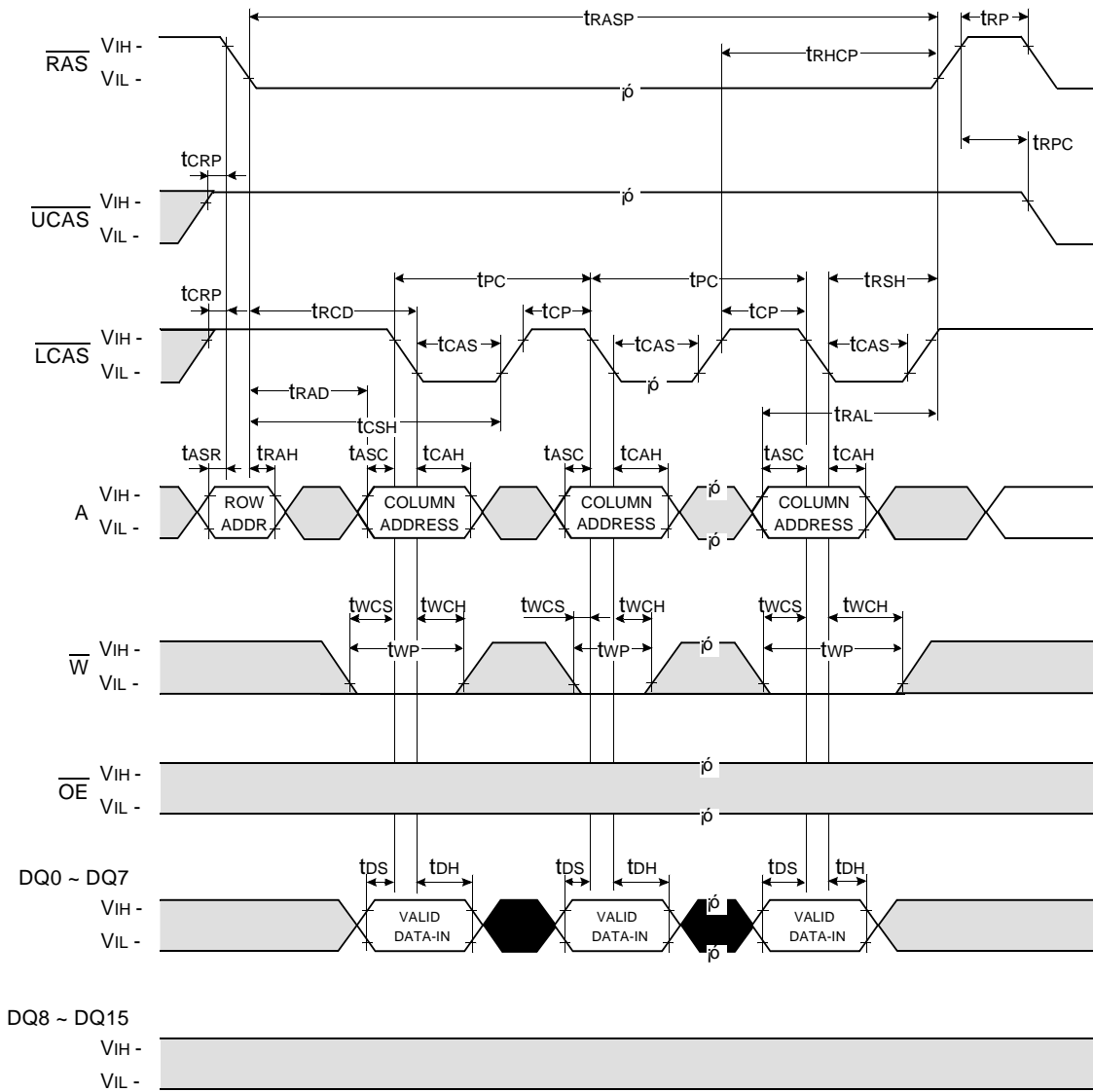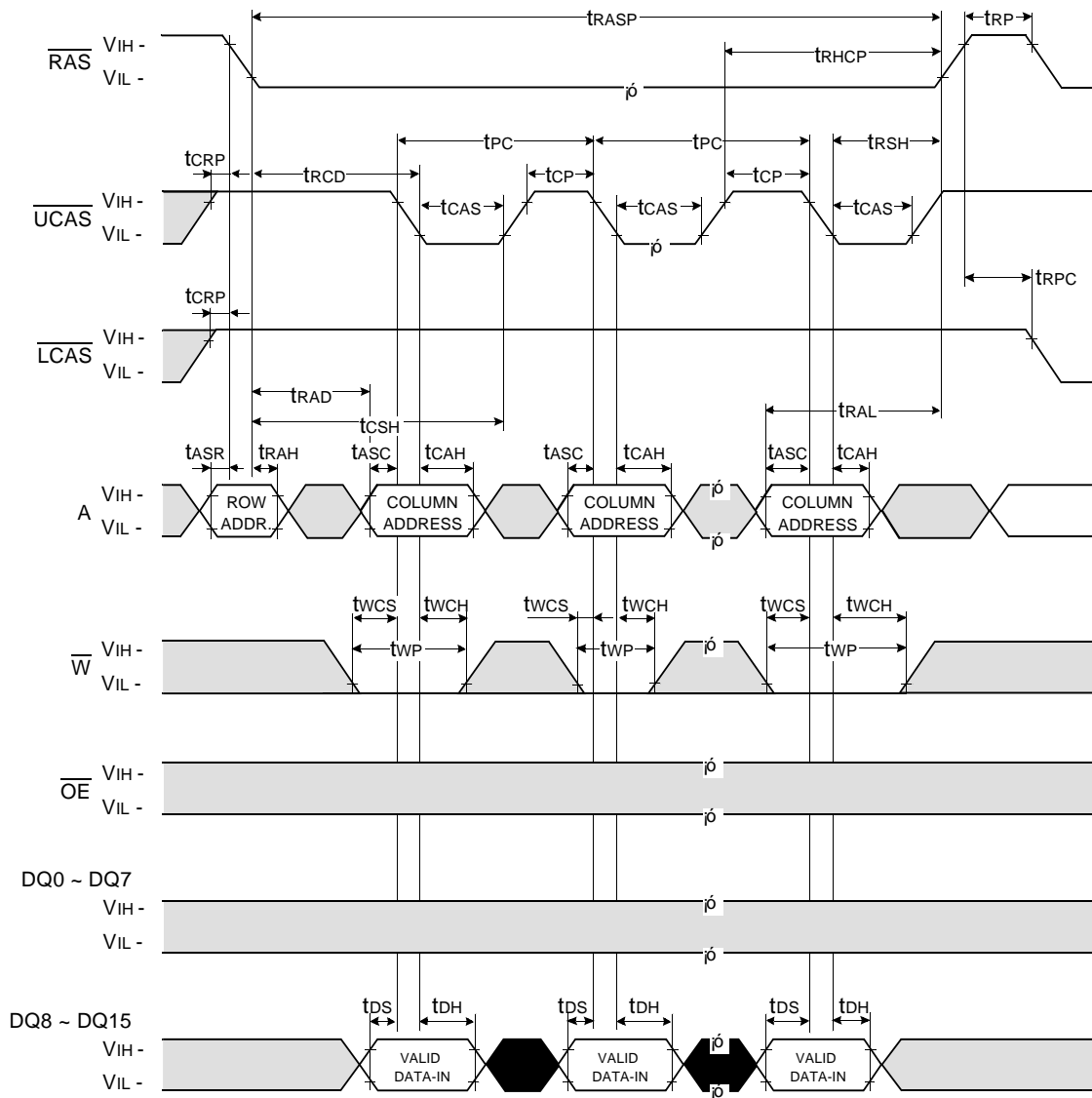


Don't care

Undefined
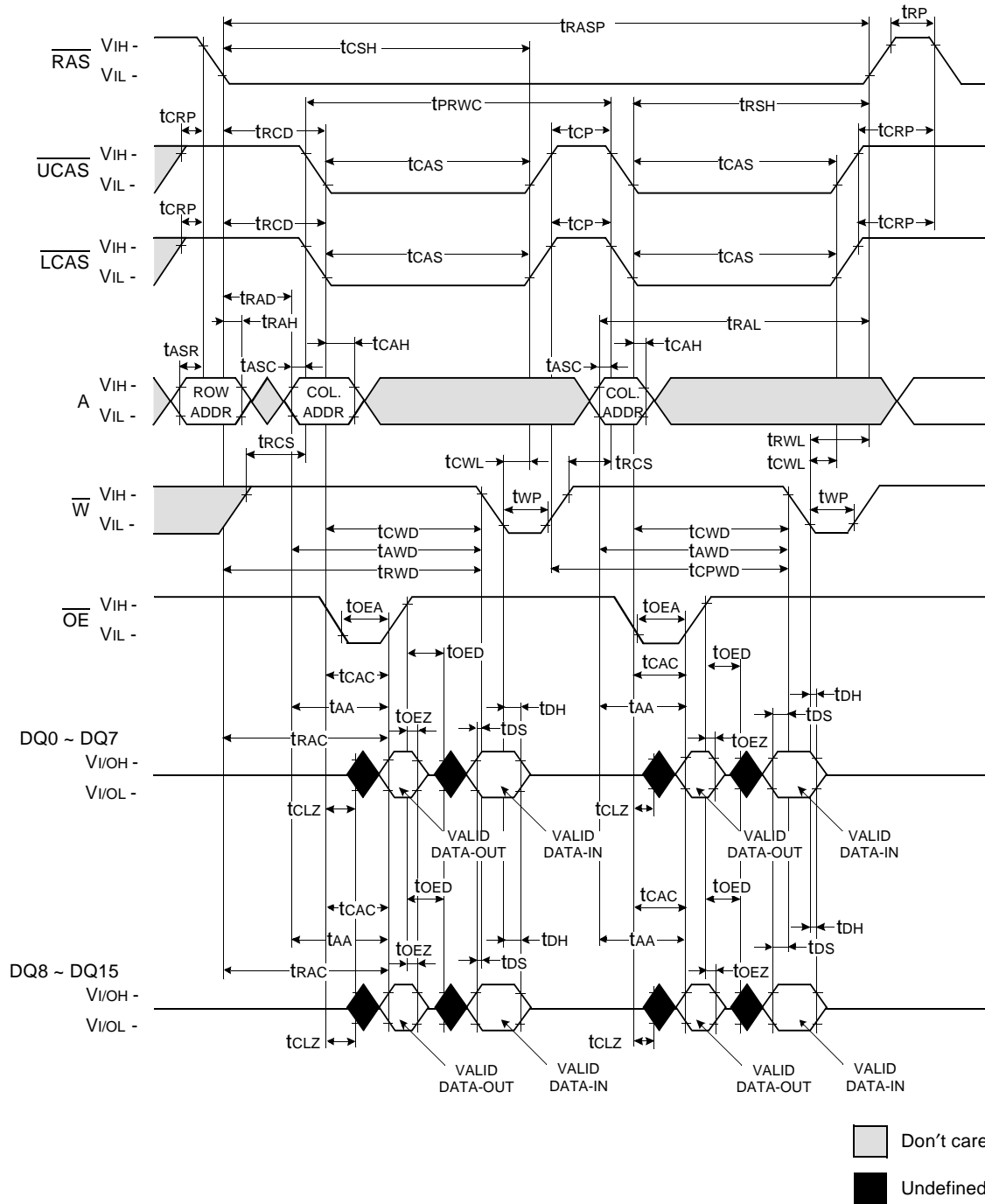
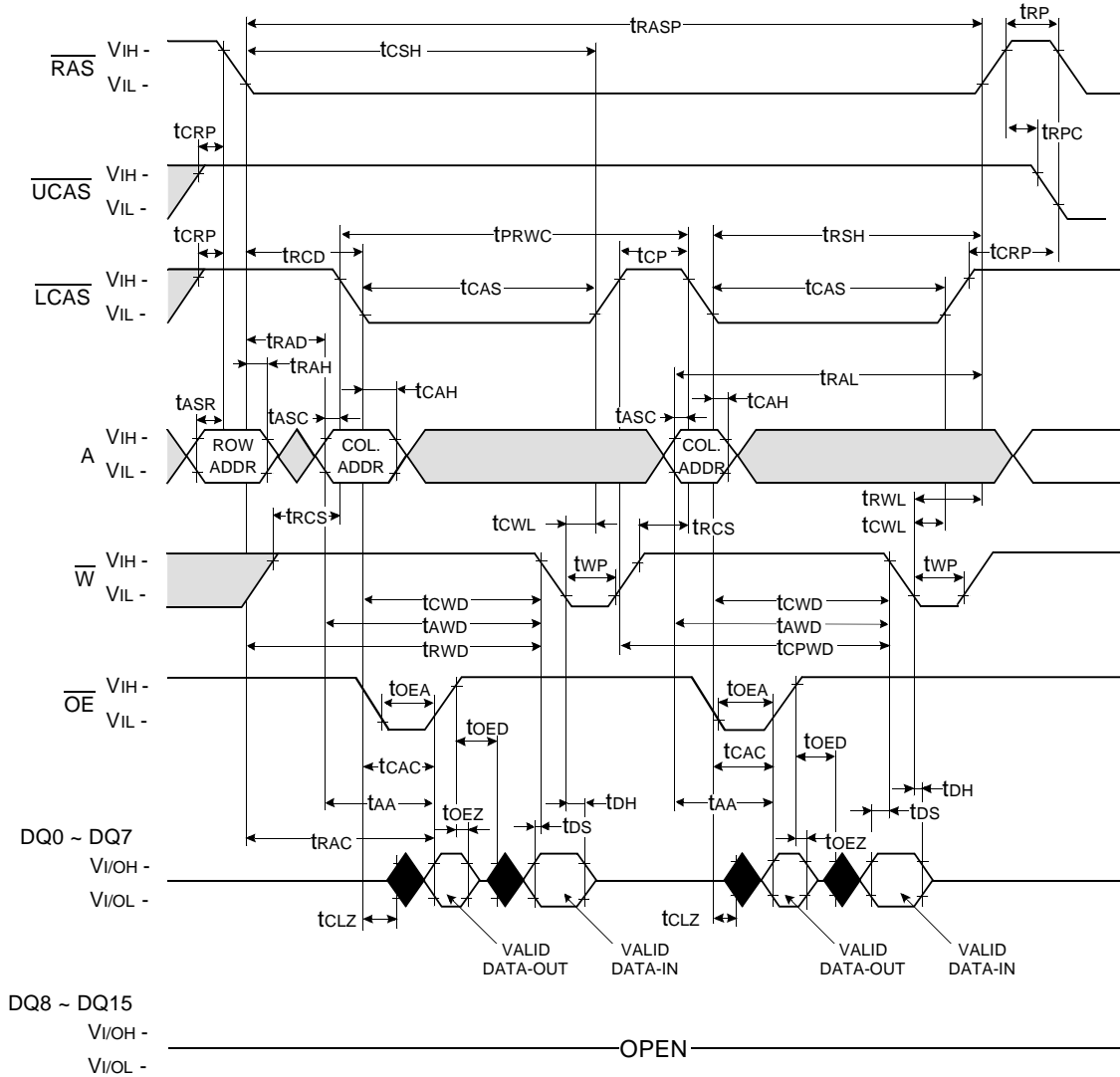## UPPER BYTE WRITE CYCLE ( EARLY WRITE )

NOTE : $D_{OUT}$ = OPEN

### WORD WRITE CYCLE ( $\overline{OE}$ CONTROLLED WRITE )

NOTE : D$_{OUT}$ = OPEN



Don't care

Undefined

## LOWER BYTE WRITE CYCLE ( $\overline{OE}$ CONTROLLED WRITE )

NOTE : D~OUT~ = OPEN

## UPPER BYTE WRITE CYCLE ( $\overline{OE}$ CONTROLLED WRITE )

NOTE : D$_{OUT}$ = OPEN
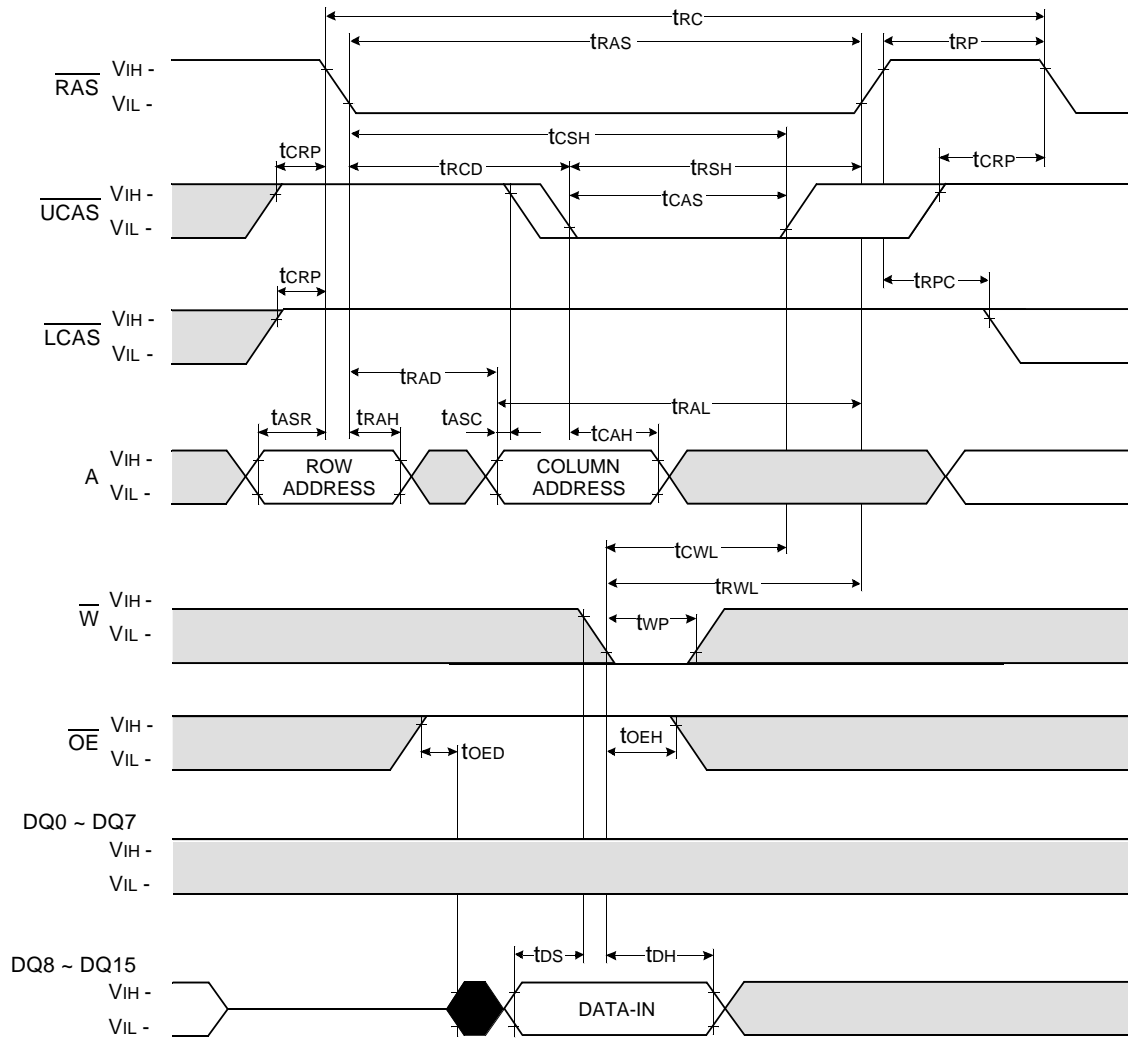


Don't care

Undefined

## WORD READ - MODIFY - WRITE CYCLE
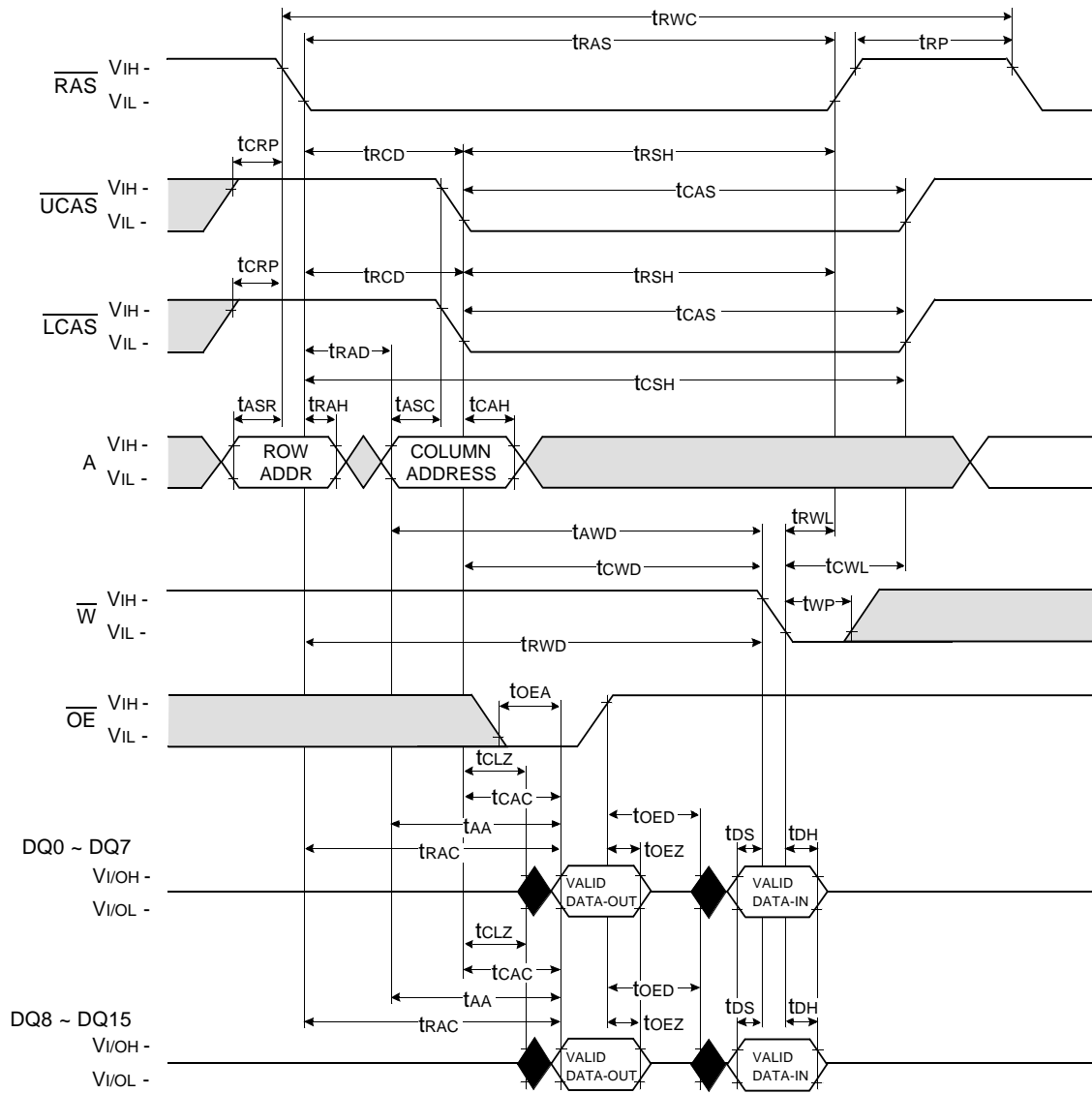


Don't care

Undefined

**LOWER-BYTE READ - MODIFY - WRITE CYCLE**
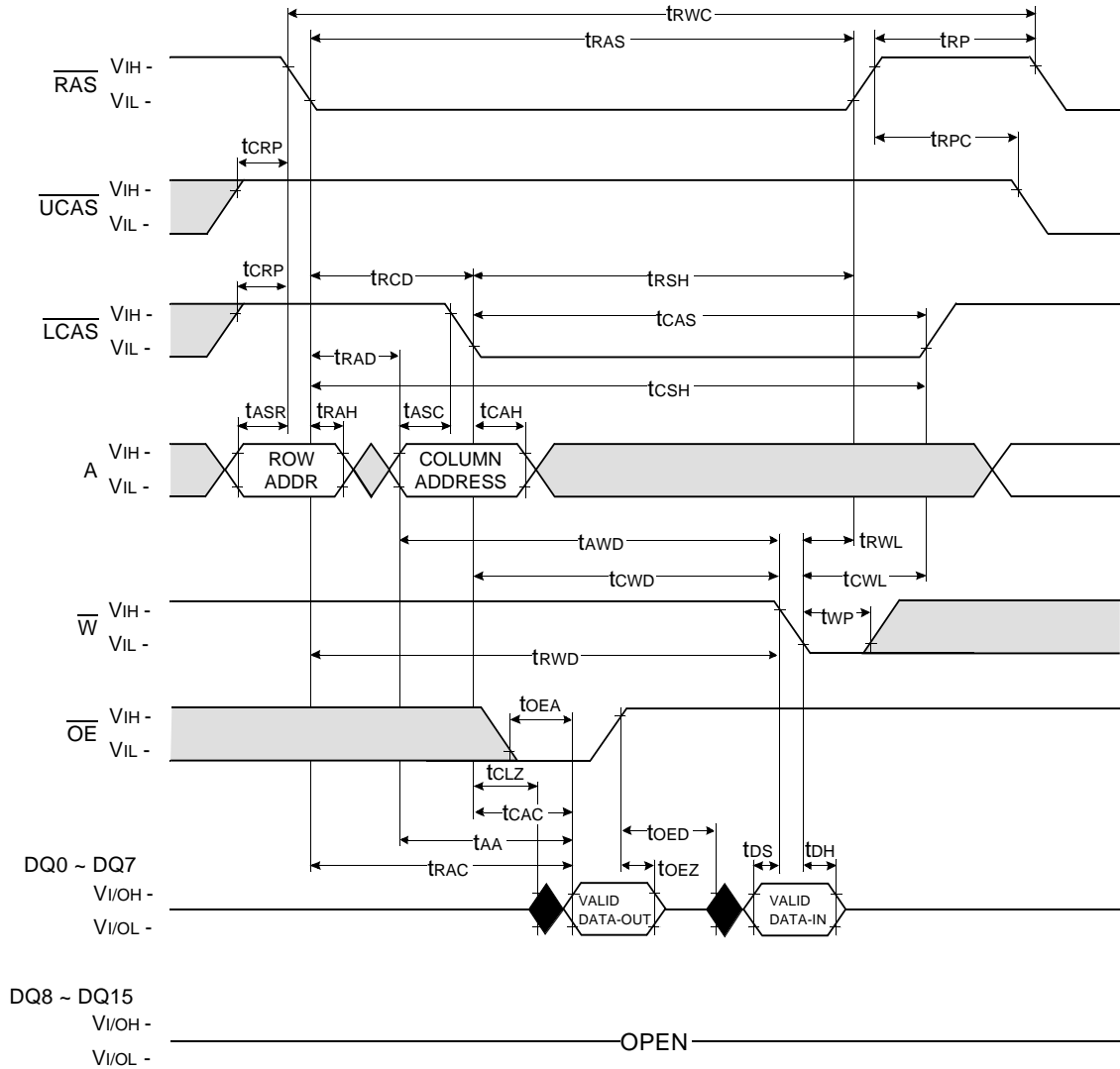


Don't care

Undefined

**UPPER-BYTE READ - MODIFY - WRITE CYCLE**
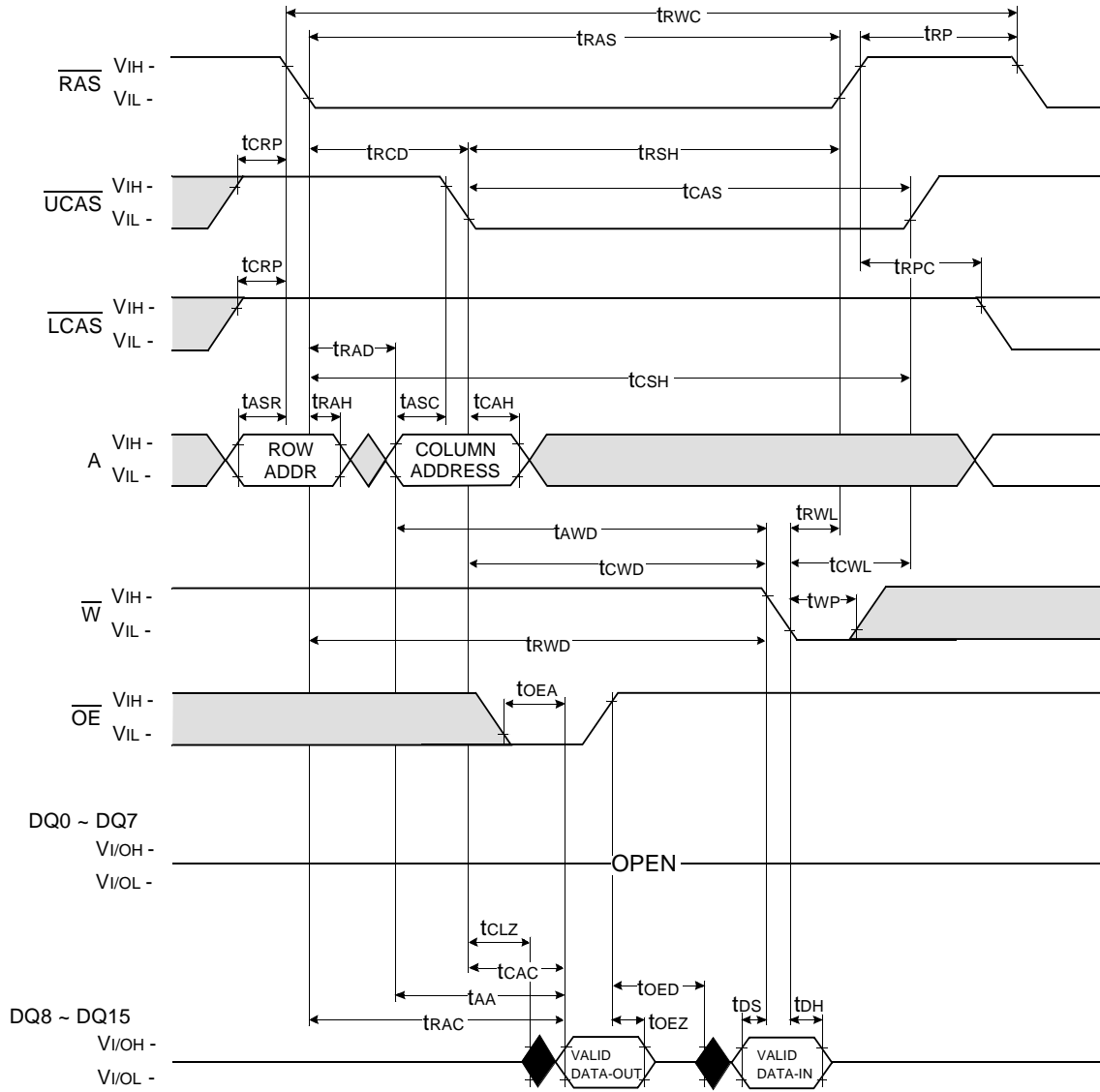
### FAST PAGE MODE WORD READ CYCLE
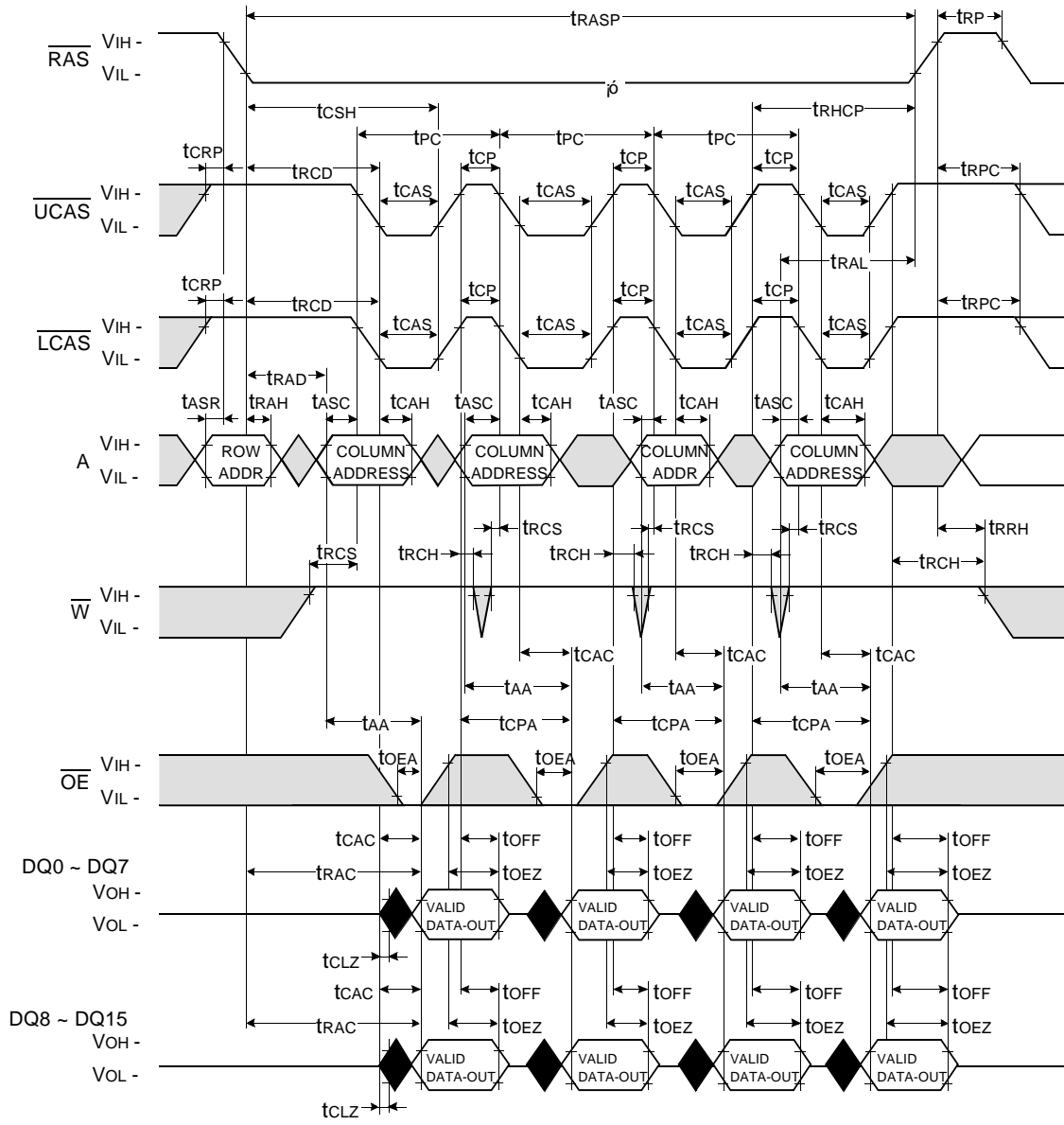


Don't care

Undefined

## FAST PAGE MODE LOWER BYTE READ CYCLE
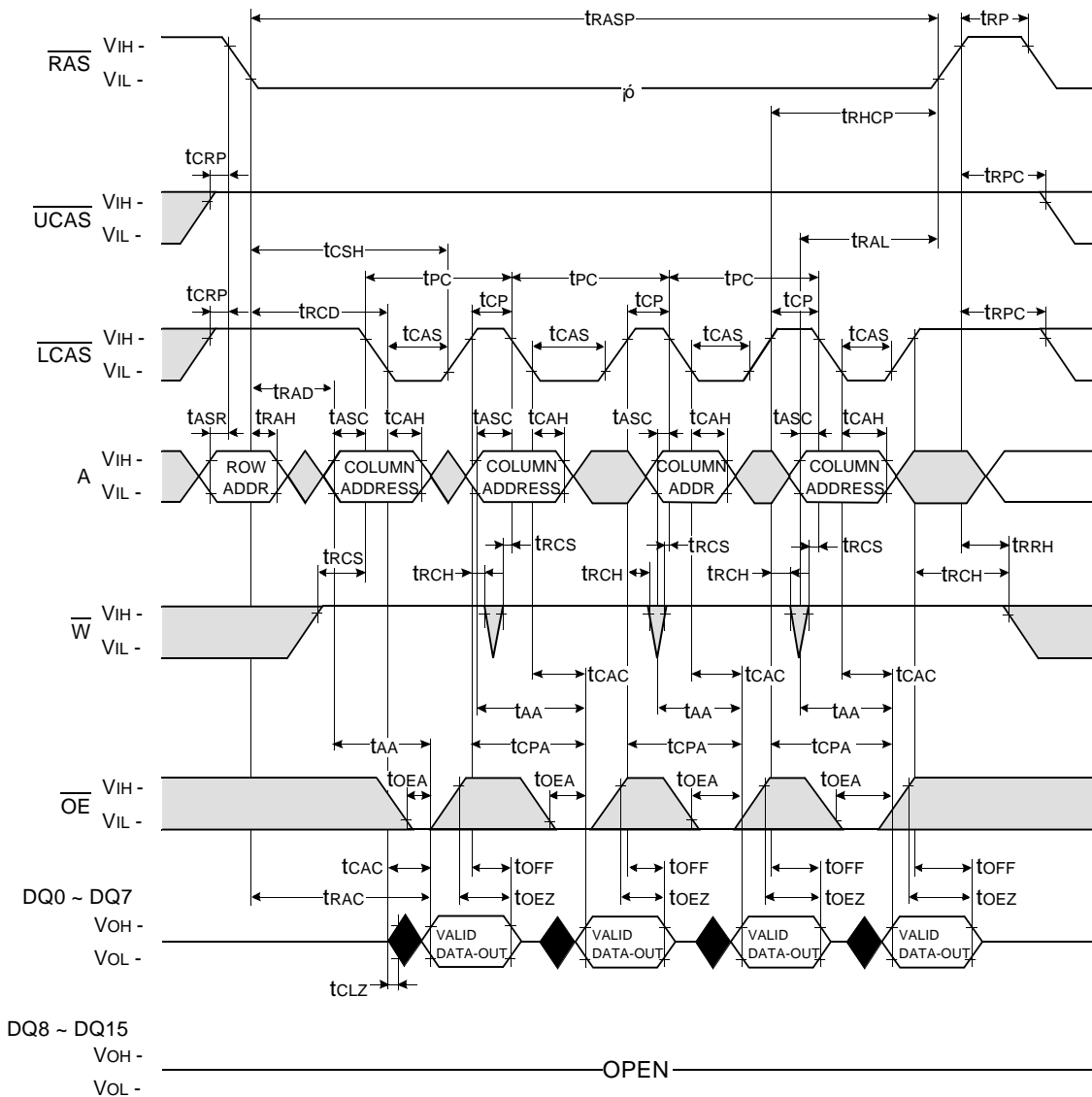
## FAST PAGE MODE UPPER BYTE READ CYCLE
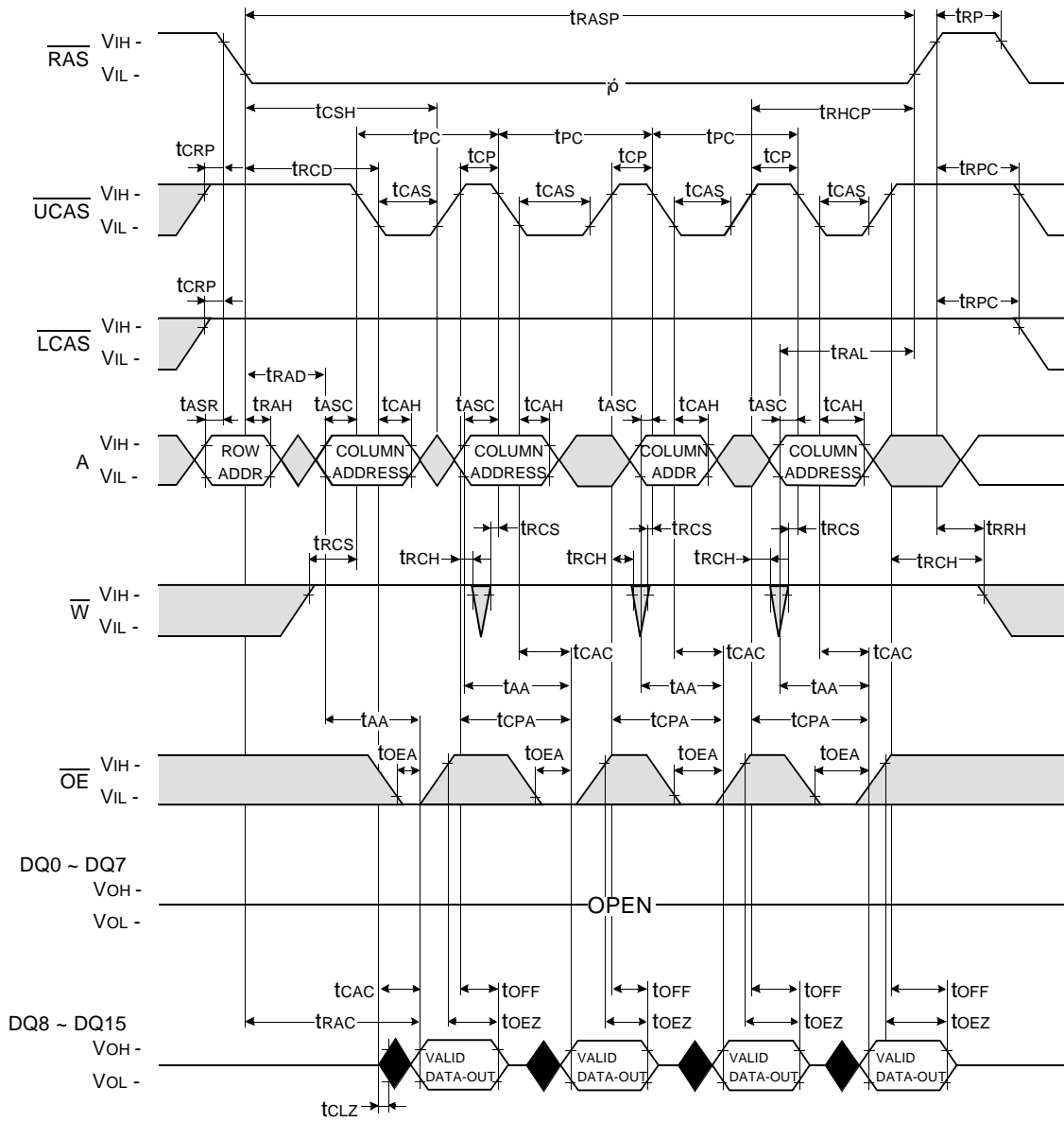


| | Don't care |
|---|---|
| | Undefined |

## FAST PAGE MODE WORD WRITE CYCLE ( EARLY WRITE )
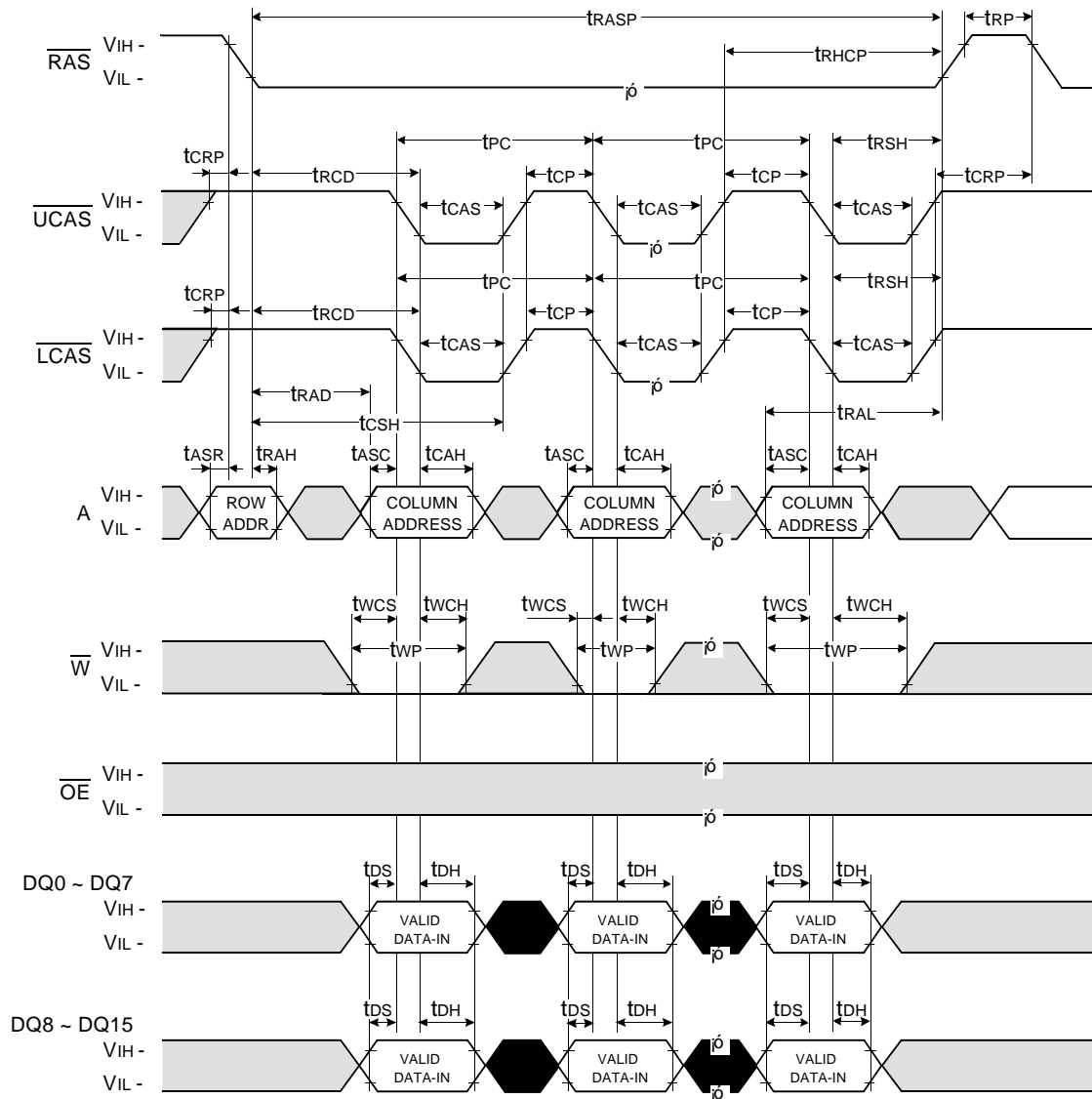
NOTE : $D_{OUT}$ = OPEN

## FAST PAGE MODE LOWER BYTE WRITE CYCLE ( EARLY WRITE )

NOTE : D$_{OUT}$ = OPEN

## FAST PAGE MODE UPPER BYTE WRITE CYCLE ( EARLY WRITE )

NOTE : D<sub>OUT</sub> = OPEN

**FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE**

**FAST PAGE MODE LOWER BYTE READ - MODIFY - WRITE CYCLE**



Don't care

Undefined

## FAST PAGE MODE UPPER BYTE READ - MODIFY - WRITE CYCLE
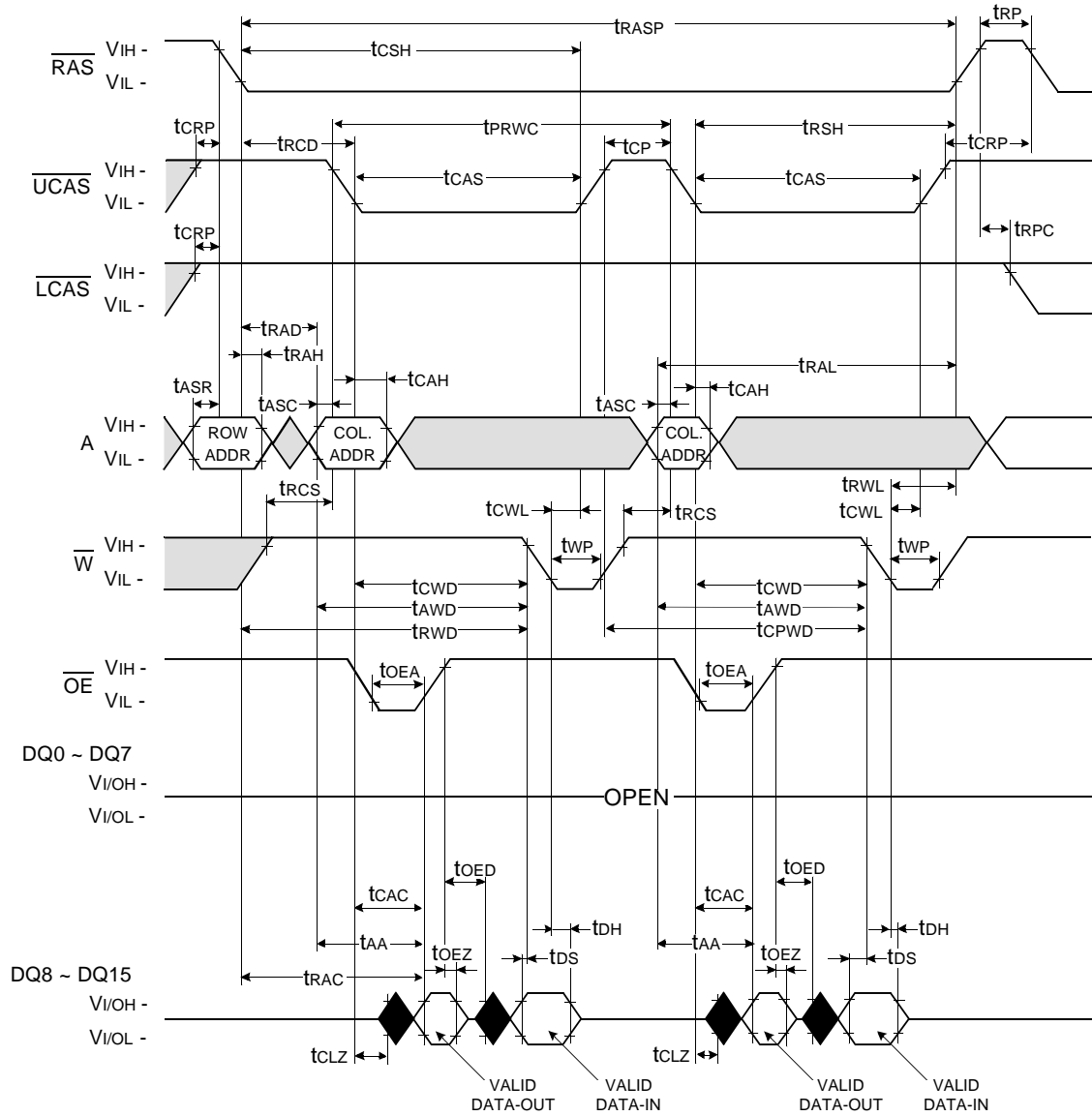


| | |
|---|---|
| ▨ | Don't care |
| ■ | Undefined |

## $\overline{RAS}$ - ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$ , D$_{IN}$ = Don't care
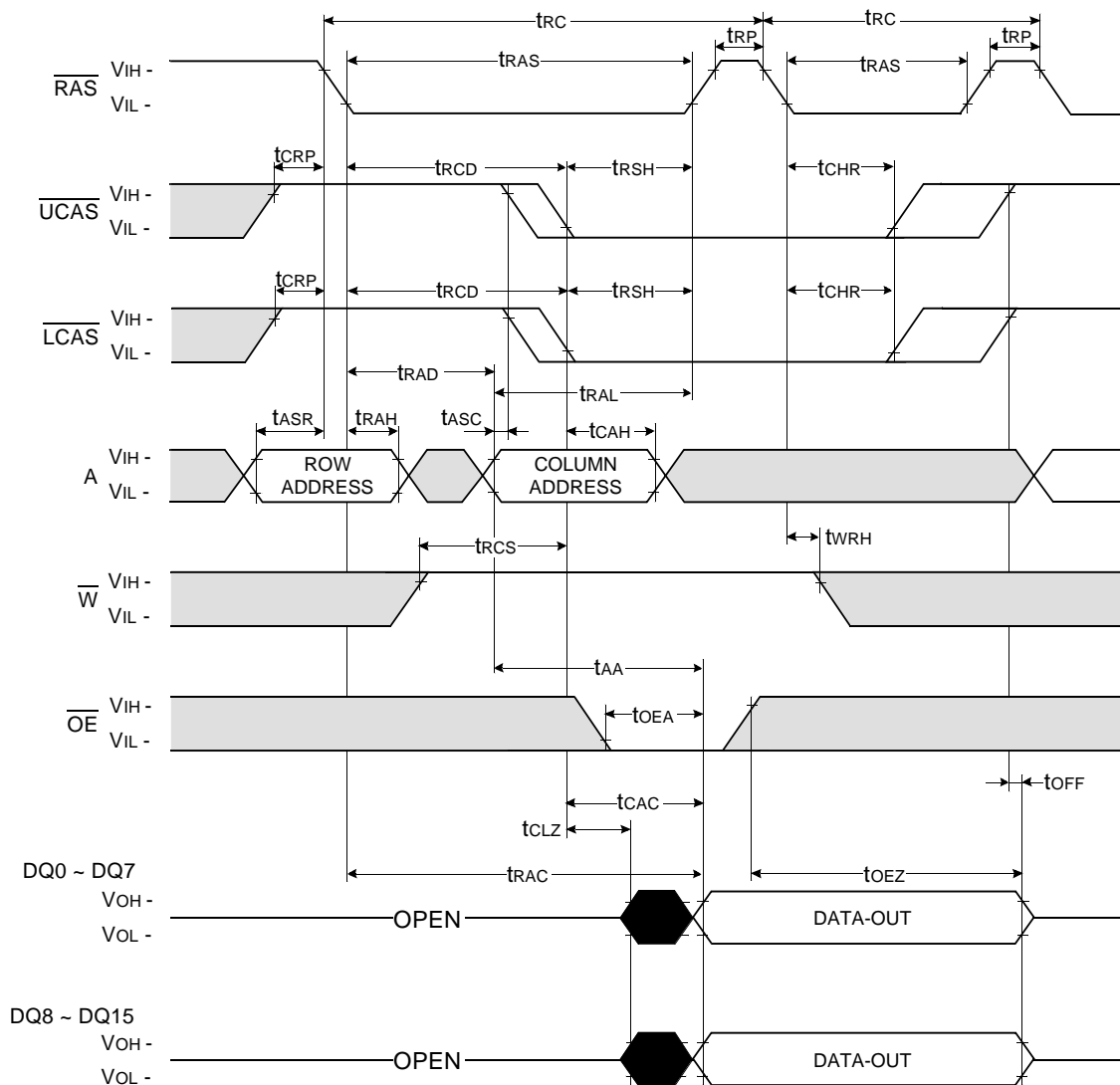
D$_{OUT}$ = OPEN
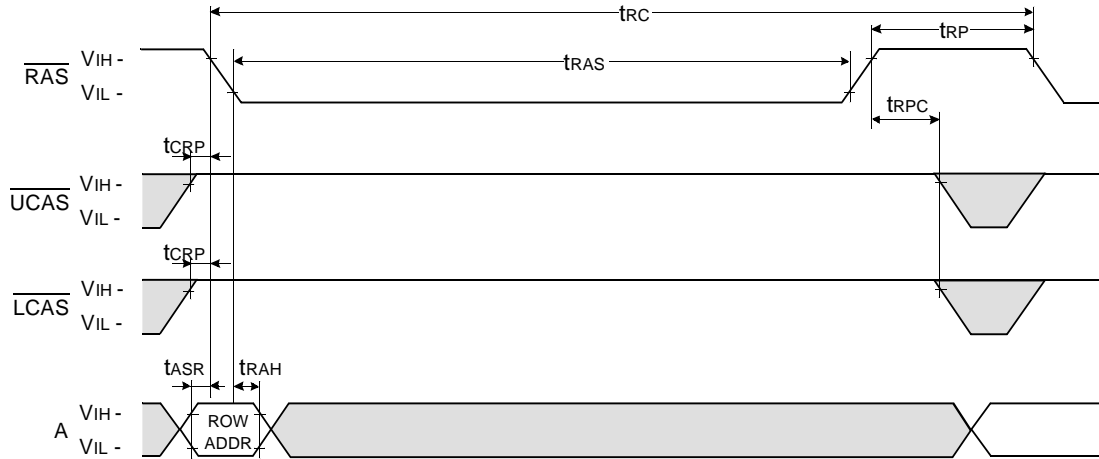


## $\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$ , A = Don't care
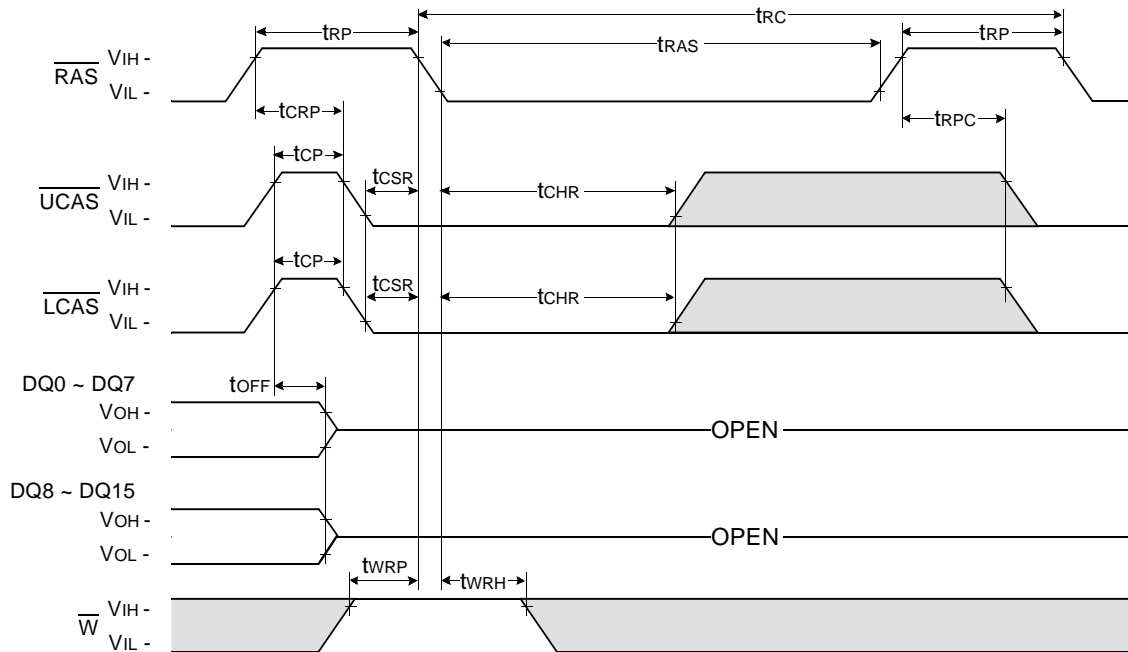


Don't care

Undefined

**HIDDEN REFRESH CYCLE ( READ )**
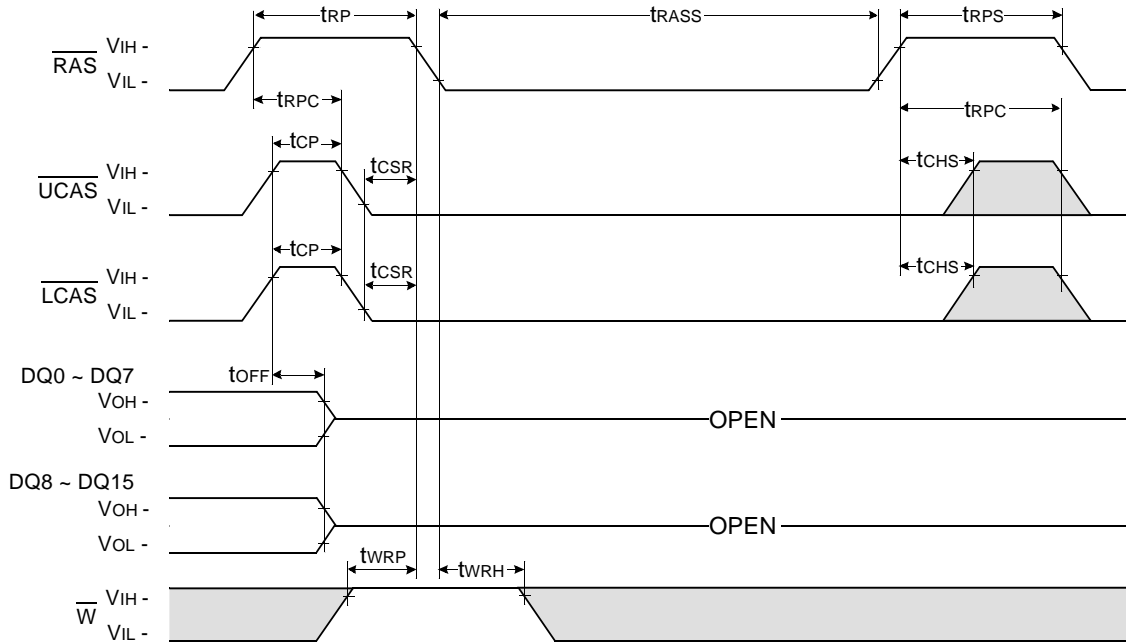


SAMSUNG
**ELECTRONICS**

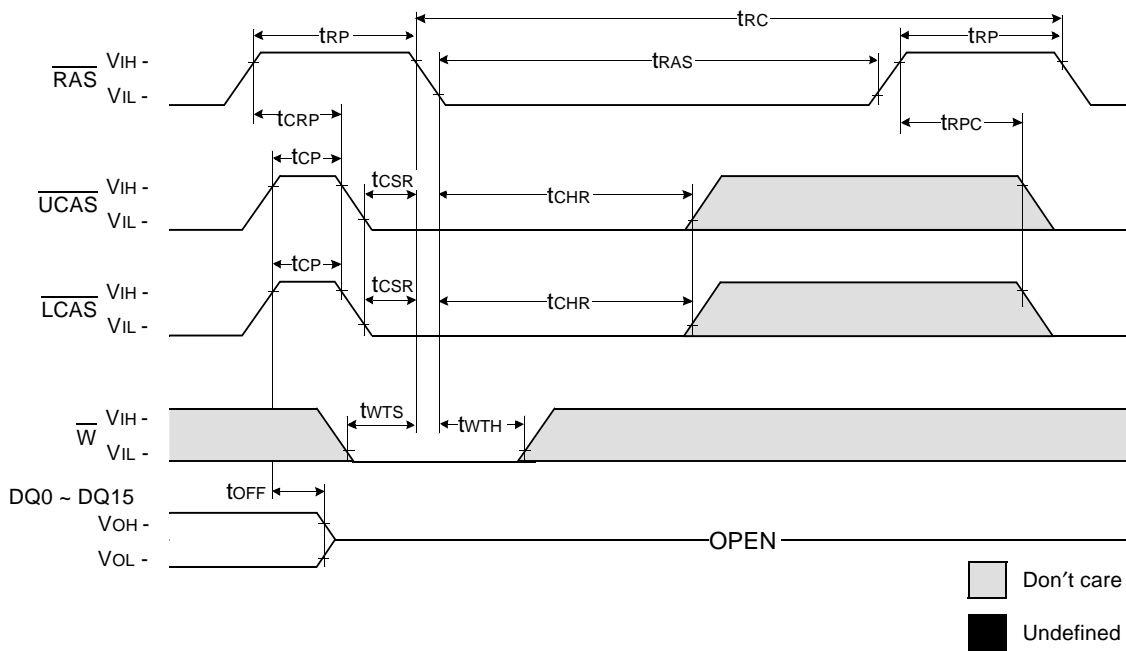## HIDDEN REFRESH CYCLE ( WRITE )

NOTE : D~OUT~ = OPEN
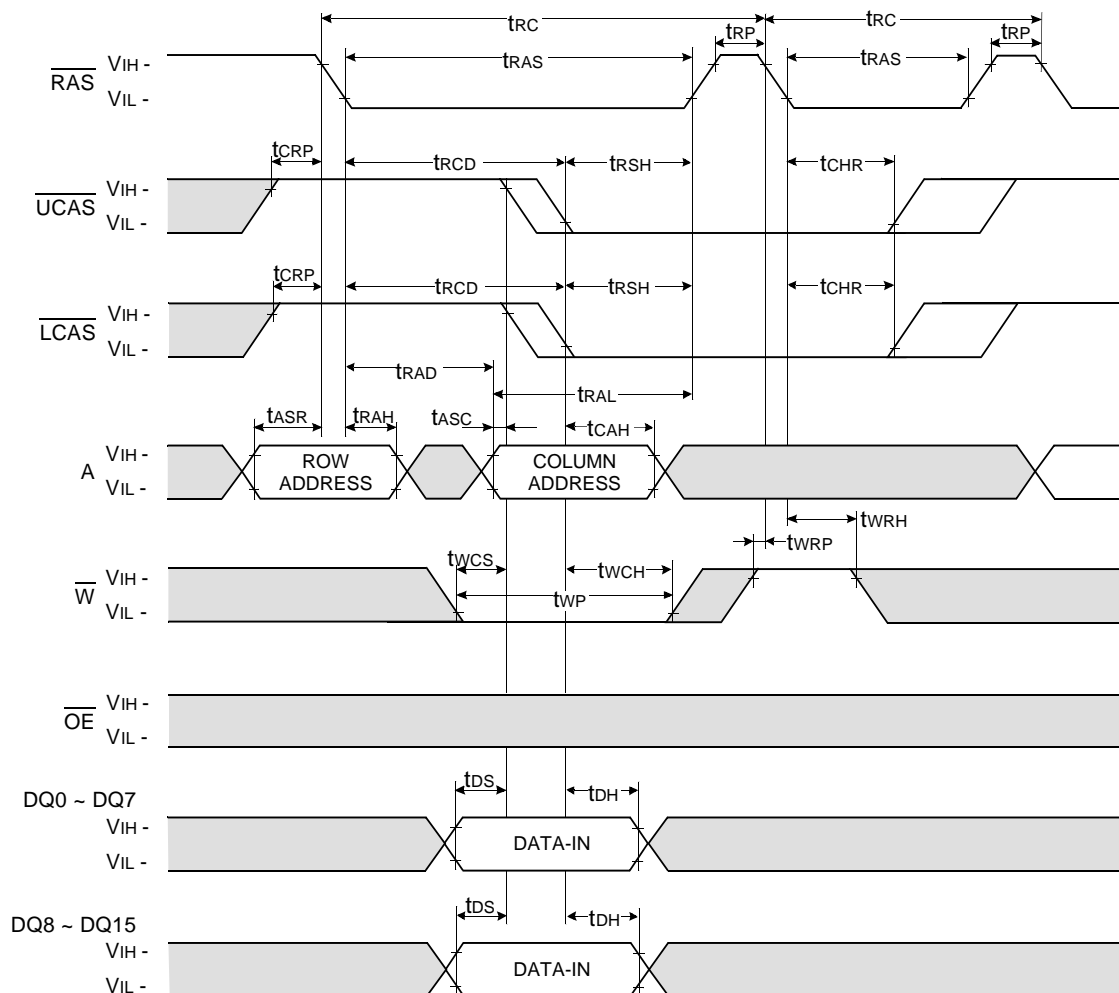
## CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : $\overline{OE}$ , A = Don't care



## TEST MODE IN CYCLE

NOTE : $\overline{OE}$ , A = Don't care



Don't care

Undefined

**PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II)**

**50 TSOP(II) 400mil**

Units : Inches (millimeters)



0.455 (11.56)
0.471 (11.96)

0.400 (10.16)

0.004 (0.10)
0.010 (0.25)

0.841 (21.35) MAX

0.821 (20.85)
0.829 (21.05)

0.047 (1.20) MAX

0.034 (0.875)

0.0315 (0.80)

0.002 (0.05) MIN

0.010 (0.25)
0.018 (0.45)

0.010 (0.25) TYP

0.018 (0.45)
0.030 (0.75)

0~8°