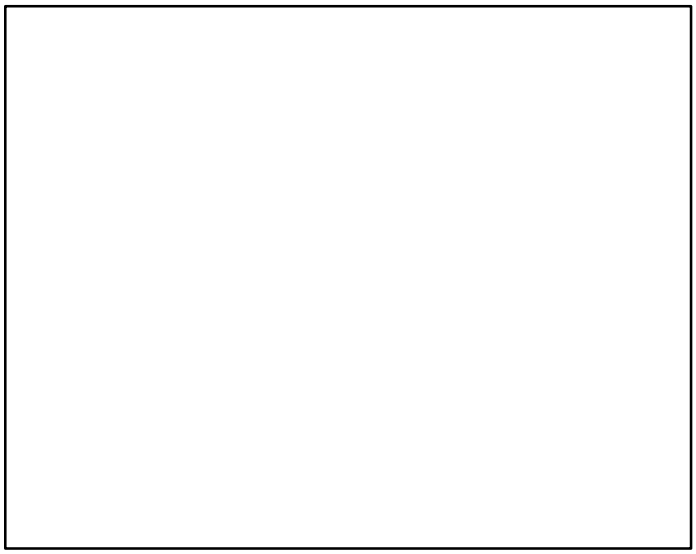
Circuit Characteristics 2

FAST AND LS TTL



CIRCUIT CHARACTERISTICS

FAMILY CHARACTERISTICS

LS TTL

The Low Power Schottky (LSTTL) family combines a current and power reduction improvement over standard 7400 TTL by a factor of 5. This is accomplished by using Schottky diode clamping to prevent saturation and advanced processing.

FAST TTL

The FAST Schottky TTL family provides a 75–80% power reduction compared to standard Schottky (54/74S) TTL and yet offers a 20–40% improvement in circuit performance over the standard Schottky due to the MOSAIC process. Also, FAST circuits contain additional circuitry to provide a flatter power/frequency curve. The input configuration of FAST uses a lower input current which translates into higher fanout.

CIRCUIT FEATURES

Circuit features of LS and FAST are best understood by examining the TTL 2-input NAND gate of each family (Figures 2-1a, b). The input/output circuits of other functions are almost identical.

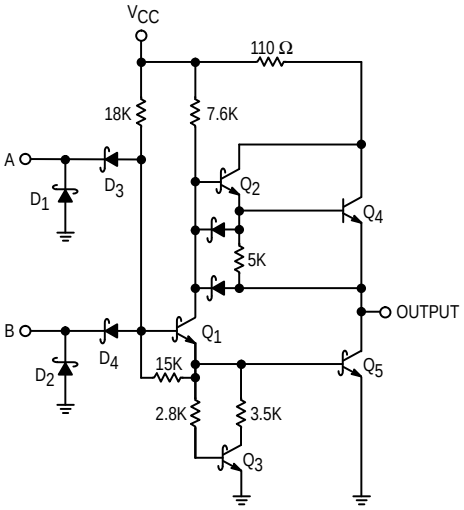


Figure 2-1a. LS00 — 2-Input NAND Gate

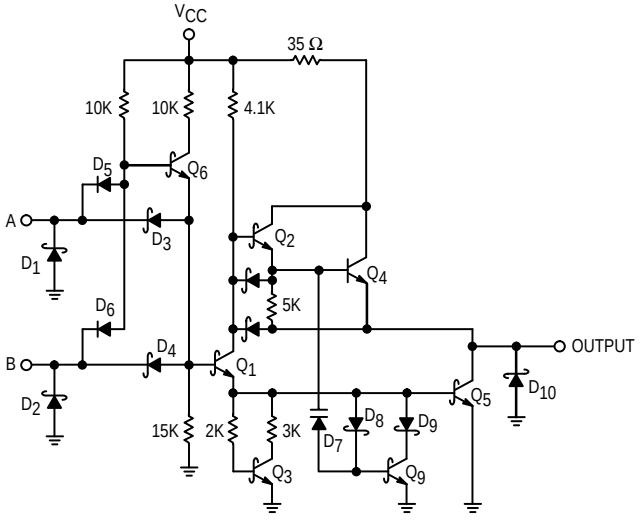


Figure 2-1b. F00 — 2-Input NAND Gate

INPUT CONFIGURATION. Motorola LSTTL circuits do not use the multi-emitter input structure that originally gave TTL its name. Most LS elements use a DTL type input circuit with Schottky diodes to perform the AND function, as exemplified by D3 and D4 in Figure 2-1a. Compared to the classical multi-emitter structure, this circuit is faster and increases the input breakdown voltage. Inputs of this type are tested for leakage with an applied input voltage of 7.0 V and the input breakdown voltage is typically 15 V or more.

The F00 input configuration utilizes a PN diode (D5 and D6) rather than the PNP transistor. This is required due to the high speed response of FAST™ logic. The PNP transistor, a relatively large device in current bipolar logic technology, has an associated capacitance large enough to make the gate input susceptible to ac noise. The PN diode results in much better ac noise immunity at the expense of increased input current.

Another input arrangement often used in LS MSI has three diodes connected as shown in Figure 2-2. This configuration gives a slightly higher input threshold than that of Figure 2-1a. A third input configuration that is sometimes used in LS TTL employs a vertical PNP transistor as shown in Figure 2-3. This arrangement also gives a higher input threshold and has the additional advantage of reducing the amount of current that the signal source must sink. Both the diode cluster arrangement and the PNP input configuration have breakdown voltage ratings greater than 7.0 V.

All inputs are provided with clamping diodes, exemplified by D1 and D2 in Figure 2-1a, b. These diodes conduct when an input signal goes negative, which limits undershoot and helps to control ringing on long signal lines following a HIGH-to-LOW transition. These diodes are intended only for the suppression of transient currents and should not be used as steady-state clamps in interface applications. A clamp current exceeding 2.0 mA and with a duration greater than 500 ns can activate a parasitic lateral NPN transistor, which in turn can steal current from internal nodes of an LS circuit and thus cause logic errors.

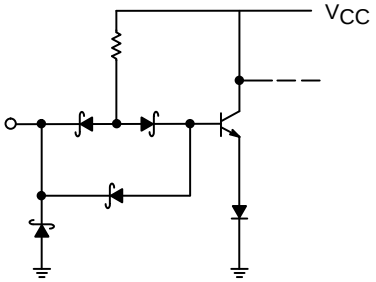


Figure 2-2. Diode Cluster Input

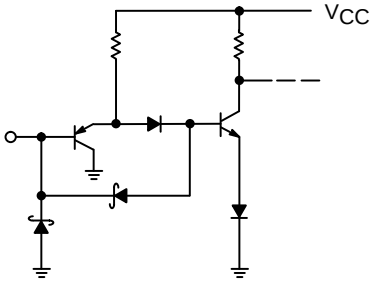


Figure 2-3. PNP Input

INPUT CHARACTERISTICS — Figure 2-4 shows the typical input characteristics of LS and FAST™. Typical transfer characteristics can be found in Figure 2-5 and input threshold variation with temperature information is provided in Table 2-1.

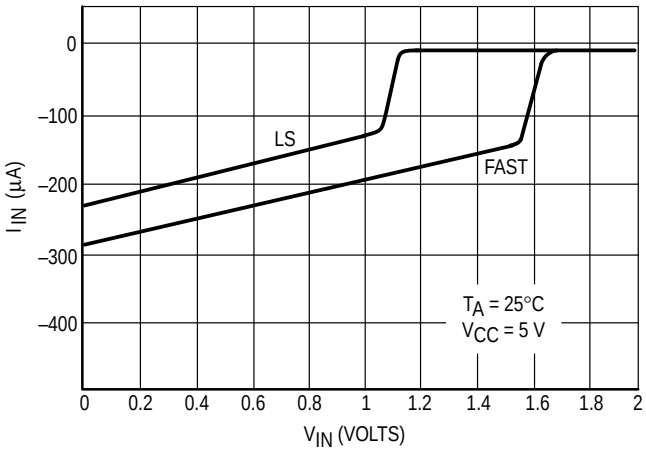


Figure 2-4. Typical Input Current versus Input Voltage

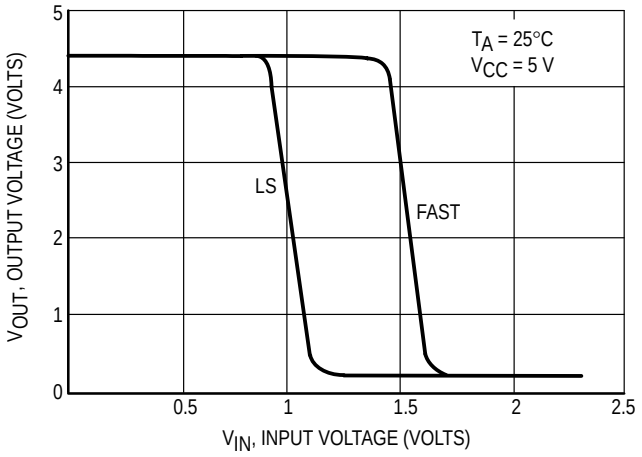


Figure 2-5. Typical Output versus Input Voltage Characteristic

Table 2.1
Typical Input Threshold Variation With Temperature

	−55°C	+25°C	+125°C
FAST	1.8	1.5	1.3
ALS	1.8	1.5	1.3
S	1.5	1.3	1.1
LS	1.2	1.0	0.8

OUTPUT CONFIGURATION. The output circuitry of LSTTL has several features not found in conventional TTL. A few of these features are discussed below.

Referring to Figures 2-1a, b, the base of the pull-down output transistor Q5 is returned to ground through Q3 and a pair of resistors instead of through a simple resistor. This arrangement is called a squaring network since it squares up the transfer characteristics (Figure 2-5) by preventing conduction in the phase splitter Q1 until the input voltage rises high enough to allow Q1 to supply base current to Q5. The squaring network also improves the propagation delay by providing a low resistance path to discharge capacitance at the base of Q5 during turn-off.

The output pull-up circuit is a 2-transistor Darlington circuit with the base of the output transistor returned through a 5.0K resistor to the output terminals, unlike 74H and 74S where it is returned to ground which is a more power consuming configuration. This configuration allows the output to pull up to one V_{BE} below V_{CC} for low values of output current.

The F00 output includes clamping diodes to limit undershoot and control ringing on long signal lines. As with the input diode clamps, these diodes are intended for transient suppression only and should not be used as steady-state clamps.

The F00 output configuration also includes additional circuitry to improve the rise time and decrease the power consumption at high operating frequencies. This circuit, which consists of Q9, D7, D8, and D9 causes Q5 to off more quickly on LOW to HIGH output transitions.

Figure 2-6 shows the extra circuitry used to obtain the “high Z” condition in 3-state outputs. When the Output Enable signal is HIGH, both the phase splitter and the Darlington pull-up are turned off. In this condition the output circuitry is non-conducting, which allows the outputs of two or more such circuits to be connected together in a bus application wherein only one output is enabled at any particular time.

FAST™ 3-state outputs have some additional circuitry due to the nature of the environment in which they are used. The effective capacitive load of a 3-state output tends to increase at high bus rates. The addition of Q10 reduces this effect by clamping the base of Q5 low when the device is in the high impedance state. In the high Z state, the output capacitance is about 5.0 pF for 24 mA outputs and about 12 pF for 64 mA outputs.

An additional feature of many FAST™ 3-state devices is the incorporation of power-up circuitry to guarantee that the output will not sink current if the device is disabled during the application or removal of power.

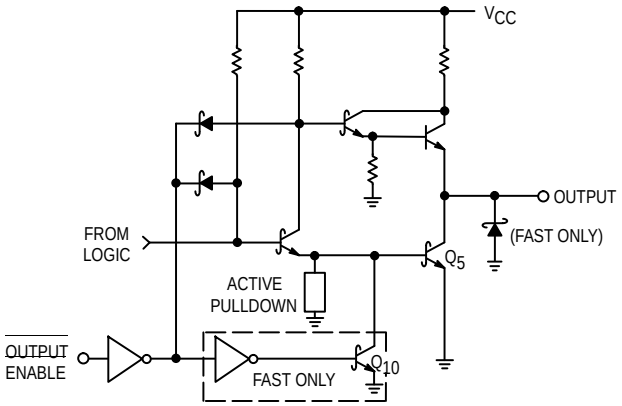


Figure 2-6. Typical 3-State Output Control

OUTPUT CHARACTERISTICS. Figure 2-7 shows the LOW-state output characteristics for LS and FAST™. For LOW I_{OL} values, the pull-down transistor is clamped out of deep saturation to shorten the turn-off delay. Figure 2-8 shows the HIGH-state output characteristics.

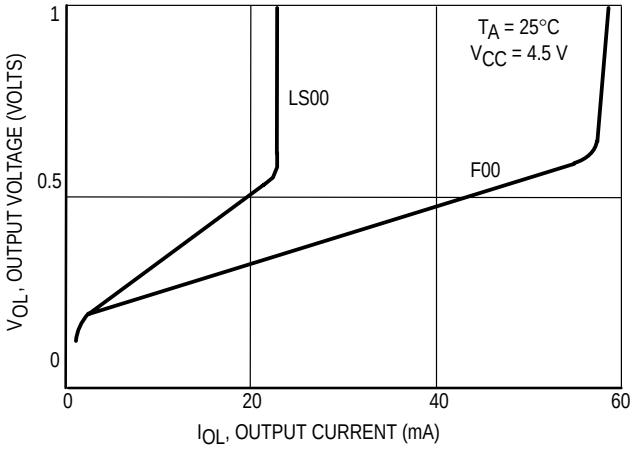


Figure 2-7a. Output Low Characteristic

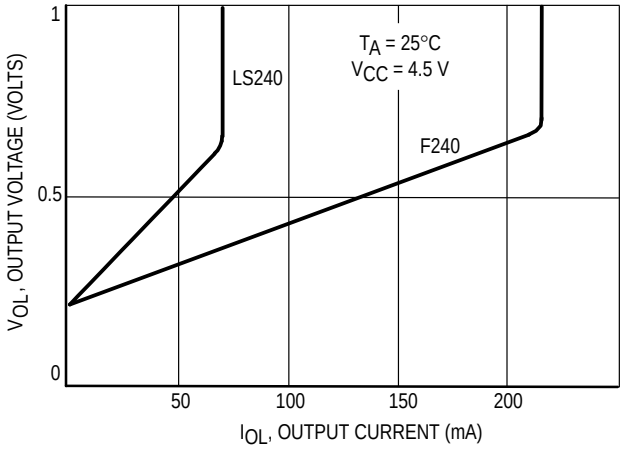


Figure 2-7b. Output Low Characteristic

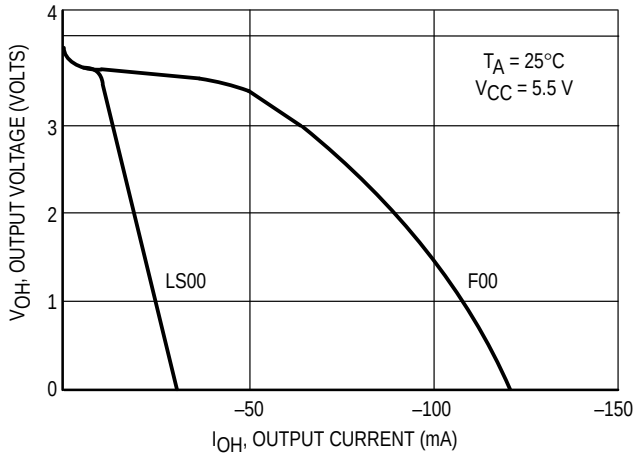


Figure 2-8a. Output High Characteristic

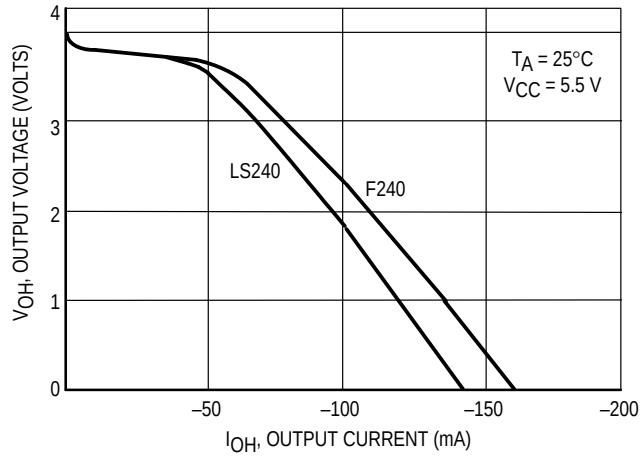


Figure 2-8b. Output High Characteristic

AC SWITCHING CHARACTERISTICS. The propagation through a logic element depends on power supply voltage, ambient temperature, and output load. The effect of each of these parameters on ac propagation is shown in Figures 2-9 through 2-11.

Propagation delays are specified with only one output switching, the delay through a logic-element will increase to some extent when multiple outputs switch simultaneously due to inductance internal to the IC package. This effect can be seen by comparing Figures 2-11c and 2-11d.

For LS TTL, limits are guaranteed at 25°C, V_{CC} = 5.0 V, and C_L = 15 pF (normally, resistive load has minimal effect on propagation delay) FAST™ and TTL limits are guaranteed over the commercial or military temperature and supply voltage ranges and with C_L = 50 pF.

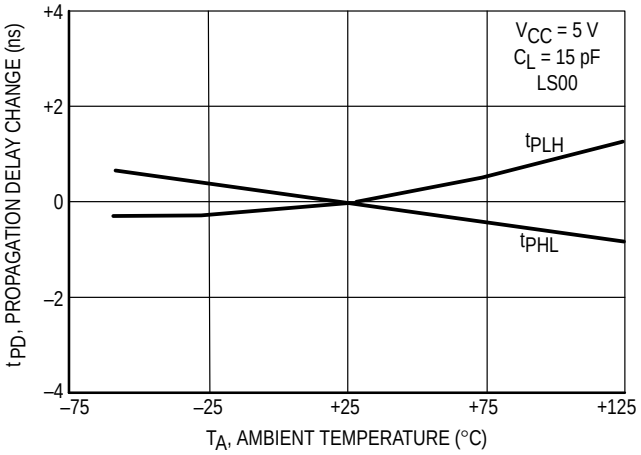


Figure 2-9

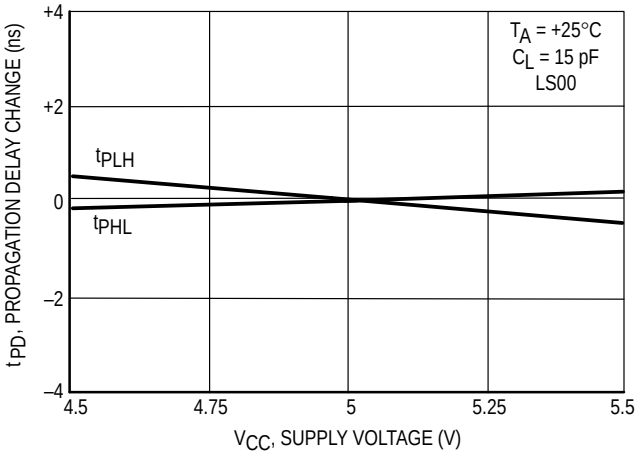


Figure 2-10

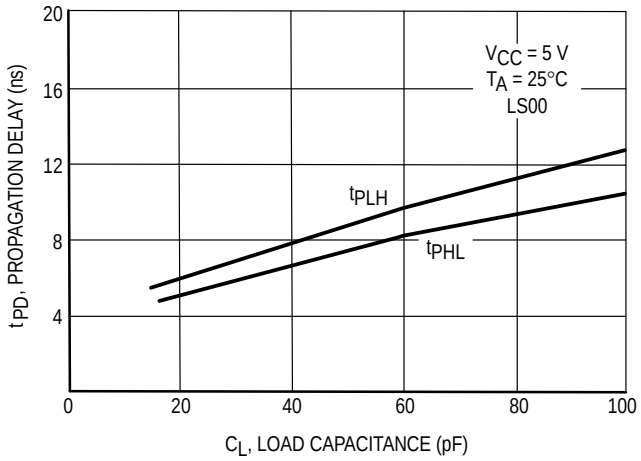


Figure 2-11a*

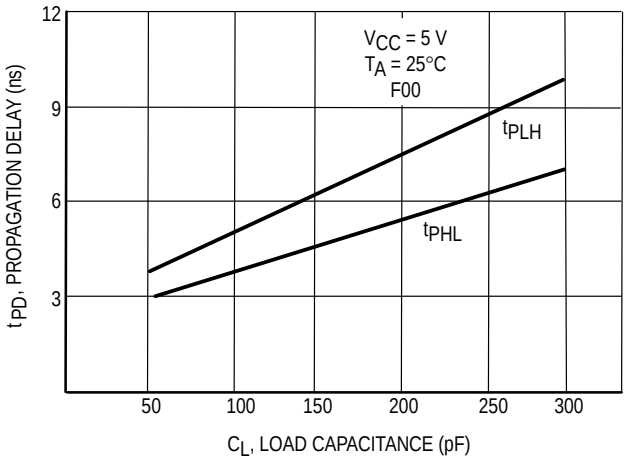


Figure 2-11b*

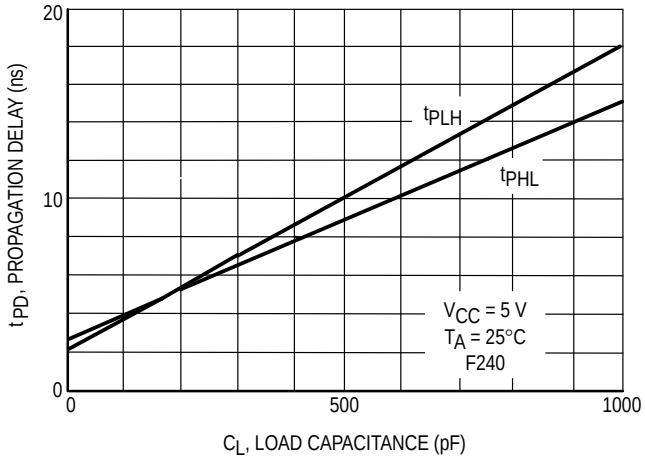


Figure 2-11c*

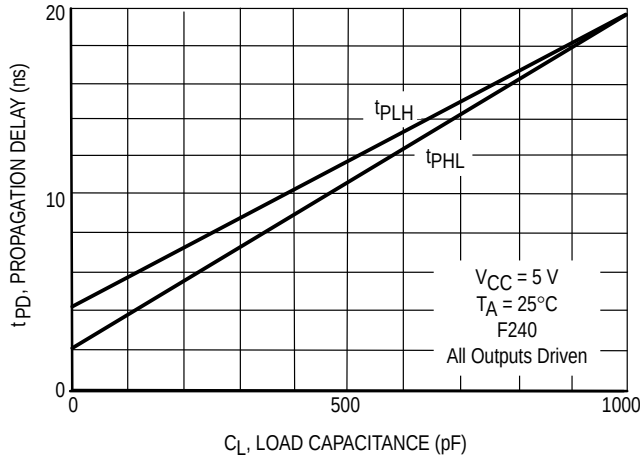


Figure 2-11d*

*Data for Figures 2-11a through 2-11c was taken with only one output switching at a time. Figure 2-11d data was taken with all 8 inputs of the F240 tied together.

LS/FAST ESD CHARACTERISTICS. Electrostatic Discharge (ESD) sensitivity for Motorola TTL is characterized using several methodologies (HBM, MM, CDM). It is extremely important to understand that ESD sensitivity values alone are not sufficient when comparing devices. In an attempt to reduce correlation problems between various pieces of test equipment, all of which meet Mil-Std-883C requirements, tester specific information as well as actual device ESD hardness levels are given in controlled documents and are available upon request. The continuing improvements of ESD sensitivity through redesigns of Motorola TTL has resulted in minimum ESD levels for all new products and redesigns of >4000 volts for FAST and >3500 volts for LS. For device specific values reference the following specifications:

LS: 12MRM 93831A
FAST: 12MRM 93830A