# M54/74HC242 M54/74HC243

## QUAD BUS TRANSCEIVER (3-STATE)

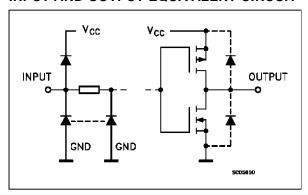
- HIGH SPEED tpD = 9 ns (TYP.) AT VCC = 5 V
- LOW POWER DISSIPATION  $I_{CC} = 4 \mu A \text{ (MAX.)}$  AT 25 °C
- OUTPUT DRIVE CAPABILITY
   15 LSTTL LOADS
- BALANCED PROPAGATION DELAYS tplh = tphl
- SYMMETRICAL OUTPUT IMPEDANCE IOL = IOH = 6 mA (MIN.)
- HIGH NOISE IMMUNITY

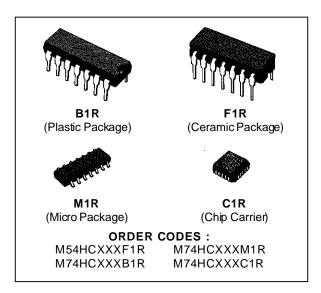
  VNIH = VNIL = 28 % Vcc (MIN.)
- WIDE OPERATING VOLTAGE RANGE V<sub>CC</sub> (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS242/243

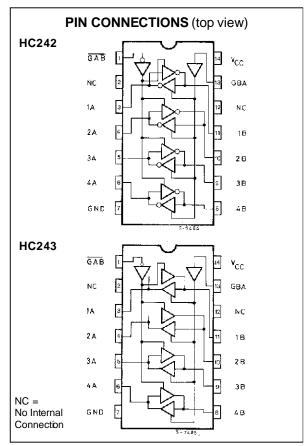
#### **DESCRIPTION**

The M54/74HC242/243 are high speed CMOS TRANSCEIVER (3-STATE) QUAD BUS FABRICATED IN SILICON GATE C<sup>2</sup>MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The HC242/243 are 3 STATE bi-directional inverting and non-inverting buffers and are intended for two-way asynchronous communication between data buses. They are high drive current outputs which enable high speed operation when driving large bus capacitances. Each device has one active high enable (GBA), and one active low enable (GAB). GBA enables the A outputs and GAB enables the B outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

#### INPUT AND OUTPUT EQUIVALENT CIRCUIT

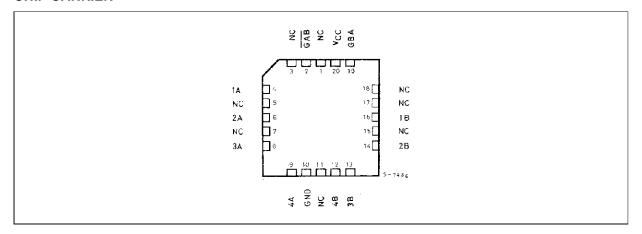






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#### **CHIP CARRIER**



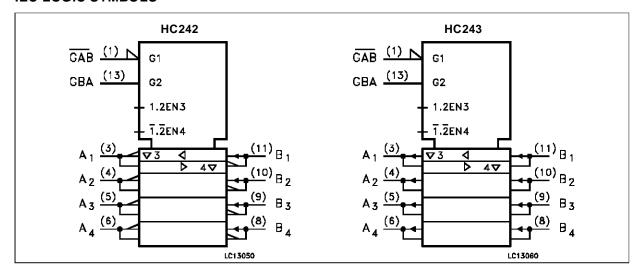
#### **TRUTH TABLE**

INP	UTS	FUNC	TION	OUTPUTS		
GAB	GBA	A BUS	B BUS	HC242	HC243	
Н	Н	OUTPUT	INPUT	$A = \overline{B}$	A = B	
L	L	INPUT	OUTPUT	$B = \overline{A}$	B = A	
Н	L	HIGH IMF	PEDANCE	Z	Z	
L	Н	HIGH IME	PEDANCE	Z	Z	

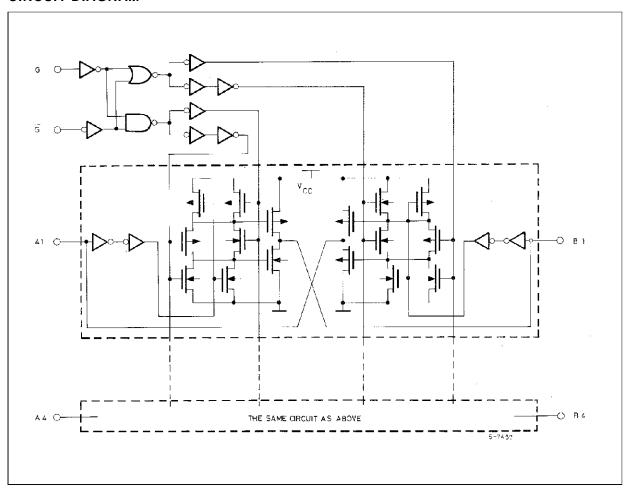
## PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	GAB	Output Enable Input (active LOW)
2, 12	NC	Not connected
3, 4, 5, 6	1A to 4A	Data Inputs/Outputs
11, 10, 9, 8	1B to 4B	Data Inputs/Outputs
13	GBA	Output Enable Input
7	GND	Ground (0V)
14	Vcc	Positive Supply Voltage

### **IEC LOGIC SYMBOLS**



### **CIRCUIT DIAGRAM**



## **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7	V
VI	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
Vo	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
lok	DC Output Diode Current	± 20	mA
Io	DC Output Source Sink Current Per Output Pin	± 35	mA
Icc or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 70	mA
PD	Power Dissipation	500 (*)	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied. (\*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C



## **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter		Value	Unit
Vcc	Supply Voltage		2 to 6	V
VI	Input Voltage		0 to V <sub>CC</sub>	V
Vo	Output Voltage		0 to V <sub>CC</sub>	V
Тор	Operating Temperature: <b>M54HC</b> Series <b>M74HC</b> Series		-55 to +125 -40 to +85	o° o°
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> = 2 V	0 to 1000	ns
		$V_{CC} = 4.5 \text{ V}$	0 to 500	
		$V_{CC} = 6 V$	0 to 400	

### **DC SPECIFICATIONS**

		Test Conditions			Value							
Symbol	Parameter	V <sub>CC</sub>							o 85 °C  -55 to 125 °C 4HC   54HC			Unit
		( )			Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
$V_{IH}$	High Level Input	2.0			1.5			1.5		1.5		
	Voltage	4.5			3.15			3.15		3.15		V
		6.0			4.2			4.2		4.2		
$V_{IL}$	Low Level Input	2.0					0.5		0.5		0.5	
	Voltage	4.5					1.35		1.35		1.35	V
		6.0					1.8		1.8		1.8	
$V_{OH}$	High Level	2.0	V <sub>I</sub> =		1.9	2.0		1.9		1.9		
	Output Voltage	4.5	VI =	I <sub>O</sub> =-20 μA	4.4	4.5		4.4		4.4		
	6.0	or		5.9	6.0		5.9		5.9		V	
		4.5	VIL	I <sub>O</sub> =-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I <sub>O</sub> =-7.8 mA	5.68	5.8		5.63		5.60		
$V_{OL}$	Low Level Output	2.0	V <sub>I</sub> =			0.0	0.1		0.1		0.1	
	Voltage	4.5	VI =	I <sub>O</sub> = 20 μA		0.0	0.1		0.1		0.1	
		6.0	or			0.0	0.1		0.1		0.1	V
		4.5	V <sub>IL</sub>	I <sub>O</sub> = 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I <sub>O</sub> = 7.8 mA		0.18	0.26		0.33		0.40	
lı	Input Leakage Current	6.0	V <sub>I</sub> = '	Vcc or GND			±0.1		±1		±1	μΑ
loz	3 State Output Off-state Current	6.0	$V_I = V_{IH} \text{ or } V_{IL}$ $V_O = V_{CC} \text{ or GND}$				±0.5		±5		±10	μΑ
Icc	Quiescent Supply Current	6.0	V <sub>I</sub> = '	√cc or GND			4		40		80	μΑ

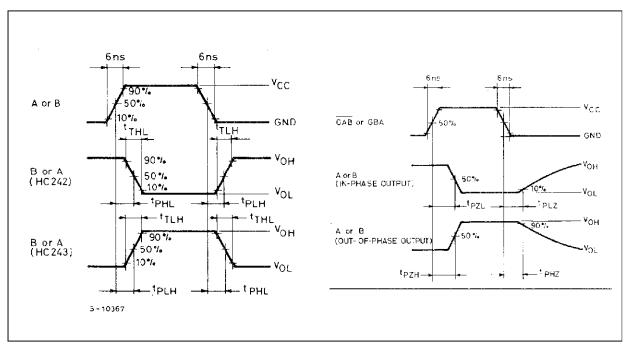


## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6 \text{ ns}$ )

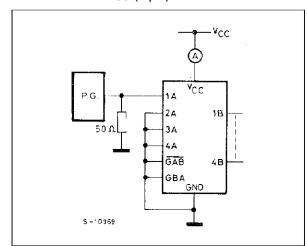
		Test Conditions			Value										
Symbol Parameter		V <sub>CC</sub>	C <sub>L</sub>			<sub>A</sub> = 25 <sup>c</sup> C and 7		1	85 °C HC		125 °C HC	Unit			
	(V)	(pF)		Min.	Тур.	Max.	Min.	Max.	Min.	Max.					
t <sub>TLH</sub>	Output Transition	2.0				25	60		75		90				
$t_{THL}$	Time	4.5	50			7	12		15		18	ns			
		6.0				6	10		13		15				
t <sub>PLH</sub>	Propagation	2.0				39	90		115		135				
$t_{PHL}$	Delay Time	4.5	50			13	18		23		27	ns			
		6.0				11	15		20		23				
		2.0				51	145		180		220				
		4.5	150			17	29		36		44	ns			
		6.0				14	25		31		37				
$t_{PZL}$	3 State Output	2.0				57	145		180		220				
t <sub>PZH</sub>	Enable Time	4.5	50	$0   R_L = 1 K\Omega$	$R_L = 1 K\Omega$	$R_L = 1 K\Omega$	$0 \mid R_L = 1 \text{ K}\Omega$		18	29		36		44	ns
		6.0				15	25		31		37				
		2.0				70	175		220		265				
		4.5	150	$R_L = 1 K\Omega$		22	35		44		53	ns			
		6.0				19	30		37		45				
t <sub>PLZ</sub>	3 State Output	2.0				45	150		190		225				
$t_{PHZ}$	Disable Time	4.5	50	$R_L = 1 K\Omega$		20	30		38		45	ns			
		6.0				17	26		32		38				
C <sub>IN</sub>	Input Capacitance					5	10		10		10	pF			
C <sub>PD</sub> (*)	Power Dissipation Capacitance			r HC242 r HC243		30 35						рF			

<sup>(\*)</sup>  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$ 

#### SWITCHING CHARACTERISTICS TEST WAVEFORM



## TEST CIRCUIT Icc (Opr.)



#### **CCP CALCULATION**

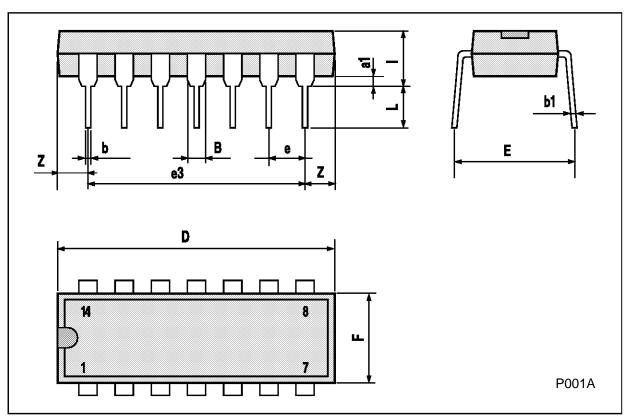
C<sub>PD</sub> is to be calculated with the following formula by using the measured value of ICC (Opr.) in the test circuit opposite

$$C_{PD} = \frac{I_{CC} (Opr.)}{f_{IN} x V_{CC}}$$

In determining the typical value of CPD, a relatively high frequency of 1MHz was applied to fIN, in order to eliminate any error caused by the quiescent supply current.

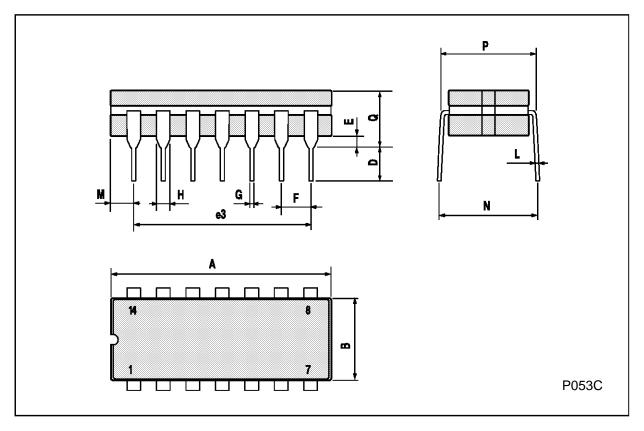
# Plastic DIP14 MECHANICAL DATA

DIM.		mm			inch			
Diwi.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
a1	0.51			0.020				
В	1.39		1.65	0.055		0.065		
b		0.5			0.020			
b1		0.25			0.010			
D			20			0.787		
E		8.5			0.335			
е		2.54			0.100			
e3		15.24			0.600			
F			7.1			0.280		
I			5.1			0.201		
L		3.3			0.130			
Z	1.27		2.54	0.050		0.100		



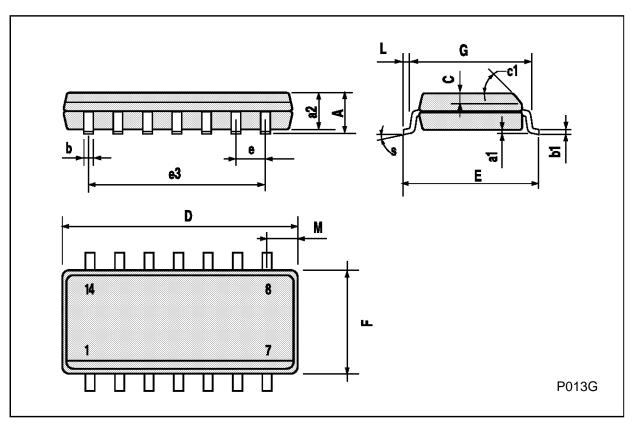
# **Ceramic DIP14/1 MECHANICAL DATA**

DIM.		mm		inch			
DIWI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Α			20			0.787	
В			7.0			0.276	
D		3.3			0.130		
E	0.38			0.015			
e3		15.24			0.600		
F	2.29		2.79	0.090		0.110	
G	0.4		0.55	0.016		0.022	
Н	1.17		1.52	0.046		0.060	
L	0.22		0.31	0.009		0.012	
M	1.52		2.54	0.060		0.100	
N			10.3			0.406	
Р	7.8		8.05	0.307		0.317	
Q			5.08			0.200	



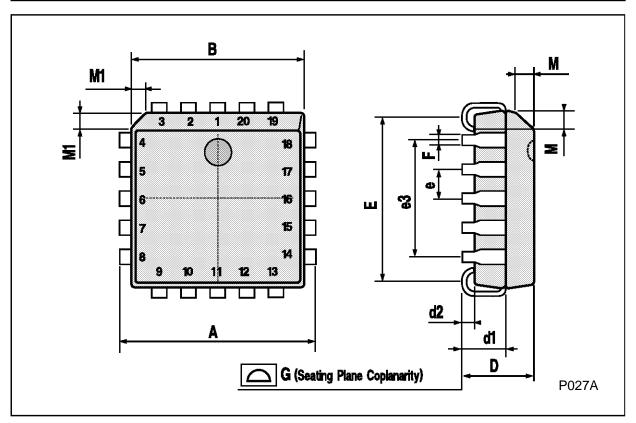
# **SO14 MECHANICAL DATA**

DIM.		mm			inch		
DIIVI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
А			1.75			0.068	
a1	0.1		0.2	0.003		0.007	
a2			1.65			0.064	
b	0.35		0.46	0.013		0.018	
b1	0.19		0.25	0.007		0.010	
С		0.5			0.019		
c1			45°	(typ.)			
D	8.55		8.75	0.336		0.344	
Е	5.8		6.2	0.228		0.244	
е		1.27			0.050		
e3		7.62			0.300		
F	3.8		4.0	0.149		0.157	
G	4.6		5.3	0.181		0.208	
L	0.5		1.27	0.019		0.050	
М			0.68			0.026	
S			8° (ı	max.)			



## PLCC20 MECHANICAL DATA

DIM.		mm		inch		
Diwi.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α	9.78		10.03	0.385		0.395
В	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
е		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
М		1.27			0.050	
M1		1.14			0.045	



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