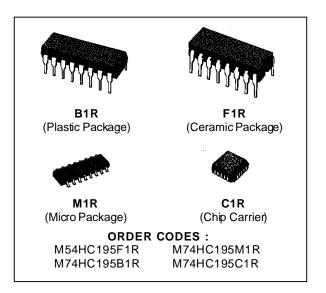


#### 8 BIT PIPO SHIFT REGISTER

- HIGH SPEED
- $t_{PD} = 13 \text{ ns} (TYP.) \text{ at } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION I<sub>CC</sub> = 4 μA (MAX.) at T<sub>A</sub> = 25 °C 6 V
- HIGH NOISE IMMUNITY

  VNIH = VNIL = 28 % VCC (MIN.)
- OUTPUT DRIVE CAPABILITY 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE | I<sub>OH</sub> | = I<sub>OL</sub> = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS tplh = tphl
- WIDE OPERATING VOLTAGE RANGE V<sub>CC</sub> (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS195



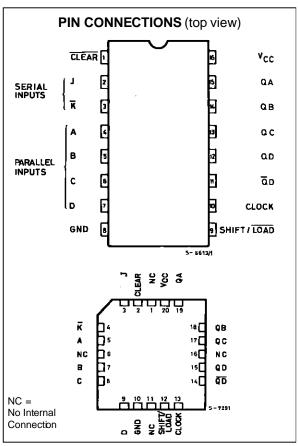
#### **DESCRIPTION**

The M54/74HC195 is a high speed CMOS 4 BIT PIPO SHIFT REGISTER fabricated in silicon gate C<sup>2</sup>MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This shift register features parallel inputs, parallel outputs, J-K serial inputs, a SHIFT/LOAD control input, and a direct overriding CLEAR. This shift register can operate in two modes: Parallel Load; Shift from QA towards QD.

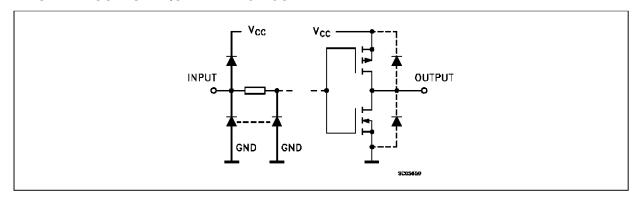
Parallel loading is accomplished by applying the four bits of data, and taking the SHIFT/LOAD control input low. The data is loaded into the associated flip flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the SHIFT/LOAD control input is high. Serial data for this mode is entered at the J-K inputs. These inputs allow the first stage to perform as a J-K or TOGGLE flip flop as shown in the truthtable.

All inputs are equipped with protection circuits against static discharge transient excess voltage.



October 1992 1/13

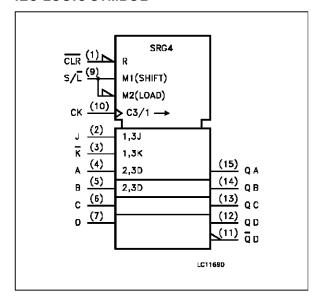
#### INPUT AND OUTPUT EQUIVALENT CIRCUIT



#### **PIN DESCRIPTION**

PIN No	SYMBOL	NAME AND FUNCTION
1	CLEAR	Reset Input (Active LOW)
2	J	First Stage J Input (Active LOW)
3	K	First Stage $\overline{K}$ Input (Active LOW)
4, 5, 6, 7	A to D	Parallel Data Input
9	SHIFT/LOAD	Control Input
10	CLOCK	Clock Input (LOW to HIGH Edge-triggered)
11	QD	Inverted Output From The Last Stage
15, 14, 13, 12	QA to QD	Paralle Outputs
8	GND	Ground (0V)
16	V <sub>CC</sub>	Positive Supply Voltage

#### **IEC LOGIC SYMBOL**



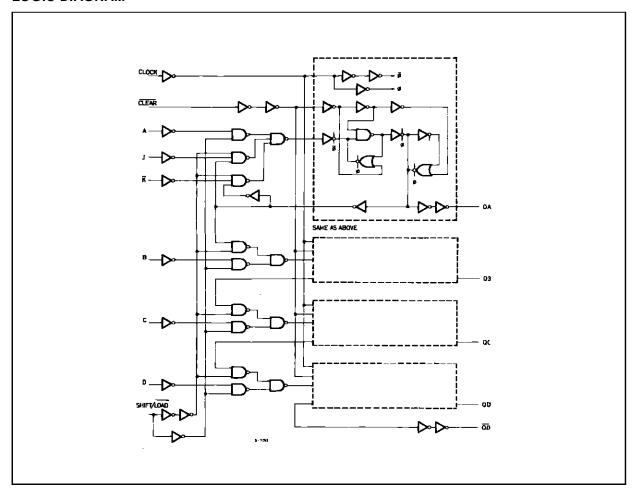
#### **TRUTH TABLE**

INPUTS									OUTPUS				
CLEAR	SHIFT/	СГОСК	SER	RIAL		PARA	LLEL		QA	QB	QC	QD	$\overline{Q}D$
	LOAD	CLOCK	J	K	Α	В	С	D	Ψ.Λ	Q D	QC	QD.	עש
L	Х	Х	Χ	Х	Χ	Χ	Χ	Χ	L	L	L	┙	Ш
Н	L		X	Х	а	b	С	d	а	b	С	d	d
Н	Н		Х	Х	Х	Χ	Х	Х	QA0	QB0	QC0	QD0	QD0
Н	Н		L	Н	Χ	Χ	Х	Χ	QA0	QA0	QBn	QCn	QCn
Н	Н		L	L	Х	Х	Х	Х	L	QAn	QBn	QCn	QCn
Н	Н		Н	Н	Χ	Χ	Х	Х	Н	QAn	QBn	QCn	QCn
Н	Н		Н	L	Х	Х	Х	Х	QAn	QAn	QBn	QCn	QCn

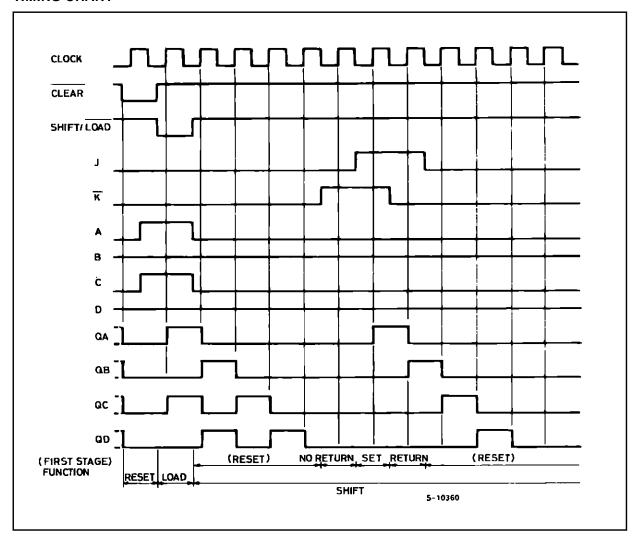
X: Don't Care: The level of QA, QB, QC, respectively, before the mst recent positive transition of the clock.



#### **LOGIC DIAGRAM**



#### **TIMING CHART**



#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
Vcc	Supply Voltage	-0.5 to +7	V
VI	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
Vo	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
lok	DC Output Diode Current	± 20	mA
lo	DC Output Source Sink Current Per Output Pin	± 25	mA
Icc or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 50	mA
P <sub>D</sub>	Power Dissipation	500 (*)	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
TL	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied. (\*) 500 mW:  $\cong$  65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter		Value	Unit
$V_{CC}$	Supply Voltage		2 to 6	V
$V_{I}$	Input Voltage		0 to V <sub>CC</sub>	V
Vo	Output Voltage		0 to V <sub>CC</sub>	V
$T_{op}$	Operating Temperature: <b>M54HC</b> Series <b>M74HC</b> Series		-55 to +125 -40 to +85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	$V_{CC} = 2 V$	0 to 1000	ns
		$V_{CC} = 4.5 \text{ V}$	0 to 500	
		$V_{CC} = 6 V$	0 to 400	

#### **DC SPECIFICATIONS**

		To	est Co	nditions	Value								
Symbol	Parameter	Vcc			T <sub>A</sub> = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		Unit	
		(V)			Min.	Тур.	Max.	Min.	Max.	Min.	Max.		
$V_{IH}$	High Level Input	2.0			1.5			1.5		1.5			
	Voltage	4.5			3.15			3.15		3.15		V	
		6.0			4.2			4.2		4.2			
$V_{IL}$	Low Level Input	2.0					0.5		0.5		0.5		
	Voltage	4.5					1.35		1.35		1.35	V	
		6.0					1.8		1.8		1.8		
$V_{OH}$		2.0	Vı =		1.9	2.0		1.9		1.9			
Output Voltage	4.5	VI –	'   la=-'2()     /\	4.4	4.5		4.4		4.4				
		6.0	VIH		5.9	6.0		5.9		5.9		V	
		4.5	V <sub>IL</sub>	I <sub>O</sub> =-4.0 mA	4.18	4.31		4.13		4.10			
		6.0		I <sub>O</sub> =-5.2 mA	5.68	5.8		5.63		5.60			
$V_{OL}$	Low Level Output	2.0	Vı =			0.0	0.1		0.1		0.1		
	Voltage	4.5	V <sub>I</sub> –	I <sub>O</sub> = 20 μA		0.0	0.1		0.1		0.1		
		6.0	or			0.0	0.1		0.1		0.1	V	
		4.5	VIL	I <sub>O</sub> = 4.0 mA		0.17	0.26		0.33		0.40		
		6.0		I <sub>O</sub> = 5.2 mA		0.18	0.26		0.33		0.40		
lı	Input Leakage Current	6.0	Vı = '	Vcc or GND			±0.1		±1		±1	μΑ	
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = '	V <sub>CC</sub> or GND			4		40		80	μΑ	

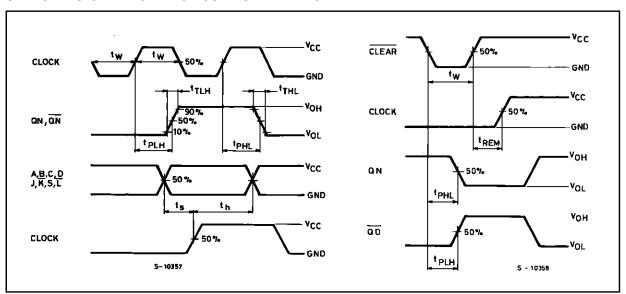
### AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

		Test Conditions				Value				
Symbol	Parameter	Vcc		A = 25 C C and		1	85 °C HC		125 °C HC	Unit
		(V)	Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
t <sub>TLH</sub>	Output Transition	2.0		30	75		95		115	
$t_{THL}$	Time	4.5		8	15		19		23	ns
		6.0		7	13		16		20	
t <sub>PLH</sub>	Propagation	2.0		48	125		155		190	
t <sub>PHL</sub>	Delay Time	4.5		16	25		31		38	ns
	(CLOCK- Qn, $\overline{QD}$ )	6.0		14	21		26		32	
t <sub>PLH</sub>	Propagation	2.0		45	120		150		180	
$t_{PHL}$	Delay Time	4.5		15	24		30		36	ns
	$(\overline{CLEAR}\text{-}Qn,\overline{QD})$	6.0		13	20		26		31	
$f_{MAX}$	Maximum Clock	2.0	7.6	15		6		5		
	Frequency	4.5	38	60		30		25		MHz
		6.0	45	71		35		30		
t <sub>W(H)</sub>	t <sub>W(L)</sub> Width	2.0		20	75		95		115	
$t_{W(L)}$		4.5		5	15		19		23	ns
(CLOCK)	6.0		4	13		16		20		
t <sub>W(L)</sub>	Minimum Pulse	2.0		20	75		95		115	
	Width	4.5		5	15		19		23	ns
	(CLEAR)	6.0		4	13		16		20	
ts	Minimum Set-up	2.0		28	75		95		115	
	Time	4.5		7	15		19		23	ns
	(PI)	6.0		6	13		16		20	
ts	Minimum Set-up	2.0		28	75		95		115	
	Time	4.5		7	15		19		23	ns
	$(J, \overline{K}, S/\overline{L})$	6.0		6	13		16		20	
th	Minimum Hold	2.0			0		0		0	
Time	4.5			0		0		0	ns	
		6.0			0		0		0	
$t_{REM}$	Minimum	2.0			5		5		5	
	Removal Time	4.5			5		5		5	ns
		6.0			5		5		5	
$C_{IN}$	Input Capacitance			5	10		10		10	pF
C <sub>PD</sub> (*)	Power Dissipation Capacitance			72						pF

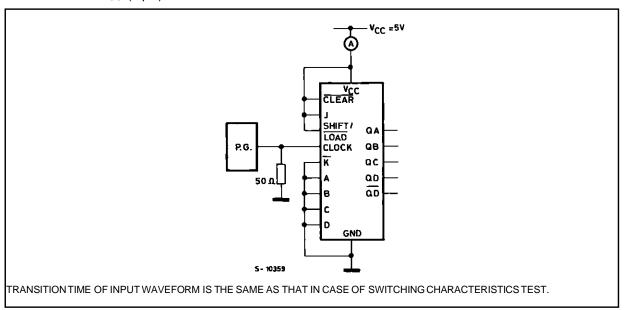
<sup>(\*)</sup>  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$ 



#### SWITCHING CHARACTERISTICS TEST WAVEFORM

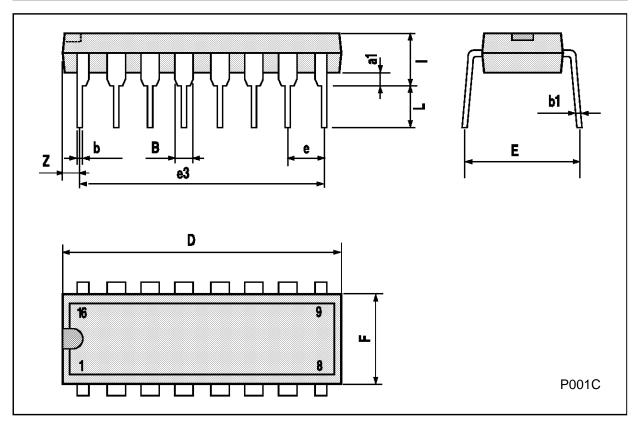


#### TEST CIRCUIT ICC (Opr.)



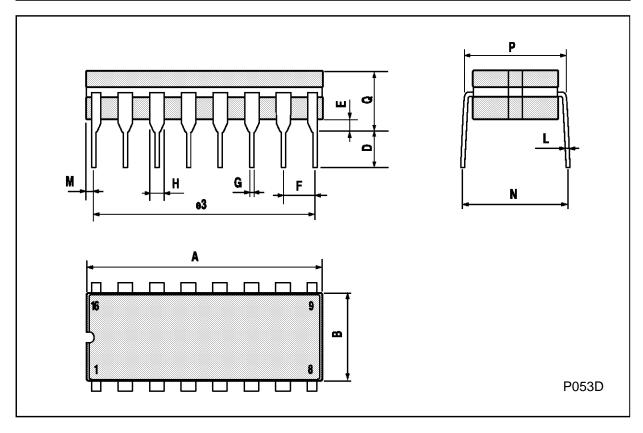
# Plastic DIP16 (0.25) MECHANICAL DATA

DIM.		mm			inch	
Diwi.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
В	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
е		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
ı			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



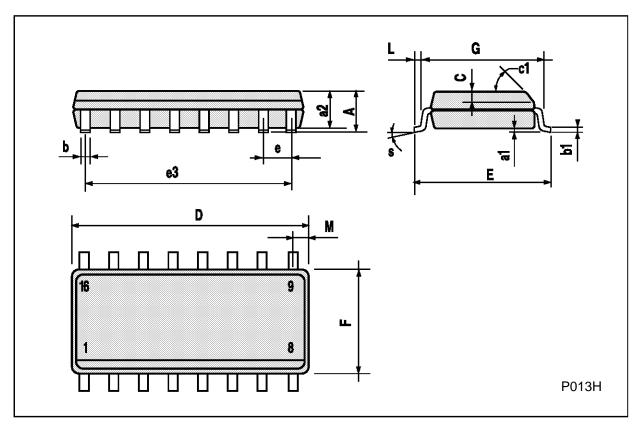
## **Ceramic DIP16/1 MECHANICAL DATA**

DIM.		mm		inch				
Diwi.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
А			20			0.787		
В			7			0.276		
D		3.3			0.130			
Е	0.38			0.015				
e3		17.78			0.700			
F	2.29		2.79	0.090		0.110		
G	0.4		0.55	0.016		0.022		
Н	1.17		1.52	0.046		0.060		
L	0.22		0.31	0.009		0.012		
М	0.51		1.27	0.020		0.050		
N			10.3			0.406		
Р	7.8		8.05	0.307		0.317		
Q			5.08			0.200		



# SO16 (Narrow) MECHANICAL DATA

DIM.		mm			inch	
DIIVI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
С		0.5			0.019	
c1			45°	(typ.)		
D	9.8		10	0.385		0.393
Е	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
М			0.62			0.024
S			8° (ı	max.)		



## **PLCC20 MECHANICAL DATA**

DIM.		mm		inch				
Diiii.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
А	9.78		10.03	0.385		0.395		
В	8.89		9.04	0.350		0.356		
D	4.2		4.57	0.165		0.180		
d1		2.54			0.100			
d2		0.56			0.022			
E	7.37		8.38	0.290		0.330		
е		1.27			0.050			
e3		5.08			0.200			
F		0.38			0.015			
G			0.101			0.004		
М		1.27			0.050			
M1		1.14			0.045			



Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsability for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may results from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectonics.

© 1994 SGS-THOMSON Microelectronics - All Rights Reserved

SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A

