DISCRETE SEMICONDUCTORS

DATA SHEET

BST82

N-channel enhancement mode vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995





BST82

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in SOT23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low R_{DS(on)}

QUICK REFERENCE DATA

Drain-source voltage	V _{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \le 2 \text{ ms}$)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	175 mA
Total power dissipation up to $T_{amb} = 25 ^{\circ}C$	P_{tot}	max.	300 mW
Drain-source ON-resistance			
$I_D = 150 \text{ mA}; V_{GS} = 5 \text{ V}$	R _{DS(on)}	typ.	7 Ω
	20(0)	max.	10 Ω
Transfer admittance			
$I_D = 175 \text{ mA}; V_{DS} = 5 \text{ V}$	Y _{fs}	typ.	150 mS

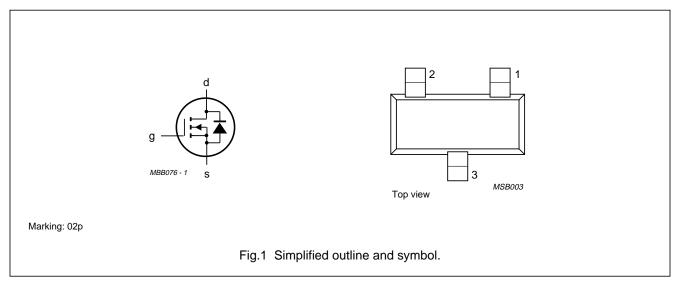
PINNING - SOT23

1 = gate

2 = source

3 = drain

PIN CONFIGURATION



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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \le 2 \text{ ms}$)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_{D}	max.	175	mΑ
Drain current (peak)	I_{DM}	max.	600	mΑ
Total power dissipation up to T _{amb} = 25 °C (note 1)	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	-65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1) $R_{th j-a} = 430 \text{ K/W}$

Note

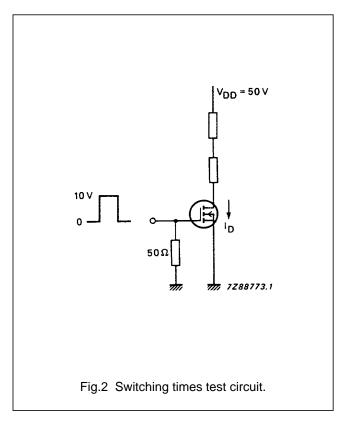
^{1.} Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0.7 mm.

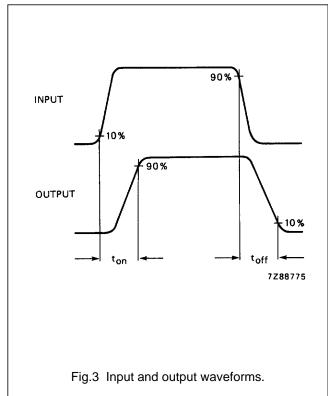
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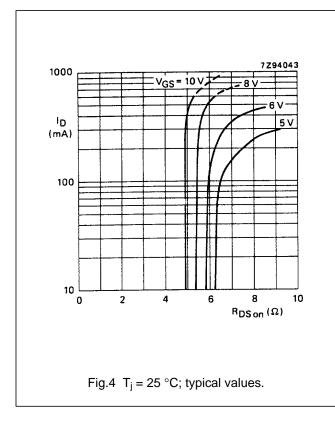
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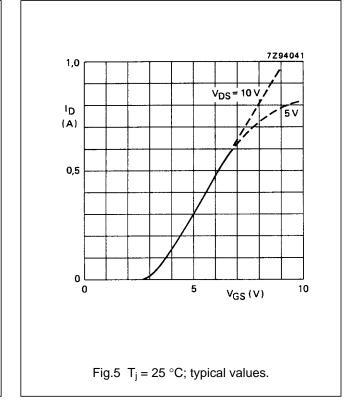
CHARACTERISTICS				
$T_j = 25$ °C unless otherwise specified				
Drain-source breakdown voltage				
$I_D = 10 \mu A; V_{GS} = 0$	$V_{(BR)DSS}$	min.	80	V
Drain-source leakage current				
$V_{DS} = 60 \text{ V}; V_{GS} = 0$	I_{DSS}	max.	1.0	μΑ
Gate-source leakage current				
$V_{GS} = 20 \text{ V}; V_{DS} = 0$	I_{GSS}	max.	100	nΑ
Gate-source cut-off voltage		i	4 5	\/
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$	$V_{(P)GS}$	min. max.	1.5 3.5	
Drain-source ON-resistance			_	_
$I_D = 150 \text{ mA}; V_{GS} = 5 \text{ V}$	R _{DS(on)}	typ.	7 10	Ω
	, ,	max.	10	22
Transfer admittance				
$I_D = 175 \text{ mA}; V_{DS} = 5 \text{ V}$	Y _{fs}	typ.	150	mS
Input capacitance at f = 1 MHz				
$V_{DS} = 10 \text{ V}; V_{GS} = 0$	C_{iss}	typ.		pF
		max.	30	pF
Output capacitance at f = 1 MHz		4	40	
$V_{DS} = 10 \text{ V}; V_{GS} = 0$	C_{oss}	typ. max.	13 20	•
		max.	20	P'
Feedback capacitance at f = 1 MHz				
$V_{DS} = 10 \text{ V}; V_{GS} = 0$	C_{rss}	typ.		pF
		max.	6	pF
Switching times (see Figs 2 and 3)		typ.	4	ns
$I_D = 175 \text{ mA}; V_{DD} = 50 \text{ V}; V_{GS} = 0 \text{ to } 10 \text{ V}$	t_on	max.	10	ns
	$t_{\sf off}$	typ. max.	4 10	ns ns
		max.	10	113

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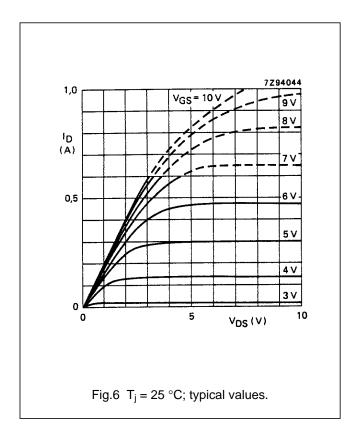


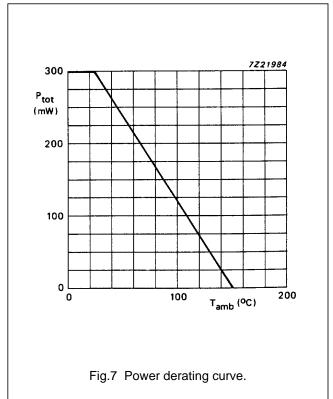


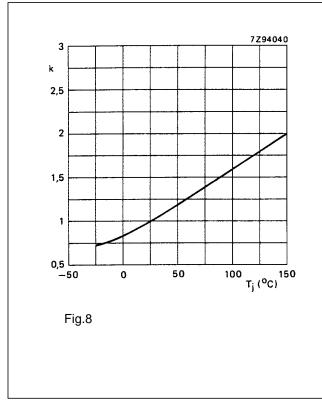


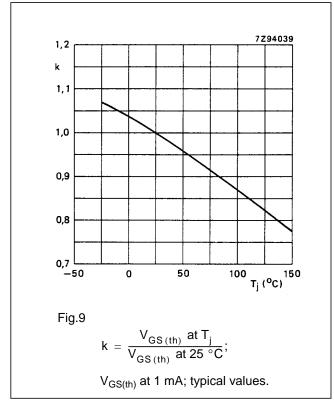


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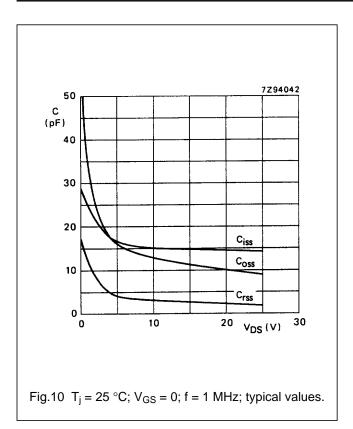






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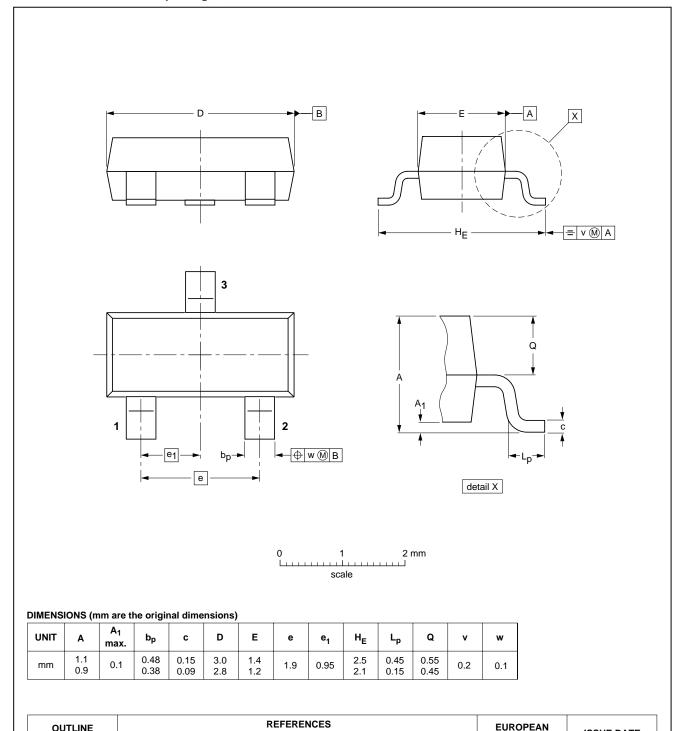


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PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT23



OUTLINE					BROUTOTION ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT23						97-02-28	

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DEFINITIONS

Data sheet status			
Objective specification This data sheet contains target or goal specifications for product development.			
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.		
Product specification	Product specification This data sheet contains final product specifications.		
Application information			
Where application information is given, it is advisory and does not form part of the specification.			

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NOTES

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Printed in The Netherlands

Date of release: April 1995

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