SCENIX

SX18AC75/SX20AC75/SX28AC75/SX20AC100/SX28AC100

High-Performance 8-Bit Microcontrollers with EE/Flash Program Memory and In-System Programming Capability

1.0 PRODUCT OVERVIEW

1.1 Introduction

The SX18AC75, SX20AC75, SX28AC75, SX20AC100 and SX28AC100 are members of the SX family of high-performance 8-bit microcontrollers fabricated in an advanced CMOS process technology. The advanced process, combined with a RISC-based architecture, allows high-speed computation, flexible I/O control, and efficient data manipulation. Throughput is enhanced by operating the device at frequencies up to 100MHz and by optimizing the instruction set to include mostly single-cycle instructions.

On-chip functions include a general-purpose 8-bit timer with prescaler, an analog comparator, a brown-out detector, a watchdog timer, a power-save mode with multi-source wakeup capability, an internal R/C oscillator, user-selectable clock modes, and high-current outputs.

1.2 Key Features

- 75 MIPS performance at 75 MHz oscillator frequency (SX18/20/28AC75)
- 100 MIPS performance at 100 MHz oscillator frequency (SX20/28AC100)
- 2048 x 12 bits EE/Flash program memory rated for 10,000 rewrite cycles
- 136 x 8 bits SRAM
- In-system programming capability through OSC pins
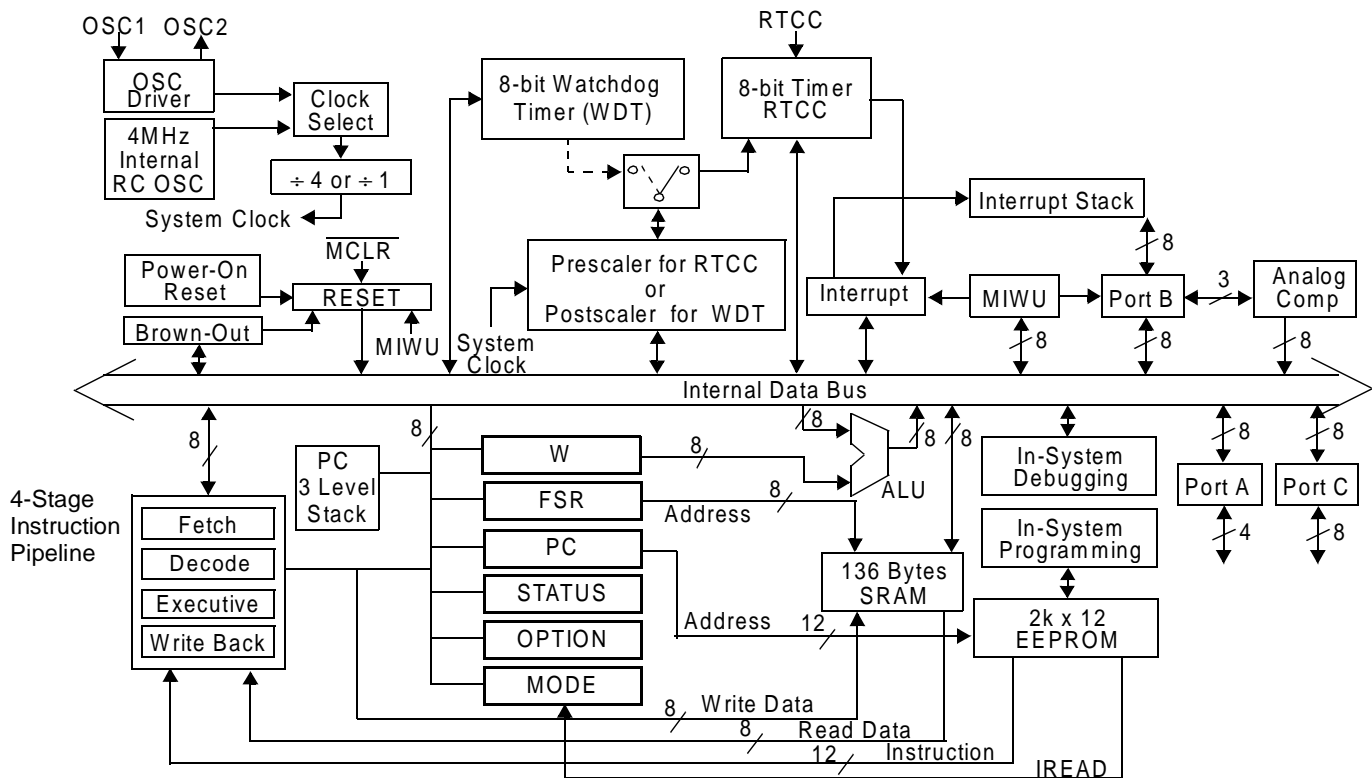- Internal RC oscillator with configurable rate from 31.25 KHz to 4 MHz, $\pm$8% accuracy

Figure 1-1. Block Diagram

1.2   Key Features (Continued)

- User selectable clock modes:
  - Internal RC oscillator
  - External oscillator
  - Crystal/resonator options
- External RC oscillator
- Analog comparator
- Brown-out detector (4.2V, on/off)
- Multi-Input Wakeup (MIWU) on eight pins
- Fast lookup capability through run-time readable code
- Complete development tool support available through Parallax

1.2.1 CPU Features

- Fully static design – DC to 100 MHz operation
- Fast instruction cycle time
  - 13.3 ns (SX18/20/28AC75)
  - 10 ns (SX20/28AC100)
- Mostly single-cycle instructions
- Selectable 8-level deep hardware subroutine stack
- Single-level interrupt stack
- Fixed three-cycle interrupt response time
- Hardware context save/restore for interrupt
- Designed to be pin-compatible and upward code-compatible with the PIC165x®

1.2.2 I/O Features

- Software-selectable I/O configuration
  - Each pin programmable as an input or output
  - TTL or CMOS level selection on inputs
  - Internal weak pull-up selection on inputs (~20 kΩ to V_{dd})
- Schmitt trigger inputs on Port B and Port C
- All outputs capable of sinking/sourcing 30 mA
- Symmetrical drive on Port A outputs (same V_{drop} +/-)

1.3   Architecture

The SX devices use a modified Harvard architecture. This architecture uses two separate memories with separate address buses, one for the program and one for data, while allowing transfer of data from program memory to SRAM. This ability allows accessing data tables from program memory. The advantage of this architecture is that instruction fetch and memory transfers can be overlapped with a multi-stage pipeline, which means the next instruction can be fetched from program memory while the current instruction is being executed using data from the data memory.

The SX family implements a four-stage pipeline (fetch, decode, execute, and write back), which results in execution of one instruction per clock cycle. At the maximum operating frequency of 100 MHz, instructions are executed at the rate of one per 10-ns clock cycle.

1.4   Programming and Debugging Support

The SX devices are currently supported by the SX-Key™ offered by Parallax, Inc. This tool provides an integrated development environment including editor, macro assembler, debugger, and programmer.

1.5   Applications

Emerging applications and advances in existing ones require higher performance while maintaining low cost and fast time-to-market.

The SX devices provide solutions for many familiar applications such as process controllers, electronic appliances/tools, security/monitoring systems, digital filter implementation, high speed video processing, and telecommunication devices such as a FSK modems with DTMF generation/detection and Caller ID function. With 75 MHz or 100 MHz performance, the SX devices can even replace FPGAS, PLDs, and DSP functions. The deterministic executive of time-critical functions allows efficient implementation of real-time kernels. In addition, the enhanced throughput allows efficient development of software modules called Virtual Peripherals to replace on-chip hardware peripherals. The concept of Virtual Peripherals provides benefits such as using a more simple device, reduced component count, fast time to market, increased flexibility in design, and ultimately overall system cost reduction.

Some examples of Virtual Peripheral modules are:

- Serial, Parallel, I^2C™, Microwire™ (μ-Wire), Dallas μ-Wire, SPI, DMX-512, X-10, IR transceivers
- Frequency generation and measurement
- Spectrum analysis
- Multi-tasking, interrupts, and networking
- Resonance loops
- DRAM drivers
- Music and voice synthesis
- PPM/PWM output
- Delta/Sigma ADC
- DTMF I/O and call progress
- 300/1200 baud modem
- Quadrature encoder/decoder
- Peripheral Interface Device (PID) and servo control
- Video controller

2.0 CONNECTION DIAGRAMS

2.1 Pin Assignments
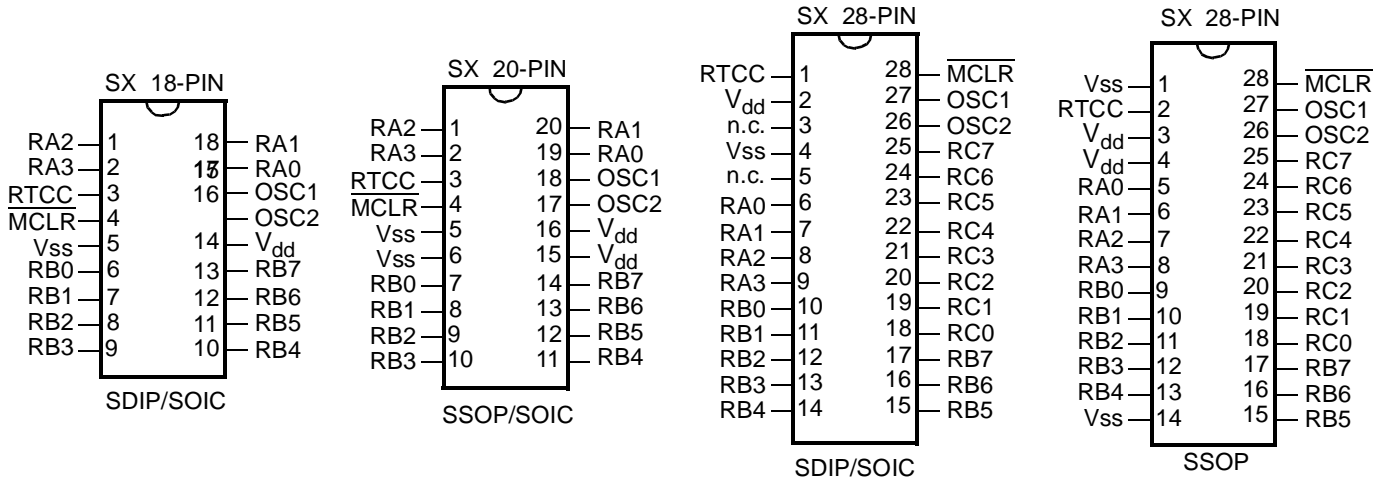
2.2 Pin Descriptions

Name	Pin Type	Input Levels	Description
RA0	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RA1	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RA2	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RA3	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RB0	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; comparator output; MIWU input
RB1	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; comparator negative input; MIWU input
RB2	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; comparator positive input; MIWU input
RB3	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU input
RB4	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU input
RB5	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU input
RB6	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU input
RB7	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU input
RC0	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC1	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC2	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC3	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC4	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC5	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC6	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC7	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RTCC	I	ST	Input to Real-Time Clock/Counter
$\overline{MCLR}$	I	ST	Master Clear reset input – active low
OSC1/In/Vpp	I	ST	Crystal oscillator input – external clock source input
OSC2/Out	O	CMOS	Crystal oscillator output – in R/C mode, internally pulled to V_{dd} through weak pull-up
V_{dd}	P	–	Positive supply pin
Vss	P	–	Ground pin
Note:I = input, O = output, I/O = Input/Output, P = Power, TTL = TTL input, CMOS = CMOS input, ST = Schmitt Trigger input, MIWU = Multi-Input Wakeup input			

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2.3   Part Numbering

Table 2-1. Ordering Information

Device	Pins	I/O	EE/Flash (Words)	RAM (Bytes)
SX18AC75/SO	18	12	2K	136
SX18AC75/DP	18	12	2K	136
SX20AC75/SS	20	12	2K	136
SX20AC100/SO	20	12	2K	136
SX28AC75/SO	28	20	2K	136
SX28AC75/DP	28	20	2K	136
SX28AC75/SS	28	20	2K	136
SX28AC100/SO	28	20	2K	136

SX18ACXX-LI/SO

Package Type

Extended Temperature

Low Voltage

Speed

Memory Size

Feature Set

Pin Count

SceniX

Blank =   50 MHz

75 =   75 MHz

100 =   100 MHz

A =   512 word

B =   1k word

C =   2k word

D =   4k word
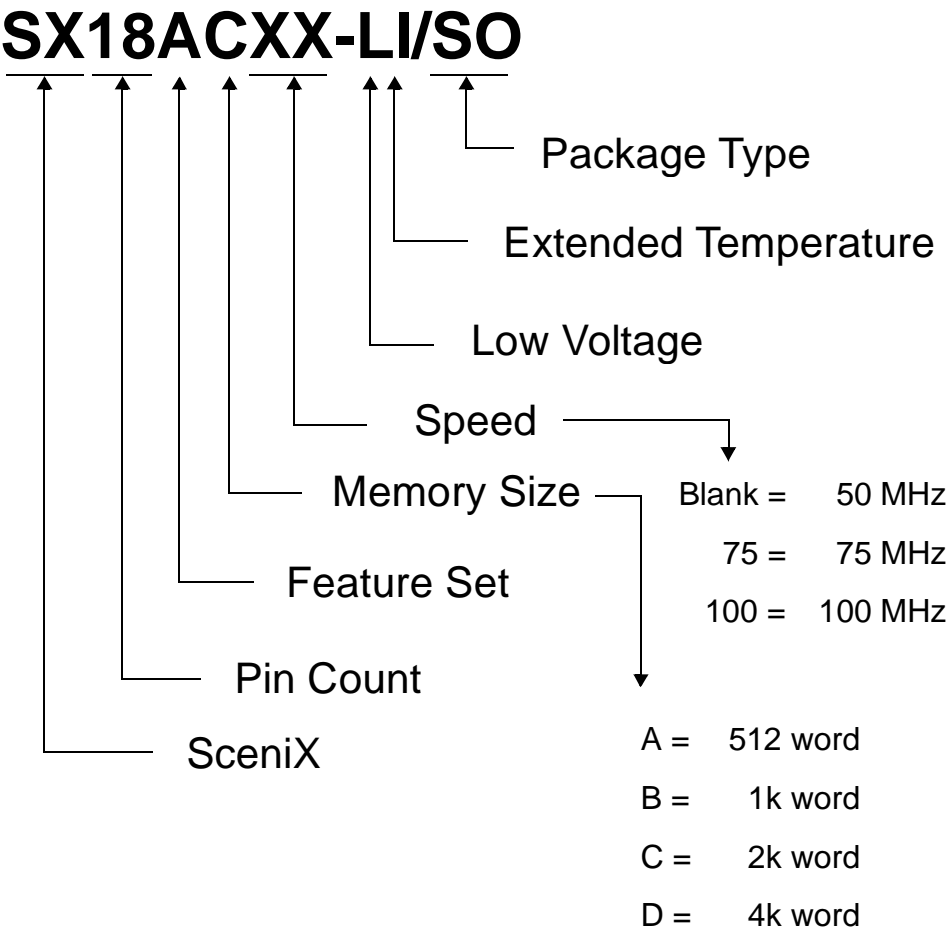
Figure 2-1. Part Number Reference Guide

                                                 www.scenix.com

MANUFACTURERS REPRESENTATIVES

Benelux

Memec Benelux
Gen. De Wittelaan, 17 B10
2800 Mechelen
Tel: (32) 15-400-0800
Email:
BdeVries@meb.memec.com

France

A2M
5 rue Carle Vernet
92315 Sevres Cedex
Tel: (33) 1-4623-7900
Email: mgadreau@tekelec.fr

Germany

Topas Electronic GmbH
Fliegerstrasse 1
30179 Hannover
Tel: (49) 898-991-430
Email: ulf.Topas@t-online.de

Scantec Mikroelektronik GmbH
Behringstrasse 10
82152 Planegg
Tel: (49) 511-968-640
Email: stenwaldo@com-
puserve.com

United Kingdom

Ambar Components
Rabans Close
Aylesbury
HP19 3RS Bucks
Tel: (944) 129-639-7396
Email:
rthomson@acp.memec.com

Ireland

Curragh Technology
Block H, Lock Quay
Clare Street
Limerick
Tel: (353) 6-131-6116
Email: jburton@ctl.memec.com

Italy

Silverstar-Celdis
Viale Fulvio Testi, 280
20126 Milano
Tel: (39) 2-661-251
Email: rbaldoni@arrowitaly.com

Norway

BIT Elektronikk
Smedsvingen 4
PO BOX 194
1360 Nesbru
Tel: (47) 66-776-599
Email: njh@bit.no

Switzerland

Computer Components AG
Neunbrunnenstrasse 55
8050 Zurich
Tel: (41) 13-086-655
Email: kolbicz@ccontrols.ch

China/Hong Kong

C. S. T. Technology, Ltd.
Room 907, Tower 1, Silvercord
30 Canton Road, TST
Kowloon, Hong Kong
Tel: (852) 2376-1882
Email:
sunadmin@sunrise.com.hk

Room 3113, Everbright ITIC
Bldg.
15 Bai Shi Qiao Road
Hai Dian Dist., Beijing, 100081
Tel: (010) 6848-6895
Email:
sunadmin@sunrise.com.hk

Room 519, Changning S&T
Bldg.
No. 201 Tian Shan Zhi Road
Shanghai, 200051
Tel: (201) 6259-4939
Email:
sunadmin@sunrise.com.hk

8/F, Block B, Overseas Decora-
tion Bldg.
11 Zhenhua Road
Shenzhen, 518031
Tel: (0755) 332-5656
Email:
sunadmin@sunrise.com.hk

Taiwan

Promate Electronic Co., Ltd.
4F 32m Sec.1, Huan Shan Road
Nei Hu, Taipei 114
Tel: (886) 2-2659-0303
Email: irving@promate.com.tw

Pinnacle Technology Co.
4F, 270, Sec. 3, Nan-Kang Road
Taipei
Tel: (886) 2-2788-4800
Email: pinnacle@ms1.hinet.net

Japan

Sumisho Electronic Devices
Corp.
1 Kandamitoshirocho
Chiyoda-ku, Tokyo 101
Tel: (81) 3-5282-7225
Email:
masayuki_kobayashi@sed.co.jp

Korea

Comfile Technology
30-1 Shingae-Dong
Youngsan-Gu, Seoul 140-090
Tel: (82) 2-711-2592
Email:
comfile@soback.kornet.nm.kr

Team Korea
292-6 Yatap-Dong, Bundang-Ku
Sungam-Si, Kyungki-Do
Tel: (82) 342-705-1825
Email:
mikechoi@teamkorea.com
http://www.teamkorea.com

For the latest contact and support information on SX devices, please visit the Scenix Semiconductor website at www.scenix.com. The site contains technical literature, local sales contacts, tech support and many other features.

Scenix Semiconductor, Inc.   **3160 De La Cruz Blvd., Suite #200**
Santa Clara, CA 95054
(408) 327-8888
http://www.scenix.com

Sales and Tech Support Contact Information

US DISTRIBUTOR

Unique Technologies

9980 Huennekens Street

San Diego, CA 92121

(800) 677-5664   Corporate Headquarters

(800) 556-0225   Direct to Local Office

DEVELOPMENT TOOLS

Parallax Inc.

3805 Atherton Road, Suite 102

Rocklin, CA 95765

(916) 624-8333

http://www.parallaxinc.com

MANUFACTURERS REPRESENTATIVES

South Nevada; Utah, Idaho; Montana; Wyoming; Colorado; New Mexico; Arizona

Nelco Electronix
Chandler
Tel: (602) 726-2334
Email: nelcoaz@aol.com

9725 E. Hampden Avenue
Suite 100
Denver, CO 80231
Tel: (303) 671-7677
Email: nelcoelect@aol.com

Boise
Tel: (208) 343-9171
Email: nelcotd@aol.com

Albuquerque
Tel: (505) 293-1399
Email: nelco@swcp.com

El Paso
Tel: (915) 833-7300
Email: nelco@dzn.com

Utah
Tel: (208) 343-9171
Email: nelcotd@aol.com

New York; East Pennsylvania; South New Jersey

Quality Components, Inc.
4211 Anita Drive
Collegeville, PA 19426
Tel: (800) 965-8885
Email: brogers@quality-component.com

116 Fayette Street
Manilus, NY 13104
Tel: (315) 682-8885

Tennesse; N. Carolina; S. Carolina; Georgia; Alabama; Mississippi

STG
101 Washington Street
Suite 6
Huntsville, AL 35801
Tel: (205) 534-2376
Email: hstokes@stghsv.com

6045 Atlantic Boulevard
Norcross, GA 30071
Tel: (770) 239-7576
Email: hstokes@stghsv.com

207 New Edition Court
Cary, NC 27511
Tel: (919) 468-1524
Email: hstokes@stghsv.com

North California

Impact Technical Sales, Inc.
1150 N. First St. #205
San Jose, CA 95112
Tel: (408) 291-5100
Email: info@impactTSI.com

South California

Spectrum Rep Company
31368 Via Colinas
Suite 101
Westlake Village, CA 91362
Tel: (818) 706-2919
Email: larryclark@spectrum-rep.com
http://www.spectrumrep.com

30211 Avenida de las Banderas
Suite 200
Rancho Santa Margarita,
CA 92688
Tel: (949) 766-6700
Email: paul@spectrumrep.com

27281 Las Ramblas
Suite 200
Mission Viejo, CA 92691
Tel: (949) 367-3132
Email: zig@spectrumrep.com

16776 Bernardo Ctr. Dr.
Suite 203
San Diego, CA 92128
Tel: (619) 618-1440
Email: paul@spectrumrep.com

N. Dakota; S. Dakota; Minnesota

Com-Tek Sales, Inc
3502 Shoreline Drive
Navarre, MN 55392-0017
Tel: (612) 471-7181
Email: comtek@comtek-sales.com

Michigan; Indiana; Ohio; Kentucky; West Pennsylvania

Schillinger Associates, Inc.
2297 East Boulevard
Kokomo, IN 46902
Tel: (765) 457-7241
Email: saicorp@msn.com

Southeast New York; North New Jersey

ERA
354 Veterans Memorial Highway
Commack, NY 11725
Tel NY: (516) 543-0510
Tel NJ: (800) 645-5500
Email: info.era@erareps.com
http://www.erareps.com

Texas; Oklahoma; Arizona; Louisiana

TechSource
7605 Parkview Circle
Austin, TX 78731
Tel: (512) 502-9962
Fax: (512) 502-9985

Wisconsin; Illinois

Dynamic Technical Sales
416 East State Parkway
Suite 212
Schaumburg, IL 60173
Tel: (847) 755-5490
Email: dts@dtsrep.com

553 Industrial Drive
Suite 6
Hartland, WI 53029
Tel: (414) 367-1821
Email: dtsinc@execpc.com

For the latest contact and support information on SX devices, please visit the Scenix Semiconductor website at www.scenix.com. The site contains technical literature, local sales contacts, tech support and many other features.

Scenix Semiconductor, Inc.   **3160 De La Cruz Blvd., Suite #200**

Santa Clara, CA 95054

(408) 327-8888

http://www.scenix.com