

54F/74F544 Octal Registered Transceiver

General Description

The 'F544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA (20 mA Mil) while the B outputs are rated for 64 mA (48 mA Mil). The 'F544 inverts data in both directions.

Features

- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 24 mA (20 mA Mil), B outputs sink 64 mA (48 mA Mil)
- 300 mil slim PDIP

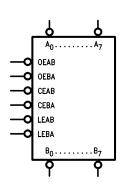
| Commercial | Military | Package Number | Package Description |
|--------------------|--------------------|-------------------|--|
| 74F544SPC | | N24C | 24-Lead (0.300" Wide) Molded Dual-In-Line |
| | 54F544DM (Note 2) | J24A | 24-Lead Ceramic Dual-In-Line |
| | 54F544SDM (Note 2) | J24F | 24-Lead (0.300" Wide) Ceramic Dual-In-Line |
| 74F544SC (Note 1) | | M24B | 24-Lead (0.300" Wide) Molded Small Outline, JEDEC |
| 74F544MSA (Note 1) | | MSA24 | 24-Lead Molded Shrink Small Outline, EIAJ, Type II |
| | 54F544FM (Note 2) | W24C | 24-Lead Cerpack |
| | 54F544LM (Note 2) | E28A | 24-Lead Ceramic Leadless Chip Carrier, Type C |

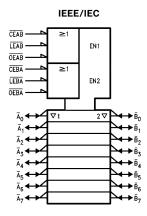
Note 1: Devices also available in 13" reel. Use suffix = SCX and MSAX.

 $\textbf{Note 2:} \ \textbf{Military grade device with environmental and burn-in processing.} \ \textbf{Use suffix} = \textbf{DMQB, FMQB and LMQB}$

TI /F/9555-2

Logic Symbols





TL/F/9555-1

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Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



A₆ A₅ A₄ NC A₃ A₂ A₁
11 10 9 8 7 6 5

A₇ 12

CEAB 13

NC 15

OEAB 16

LEAB 17

B₇ 18

19 20 21 22 23 24 25

B6 B5 B4 NC B3 B2 B1

Pin Assignment

for LCC

TL/F/9555-4

TL/F/9555-3

Unit Loading/Fan Out

| | | 54F/74F | | | | |
|-----------------------------------|---|------------------|---|--|--|--|
| Pin Names Description | | U.L. HIGH/LOW | Input I _{IH} /I _{IL} Output I _{OH} /I _{OL} | | | |
| OEAB | A-to-B Output Enable Input (Active LOW) | 1.0/1.0 | 20 μA/-0.6 mA | | | |
| OEBA | B-to-A Output Enable Input (Active LOW) | 1.0/1.0 | 20 μA/ – 0.6 mA | | | |
| CEAB | A-to-B Enable Input (Active LOW) | 1.0/2.0 | 20 μA/-1.2 mA | | | |
| CEBA | B-to-A Enable Input (Active LOW) | 1.0/2.0 | 20 μA/-1.2 mA | | | |
| LEAB | A-to-B Latch Enable Input (Active LOW) | 1.0/1.0 | 20 μA/ – 0.6 mA | | | |
| LEBA | B-to-A Latch Enable Input (Active LOW) | 1.0/1.0 | 20 μA/-0.6 mA | | | |
| $\overline{A}_0 - \overline{A}_7$ | A-to-B Data Inputs or | 3.5/1.083 | 70 μΑ/ -650 μΑ | | | |
| | B-to-A TRI-STATE Outputs | 150/40(33.3) | -3 mA/24 mA (20 mA) | | | |
| $\overline{B}_0 - \overline{B}_7$ | B-to-A Data Inputs or | 3.5/1.083 | 70 μΑ/ -650 μΑ | | | |
| | A-to-B TRI-STATE Outputs | 600/106.6(80) | -12 mA/64 mA (48 mA) | | | |

Functional Description

The 'F544 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{\text{CEAB}}$) input must be LOW in order to enter data from $\overline{\text{A}}_0-\overline{\text{A}}_7$ or take data from $\overline{\text{B}}_0-\overline{\text{B}}_7$, as indicated in the Data I/O Control Table. With $\overline{\text{CEAB}}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{\text{LEAB}}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{\text{LEAB}}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both LOW, the TRI-STATE® B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$ and $\overline{\text{OEBA}}$ inputs.

Data I/O Control Table

| | Inputs | | Latch Status | Output Buffers | | |
|------|--------|------|--------------|----------------|--|--|
| CEAB | LEAB | OEAB | Laton Otatus | Catput Barrers | | |
| Н | Х | Х | Latched | High Z | | |
| Χ | Н | Χ | Latched | _ | | |
| L | L | Χ | Transparent | _ | | |
| Χ | X | Н | _ | High Z | | |
| L | X | L | _ | Driving | | |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{\text{CEBA}},$ $\overline{\text{LEBA}}$ and $\overline{\text{OEBA}}$

A₁ — DETAIL A — B₀ A₂ — O A₃ — O A₄ — O A₅ — O A₆ — O A₇ — O DETAIL A × 7 DE

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

CEBA ·

LEBA -

- OEAB

TL/F/9555-5

CEAB

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} Pin Potential to

Ground Pin -0.5V to +7.0V Input Voltage (Note 2) -0.5V to +7.0V

Input Current (Note 2) $$-30~\rm{mA}$ to $+5.0~\rm{mA}$ Note 1: Absolute maximum ratings are values beyond which the device may

be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature

Supply Voltage

Military +4.5V to +5.5V Commercial +4.5V to +5.5V

DC Electrical Characteristics

| Symbol | Parameter . | | 54F/74F | | | Units | V _{CC} | Conditions | |
|------------------------------------|---------------------------------------|---|--|-----|----------------------------|-------|-----------------|---|--|
| Зупівої | | | Min | Тур | Max | Units | V CC | Conditions | |
| V _{IH} | Input HIGH Voltage | | 2.0 | | | V | | Recognized as a HIGH Signal | |
| V _{IL} | Input LOW Voltage | | | | 0.8 | V | | Recognized as a LOW Signal | |
| V _{CD} | Input Clamp Diode Vo | oltage | | | -1.2 | ٧ | Min | $I_{IN} = -18 \text{ mA},$ (except \overline{A}_n , \overline{B}_n) | |
| V _{OH} | Output HIGH Voltage | 54F 10% V _{CC} 54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC} | 2.5 2.4 2.0 2.5 2.4 2.0 2.7 2.7 | | | V | Min | $\begin{split} I_{OH} &= -1 \text{ ma } (\overline{A}_n) \\ I_{OH} &= -3 \text{ ma } (\overline{A}_n, \overline{B}_n) \\ I_{OH} &= -12 \text{ ma } (\overline{B}_n) \\ I_{OH} &= -1 \text{ ma } (\overline{A}_n) \\ I_{OH} &= -1 \text{ ma } (\overline{A}_n, \overline{B}_n) \\ I_{OH} &= -15 \text{ ma } (\overline{B}_n) \\ I_{OH} &= -1 \text{ ma } (\overline{A}_n, \overline{B}_n) \\ I_{OH} &= -1 \text{ ma } (\overline{A}_n, \overline{B}_n) \\ I_{OH} &= -3 \text{ ma } (\overline{A}_n, \overline{B}_n) \end{split}$ | |
| V _{OL} | Output LOW Voltage | 54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} | | | 0.5 0.55 0.5 0.55 | V | Min | $\begin{split} &I_{OL} = 20 \text{ mA } (\overline{A}_n) \\ &I_{OL} = 48 \text{ mA } (\overline{B}_n) \\ &I_{OL} = 24 \text{ mA } (\overline{A}_n) \\ &I_{OL} = 64 \text{ mA } (\overline{B}_n) \end{split}$ | |
| I _{IH} | Input HIGH Current | 54F 74F | | | 20.0 5.0 | μΑ | Max | $V_{IN} = 2.7V \text{ (except } \overline{A}_n, \overline{B}_n \text{)}$ | |
| I _{BVI} | Input HIGH Current Breakdown Test | 54F 74F | | | 100 7.0 | μΑ | Max | $V_{IN} = 7.0V \text{ (except } \overline{A}_n, \overline{B}_n \text{)}$ | |
| I _{BVIT} | Input HIGH Current Breakdown (I/O) | 54F 74F | | | 1.0 0.5 | mA | Max | $V_{IN} = 5.5V (\overline{A}_n, \overline{B}_n)$ | |
| I _{CEX} | Output HIGH Leakage Current | 54F 74F | | | 250 250 | μΑ | Max | $V_{OUT} = V_{CC}(\overline{A}_n, \overline{B}_n)$ | |
| V _{ID} | Input Leakage Test | 74F | 4.75 | | | ٧ | 0.0 | $I_{\text{ID}} = 1.9 \ \mu\text{A}$ All Other Pins Grounded | |
| I _{OD} | Output Leakage Circuit Current | 74F | | | 3.75 | μΑ | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded | |
| I _{IL} | Input LOW Current | | | | -0.6 -1.2 | mA | Max | $V_{IN} = 0.5V (\overline{OEAB}, \overline{OEBA})$ $V_{IN} = 0.5V (\overline{CEAB}, \overline{CEBA})$ | |
| I _{IH} + I _{OZH} | Output Leakage Curr | ent | | | 70 | μΑ | Max | $V_{OUT} = 2.7V (\overline{A}_n, \overline{B}_n)$ | |
| I _{IL} + I _{OZL} | Output Leakage Curr | ent | | | -650 | μΑ | Max | $V_{OUT} = 0.5V (\overline{A}_n, \overline{B}_n)$ | |

DC Electrical Characteristics (Continued)

| Symbol | Parameter | | 54F/74F | | Units | v _{cc} | Conditions | |
|------------------|------------------------------|-------------|---------|------------|-------|-----------------|---|--|
| | rainetei | Min | Тур | Max | Omis | | | |
| los | Output Short-Circuit Current | -60 -100 | | 150 225 | mA | Max | $V_{OUT} = 0V (\overline{A}_n)$ $V_{OUT} = 0V (\overline{B}_n)$ | |
| I _{ZZ} | Bus Drainage Test | | | 500 | μΑ | 0.0V | $V_{OUT} = 5.25V (\overline{A}_n, \overline{B}_n)$ | |
| I _{CCH} | Power Supply Current | | 70 | 105 | mA | Max | V _O = HIGH | |
| I _{CCL} | Power Supply Current | | 85 | 130 | mA | Max | $V_O = LOW$ | |
| Iccz | Power Supply Current | | 83 | 125 | mA | Max | $V_O = HIGH Z$ | |

AC Electrical Characteristics

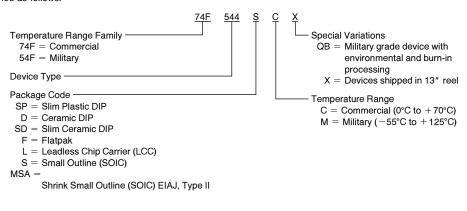
| | | $74F$ $T_{A} = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_{L} = 50 \text{ pF}$ | | | 54F T _A , V _{CC} = Mil C _L = 50 pF | | 7- | 4F | |
|--------------------------------------|--|---|-------------|-------------|---|--------------|--|--------------|-------|
| Symbol | Parameter | | | | | | T _A , V _{CC} = Com C _L = 50 pF | | Units |
| | | Min | Тур | Max | Min | Max | Min | Max | |
| t _{PLH} t _{PHL} | Propagation Delay Transparent Mode \overline{A}_n to \overline{B}_n or \overline{B}_n to \overline{A}_n | 3.0 3.0 | 7.0 5.0 | 9.5 6.5 | 3.0 2.5 | 12.0 8.5 | 3.0 3.0 | 10.5 7.5 | ns |
| t _{PLH} | Propagation Delay LEBA to Ā _n | 6.0 4.0 | 10.0 7.0 | 13.0 9.5 | 6.0 4.0 | 18.0 11.5 | 6.0 4.0 | 14.5 10.5 | ns |
| t _{PLH} | Propagation Delay LEAB to B _n | 6.0 4.0 | 10.0 7.0 | 13.0 9.5 | 6.0 4.0 | 18.0 11.5 | 6.0 4.0 | 14.5 10.5 | ns |
| t _{PZH} t _{PZL} | Output Enable Time $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to $\overline{\text{A}}_n$ or $\overline{\text{B}}_n$ $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ to $\overline{\text{A}}_n$ or $\overline{\text{B}}_n$ | 3.0 4.0 | 7.0 7.5 | 9.0 10.5 | 3.0 4.0 | 11.0 13.0 | 3.0 4.0 | 10.0 12.0 | - ns |
| t _{PHZ} | Output Disable Time \overline{OEBA} or \overline{OEAB} to \overline{A}_n or \overline{B}_n \overline{CEBA} or \overline{CEAB} to \overline{A}_n or \overline{B}_n | 1.0 2.5 | 6.0 5.5 | 8.0 10.5 | 2.0 2.0 | 10.0 9.5 | 1.0 2.5 | 9.0 11.5 | |

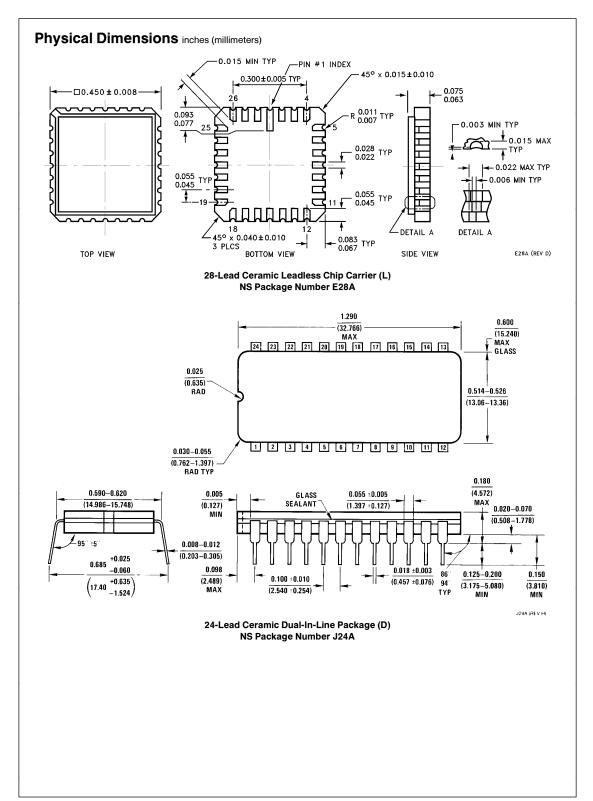
AC Operating Requirements

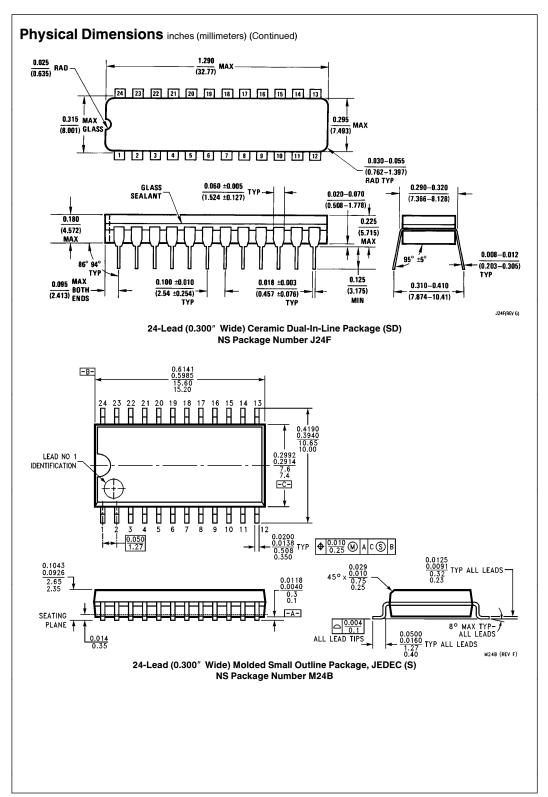
| | | $74F$ $T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ | | 54 | F | 74F | | |
|--|--|---|-----|------------------------------|-----|--|-----|-------|
| Symbol | Parameter | | | ${\sf T_A,V_{CC}}={\sf Mil}$ | | T _A , V _{CC} = Com | | Units |
| | | Min | Max | Min | Max | Min | Max | |
| t _s (H) t _s (L) | Setup Time, HIGH or LOW \overline{A}_n or \overline{B}_n to \overline{LEBA} or \overline{LEAB} | 3.0 3.0 | | 3.0 3.0 | | 3.0 3.0 | | ns |
| t _h (H) t _h (L) | Hold Time, HIGH or LOW \overline{A}_n or \overline{B}_n to \overline{LEBA} or \overline{LEAB} | 3.0 3.0 | | 3.0 3.0 | | 3.0 3.0 | | 113 |
| t _w (L) | Latch Enable, B to A Pulse Width, LOW | 6.0 | | 9.0 | | 7.5 | | ns |

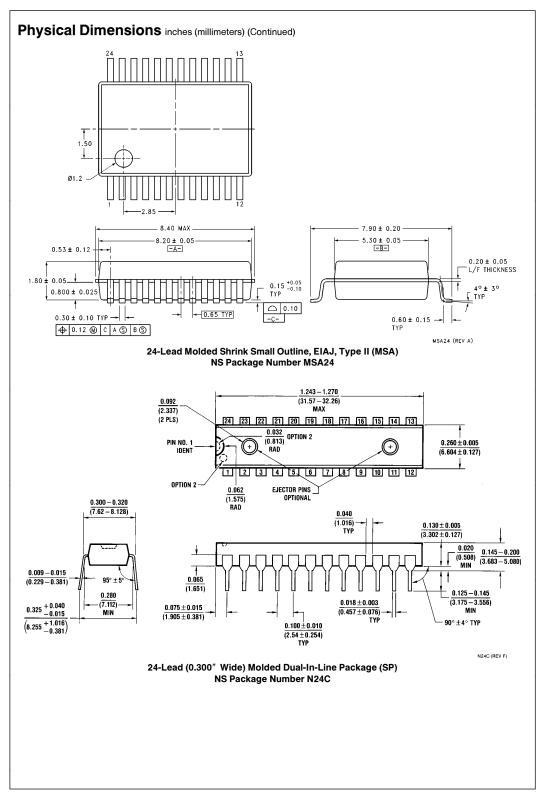
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

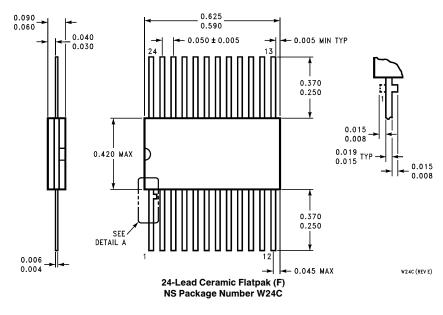








Physical Dimensions inches (millimeters) (Continued)



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