



Tessent® SiliconInsight® User's Manual for the LV Flow

Software Version 2014.2

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Chapter 1

About This Manual

This manual introduces the Mentor Graphics embedded test-based manufacturing test flow and provides detailed information on how to use the Tesson SiliconInsight software. It includes step-by-step instructions on how to use the Tesson SiliconInsight® software to direct the embedded test resources on the DUT to perform production go/no-go and detailed diagnosis of memories, logic, and I/Os. In addition, this manual describes how to setup Tesson SiliconInsight Desktop, Tesson SiliconInsight ATE, and Tesson SiliconInsight Production Datalogging.

Note



To perform Tesson SerdesTest diagnostics with Tesson SiliconInsight, refer to the [Tesson SerdesTest User's Manual](#). To perform Tesson PLLTest diagnostics with Tesson SiliconInsight, refer to the [Tesson PLLTest User's Manual](#).

Refer to “[Getting Help](#)” for support options and related documentation.

Manual Contents

This manual contains the following chapters:

- [Tesson SiliconInsight Overview](#) introduces the Mentor Graphics Tesson SiliconInsight product for the LV flow. It provides a high-level overview of the tool, its use models and related software configurations, and Mentor Graphics’ Built-In Self Test (BIST) technology and products.
- [Diagnosing Device Failures](#) describes in general how to diagnose the failures. The following three chapters provide detailed information on the specific diagnostics.
- [Performing Memory BIST Diagnostics](#) provides step-by-step instructions on how to use the Tesson SiliconInsight software to diagnose memory BIST controllers on the DUT.
- [Performing Logic Test Diagnostics](#) provides step-by-step instructions on how to use the *Logic Test Diagnostics* using the Tesson SiliconInsight tools to direct logic BIST controllers on the DUT to perform production go/no-go and detailed diagnosis of logic.
- [Performing I/O, TAP, WTAP Tests and Diagnosis](#) provides step-by-step instructions on how to use the Tesson SiliconInsight software to direct embedded test resources on the DUT to perform production go/no-go and detailed diagnosis of device I/Os, TAP, and WTAPs.

- **Diagnosing and Validating Memory With Enhanced Stop-On-Nth-Error Test Patterns** describes how to generate enhanced Stop-On-Nth-Error (ESOE) test patterns, collect the failing cycle data, and convert the failure log files into memory bitmap data suitable for diagnostic purposes.
- **Setting Up and Using Tesson SiliconInsight Desktop** describes how to install and use Tesson SiliconInsight Desktop and how to configure Tesson SiliconInsight Desktop for a multi-site environment.
- **Setting Up Tesson SiliconInsight ATE** provides step-by-step instructions on how to use the Tesson SiliconInsight software with different ATE platforms. It includes reference information about the relevant API calls, runtime options, and files that are used in Tesson SiliconInsight ATE.
- **Setting Up Tesson SiliconInsight Production Datalogging** provides step-by-step instructions on how to use the Tesson SiliconInsight software to direct the embedded test resources on the DUT to perform production go/no-go and detailed diagnosis of memories, logic, PLLs, and I/Os.
- **Memory BIST Algorithms** describes Mentor Graphics library of test patterns or algorithms for testing your memories. These algorithms represent some algorithms that you may perform on your memories using Tesson MemoryBIST programmable and non-programmable controllers. You can use the detailed algorithm examples provided in this appendix as a basis for creating your own algorithms.

Chapter 2

Tessent SiliconInsight Overview

This chapter introduces the Mentor Graphics Tessent SiliconInsight product for the LV flow. It provides a high-level overview of Tessent SiliconInsight's capabilities and benefits, describes the supported Tessent SiliconInsight use models and related software configurations, and provides a review of Mentor Graphics' Built-In Self Test (BIST) technology and products. It describes the concept of embedding test capabilities within the device and explains how these resources can be used to diagnose failures and characterize device performance.

This chapter covers the following topics:

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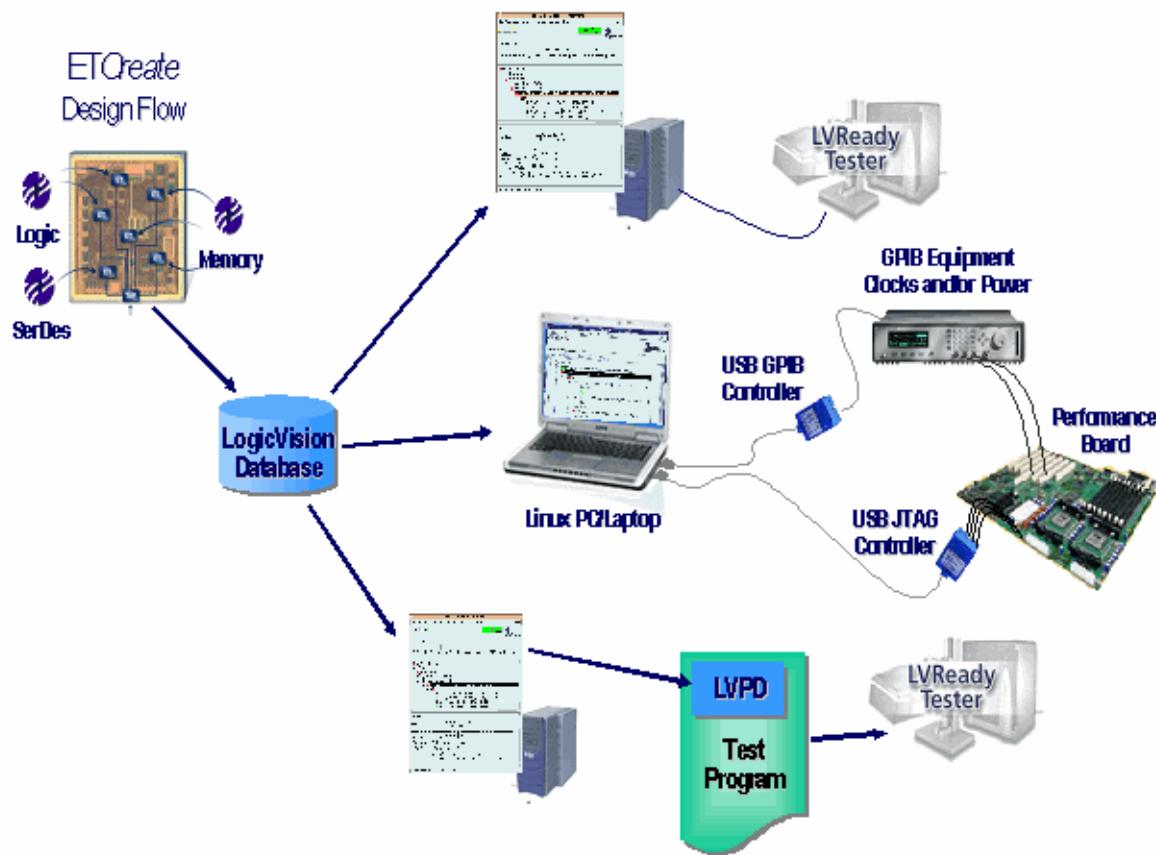
Bring-Up and Diagnosis with Tessent SiliconInsight

The traditional ATPG-based silicon bring-up flow represents a significant component of the product development cycle and can often take weeks if not months to complete. These delays are getting even worse with the adoption of at-speed and ATPG compression methodologies. This lengthy bring-up process not only represents significant engineering costs but more importantly a delay in getting working samples to the end customer and therefore a direct impact to the product launch time-line. Therefore, any reductions in the bring-up time will have a direct effect on the success and eventually the profitability of the device.

Mentor Graphics' BIST-based bring-up flow is significantly simpler than the traditional ATPG-based flow and removes much of the complexity for the designer. [Figure 2-1](#) illustrates how it works.

Designers use Mentor Graphics' LV Flow to create and integrate BIST resources into a design. As part of the final sign-off process, the LV Flow generates a Mentor Graphics database (LVDB) which contains extensive information on the BIST resources and the design itself. The LVDB provides Mentor Graphics' automated Tessent SiliconInsight software with the information it needs to control and interpret results from the BIST within the DUT. Rather than having to create test patterns to run specific tests, the design engineer simply specifies easy-to-understand high-level test options in a *Silicon Insight* configuration file or through the software's interactive GUI. The software then controls the tester to communicate with the various on-chip BIST resources to perform the desired tests and then extract and interpret the results. Since all of the BIST resources have been verified during the design phase, there is no test related debug to perform on the tester. The result is *fully interactive diagnosis and characterization* for logic, memories and mixed-signal structures.

Figure 2-1. Mentor Graphics Back-End Diagnostic Flow



The Tessent SiliconInsight software can be used interactively on most commercial testers. However, the only requirements for running BIST are communication to the standard five-pin JTAG test interface and the delivery of power and clocking to the device. Power and clocking are often provided within a performance board environment. In this case, no test equipment is required, and communication to the JTAG port can be achieved with a simple PC or laptop connected to a USB-to-JTAG interface cable. An optional USB-to-GPIB interface cable is also

supported for driving bench-top clock generators and power supplies for even more detailed characterization. This not only reduces the cost associated with tying up an expensive tester, but also allows bring-up activity to occur anytime, and, thus, further accelerates the overall bring-up process.

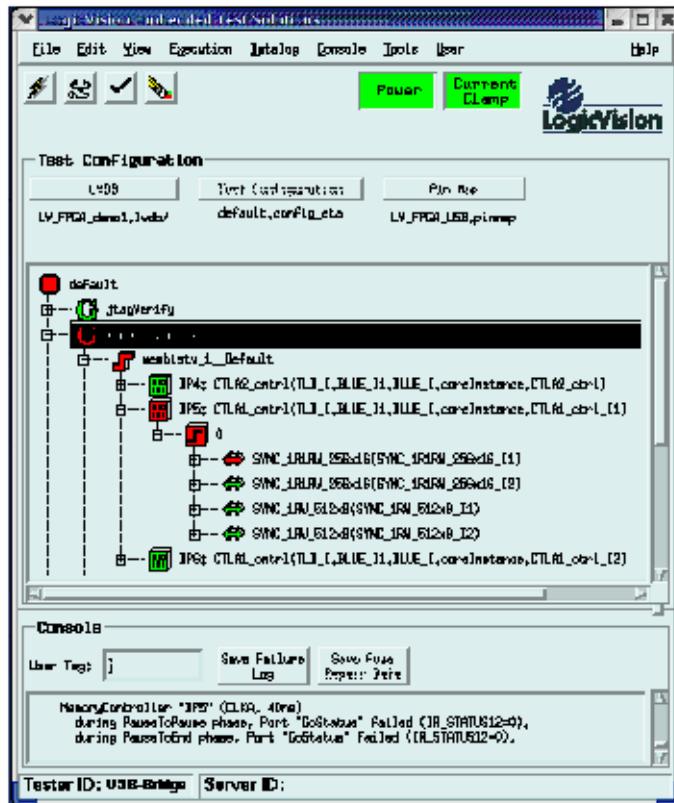
Production datalogging can also be performed by integrating Tessent SiliconInsight library routines into the test program which can then be accessed through user function calls. This allows detailed BIST datalogging to be performed on any test floor without the need to install any software.

For details about these different use models, refer to “[Tessent SiliconInsight Configurations](#).”

Interactive Diagnostics

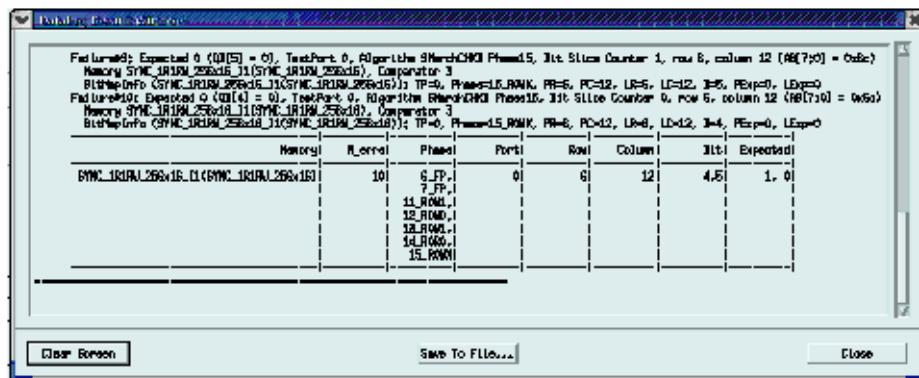
Tessent SiliconInsight provides a fully interactive graphical environment for diagnosing and characterizing circuitry tested using Mentor Graphics' BIST capabilities. The graphical environment provides a visual representation of the BIST resources within the device and the order in which they are to be executed. Embedded test controllers are represented as individual icons within the main GUI panel. All embedded test controller settings and options as well as the overall execution order can be modified interactively using the GUI as shown in [Figure 2-2](#).

Figure 2-2. Tessent SiliconInsight Main GUI



For example in the GUI display shown in [Figure 2-2](#), three memory BIST controllers (*BP4*, *BP5*, and *BP6*) are displayed along with their most recent execution results. The display shows that *BP5* has detected failures and that these are associated with only one of the four tested memories (shown as bidirectional arrows). More details on the failing memory can be easily generated. Failing memory, memory port, and memory I/O information are generated instantaneously and displayed both graphically as well as sent to a datalog file for future processing. Bit-level failure information can also be generated. Within just seconds of invoking the diagnostic function, the tool displays a detailed report of all failures encountered up to the number requested as shown in [Figure 2-3](#).

Figure 2-3. Detailed Memory Diagnosis



For each failure the tool displays the following:

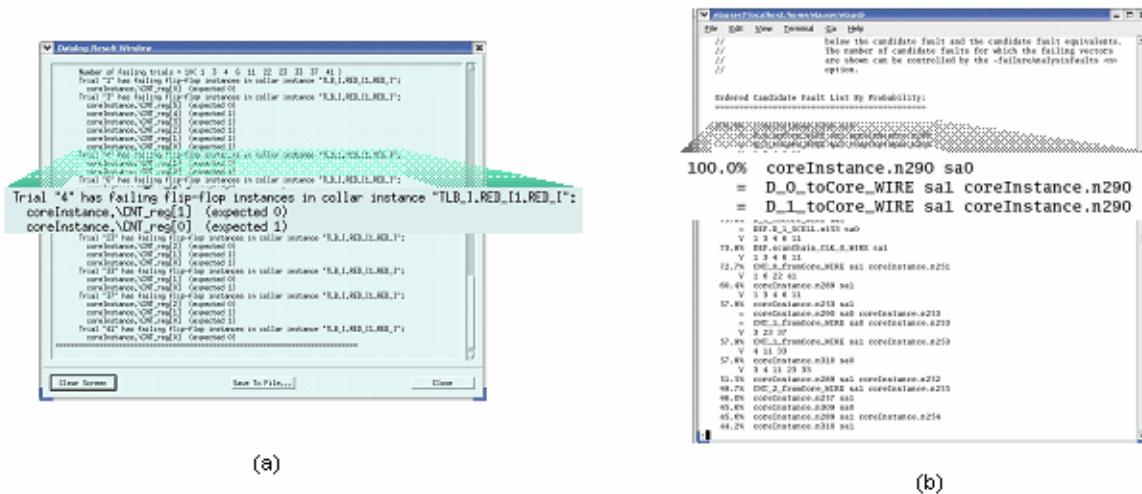
- Failing memory port
- Failing row and column addresses and bit position
- The algorithm used to test the memory and the phase of this algorithm in which the failure was detected

This information is displayed in text format for each failure as well as provide in a table summary format for easier analysis.

Three levels of automated logic diagnostics are also supported. At all levels, both static and at-speed failures can be diagnosed:

- **Pattern level**—identifies which pseudo-random test patterns are failing within each core. The number of failing patterns to diagnose can be specified.
- **Flip-flop level**—identifies which flip-flops in the design are capturing faulty values within each failing pattern—refer to [Figure 2-4\(a\)](#). The number of failing flip-flops to diagnose per failing pattern can be specified.
- **Gate level**—provides a report on the location of the suspected net, or nets, where defects can be found as shown in [Figure 2-4\(b\)](#). This information can also be fed to third-party defect analysis tools.

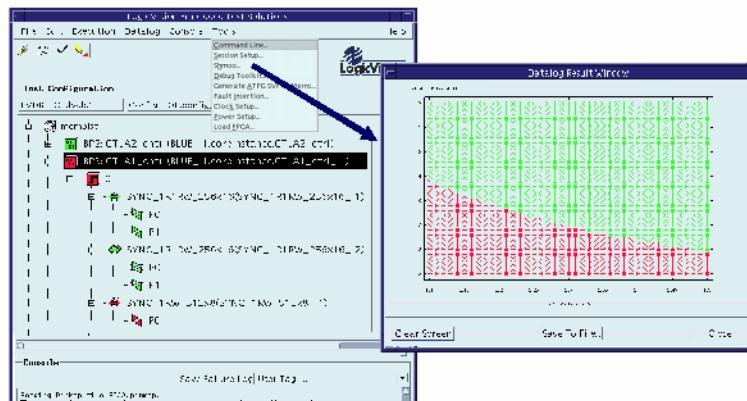
Figure 2-4. Flop-Flop and Gate Level Diagnostics



Performance Characterization

Tessent SiliconInsight provides capabilities for circuit performance characterization. A built-in Shmoo tool allows measuring a circuit's performance across any voltage and/or frequency range (see [Figure 2-5](#)). Performance can also be measured under various circuit activity levels. For example, a memory's maximum frequency can be logged when no other circuit activity exists within the chip, when only certain other memories are active or when all memories are being exercised. If logic BIST is also being used, then the logic activity level can also be controlled. All activity levels are easily set within the graphical environment and require no specific knowledge of the BIST or the design. This detailed and interactive characterization capability is very powerful in determining specific design areas (e.g. memories, logic blocks or paths) that are the slowest and thus limiting the overall speed of the design.

Figure 2-5. Tessent SiliconInsight's Built-In Shmoo Utility



Tessent SiliconInsight Configurations

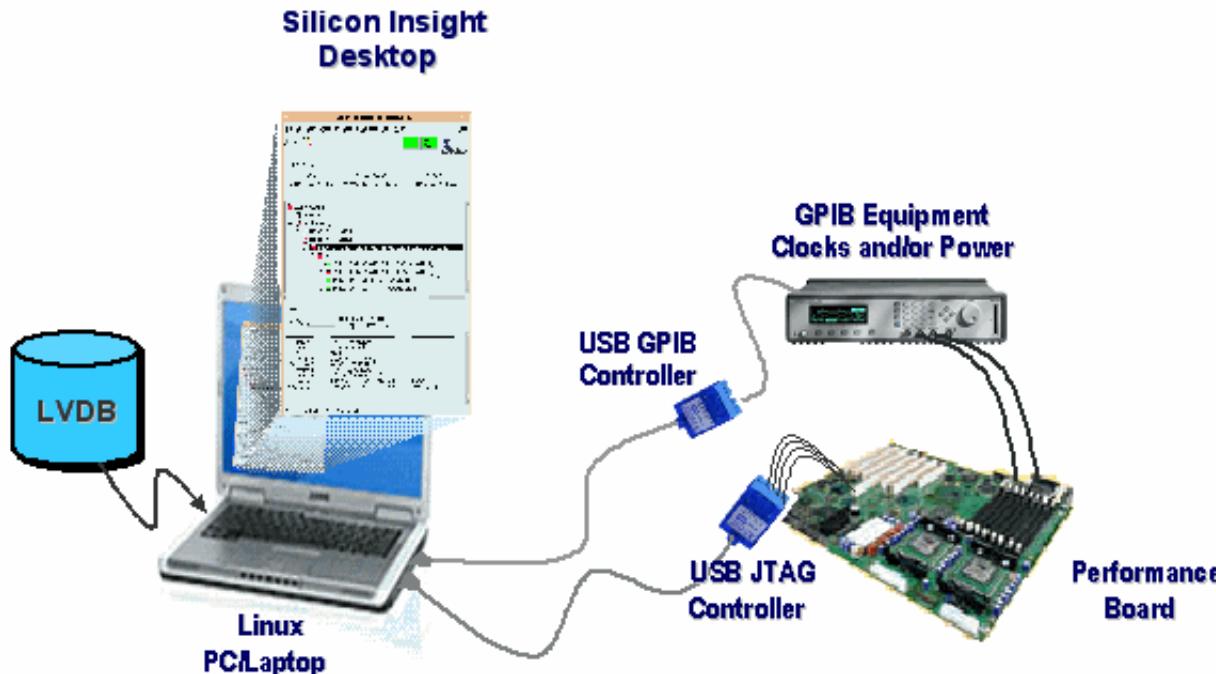
Tessent SiliconInsight can be used under three different configurations. The choice of which to use depends on whether interactive diagnostics or production datalogging is to be performed. For interactive diagnostics, Tessent SiliconInsight can be used either on a commercial tester platform or on a PC /laptop in a lab or office environment.

Desktop Interactive Configuration

In the configuration illustrated in [Figure 2-6](#), Tessent SiliconInsight Desktop is used to perform interactive diagnostic or characterization activities using a Linux-based PC or laptop connected to a performance board through a USB-to-JTAG interface and, optionally, a USB-to-GPIB interface for controlling external clock generators and/or power supplies.

For details on setting up this PC/laptop configuration, refer to Chapter 8, “[Setting Up and Using Tessent SiliconInsight Desktop](#).”

Figure 2-6. Desktop Interactive Configuration



ATE Interactive and Datalogging Configuration

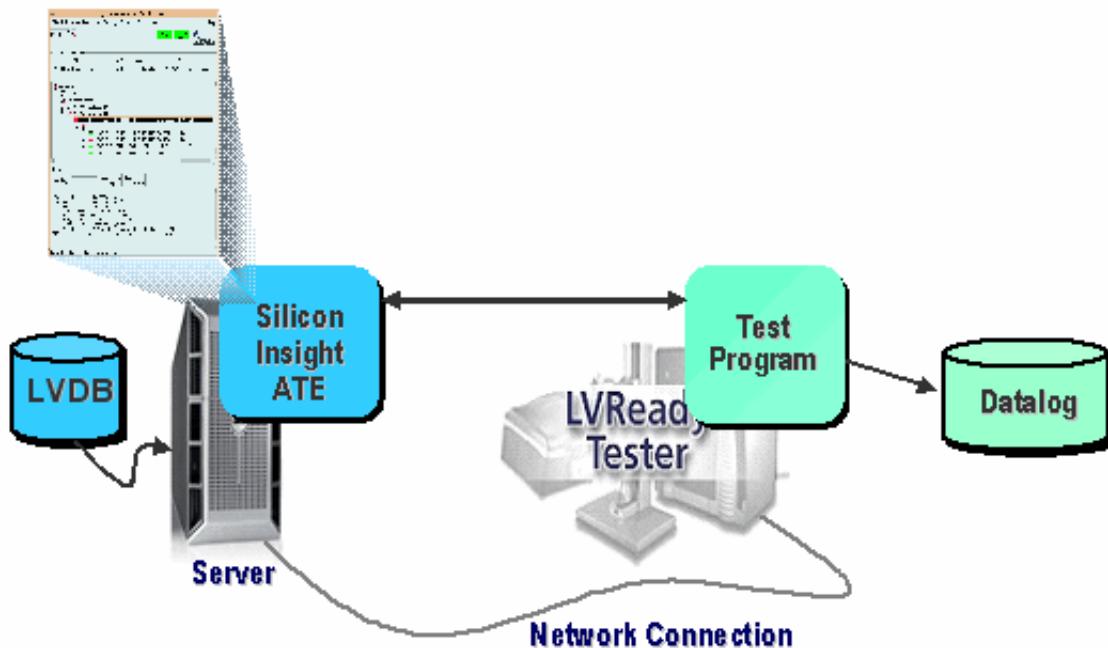
In the configuration illustrated in [Figure 2-7](#), Tessent SiliconInsight ATE is used to perform interactive diagnostic or characterization activities using an LVReady™ tester. An LVReady tester is an ATE platform for which interfaces have been developed between the tester's system software and the Tessent SiliconInsight software and libraries. Most 3rd party commercial ATE

platforms are LVReady. For a complete updated list of LVReady testers, contact your Mentor Graphics account manager.

The Tessent SiliconInsight ATE software can be installed directly on the tester's workstation or on a server connected to the tester, depending on the tester's capabilities. This configuration also enables comprehensive production datalogging from the test program.

For details on setting up your test program for this configuration, refer to Chapter 9, “[Setting Up Tessent SiliconInsight ATE](#).”

Figure 2-7. ATE Interactive and Datalogging Configuration

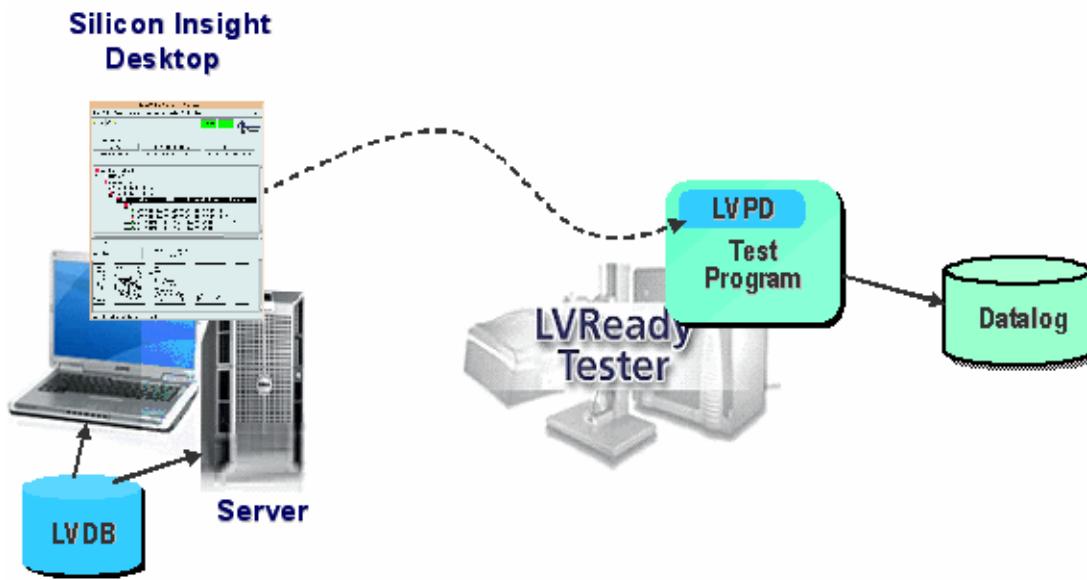


Production Datalogging Configuration

In the configuration illustrated in [Figure 2-8](#), either Tessent SiliconInsight Desktop or Tessent SiliconInsight ATE (*online* or *offline*) can be used to create a Mentor Graphics Production Database (LVPD). The LVPD is used in the test program for remote datalogging. The LVPD is a reduced version of the LVDB which also contains software routines that provide similar functionality to the real-time Tessent SiliconInsight software. These routines are linked into any test program and are accessed through user function calls. This allows detailed BIST datalogging to be performed on any test floor without the need to install any Tessent SiliconInsight software.

For details on setting up your test program for this configuration, refer to Chapter 10, “[Setting Up Tessent SiliconInsight Production Datalogging](#).”

Figure 2-8. Production Datalogging Configuration



BIST Technology Review

BIST is a natural evolution of two distinct test approaches: External ATE and conventional Design for Test (DFT). Building on conventional DFT approaches such as scan, BIST integrates the high-speed and high-bandwidth portions of the external ATE directly into the ICs. This integration facilitates chip-, board-, and system-level test, diagnosis, and debug. BIST consists of user-configurable IP (intellectual property), in the form of design objects delivered as Register Transfer Language (RTL) soft cores. These IP design objects implement pattern generators (either random or algorithmic), results compression, the collection of diagnostic data, and precision timing for at-speed delivery of the tests. The BIST solution cost-effectively replaces most of the ad-hoc DFT methods in use today and the time-consuming task of creating functional test patterns. BIST seamlessly integrates multiple disciplines:

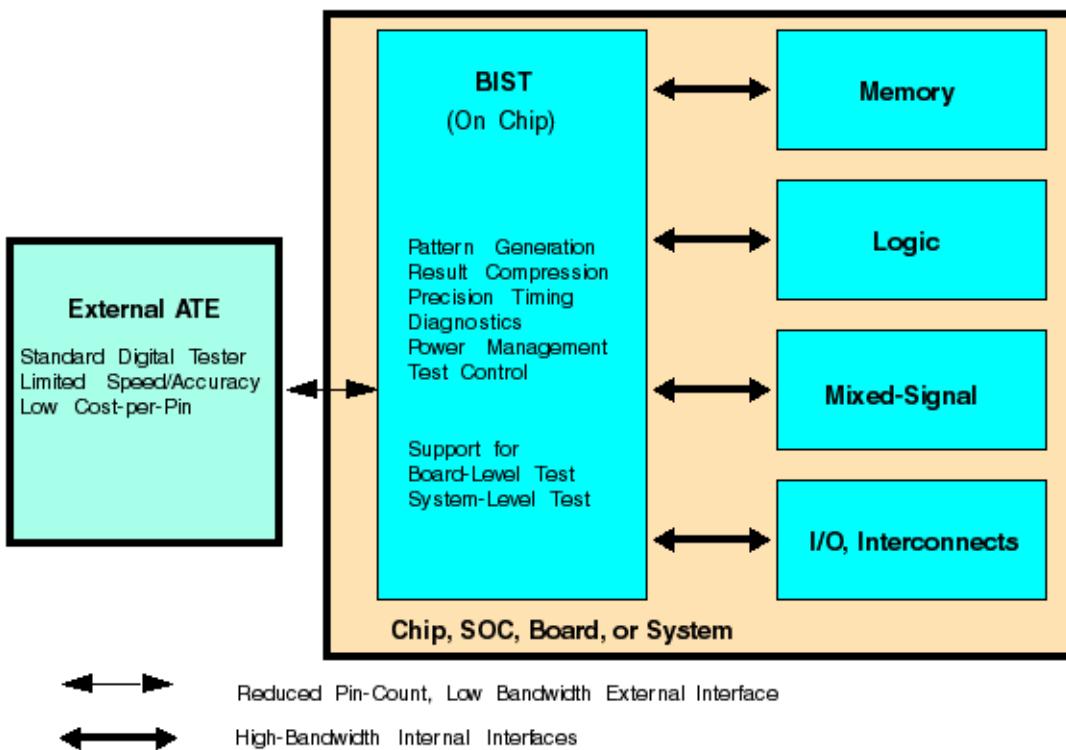
- DFT features, such as scan.
- Precision, high-speed timing for at-speed test.
- Test support for many different block types (logic, memories, processors, and analog circuitry).
- Capabilities for diagnosis and characterization.

Because the test technology is embedded, it provides benefits throughout the product life cycle. The aim of the BIST approach is to design in a chip all ATE features that are block specific or bandwidth limited by chip I/O, as [Figure 2-9](#) illustrates.

- On-chip data generation reduces the volume of external patterns and can be customized per block type.

- On-chip go/no-go and diagnostic data compression reduce ATE data logging.
- On-chip timing generation achieves true at-speed test that can scale to match process performance.

Figure 2-9. BIST: Solving the Bandwidth Problem

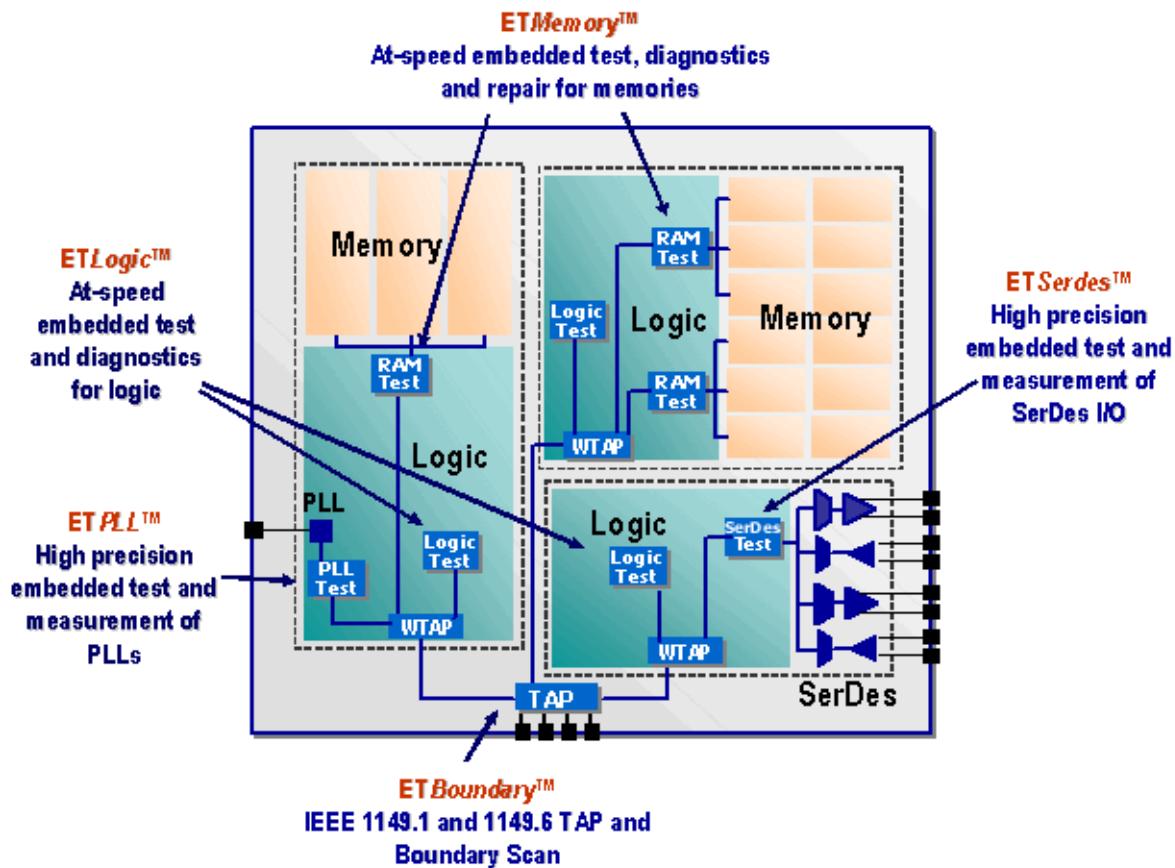


At the chip, board, and system levels, BIST provides the following key advantages:

- Cost-effective at-speed test of logic, memory, cores, mixed-signal modules, and board-level interconnect.
- Diagnostics and debug for random logic, embedded memories, mixed-signal cores, and legacy cores at the chip level.
- Diagnostics and debug for I/Os, interconnects, and memory modules at the board and system levels.

[Figure 2-10](#) illustrates Mentor Graphics' BIST products. Mentor Graphics' overall solution is based on a hierarchical access infrastructure based on the IEEE 1149.1 standard test access port (TAP) and the IEEE 1500 core test access interface (WTAP in the diagram). The appropriate type of BIST controller is used with each type of circuit to be tested—for example, memory, logic, SerDes or phase-locked loop. Details of each of the above types of BIST capabilities are described in the following sections.

Figure 2-10. Mentor Graphics BIST Products



Test Access Port and Boundary Scan

The IEEE 1149.1 Test Access Port (TAP) and Boundary Scan technology was developed in the late 1980s by the Joint Test Action Group (JTAG), and was standardized in 1990 by the IEEE. It defines a chip-level test structure that is used to implement a simplified board and system-level test strategy.

The IEEE 1149.1 standard is based on the concept of a serial shift register around the boundary of the device. The term *boundary scan* derives from this concept. Adherence to the IEEE 1149.1 standard facilitates interoperability between chips from different vendors. The standard is supported by numerous suppliers of commercial tools and ATE equipment.

Boundary-scan (BScan) design is a DFT method that is applied to the input and output pin circuitry of a chip to enhance accessibility and testability. Through BScan, each I/O bonding pad is associated with a combination of latches, flip-flops, and multiplexers that, in test mode, can be configured in several ways to perform the following basic test-mode functions:

- Sample or force data on inputs.

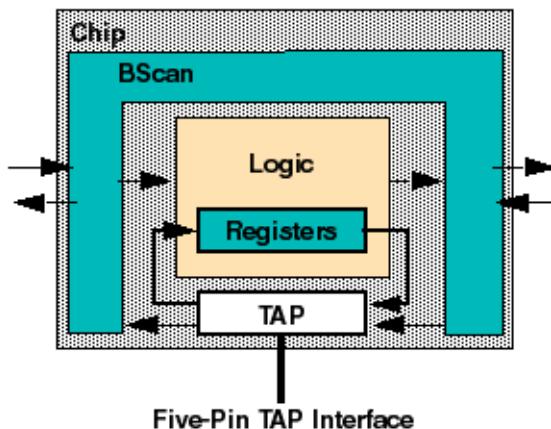
- Sample or force data on outputs.
- Force input data and sample output data on bi-directionals.
- Selectively disable or enable each output.

The IEEE 1149.1 standard provides for boundary-scan cells and a five-pin TAP. These pins include the following:

- *TDI*—Test data-in
- *TDO*—Test data-out
- *TCK*—Test clock
- *TMS*—Test-mode select
- *TRST*—Test reset (optional)

These pins provide a standard protocol for loading and unloading TAP instructions, boundary-scan chains, and internal scan chains, as [Figure 2-11](#) illustrates. The protocol also defines standard TAP instructions for test operation modes.

Figure 2-11. BScan Access Using the Five-Pin TAP Interface



Data can be shifted through the shift register in serial mode, starting from a dedicated *test data-in* (TDI) chip input pin and terminating at a *test data-out* (TDO) chip output pin. A *test clock* (TCK) is fed through another dedicated chip input pin. The mode of operation is controlled by a dedicated *test mode select* (TMS) control input pin.

By applying the appropriate pattern to the TDI, TDO, and TMS pins, the TAP can be used to place the chip into any desired test mode. The standard specifies a number of default test modes, including internal test mode, external test mode, and bypass mode.

The key benefits of the IEEE 1149.1 TAP and boundary-scan combination are the following:

- Provides common access protocol for all test features in the chip, including Mentor Graphics' BIST controllers.
- Supports manufacturing test at multiple levels through the internal and external test modes.
- Enables low-cost chip test and burn-in, requiring contact of power pins, TAP interface pins, and clock pins. Contact occurs through low-cost testers and probes. Such testing applies to all levels of packaging of the product (wafer, chip, board, and system).
- Reduces test pattern development and debugging time at all levels of packaging, resulting in faster time to market. Pattern development and debugging are reduced because access to all chip test features is identical for all chips. Additionally, the IEEE 1149.1 standard is universally supported by many tool and ATE vendors.

Logic BIST

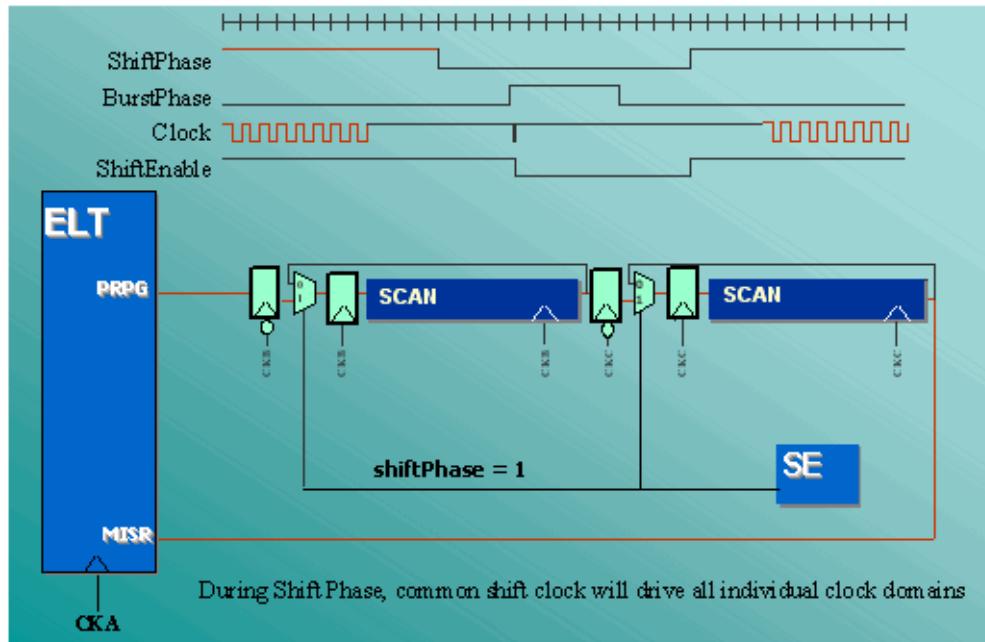
Mentor Graphics provides an at-speed logic test capability using a patented, true at-speed, multi-frequency, multi-domain logic BIST approach. The logic BIST capability is based on the extension of a scan circuit (usually full scan) into a self-test version. This self-test is performed using a pseudo-random pattern generator (PRPG) as stimuli generator and a multiple input signature register (MISR)-based cyclic-redundancy checker (CRC) for output results compression. The logicBIST controller, commonly referred to as the embedded logic Test controller (ELT), consists of the PRPG, the MISR, and a state machine capable of operating at full application speeds.

Logic BIST Operation

The logic BIST sequence of operation is as follows:

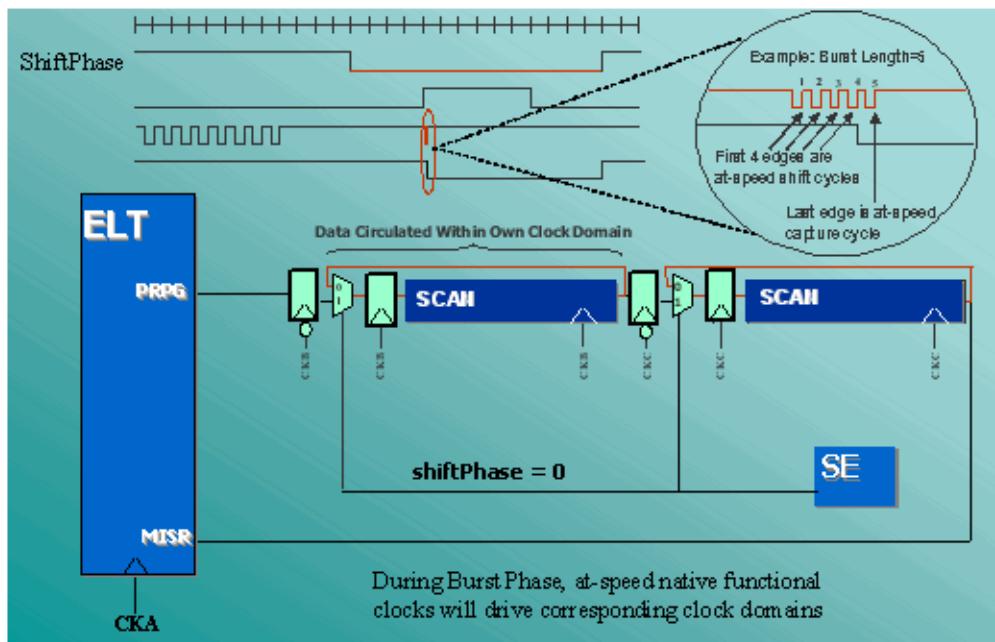
- During the *Shift* phase, random patterns generated by the PRPG are loaded/unloaded into the scan chains at a common frequency, that is independent of the functional speed of the clock domain. The shift phase frequency is adjustable at device run time that allows you to trade-off between test quality, power requirements, and test time. The clock that is used during the shift phase is referred to as the *Shift Clock*. Refer to [Figure 2-12](#) for more information.

Figure 2-12. Logic BIST Shift Phase Operation



- Once all scan chains are loaded, the scan chains are closed into rotating segments. This is known as the *Burst Phase*. Data inside each segment is rotated at the true functional frequency to create at-speed activity. The number of rotations (*burst length*) and the frequency of rotation (burst clock frequency) are again adjustable at runtime. [Figure 2-13](#) provides a pictorial representation of the *burst phase*.

Figure 2-13. Burst Phase Operation of the BurstMode Logic BIST



- At the end of the rotation phase, a single capture cycle captures the data into the scan flops and responses are compressed by the MISR.
- At the end of the self-test cycle, when the last random pattern has been applied, the final signature is scanned out from the MISR and compared to a reference signature by the external ATE.

Diagnosis

With logic BIST, several levels of diagnosis are available. MISR signatures, PRPG seeds, and all other registers of the BIST controller can be unloaded and inspected through a serial interface for diagnostic purposes.

The following features are available for device failure diagnosis:

- Signature unload at the end of individual logicBIST trial (scan pattern) or a range of trials.
- Scan flop unload with the captured values at the end of a single logicBIST trial. By comparing the unloaded values to the expected capture values, failures can be narrowed down to the cone of logic captured by a single flop.
- Selectable burst clock frequency between the shift clock or functional clock to diagnose speed related failures.
- Adjustable burst length to diagnose Multi-cycle paths, noise and IR drop issues.

Power

By default, all output drivers are turned off to minimize power consumption during logic BIST. However, the power consumption of the chip can still exceed the maximum ratings when testing at speed. This is due to the higher level of activity of the circuit caused by the application of random patterns.

Mentor Graphics' bust mode logic BIST has a run-time programmable power-level feature that allows control of the average power and peak power without sacrificing at-speed testing. This is done by adjusting the scan rate, the number of burst cycles (*burst length*), and the spacing between the burst pulses.

For details about the logic BIST capability, refer to Chapter 5, “[Performing Logic Test Diagnostics](#).”

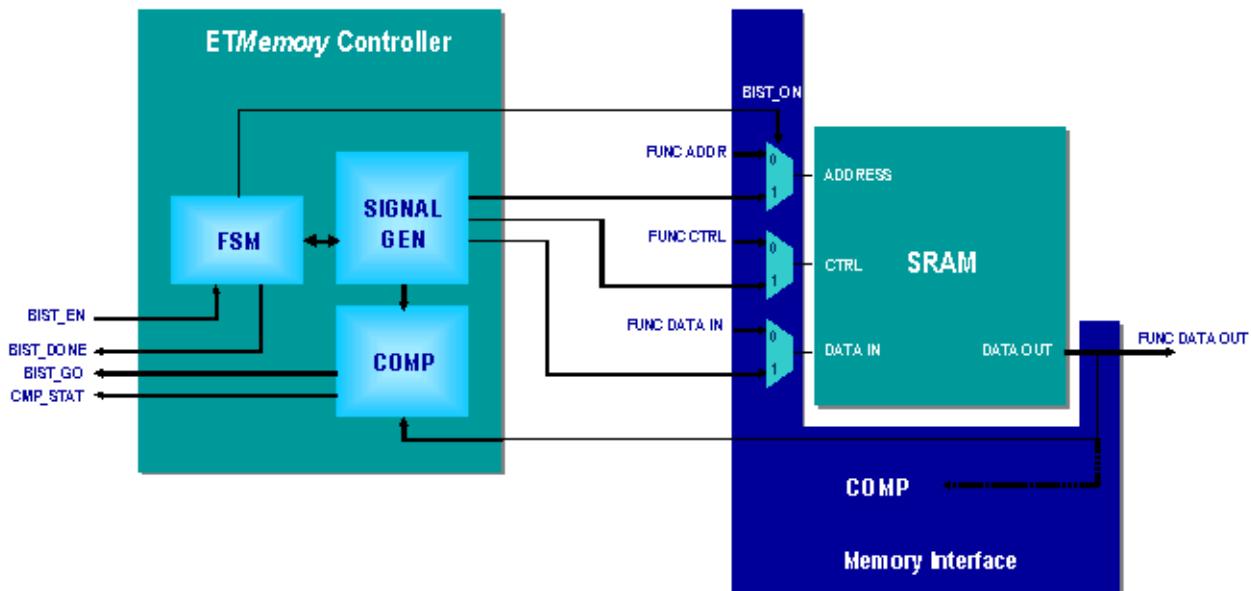
Memory BIST

Memory BIST eliminates the design effort needed to make embedded memories accessible for external tests and provides at-speed self-test using standard memory testing patterns. Mentor

Graphics' memory BIST provides a patented, deterministic BIST for embedded single and multiple-port SRAMs, ROMs, and DRAMs.

Figure 2-14 illustrates Mentor Graphics' basic memory BIST architecture.

Figure 2-14. Basic Memory BIST Architecture



Algorithms and Coverage

The memory BIST controller implements one of a number of available March-based test algorithms which can be serialized to dramatically reduce routing and gate area yet allow for at-speed BIST operation. The algorithms cover a large number of defects (stuck cells, address decoder faults, all two-bit coupling faults, stuck-open access transistors, write-recovery faults, destructive reads, and others). A *Checkerboard* algorithm is also included to detect coupling faults based on a physical map. The *Checkerboard* algorithm can also be combined with the *March* algorithm to test RAM retention time.

A patented *ShadowRead* and *ShadowWrite* test scheme for multiple-port memories yields superior quality. These tests cover bit-line shorts and word-line shorts that belong to different ports.

The controller also supports a two-pass, read-only algorithm to test ROMs. The two-pass algorithm eliminates possible error-masking for higher coverage.

Mentor Graphics' programmable memory BIST allows any number of user-defined memory test algorithms to be either hard-coded into the BIST controller at design time (hard programming option) or downloaded into the controller at test time through the TAP (soft programming option).

Diagnosis

Several features of Mentor Graphics' memory BIST are available for diagnosing failures. The DONE output of the controller is used to indicate whether the failure occurred in the memory itself or the controller. When multiple memories are tested in parallel, a separate go/no-go signal can be generated for each one in addition to the global go/no-go signal to locate any failing memories. Optional comparator status outputs can be monitored in real time to log each compare error that occurred. The diagnostic resolution is adjustable down to the bit level.

Another memory diagnostic capability is a Stop-On- N^{th} -Error feature that can stop the controller after the n^{th} miscompare and scan out all relevant information on the failure through the IEEE 1149.1 TAP interface. The embedded test controller can then resume testing and stop on the next error.

For details about the memory BIST capability, refer to Chapter 4, “[Performing Memory BIST Diagnostics](#).”

Built-In Redundancy Analysis and Self-Repair

Redundancy analysis is available in Mentor Graphics' memory BIST to support repairable memories. All row and/or column redundancy schemes are supported. The redundancy analysis is performed during the execution of the memory BIST controller. The repairable status and the fuse repair map can be scanned out at the end of the execution for each of the memories containing redundant elements.

Mentor Graphics' memory BIST also supports full on-chip self-repair. An on-chip fuse controller is added to program the repair information into an embedded programmable fuse array during manufacturing test. The fuse controller also serves to read out the programmed fuse info from the fuse array and distribute it to the memories during chip power up.

PLL BIST

Tessent PLLTest is a BIST that measures and tests the performance of PLLs (also DLLs and FLLs). Unlike conventional PLL BISTS, Mentor Graphics' BIST solution connects to only the standard inputs and outputs of the PLL, and it does not use delay lines. It performs production-speed diagnostic tests of many parameters, uniquely ranging from picosecond jitter to millisecond lock times. It validates most of the parameters that a designer considers during a PLL design.

Mentor Graphics' solution can verify parameters of a PLL with picosecond accuracy at wafer-probe, package test, and board test. This includes jitter, duty cycle distortion, and phase delay. The under-sampling test techniques used by the BIST provide unlimited measurement resolution and frequency scalability. This is achieved by using a single latch or D-type flip-flop to perform the under-sampling, and generating its sampling clock with an off-chip telecom-quality PLL or another PLL on-chip, adjusting its frequency to control the basic sampling

resolution and measurement bandwidth: an extremely flexible and powerful aspect of the same ULTRA concept used in Tessent SerdesTest. Because the BIST circuitry is purely digital, synchronous, and embedded, its measurement noise floor is lower than for any external test approach.

For details about the PLL BIST capability, refer to the [Tessent PLLTest User's Manual](#).

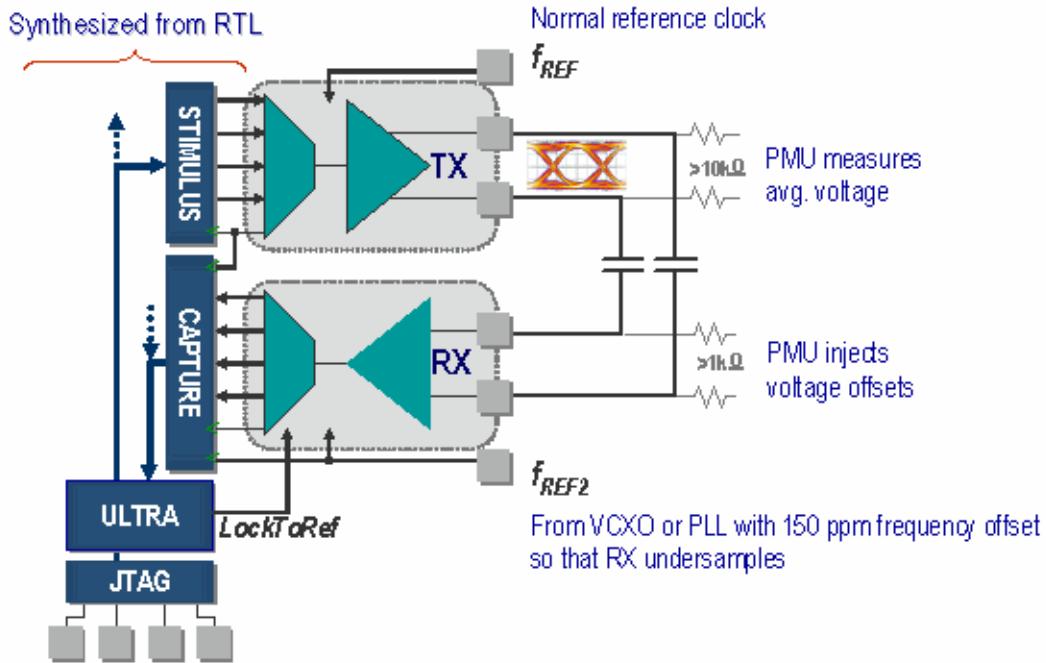
Tessent SerDes BIST

Tessent SerDes Test is a BIST that structurally measures and tests SerDes performance, typically using the standard serial loopback shown in [Figure 2-15](#). Unlike conventional specification-based testing, Mentor Graphics' BIST solution performs production-speed diagnostic tests of the individual parameters that determine the signal-eye opening and, uniquely, the receiver's sampling point within the eye. It validates the parameters that a designer considers during a SerDes core design, using circuitry that can achieve unlimited time resolution.

Mentor Graphics' solution can verify all the parameters of a SerDes channel with sub-picosecond accuracy at wafer-probe, package test, and board test. This includes jitter and distortion elements produced by the transmitter or within the receiver.

The super-Nyquist test techniques used by the BIST solution provide unlimited measurement resolution and bandwidth scalability. This is achieved by using the receiver itself to perform the under-sampling, and adjusting its reference frequency off-chip to control the basic sampling resolution and measurement bandwidth: an extremely flexible and powerful aspect of the ULTRA concept. Because the BIST circuitry is also digital, synchronous, and embedded, its measurement noise floor is lower than for any external test approach.

Figure 2-15. Tessent SerDes BIST Architecture



The benefits of Tessent SerDes BIST include the following:

- Lowest Cost-of-Test and Time-to-Volume
 - Fast, multi-gigahertz I/O test, on any tester
 - Unlimited number of lanes and serial data rate
 - Fast silicon bring-up - days instead of months
 - Use at wafer-sort, packaged IC, and board test
- Diagnostic Tests that Maximize Yield and Quality
 - Measures waveform, jitter, and jitter tolerance
 - Unique tests and comprehensive fault coverage
 - Sub-picosecond accuracy
 - Repeatability that permits reduced guardbands
 - Measures high and low frequency jitter separately
 - Golden PLL-like method, as required by standards

For more information about the Tessent SerDes BIST capability, see the [*Tessent SerdesTest User's Manual*](#).

Chapter 3

Diagnosing Device Failures

This chapter describes in general how to diagnose device failures. The following three chapters provide detailed information on the specific diagnostics:

- Performing Memory BIST Diagnostics
- Performing Logic Test Diagnostics
- Performing I/O, TAP, WTAP Tests and Diagnosis

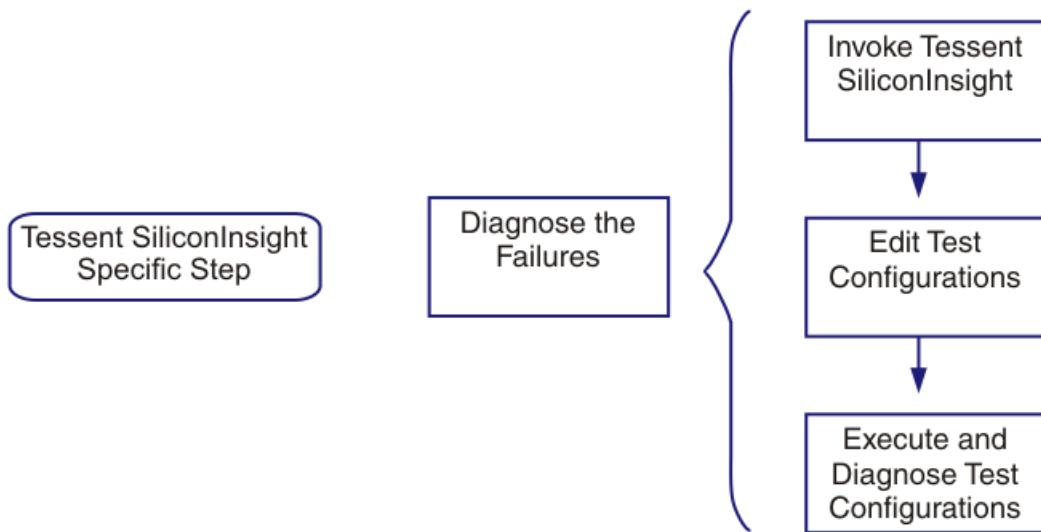
Chapter topics follow this sequence:

Basic Tesson SiliconInsight Flow	35
Invoking Tesson SiliconInsight	36
Invoking Tesson SiliconInsight in Offline Mode	37
Invoking Tesson SiliconInsight in the USB Mode	40
Invoking Tesson SiliconInsight in the LVReady ATE Mode	41
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Adding Test Groups	49
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Executing and Diagnosing Test Configurations	52
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Basic Tesson SiliconInsight Flow

Figure 3-1 shows the basic flow for Tesson SiliconInsight once you have configured the tool for your environment.

Figure 3-1. SiliconInsight-Specific Operations



The sub-steps of the Tesson SiliconInsight process are:

1. **Invoking Tesson SiliconInsight**—Launch the Tesson SiliconInsight GUI. The Tesson SiliconInsight GUI is launched differently depending on the different modes of operation—*offline* or *LVReady ATE*.
2. **Editing Test Configurations**—Optionally, edit the Tesson SiliconInsight test configuration either to optimize for the production flow or to create diagnostic test benches. A default test configuration called *default.config_eta* is always provided by the design group and is included in the device’s LVDB database.
3. **Executing and Diagnosing Test Configurations**—Execute the test configurations and perform diagnosis of the failed test steps.

The following sections provide more details for each of the above sub-steps.

Invoking Tesson SiliconInsight

The Tesson SiliconInsight invocation involves launching the Tesson SiliconInsight GUI. The Tesson SiliconInsight GUI is launched differently depending on the different modes of operation as explained in the following sections:

- [Invoking Tesson SiliconInsight in Offline Mode](#)
- [Invoking Tesson SiliconInsight in the USB Mode](#)
- [Invoking Tesson SiliconInsight in the LVReady ATE Mode](#)

A common technique used for all three modes is described in the section “[Specifying the Tesson SiliconInsight Files Using GUI](#).”

Invoking Tesson SiliconInsight in Offline Mode

In the *offline* mode of operation, the Tesson SiliconInsight server is not connected to the test program. This mode of operation is best suited for creating/editing the test configuration and validating the pin map file. You invoke Tesson SiliconInsight software in the *offline* mode using the following command-line options:

```
tesson -siliconinsight -ate \
-server offline \
-lvdb <LVDBName> \
-pinmapFile <pinmapFileName> \
-configFile <testConfigFileName>
[-bondingOption <bonding_option>]
```

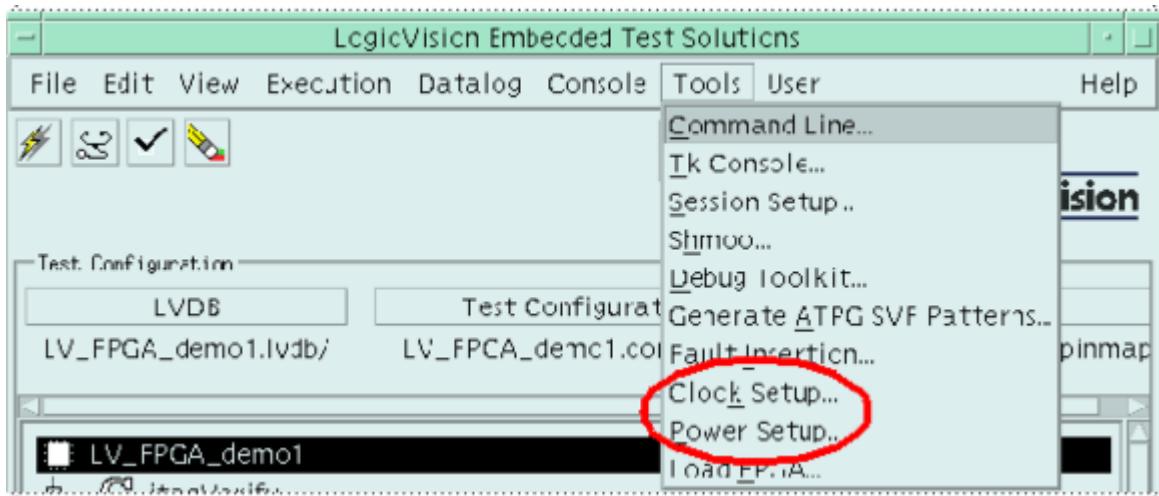
where valid values are as follows:

- **-server offline**—instructs Tesson SiliconInsight server to be invoked in the offline mode. In this mode, the server will not try to connect to a test program. This is a mandatory argument.
- **-lvdb <LVDBName>**—specifies the full hierarchical file system path to the LVDB. This is an optional argument, as the LVDB can be specified from the Tesson SiliconInsight GUI as well.
- **-pinmapFile <pinmapFileName>**—specifies the full hierarchical file system path to the pin. This is an optional argument, as the pin map file can be specified from the Tesson SiliconInsight GUI as well.
- **-configFile <testConfigFileName>**—specifies the full hierarchical file system path to the Tesson SiliconInsight test configuration file. This is an optional argument, as the configuration file can be specified from the Tesson SiliconInsight GUI as well.
- **-bondingOption <bonding_option>**—Specifies one of the bonding options, as they appear in the *tcm* file, when the LVDB has multiple bonding options.

Refer to “[Specifying the Tesson SiliconInsight Files Using GUI](#)” for an alternative way to specify the input files.

After the Tesson SiliconInsight GUI window is displayed, you need to perform the power supply and clock setup operations, before you proceed to diagnose the device. You invoke the power and clock setup dialog boxes by choosing the **Tools > Power Setup** menu option as shown in [Figure 3-2](#).

Figure 3-2. Invoking the Clock and Power Setup Menu Tessent SiliconInsight Desktop with GPIB Option

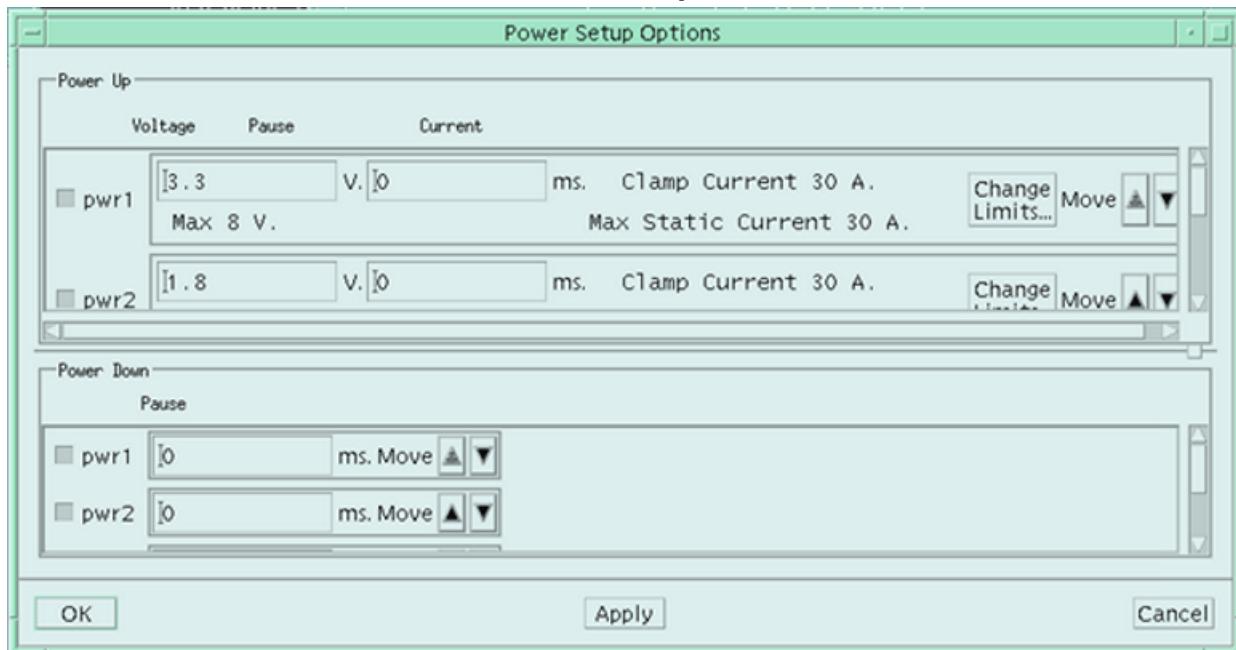


Power Supply Setup

The power supply setup allows you to define the voltage and current requirements of your device. The **Power Setup Options** dialog box is displayed as shown in [Figure 3-3](#). The box is configured to have up-to four power supplies, but is shipped with two power supplies by default. For each power supply, specify the following values:

1. Specify the power up and power down sequence using the arrows labeled **Move**.
2. In the power up sequence, specify the voltage to be supplied, pause time in milliseconds, and the clamp current limits. Use the **Change Limits** dialog box to change the current limits.
3. In the power down sequence, specify the pause time for each power supply.

Figure 3-3. Power Setup Options Dialog Box Tesson SiliconInsight Desktop with GPIB Option

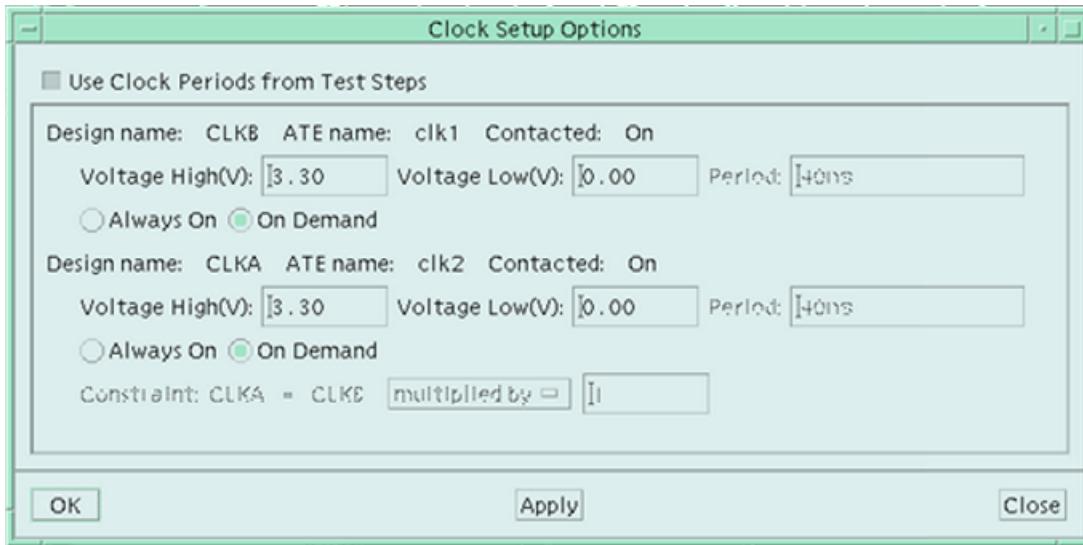


Clock Setup

The clock setup allows you to define the clock levels and periods required for your device. The Clock Setup Options dialog box is displayed as shown in [Figure 3-4](#). The box is configured to have up-to two frequency generators. Using the Clock Setup Options dialog box, specify the following values:

- Whether the clock periods should be taken from the values specified in the test steps in the Tesson SiliconInsight test configuration or if the clock periods are controlled from the asynchronous clock generators,
- The voltage levels that define the logical high and logical low,
- Whether the clocks should be always turned on or if they should turn on as demanded by the test step in the test configuration, and
- The clock periods and ratio between the clock frequencies, when the clock periods are *not* taken from the test configuration.

Figure 3-4. Clock Setup Options Dialog Box Tesson SiliconInsight Desktop with GPIB Option



Invoking Tesson SiliconInsight in the USB Mode

In the USB mode of operation, the Tesson SiliconInsight software is running on a computer (laptop/desktop) using Linux. The TAP of the DUT is connected to the USB port of the computer through a USB-JTAG adaptor. This is the simplest mode of operation in terms of Tesson SiliconInsight setup. You invoke Tesson SiliconInsight software in the USB mode with the following command-line options:

```
tesson -siliconinsight -desktop \
    -lvdb <LVDBName> \
    -pinmapFile <pinmapFileName> \
    -configFile <testConfigFileName>
    [-bondingOption <bonding_option>]
```

where the valid values are as follows:

- **-lvdb <LVDBName>**—specifies the full hierarchical file system path to the LVDB. This is an optional argument, as the LVDB can be specified from the Tesson SiliconInsight GUI as well.
- **-pinmapFile <pinmapFileName>**—specifies the full hierarchical file system path to the pin map file. Only the TAP pins must be mapped. The rest of the pins of the device must be declared as uncontacted.
- **-configFile <testConfigFileName>**—specifies the full hierarchical file system path to the Tesson SiliconInsight test configuration file. This is an optional argument, as the configuration file can be specified from the Tesson SiliconInsight GUI as well.
- **-bondingOption <bonding_option>**—Specifies one of the bonding options, as they appear in the *tcm* file, when the LVDB has multiple bonding options.

Refer to “[Specifying the Tesson SiliconInsight Files Using GUI](#)” for an alternative way to specify the input files.

In this setup, the DUT is powered and clocked by external instruments. This product is ideal for diagnosis of devices in a self-powered and self-clocked system boards.

Supported USB-JTAG Adaptors

For specific information on supported USB-to-JTAG adaptors, refer to the “[Setting Up and Using Tesson SiliconInsight Desktop](#).”

Invoking Tesson SiliconInsight in the LVReady ATE Mode

In *LVReady* ATE mode of operation, the Tesson SiliconInsight server is connected to the test program running on an *LVReady* ATE platform. This mode of operation is best suited to debugging or diagnosing the device failures using the ATE that you are already familiar with. Launching Tesson SiliconInsight in this mode is no different than running your test program on the ATE. With the appropriate *.eta_tp_setup* file settings, the test program will launch the Tesson SiliconInsight server and the Tesson SiliconInsight GUI. You can then interact with the Tesson SiliconInsight GUI to perform the diagnostic tasks. You must ensure that the following steps are performed, before invoking Tesson SiliconInsight on an *LVReady* ATE platform:

- The *.eta_tp_setup* file contains the following entry:

```
TP_RUNMODE = debug;
```
- The test program should only contain the single API call: [ETAStrt\(\) API](#). The format of this call will be dependent on the specific ATE system. You do not need to invoke *ETAExecuteStep()* call, since the test step execution is controlled from the Tesson SiliconInsight GUI.

Specifying the Tesson SiliconInsight Files Using GUI

You can load the following Tesson SiliconInsight required files using the GUI, instead of specifying them on the command line:

- The Mentor Graphics Data Base (LVDB)
- A Tesson SiliconInsight Test Configuration file
- The Tesson SiliconInsight pin map file

Note

 You can use this method of specifying the Tessent SiliconInsight files in the offline mode only.

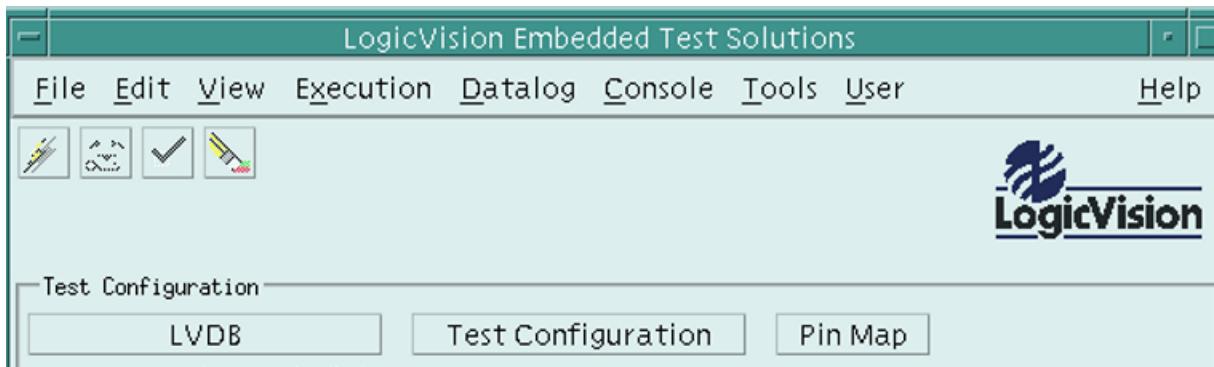
When you launch the Tessent SiliconInsight GUI without specifying the required files, it will be displayed with a blank configuration window as shown in [Figure 3-5](#).

Figure 3-5. Tessent SiliconInsight GUI With a Blank Configuration Window



You can then click on the buttons labeled **LVDB**, **Test Configuration**, and **Pin Map** to load the LVDB, Tessent SiliconInsight Test Configuration, and the pin map file respectively, as shown in [Figure 3-6](#).

Figure 3-6. File Loading Buttons on the Tesson SiliconInsight GUI



Each of these buttons would bring up a file selection dialog box that allows you to specify the appropriate file.

Creating a Tesson SiliconInsight Pin Map File

The Tesson SiliconInsight pin mapping file provides a mapping between design pin names and the ATE pin names. The ATE pin names are the names used in the test program to refer to the device pins mapped to specific tester channels. Additionally, you can use this file to define which device pins are contacted by the tester.

Since the LVDB only contains the design data, this information is required by Tesson SiliconInsight so that appropriate test patterns and timing information can be generated that will be understood by the test program.

To prepare the Tesson SiliconInsight pin map file, perform these operations:

1. [Locating the Template Pin Map File](#)
2. [Editing the Template Pin Map File](#) to specify the mapping. You might need some information from the design engineer to complete this step.

Locating the Template Pin Map File

You need to locate the template Pin Map file in the LVDB and make a copy of it.

The LVDB generated by the LV Flow tools contains a template pin map file. This file is called `<design name>.pinmap_tpl`. This file is located inside the LVDB. An example template pin map file is shown in [Figure 3-7](#)

Figure 3-7. Template Pin Map File in the LVDB

```

//-----
// This file created by: embeddedTestVerify
// Software version: 5.0b.SP1      Build 20060720.007
// Created on: 08/04/06 08:11:12
//-----
//  

PinMap (car) {  

  Pins {  

    // <design name> : <ATE name> <Tester channel  

    type>;  

    CK33 : CK33;  

    CK25 : CK25;  

    COORD0 : COORD0;  

    COORD1 : COORD1;  

    COORD2 : COORD2;  

    D1 [3] : D1 [3];  

    D1 [2] : D1 [2];  

    ...  

    ...  

  }  

}

```

The template pin map file has the following features:

- All design pin names are listed on the left-hand side.
- The ATE pin names are assumed to be the same as the design pin names and are listed on the first column on the right-hand side of the pin map file entry.
- The optional ATE tester channel type column is omitted. Typically, this information is not required for production testers that have many tester channels. A desktop diagnostic tester, like the *Validator Debug Station* from Mentor Graphics, would require you to specify the tester channel type assignment.

Editing the Template Pin Map File

You edit the template Pin Map file to specify the mapping. You might need some information from the design engineer to complete this step.

The template pin map file could be edited in a text editor or could be generated by a custom program. Follow these steps to generate a valid pin map file:

- If the design pin names and the ATE pin names are the same for the device, and each device pin is mapped to a unique test channel, then you can simply use the template pin map file without any changes. Otherwise, follow rest of the steps.
- For each device pin that is contacted by a tester channel, edit the entry to the right-hand side of the ‘:’ (colon) to specify the ATE pin name.
- For each device pin that is uncontacted by a tester channel, specify a ‘-’ (dash) on the right-hand side of the ‘:’ (colon).

- Typically, you will declare all pins as uncontacted, and you will need to specify the mapping only for the following pins, except for the I/O test steps in which all the device pins appear in the pattern:
 - TAP pins (TDI, TDO, TMS, TCK, TRST)
 - TAP Compliance Enable pins that must be held at constant logical values during the test mode
 - Asynchronous set/reset pins that must be held at constant logical values during the test mode
 - Memory BIST CompStat pins which are monitored for diagnostic results (for *ETDiagnostics* usage only)

[Figure 3-8](#) provides an example of the edited pin map file.

Figure 3-8. Example of a Final Pin Map File

```
PinMap (<car>) {
    Pins {
        // <design name>: <ATE name>
        CK33          : CLK1;
        CK25          : CLK2; ← ATE pin names—different
        D1[3]         : DATA3;      from design pin names
        D1[2]         : DATA2;
        COORD1        : -;           ← Uncontacted pin
        COORD0        : COORD0;
        COORD2        : COORD2; ← ATE pin names—the
        ...           . . .           same as design pin names
    }
}
```

Pin Map File Syntax

[Figure 3-9](#) summarizes the Tesson SiliconInsight pin map File syntax. Detailed descriptions of wrappers and properties available within the pin mapping file follow the figure.

Figure 3-9. Tesson SiliconInsight Pin Map File Syntax

```
PinMap (<pinMapName>) {
    The Pins Sub-Wrapper {
        <designPinName>: <ATEPinName> [<ATEChannelType>] / -];
        .
        . //Repeat for each design pin requiring a mapping.
        .
    }
    The PullUps Sub-Wrapper {
```

```

<designPinName>;
.
. //Repeat for each design pin tied to a pull up.
.
}
The PullDowns Sub-Wrapper {
<designPinName>;
.
. //Repeat for each design pin tied to a pull down.
.
}

```

The PinMap Wrapper

The ***PinMap*** wrapper allows you to define the pin map name.

Syntax

The ***PinMap*** wrapper begins with the following:

Pinmap (<pinMapName>) {

where *pinMapName* is the name of a pin map.

Usage Conditions

None

The Pins Sub-Wrapper

The ***Pins*** sub-wrapper contains the list of pin mappings. Each line within this wrapper defines the mapping for one design pin.

Syntax

The available syntax for each line within the ***Pins*** sub-wrapper is as follows:

<designPinName>: <ATEPinName> [<ATEChannelType>] / -];

where valid values are as follows:

- *designPinName*—is the name of the pin as specified within the design netlist.
- *ATEPinName*—is the name of the pin as specified in the test program.
- *ATEChannelType*—is the name of the tester channel type to which the pin is connected. Each *ATEChannelType* refers to a particular channel resource definition provided in the tester description file (TDF).
- dash (-)—indicates that the pin is not connected to the tester. For an example of this value, refer to Example 3 below.

Usage Conditions

These usage conditions apply:

- If the *ATEChannelType* is omitted from a pin mapping, then the pin is assumed to be connected to default tester channel resources. Default tester channel resources are hard-coded as described by the following TDF *ATEChannel* wrapper:

```
ATEChannel (default) {
    Control {
        Type: ThreeState;
        MultiEdge: Yes;
    }
    Observation {
        Type: ThreeState;
    }
}
```

- To specify a pin as being not contacted, you must replace *ATEPinName* with a dash (-). Under this condition, the *ATEChannelType* must be omitted.

 **Note** A pin connected to an asynchronous clock generator on the loadboard should be defined as being not contacted in the Tesson SiliconInsight pin map file.

- If a mapping for a pin is not provided in the Tesson SiliconInsight pin mapping file, then the pin is assumed to be contacted to default tester channel resources, and the *ATEPinName* is assumed to be identical to the *designPinName*.
- You can specify duplicate ATE pin names for asynchronous clocks with the same clock period. Duplicates allow you to test a chip with more clocks. Two embedded test controllers can share a clock in a test step if both controllers have the same clock period. If the controllers are in different test steps, the clock periods can be different.

The following examples shows how the syntax in the *Pins* sub-wrapper can be specified.

Example 1

This example indicates that the pin with design name *dpinA* is referred to as *tpinA* in the test program and is connected to tester channel type *chan1*.

```
dpinA: tpinA chan1;
```

Example 2

This example indicates that the pin with design name *dpinB* is referred to as *tpinB* in the test program and is connected to default tester channel resources.

```
dpinB: tpinB;
```

Example 3

This example indicates that the pin with design name *dpinC* is not contacted by the tester.

```
dpinC: -;
```

Related Information

None

The PullDowns Sub-Wrapper

The **PullDowns** sub-wrapper is used to indicate which chip pins are pulled down.

Syntax

Each line within the **PullDowns** sub-wrapper has the following syntax:

```
<designPinName>;
```

where *designPinName* is the name of a pin as specified within the design netlist.

Usage Conditions

None

Example

This example indicates that the design pins *DataIn3* and *DataIn11* are connected to pull-downs.

```
PullDowns {  
    DataIn3;  
    DataIn11;  
}
```

Related Information

None

The PullUps Sub-Wrapper

The **PullUps** sub-wrapper is used to indicate which chip pins are pulled up.

Syntax

Each line within the **PullUps** sub-wrapper has the following syntax:

```
<designPinName>;
```

where *designPinName* is the name of a pin as specified within the design netlist.

Usage Conditions

None

Example

This example indicates that the design pins *DataIn2* and *DataIn7* are connected to pull-ups:

```
PullUps {  
    DataIn2;  
    DataIn7;  
}
```

Related Information

None

Editing Test Configurations

During this *optional* sub-step, you edit the Tesson SiliconInsight test configuration either to optimize for the production flow or to create diagnostic test benches. A default test configuration is always provided by the design group and is included in the device's LVDB database.

A *test configuration* is a collection of test groups and defines the flow for the embedded test of a particular device. There might be more than one test configuration for a device, each with a different test flow and /or test properties. The default test configuration for a device is provided by the design group and resides in the LVDB. The test configuration files are encrypted and they have the extension `.config_eta`.

To edit a test configuration, you can invoke Tesson SiliconInsight in the *offline* mode as described in the section "[Invoking Tesson SiliconInsight in Offline Mode](#)."

To populate the test configuration tree, perform these operations described in the following sections:

- [Adding Test Groups](#)
- [Creating Test Steps](#)

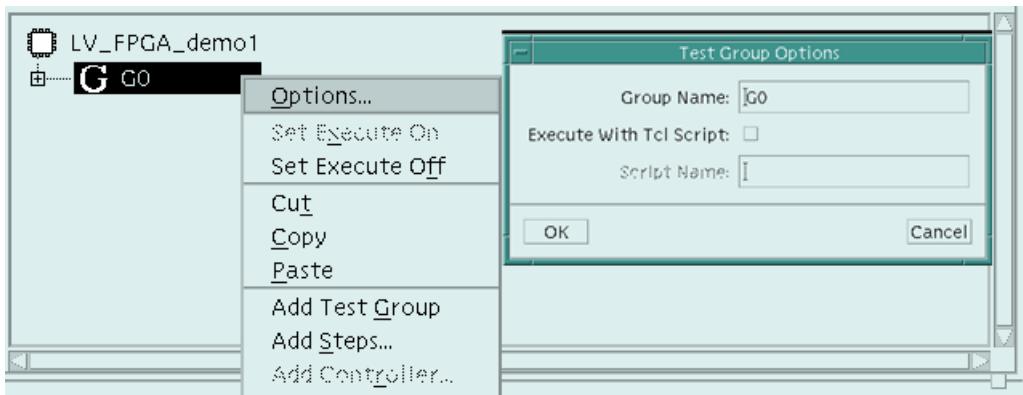
Adding Test Groups

A *test group* is a collection of test steps and ATE steps. All steps in a test group are executed serially.

To create test groups in a test configuration, perform the following operations:

1. Right mouse button click on the root configuration node icon in the **Test Configuration** area and select **Add Test Group**. This adds a test group with default name *G0*.
2. Right mouse button click on the *G0* icon and select **Options** to bring up the **Group Options** panel as shown in [Figure 3-10](#).

Figure 3-10. Launching Group Options Panel



3. In the **Group Options** panel, change the name of the test group *G0* to the desired name - for example *membistVerify* - by typing in the text area displaying the test group name.
4. Click **OK** in the **Group Options** panel.
5. Repeat Steps 1 through 4 to add additional test groups.
6. The test configuration area of the Tessent SiliconInsight GUI main window at this point appears as illustrated in [Figure 3-11](#).

Figure 3-11. Test Configuration Area with Test Groups



7. Save the test configuration by choosing **Save Config** from the **File** menu.

Next, you will create test steps in each of the test groups.

Creating Test Steps

Typically, a *test step* executes one or more embedded test controllers. A test step also can perform other tasks, such as execute an embedded I/O test. You can add one or more test steps to a test group. All of the test steps in a test group are executed serially. You can add one or more controllers to a test step. All the controllers in a test step must be of the same type and are

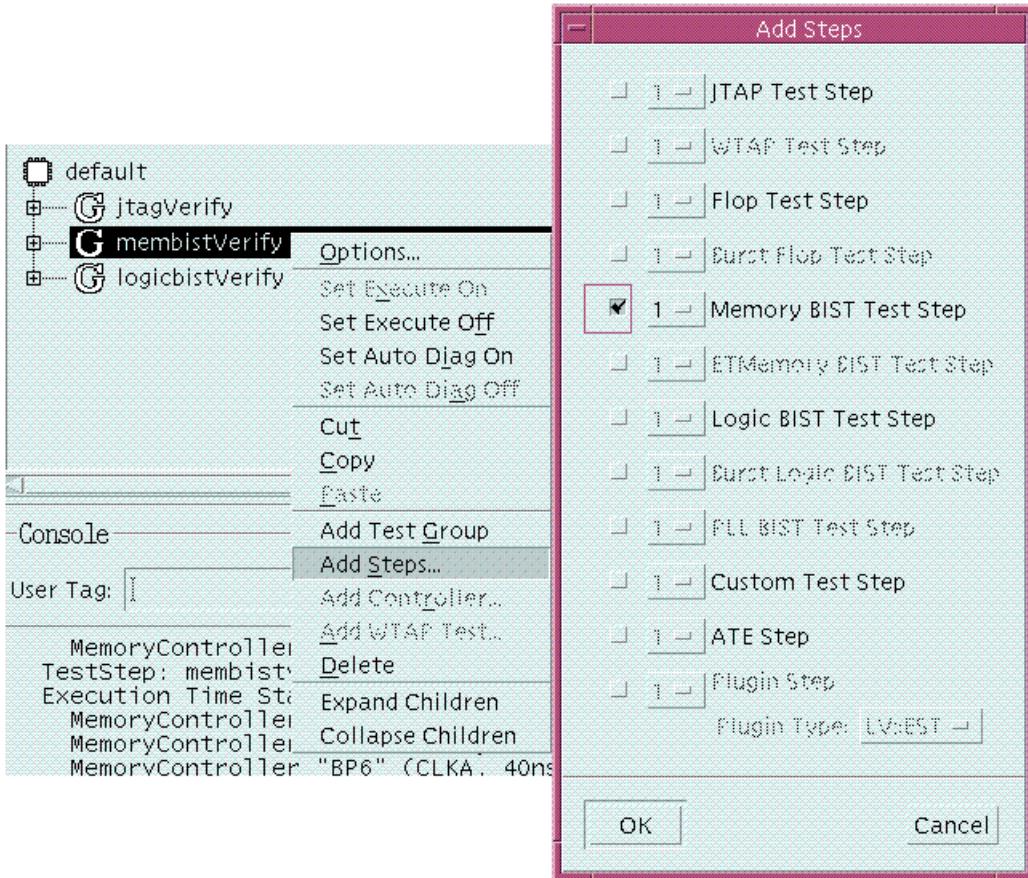
executed in parallel. The test step properties are common to all of the controllers in that test step.

An embedded test controller also can appear in multiple test steps. For example, you can run the controller under different test conditions (such as different clock frequency).

To add a test step to the test group *membistVerify* and then to add the memory BIST controller *BP4*, perform the following steps:

1. Right mouse button click on the *membistVerify* icon in the **Test Configuration** area and select the **Add Steps** menu item. This brings up the **Add Steps** panel.
2. Click on the **Memory BIST Test Step** selection button, as shown in [Figure 3-12](#), to add a single test step for the memory BIST controllers and click **OK**. This adds test step *S0* to the test group *membistVerify*.

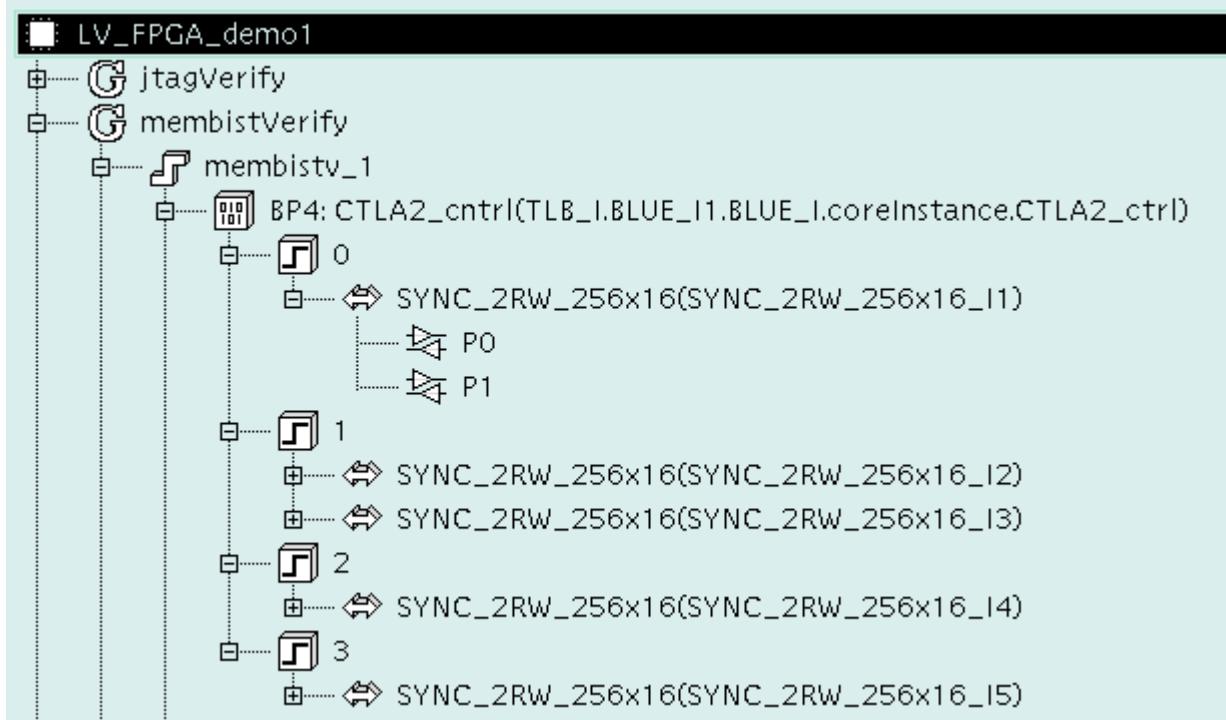
Figure 3-12. Adding A Memory BIST Test Step



3. Right mouse button click on the *S0* icon and select the **Options** menu item to bring up the **Memory BIST Test Step Options** panel.
4. Change the name of the test step *S0* to *mem* by typing the new name in the text area displaying *S0*.

5. You can edit the other options for this test step.
6. To add the Memory BIST controller *BP4* to the test step, right mouse button click on the *mem* test step icon and select the **Add Controllers** menu item to bring up the **Add Controllers** panel. This panel displays the available controllers that can be added to the test step. Select the desired controller and click **OK**. Click on the **Expand** icon to the left of the *BP4* controller node to view the controller steps and memories within the controller. Click on the **Expand** icon to the left of the memory nodes to view the memory ports. At this point, the test configuration area appears as illustrated in [Figure 3-13](#).

Figure 3-13. Test Configuration Area with Test Steps and Controller Steps



7. You can similarly add test steps and controller steps to rest of the test groups in the test configuration.

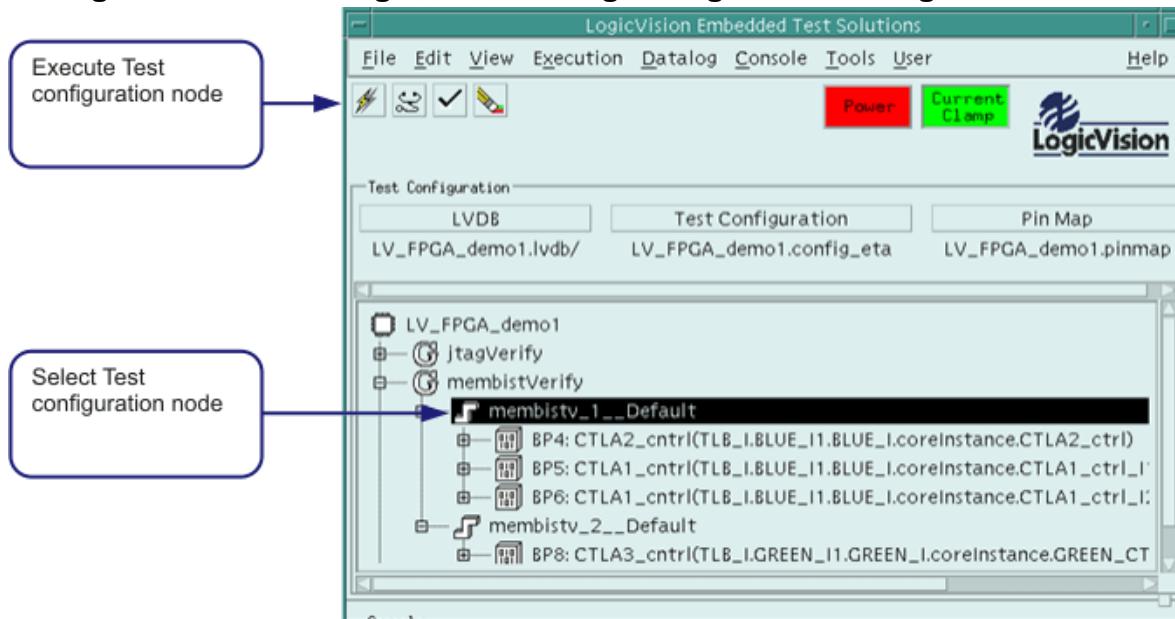
Executing and Diagnosing Test Configurations

Once you have invoked the Tessent SiliconInsight GUI, you can execute the test configurations and perform diagnosis of the failed test steps. You must be running in the USB or the LVReady ATE mode to get meaningful results for execution.

Executing Test Configuration

You can execute the entire test configuration or select one or more test configuration nodes for execution. After you select the test configuration node(s) of interest, simply click on the **Execute** (lightning bolt) button on the tool bar as shown in [Figure 3-14](#).

Figure 3-14. Selecting and Executing a Single Test Configuration Node



Execution Sequence of Events

The following sequence of events occurs during execution:

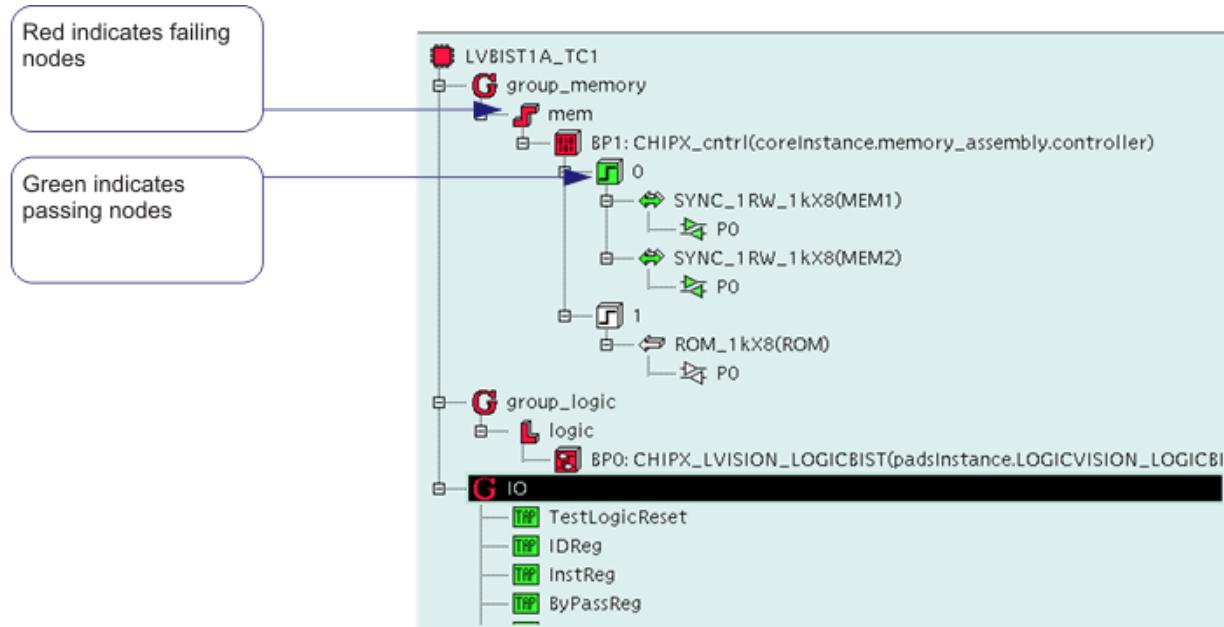
- For each test step executed, the Tesson SiliconInsight server generates ATE patterns if they are not already generated. For example, if you modify one or more test properties, the patterns are re-generated.
- The patterns generated by the Tesson SiliconInsight server are loaded onto the tester hardware if they are not already loaded or if the patterns have changed.
- The patterns loaded on the tester hardware are executed.
- The results of pattern execution are sent back to the Tesson SiliconInsight server.
- The Tesson SiliconInsight server processes the results and reports go/no-go results in the **Console** area of the Tesson SiliconInsight GUI main window. The format of the test results is described in “[Using the Datalog Results](#).”

Tesson SiliconInsight tool menus are context sensitive and some entries are inaccessible (appear as a dimmed menu item) until you select a dependant item. For example, the menu item **Execution > Pattern Loop** is inaccessible until you select a test step.

Execution Results Indication

The colors in the **Test Configuration** area also indicate the pass/fail results of an execution as shown in [Figure 3-15](#).

Figure 3-15. Execution Result Indication



If at least one test group in the test configuration fails, the entire test is reported as failing, and the colors in the **Test Configuration** area change as follows:

- Each of the embedded test controllers that detect failures turn *red*.
- Each of the failing steps turn *red*. A step is reported as failing if at least one embedded test controller in that step detects a failure.
- Each of the failing test groups turn *red*. A test group is reported as failing if at least one step in that test group fails.

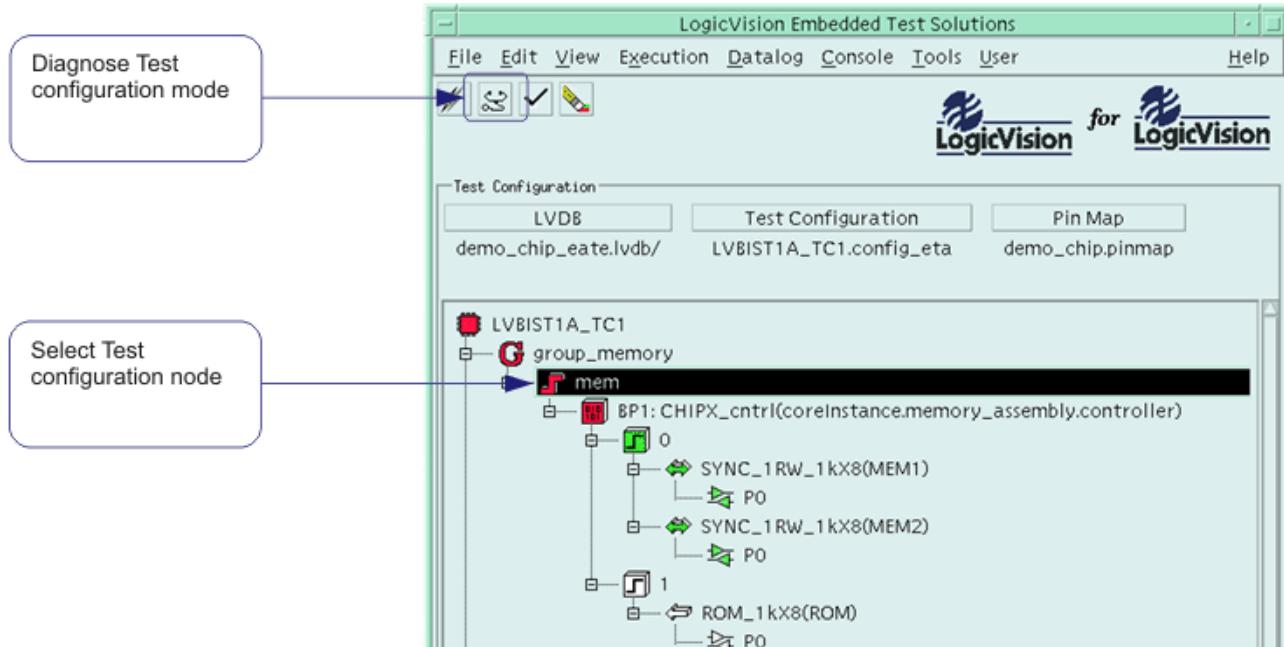
If all test groups in the test configuration pass, the entire test is reported as passing, and the colors in the **Test Configuration** area change as follows:

- Each of the passing embedded test controllers turn *green*.
- Each of the passing steps turn *green*. A step is reported as passing if all the embedded test controllers in that step pass.
- Each of the passing test groups turn *green*. A test group is reported as passing if all the steps in that test group pass.

Diagnosing Test Configuration

You can diagnose either the entire test configuration or select one or more failed test configuration nodes for diagnosis. After you select the failed test configuration node(s) of interest, simply click on the **Diagnose** (stethoscope) button on the tool bar as shown in [Figure 3-14](#) to perform automatic diagnosis. Alternatively, you can perform manual diagnosis by modifying the test step/controller step options and executing the test configuration nodes repeatedly.

Figure 3-16. Selecting and Diagnosing Test Configuration Nodes



Using the Datalog Results

Execution results are automatically datalogged by the Tessent SiliconInsight software when you execute a test from the GUI. The datalog results are printed in the **Console** area along with the status messages from the server. The Tessent SiliconInsight GUI allows you to print the datalog results to a separate window or to a file.

Datalog Format

Datalog for each execution has a single header record that contains the LVDB directory and name, and the test configuration name.

For each test group, datalog results of all steps in that test group are logged. Datalog results of each step are categorized as follows:

- PASSED

- FAILED
- NOT_EXECUTED
- UNKNOWN

If the execution of a step is disabled, then that step is marked NOT_EXECUTED in the datalog result. Datalog results are marked UNKNOWN if the step was executed but the pass/fail results are not available for some reason. For each step, the *Execution Time Stamp* is printed if the step was executed. For each failing step, the failures detected by each embedded test controller are printed.

The format of the datalog results is shown in [Figure 3-17](#).

The detailed datalog format for each controller type (memory, logic, I/O or PLL) is discussed in the corresponding chapters.

Figure 3-17. Datalog Results

```
=====
LVDB Directory:      /home/sai/DocReview/test/demo_chip_eate.lvdb
LVDB Name:          demo_chip_eate.lvdb
Test Config:        demo_chip_config

TestGroup: group_memory
  TestStep: mem (FAILED)
    Execution Time Stamp: 09/09/03 16:55:17
      MemoryController "BP1" (CLKIN, 14.3ns)
      Port "gostatus" failed (IR_STATUS9=0).

TestGroup: group_logic
  TestStep: logic (FAILED)
    Execution Time Stamp: 09/09/03 16:55:17
      LogicController "BP0" (CLKIN, 14.3ns)
      Trial "128" MISR 24-bit signature is: "0xa6edad"
          expected is: "0xa039eb".

TestGroup: IO
  TestStep: Input (FAILED)
    Execution Time Stamp: 09/09/03 16:55:17
      (tck, 200ns)
      Boundary scan pin "IN6" failed IOTest "Input". Actual value is "1" (expected "0").
  TestStep: IDReg (PASSED)
    Execution Time Stamp: 09/09/03 16:55:17
      (tck, 200ns)

TestGroup: group_pll
  TestStep: pll (PASSED)
    Execution Time Stamp: 09/09/03 16:55:17
      PLLController "BP2" (CLKIN, 14.3ns)
=====
```

For detailed information on specific diagnostics, refer to the following chapters:

- [Performing Memory BIST Diagnostics](#)

- Performing Logic Test Diagnostics
- Performing I/O, TAP, WTAP Tests and Diagnosis

Note



To perform Tessent SerdesTest diagnostics with Tessent SiliconInsight, refer to the *Tessent SerdesTest User's Manual*. To perform Tessent PLLTest diagnostics with Tessent SiliconInsight, refer to the *Tessent PLLTest User's Manual*.

Chapter 4

Performing Memory BIST Diagnostics

This chapter provides step-by-step instructions on how to use the Tesson SiliconInsight software to diagnose memory BIST controllers on the DUT.

 **Note** Chapter 7, “[Diagnosing and Validating Memory With Enhanced Stop-On-Nth-Error Test Patterns](#)” describes the particular process for performing Memory BIST diagnostics with enhanced Stop-on-Nth-Error test patterns.

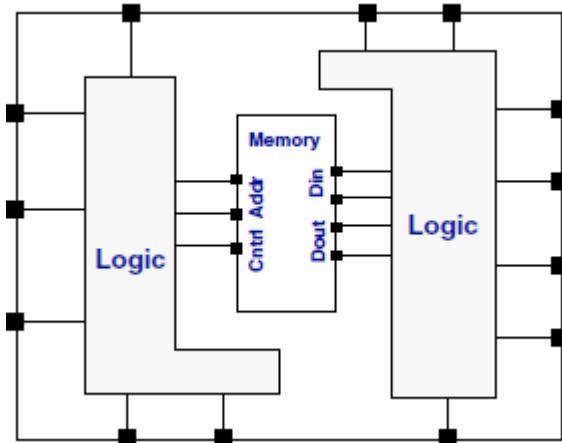
Chapter topics follow this sequence:

Understanding Memory BIST	59
BIST for Embedded Memories	60
Programmable Memory BIST with Tesson MemoryBIST	63
Diagnosis	64
Built-In Repair Analysis	68
Using Programmable Algorithms	70
Setting Up Memory BIST	72
Obtaining Controller-Level Go/No-Go Results	74
Obtaining Comparator-level Go/No-Go Result	74
Parallel Static Retention Testing	75
Execution Disabling	76
Performing Bit-Level Diagnosis with CompStat	77
Automatic Diagnosis	77
Interactive Debug	83
Performing Bit-Level Diagnosis with Stop-On-Error	91
Automatic Diagnosis	91
Interactive Debug	95
Faster Diagnosis	98
Performing Bit-Level Diagnosis with ROM Diagnostics	100
Interactive Debug	100

Understanding Memory BIST

A memory is considered embedded if *some or all of its terminals are not directly connected to the pins of the host chip*. For illustration purposes, a simplified representation of an embedded memory is illustrated in [Figure 4-1](#).

Figure 4-1. Representation of an Embedded Memory



Embedded memories are becoming increasingly common in today's large ASIC designs. It is not uncommon to have multiple embedded memories in a single ASIC. Not only are embedded SRAMs being used, but ROMs and DRAMs are being integrated into very deep sub-micron (VDSM) ASICs.

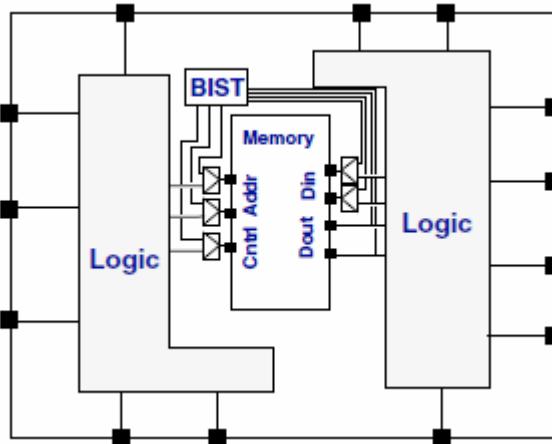
This increased use of embedded memories has resulted in an urgent need to develop ways of adequately testing these inherently difficult-to-access memories. A description and the advantages of the BIST approach to testing embedded memories is provided in "[BIST for Embedded Memories](#)." This section shows how BIST can be used to effectively test any number of embedded memories integrated into a single chip.

BIST for Embedded Memories

The key to solving the embedded memory input and output access problem described in the previous section is to generate the necessary test patterns and analyze the test responses local to the embedded memory. This is the memory BIST approach, as illustrated in [Figure 4-2](#).

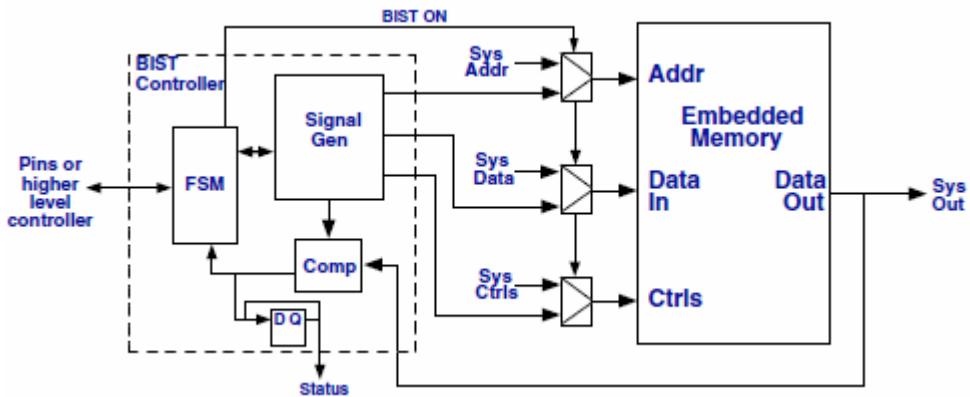
A local memory BIST controller is used to generate the test patterns and observe the test responses from the memory. Multiplexing logic chooses between address and data originating from the memory BIST controller or from the system logic.

Figure 4-2. BIST Approach for an Embedded Memory



A more detailed view of a typical embedded memory BIST architecture is provided in [Figure 4-3](#).

Figure 4-3. Typical BIST Architecture for Testing Embedded Memories



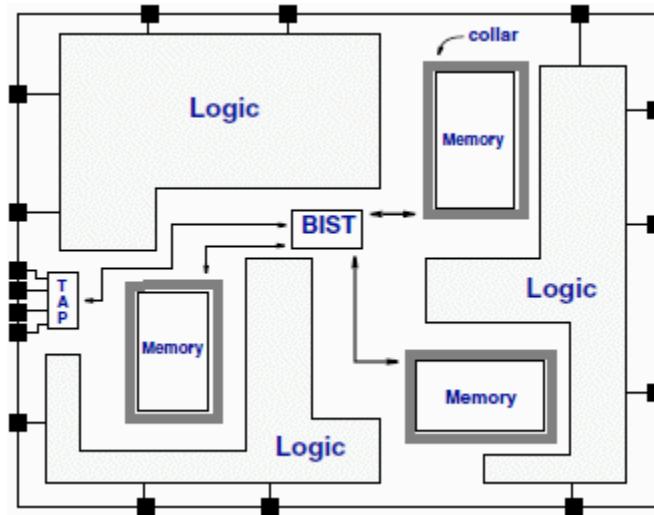
The memory BIST controller consists of three main blocks:

- A *signal generation block* contains the circuitry to produce the address, data, and control values necessary to create each test pattern that is to be applied to the memory. This block typically contains an up/down counter for generating the address sequences needed by most memory test algorithms.
- A *comparator* to compare the values read out of the memory with expected values generated by the signal generation block on a cycle-by-cycle basis. The result of each comparison is accumulated into a status flip-flop in order to provide a go/no-go result at the end of the test. Often the comparison result is brought out to a chip-pin for real-time monitoring.
- A *finite state machine* (FSM) is used to control the overall sequence of events. It determines, for example, if the address counter should be counting up or down or if the data being generated should be a marching 0 or marching 1 pattern.

The memory BIST controller typically requires very simple initialization and control to operate. The initialization may consist of, for example, which memory test algorithm to apply or to simply clear the status flip-flop. The initialization and control may come from a chip-level test controller or from a source external to the chip. In many cases, the controller is wired to an IEEE 1149.1 test access port (TAP). This provides an industry-standard interface for accessing the memory BIST controller.

Generally, a single memory BIST controller can be used to test more than one embedded memory on a chip. A typical scenario for a chip is illustrated in Figure 4-4.

Figure 4-4. Sharing a BIST Controller Among Several Embedded Memories



Shown in Figure 4-4 is a single controller used to test three separate embedded memories. Multiple memories can be tested either sequentially or in parallel. The advantage of testing the memories in parallel is a reduced test time. However, there are disadvantages to parallel testing that must be considered:

- The power consumption that results from testing several memories together could be large.
 - Certain memory BIST controller resources need to be duplicated. For example, a separate comparator is needed for every memory tested in parallel.

There is also a potential disadvantage to using a single controller for multiple embedded memories. If the memories are not localized to one area of the chip, then a large amount of wiring may be needed to route the address and data lines from the controller to each of the memories. This is especially true for the data lines given the large data widths (64- bits, 128-bits, and so on) many memories now have.

Programmable Memory BIST with Tessonnt MemoryBIST

Mentor Graphics has introduced Tessonnt MemoryBIST product with the release LV2005, Version 6.0. This memory BIST product offers the following benefits:

- Test multiple memories using one memory BIST controller that has one or more BIST steps, where BIST steps are run in sequence
- Test memories in parallel in one BIST step or in sequence in several BIST steps
- Define one or more custom test memory algorithms that will be hard-coded into the memory BIST controller
- Choose memory test algorithms from Mentor Graphics library of algorithms to be hard-coded into the memory BIST controller
- Run the memory BIST controller for all steps with the specific algorithms assigned at generation time (default configuration)
- Run the memory BIST controller in diagnostic mode where you can freeze on a specific BIST step, specific memory test port, or specific error count
- Select a hard-coded memory BIST algorithm to be applied to a specific memory BIST step at the tester
- Select an algorithm from a library of algorithms to be applied to a specific memory BIST step
- Define a custom algorithm at the tester time to be applied to a specific memory BIST step
- Perform repair analysis on memories implementing different redundancy schemes, such as *row only*, *column only*, or *row and column*.

Tessonnt MemoryBIST is a highly advanced product that addresses several limitations of the existing memory BIST solutions:

- Tessonnt MemoryBIST *combines the power of memory BIST with the tester programmability*. When you use Tessonnt MemoryBIST you are including an embedded tester on the chip which enables you to test and diagnose the embedded memories with algorithms that were not considered while designing the chip—the *post-silicon programmability*.
- Tessonnt MemoryBIST also provides the ability to *use different types of repairable memories in one controller*. You can use the repair analysis to implement a self-repair solution for repairable memories to significantly improve the chip yield without sacrificing a lot of silicon area overhead.

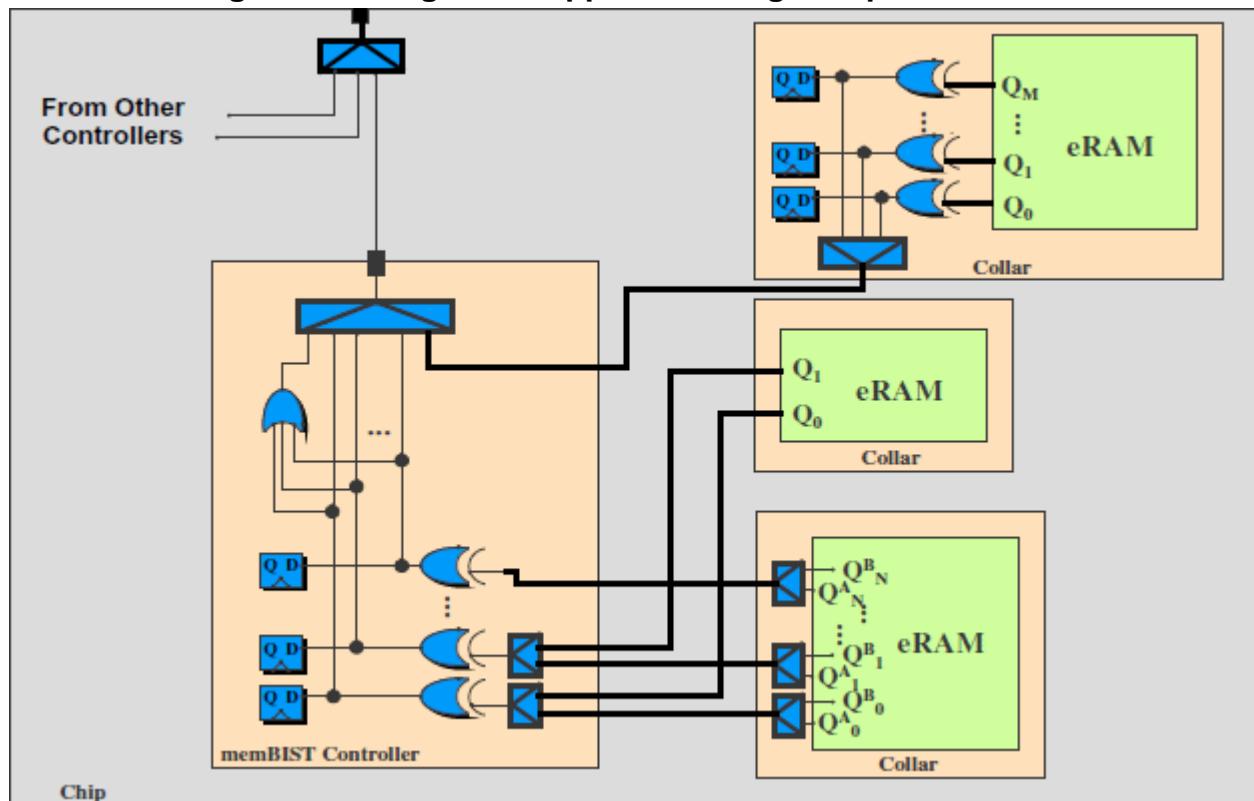
Tessent MemoryBIST also provides significant flexibility and automation in designing optimal memory BIST configuration to meet your chip power and test time budget.

For detailed information on the memory BIST algorithms provided by Mentor Graphics, refer to Appendix A, “Memory BIST Algorithms.”

Diagnosis

One of the most basic diagnostic capabilities supported by the memory BIST methodology is illustrated in Figure 4-5. In this scenario, one or more *compare status* signals from the memory BIST controller are routed directly to chip pins. These compare status signals provide cycle-by-cycle compare results. A compare status output can be made to correspond to anything from the full memory word to a single bit of the word. Each of these outputs are routed directly to pins for monitoring by the tester. Additionally, failure data from multiple memory BIST controllers can be monitored at a single pin by employing the comparator sharing scheme. Figure 4-5 shows an example of such a scheme.

Figure 4-5. Diagnostic Approach using CompStat Method

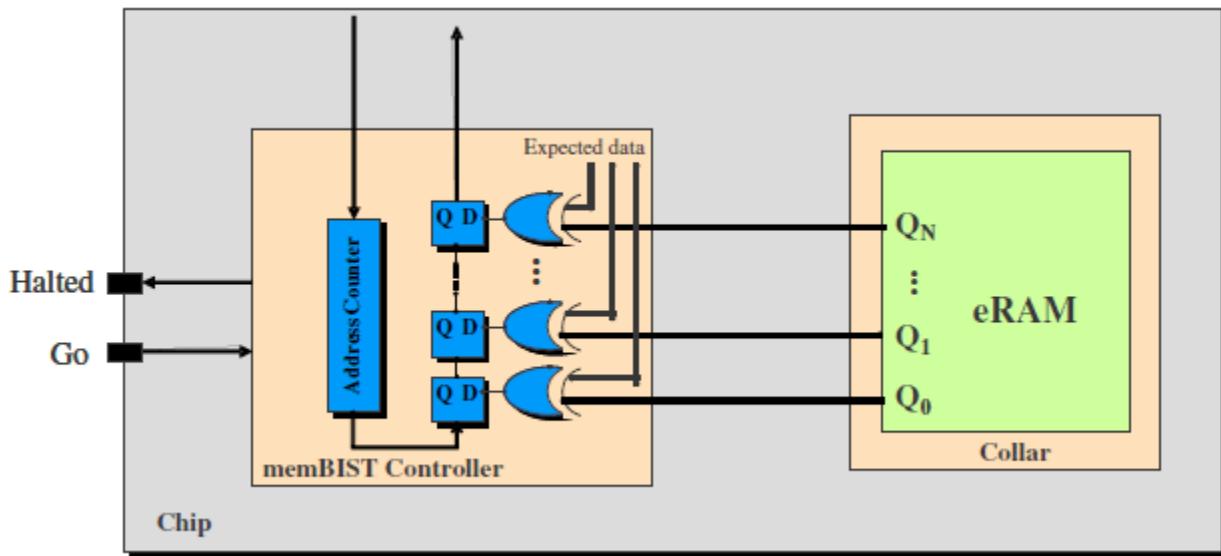


In order to extract enough failure data to resolve down to individual bit failures (typically referred to as full failure bit mapping), as many compare status pins as bits in the memory word are needed. This, of course, can result in an unacceptably large number of pins. Furthermore, the tester needs to operate at the same clock rate as the memory BIST controller, because the compare status pins provide new data at every clock cycle. Fortunately, most problems can be

diagnosed at speeds that are appropriate for low-performance testers. However, some problems might require to run the test at speed.

To eliminate the above constraints, a purely scan-based diagnostic methodology is also supported, as depicted in [Figure 4-6](#).

Figure 4-6. Diagnostic Approach Using Stop-On-Nth-Error Serial Scan



This approach is referred to as *Stop-On-Nth-Error* for the following reason: the memory BIST controller is equipped with an error count register that is scan initialized before each run. When the controller has encountered a number of errors equal to that specified in the error register, it stops so that all pertinent error information (algorithm step, address, failing bit position, and so forth) can be scanned out of the controller. By iteratively scanning in subsequent error counts and running the controller, all bit-fail data can eventually be extracted.

Diagnosis Pattern Reuse Mode

Typically, the auto diagnose algorithm for memory BIST generates a patchable pattern. Then, the algorithm patches and executes that pattern for every iteration of diagnosis for every instance of the DUT tested. The *Diagnosis Pattern Reuse Mode* feature prevents regeneration of the initial patch-enable pattern for every DUT diagnosed; that is, once the initial patch-enable pattern is generated and loaded, the pattern is reused for every DUT. This mode is available on ATE platforms that support pattern patching.

Using the *Diagnosis Pattern Reuse Mode* feature, you can choose to cache all memory BIST controllers or to cache the diagnostic vectors only for controllers with **Diag-On** enabled. You can also indicate that no caching of diagnostic patterns is to be performed.

In addition, this mode allows you to pre-generate and pre-load all cached diagnostic patterns when the patterns are initially generated and loaded. This prevents vector memory from running out in the middle of characterizing a batch of wafers and devices.

Bit-Map Information Generation

Memory failure data can be generated by Tesson SiliconInsight in a format suitable for bit-map generation. This failure data identifies the failing phase and operation of the test algorithm. The following algorithms are supported when dealing with non-programmable controllers:

- SMarch
- SMarchCHKB
- SMarchCHKBci
- SMarchCHKBcil
- SMarchCHKBvcd

When dealing with programmable controllers, any algorithm can be diagnosed.

Additionally, the failing memory, memory port, failing bit, and physical and logical address information are also identified. The bit-map information is generated using the CompStat and Stop-On-Error features and provides bit- and word-levels of failure information.

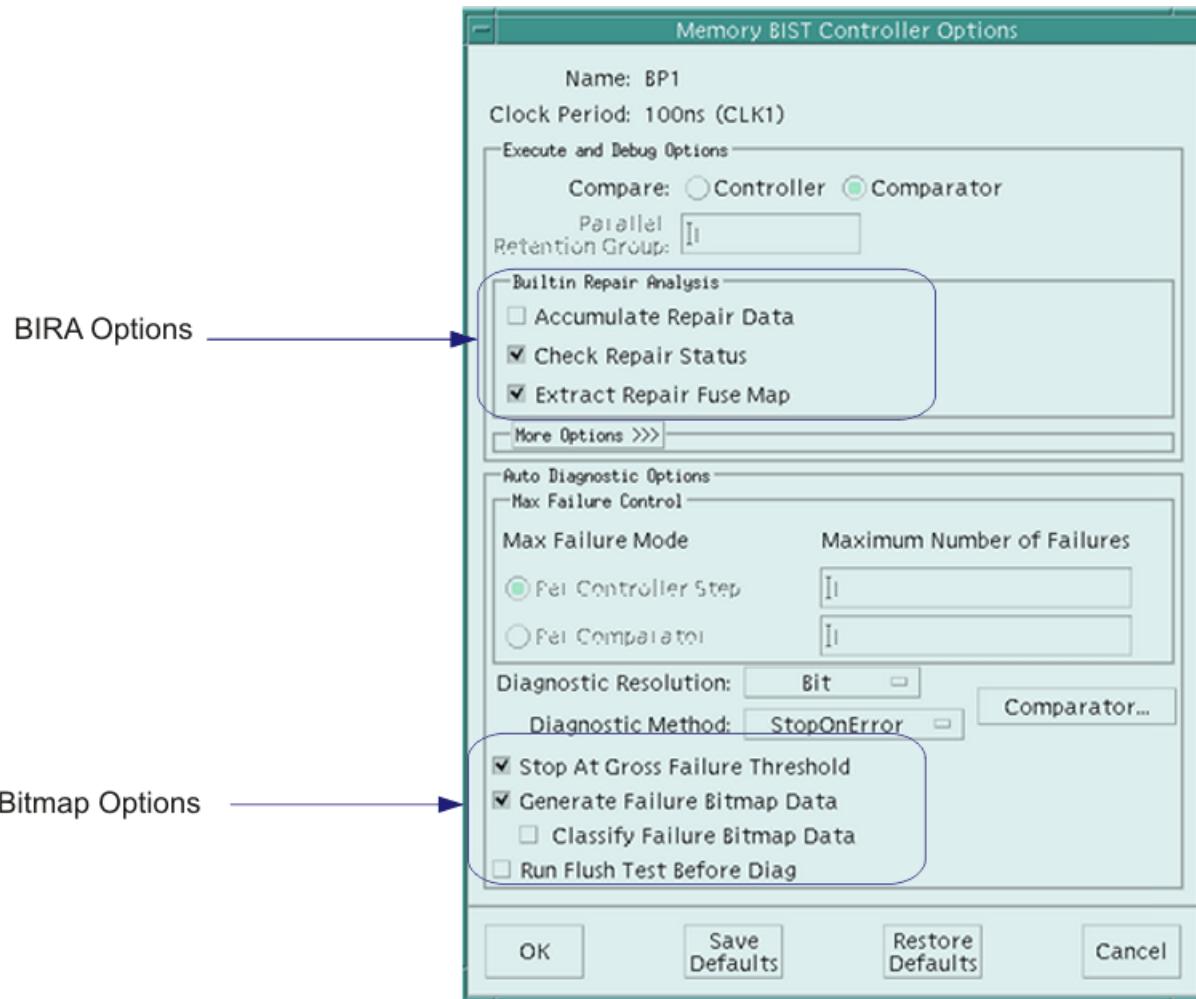
The threshold for gross failures is used to limit data collection for memories that have gross failures. The threshold for gross failures is automatically established for each memory.

You can decide to control the failure bit-map data collection by manually limiting the data collection instead of using the gross failure threshold. The format of the memory failure data for bit-map generation is identical for Stop-On-Error and CompStat diagnostics. The options you use for bit-map data collection are described below.

Generate Failure Bitmap Data

You can use the **Generate Failure Bitmap Data** option to either enable or disable the generation of memory failure data. [Figure 4-7](#) shows how to set this option from a memory BIST controller options dialog box.

Figure 4-7. Specifying the Failure Bitmap Data and BIRA Related Options



When the **Generate Failure Bitmap Data** option is checked, the memory failure data for bit-map is automatically generated based on the *Diagnostic Resolution and Method*:

- When **Diagnostic Resolution** is set to *Word*, memory failure data is generated for bit-map at word level.
- When **Diagnostic Resolution** is set to *Bit*, and **Diagnostic Method** is set to either *StopOnError* or *CompStat*, memory failure data is generated for bit-map at bit level.
- For other selections of *Diagnostic Resolution and Method*, no failure data is generated for bit-map.

Stop At Gross Failure Threshold

You can use the **Stop At Gross Failure Threshold** option to enable or disable automatic interruption of memory failure data collection. When the **Stop At Gross Failure Threshold** option is checked (refer to [Figure 4-7](#)), a threshold to interrupt failure data collection is computed for each memory in the current controller step. This threshold may differ from one

memory to the next, depending on the size of the memory. If the threshold is reached for at least one of the memories within the controller step, failure collection for the current controller step is interrupted.

In addition, the **Max Fails Per Controller Step** option is grayed out when the **Stop At Gross Failure Threshold** option is checked.

When the **The Stop At Gross Failure Threshold** option is not checked, the failure collection data is limited by the value specified for the **Max Fails Per Controller Step** or **Max Fails Per Comparator** option, located in the **Memory BIST Controller Auto Diagnostic Options**.

Classify Failure Bitmap Data

You can use the **Classify Failure Bitmap Data** option to enable or disable the data classification for bit-map. When the **Classify Failure Bitmap Data** option (refer to [Figure 4-7](#)) is checked, failure data classification for bit-map is generated in a tabular format.

When the **Generate Failure Bitmap Data** option is not checked, the **Classify Failure Bitmap** option is grayed out.

Built-In Repair Analysis

Memory BIST supports Built-In Repair Analysis for customers that want to perform memory test and repair analysis in production environment with minimal time impact. Row, Bank, Column and IO redundancy are supported. The redundancy information needs to be extracted by the Tesson SiliconInsight to allow repair.

Using the Tesson SiliconInsight, you can perform the following operations:

- Enable/disable extraction of repair analysis information,
- Save the redundancy analysis information extracted from the last BIST execution to a file

The options you use for repair analysis are described below. These options are grayed out when the memory BIST controller does not support Built-In Repair Analysis feature. Use [Figure 4-7](#) as a reference for the following description.

Accumulate Repair Data

This option is not supported anymore in Tesson SiliconInsight and is now permanently grayed out and disabled.

Check Repair Status

To extract the repair analysis status after applying the test sequence, you use the **Check Repair Status** option—located in the **Execute and Debug** area in the **Memory BIST Controller Options** panel:

- When the **Check Repair Status** option is checked, the repair status is extracted from the memory BIST controller after applying the test sequence. The repair status will then be analyzed by SI, and the **BIRA Datalog** will be displayed if the repair status indicates the memory is repairable or not. Memories will be highlighted in the following colors in the **Test Configuration** area:
 - Repairable memories—*orange*
 - Non-repairable memories—*red*
 - Non-faulty memories—*green*
- When the **Check Repair Status** option is not checked, the repair status is not extracted from the controller after applying the test sequence.

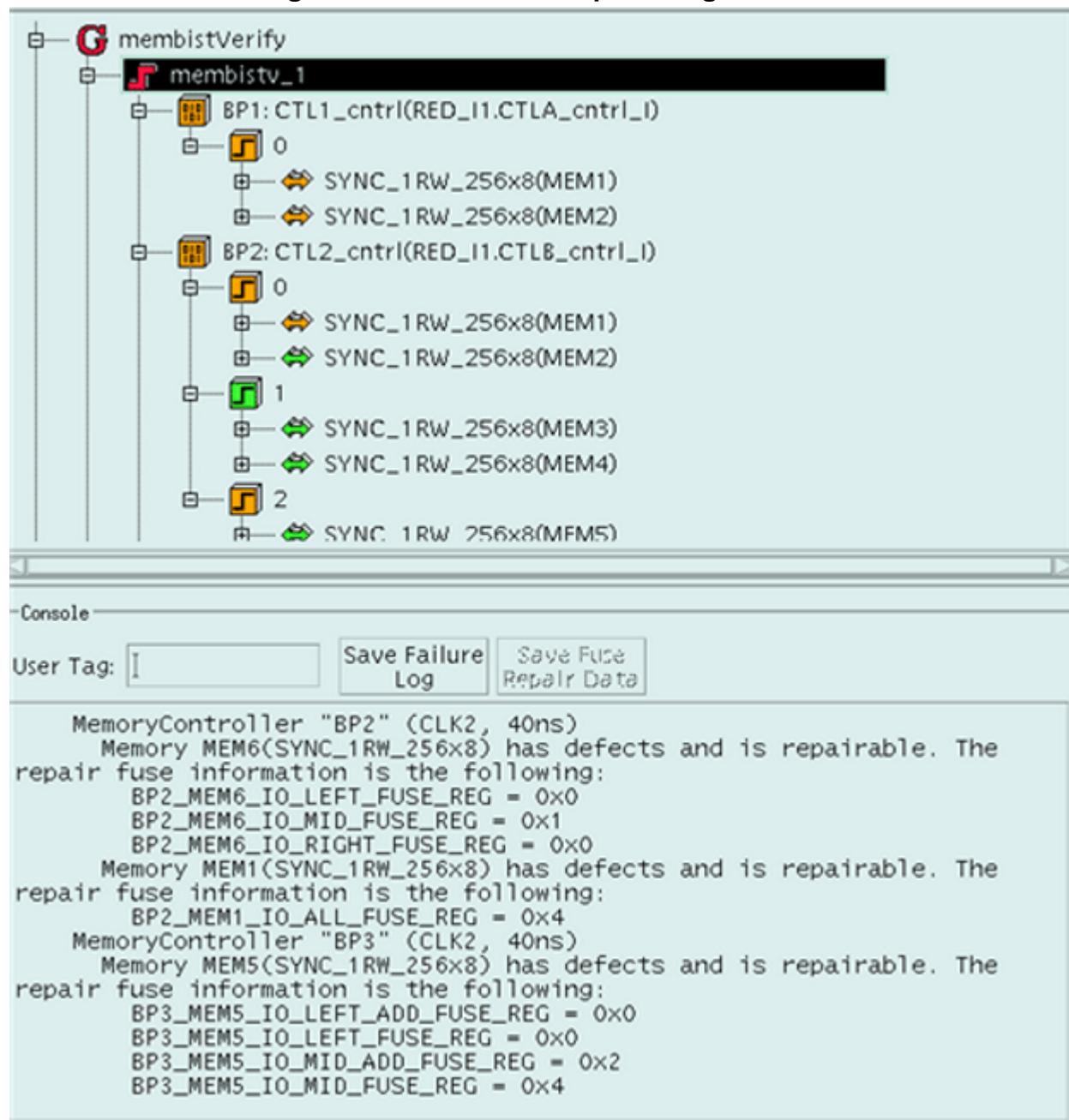
Extract Repair Fuse Map

The **Extract Repair Fuse Map** option is permanently grayed out and forced to the value of the **Check Repair Status** option. It is located in the **Execute and Debug** area of the **Memory BIST Controller Options** panel and is automatically checked when the **Check Repair Status** option is checked. It allows extraction of the repair fuse map after applying the test sequence:

- When the **Extract Repair Fuse Map** option is checked, the fuse map is extracted from the memory BIST controller after applying the test sequence. The **BIRA Fuse Map Datalog** will be displayed if the repair status indicates the memory is repairable. If the memory is not repairable, or no repair is needed, no **BIRA Fuse Map Datalog** will be provided.
- When the **Extract Repair Fuse Map** option is not checked, the repair fuse map is not extracted from the memory BIST controller after applying the test sequence.

Figure 4-8 shows the typical BIRA fuse map datalog results when you have specified the **Check Repair Status** and **Extract Repair Fuse Map** options on a controller with a repairable memory.

Figure 4-8. BIRA Fuse Map Datalog Results



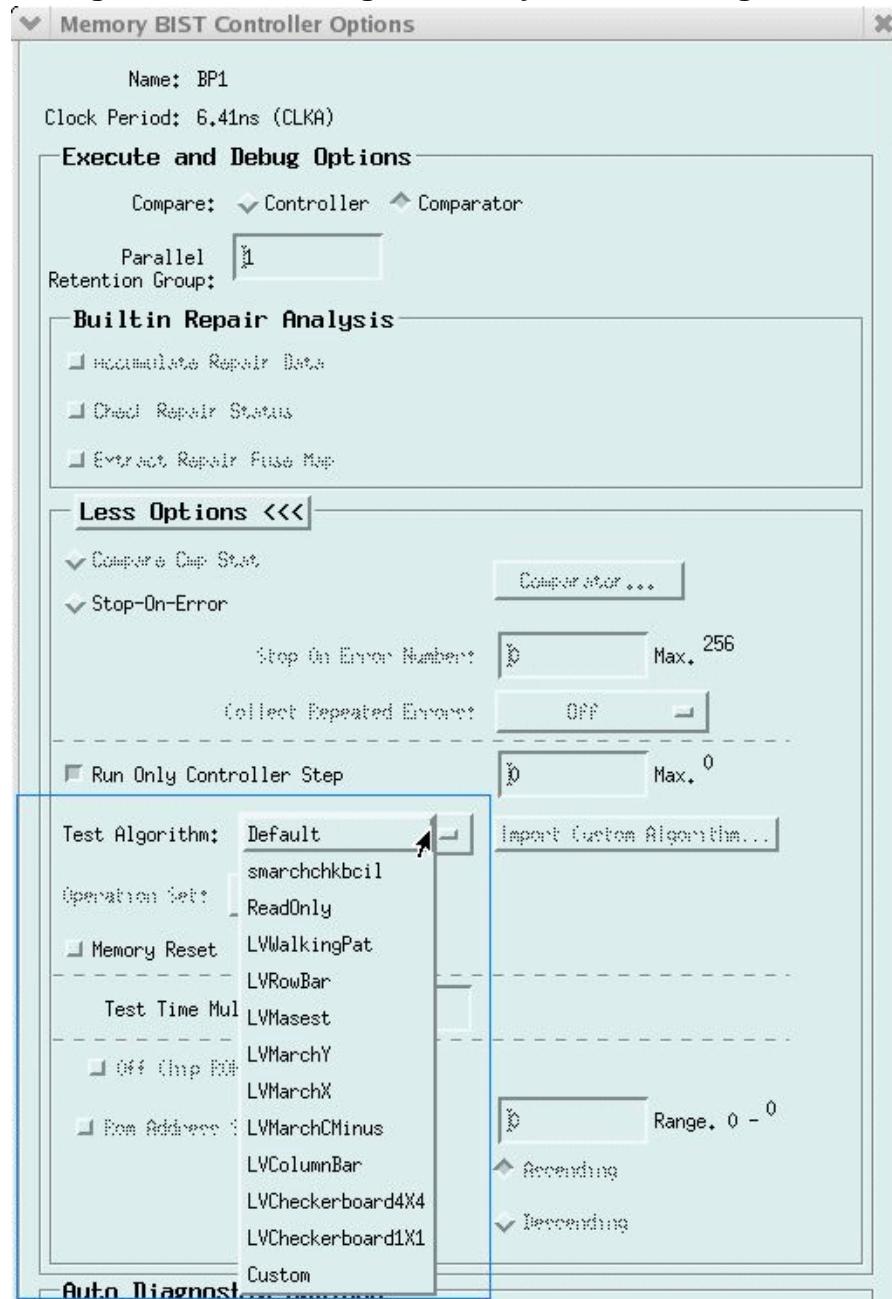
Using Programmable Algorithms

If the DUT incorporate memory BIST implementation using the programmable controllers generated using Tessent MemoryBIST, you will be able to choose the memory BIST algorithm from a list of available *hard-coded algorithm* choices. As the name implies, these choices are hard-coded during the controller generation and can not be changed. However, if the controller is generated to accept a choice of *soft-coded algorithms* (also known as *post-silicon programmable algorithms*), then you would be able to import a memory BIST algorithm and

use it. These choices are available under the **Memory BIST Controller Options** dialog box as shown in [Figure 4-9](#).

Note
Programmable algorithms can only be selected when you freeze a controller step under a memory BIST controller.

Figure 4-9. Choosing a memory BIST Test Algorithm



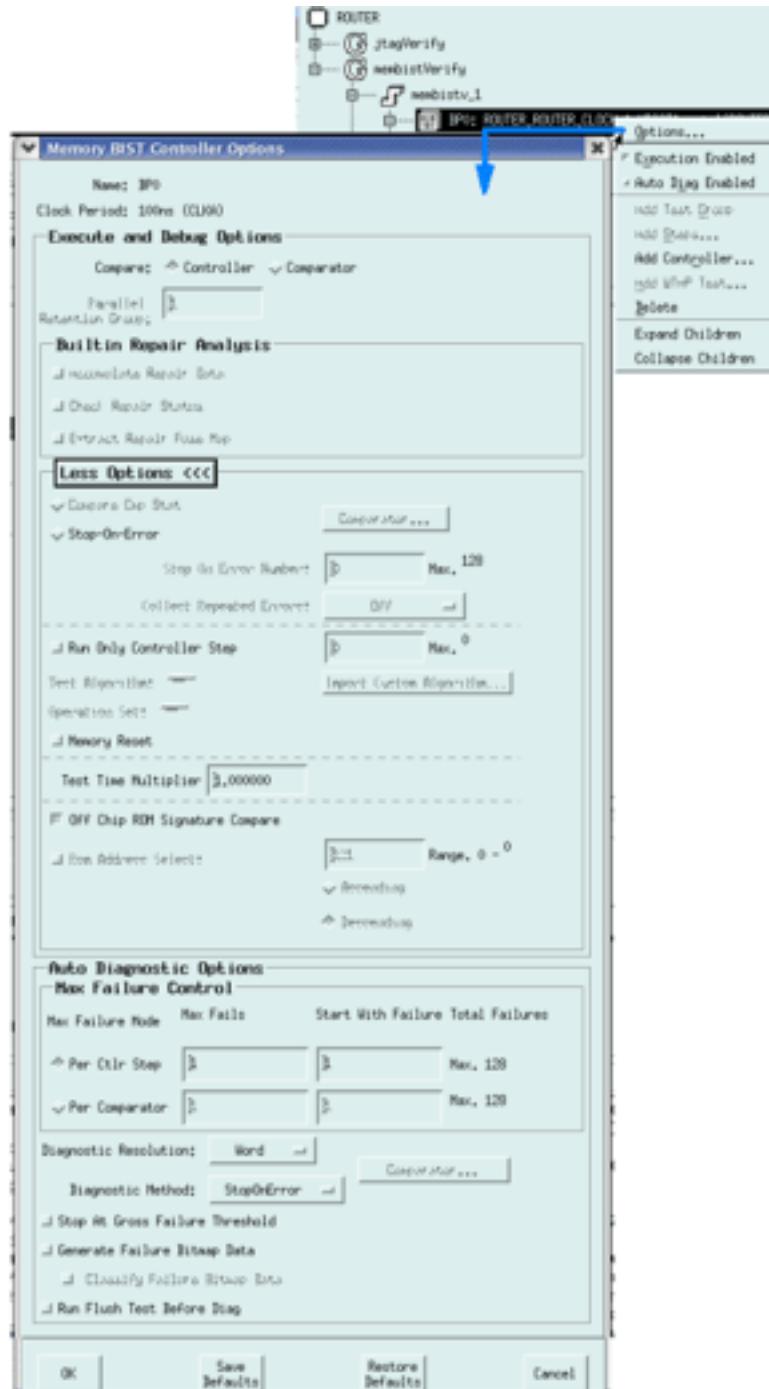
Setting Up Memory BIST

When you bring up the *default.config_eta* configuration file provided within the Mentor Graphics database (LVDB), all memory BIST controllers within your chip are properly configured for execution. The various settings for each controller was set by the design team. You can, however, change these by editing the test configuration from within the Tessonent SiliconInsight GUI.

To edit the memory BIST options, perform the following:

1. Launch the Tessonent SiliconInsight in offline mode as shown in “[Invoking Tessonent SiliconInsight in Offline Mode](#).”
2. Right mouse button click on a memory BIST *controller test step* icon in the **Test Configuration** area and choose the **Options** to bring up the **Memory BIST Controller Options** menu as illustrated in [Figure 4-10](#).

Figure 4-10. Memory BIST Controller Options Menu



3. Click on the **More Options** button to fully expand the menu. You can set the *Compare Cmp Stat* radio button for CompStat based diagnosis or set the Stop-On-Nth-Error options.

As illustrated in [Figure 4-10](#), the **Memory BIST Controller Options** menu has two main sections: **Execute and Debug Options** and **Auto Diagnostic Options**.

Note



The **Collect Repeated Errors** option has been disabled in membist controllers. It is still supported in Tessent SiliconInsight for legacy controllers (old designs). If it remains grayed out after you select **Stop-On-Error**, it means the controller does not support it and you should not try to manipulate it.

Obtaining Controller-Level Go/No-Go Results

For go/no-go testing, you can use the **Compare** option to set the amount of desired data logging resolution. Setting this option to *Controller* indicates that you are only interested in knowing whether or not all tests of the memory BIST controller passed.

With **Compare** set to *Controller*, click on the **OK** button to accept the setting and close the menu panel. Highlight a memory BIST controller before you click on the **Execute** button (lightning bolt icon) in the tool bar to have the controller execute its tests. A result in the **Console** area appears as illustrated in [Figure 4-11](#). Notice that only a global fail result is displayed.

Note



When **Compare** is set to *Controller* or *Comparator*, it is ignored if either **CompareCompStat** or **Stop-On-Error** is enabled. Therefore, the GUI results of the execution with either **CompareCompStat** or **Stop-On-Error** enabled do not include the results and datalog of the **Compare** option.

Figure 4-11. Sample Result of Execution with Compare Set to Controller

```
=====
LVDB Directory:      demo_chip_eate.lvdb
LVDB Name:          demo_chip_eate.lvdb
Test Config:        LVBIST1A_TC1
TestStep: mem (FAILED)
Execution Time Stamp: 01/08/07 09:55:08
    MemoryController "BP1" (tck, 14.3ns)
    Port "GoStatus" failed (IR_STATUS9=0).
=====
```

Obtaining Comparator-level Go/No-Go Result

On the **Memory BIST Controller Options** menu, you can set the **Compare** option to *Comparator*. You can further enable the **Run Only Controller Step** option to focus only on the memories you are interested in. After clicking on the **Execute** button, a result similar to the one illustrated in the **Console** area in [Figure 4-12](#) appears. Note that the failing memories as well as the failing data-bit slices within the memories are identified.

The width of a data-bit slice can range from a single bit to the entire width of the memory. It is based on how comparators in the memory BIST controller were configured at design time and

cannot be altered. In this example, a single comparator was used for each set of four data bits. Note that obtaining the failing data-bit slice information does not require any more tester time than obtaining the simple global go/no-go result.

Figure 4-12. Sample Result of Execution with Compare Set to Comparator

```

LVDB Directory: demo_chip_eate.lvdb
LVDB Name: demo_chip_eate.lvdb
Test Config: LVBIST1A_TC1

TestGroup: group_memory
TestStep: mem (FAILED)
Execution Time Stamp: 01/08/07 09:57:48
MemoryController "BP1" (tck 14.3ns)
    Collar "MEM2(SYNC_1RW_1kX8)" register "BP1_GO_ID_REG4" failed (-1). Failed data bits = d[bitRange]>d[7:4].
    Collar "MEM2(SYNC_1RW_1kX8)" register "BP1_GO_ID_REG3" failed (-1). Failed data bits = d[bitRange]>d[3:0].
    Collar "MEM1(SYNC_1RW_1kX8)" register "BP1_GO_ID_REG2" failed (-1). Failed data bits = d[bitRange]>d[7:4].
    Collar "MEM1(SYNC_1RW_1kX8)" register "BP1_GO_ID_REG1" failed (-1). Failed data bits = d[bitRange]>d[3:0].

```

Failing memories are identified ...and failing bit slices.

Parallel Static Retention Testing

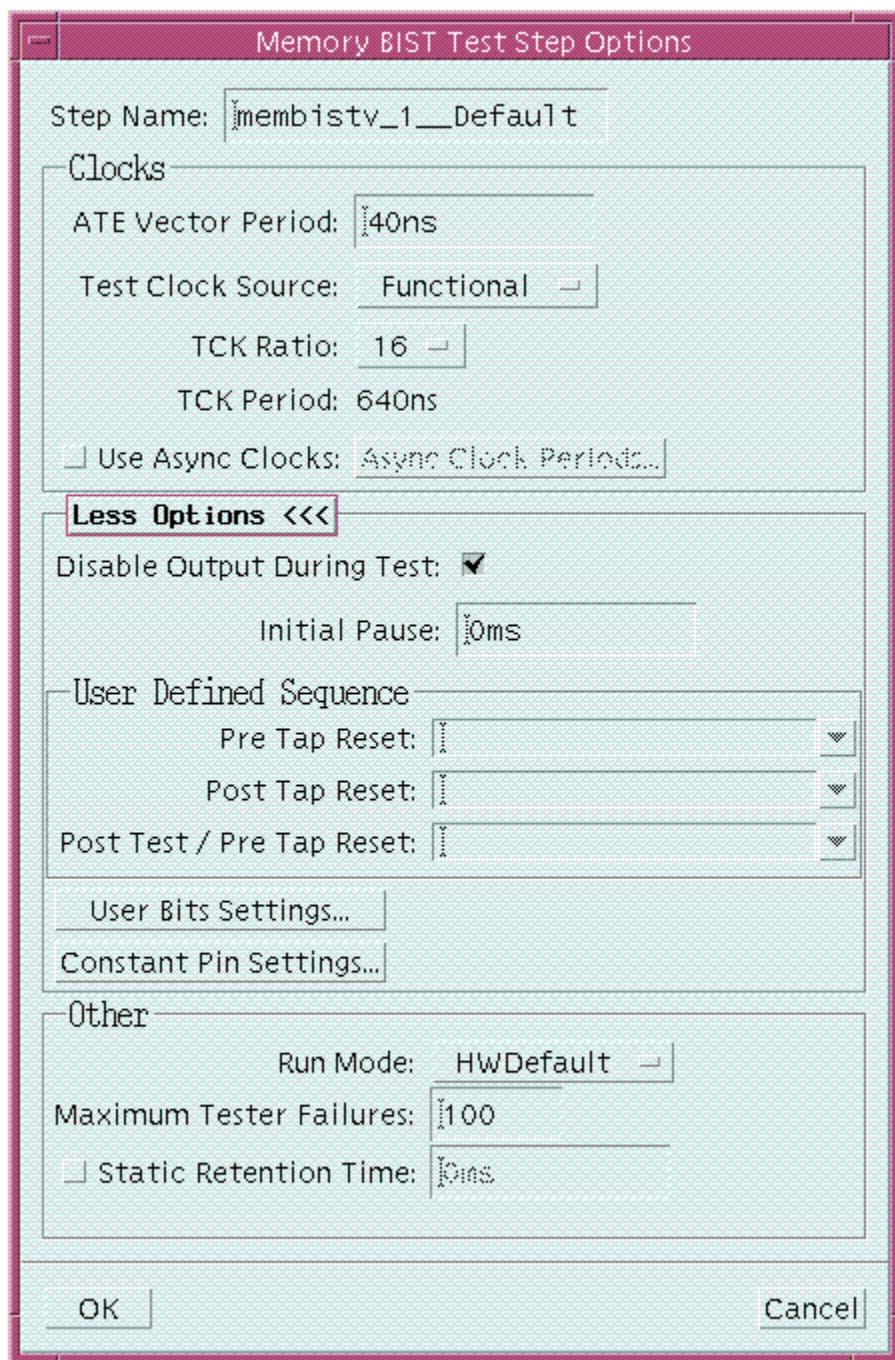
A general concern regarding static retention tests is that they consume a large amount of tester time. Typically, the more memories you have to test, the more tester time is needed for retention testing. This is because a static retention test is applied sequentially to each memory. With chips now containing as many as hundreds of memories, the time requirements for these tests can become unacceptable.

Fortunately, Mentor Graphics provides a way around this problem. A memory BIST controller can apply static retention tests to all the memories it tests at the same time. This is done regardless of whether the memories are tested sequentially or in parallel. This approach is called *Parallel Static Retention Testing* and is invoked at the test step level.

To invoke parallel static retention testing on your chip, perform the following steps:

1. Right mouse button click on the memory test step icon and choose the **Options** to access the **Memory BIST Test Step Options** menu.
2. Click on the **Static Retention Time** option box in the **Other** section of the **Memory BIST Test Step Options** menu, as illustrated in [Figure 4-13](#).
3. Set the **Run Mode** option to *HWDefault* and enter a positive number in the **Static RetentionTime** field, such as *10ms*. Now, when you execute the test step, a Parallel Static Retention Test is performed in addition to each of the memory BIST controller's tests in that step.

Figure 4-13. Memory BIST Test Step Options Menu

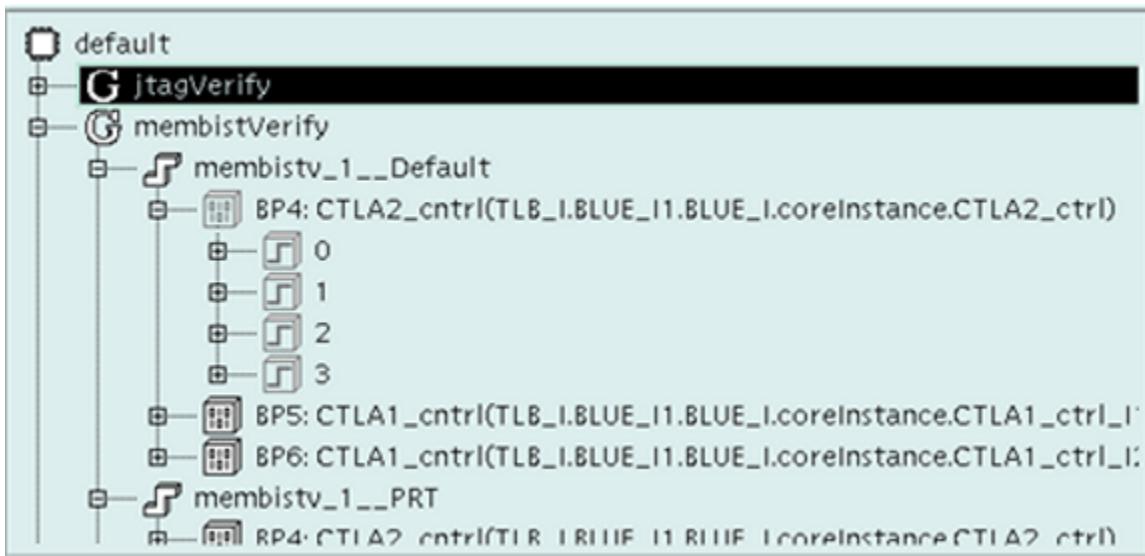


Execution Disabling

In some circumstances, if a test step contains several controllers, you can disable the execution of one or more of these controllers. This might be the case, for example, when you are trying to debug a particular memory.

Any node within the test configuration (down to embedded test controllers) can be easily disabled by right mouse button clicking on its icon and turning off the **Execute Enable** option. That icon and all icons in its sub-tree is greyed out, which indicates all are disabled. [Figure 4-14](#) illustrates the result of disabling the *BP4* memory BIST controller.

Figure 4-14. Disabling Execution



When a node is re-enabled, the enable execution status of the node's children reverts back to what they were prior to the parent node being disabled.

Continuing with the example, if you now disable the *membistVerify* test step icon, all nodes in this test step become disabled. If the *membistVerify* test step is then re-enabled, all nodes in the test step are not automatically enabled. Instead, they rather revert back to what they were before, as shown in [Figure 4-14](#).

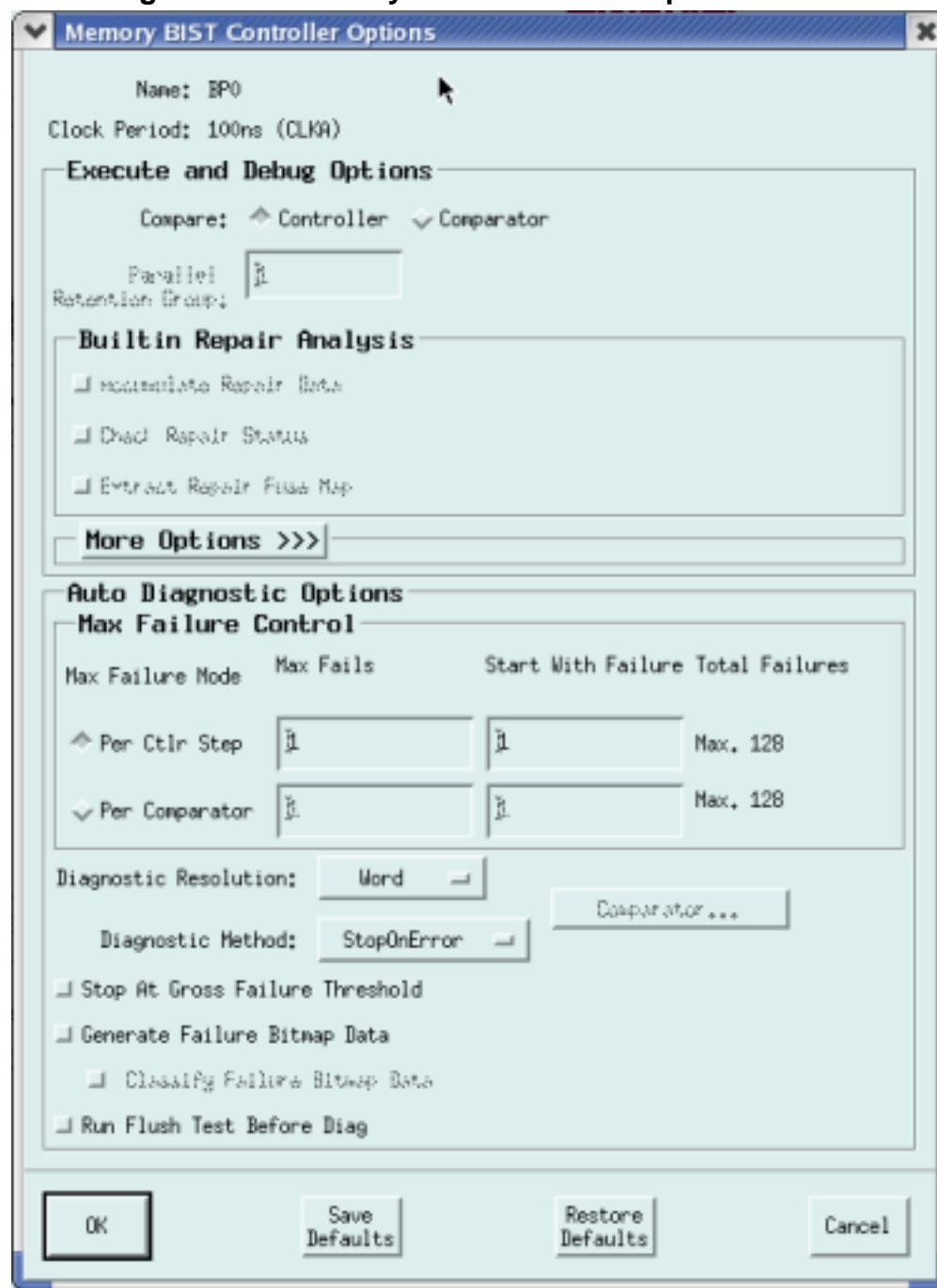
Performing Bit-Level Diagnosis with CompStat

One of the most powerful features of Mentor Graphics' embedded test blocks is their support of real time diagnosis. This section describes how to use the Compare Status-based memory BIST diagnostic approach.

Automatic Diagnosis

Performing automatic memory diagnosis using the Tessent SiliconInsight GUI is simple. Right mouse button click on the memory BIST controller icon *BPI* and select **Options** to bring up the **Memory BIST Controller Options** menu as illustrated in [Figure 4-15](#).

Figure 4-15. Memory BIST Controller Options Menu



The **Max Failure Control** section within the **Auto Diagnostic Options** section allows you to specify the **Maximum Number of Failures** you want diagnosed **Per Controller Step** or **Per Comparator**. You can select the desired **Max Failure Mode** and set the corresponding **Maximum Number of Failures** to any desired value. For the example, leave the **Max Failure Mode** set to **Per Controller Step** and set the corresponding **Maximum Number of Failures** value to 2.

To perform Compare Status-based diagnosis, leave the **Diagnostic Method** cascade button set to *CompStat*. The **Diagnostic Resolution** cascade button allows you to decide if you want to simply know which comparators are detecting errors or precisely which bits in the memory are failing. Make sure this is set to *Bit* to obtain full bit-level diagnosis. Click **OK** to accept your settings and close the **Memory BIST Controller Options** menu and then click on the **Diagnose** icon in the tool bar (the stethoscope icon) to activate automatic diagnosis. You obtain results similar to the ones shown in [Figure 4-16](#).

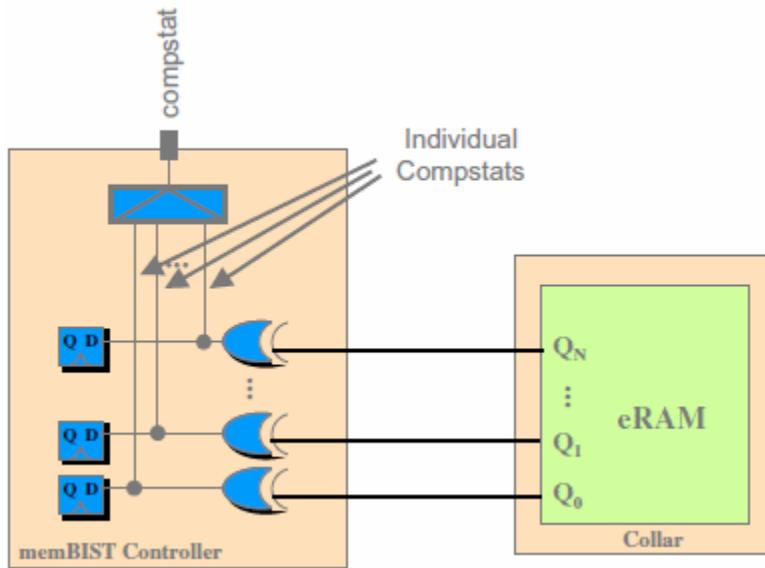
Figure 4-16. Sample Results of Automatic CompStat Based Diagnosis

```
=====
=====
LVDB Directory:      demo_chip_eate.lvdb
LVDB Name:          demo_chip_eate.lvdb
Test Config:        LVBIST1A_TC1
  TestStep: mem (FAILED)
  Execution Time Stamp: 01/08/07 10:09:57
    MemoryController "BP1" (tck, 14.3ns)
    Failure#1: Expected 1 (Q[0] = 1) (Cycle 14), TestPort 0,
Algorithm SMarch Phase2, Bit Slice Counter 0, row 0, column 0
(A[9:0] = 0x000)
    Memory  MEM1(SYNC_1RW_1kX8), Comparator 1
    Failure#2: Expected 1 (Q[0] = 1) (Cycle 15), TestPort 0,
Algorithm SMarch Phase2, Bit Slice Counter 0, row 0, column 0
(A[9:0] = 0x000)
    Memory  MEM1(SYNC_1RW_1kX8), Comparator 1
=====
```

CompStat Failure Datalog

As shown in [Figure 4-17](#), several comparators are typically used to compare the outputs of a memory.

Figure 4-17. Memory BIST Comparator Architecture



For large memories, a comparator is often used for each memory output as full bit-level diagnostic resolution is typically desired. Smaller memories might have several outputs sharing a comparator. The number of comparators is determined at design time and cannot be altered. Automatic diagnosis is performed by examining the results of each failing comparator one at a time. For each of these comparators, the Tesson SiliconInsight GUI outputs the following line to identify the comparator:

```
Collar <memory_instance_name> register <comparator_register_name> failed
(=1). Failed data bits = d[bitRange]>d[n:m].
```

where the above syntax represents the following:

- *memory_instance_name*—identifies the collar (and hence the memory) associated with the failing comparator.
- *comparator_register_name*—identifies the controller register associated with the failing comparator. This register is used to accumulate the comparator outputs and uniquely identifies the comparator.
- *d[n:m]*—is the memory bit range associated with the failing comparator.

Following the above comparator identification, the Tesson SiliconInsight GUI outputs the following lines for each failure detected by the failing comparator:

```
Failure#n: Expected <exp1> (<logical_pin_name> = <exp2>) (Cycle <cy>),
TestPort <tp>, Algorithm <algo> <Phasek / Instruction i>, Bit Slice
Counter <bsc>, bank <bank>, row <row>, column <col>
(<logical_address[msb:lsb]> = <address>), counterA <ac>, delay counter
<dc>
```

where the above syntax represents the following:

- *<exp1>*—physical data value that is expected on the failing comparator (the opposite value is actually read).
- *<logical_pin_name>*—logical pin name on which the failure is detected.
- *<exp2>*—logical data value that is expected on the memory port.
- *<cy>*—clock cycle on which the failure is detected.
- *<tp>*—test port in which the failure was detected. This is only meaningful for multi-port memories. A test port represents a pairing of a memory input port and a memory output port for test application purposes.
- *<algo>*—test algorithm applied to the memory.
- *<Phasek / Instruction i>*—the algorithms applied by the memory BIST controller consist of several phases. Within each phase, a specific pattern is applied to the memory using a specific address sequence. If the phase identification is known, it will be displayed (Phasek), otherwise, the instruction identification (Instruction i) will be displayed. Descriptions of the available algorithms and their phases are provided in Appendix A, “Memory BIST Algorithms.”
- *<bsc>*—if a comparator is shared among several memory bits, this represents the specific bit within the bit slice that the failure is detected on.
- *<bank>*—physical bank address in which the fault is detected is displayed if the memory has a bank segment.
- *<row>*—physical row address in which the fault is detected.
- *<col>*—physical column address in which the fault is detected.
- *<logical_address[msb:lsb]>*—logical address name and bit range on which the failure is detected.
- *<address>*—logical address at the memory port on which the failure is detected.
- *<ac>*-counter A value when the fault is detected is displayed if the algorithm uses counter A.
- *<dc>*-delay counter value when the fault is detected is displayed if the algorithm uses delay counter.
- *<memory_instance_name>*—memory collar instance where the fault was detected.
- *<comp>*—number of the individual comparator that detected the fault.

If the **Generate Failure Bitmap Data** feature (see [Figure 4-7](#)) is enabled, then the Tessent SiliconInsight GUI also outputs the following lines:

```
MemoryInfo (<memory_collar_name>(<memory_library_name>)): Algo=<algo>,
#P=<no_ports>, #R=<no_rows>, #C=<no_columns>, #B=<no_bits>,
BG=<bit_grouping>, GF=<T | F>
```

```
BitMapInfo (<memory_collar_name>(<memory_library_name>)) : TP=<test_port>,  
Phase=<phase_id | instr_id>, PB=<phys_bank>, PR=<phys_row>,  
PC=<phys_col>, LB=<log_bank>, LR=<log_row>, LC=<log_col>, B=<bit_no>,  
PExp=<phys_exp>, LExp=<log_exp>
```

where the above represents the following criteria:

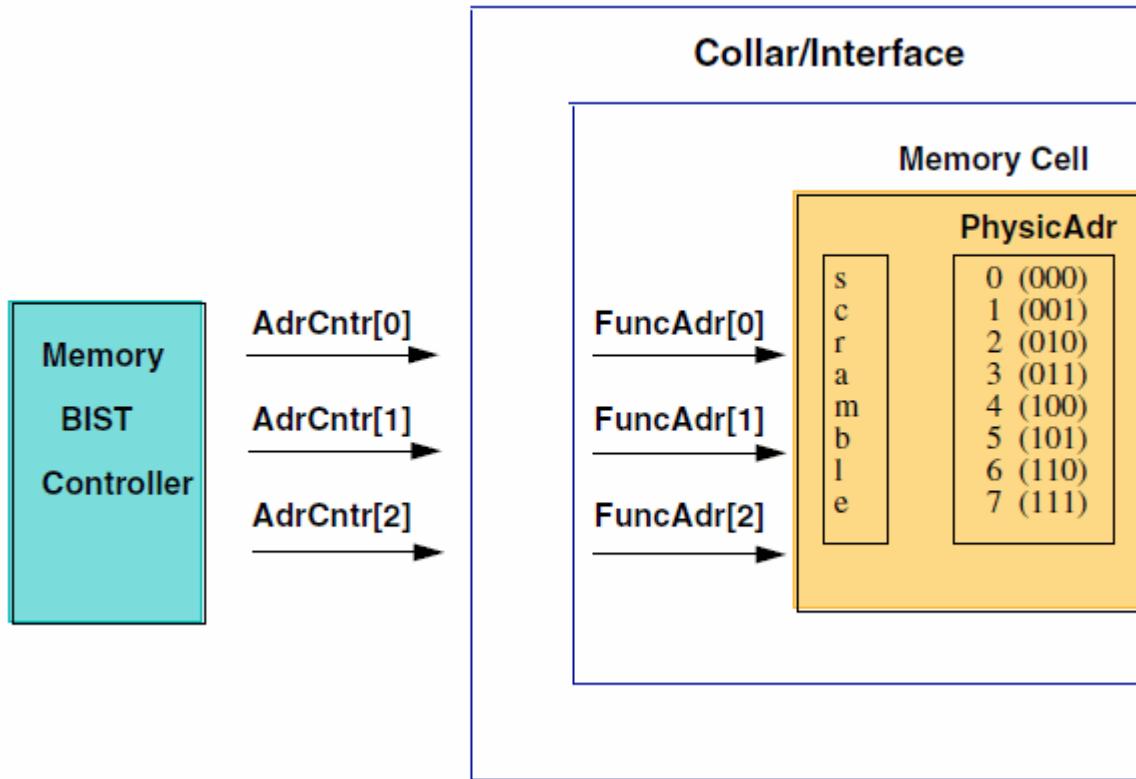
- *<memory_collar_name>* — memory collar identification on which some failures occurred
- *<memory_library_name>* — library model used for this failing memory collar
- *<algo>* — test algorithm identification
- *<no_ports>* — number of ports accessing this memory
- *<no_rows>* — number of rows in this memory
- *<no_columns>* — number of columns in this memory
- *<no_bits>* — number of bits in this memory
- *<bit_grouping>* — bit grouping for this memory
- *<T / F>* — indicates if the failing memory has gross failure (T) or not (F)
- *<test_port>* — the test port on which the failure occurred
- *<phase_id / instr_id>* — phase and operation on which the failure occurred (when known) or failing instruction (when phase is unknown)
- *<phys_bank>* — physical bank on which the failure occurred
- *<phys_row>* — physical row on which the failure occurred
- *<phys_col>* — physical column on which the failure occurred
- *<log_bank>* — logical bank (at the port) on which the failure occurred
- *<log_row>* — logical row (at the port) on which the failure occurred
- *<log_col>* — logical column (at the port) on which the failure occurred
- *<bit_no>* — failing bit
- *<phys_exp>* — physical data value that is expected on the failing comparator (the opposite value is actually read)
- *<log_exp>* — logical data value that is expected on the memory data port

Physical Versus Logical Address

In [Figure 4-18](#), the physical position in the memory cell (**PhysicAdr[n]**) refers to the physical address, and the value for the memory bus address (**FuncAdr[n]**) refers to the logical address. The memory BIST controller **AdrCntr[]** is the same as **PhysicAdr[]**. For this to be effective,

the collar cancels the effect of scramble by applying the inverse equations to obtain the memory bus address **FuncAdr[]**.

Figure 4-18. Physical and Logical Address



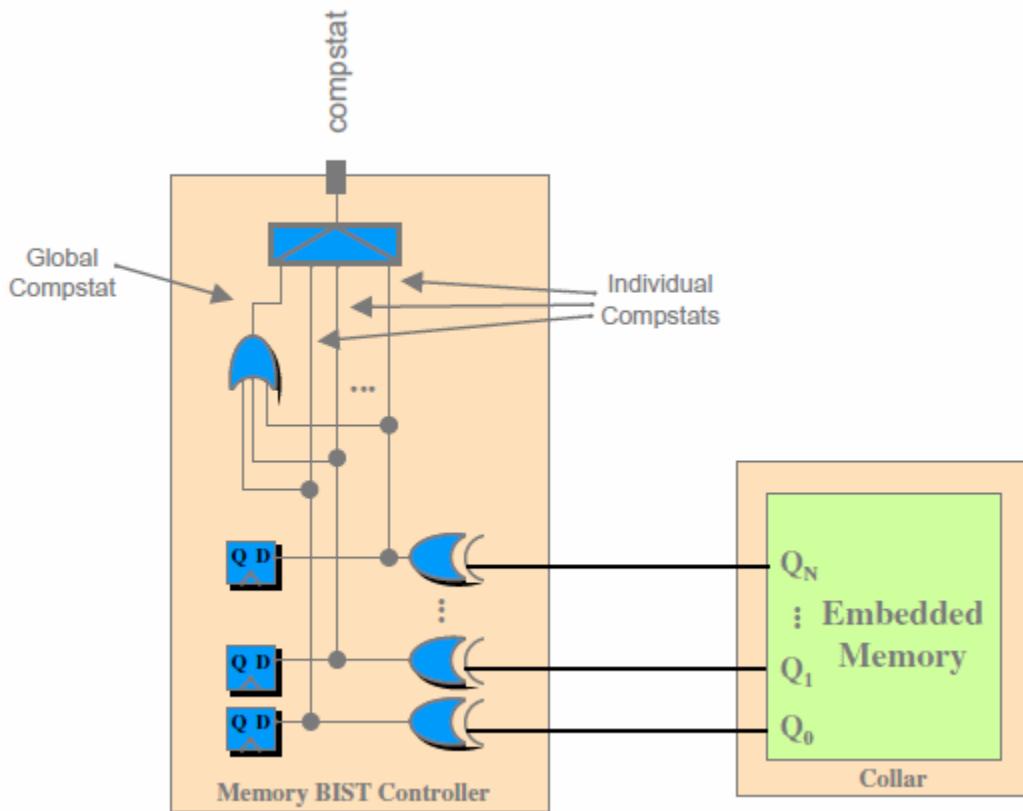
Interactive Debug

During automatic diagnosis, all of the individual comparators are examined for errors. Frequently, these comparators are not directly accessible from a chip pin. As shown in [Figure 4-19](#), the comparators are typically routed through a multiplexer to a single output. Therefore to examine all errors, the Tessent SiliconInsight software runs the memory BIST controller as many times as there are failing comparators for the memory being tested.

Using Global Comparator

If you are only interested in the failing addresses, the individual comparators do not need to be examined. As illustrated in [Figure 4-19](#), the memory BIST controller also contains a global comparator signal. This signal is simply the logical OR of the individual comparators and therefore provides failure resolution down to the address but not to the individual bit.

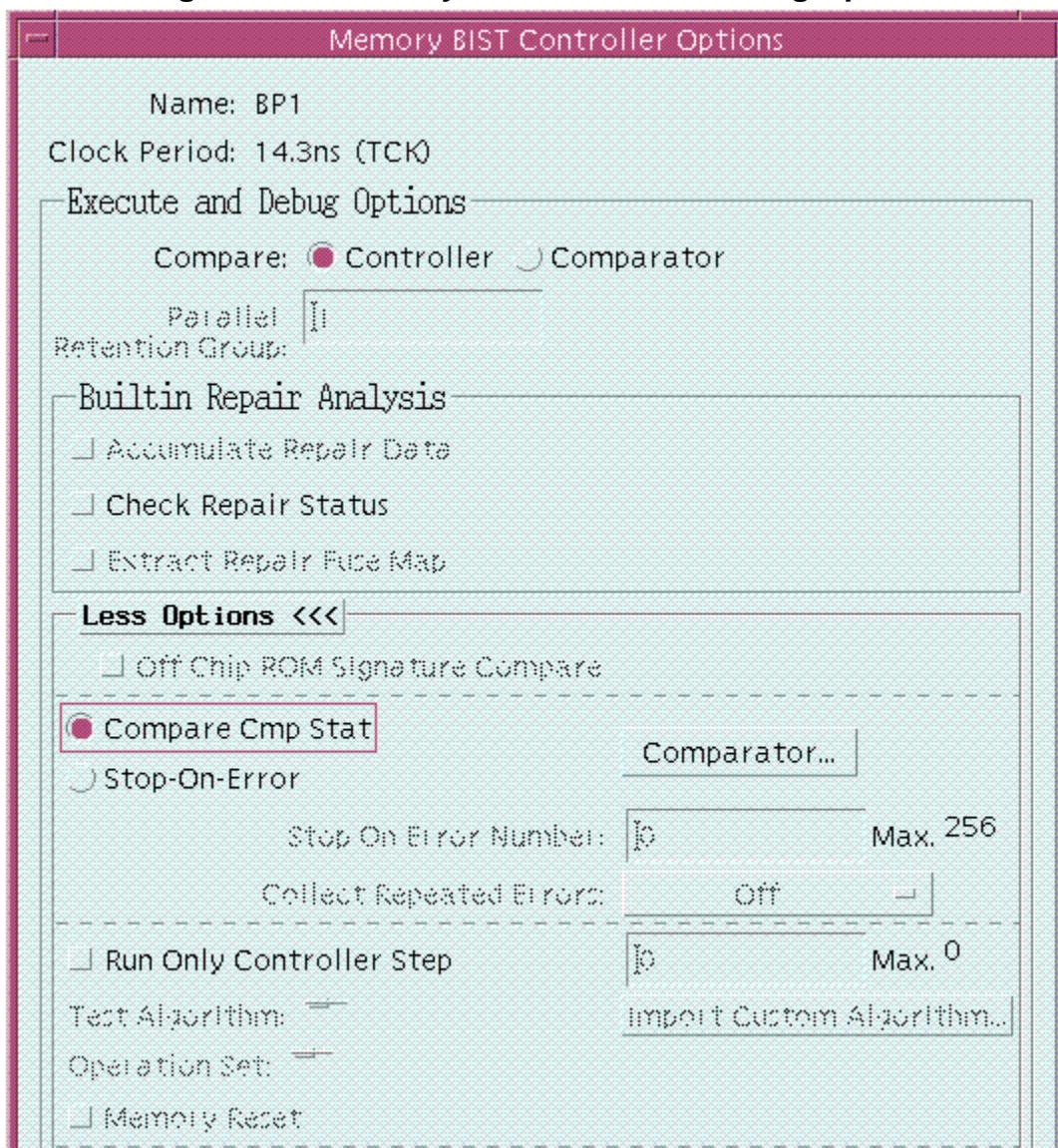
Figure 4-19. Global and Individual Comparators



For the Tessent SiliconInsight software to diagnose using only the global comparator, perform the following steps:

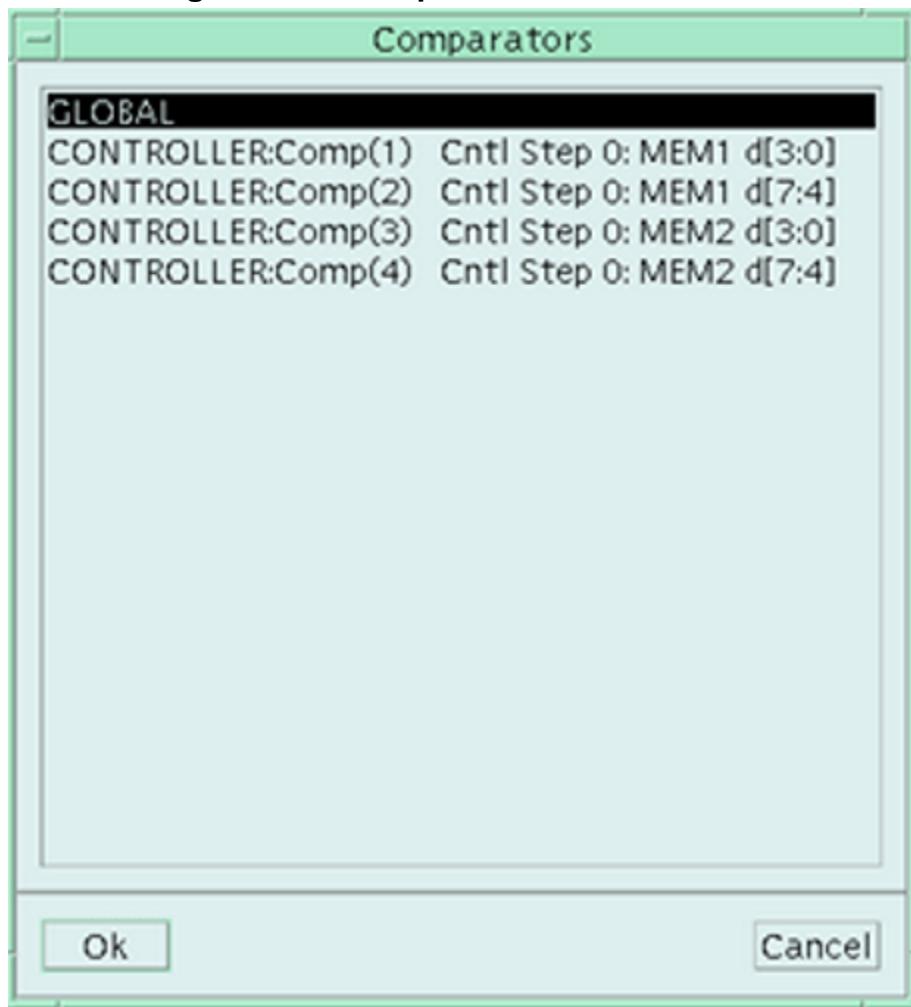
1. Right mouse button click on the *mem* test step icon and select **Options** to bring up the **Memory BIST Test Step Options** panel.
2. Set the **Test Clock Source** option to *tck*. This must be set because compstat-based diagnosis requires TCK-based clocking.
3. Set the **Run Mode** option to *RunTimProg*.
4. Click **OK** to close the **Test Step Options** panel.
5. Right mouse button click on the memory BIST controller icon and choose **Options** to bring up the **Memory BIST Controller Options** menu.
6. Click on the **More Options** button to expand the debug section of the panel as illustrated in [Figure 4-20](#).

Figure 4-20. Memory BIST Controller Debug Options



7. Click on the **Compare Comp Stat** button and then click on the **Comparator** button to bring up the **Comparators** menu as illustrated in [Figure 4-21](#).

Figure 4-21. Comparator Selection Menu



Each line in this menu lists an available comparator to be monitored. Each comparator is described using its assigned number as well as the memory bit slice that it monitors. For example, as shown in Figure 4-21, the memory BIST controller in this example has four comparators—the first two associated with memory *MEM1* and the last two associated with memory *MEM2*. The third comparator, for example, is associated with the [3:0] bit slice of memory *MEM2*.

The **Comparator** menu also lists the global comparator on the first line. To use the global comparator, click on this line and then click **OK** to accept your choice.

8. Click **OK** in the **Memory BIST Controller Options** panel to accept the changes.
9. Click on the **Execute** icon in the menu bar. The Tessent SiliconInsight software executes the memory BIST controller and interprets the global comparator values.

Sample results from the execution are shown in Figure 4-22. Notice that these results are very similar to the ones obtained during automatic diagnosis (Refer to Figure 4-16). The only difference is that the **Comparator** field is not present.

Figure 4-22. Sample Diagnosis Results

```
=====
=====  
LVDB Directory:      demo_chip_eate.lvdb  
LVDB Name:          demo_chip_eate.lvdb  
Test Config:        LVBIST1A_TC1  
  
TestGroup: group_memory  
TestStep: mem (FAILED)  
Execution Time Stamp: 01/08/07 10:14:32  
    MemoryController "BP1" (tck, 14.3ns)  
        Collar "MEM2(SYNC_1RW_1KX8)" register "BP1_GO_ID_REG4" failed (=1).  
Failed data bits = d[bitRange]>d[7:4].  
        Collar "MEM2(SYNC_1RW_1KX8)" register "BP1_GO_ID_REG3" failed (=1).  
Failed data bits = d[bitRange]>d[3:0].  
        Collar "MEM1(SYNC_1RW_1KX8)" register "BP1_GO_ID_REG2" failed (=1).  
Failed data bits = d[bitRange]>d[7:4].  
        Collar "MEM1(SYNC_1RW_1KX8)" register "BP1_GO_ID_REG1" failed (=1).  
Failed data bits = d[bitRange]>d[3:0].  
=====
```

In addition to reviewing only the global comparator results, you might want to concentrate on the results of just one or a few of the individual failing comparators. You can also accomplish this using the comparators menu as follows:

1. Click on the **Compare Comp Stat** button and then click on the **Comparator** button to bring up the **Comparators** menu.
2. Choose the third comparator and click **OK**.
3. Click **OK** again to close the **Memory BIST Controller Options** menu.
4. Click on the **Execute** button.

You obtain results similar to the ones shown in [Figure 4-23](#). Once again, these results are similar to the ones obtained from automatic diagnosis (Refer to [Figure 4-16](#)). The difference is that only the results for the chosen comparator (in this case, *Comparator 3*) are displayed.

Figure 4-23. Sample Diagnosis Result Using Individual Compare Status Signal

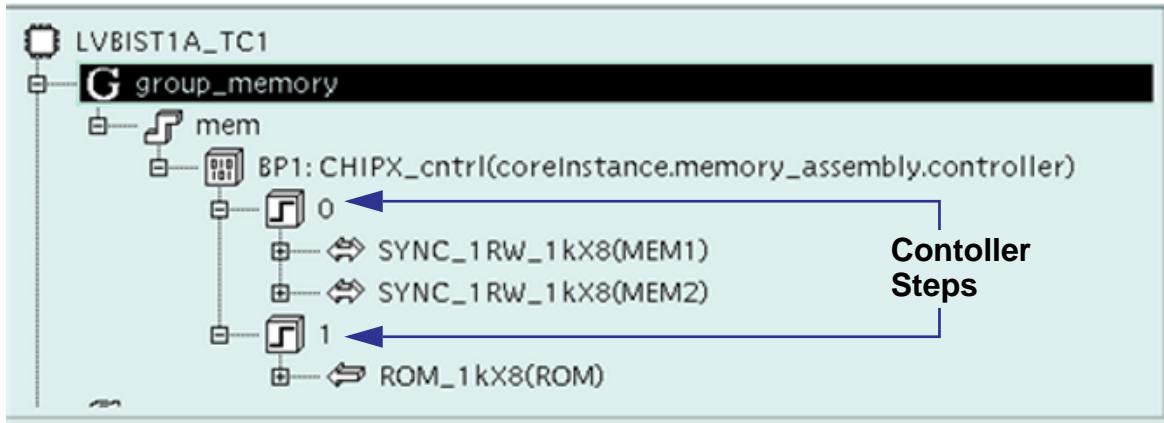
```
=====
LVDB Directory:      demo_chip_eate.lvdb
LVDB Name:          demo_chip_eate.lvdb
Test Config:        LVBIST1A_TC1

TestGroup: group_memory
TestStep: mem (FAILED)
Execution Time Stamp: 01/08/07 13:59:47
    MemoryController "BP1" (tck, 14.3ns)
        Failure#1: Expected 1 (Q[0] = 1) (Cycle 14), TestPort 0, Algorithm
SMarch Phase2, Bit Slice Counter 0, row 0, column 0 (A[9:0] = 0x000)
            Memory MEM2(SYNC_1RW_1kX8), Comparator 3
        Failure#2: Expected 1 (Q[0] = 1) (Cycle 15), TestPort 0, Algorithm
SMarch Phase2, Bit Slice Counter 0, row 0, column 0 (A[9:0] = 0x000)
            Memory MEM2(SYNC_1RW_1kX8), Comparator 3
        Failure#3: Expected 1 (Q[3] = 1) (Cycle 16), TestPort 0, Algorithm
SMarch Phase3, Bit Slice Counter 3, row 0, column 0 (A[9:0] = 0x000)
            Memory MEM2(SYNC_1RW_1kX8), Comparator 3
=====
```

Handling Multiple Controller Steps

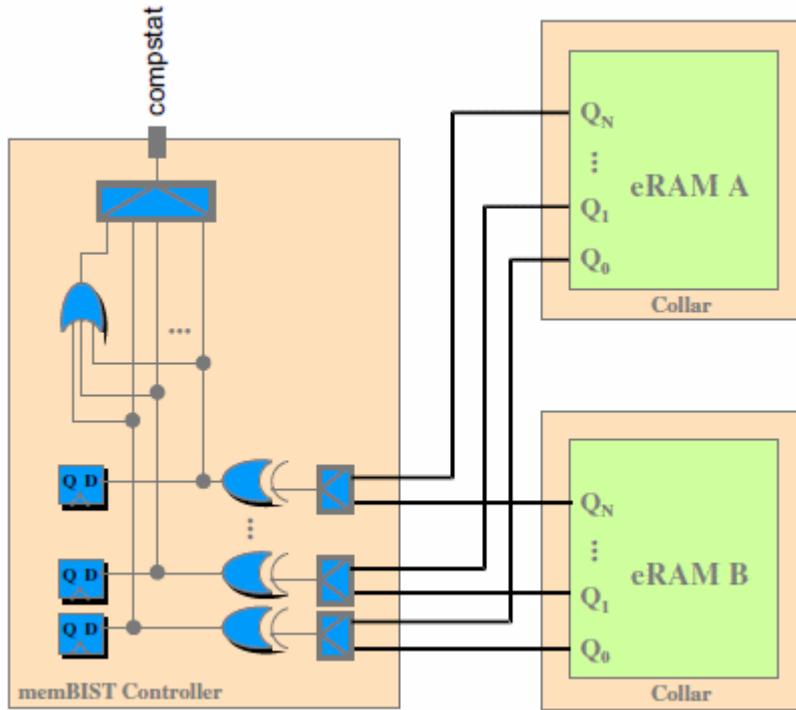
A memory BIST controller can be configured to sequence through several *steps*. Within each step, one or more memories are tested in parallel. For example, note the **Test Configuration** window in [Figure 4-24](#). The memory BIST controller in the Mentor Graphics demo chip has two steps. In *Step 0*, the controller tests two RAMs (*mem1* and *mem2*), and in *Step 1*, it tests a ROM. The number of steps a memory BIST controller has and how they are configured is hard-coded at design time and therefore cannot be altered.

Figure 4-24. Memory BIST Controller Steps



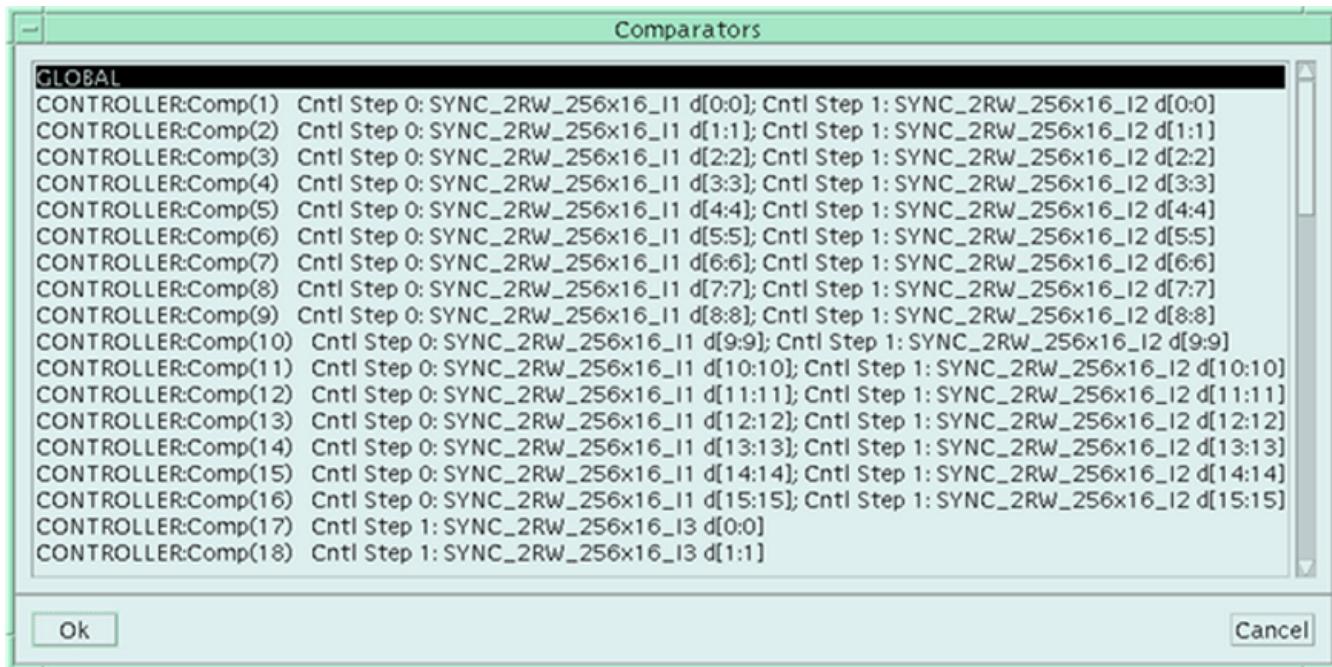
When multiple controller steps exist, the comparators are shared between memories tested in different steps. For example, the embedded memories *A* and *B* in [Figure 4-25](#) are tested in separate controller steps and thus share comparators.

Figure 4-25. Sharing Comparators



The way comparators are shared is reflected in the **Comparators** menu. A sample menu with shared comparators is shown in [Figure 4-26](#). In this example, the first 16 comparators are shared between the two memories *sync_2rw_256x16_i1* and *sync_2rw_256x16_i2*. Comparators 17 through 21 are only used by memory *sync_2rw_256x16_i3*. These are not shared since more comparators are needed in *Controller Step 1* than are needed in controller *Step 0*.

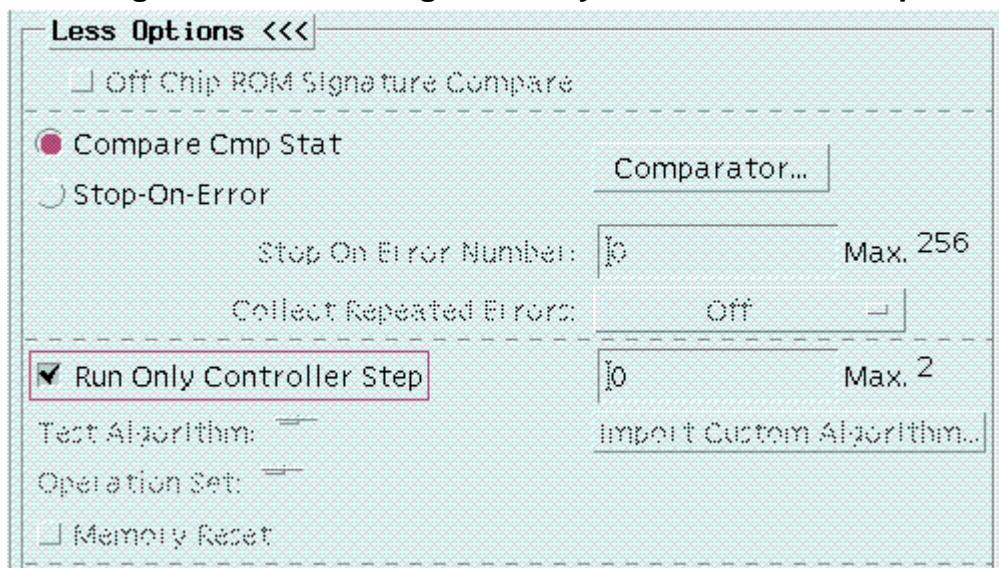
Figure 4-26. Comparator Menu Showing Shared Comparators



When choosing a specific comparator to perform diagnosis, select the controller step that contains the memory you want to diagnose. To accomplish this, perform the following:

1. Right mouse button click on the memory BIST controller and choose **Options** to bring up the **Memory BIST Controller Option** menu.
2. Click on the **More Options** button to expand the debug section.
3. Click on the toggle button to enable the **Run Only Controller Step** option, as illustrated in [Figure 4-27](#).

Figure 4-27. Choosing a Memory BIST Controller Step



4. Enter the desired step number in the **Run Only Controller Step** field.

Performing Bit-Level Diagnosis with Stop-On-Error

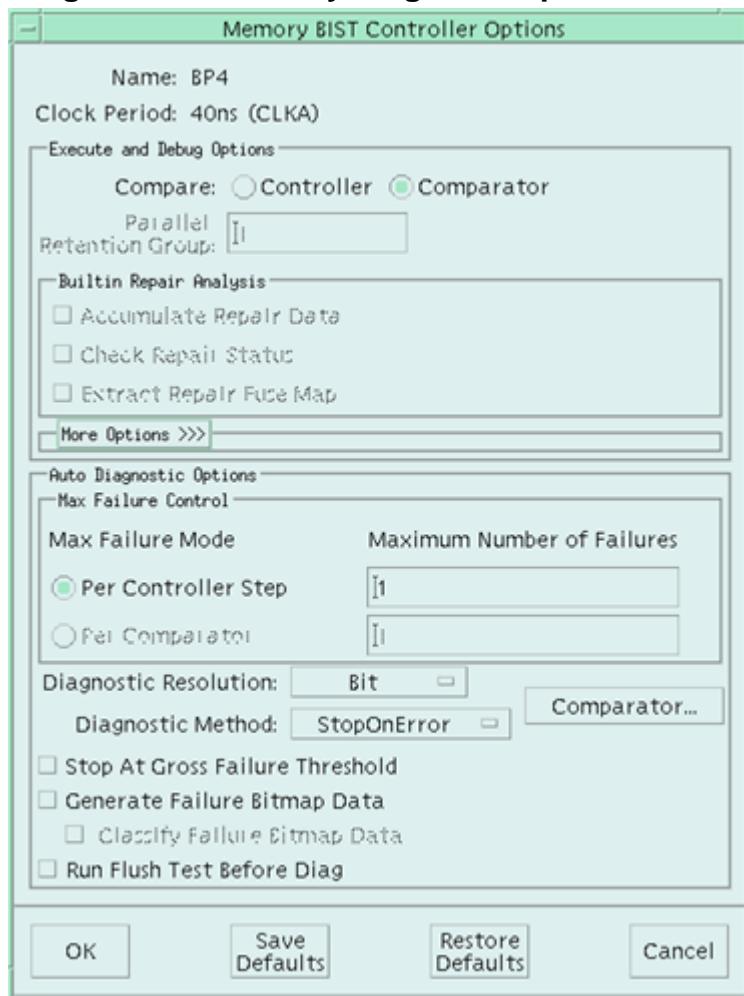
This section describes how to perform at-speed diagnosis using the *Stop-On-Error*-based memory BIST diagnostic approach.

Automatic Diagnosis

To automatically diagnose memory failures using the memory BIST Stop-On-Error approach, perform the following steps:

1. Right mouse button click on the memory BIST controller icon of interest in the **Test Configuration** area to bring up the **Memory BIST Controller Options** menu as illustrated in [Figure 4-28](#).

Figure 4-28. Memory Diagnosis Options Menu



2. Leave the **Max Failure Mode** set to **Per Controller Step** and specify a number for the corresponding **Maximum Number of Failures** field within the **Auto Diagnostic Options** section.

You can specify the number of failures you want diagnosed per controller step. You can set this number to any desired value. Keep in mind that the diagnosis time is directly proportional to this number.

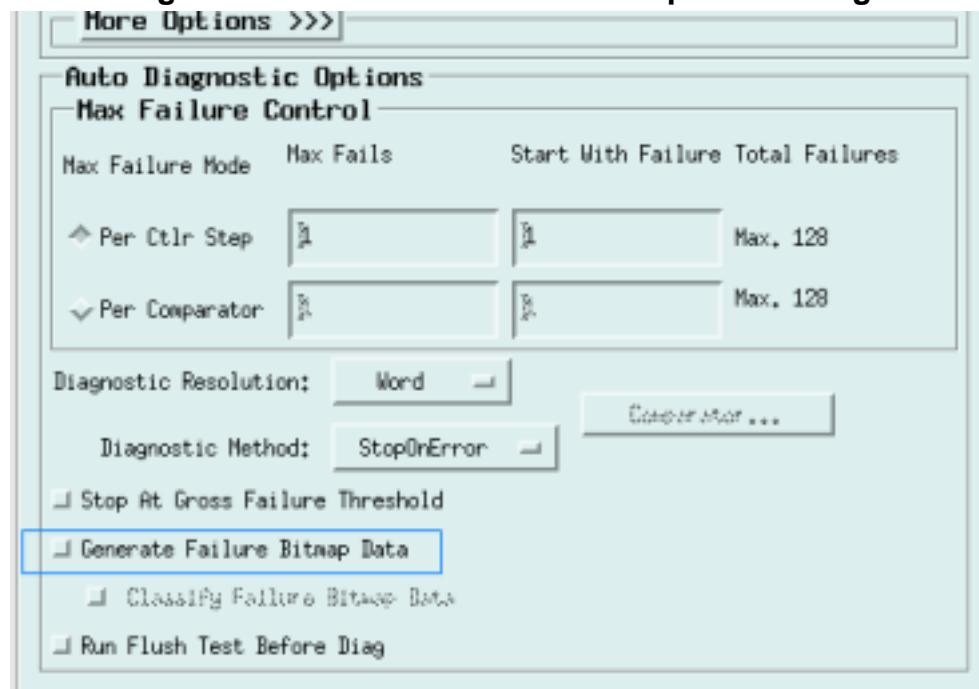
3. Since the intent is to use the Stop-On-Error diagnostic approach, set the **Diagnostic Method** cascade button to *StopOnErrorHandler*. The **Diagnostic Resolution** cascade button allows you to decide if you want to simply know which comparators are detecting errors or if you want to know precisely which bits in the memory are failing. The **Stop-On-Error Diagnostics** method is only available when the bit **Diagnostic Resolution** is selected.
4. Click **OK** to accept your settings and close the **Memory BIST Options** menu.

5. Select the icon you want to diagnose and then click on the **Diagnose** icon in the tool bar (the stethoscope icon) to activate automatic diagnosis.

You can automatically diagnose any icon from the full test configuration down to an individual memory. However, you typically diagnose a controller step or a single memory.

Additionally, you can generate failure bitmap data by selecting the **Generate Failure Bitmap Data** in the **Memory Diagnosis Options** menu as shown in [Figure 4-29](#).

Figure 4-29. Generate Failure Bitmap Data Dialog



A sample Stop-On-Error diagnosis output is shown in [Figure 4-30](#).

Figure 4-30. Sample Results of Automatic Stop-On-Error based Diagnosis

```
=====
LVDB Directory:      LV_FPGA_demo1.lvdb
LVDB Name:          LV_FPGA_demo1.lvdb
Test Config:        default
    TestStep: membistv_1__Default (FAILED)
    Execution Time Stamp: 01/08/07 14:59:21
        MemoryController "BP4" (CLKA, 40ns)
        MemoryController "BP5" (CLKA, 40ns)
            Failure#1: Expected 0 (Q[6] = 0), TestPort 0, Algorithm
SMArchCHKB Phase15, Bit Slice Counter 0, row 63, column 15 (A[8:0]
= 0x1ff)
            Memory SYNC_1RW_512x8_I1(SYNC_1RW_512x8), Comparator 20
            MemoryController "BP6" (CLKA, 40ns)
                Failure#1: Expected 0 (Q[2] = 0), TestPort 0, Algorithm
SMArchCHKB Phase15, Bit Slice Counter 0, row 63, column 15 (A[8:0]
= 0x1ff)
            Memory SYNC_1RW_512x8_I2(SYNC_1RW_512x8), Comparator 22
```

The Tesson SiliconInsight GUI outputs a two line message for each detected memory failure as follows:

Failure #n: Expected <exp1>(<logical_pin_name> =<exp2>) TestPort <tp>, Algorithm <algo> PhaseK / Instruction<i>, Bit Slice Counter <bsc>, bank <bank>, row <row>, column <col> (<logical_address[msb:lsb]> = <address>), counterA <ac>, delay counter <dc> Memory <memory_instance_name>, Comparator <comp>

where the above represents the following criteria:

- <exp1>—physical data value that is expected on the failing comparator (the opposite value is actually read).
- <logical_pin_name>—logical pin name on which the failure is detected.
- <exp2>—logical data value that is expected on the memory port.
- <tp>—test port in which the failure was detected. This is only displayed for a multi-port memory. A test port represents a pairing of a memory input port and a memory output port for test application purposes.
- <algo>—test algorithm applied to the memory. Descriptions of the supported algorithms are provided in Appendix A, “[Memory BIST Algorithms](#).”
- <Phasek / Instruction i>—the algorithms applied by the memory BIST controller consist of several phases. Within each phase, a specific pattern is applied to the memory using a specific address sequence. If the phase identification is known, it will be displayed (Phasek), otherwise, the instruction identification (Instruction i) will be displayed. Descriptions of the available algorithms and their phases are provided in Appendix A, “[Memory BIST Algorithms](#).”
- <bsc>—if a comparator is shared among several memory bits, this represents the bit within that bit slice that the failure was detected on.

- $<bank>$ -physical bank address in which the fault is detected is displayed if the memory has bank segment.
- $<row>$ —logical row address in which the fault was detected.
- $<col>$ —logical column address in which the fault was detected.
- $<logical_address[msb:lsb]>$ —logical address name and bit range on which the failure is detected.
- $<address>$ —logical address at the memory port on which the failure is detected.
- $<ac>$ -counter A value when the fault is detected is displayed if the algorithm uses counter A.
- $<dc>$ -delay counter value when the fault is detected is displayed if the algorithm uses delay counter.
- $<memory_instance_name>$ —memory collar instance where the fault was detected.
- $<comp>$ —the number of the individual comparator that detected the fault.

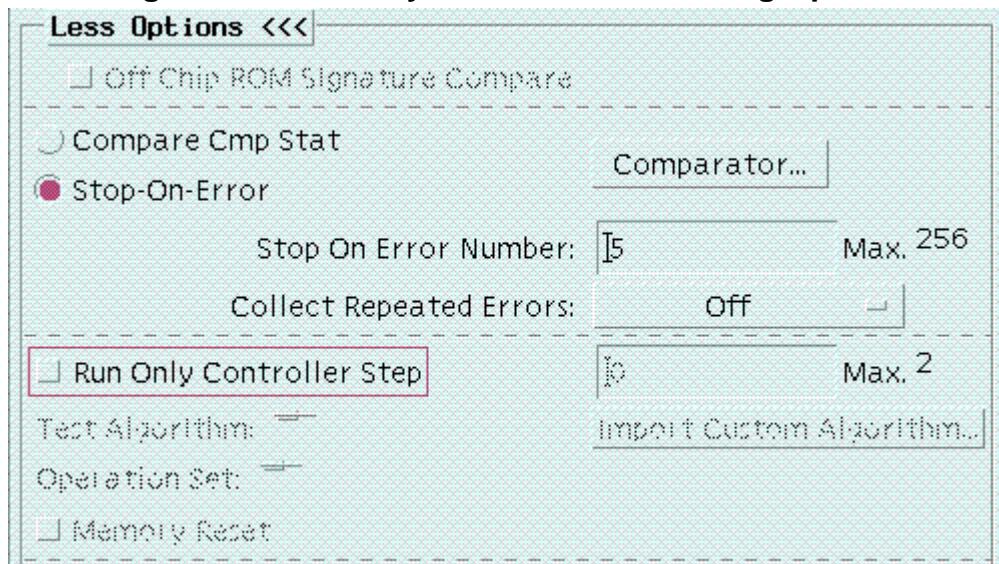
Interactive Debug

It is not uncommon during a debug session to want to only examine specific memory failures. The Tesson SiliconInsight software provides support for such flexibility through a more interactive approach.

To examine a particular failure, perform the following:

1. Bring up the **Memory BIST Controller Options** menu by right mouse button clicking on the memory BIST controller of interest.
2. Click on the **More Options** button to expand the debug section of the menu as illustrated in [Figure 4-31](#).

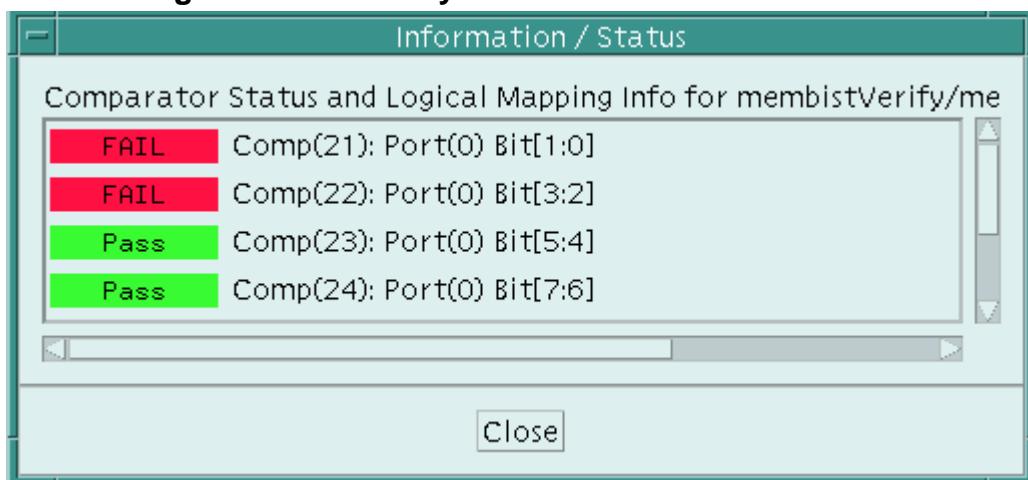
Figure 4-31. Memory BIST Controller Debug Options



3. Click on the toggle button that enables the **Stop-On-Error** option.
4. Type the failure number that you want to examine in the **Stop-On-Error Number** field.
5. Click **OK** to accept your changes and close the **Memory BIST Controller Options** menu.
6. Select the particular memory you want to diagnose in the **Test Configuration** area and click on the **Execute** button. The Tessent SiliconInsight GUI extracts and displays the failure information you requested.

In some cases, you might want to concentrate on failures that occur within one or more particular bit positions within the memory. To accomplish this, you must determine which bit positions are failing. This information is available by clicking on the View menu and selecting the **Memory Info/Status** item. This brings up the **Memory Information / Status** window as illustrated in [Figure 4-32](#).

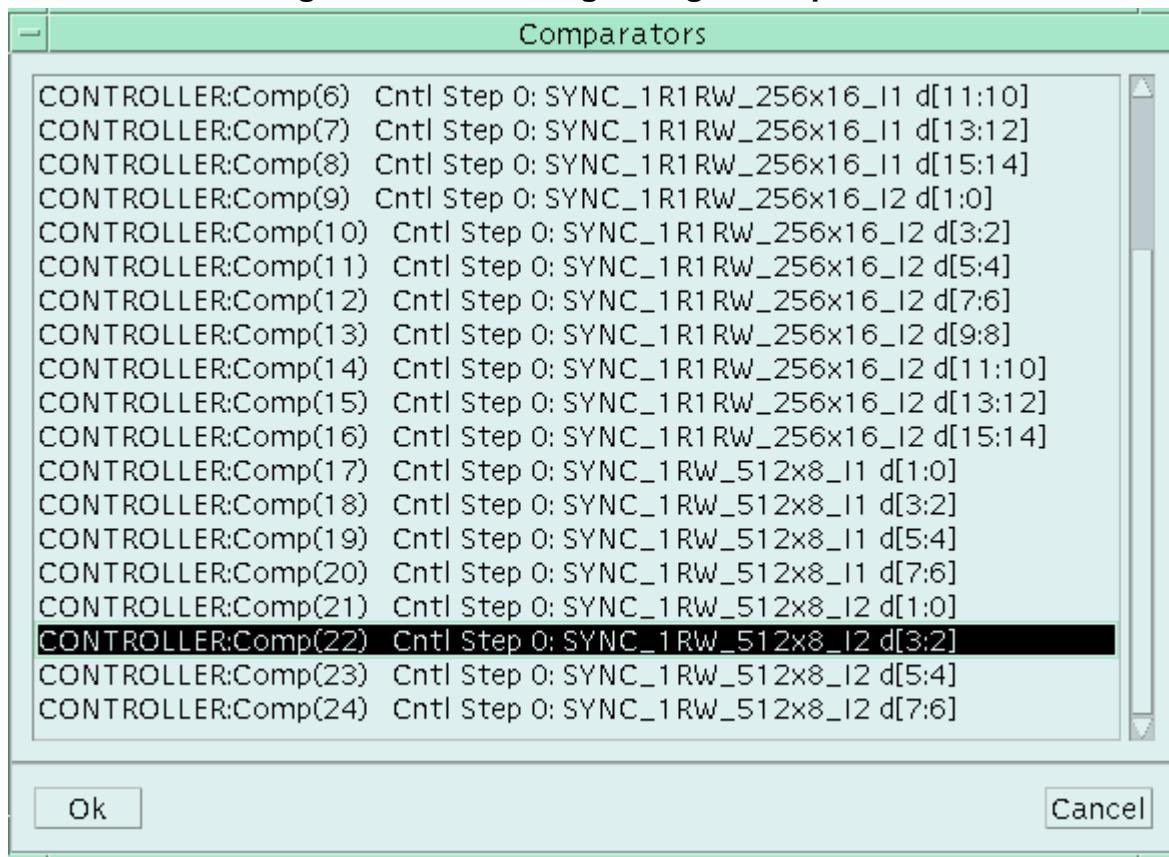
Figure 4-32. Memory Information / Status Window



This window displays which bit positions for the selected memory have failures detected on them. In [Figure 4-32](#), bit ranges 1:0 and 3:2 (*Comparators 21, and 22*) show failures. If you want to concentrate on bit range 3:2, for example, you instruct the Tesson SiliconInsight GUI to perform this as follows:

1. Bring up the **Memory BIST Controller Options** panel and expand the **Debug Options** section.
2. Click on the **Comparator** button to bring up the comparators menu as illustrated in [Figure 4-33](#).

Figure 4-33. Selecting a Single Comparator



3. Select *Comparator 22*, which is associated with bit slice 3:2.
4. Click **OK** to close the menu.
5. Click **OK** to close the **Memory BIST Controller Options** menu.
6. Click on the **Execute** button.

In this case, only the first failure found on the selected comparator (number 22 in this example) is displayed.

Faster Diagnosis

Because each failure must be scanned out from the embedded test controller one at a time, the Stop-On-Error diagnostic approach can be very time consuming. The Mentor Graphics memory BIST controllers support a methodology for speeding up Stop-On-Error diagnosis at the expense of resolution. The methodology is referred to as *Error Collection* and consists in having the controller accumulate errors that are detected within a common section and only stop when an error in a new section is detected. These sections can be a memory bit slice, a memory row or column, or an algorithm phase.

As an example, if the first 8 failures occur on row 1 in the same phase (6), rather than extract each of these failures, you can instruct the controller to extract just the first failure and skip over the rest while keeping a count of the number skipped. The controller stops only when it encounters a failure in a different row or in the same row during a different phase of the algorithm.

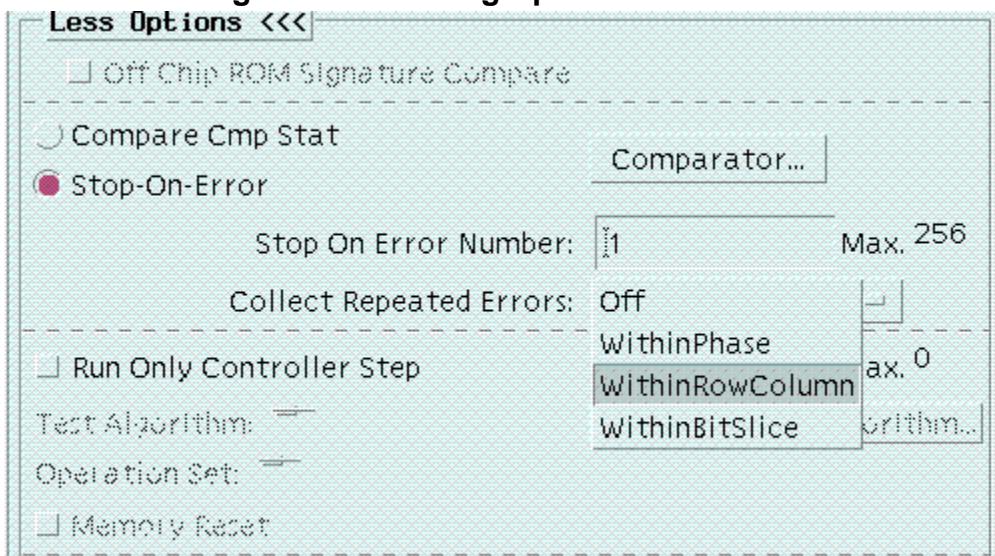
You instruct a memory BIST controller to perform row error collection as follows:

1. Bring up the **Memory BIST Controller Options** menu for the controller of interest and expand the **Debug** section of the panel.
2. Enable the **Stop-On-Error** property.
3. Click on the **Collect Error** cascade button and select *WithinRowColumn* as illustrated in [Figure 4-34](#).

Note

 Controller versions prior to 2009 support the **WithinPhase**, **WithingRowColumn**, and **WithinBitSlice** options. These options are greyed out for post-2009 controller versions.

Figure 4-34. Setting Up Error Collection



When the controller is executed, it skips failures in a common row or column within the same phase. If the number specified in the **Stop On Error Number** field corresponds to a failure that is to be skipped, the controller stops on the next failure that is *not* to be skipped.

Performing Bit-Level Diagnosis with ROM Diagnostics

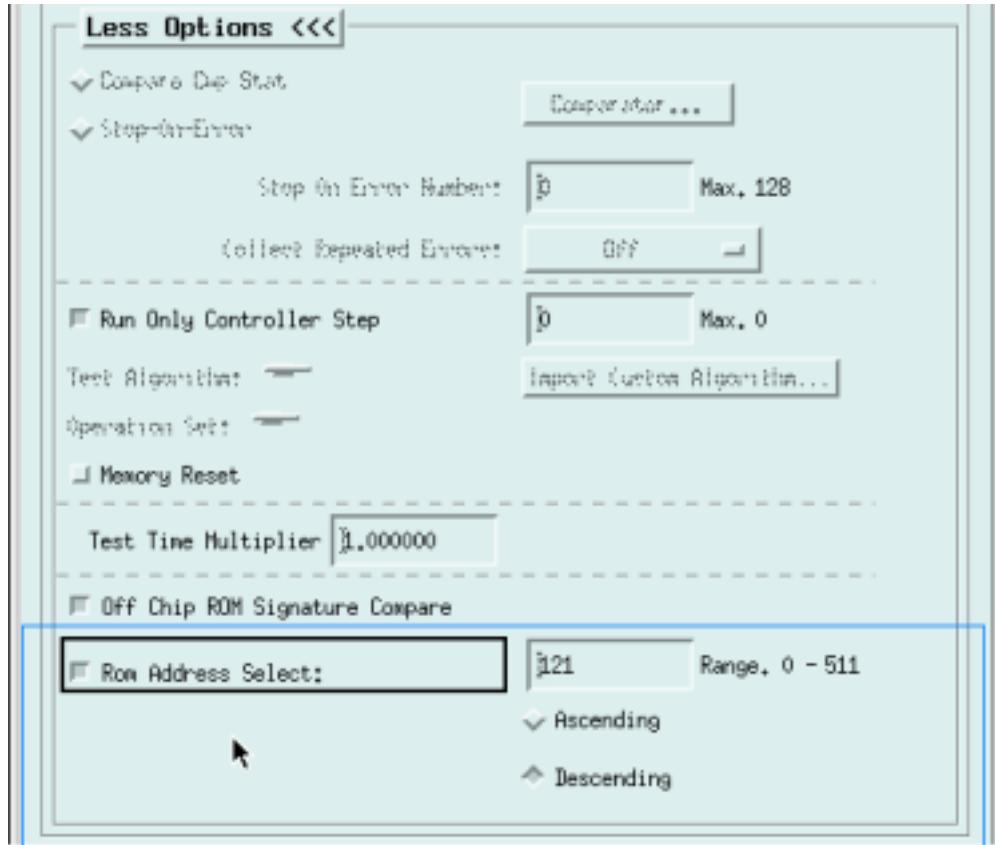
Interactive Debug

It is not uncommon during a debug session to want to only examine specific memory failures. The Tesson SiliconInsight software provides support for such flexibility through a more interactive approach.

To examine a particular failure, perform the following:

1. Bring up the **Memory BIST Controller Options** menu by right mouse button clicking on the memory BIST controller of interest.
2. Click on the **More Options** button to expand the debug section of the menu as illustrated in [Figure 4-35](#)

Figure 4-35. Memory BIST Controller Debug Options



3. Click on the toggle button to enable the **Run Only Controller Step** option and select a ROM controller step.

4. Click on the toggle button that enables the **Rom Address Select** option.
5. Type the failure number that you want to examine in the **Rom Address Number** field.
6. Choose either Ascending or Descending
7. Click **OK** to accept your changes and close the **Memory BIST Controller Options** menu.
8. Select the particular memory you want to diagnose in the **Test Configuration** area and click on the **Execute** button. The Tesson SiliconInsight GUI extracts and displays the failure information you requested.

Chapter 5

Performing Logic Test Diagnostics

This chapter provides step-by-step instructions on how to use Logic Test Diagnostics to direct logic BIST controllers on the DUT to perform production go/no-go and detailed diagnosis of logic.

Chapter topics follow this sequence:

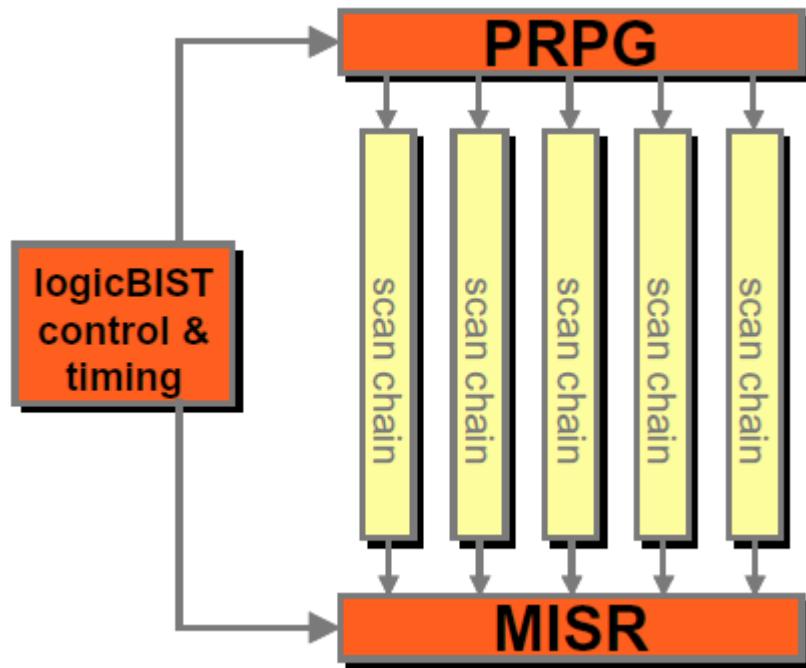
Understanding Logic BIST	103
Execution Flow	104
Diagnosis	105
Clock Control in Burst-Mode Logic BIST	107
Finding Failing Gates	109
Setting Up Logic BIST	112
Clock Control in Burst Mode LogicBIST Controller	113
Clock Control in Legacy Logic BIST Controller	116
Performing Automatic Diagnosis	119
Performing Manual Debug	121
Ignore Vectors in BurstMode Logic BIST Controller	124
Diagnosing Down to Failing Gates	124
Generating a Failure Log File	124
Invoking gateDiagnose	127
Understanding the Gate Diagnostic Output File	129
gateDiagnose Runtime Options Reference	131
gateDiagnose Syntax	131

Understanding Logic BIST

The basic logic BIST architecture is illustrated in [Figure 5-1](#). The logic BIST controller consists of three main components:

- *PRPG*—The pseudo-random pattern generator provides random patterns that are scanned into the internal scan chains.
- *MISR*—The multiple-input signature register compresses results scanned out of the scan chains into a multiple bit signature.
- *Control and Timing block*—This block sequences the activities of the PRPG, MISR, and internal scan chains.

Figure 5-1. LV2004 Version 4.X Logic BIST Architecture



Although a single logicBIST controller can be used to test all logic within a chip, most large chips contain several of these controllers. Additionally, most large designs consist of several cores. A typical scenario is to have a logicBIST controller within each physical region and an additional controller to test the interconnect between the cores and any top-level logic.

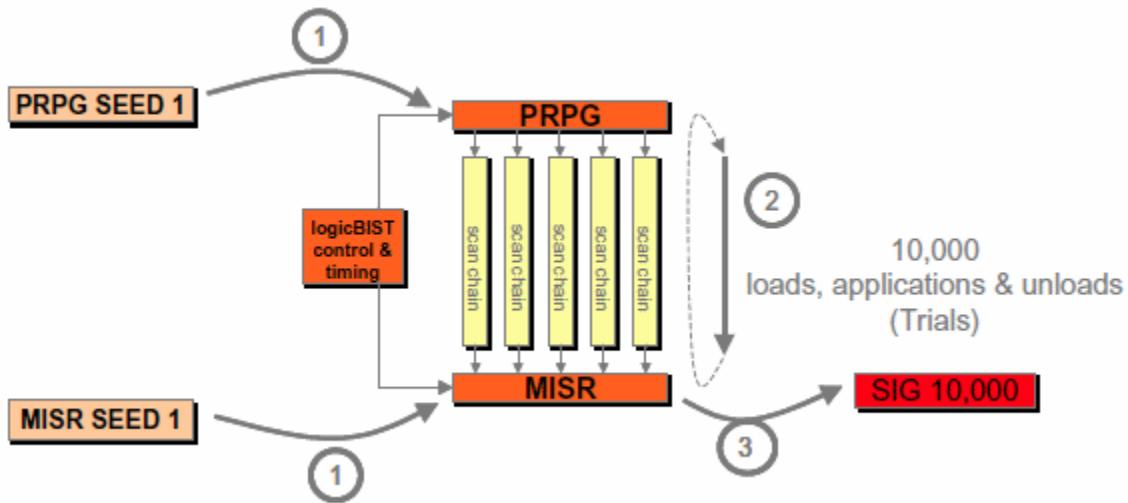
Execution Flow

The execution flow of a logicBIST controller is depicted in [Figure 5-2](#). The flow consists of three steps:

- The PRPG and MISR are scan initialized to known values.
- A large number of logic BIST *trials* are applied to the logic. A trial consists of the following:
 - Loading the scan chains with the random values generated by the PRPG.
 - Applying these random values to the functional logic and capturing the responses back into the scan chains.
 - Unloading and compressing the scan chain values into the MISR.
- Scanning out the signature accumulated within the MISR and comparing the scanned out value to a known value to determine a pass or fail result.

The execution flow is performed automatically by the Tессent SiliconInsight software at the click of a button. This information is described later in the chapter.

Figure 5-2. Logic BIST Execution Flow

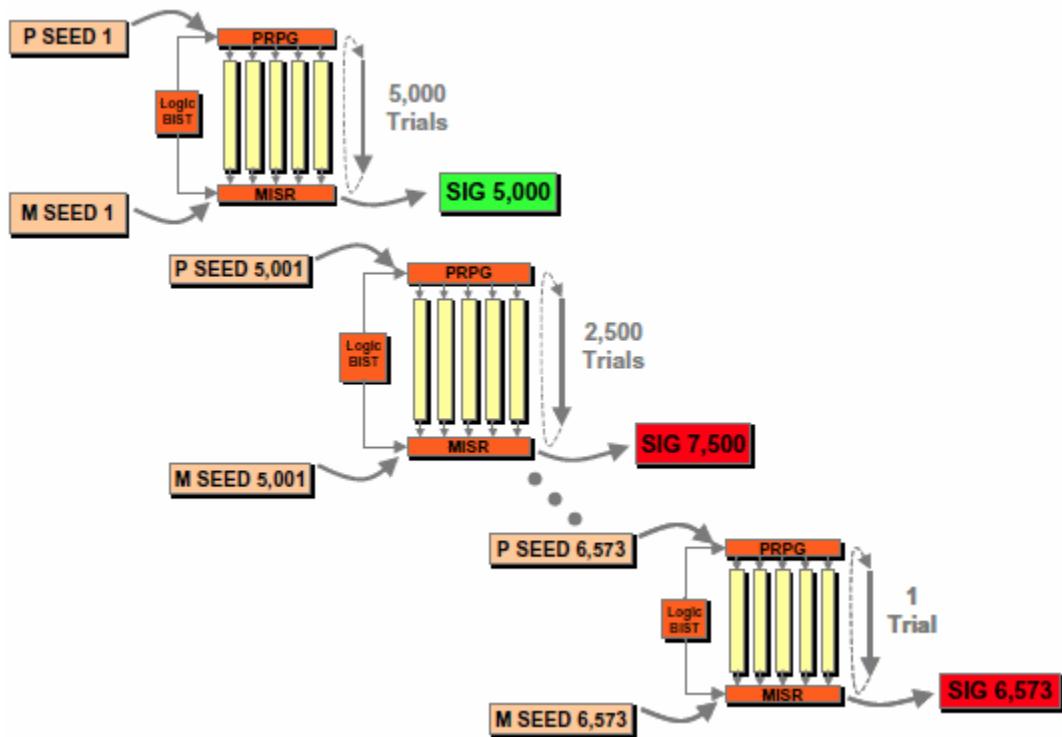


Diagnosis

A logic BIST controller can be used to obtain a pass/fail result and to provide diagnosis down to the flip-flop level. To achieve this level of diagnostic resolution, the basic execution flow must be enhanced to allow for an iterative search process. The diagnostic flow is best described through an example. Consider the initial execution flow shown in [Figure 5-3](#). Assume that the signature scanned out of the MISR after the 10,000 trials is incorrect and thus a failure has been detected. This means that one or more of the trials resulted in one or more incorrect bit (flip-flop) values being scanned into the MISR.

The most basic diagnosis is to find the first of these failing trials. To achieve this, a binary search algorithm is used. The algorithm is based on instructing the logic BIST controller to apply increasingly smaller (by one half) trial subsets until a single failing trial is found. Continuing with the example, the first step is to apply only the first 5000 trials, as illustrated in [Figure 5-3](#).

Figure 5-3. Logic BIST Diagnostic Flow Example

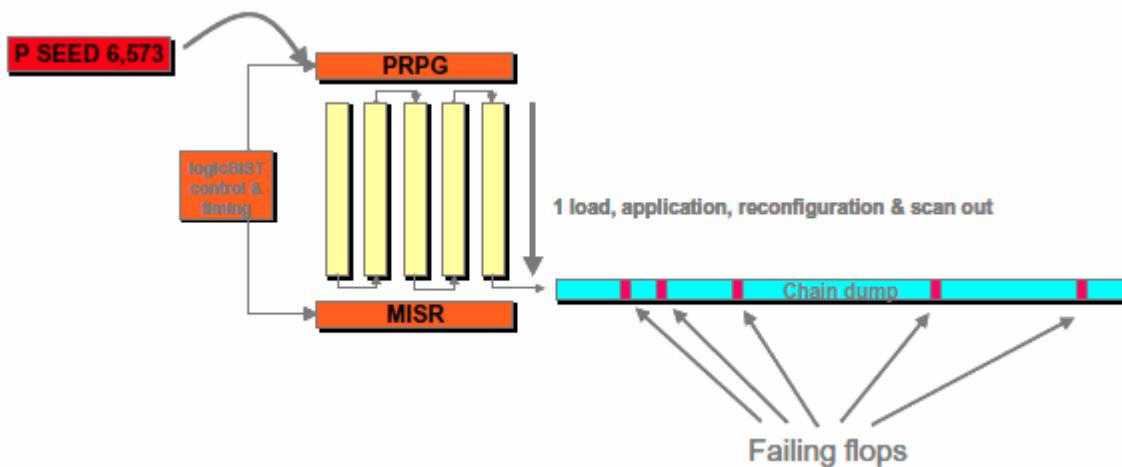


Assuming the signature accumulated after the first 5000 trials is as expected, then the first failing trial is in the second half of the 10,000 trial range. Therefore, next step is to initialize the PRPG and MISR to instruct the controller to apply trials 5001 to 7500. If the accumulated signature is still incorrect, then the first failing trial is in the 5001 to 7500 trial range, so the search is narrowed to within that range. This binary division of the trial range continues down to a single trial.

To determine which flip-flops are failing within the failing trial, the PRPG can be scan initialized to instruct the controller to re-apply the failing trial. However, instead of unloading and compressing the scan-chain values into the MISR, the scan chains are re configured into one long scan chain and its contents are scanned out through the TAP and compared with expected values, as illustrated in [Figure 5-4](#).

The entire diagnostic process is handled automatically by the Tessent SiliconInsight software. Typically, you only need to set a few basic diagnostic options and click on the **Diagnose** button. The automatic diagnostic process is described in “[Performing Automatic Diagnosis](#).”

Figure 5-4. Flop Level Diagnosis



Diagnosis Pattern Reuse Mode

Typically, the auto diagnose algorithm for logic BIST generates a patchable pattern. Then, the algorithm patches and executes that pattern for every iteration of diagnosis for every instance of the DUT tested. The *Diagnosis Pattern Reuse Mode* prevents regeneration of the initial patchable pattern for every DUT diagnosed; that is, once the initial patchable pattern is generated and loaded, the pattern is reused for every DUT. This mode is available on ATE platforms that support pattern patching.

Using the *Diagnosis Pattern Reuse Mode*, you can choose to cache all logic BIST controllers or to cache the diagnostic vectors only for controllers with **Diag-On** enabled. You can also indicate that no caching of diagnostic patterns is to be performed.

In addition, this mode allows you to pre-generate and pre-load all cached diagnostic patterns when the patterns are initially generated and loaded. This prevents vector memory from running out in the middle of characterizing a batch of wafers and devices.

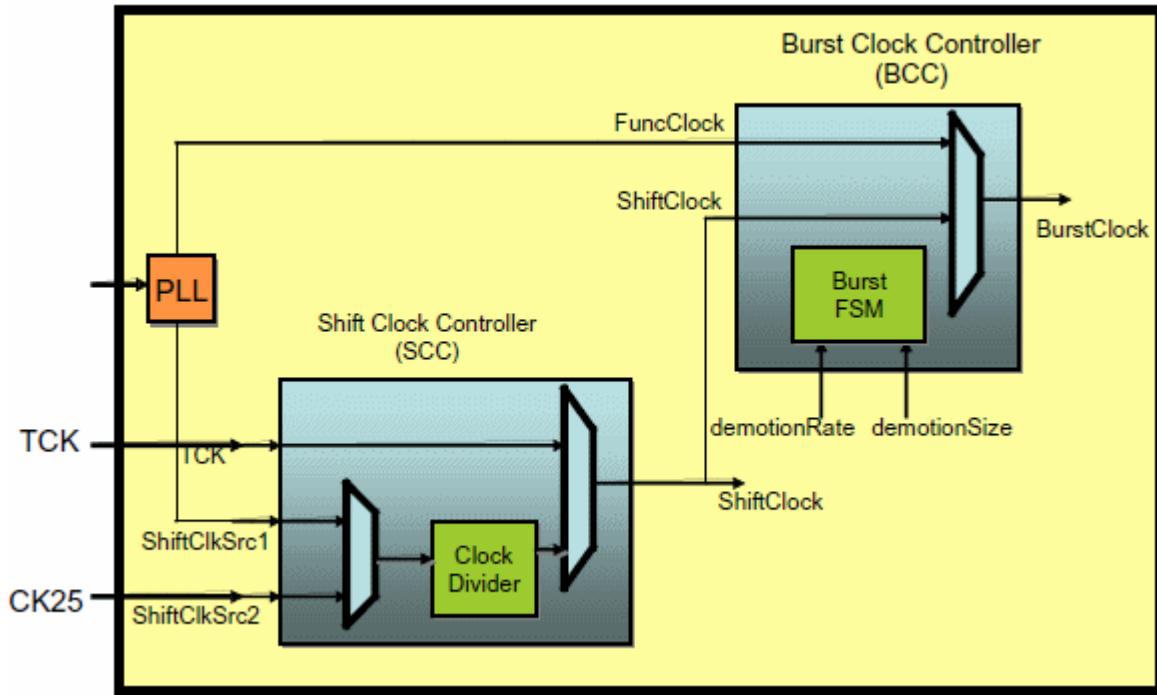
Clock Control in Burst-Mode Logic BIST

Mentor Graphics has introduced the revolutionary Burst-Mode LogicBIST timing architecture as of LV2005 (Version 5.0). The hallmark of the Burst-Mode LogicBIST architecture is the separation of the scan shift and scan capture phases. The scan shift phase can be done at low clock speeds using a common clock source for all the clock domains. Once the scan chains are fully loaded, the controller shifts to the burst phase, in which the true functional clocks are applied. The scan chains are still left in the shift mode while the scan data rotates through the scan chains for a few cycles. Then a single capture cycle is applied and the data is shifted out to the MISR.

Figure 5-5 shows a very simplified Burst-Mode Logic BIST Clocking architecture. This flexible clocking architecture allows you to select at runtime the following:

- **Shift Clock Control**—One of two shift clock sources or TCK. Additionally, the shift clock sources could be divided by a factor of 2, 4, 8, or 16 as needed, driven by the power consumption of the chip during the shift mode.
- **Burst Clock Control**—The true functional clock or the shift clock.

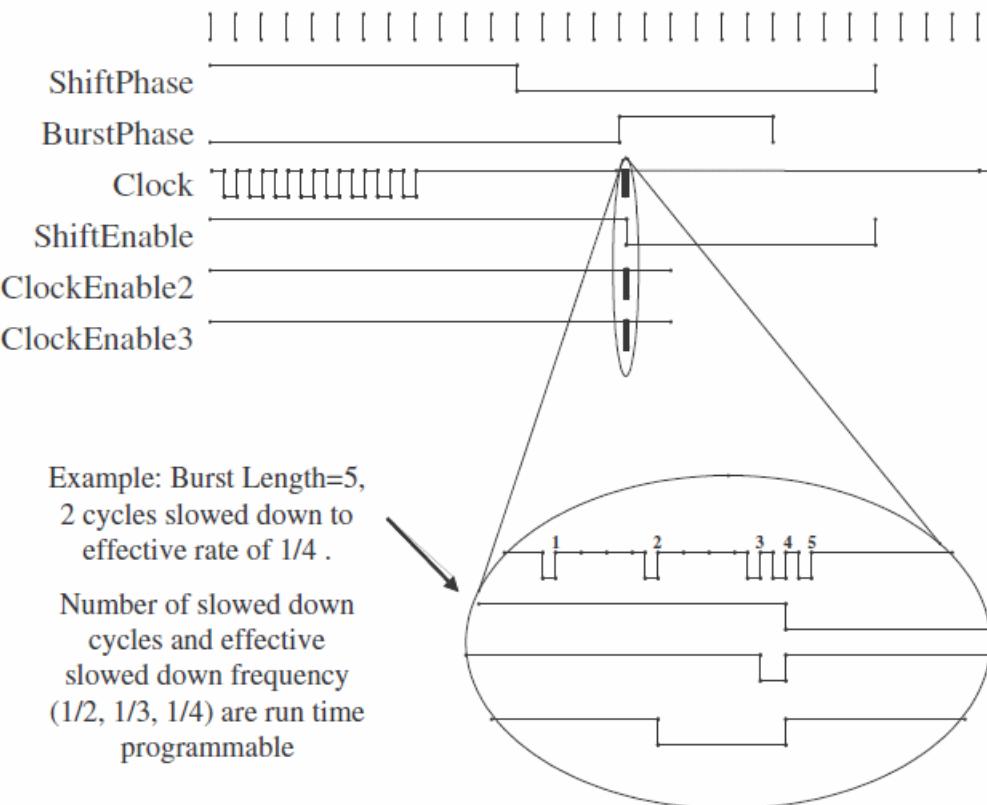
Figure 5-5. Burst Mode LogicBist Clocking Control



Note that each Burst-Mode logic BIST controller will include one **Shift Clock Controller** (SCC) and one or more **Burst Clock Controllers** (BCC) for each clock domain to be tested at-speed in the layout region.

Additionally, you can control the at-speed burst clock waveform as shown in [Figure 5-6](#). For example, you can control how many at-speed shift cycles to be slowed down during the burst phase (*slowed down cycles*) and the spacing between the slowed down pulses (*effective slowed down frequency*). Note that the number of at-speed burst cycles (*burst length*) that a BCC will generate is fixed at the design time and cannot be controlled during Tesson SiliconInsight. You should trade off these values with considerations for power consumption, test time, and test quality.

Figure 5-6. Burst Waveform Control



Finding Failing Gates

Once failing flip-flop data is gathered, the data can be analyzed to diagnose the failures down to the gate and to help debug the design or improve yield. In both design debug and yield improvement modes, the analysis can be done offline.

Narrowing the diagnosis from failing flip-flops down to one or more failing gates presents several challenges:

- *Fault Model*—diagnosis requires comparing observed failing output to simulated failures of modeled faults. Since actual defects do not always correspond to a modeled fault, a perfect match cannot always be found between observed failures and simulated faulty behavior.
- *Multiple faults*—fault simulation usually uses the single fault model; that is, it assumes that one fault is present in the circuit at a time. However, a failing device might have more than one defect, which makes it difficult to match single fault simulations to observed failing data.
- *Diagnosis sign-off*—sign-off of a chip with gate-level diagnosis capability in the past required the building of a fault dictionary. Diagnosis would then consist of searching the fault dictionary for a match with the observed failing data. Such an approach is no

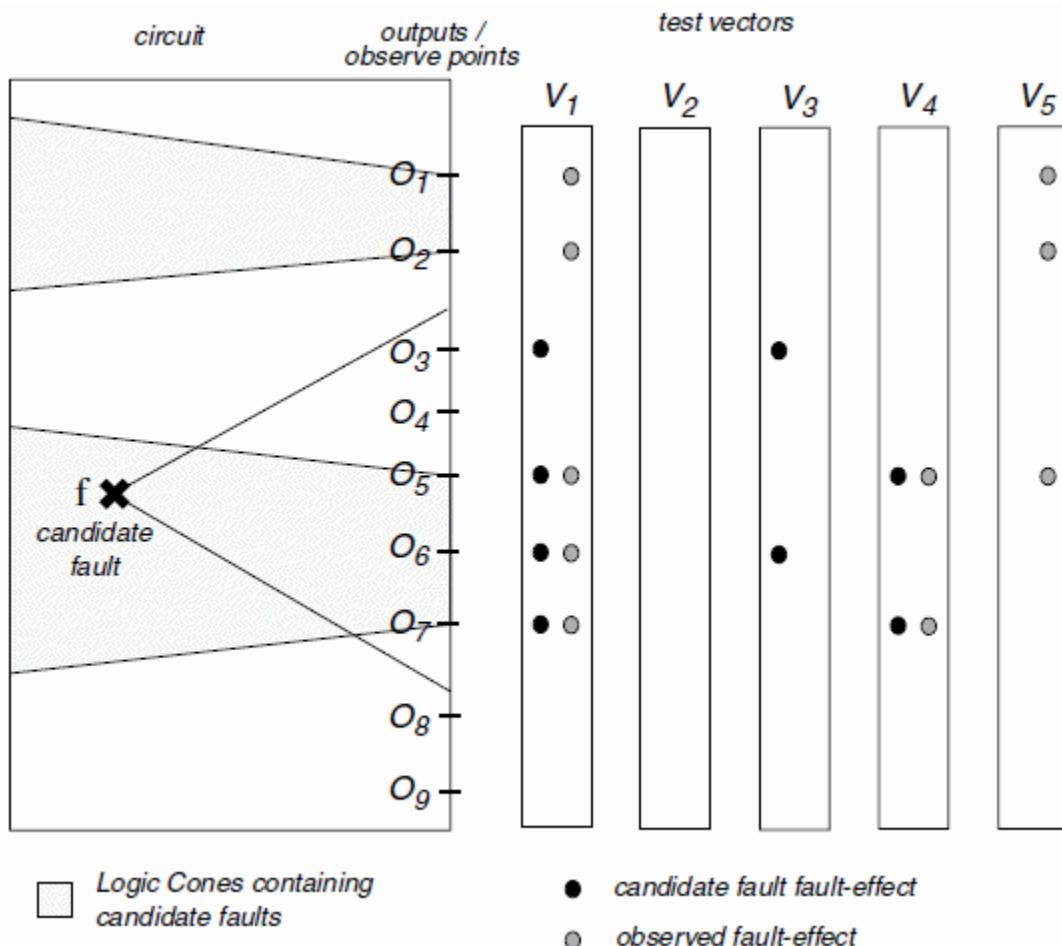
longer viable, as the size of the dictionary is becoming prohibitive. Instead, it is preferred to perform diagnosis dynamically using the observed failing data as input to a diagnostic fault simulation.

In order to support diagnosis in the presence of more than one fault or in the presence of an unmodelled defect, the diagnosis engine does not search for perfect matches. Instead, it uses metrics to order candidate faults and their match likelihood. The order favors the candidate with the biggest fault effect; that is, the fault that ends up affecting the most observed outputs. The following metrics are used for each fault candidate:

- *Candidate fault fault-effect match ratio*—the percentage of fault effects of the candidate fault that match observed fault effects.

Figure 5-7 illustrates metrics for a fault, where for Vector 1, three out of the four fault effects of fault f match observed fault effects from the failing chip. In Vector 2 and 5, there are no fault effects for f , so the match ratio for V_2 and V_5 is not computed.

Figure 5-7. Metrics Example for a Fault f



For Vector 3, fault f has two fault effects; however, there are no corresponding observed fault effects. The match ratio is 0. In such a case, the fault is considered not excited and

the match ratio of 0 is not taken into account when the cumulative (average) match ratio for the fault is computed. The fact that the fault was not excited is reflected in the fault excitation ratio metric described below. For Vector 4, there is a perfect match; therefore, the match ratio is 100 percent.

This metric helps diagnose bridging defects and transition defects, which match well with the stuck-at faults on the defect site when excited, but are not excited in every vector for which the stuck at fault is.

- *Observed fault effect mismatch ratio*—the percentage of observed fault-effects that do not match the candidate fault fault-effects.

In the example of [Figure 5-7](#), there are five observed fault effects in Vector 1. Of these faults, two do not match the fault effects of candidate fault *f*, resulting in a mismatch ratio of 40%. In vectors 2 and 3, there are no observed fault effects, so the mismatch ratio is not calculated. In Vector 4, both observed fault effects match the candidate fault effects, so the mismatch ratio is 0. In Vector 5, there are three observed fault effects and no candidate fault effects, so the mismatch ratio is three out of three or 100%.

- *Candidate fault excitation ratio*—the number of vectors for which at least one candidate fault fault-effect matched an observed fault effect divided by the number of vectors for which there exists at least one candidate fault fault-effect.

The above metrics are also combined into an overall metric with equal weight as follows:

$$\text{overall metric} = (\text{match ratio} + (1-\text{mismatch ratio}) + \text{excite ratio}) / 3$$

[Table 5-1](#) shows the metrics as calculated for the example of [Figure 5-7](#). Note that if the actual defect is a single stuck-fault, the overall metric for that fault is 100%.

Table 5-1. Example of Calculated Metric for Fault f

Metric	Vector 1	Vector 2	Vector 3	Vector 4	Vector 5	Cum. Metric	Sample Size
Match Ratio	3/4 = 75%	N/A	0/2 = 0%*	2/2 = 100%	N/A	5/6 = 83%	2
Mismatch Ratio	2/5 = 40%	N/A	N/A	0/2 = 0%	3/3 = 100%	5/10 = 50%	3
Fault Excitation	1	N/A	0	1	N/A	2/3 = 67%	3
Overall Metric: [.83 + (1-0.5) +0.67] / 3 = .667 or 66.7%							
* 0% Match ratios are not counted towards cumulative ratio							

Setting Up Logic BIST

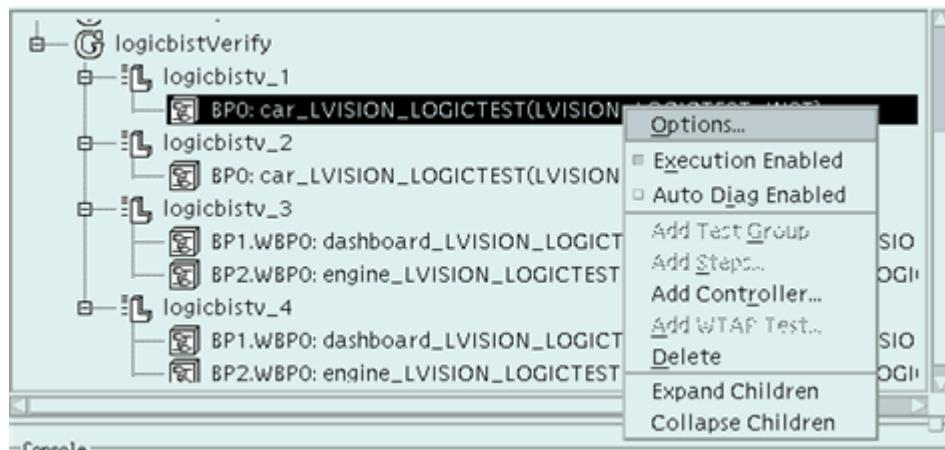
When you bring up the *default.config_eta* configuration file that is provided within the hand-off database (LVDB), all logicBIST controllers within your chip are properly configured for execution. The various settings for each controller were set by the design team. You can, however, change these settings by editing the test configuration from within the Tessent SiliconInsight GUI.

There are only two basic settings that you can modify for a logicBIST controller: the number of trials it applies and the speed at which it applies them.

To understand how to make these changes from the Tessent SiliconInsight GUI, perform the following steps:

1. Bring up the Tessent SiliconInsight GUI by using one of the three modes—offline or LVReady ATE—as described in more detail in the section [Invoking Tessent SiliconInsight](#).
2. Right mouse button click on the logic BIST controller icon from the **Test Configuration** window and choose **Options** to bring up the **Logic BIST Controller Options** menu as illustrated in [Figure 5-8](#).

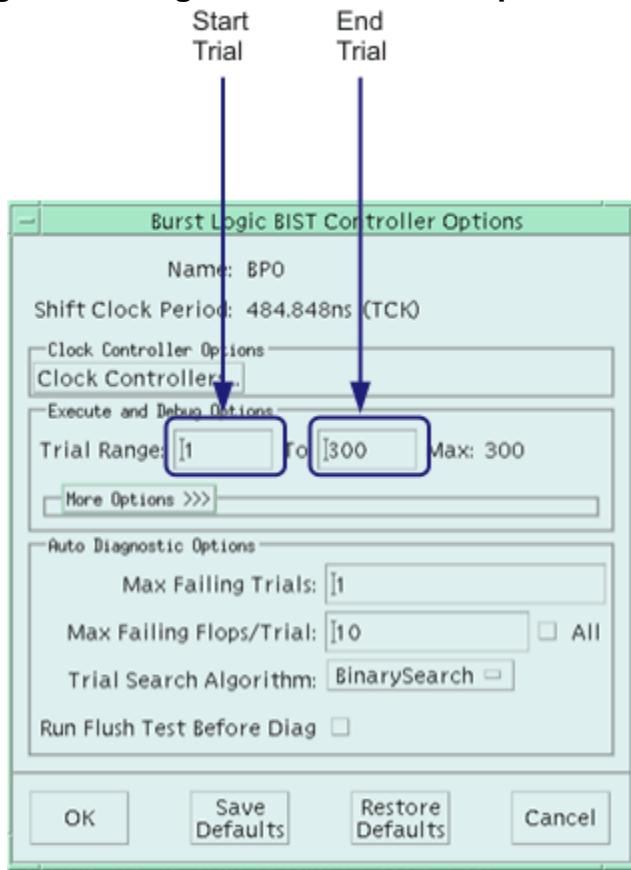
Figure 5-8. Accessing the Logic BIST Controller Options Menu



As shown in [Figure 5-9](#), the **Logic BIST Controller Options** menu allows you to change the trial range that is applied by the controller.

The *Start Trial* number must be greater than zero. The *End Trial* number must be greater than or equal to the *Start Trial* number and cannot exceed the maximum number of trials supported by the controller. This maximum value is displayed in the **Max** field. If you enter a number larger than the maximum supported, the number is automatically changed to the maximum value.

Figure 5-9. Logic BIST Controller Options Menu



Changing the trial range effects both the test time and fault coverage. The change in these two metrics is directly proportional to the change in the trial range. Therefore, the trial range allows you to make trade-offs between test time and fault coverage.

To modify the speed at which the Trials are applied by the logic BIST controller, you need to perform different actions, based on if you are using the *burst mode* logicBIST controller (LV2005 or later) or the the *legacy* logicBIST controller (LV2004, Version 4.2b or earlier).

Clock Control in Burst Mode LogicBIST Controller

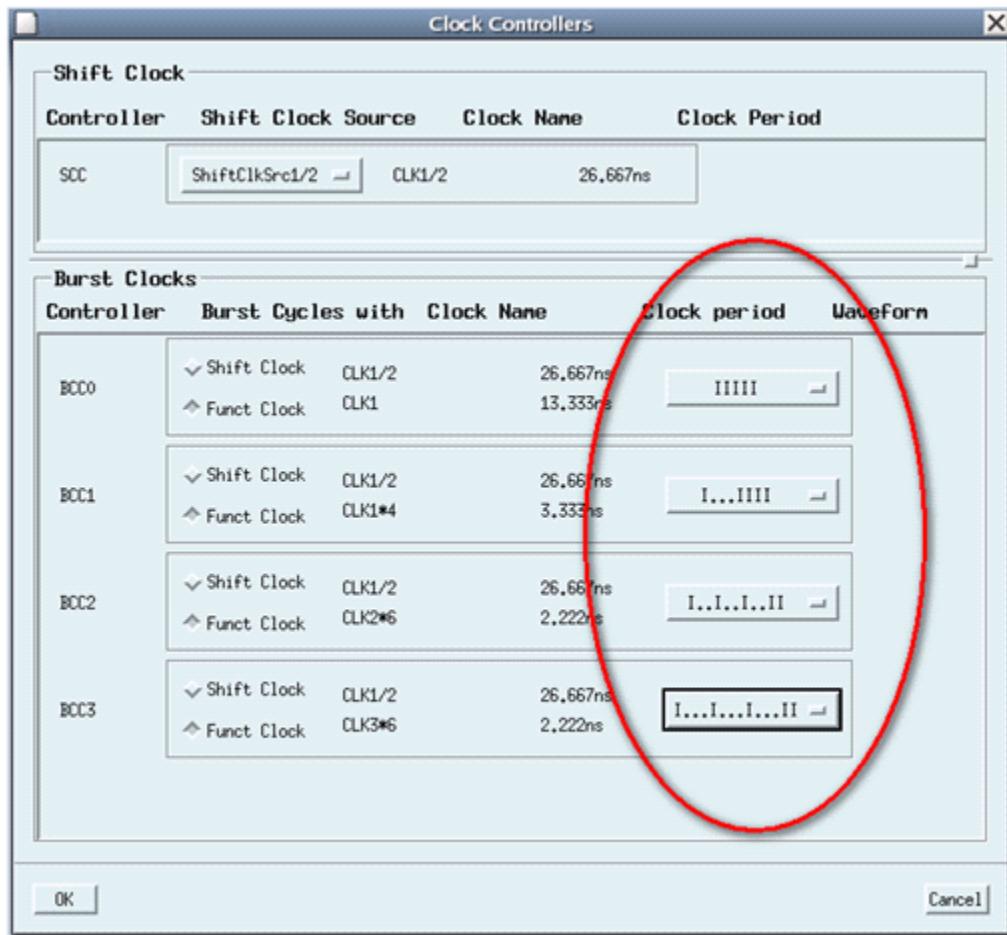
In the burst-mode logicBIST controller, you have independent control over the shift clock and the burst clock. Since there could be more than one Burst Clock Controllers (BCC), you can individually control the capture speed of each clock domain in your design. Note that there may be tester limitations on applying multiple at-speed clocks at the same time.

Controlling Shift Clock

To specify the shift clock, you perform the following:

1. Right mouse button click on the logicBIST controller icon and choose **Options** menu item. This brings up the Burst LogicBIST Controller Options dialog box as shown in [Figure 5-9](#).
2. Click on the **Clock Controllers** button to bring up the Clock Controllers dialog box as shown in [Figure 5-10](#).

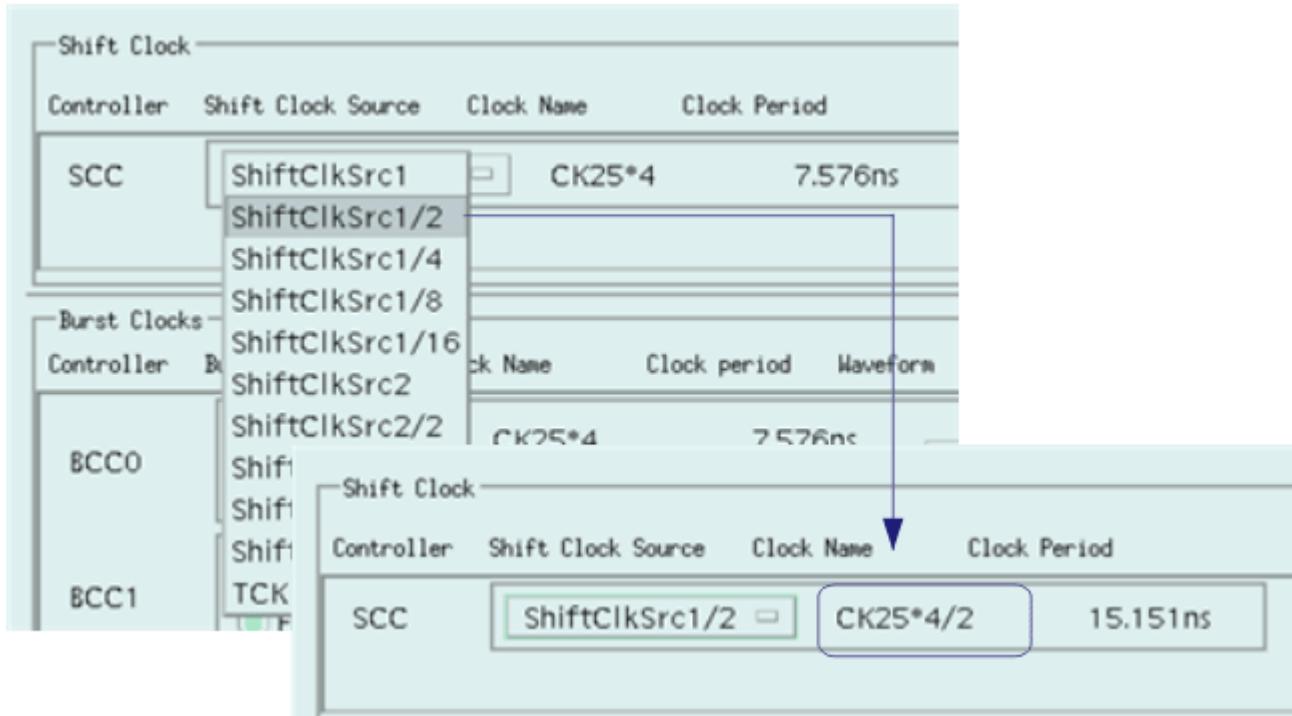
Figure 5-10. Burst Mode Logic BIST Clock Controllers Dialog



3. In the **Shift Clock** area of the dialog box, you can choose the shift clock source using the drop-down list box as shown in [Figure 5-11](#). As you choose the shift clock source, the **Clock Name** field is updated to display any multiplication or division of the primary clock source (e.g. clock going through a \times or a divider). Similarly, the **Clock Period** field is updated as well to show the final resulting shift frequency. You have the following choices for a shift clock:
 - *ShiftClkSrc1*—shift clock source #1 as configured during the design time
 - *ShiftClkSrc1/2*—shift clock source #1 as configured during the design time at divide-by-2 rate

- *ShiftClkSrc1/4*—shift clock source #1 as configured during the design time at divide-by-4 rate
- *ShiftClkSrc1/8*—shift clock source #1 as configured during the design time at divide-by-8 rate
- *ShiftClkSrc2*—shift clock source #2 as configured during the design time
- *ShiftClkSrc2/2*—shift clock source #2 as configured during the design time at divide-by-2 rate
- *ShiftClkSrc2/4*—shift clock source #2 as configured during the design time at divide-by-4 rate
- *ShiftClkSrc2/8*—shift clock source #2 as configured during the design time at divide-by-8 rate
- *TCK*—TAP Scan Clock (TCK)

Figure 5-11. Burst Mode LogicBIST Shift Clock Selection



In the example shown in [Figure 5-11](#), the *ShiftClkSrc1* is sourced at the chip pin CK25 (100 MHz) and goes through a clock multiplier before reaching the SCC. Since *ShiftClkSrc1/2* is chosen as the Shift Clock Source, this clock is then divided by 2, before being output as the shift clock.

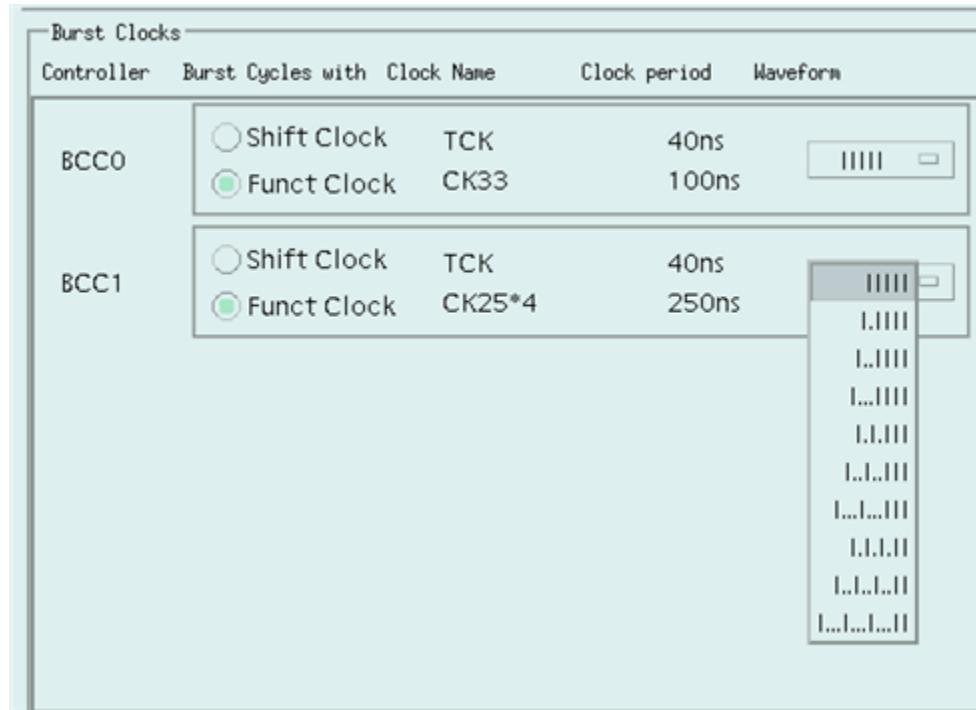
Controlling Burst Clock

As shown in [Figure 5-10](#), in the **Clock Controllers** dialog box, the **Burst Clocks** section allows you to specify the burst clock to use. All the burst clock controllers used by the selected logic BIST controllers are listed here. You can choose either the shift clock to be used as the burst clock or you can choose the burst clock that was pre-configured during the design time.

Controlling Burst Waveform

For each BCC, you also have the ability to control the burst waveform, if you use **Funct Clock** as the burst clock. The waveforms choices are shown with a graphical representation as shown in [Figure 5-12](#). The number of allowable waveforms depends on the burst length of the BCC that was chosen at the design time. The waveforms are ordered such that those resulting in the minimum test time and maximum peak power consumption are at the top. The waveforms that result in the minimum peak power, but take longer test time are at the bottom.

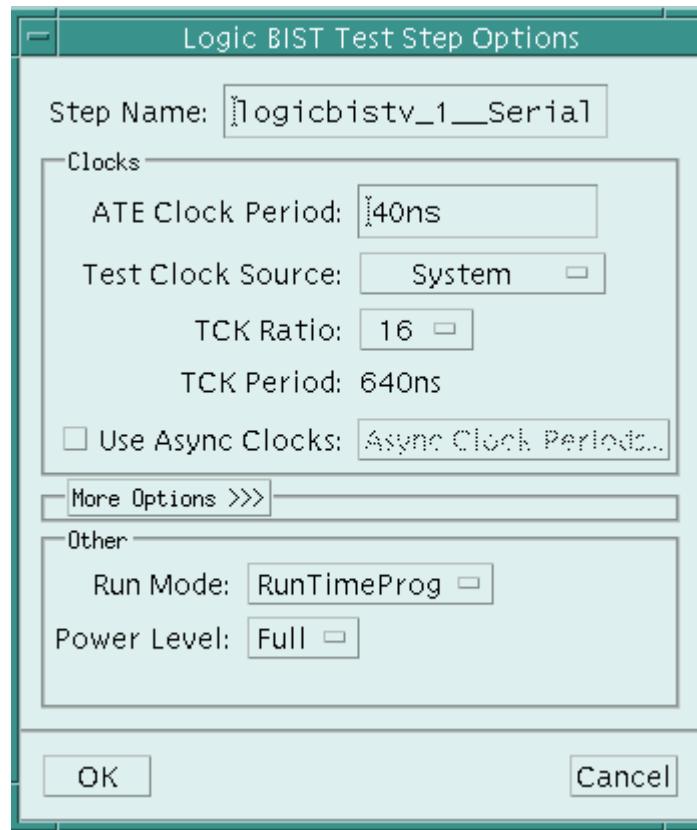
Figure 5-12. Burst Mode LogicBIST BCC Waveform Selection



Clock Control in Legacy Logic BIST Controller

In the legacy logicBIST controller, a single clock controls both the scan shift and the capture waveform. To control the frequency of this clock, you perform the following:

1. Right mouse button click on the logicBIST test step icon and choose **Options** to bring up the **Logic BIST Test Step Options** menu as illustrated in [Figure 5-13](#).

Figure 5-13. Accessing the Test Step Options Menu

Changing the Power Level

1. Set the power level from the **Power Level** cascade button in the **Other** section of the menu, as illustrated in [Figure 5-14](#). You can set the power level from *Full* to *1/8* of full power in *1/8* decrements.

The power level refers to the amount of power the logic tested by the logic BIST controller consumes while being tested. This power is directly proportional to how fast values are being scanned into the internal scan chains or, in other words, how fast the trials are being applied. The faster the trials are applied, the more power is consumed. Note that applying the trials more quickly also reduces the overall test time. So the power level provides another test time trade-off.

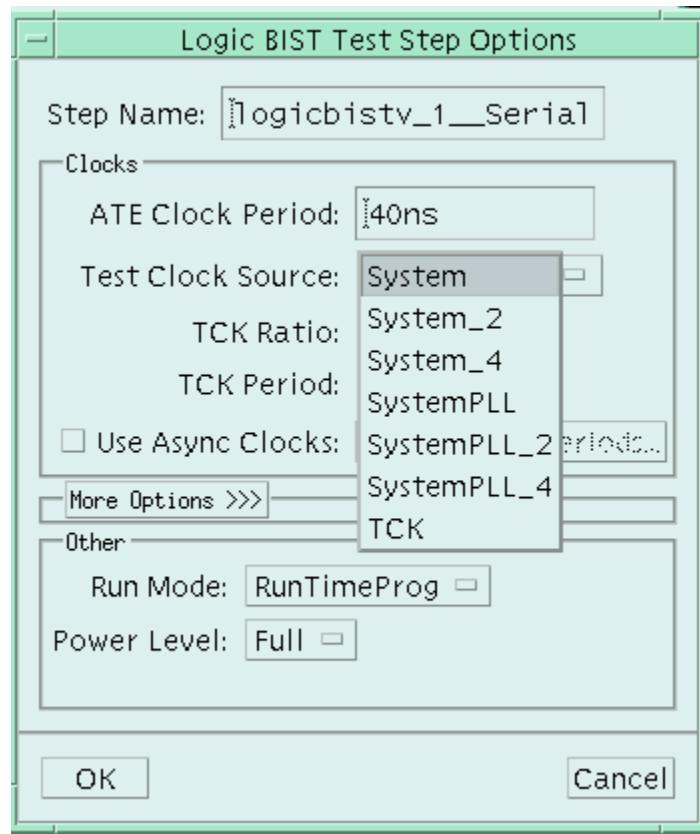
Figure 5-14. Changing the Power Level



Changing the Test Clock

1. You can also change the test clock to apply during the logicBIST from the same dialog box. This allows you to debug speed related failures. Choose the appropriate test clock from the **Test Clock Source** drop-down list box as shown in [Figure 5-15](#). Your choices are:
 - o *System* — apply the at-speed system clock
 - o *System_2* — apply the at-speed system clock at divide-by-2 frequency
 - o *System_4* — apply the at-speed system clock at divide-by-4 frequency
 - o *System* — apply the system clock that is the output of a
 - o *System_2* — apply the system clock that is the output of a at divide-by-2 frequency
 - o *System_4* — apply the system clock that is the output of a at divide-by-4 frequency
 - o *TCK* — apply the TCK clock

Figure 5-15. Changing the Test Clock



Performing Automatic Diagnosis

One of the most powerful features of the Embedded Test Flow is its support of automated real time diagnosis. The Tessent SiliconInsight software supports three levels of logic diagnosis:

- *Trial level*—identifies which trials are failing. This is useful, for example, to identify correlations between different failing devices.
- *Flip-flop level*—identifies which flip-flops in the design are capturing faulty values within any given trial. This is useful for identifying which sections of the device contain defects.
- *Gate level*—provides a report on which gate or gates a given defect can be found. This information can also be fed to third-party defect analysis tools.

Performing logic diagnosis using the Tessent SiliconInsight GUI is simple. Perform the following steps:

1. Right mouse button click on the logicBIST controller icon and select **Options** to bring up the **Logic BIST Controller Options** menu.

2. Set the **Max Failing Trials** field within the **Auto Diagnostic Options** as illustrated in [Figure 5-16](#).

Figure 5-16. Setting Logic BIST Diagnosis Options



Using the **Max Failing Trials** field, you can specify how many failing trials to be identified. This number can range anywhere from *1* to the maximum number of trials applied by the logicBIST controller. When the goal is to visually inspect the diagnostic data (as opposed to feeding it to other analysis tools), you might want to specify a low number in order to keep the log to a manageable size.

3. Set the **Max Failing Flops/Trial** field.

The **Max Failing Flops/Trial** field allows you to specify how many failing flip-flops within each failing trial are to be identified. This number can range from *1* to the total number of flip-flops within any internal scan chain. Once again, if the goal is visual inspection of the diagnostic data, keep this number small.

4. Set the **Trial Search Algorithm** field to *BinarySearch*.

The **Trial Search Algorithm** field allows you to choose which approach the Tessent SiliconInsight software takes to isolate the failing trials. The *BinarySearch* algorithm is best when searching for the first few failing trials because it quickly narrows down the search space.

If the goal is to record a large number of failing trials, then choose the *LinearSearch* algorithm.

If the goal is to record a large number of failing trials and to narrow down the search space, choose the *HybridSearch* algorithm. This option greatly improves the performance of diagnosis. The *HybridSearch* algorithm combines the linear and binary search approaches. With the linear approach, Tessent SiliconInsight searches for the largest number of failing trials in three iterations. As soon as an iteration of the linear search does not yield a failing trial, the binary approach is executed. The binary approach searches for the remaining failing trials—if any exist.

Once the above diagnostic options are set, you invoke diagnosis by selecting the logicBIST controller icon and then clicking on the **Diagnose** button in the tool bar.

During diagnosis, a status window labeled **Diagnosis in Progress** is displayed. Once diagnosis is complete, the results are displayed in the **Console** area. Note that the diagnosis process can take seconds to minutes depending on the amount of diagnosis requested.

The diagnostic results for an example are illustrated in [Figure 5-17](#). As illustrated, two failing trials (76 and 116) are identified as requested. Also, a single failing flip-flop is identified per failing trial (in this case the same one). Notice that the full hierarchical netlist name of the failing flip-flop is provided. This information can be used directly by the design engineers without any data translation.

Figure 5-17. Sample Result of Automatic Diagnosis



```
=====
LVDB Directory: /home/sai/DocReview/test/demo_chip_eate.lvdb
LVDB Name: demo_chip_eate.lvdb
Test Config: LVBIST1A_TC1
TestStep: logic (FAILED)
Execution Time Stamp: 09/09/03 18:11:05
LogicController "BPO" (CLKIN, 14.3ns)
Number of failing trials = 2( 76 116 )
Trial "76" has failing flip-flop instances:
coreInstance.memory_assembly.controller.MBIST_CTL_COMP.\GO_ID_REG_reg[0] (expected 0)
Trial "116" has failing flip-flop instances:
coreInstance.memory_assembly.controller.MBIST_CTL_COMP.\GO_ID_REG_reg[0] (expected 1)
=====
```

I

Failing Trials Failing Flip-Flops

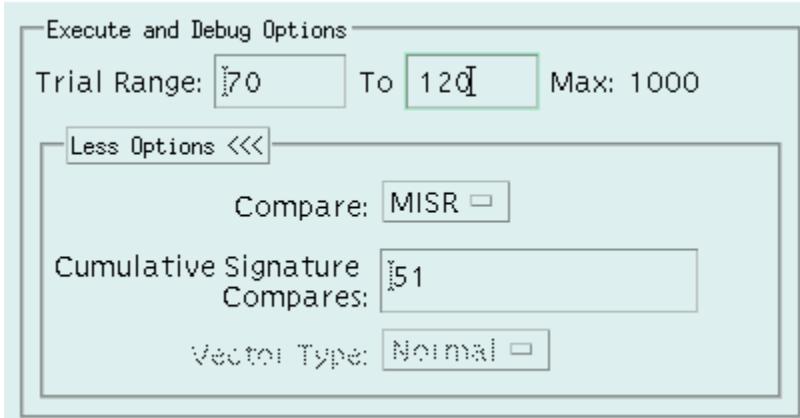
Performing Manual Debug

As described in the previous section, the Tessent SiliconInsight software provides a fully automated way of obtaining detailed diagnostic information. However, you might want to concentrate on specific problem areas. Therefore, a more interactive approach is often needed. To accommodate this, the Tessent SiliconInsight software provides more direct ways of diagnosing failing trials and flip-flops. To understand these capabilities, a more manual approach to obtaining the same diagnostic results as in the previous section is described here.

To begin the manual debug process, perform the following steps:

1. Right mouse button click on the logicBIST controller icon and select **Options**.
2. Set the **Trial Range** to the desired value as shown in [Figure 5-18](#).

Figure 5-18. Changing Options for Debug



3. Click on the **More Options** button to expand the debug section of the menu (if not already expanded).
4. Set the cascade button in the **Compare** field to *MISR*.

This indicates that you want the Tesson SiliconInsight server to only examine the MISR contents as opposed to looking at the individual flip-flop values. This results only in trial-level resolution.

5. You can set the **Cumulative Signature Compares** field. In this example, it was set to 51 (=120-70)+1

Setting this field to a smaller number results in less diagnostic resolution, but reduces the time needed to obtain all signatures. The time requirements can become excessive when large trial ranges are used.

6. Click **OK** to close the **Logic BIST Controller Options** menu.
7. Select the logicBIST controller icon and click on the **Execute** button.

Once execution has completed, the results similar to that shown in [Figure 5-19](#) appear in the **Console** area. Note that there are two failing trials (76 and 116) within the requested trial range. This might be all the information needed for debug. For example, this information is useful if you are trying to correlate the results of different devices. In the example, however, the interest is in determining which flip-flops are failing. Therefore, more debug is required.

Figure 5-19. Result of Trial Level Diagnosis

```

LVDB Name: demo_chip_eate.lvdb
Test Config: LVBIST1A_TC1
TestStep: logic (FAILED)
Execution Time Stamp: 09/09/03 18:22:12
LogicController "BPO" (CLKIN, 14.3ns)
  Trial "76" M[0] 24-bit signature is: "0x46f24d"
    expected is: "0x13e718".
  Trial "116" M[0] 24-bit signature is: "0x768581"
    expected is: "0x23d0d4".
=====
I
Failing Trials

```

1. Bring up the **Logic BIST Controller Options** menu by right mouse clicking on the logicBIST controller icon.
2. Set the **Trial Range** to 76 to help determine which flip-flops are failing within this particular trial.
3. Set the **Compare** cascade button to *Flop* to diagnose down to the failing flip-flops.

Notice that the **Cumulative Signature Compares** field becomes greyed out. This is because when diagnosing down to the flip-flop level, a single trial is examined.

4. Click **OK** to close the **Logic BIST Controller Options** menu. Select the logicBIST controller icon and click on the **Execute** button.

Once execution is complete, you should obtain the results shown in [Figure 5-20](#). As with automatic diagnosis, the full hierarchical netlist name of the failing flip-flop is listed. Note that all failing flip-flops are listed regardless of the value set in the **Max Failing Flops/Trial** field of the **Auto Diagnostic Options** section of the menu.

Figure 5-20. Result of Flip-Flop Level Diagnosis

```

=====
LVDB Directory: /home/sai/DocReview/test/demo_chip_eate.lvdb
LVDB Name: demo_chip_eate.lvdb
Test Config: LVBIST1A_TC1
TestStep: logic (FAILED)
Execution Time Stamp: 09/09/03 18:23:42
LogicController "BPO" (CLKIN, 14.3ns)
  Trial "76" has failing flip-flop instances:
    coreInstance.memory_assembly.controller.MBIST_CTL_COMP.\GO_ID_REG_reg[0] (expected 0)
=====

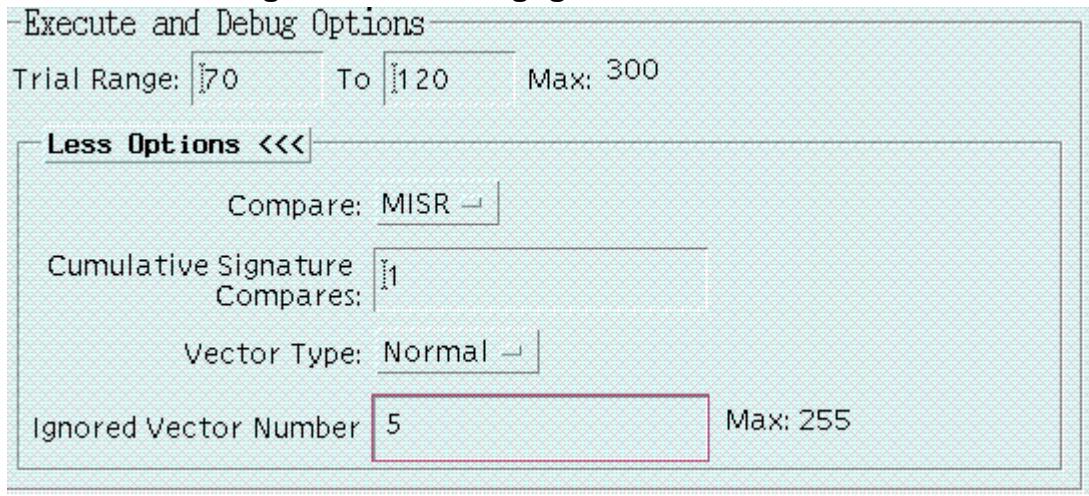
```

Ignore Vectors in BurstMode Logic BIST Controller

In the BurstMode logic BIST controller, you can choose to ignore the first N vectors for the MISR accumulation, in which case, the MISR will be initially loaded with the seed for vector number equal to the start **Trial Range** plus N .

To specify the number of vectors to be ignored, you set the **Ignored Vector Number** to the desired value as shown in [Figure 5-21](#). In this example, it will load the seed for vector 75 and ignore vectors 70 to 74 in the MISR accumulation when executing the test.

Figure 5-21. Setting Ignore Vector Number



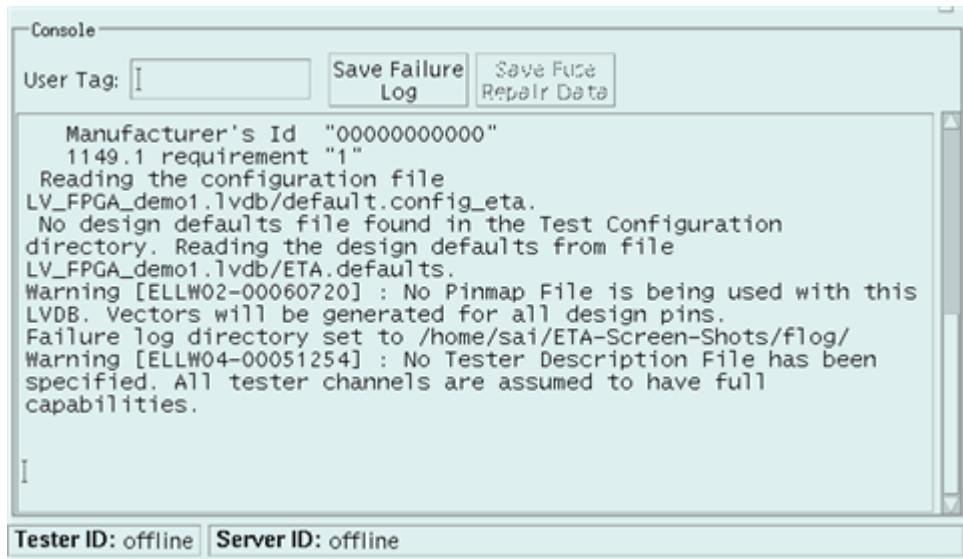
Diagnosing Down to Failing Gates

Diagnosing down to failing trials or failing flip-flops is achieved interactively using the Tessent SiliconInsight GUI. To diagnose down to failing gates requires offline processing of the failing trial and flip-flop data. This offline processing is performed by Mentor Graphics' **gateDiagnose** tool. This tool takes as input one or more failure log (*.flog*) files generated by the Tessent SiliconInsight GUI and design netlist related files. The **gateDiagnose** tool analyzes the failures recorded in the failure log files and reports the most probable candidate faults into one or more gate diagnostic output (*.gdiag*) files. One gate diagnostic output file is generated for each processed failure log file.

Generating a Failure Log File

Tessent SiliconInsight automatically accumulates all failure information that is obtained as a result of logicBIST diagnosis performed during the current session. At any point in time, this accumulated failure information can be flushed to one or more failure log files for later offline processing. Creating the failure log files is as simple as clicking on the **Save Failure Log** button in the **Console** area, as illustrated in [Figure 5-22](#).

Figure 5-22. Saving a Failure Log File



A separate failure log file is created for each logicBIST controller for which failure information was accumulated; that is, for which a successful diagnosis was performed. The naming convention used for the failure log files is as follows:

<design_name>_BP<n>_<tag>.flog

where the above syntax represents the following criteria:

- *design_name*—is the name of the design being diagnosed. This name is automatically extracted from the LVDB.
- *BP<n>*—is the BIST port number associated with the logicBIST controller. BIST port numbers appear next to each logicBIST controller's icon in the **Test Configuration** area.
- *tag*—is the tag name that was last entered in the **User Tag** field in the **Console** area. This tag is used to differentiate failure information obtained at different times and typically under different conditions. If this tag is not changed between consecutive failure log file creations, the old failure log files are overwritten.

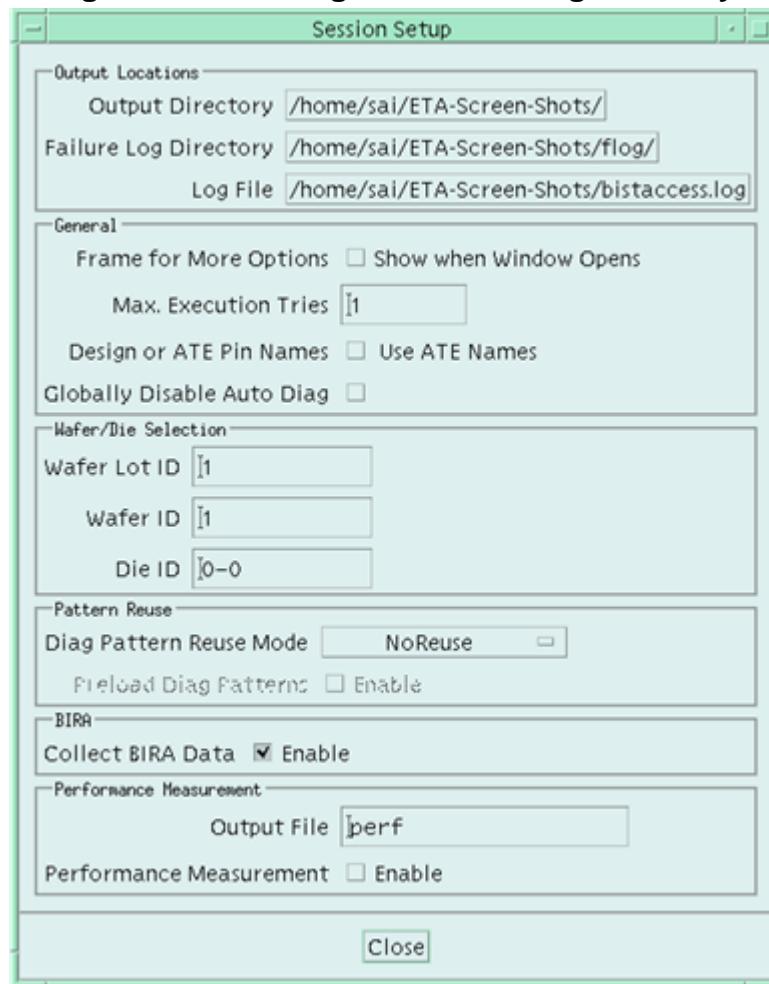
For example, the failure log file for a logicBIST controller is named as follows:

LVBIST1A_BP0_example.flog

Failure log files are saved in the failure log directory. This directory is specified as follows:

1. From the **Tools** pull-down menu, choose the **Session Setup** menu item to bring up the **Preferences** menu as shown in [Figure 5-23](#).
2. Click on the **Failure Log Directory** button to bring up the **Select Failure Log Directory** window. From here you can set any UNIX directory.

Figure 5-23. Setting the Failure Log Directory



Invoking gateDiagnose

Note



To perform gateDiagnosis with a failure log file generated from Tessent SiliconInsight v9.0 and later, and a LVDB from a release *earlier* than Tessent v9.5, you must use ETVerify as shown below to generate the required additional files:

```
etv <designName>
  -inputLVDBName <lvdbDirectoryName>.lvdb
  -configFile <lvdbDirectoryName>.lvdb/<designName>.etManufacturing
  -lbistVectorDump on
```

For failure log file from Tessent SiliconInsight v9.0 and later, and LVDB of version v9.5 and later, nothing special is required.

Once all failure log files of interest are created, the Tessent SiliconInsight GUI (and hence tester) is no longer needed to continue the gate-level diagnostic process. You only need a workstation that has access to the failure log files and the design's LVDB. From this workstation, you can invoke the gateDiagnose tool using the following command line syntax:

```
gatediag <designName>
  -lvdb <lvdbDirectoryName>
  -mode LogicBist
  -failureAnalysisFaults <n>
  -failureLog <flogFileList>
  -hp1Output (On) | Off
  -maxFailingVectors <n>
  -minSampleSize <n>
  -dropThreshold <n>
  -showAllRatios On | (Off)
  -showEquivalentFaults <n>
  -outDir <outputDirectoryName>
  -log <logFileName>
  -minSampleSize <n>
  -simFiles <simFilesName>
```

where the above syntax represents the following runtime options:

- <*designName*>—specifies the name of the design to perform gate-level diagnosis. *designName* can be the top-level chip or an ELT block.
- **-lvdb**—specifies the path to the LVDB of the design. The LVDB contains design netlist related files needed by gateDiagnose.
- **-mode**—specifies the test mode applied that generated the failure log files. For logicBIST failure information, this mode must be set to *LogicBist*.
- **-failureAnalysisFaults**—specifies the number of top probable candidate faults for which the failing vectors will be reported in the .gdiag file. The number of failing

vectors reported for each candidate fault is controlled by the **-maxFailingVectors** option.

- **-failureLog**—specifies either a single failure log file or a list of failure log files. The failure log files must all correspond to the same design and logicBIST controller.
- **-hplOutput**—specifies whether a diagnostic output file in HPL format is to be generated for each input failure file.
- **-maxFailingVectors**—specifies the maximum number of failing vectors to be listed for a particular candidate fault. The number of failing vectors listed for candidate faults in the *.gdiag* file is controlled by the **-failureAnalysisFaults** option. The default value for this option is *5*.
- **-minSampleSize**—specifies the minimum number of samples from which a metric of a candidate fault has been calculated before the fault is made eligible for fault dropping. A fault is dropped from further consideration when it is no longer considered as a likely culprit for the observed failures on the tester. The default value for this option is *15*.
- **-dropThreshold**—specifies the overall metric value below that a candidate fault eligible for dropping gets dropped. A fault is dropped from further consideration when it is no longer considered as a likely culprit for the observed failures on the tester. A candidate fault is eligible for dropping if the sample size of the fault is equal to or greater than the **-minSampleSize** value. The default value for this option is *10*.
- **-showAllRatios**—specifies whether all computed metric ratios are reported in the *.gdiag* file, which is generated by *gateDiagnose*. By default, only the *Overall* ratio is reported.
- **-showEquivalentFaults**—controls the number of top candidate faults for which their equivalent faults are listed. This option defaults to *10*.
- **-outDir**—specifies the path to the directory where the log file and the diagnostic output files are saved.
- **-log**—specifies the name of the log file generated by *gateDiagnose*. The default is *gatediag.log*.
- **-minObservedSampleSize**—specifies the minimum number of samples with observed fault effects on the tester that must be analyzed before any faults can become eligible for fault dropping.
- **-simFiles**—specifies the name of the file that contains all information to properly load the gate-level netlist into Verilog.

For details about the *gateDiagnose* runtime options, refer to

By default, if you do not specify runtime options on the command line, *gateDiagnose* extracts the options from the *.flog* file. You must, however, specify the **-failurelog** option to point to the *.flog* file or list of *.flog* files.

Example

To invoke gateDiagnose for the running example, use the following syntax:

```
gatediag LVBIST1A
  -mode LogicBist
  -lvdb <eta_install_path>demo_chip_eate
  -failurelog <eta_install_path>/
    LVBIST1A_BP0_example.flog
```

Understanding the Gate Diagnostic Output File

By default, the gateDiagnose tool generates the gate-level diagnosis output file, *.gdiag*, illustrated in [Figure 5-24](#), when the **-showAllRatios** command-line option is set to *Off*. The first several lines of the file echo the options used to invoke the gateDiagnose tool. Also, the contents of this file reports a single-ordered list of candidate faults based on the overall probability ratio.

In addition, a list of *n* failing vectors are reported for the first *m* probable candidate faults. The value of *n* is controlled by the command-line option **-maxFailingVectors** and *m* is controlled by the option **-failureAnalysisFaults**.

In the [Figure 5-24](#), note that the list of failing vectors are provided after the candidate fault and its equivalents. The failing vector is prefixed with **v** character.

Figure 5-24. Gate Diagnostic Output File When -showAllRatios is Off

```
#####
##          Diagnostic Summary          ##
#####
File created by      : gateDiagnose
Version             : 4.1   Build xxxx
Created on          : 12/25/02  13:06:41
Module              : fifo_ic_COLLAR;
Mode                : LogicBist;
LVDB                : fifo_ic.lvdb;
Failure Log File   : fifo_ic.flog;
Vector file         : LV_WORKDIR/fifo_ic.vector_lbist;

Ordered Candidate Fault List By Probability:
=====
100.0%      coreInstance.UNITA1_COUNTER.n61           sa1
            = coreInstance.\CNT_MINUS_ONE[0]           sa0
            v 14 28 59 99 127
83.3%       coreInstance.n594   sa0
            v 28 36 156
67.2%       coreInstance.\CNT_reg[0]           .DD sa0
            v 11 76 88
```

When you specify **-showAllRatios On**, the gateDiagnose tool generates a *.gdiag* file that contains four sections. Each section provides an ordered candidate fault list based on either the

Overall ratio, Match Ratio, Mismatch Ratio, or Excitation Ratio metrics. These metrics are described in section “[Finding Failing Gates](#).” The first section, based on the overall ratio, typically provides the most useful candidate fault list information.

In each section, candidate faults are listed in order of their likelihood, starting with the most likely. Each candidate fault consists of a full hierarchical design net name and an associated stuck-at fault.

The faults listed with the equal sign (=) are equivalent faults. The equivalent faults have the same probability value as the candidate fault listed directly before them.

For example, in [Figure 5-25](#), the most likely defect type and location is a stuck-at-one defect on the design net *coreInstance.UNITA1_COUNTER.n61* or a stuck-at-zero defect on the equivalent net *coreInstance/CNT_MINUS_ONE[0]*. Since the probability is listed as 100%, the defect is definitely located on that net or the equivalent fault net and behaves as a stuck-at-one or stuck-at-zero fault.

Figure 5-25. Gate Diagnostic Output File When -showAllRatios is On

```
#####
## Diagnostic Summary ##
#####
File created by          : gateDiagnose
Version                  : 4.0c Build xxxxx
Created on                : 10/20/02 13:06:41
Module                   : LVBIST1A;
Mode                     : logicbist;
LVDB                     : demo_chip_eate;
Failure Log File         : LVBIST1A_BP0_example.flog;

Ordered Candidate Fault List By Overall Ratio:
=====
100.0%      coreInstance.UNITA1_COUNTER.n61           sa1
=          coreInstance.\CNT_MINUS_ONE[0]             sa0
v          14 28 59 99 127
83.3%      coreInstance.n594   sa0
v          28 36 156
67.2%      coreInstance.\CNT_reg[0]                 .DD sa0
v          11 76 88

Ordered Candidate Fault List By Match Ratio:
=====
100.0%  coreInstance.UNITA1_COUNTER.n61  sa1
=  coreInstance.\CNT_MINUS_ONE[0]  sa0
100.0%  coreInstance.n594  sa0

Ordered Candidate Fault List By Mismatch Ratio:
=====
0.0%  coreInstance.UNITA1_COUNTER.n61  sa1
=  coreInstance.\CNT_MINUS_ONE[0]  sa0
```

```

0.0% coreInstance.n594 sa0

Ordered Candidate Fault List By Excitation Ratio:
=====
100.0% coreInstance.UNITA1_COUNTER.n61 sa1
      = coreInstance.\CNT_MINUS_ONE[0]   sa0
  50.0% coreInstance.n594 sa0

```

gateDiagnose Runtime Options Reference

This section describes the runtime options you use to run Mentor Graphics' gateDiagnose tool. This tool enables you to perform gate-level diagnosis on the Tessent SiliconInsight server.

This section describes the available runtime options in this sequence:

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-failureAnalysisFaults	134
-failureLog	135
-hplOutput	136
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-lvdb	138
-maxFailingVectors	139
-minObservedSampleSize	140
-minSampleSize	141
-mode	142
-outDir	143
-showAllRatios	144
-showEquivalentFaults	145
-simFiles	146

gateDiagnose Syntax

The complete syntax for running gateDiagnose from the command line is listed below.

```

gatediag -help
gatediag <designName>
  -dropThreshold <n>
  -failureAnalysisFaults <n>
  -failureLog <flogFileList>
  -hplOutput (On) | Off
  -log <logfilename>
  -lvdb <lvdbDirectoryName>
  -maxFailingVectors <n>
  -minObservedSampleSize <n>
  -minSampleSize <n>
  -mode Single | Multi | LogicBist | ControllerChain

```

```
-outDir <outputDirectoryName>
-showAllRatios On | (Off)
-showEquivalentFaults <n>
-simFiles <simFilesFileName>
```

Valid values for command-line options are *case-insensitive*.

In the syntax above, the variables represent the following:

designName identifies the prefix for all generated module names and all design-related output files, except the log file. *designName* also specifies the default prefix for the input configuration file.

Specifying the **-help** option displays a summary of the command-line syntax and usage. Typing **gatediag** without any parameters also displays this summary.

By default, if you do not specify runtime options on the command line, the **gateDiagnose** tool extracts the options from the *.flog* file. You must, however, specify the **-failureLog** option to point to the *.flog* file or list of *.flog* files.

-dropThreshold

The **-dropThreshold** option specifies the overall metric value below which a Candidate Fault eligible for dropping gets dropped. A fault is dropped from further consideration when it is no longer considered as a likely culprit for the observed failures on the tester. A Candidate Fault is eligible for dropping if the sample size of the Fault is equal to or greater than the **-minSampleSize** value.

Syntax

The following syntax specifies this option:

```
-dropThreshold <n>
```

where *n* is an integer specifying the metric threshold in percent.

Default Value

The default value is *10*.

Usage Conditions

The integer value specified for the **-dropThreshold** must be in the range of *0* and *100* percent inclusive. A value of *0* implies that no candidate faults will be dropped. The value of *100* implies that only faults with perfect matches are kept.

Example

In this example, gateDiagnose will drop candidate faults if the overall metric computed for the fault is falls below 15% and the sample size is at least 12.

```
gatediag circuitA -mode multi -lvdb circuitA.lvdb      -failureLog  
circuitA.flog -minSampleSize 12                      -dropThreshold 15
```

Related Information

[-minObservedSampleSize](#)

-failureAnalysisFaults

The **-failureAnalysisFaults** option specifies the number of top probable candidate faults for which the failing vectors will be reported in the *.gdiag* file. The number of failing vectors reported for each candidate fault is controlled by the **-maxFailingVectors** option.

Syntax

The following syntax specifies this option:

```
-failureAnalysisFaults <n>
```

where *n* is an integer specifying the number of candidate faults with failing vectors.

Default Value

The default value is *10*.

Usage Conditions

None

Example

In this example, *gateDiagnose* reads the *circuitA.flog* failure log file and reports the failing vectors for the top *15* candidate faults.

```
gatediag circuitA -mode LogicBist -lvdb circuitA.lvdb -failureLog
circuitA.flog -maxFailingVectors 10 -failureAnalysisFaults 15
```

Related Information

[-maxFailingVectors](#)

-failureLog

The **-failureLog** option specifies the failure log file or the list of failure log files for gateDiagnose to use for gate-level diagnosis.

Syntax

The following syntax specifies this option:

```
-failureLog <flogFileList>
```

where *flogFileList* is one or more valid operating system file names.

Default Value

None

Usage Conditions

At least one failure log file must be specified.

Example

In this example, gateDiagnose reads the *circuitA_1.flog* and the *circuitA_2.flog* failure log files to identify the most likely fault(s) that may be causing the failure.

```
gatediag circuitA -mode single -failureLog circuitA_1.flog circuitA_2.flog  
-lvdb circuitA.lvdb
```

Related Information

None

-hplOutput

The **-hplOutput** option specifies whether a diagnostic output file in HPL format is to be generated for each input failure log file.

Syntax

The following syntax specifies this option:

-hplOutput (*On*) / *Off*

where valid values are as follows:

- ***On***—instructs gateDiagnose to generate a diagnostic output file in HPL format for each input failure log file.
- ***Off***—specifies that no diagnostic output files are to be generated.

Default Value

The default value is *On*.

Usage Conditions

None

Example

In this example, gateDiagnose is instructed to generate a diagnostic output file in HPL format for each input failure log file.

```
gatediag circuitA -mode LogicBist -failureLog
circuitA.flog -lvdb circuitA.lvdb -log myGDiag.log
-hplOutput On
```

Related Information

None

-log

The **-log** option specifies the name of the log file generated by gateDiagnose.

Syntax

The following syntax specifies this option:

```
-log <logFileName>
```

where *logFileName* can be any valid operating system file name.

Default Value

The default file name is *gatediag.log*.

Usage Conditions

None

Example

In this example, gateDiagnose generates a log file explicitly named *myGDiag.log* in the current working directory.

```
gatediag circuitA -mode LogicBist -failureLog  
circuitA.flog -lvdb circuitA.lvdb -log myGDiag.log
```

Related Information

None

-lvdb

The **-lvdb** option specifies the path to the Mentor Graphics database of a chip or a core with embedded test.

Syntax

The following syntax specifies this option:

```
-lvdb <lvdbDirectoryName>
```

where *lvdbDirectoryName* can be any valid operating system directory name.

Default Value

None

Usage Conditions

This option must be specified. The specified mode must match the lvdb property of all failure log files.

Example

In this example, gateDiagnose performs gate level diagnose on failure data from the embedded core UNITA_COLLAR.

```
gatediag UNITA_COLLAR -mode Single -failureLog UNITA_COLLAR_BP0.flog -lvdb  
..../UNITA_COLLAR.lvdb
```

Related Information

[-failureLog](#)

-maxFailingVectors

The **-maxFailingVectors** option specifies the maximum number of failing vectors reported for a specific candidate fault. A vector is a failing vector for a candidate fault if the application of that vector results in observable fault-effects for the candidate fault. The number of candidate faults for which the failing vectors are reported is controlled by the **-failureAnalysisFaults** option.

Syntax

The following syntax specifies this option:

```
-maxFailingVectors <n>
```

where *n* is an integer specifying the maximum number of failing vectors to report for each candidate fault.

Default Value

The default value is 5.

Usage Conditions

None

Example

In this example, gateDiagnose reports up to a maximum of 8 failing vectors for the top 5 candidate faults.

```
gatediag circuitA -mode LogicBist -lvdb circuitA.lvdb -failureLog  
circuitA.flog -failureAnalysisFaults 5 -maxFailingVectors 8
```

Related Information

[-failureAnalysisFaults](#)

-minObservedSampleSize

The **-minSampleSize** option specifies the minimum number of samples with observed fault effects on the tester that must be analyzed before any faults can become eligible for fault dropping.

Syntax

The following syntax specifies this option:

-minSampleSize <n>

where *n* is an integer specifying the minimum sample size.

Default Value

The default value is *1*.

Usage Conditions

None

Example

The syntax in this example specifies to gateDiagnose the minimum number of samples with observed fault effects on the tester.

```
gatediag circuitA -lvdb circuitA.lvdb -failureLog circuitA.flog -mode
single -minSamplesize 12
```

Related Information

None

-minSampleSize

The **-minSampleSize** option specifies the minimum number of samples from which a metric of a candidate fault has been calculated before the fault is made eligible for fault dropping. A fault is dropped from further consideration when it is no longer considered as a likely culprit for the observed failures on the tester.

Syntax

The following syntax specifies this option:

```
-minSamplesize <n>
```

where *n* is an integer specifying the minimum sample size.

Default Value

The default value is *15*.

Usage Conditions

The **-minSampleSize** option is applicable only if the **-dropThreshold** option value is greater than *0*. A drop threshold value of *0* implies that no faults will be dropped.

Example

In this example, gateDiagnose drops candidate faults if the overall metric computed for the fault falls below the drop default threshold value and the sample size is at least *12*.

```
gatediag circuitA -lvdb circuitA.lvdb -failureLog circuitA.flog -mode
single -minSampleSize 12
```

Related Information

[-dropThreshold](#)

-mode

The **-mode** option identifies the test configuration for which the failures were observed.

Syntax

The following syntax specifies this option:

```
-mode Single | Multi | LogicBist | ControllerChain
```

where valid values are as follows:

- *Single*—specifies the single-chain scan-Thru-TAP configuration.
- *Multi*—specifies the multi-chain scan-Thru-TAP configuration.
- *LogicBist*—specifies the logicBIST configuration.
- *ControllerChain*—specifies the ControllerChain configuration.

Default Value

None

Usage Conditions

This option must be specified. The specified mode must match the mode property of all failure log files.

Example

In this example, gateDiagnose performs gate-level diagnose on failure data from logic BIST mode runs.

```
gatediag circuitA -mode LogicBist -failureLog circuitA.flog -lvdb
circuitA.lvdb
```

Related Information

[-failureLog](#)

-outDir

The **-outDir** option specifies the path to the directory where the log file and the diagnostic output files are saved.

Syntax

The following syntax specifies this option:

```
-outDir <outputDirectoryName>
```

where *outputDirectoryName* can be any valid operating system directory name.

Default Value

The current working directory.

Usage Conditions

The specified output directory must have the read, write, and execute file permissions. The *gatediag log* file is written out into the output directory unless the log filename is explicitly specified with a path name.

Example

In this example, *gateDiagnose* performs gate-level diagnose on the failure data and saves the results in the directory *outDir*.

```
gatediag UNITA_COLLAR -mode Single -failureLog UNITA_COLLAR_BP0.flog -lvdbs  
./UNITA_COLLAR.lvdb      -outDir outDir
```

Related Information

[-log](#)

-showAllRatios

The **-showAllRatios** option specifies whether all computed metric ratios are reported in the *.gdiag* file, which is generated by *gateDiagnose*.

Syntax

The following syntax specifies this option:

-showAllRatios *On* / (*Off*)

where valid values are as follows:

- *On*—specifies that the candidate faults for all ratios, *Overall*, *Match*, *Mismatch*, and *Excitation*, are reported in the *.gdiag* file.
- *Off*—specifies that only the overall probability candidate fault list is reported in the *.gdiag* file.

Default Value

The default value is *Off*.

Usage Conditions

None

Example

In this example, *gateDiagnose* performs gate-level diagnose on the failure data and reports all ratios.

```
gatediag circuitA -mode LogicBist -failureLog  
circuitA.flog -lvdb circuitA.lvdb -showAllRatios On
```

Related Information

None

-showEquivalentFaults

The **-showEquivalentFaults** option specifies the number of top candidate faults of each metric where all equivalent faults of the candidate are shown.

Syntax

The following syntax specifies this option:

```
-showEquivalentFaults <n>
```

where *n* is an integer specifying the number of candidate faults to show the equivalents.

Default Value

The default value is *10*.

Usage Conditions

The integer value specified for the **-showEquivalentFaults** must be greater than or equal to *0*.

Example

In this example, gateDiagnose will show the equivalent faults for the first *15* candidate faults for each computed metric.

```
gatediag circuitA -mode multi -lvdb circuitA.lvdb           -failureLog  
circuitA.flog -showEquivalentFaults 15
```

Related Information

None

-simFiles

The **-simFiles** option specifies the name of the file that contains all information to properly load the gate-level netlist into Verilog.

Syntax

The following syntax specifies this option:

```
-simFiles <simFileName>
```

where simFileName is a valid operating system file name.

Default Value

None

Usage Conditions

The following items are specified in the <simFileName>:

- Top-level netlist
- scan_shell files for all ELTs
- All **-y** and **-v** options to load libraries and library files
- Any other Verilog options necessary for properly loading the netlist For example, **+librescan**, **+libext**, **-f** to load an additional file with Verilog options.

Example

In this example, gateDiagnose uses the simFiles_gate file to load the gate-level netlist into Verilog.

```
gatediag circuitA -mode single -lvdb circuitA.lvdb
-failureLog circuitA.flog -simFiles simFiles_gate
```

Related Information

None

Chapter 6

Performing I/O, TAP, WTAP Tests and Diagnosis

This chapter provides step-by-step instructions on how to use the Tessent SiliconInsight software to direct embedded test resources on the DUT to perform production go/no-go and detailed diagnosis of device I/Os, TAP, and WTAPs.

Chapter topics follow this sequence:

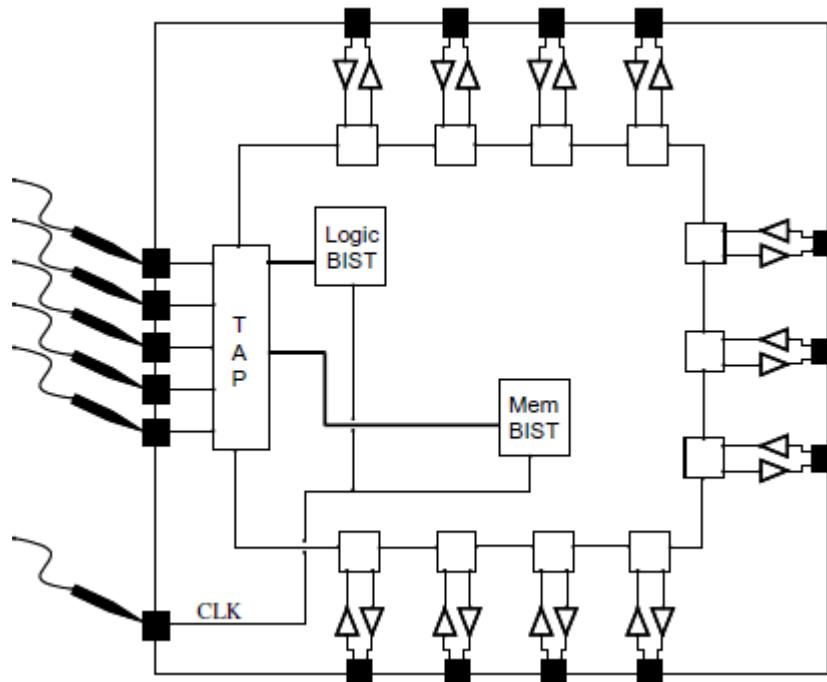
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Understanding Embedded I/O Testing

Testing high performance integrated circuits at wafer level is getting more complicated and expensive. As the frequencies increase, more unusual techniques must be employed to minimize signal coupling, wire inductance, and transmission line effects. The number of probes also is increasing and, as a result, so too are the capacitance and inductance between probes, the poor probe-to-pad contact, and the number of tester channels.

One way to address this increasing number of probes is to adopt a minimum pin count (MPC) testing approach. The goal in this approach is to have the tester physically probe the least number of device pins or pads as possible. This can be achieved using the embedded test architecture illustrated in [Figure 6-1](#). In this architecture, only the five TAP pins used to access the various embedded test controllers and one or more clock pins are contacted. The TAP interface also can be used to access an IEEE 1149.1 boundary-scan chain that provides direct access and control to the device I/O.

Figure 6-1. Minimum Pin Count Test Architecture



When a pad is bidirectional, the boundary-scan cell associated with the pad can be used to apply a structural test to the I/O region without requiring any probing of the pad. The local architecture is illustrated in [Figure 6-2](#).

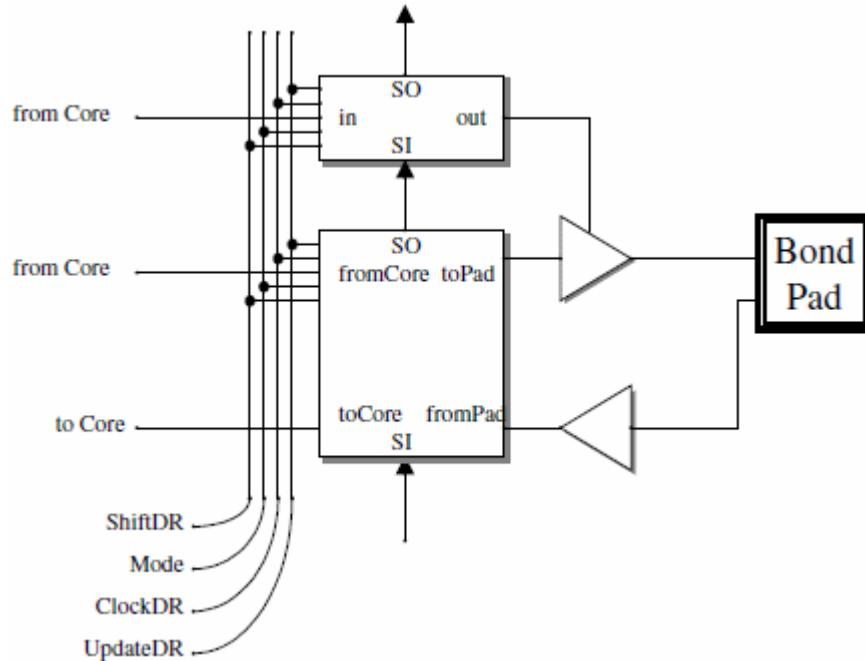
Testing Structural Faults

As the drive state of the I/O can be controlled through the boundary-scan register, the buffer functionality can be tested by loading the boundary-scan register with a known logic state, driving this state through the output buffer and capturing the resultant value in the corresponding boundary-scan register through the input buffer. This process is referred to as a *Pin Wrap* test. This test is designed to capture gross faults in the I/O region such as the following:

- Stuck-at 1 or 0
- Adjacent shorts
- Stuck open

- Non-functioning buffers

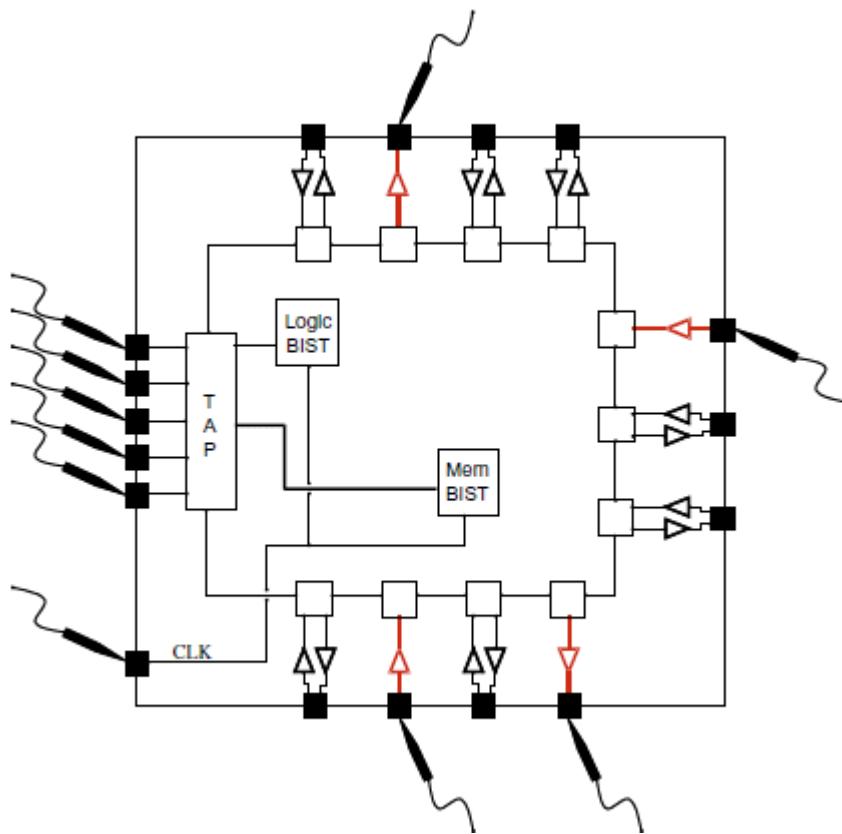
Figure 6-2. Pad with Boundary Scan and Pin Wrap



There are two approaches to deal with pads that are functionally unidirectional:

- The first approach is to simply make them bidirectional for test. That is, for output only pads, an input receiver is added while an output driver is added to input only pad cells. The additional receiver or driver can have a minimal configuration since it is not used functionally.
- If enhancing the unidirectional pad cells is not possible, a *mixed* approach can be used as depicted in [Figure 6-3](#). The bidirectional pads are tested using the *Pin Wrap* testing method while the remaining pads must be probed and tested by external equipment. There is still great value in the mixed approach. By reducing the number of pads that must be contacted, the approach allows devices with large pin counts to be tested on testers with fewer channels. Alternatively, probing less pads can also allow increasing the number of parallel sites. In both cases, test costs can be greatly reduced.

Figure 6-3. Mixed I/O test Approach



I/O Leakage Testing

To make an embedded I/O test more complete, the pin leakage must also be tested because pin leakage is very sensitive to parametric processing flaws that can affect reliability, and it is a common specified IC parameter. Leakage current that causes a pad voltage that is floating at logic 1 state to discharge to logic 0 is denoted IIH (current input high). Leakage current that causes a pad voltage that is floating at logic 0 state to charge to logic 1 is denoted IIL (current input low).

Pin leakages can be tested without any additional circuitry beyond what is needed for basic Pinwrap structural testing. Pins are first driven to a logic value, then tri-stated, and then their logic value is captured a precise time interval later. The time interval is calculated based on the pad's capacitance (typically 2~4 pF), the voltage difference between the pin's switching point voltage and the pin's initial logic value (typically 1~2V), and the pin's specified leakage current (typ. 1 µA). The typical time interval is 2~4 µs, but may be 10~50X longer for lower temperature tests where leakage current can be less than 50 nA.

The time interval is controlled by the TCK frequency and by the number of Run-Test/Idle (RTI) states between the TAP controller's Update-DR state (when the pins are tri-stated) and the Capture-DR state (when the pad's logic value is latched). This means that only pins that are tested with the same time interval can be tested simultaneously. A separate, independent I/O

Test Step is therefore needed for each pad cell type (since each will likely have different pad cell information).

Determining the time interval for the basic leakage test can be done by calculation and then verified in characterization of actual silicon, or by characterization and then verified by calculation.

To calculate the necessary time interval, the following equations are used:

The time interval $t_{LEAKTEST}$ is equal to $T_{TCK} * (2.5 + N_{RTI})$ where:

- T_{TCK} is the TCK clock period.
- N_{RTI} is the number of inserted RTI states.

If the captured value is equal to its pre-charged value, then

$$I_{IH} < C_{PADmin} * (V_{DD} - V_{SWmin}) / t_{LEAKTEST} \text{ or}$$

$$I_{IL} < C_{PAD} * (V_{SWmax} - V_{SS}) / t_{LEAKTEST}$$

where:

- C_{PADmin} is the estimated or minimum expected pad capacitance
- V_{SW} is the estimated or minimum/maximum expected input switching point voltage.

Tristate Enable Testing

If the enable signal that tristates a pin is stuck-on, then the embedded leakage test will always pass; the pad's voltage will stay at its pre-charged value. For this reason, a separate test is needed to verify that the enable is not stuck-on.

There are two separate paths leading to the tristate enable of each pin:

- The global forceDisable signal from the TAP
- The local signal supplied by an enable cell for a group of pins

For the test to be complete, each path must be tested separately.

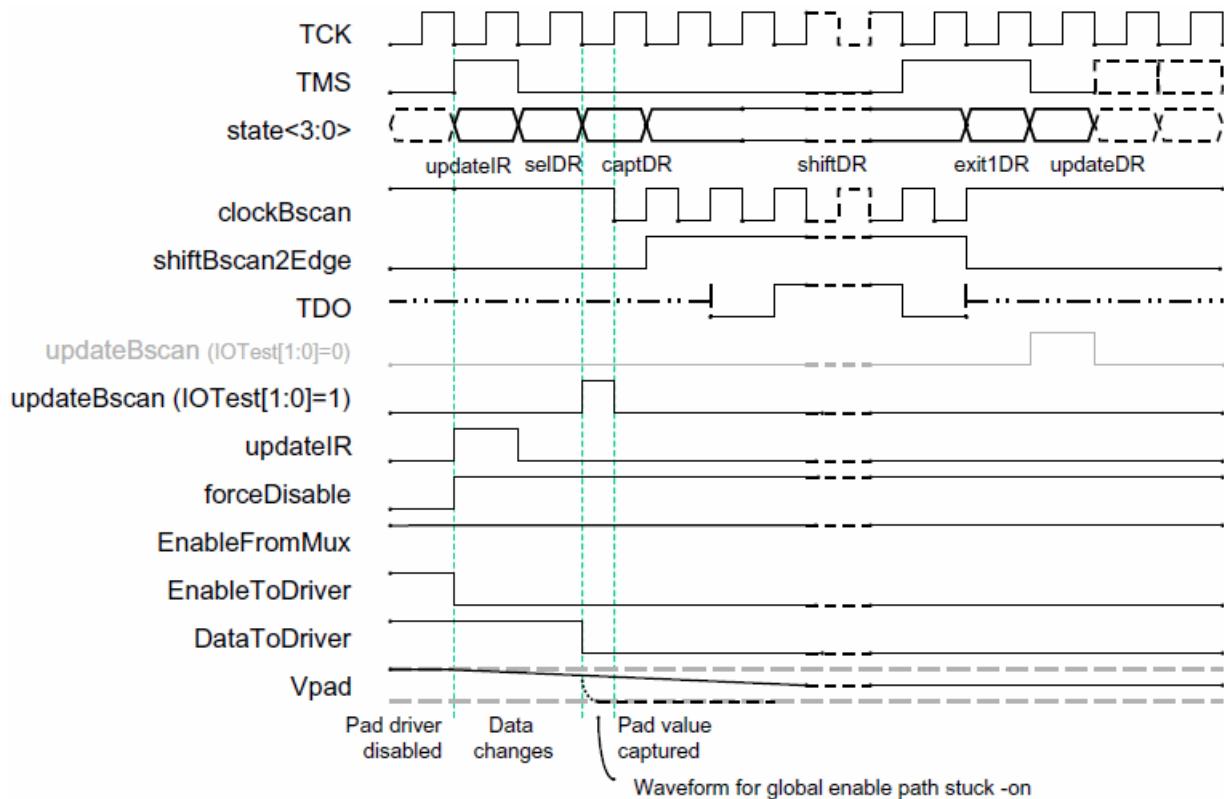
The test algorithm can be summarized as follows: Through the boundary scan, drive the pad high, then de-activate the tristate enable followed quickly by a change of the driver's input to logic low and then quickly capture logic state of pad. If the tristate enable is operating properly, then the final capture will be the initial high value applied. Otherwise, if the tristate enable is stuck at one, then the final capture value will be low and the test will fail. In the above discussion, "quickly" means it must be done before normal leakage ($1 \mu\text{A}$) discharges the pad.

The case when the tristate enable is stuck-off will be caught because this makes other tests fail, like the simple I/O wrap test.

Timing for Testing the forceDisable Path

The timing used to test the forceDisable path is shown in [Figure 6-4](#). When IOtest[1:0]=0, the updateBscan pulse occurs only during the updateDR state (if not suppressed), as shown by the grayed version of the *updateBscan* signal. When IOtest[1:0]=1, an updateBscan pulse is inserted during the captureDR state (starting one half TCK cycle before the capture edge, and ending at the capture edge). The minimum interval from updateIR (which causes forceDisable to be asserted) to captureDR is 2.5 TCK cycles, which is 2.5 μ s for a 1 MHz TCK clock rate. This test pattern (repeated for opposite data values) tests the forceDisable path to the enable input of the output drive.

Figure 6-4. TriState Enable Test Timing for forceDisable Path



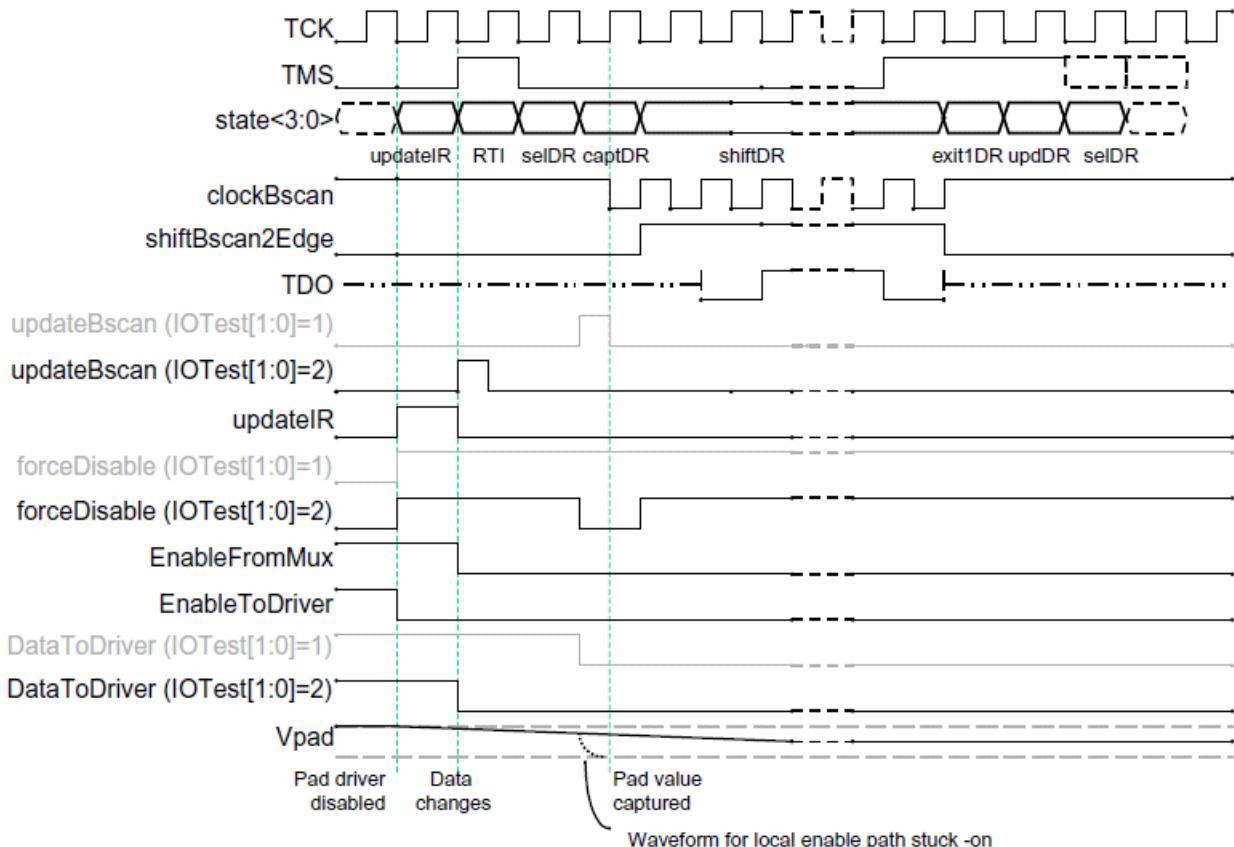
Timing for Testing the Path from the Enable Cell

To verify the enable path that originates at the boundary scan cell (*EnableFromMux*), a different timing and test pattern is needed, as shown in [Figure 6-5](#).

When IOtest[1:0]=2, the updateBscan pulse must occur earlier than for the preceding case – it occurs only during the RTI state – and the *forceDisable* signal is temporarily de-asserted during the capture-DR state to sensitize the Bscan bit enable path. This test timing and pattern

(repeated for opposite data values) tests the Bscan bit path to the enable input of the output driver. Much of this path is tested by other Bscan tests, however, the Mux-to-And gate input is uniquely tested by this sequence. The minimum interval from updateIR (which causes forceDisable to be asserted) to captureDR is 3.5 TCK cycles.

Figure 6-5. TriState Enable Test Timing for Enable Cell Path



Understanding WTAP Tests

The complexity of testing system-on-chip (SOC) technology continues to increase with new design methodologies, such as the partitioning of the chip into well-defined cores and blocks. To combat this issue, Mentor Graphics has developed a super set of the IEEE 1500 standard that allows Tessent SiliconInsight to use the distributed test access approach. This approach uses a localized instruction register and a set of supporting registers for test access and control. The localized instruction register terminates the connections of all embedded test controllers within the core to this register. The localized instruction register and associated circuitry form a wrapper test access port (WTAP).

As a mechanism to enable the use of the distributed test access with Mentor Graphics' tool suite, multiple WTAP controllers are inserted within cores and blocks of a design. The WTAP controllers are directly controlled by a chip-level JTAP controller. The instruction register of a

WTAP controller appears as a data register to the JTAP controller. At chip level, the WTAP instruction register is similar to a data register that selects the access of other data registers.

Because the WTAP controllers are not scan inserted, they must be tested with special WTAP tests. The available WTAP tests are as follows:

- [TestLogicReset Test](#)
- [InstReg Test](#)
- [BypassReg Test](#)
- [IDReg Test](#)

These tests are described in more detail below.

TestLogicReset Test

The *TestLogicReset* test verifies that the WTAP is being reset properly. The test consists of the following three phases:

- Phase A—shifts a non-default instruction in the Instruction Register and resets the WTAP forcing the JTAP to the state Test-Logic-reset.
- Phase B—verifies if the IDCode Register is present in the WTAP, that it is the Data Register selected after a reset.
- Phase C—resets the WTAP and verifies the content of the instruction register.

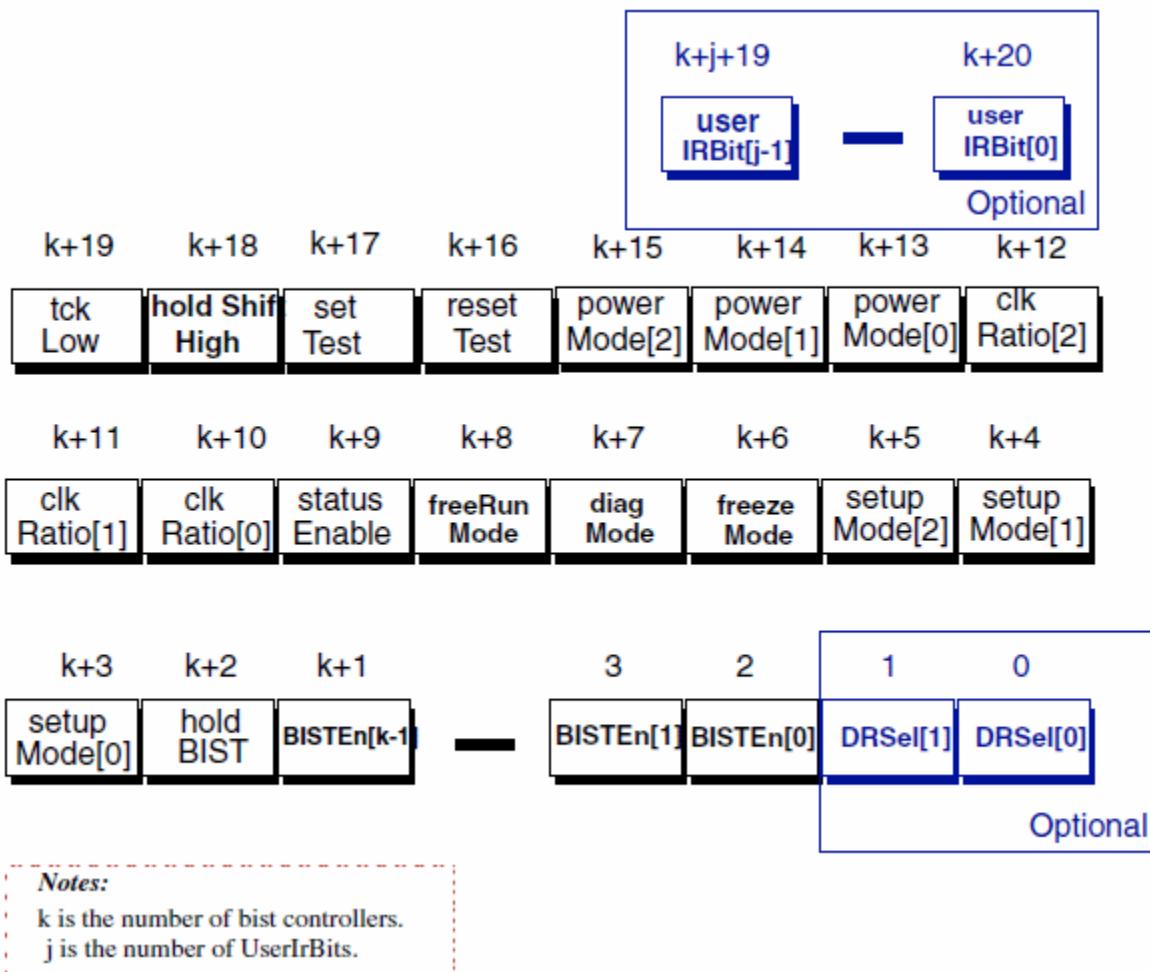
InstReg Test

The *InstReg* test verifies the functionality of the instruction register of the WTAP. The test consists of the following three phases:

- Phase A—verifies that the captured values by the 2 lsb of the instruction register are *01*.
- Phase B—verifies the functionality of the shift register inside the instruction register.
- Phase C—verifies the update flip-flops inside the instruction register capturing their values by de-asserting the instruction register *enableStatus* bit.

[Figure 6-6](#) illustrates how the WTAP instruction register bits are organized. Note that the instruction register is very similar to that of the JTAP instruction register bits.

Figure 6-6. WTAP Instruction Register Control Bit Assignments



BypassReg Test

The *BypassReg* test verifies the functionality of the bypass register of the WTAP controller. It consists of the following two phases:

- Phase A—verifies that the captured values of the bypass register is 0.
- Phase B—verifies operations of the bypass register by scanning a 11100 pattern through the bypass register and comparing with 01110.

IDReg Test

The *IDReg* test ensures that the ID register of the WTAP is responding properly and that it is automatically selected after a reset of the WTAP. It consists of the following two phases:

- Phase A—verifies that the IDCode captured and shifted out by the WTAP controller is the one specified in its BSDL description.

- Phase B—verifies that the shift register inside the IDCode register works properly.

Setting Up Embedded I/O Tests

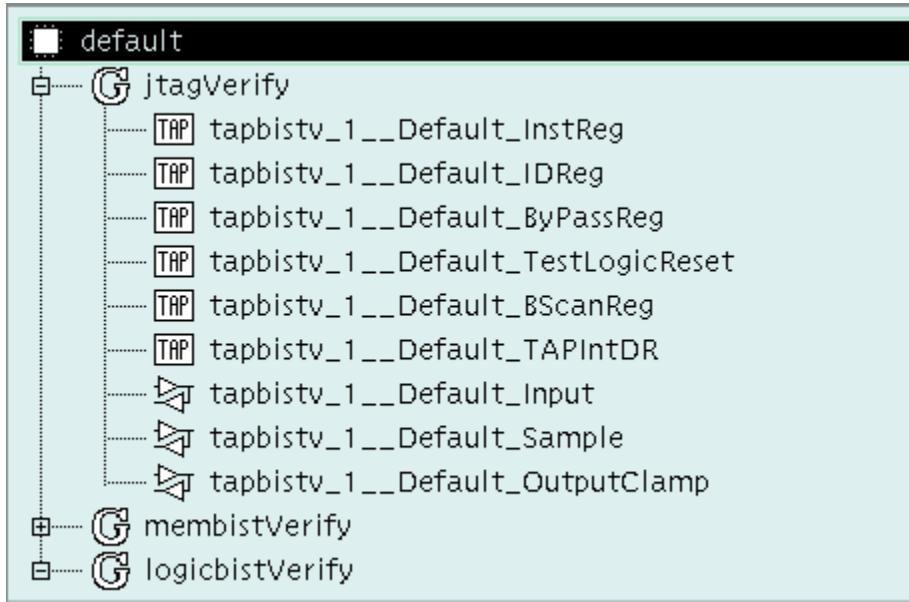
When you bring up the *default.config_eta* configuration file that is provided within the hand-off database (LVDB), all I/O tests are properly configured for execution by the design team. You can, however, change these tests by editing the test configuration from the Tessent SiliconInsight GUI. You also must ensure that information on which pins are contacted by the tester and what tester channel resources are available for each of the contacted pins is properly defined. This is accomplished using the pin map file.

Editing I/O Tests

To edit I/O tests from the Tessent SiliconInsight GUI, bring up the *ETDiagnostics* software as described in the section “[Invoking Tessent SiliconInsight](#)” if it is not already active.

Most of the available I/O related tests are included in a single test group in the *default.config_eta* file from the LVDB. As illustrated in [Figure 6-7](#), there are a total of nine TAP and I/O related tests. Six of these tests are aimed at testing the IEEE 1149.1 TAP and boundary-scan chain since these structures are used to apply the I/O tests. The TAP and boundary-scan chain also are used to test chip interconnect at the board level. Descriptions of the tests follow the figure.

Figure 6-7. TAP and I/O Tests



TAP and Boundary-Scan Tests

The six TAP and boundary-scan chain tests are as follows:

- *TestLogicReset*—verifies that the TAP is being properly reset. If the TRST pin exists, it causes a reset of the TAP controller. If there is a device ID register, which is the default data register selection, the device's ID is verified. If there is no device ID register, the test verifies that the BYPASS register can be scanned.

This test also performs a soft reset of the TAP by maintaining the TMS pin to one for 5 TCK cycles. The same verification of the ID or BYPASS registers is then performed.

- *IDReg*—ensures that the ID register is responding properly to the TAP data-register state machine. This test compares the capture values of the device ID and status registers whenever a data-register scan operation is performed. The test steps through all possible state transitions associated with a data register scan operation.
- *InstReg*—ensures that the instruction register can be loaded. The 01 least significant bits are checked on every instruction register scan operation. This test steps through all possible state transitions associated with an instruction register scan operation.

If the TAP does not track states of the finite state machine properly (FSM), the standard 01 bits of the instruction register do not appear in a subsequent IR operation.

- *BypassReg*—ensures that the data-register state machine is functioning properly and that the bypass register can be loaded. This test scans through the bypass register each time, comparing the bypass register capture value to 0. The algorithm also steps through all possible state transitions associated with a data register scan operation.

If the TAP does not track states of the finite state machine properly (FSM) properly, a 1-bit delay does not appear in subsequent data- register scan operations. The test performs a final check of the bypass operation codes by scanning a *11111* pattern through the bypass register using every operation code.

- *BScanReg*—ensures the boundary-scan data register responds properly to the TAP state machine and that the boundary-scan register can be loaded. This test uses the *SAMPLE* instruction, shifting data through the boundary scan chain only. Testing whether the boundary-scan chain can actually capture and update data to the pins is performed as part of the *Input* and *Output* tests and therefore is not included as part of this test.
- *TAPIntDR*—ensures that the TAP's internal user data register is responding properly to the TAP register state machine. The test also ensures that values can be flushed through the register.

I/O Tests

It is advisable to always perform the TAP tests before testing the I/Os themselves.

The I/O tests are as follows:

- *Input*—performs a test on all contacted input and bidirectional pins using standard IEEE 1149.1 timing. For contacted pins, the test verifies that the boundary scan cells perform a proper capture of input data sourced by the tester.

- Sample—checks that the boundary scan cells perform a proper capture of input data sourced from the tester. This test is similar to the *Input* test, with the exception that it does not include bidirectional pins. This test also uses the *SAMPLE* instruction instead of the *EXTEST* instruction.
- OutputClamp—adds clamping to the *Output* test. For each pattern during the *Output* test, after the output and bidirectional pins are strobed, the CLAMP instruction is scanned into the TAP and the outputs are then strobed again with the Bypass register selected to verify that all output values have been retained.

Leakage Tests

These I/O tests are used for testing leakage:

- *LeakageNC*—tests the leakage current of uncontacted pins. Both input leakage high (I_{IH}) and input leakage low (I_{IL}) tests are performed. The leakage test operates by driving each pin to a logic value, then tri-stating the pin, and then capturing the resulting logic value after a precise time interval.
- *TriStateEnableNC*—tests that three state output drivers can be placed in the high-impedance state.

As illustrated in [Figure 6-7](#), each TAP or I/O test is contained within a separate test step. The TAP and I/O tests are represented by the **Test Step** icons shown in [Figure 6-8](#).

Figure 6-8. TAP and I/O Test Step Icons

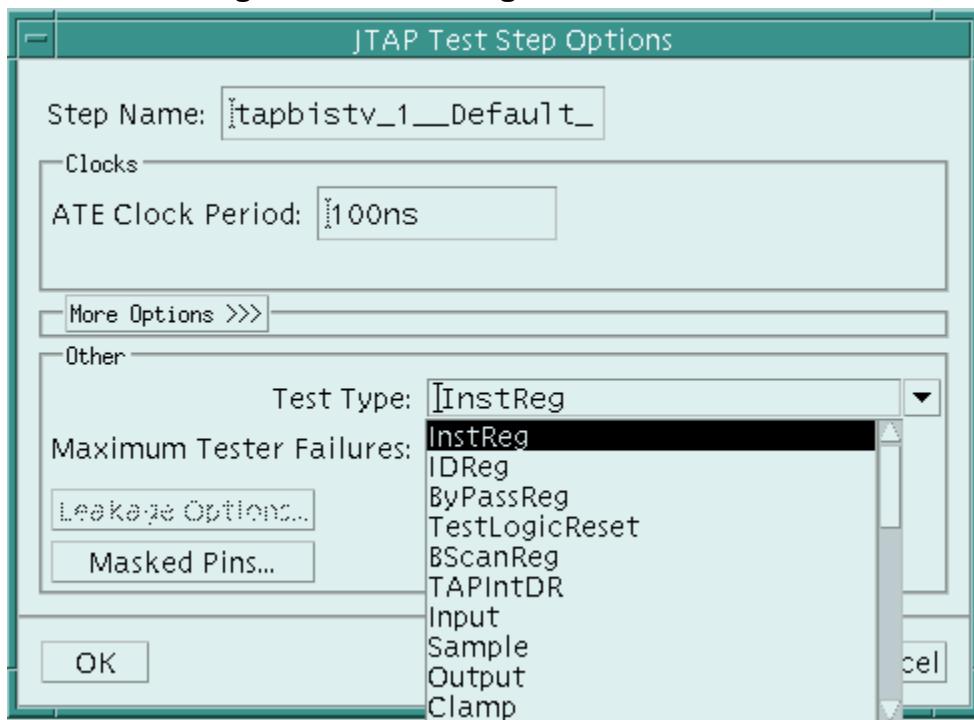


Changing Tests

To change a test for a given test step, perform the following steps:

1. Right mouse button click on the *Test Step* icon of interest and choose **Options** to bring up the **TAP I/O Test Step Options** menu.
2. Click on the **Test Type** cascade button in the **Other** section of the menu and choose the desired test, as illustrated in [Figure 6-9](#).
3. Edit the name of the *Test Step* in the **Step Name** field at the top of the menu to reflect the type of test being performed.
4. Click on the **OK** button to close the **TAP I/O Test Step Options** menu and accept your changes.

Figure 6-9. Selecting a TAP or I/O Test



Setting Up WTAP Tests

When the *default.config_eta* configuration file, provided within the hand-off database (LVDB) and containing WTAP controllers, is brought up, all required WTAP tests are properly configured for execution by the design team. These WTAP tests are grouped under **WtapVerify** as illustrated in Figure 6-10.

Figure 6-10. Default WTAP Tests



A WTAP test step can contain no more than one WTAP controller. Consequently, there are as many WTAP test steps as there are WTAP controllers in the design. The optional *IDReg* and

BypassReg tests are present only if the corresponding registers are present in the WTAP controller. The icons used for this type of test are illustrated in [Figure 6-11](#).

The WTAP tests are similar to the TAP tests. For a description of the WTAP tests, refer to the section “[Understanding WTAP Tests](#).”

Figure 6-11. WTAP Step, Controller, and Test Icons



Executing TAP and Embedded I/O Tests

From the Tessent SiliconInsight GUI, you can execute a single test step, an entire test group, or an entire test configuration by clicking on the associated icon in the **Test Configuration** area and then clicking on the **Execute** (lightning bolt) icon in the tools bar.

An example output from the **Console** area appears as illustrated in [Figure 6-12](#).

Figure 6-12. Sample Passing TAP Test Result

```
LVDB Directory:  
/rd/test/4.1/embeddedTest4.1PreProd-024/support/ETA/examples/eta_demochip/demo_chip_eate.lvdb  
LVDB Name: demo_chip_eate.lvdb  
Test Config: LVBIST1A_TC1  
TestStep: IDReg (PASSED)  
Execution Time Stamp: 09/06/03 14:25:21  
(tck, 100ns)  
=====
```

You can execute all TAP and I/O tests in the **IO** test group by clicking on the **Test Group** icon and then clicking on the **Execute** button. The results of all eleven tests is then displayed in the **Console** area. [Figure 6-13](#) illustrates a sample output that includes a failing result for the *Input* I/O test. A failing I/O test always provides the failing pin names as well as the expected and actual values driven or received. For example, the *Input* test shown in [Figure 6-13](#) detected errors on pins *IN4* and *IN6*. Both pins appear to be stuck at 1.

Figure 6-13. Sample Failing I/O Test

```

Input test failed
Test identified two failing pins

(tck, 100ns)
TestStep: Input (FAILED)
Execution Time Stamp: 09/06/03 14:27:40
(tck, 100ns)
Boundary scan pin "IN6" failed IOtest "Input". Actual value is "1" (expected "0").
Boundary scan pin "IN4" failed IOtest "Input". Actual value is "1" (expected "0").
TestStep: Sample (PASSED)
Execution Time Stamp: 09/06/03 14:27:40
(tck, 100ns)
TestStep: Output (PASSED)
Execution Time Stamp: 09/06/03 14:27:40
(tck, 100ns)
TestStep: Clamp (PASSED)
Execution Time Stamp: 09/06/03 14:27:40
(tck, 100ns)
TestStep: OutputClamp (PASSED)
Execution Time Stamp: 09/06/03 14:27:40

```

Executing Selected I/O Tests

There are two ways to execute only a subset of the available TAP and I/O tests.

- Place the desired subset into its own test group. This approach requires editing of the test configuration. This approach is useful if you plan to regularly execute the given subset.
- Maintain all tests in a single group and selectively enable the tests to be executed at any given time. If the subset of interest is likely change over time, this is a better approach.

For an example, assume you only want to execute the *OutputClamp* and *Sample* tests in the **IO** test group of the *LVBIST1A_TC1* configuration. You need to disable each of the other seven tests. To do this, right mouse button click on each of the associated nine **Test Step** icons and choose the **Execute Enable** item from the resulting pop-up menu. This toggles the execution enable status of these seven tests to off. When a test step is disabled, it is greyed out in the **Test Configuration** window.

Once you are done disabling the seven tests, the **Test Configuration** window appears as illustrated in [Figure 6-14](#). Now, when you execute the **IO** test group, only the two tests that have not been disabled are executed.

Figure 6-14. Disabled TAP and I/O Tests

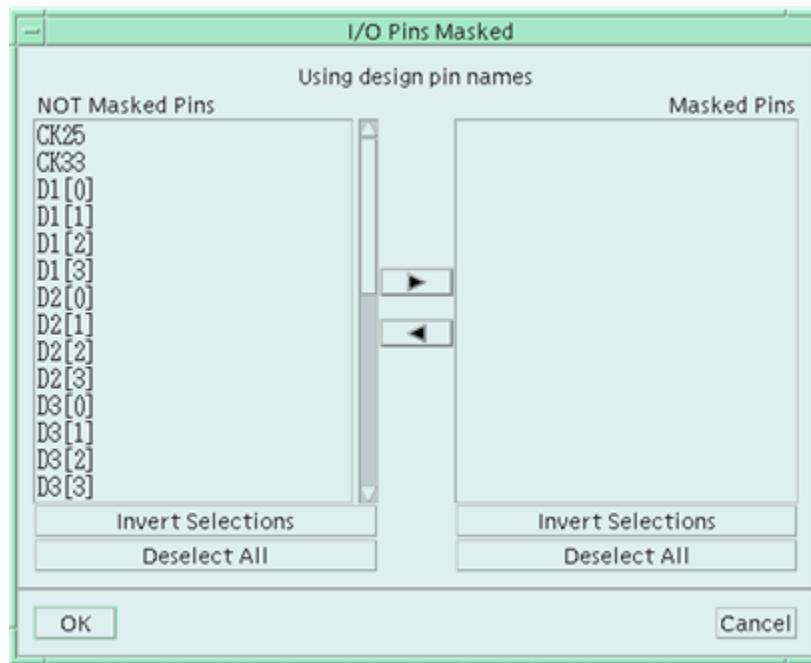


Masking Pins

When executing I/O tests, you might occasionally want to mask out the test results of certain pins. The Tessent SiliconInsight GUI allows you to mask pins on a per test steps basis. To mask one or more pins within a test step, perform the following steps:

1. Right mouse button click on the **Test Step** icon and choose **Options** to bring up the **TAP I/O Test Step Options** menu.
2. Click on the **Masked Pins** button in the **Other** section of the menu to bring up the **I/O Pins Masked** window as illustrated in [Figure 6-15](#).

Figure 6-15. I/O Pins Masked Window



3. Select the **NOT Masked Pins** scroll window on the left to mask a pin and click on the right arrow (->) button. This places the pin name into the *Masked Pins* scroll window on the right. Repeat this process for each pin you want to mask.

To unmask a pin, select it in the **Masked Pins** scroll window and click on the left arrow (<-) button.

To move a contiguous set of pins from one scroll window to the other, click on the first pin of interest in the list and then shift click on the last pin in the group to select the whole group. Click on the appropriate arrow button to then move the pins.

A **Select All** button is also provided to select all pins within a given scroll window. This is useful for moving a majority of the pins from one scroll window to the next. First select and move all the pins and then move back those pins that you do not want to move.

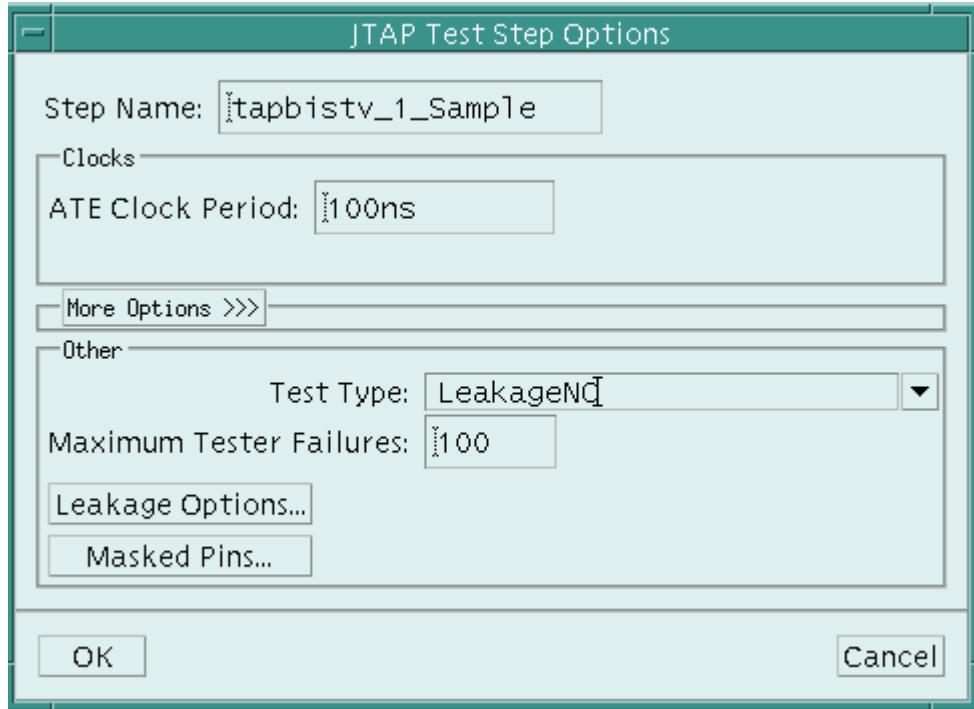
Executing a Leakage Test

Mentor Graphics supports performing an I/O leakage test on pins that satisfy the following conditions:

- The pin must not be contacted to an ATE channel (specified in the pin map file).
- The pin must be a bi-directional pin
- The pin must not be masked (specified in the I/O test step options window)

To perform an I/O leakage test, you must first create a new test step or edit an existing test step and set the **Test Type** to *LeakageNC* in the **TAP I/O Test Step** options panel as shown in [Figure 6-16](#).

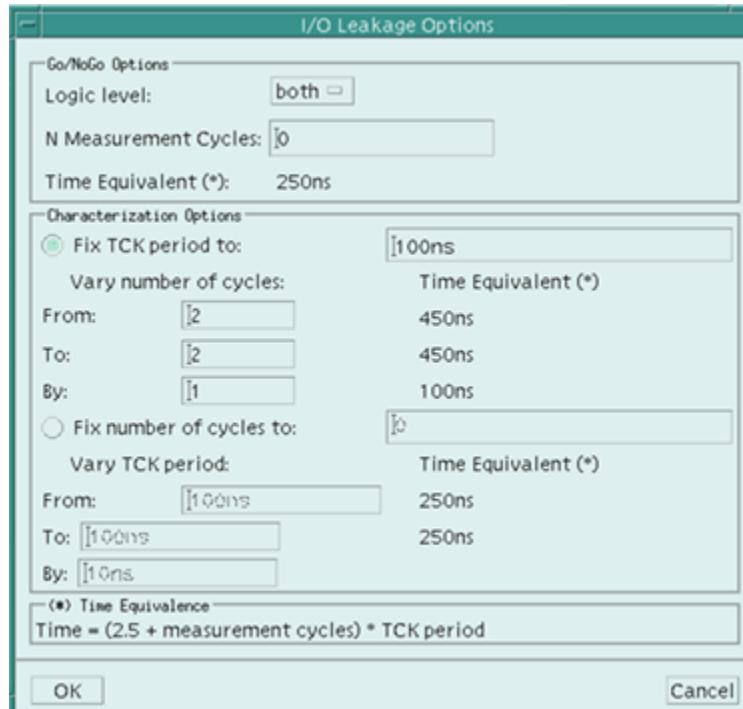
Figure 6-16. Setting Test Type to Leakage



Next, click on the **Leakage Options** button to bring up the **I/O Leakage Options** panel as shown in [Figure 6-17](#). From the **Go/No-Go Options** section you can specify the following parameters:

- **Logic Level:** specifies the type of leakage test to perform. Supported options are *IIL*, *IIH* or *Both*. Typically, you set this to *Both*.
- **N Measurement Cycles:** specifies the number of extra TCK cycles to add before the return capture is performed. The overall time interval that results from this setting is provided by the **Time Equivalent** field in the panel.

Figure 6-17. Setting Up A Leakage Test



Once the above parameters are set, click on the **OK** button to close the **I/O Leakage Options** panel and accept the settings. Click on the **Execute** button to execute the leakage test.

Performing Leakage Characterization

The Tessent SiliconInsight GUI supports shmooring of the wait time (and hence leakage current threshold) for characterization purposes. To perform a shmoos, click on the **Leakage Options** button in the **TAP I/O Test Step** options panel to bring up the **I/O Leakage Options** panel. As can be seen from the **Characterization Options** section of the panel, shmooring can be performed by either holding the TCK period fixed and varying the number of extra TCK cycles, or by holding the number of extra TCK cycles fixed and varying the TCK period.

To shmoos using a fixed TCK period, click on the **Fix TCK period to:** option and set the desired period value (refer to [Figure 6-17](#)). Next, in the **Vary number of cycles** section, set the range of extra cycles to use including the cycle increment. Click **OK** to close the **I/O Leakage Options** panel and then click on the **Diagnose** button to perform the characterization.

A sample characterization result using a fixed TCK period shmoos is shown in [Figure 6-18](#). For each tested pin, the second column in the datalog (labeled *1st Failure Cycle*) displays the first cycle at which the leakage test fails, while the fourth column (labeled *1st Failure Real Time*) displays the actual time interval at which the leakage test fails. For example, in [Figure 6-18](#), pin D2[0] first fails on cycle 8 or when a wait time interval of 1.05 us is reached.

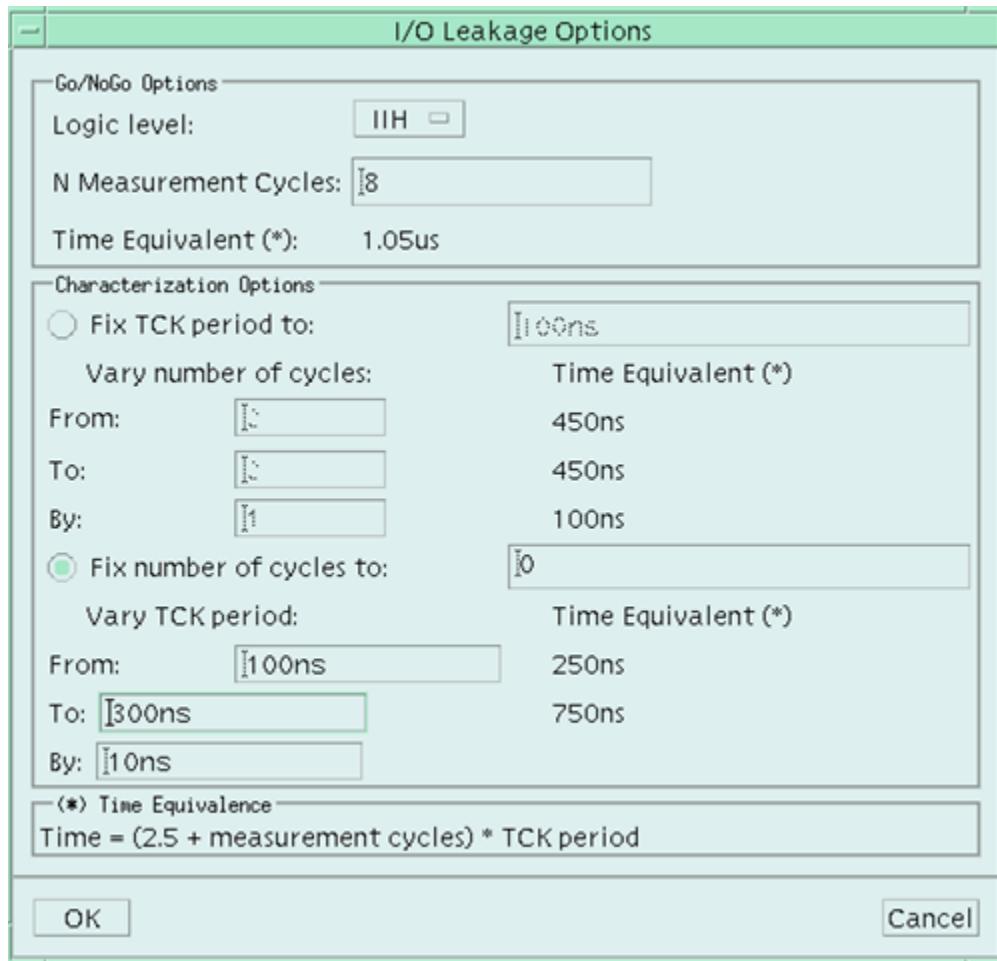
Figure 6-18. Sample Fixed Period Leakage Characterization

Logic Level: IIH
Characterization mode: FixedTCK
Target pins: Uncontacted Pins
TCK period: 100ns
Measurement Cycles: from 7 to 9 by 1

Leakage results:

Pin Name	1st Failure Cycle	1st Failure TCK period	1st Failure Real Time
D1[0]	7	100ns	950 ns
D1[1]	7	100ns	950 ns
D1[2]	7	100ns	950 ns
D1[3]	7	100ns	950 ns
D2[0]	8	100ns	1.05 us
D2[1]	8	100ns	1.05 us
D2[2]	8	100ns	1.05 us
D2[3]	8	100ns	1.05 us
DIFF_BIDI[0]	8	100ns	1.05 us
DIFF_BIDI[1]	8	100ns	1.05 us
DIFF_BIDI[2]	8	100ns	1.05 us

To shmoos using a fixed number of TCK cycles, click on the **Fix number of cycles to:** option and set the desired number of extra TCK cycles (see [Figure 6-19](#)). Next, in the **Vary TCK period** section, set the TCK period range to use including the period increment. Click **OK** to close the **I/O Leakage Options** panel and then click on the **Diagnose** button to perform the characterization.

Figure 6-19. Setting Up Fixed Cycles Leakage Characterization

A sample characterization result using a fixed number of TCK cycles shmoo is shown in [Figure 6-20](#). For each tested pin, the third column in the datalog (labeled *1st Failure TCK period*) displays the first period value at which the leakage test fails, while the fourth column (labeled *1st Failure Real Time*) displays the actual time interval at which the leakage test fails. For example, in [Figure 6-20](#), pin D2[0] first fails when a TCK period of 122.4 ns is reached or equivalently, when a wait time interval of 1.163 us is reached.

Figure 6-20. Sample Fixed Cycles Leakage Characterization

Logic Level: IIH
Characterization mode: FixedNumberOfCycles
Target pins: Uncontacted Pins
TCK period: from 100ns to 150ns by 22.4ns
Measurement Cycles: 7

Leakage results:

Pin Name	1st Failure Cycle	1st Failure TCK period	1st Failure Real Time
D1[0]	7	100ns	950 ns
D1[1]	7	100ns	950 ns
D1[2]	7	100ns	950 ns
D1[3]	7	100ns	950 ns
D2[0]	7	122.4ns	1.163 us
D2[1]	7	122.4ns	1.163 us
D2[2]	7	122.4ns	1.163 us
D2[3]	7	122.4ns	1.163 us
DIFF_BIDI[0]	7	122.4ns	1.163 us
DIFF_BIDI[1]	7	122.4ns	1.163 us

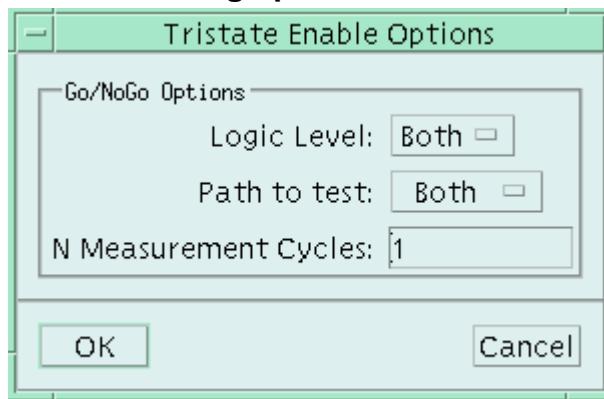
Executing a TriStateEnable Test

To perform a *TriStateEnable* test, you must first create a new test step or edit an existing test step and set the **Test Type to TriStateEnable** in the **TAP I/O Test Step** options panel.

Next, click on the **TriStateEnableNC Options** button to bring up the **Tristate Enable Options** panel as shown in [Figure 6-21](#). From this panel you can specify the following parameters:

- **Logic Level:** specifies the logic level to be driven to the tristate output driver during the test. Supported options are *Low*, *High*, or *Both*. You should typically set this to *Both*.
- **N Measurement Cycles:** specifies the number of extra TCK cycles that are to be added between the time the driver is disabled and driven to the opposite value and the time when the original value is read back. Normally, this value is set to *1*.
- **Path to test:** indicates which control path leading to the tristate enable of each pin driver is to be tested. Available options are *Local* (the local signal supplied by an enable cell for a group of pins), *Global* (the global *forceDisable* signal from the TAP) or *Both*. Typically, this is set to *Both*.

Figure 6-21. Setting up a TriStateEnableNC Test



Once the above parameters are set, click on the **OK** button to close the **Tristate Enable Options** panel and accept the settings. Click on the **Execute** button to execute the *TriStateEnable* test.

[Figure 6-22](#) shows sample failure results. In this case, the Console displays the pins that have failed the test.

Figure 6-22. Sample TriStateEnableNC Test Results

```
Pins failing I/O test TriStateEnable (local test path) with
pin precharged LOW:
    D3(3) (on-chip pull-up    not detected)
Pins failing I/O test TriStateEnable (local test path) with
pin precharged HIGH [precharge phase]:
    DIFF_BIDI(0)
    DIFF_BIDI(1)
    DIFF_BIDI(2)
    DIFF_BIDI(3)
    D3(0)
    D3(1)
    D3(2)
    D3(3)
    D2(0)
    D2(1)
    D2(2)
    D2(3)
Pins failing I/O test TriStateEnable (local test path) with
pin precharged HIGH:
    DIFF_BIDI(0)
    DIFF_BIDI(1)
    DIFF_BIDI(2)
    DIFF_BIDI(3)
    D3(3) (on-chip pull-up    not detected)
    D2(0)
```

Executing WTAP Tests

To execute a WTAP test step, click on the associated WTAP controller or WTAP test step icon in the **Test Configuration** area and then click on the **Execute** icon in the **Tools** bar. The results of the chosen tests are displayed in the **Console** area. For example, in [Figure 6-23](#) and [Figure 6-24](#), a stuck-at-one fault in the ID shift register caused failures in the *IDReg* and *TestLogicReset* tests.

You cannot click on an individual WTAP test under the WTAP controller to execute that test. If you do not want to execute a WTAP test, remove the test from the test step.

Figure 6-23. Passed and Failed WTAP Tests

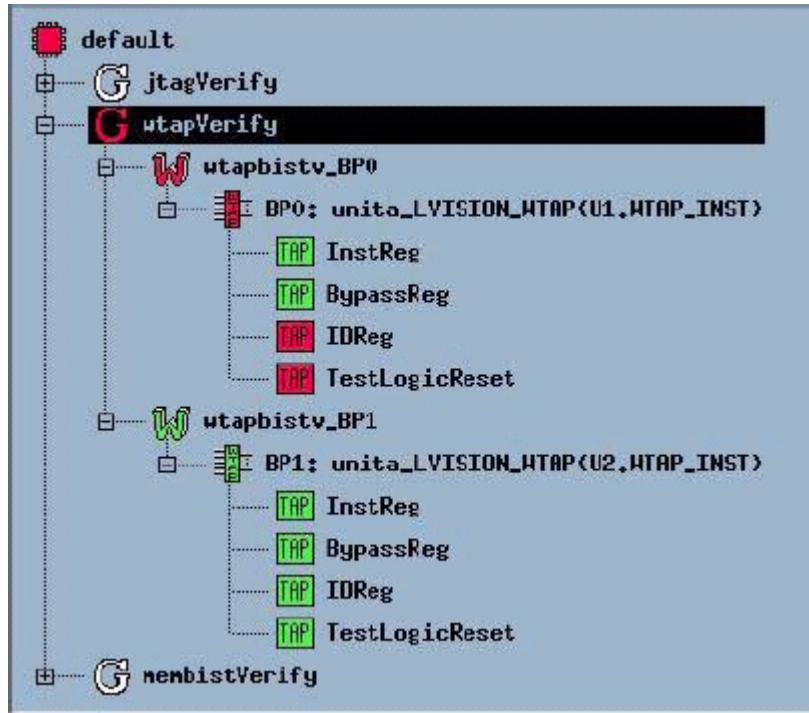


Figure 6-24. Example of Console for Failing WTAP Test

```
LVDB Directory:  
/vol02/qa/users/dcrepeau/p1500/p1500_test_cases/wtaphw_test_4.2/wtaphw_test/tsuite1/chipa2np/chipa.lvdb  
LVDB Name: chipa.lvdb  
Test Config: default  
  
TestGroup: wtapVerify  
TestStep: wtapbistv_BP0 (FAILED)  
Execution Time Stamp: 06/30/04 16:52:47  
WTAPController "BP0" {tck, 100ns}  
==> WTAP Test "IDREG" has failed.  
    ***Warning***: IDREG WTAP Test failed. LVDB and Device Under Test are possibly not  
correlated. All results from this DUT may be invalid. Compare mismatch on Register "BP0_WDR.DEVICE_ID".  
Actual 32-bit value is "0x000320ed" (expected "0x154320ed").  
    ***Warning***: IDREG WTAP Test failed. LVDB and Device Under Test are possibly not  
correlated. All results from this DUT may be invalid. Compare mismatch on Register "BP0_WDR.DEVICE_ID".  
Actual 32-bit value is "0x00000000" (expected "0x00000001").  
    ***Warning***: IDREG WTAP Test failed. LVDB and Device Under Test are possibly not  
correlated. All results from this DUT may be invalid. Compare mismatch on Register "BP0_WDR.DEVICE_ID".  
Actual 32-bit value is "0x00000000" (expected "0xffffffff").  
==> WTAP Test "TESTLOGICRESET" has failed.  
    Compare mismatch on Register "BP0_WDR.DEVICE_ID". Actual 32-bit value is "0x000320ed"  
(expected "0x154320ed").  
TestStep: wtapbistv_BP1 (PASSED)  
Execution Time Stamp: 06/30/04 16:52:47  
WTAPController "BP1" {tck, 100ns}  
=====
```


Chapter 7

Diagnosing and Validating Memory With Enhanced Stop-On-Nth-Error Test Patterns

The *Tessent MemoryBIST User's and Reference Manual* describes how to equip your memory BIST controller (MBIST) with the Stop-On-Nth-Error (SOE) memory diagnostic capability that includes a failure limit counter. The failure limit counter tracks the failure limit value and eliminates the need to generate multiple test patterns to capture multiple failures.

Note

 For purposes of this chapter, SOE with the addition of a failure limit counter is referred to as enhanced Stop-On-Nth-Error (ESOE). Refer to section “[Creating Stop-On-Nth-Error Test Benches for Bitmap Applications](#)” in the *Tessent MemoryBIST User's and Reference Manual* for more information.

This chapter describes how to generate ESOE test patterns, collect the failing cycle data, and convert the failure log files into JSON format suitable for diagnostic purposes.

In addition to diagnosing ESOE patterns, this chapter describes how to validate ESOE test diagnostic patterns in a simulated environment by using the Tessent SiliconInsight SimDUT tool and the ModelSim or Questa Verilog Simulator. This tool allows you to validate patterns before you tape-out or receive the silicon prototype.

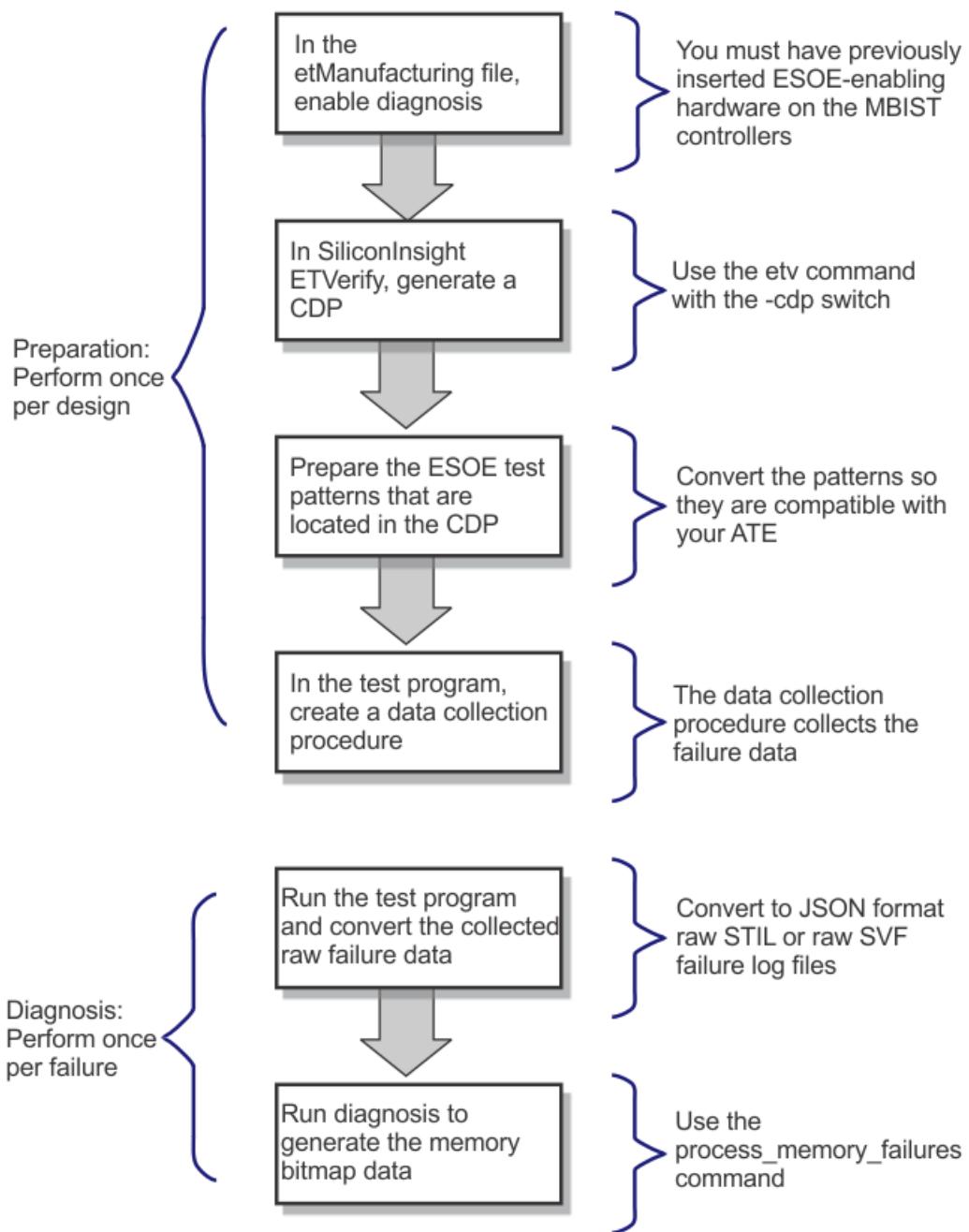
Chapter topics follow this sequence:

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Diagnosing Memory with ESOE Test Patterns

[Figure 7-1](#) shows the high-level flow for diagnosis memory with ESOE test patterns.

Figure 7-1. High-Level Flow for Diagnosing Memory with ESOE Test Patterns



Related Topics

[Generating a CDP That Contains ESOE Test Patterns](#)

[Preparing the Test Patterns and the Test Program](#)

[Collecting and Converting the Failure Data](#)

[Running Diagnosis to Generate Diagnostic Bitmap Files](#)

Generating a CDP That Contains ESOE Test Patterns

The Characterization and Debug Package (CDP) contains test patterns and mapping information that is used to map raw failure data to memory bitmaps.

The process described in this section requires you to make changes to your etManufacturing file. For details about the etManufacturing file, refer to [ETVerify Tool Reference](#).

Prerequisites

- You have inserted the required ESOE-enabling hardware into the MBIST controller as described in “[Creating Stop-On-Nth-Error Test Benches for Bitmap Applications](#)” in the *Tessent MemoryBIST User’s and Reference Manual*.

Procedure

1. In the ETVerify etManufacturing file, set the CompareGoID property to “on” as shown in [Example 7-1](#). The example shows that you have enabled diagnosis for the three controllers associated with the test named “membistpv_1.”

Example 7-1. etManufacturing File Enabled for ESOE Diagnosis

```
membistPVerify(1) { // {{{
    PatternName           : membistpv_1;
    TestClockSource      : Functional;
    ClockPeriod          : 10000ns;
    TckRatio             : 16;

    TestStep ( Default ) {
        ETATestGroupName       : membistPVerify;
        RunMode                : RunTimeProg;
        Controller ( BP2.WBP1 ) { // PCI_PCI_CLOCK_A_MBIST1_MBISTPG_CTRL
            ETAProperties {
                MaxFailsPerCtrlStep : 100;
            }
            CompareGoID          : On;
        }
        Controller ( BP3.WBP1 ) { // PCI_PCI_CLOCK_A_MBIST1_MBISTPG_CTRL
            ETAProperties {
                MaxFailsPerCtrlStep : 200;
            }
            CompareGoID          : On;
        }
        Controller ( BP4.WBP1 ) { // USB_USB_CLOCK_A_MBIST1_MBISTPG_CTRL
            ETAProperties {
                MaxFailsPerCtrlStep : 50;
            }
            CompareGoID          : On;
        }
    }
} // }}}}
```

Set the CompareGoID property for all the controllers on which you want to run diagnosis. The tool automatically generates ESOE patterns for controllers with inserted ESOE hardware. Otherwise, the tool generates non-enhanced Stop-On-Nth-Error patterns.

In the context of ESOE, the MaxFailsPerCtrlStep property within the ETAProperties wrapper defines the maximum number of failures you want to collect in the controller. If multiple controllers are defined, the highest MaxFailsPerCtrlStep property value will be used for all failing controllers being diagnosed in parallel.

2. Invoking ETVerify, generate the CDP from an existing LVDB. For example:

```
etv top -inputLVDBName TOP.lvdb -configFile TOP.etManufacturing \
-cdp stil
```

The -cdp switch supports STIL and SVF pattern formats. This switch is required for the process described in this chapter. In this example, the command creates a top.cdp file.

Refer to “[ETVerify Runtime Options](#)” in the *ETVerify Tool Reference* for details about the etv command and other options you can use.

Results

ETVerify generates a CDP named *design_name.cdp* at the same directory level as your LVDB. In the previous example, this would be the top.cdp directory.

Preparing the Test Patterns and the Test Program

After generating a CDP that contains your ESOE test patterns, you need to prepare the test patterns and the test program.

Prerequisites

- You have generated a CDP that contains ESOE test patterns as described in “[Generating a CDP That Contains ESOE Test Patterns](#).”

Procedure

1. Locate the ESOE test patterns located within the directory structure that ETVerify generated. The path is:

```
design_name.cdp/PPDIR/patterns/*.<stil | svf>
```

2. Use your pattern translator to convert the patterns to the format supported by your ATE.

Ensure that there is a one-to-one mapping between the STIL pattern cycle counts and the vector cycles of the translated ATE format. This will simplify reporting of failing cycles in terms of the STIL pattern file.

3. In the test program, for each MBIST wrapper configuration in the etManufacturing file, implement a data collection procedure that will collect the failing cycle data.

Each data collection procedure consists of the following three patterns:

- Initialize (IP0): Set the initial failure limit counter value (typically 0) and execute once.
- Execute (EP0): Run the ESOE pattern. Load the failure limit in the counter, perform the test, and scan out any failure data.
- Increment (NP0): Increment the failure limit counter.

The Execute and Increment patterns iterate until the tool reaches the maximum number of ESOE failures or until the Execute pattern stops failing.

Each wrapper may contain multiple controllers. For example, suppose you have two controllers in WrapperA and one controller in WrapperB. You would still implement one data collection procedure for WrapperA and one for WrapperB, for a total of six patterns: two each for IP0, EP0, and NP0.

[Example 7-2](#) shows a pseudo data collection procedure.

Example 7-2. Data Collection Procedure

```
// Initialize pattern
execute_pattern( DLV_IP0_membistpv_1.stil )

// Exit the loop if the next test pattern passes
loop = 0
status = fail
while (status == fail and loop < MaxLoop) {

    // Execute pattern
    status = execute_and_get_failing_cycles( DLV_EP0_membistpv_1.stil,
                                              fail_cycle_container )

    // Increment pattern
    execute_pattern( DLV_NP0_membistpv_1.stil )

    // Save the failure log
    store_data( loop, fail_cycle_data )

    // Tester iterates the Execute and Increment patterns

    loop++
}
```

Results

The tool generates the following test patterns for the membistpv_1 test:

- membistpv_1.stil: GoNoGo pattern

- DLV_IP0_membistpv_1.stil: ESOE initialize diagnostic pattern
- DLV_EP0_membistpv_1.stil: ESOE execute diagnostic pattern
- DLV_NP0_membistpv_1.stil: ESOE increment diagnostic pattern

Collecting and Converting the Failure Data

Load the test pattern and test program, and run the test program as you normally would on your ATE.

Prerequisites

- You have prepared the test patterns and the test program as described in “[Preparing the Test Patterns and the Test Program](#).”

Procedure

1. Load the test program and all the test patterns into the ATE.
2. Run the test program, and ensure that:
 - The state of the device on the tester remains the same between execution of the ESOE diagnostic patterns in the data collection procedure.
 - Phase lock loops (PLLs), if any, remain locked during data collection. Because the PLL initial sequence with a user-defined sequence is applied only to the Initialize pattern, “keep-alive” clocks are mandatory between one pattern execution and another.
3. To be compatible with process_memory_failures, you must convert the raw STIL or raw SVF failure log files to JSON format.
 - For STIL patterns, convert to CDP pattern cycles to JavaScript Object Notation (JSON) format as required by the process_memory_failures command.
 - For SVF patterns, convert to failing command ID and bit offset to JSON format as required by the process_memory_failures command.

For information about the JSON format, see <http://www.json.org>.

Results

[Example 7-3](#) shows the JSON format of a raw STIL ESOE failure log file.

Example 7-3. Raw STIL ESOE Failure Log File JSON Format

```
{  
  "Version": 1,  
  "Type": "ESOE", //Other types include Compstat, LBIST, Flop, and SOE  
  "TrackingInfo": {} // Optional and free-form value pairs to identify
```

```

        // failures and allow backmapping to a specific
        // design, lot, or set of coordinates
    "Design": "<device_name>",
    "DeviceID": "<deviceId>",
    "XCoordinate": "<x_coord>",
    "YCoordinate": "<y_coord>"

},
"FailDataType": "RawSTIL",
"RawSTIL": [
{
    "UserTestName": "membistpv_1", // Name of the test provided
                                // by user
    "StartingSOEID": 1, // First SOE run number (default is 1)
    "FailingCycles": ["14,42,69,109,136, 7", "15,16,55"]
        // Actual failing cycles, where each string in the
        // array contains the list of failing cycles for one
        // SOE run
},
{
    "UserTestName": "membistpv_3",
    "StartingSOEID": 55,
    "FailingCycles": ["14,42,69,109,136, 7", "15,42,55"]
},
{
    "UserTestName": "membistpv_7",
    "StartingSOEID": 1,
    "FailingCycles": ["14,42,69,115,130, 7", "16,45,55"]
}
]
}

```

[Example 7-4](#) shows the JSON format of a raw SVF ESOE failure log file.

Example 7-4. Raw SVF ESOE Failure Log File JSON Format

```

{
"Version": 1,
>Type": "ESOE", //Other types include Compstat, LBIST, Flop, and SOE
"TrackingInfo": { // Optional and free-form value pairs to identify
                  // failures and allow backmapping to a specific
                  // design, lot, or set of coordinates
    "Design": "<device_name>",
    "DeviceID": "<deviceId>",
    "XCoordinate": "<x_coord>",
    "YCoordinate": "<y_coord>"

},
"FailDataType": "RawSVF",
"RawSVF": [
{
    "UserTestName": "membistpv_1", // Name of the test specified
                                // by the user
    "StartingSOEID": 1, // First SOE run number (default is 1)
    // SVF failures (one string per SOE run) where each string in
    // the array contains the list of failing SVF commands and a
    // comma separated list of failing bit offsets
}
]
}

```

```
// In a given SOE Run, failing commands and their bits are
// separated using ";" 

// The following failures are for 2 SOE runs (1 and 2). We know
// this due to the setting "StartingSOEID": 1

// The first SOE run ("25:3,4; 29:6") contains failures for 2 SVF
// commands (25 and 29), where the failing bits for SVF command 25
// are 3 and 4, while the second SVF command (29) has only one
// failing bit, 6.
"CommandID:BitOffsets":["25:3,4; 29:6","25:3,4; 29:8,66"]
},
{
  "UserTestName":"membistpv_2",
  "StartingSOEID": 1,
  "CommandID:BitOffsets":["25:3,4; 29:6","25:3,4; 29:8,66"]

}
]
```

Running Diagnosis to Generate Diagnostic Bitmap Files

Use the process_memory_failures command to generate an output bitmap file formatted in standard JSON. The tool uses the raw STIL or raw SVF ESOE failure log files and the CDP as inputs.

Prerequisites

- You have generated raw STIL or raw SVF failure log files as described in “[Collecting and Converting the Failure Data](#).”

Procedure

- Run the following command to generate the diagnostic bitmap file.

```
process_memory_failures
  --cdp cdp_path
  --failData { failure_log_directory | failure_log_file }
  [ --outDir datalog_directory ]
```

Where valid values are as follows:

- **--cdp cdp_path**—Required switch that specifies the CDP directory name.
- **--failData { failure_log_directory | failure_log_file }**—A required switch that specifies a directory that contains failure logs files or a specific failure log file. If you specify a failure_log_directory, the tool only considers files with the .faillog suffix.

- `--outDir datalog_directory`—An optional switch that specifies the directory in which to store the results files. If not specified, the tool writes the bitmap files to the current working directory.

For example, suppose you have two failure log files, `log1.faillog` and `log2.faillog`, located in the `membistTest` directory, and `top.cdp` is your CDP. They both reside in the current directory. The following command generates two bitmap files named “`log1.faillog.bitmap`” and “`log2.faillog.bitmap`” and stores them in the results directory.

```
process_memory_failures --cdp top.cdp/ --failData membistTest/ --outDir ./results/
```

The following example generates a bitmap file named “`mbist_fail1.fail.bitmap`” from the specified failure log file and stores it in the results directory.

```
process_memory_failures --cdp top.cdp/ --failData mbist_fail1.fail --outDir ./results/
```

Results

As an example, for the following raw STIL ESOE failure log file as input:

```
{
  "Version": 1,
  "Type": "ESOE",
  "TrackingInfo": {
    "Design": "Top",
    "DeviceId": "0556x8952"
  },
  "FailDataType": "RawSTIL",
  "RawSTIL": [
    {
      "UserTestName": "membistpv_1",
      "StartingSOEID": 1,
      "FailingCycles": [
        "4884,4892,4908,4916,4924,367824,367840,369336,371352", "4900,4884,4892,
        "4908,4916,4924,367824,367840,369336,371352,371112" ]
    }
}
```

The tool outputs the following bitmap file:

```
{
  "CreatedWith" : "process_memory_failures version: 2013.2",
  "TrackingInfo" : {
    "Design" : "Top",
    "DeviceId" : "0556x8952"
  },
  "Header" : "FailureIndex ControllerName Memory Expected \
  TestPort PhaseOrInstruction BitPosition Bank Row Column",
  "Failures" : [
    "0 BP0  MEM3 0 0 1 1 0 0 0",
    "1 BP1  MEM4 0 0 1 7 0 0 1",
    "2 BP1  MEM4 0 0 1 7 0 0 1"
  ]
}
```

Related Topics

[The Diagnostic Bitmap File](#)

The Diagnostic Bitmap File

The diagnostic bitmap file produced by process_memory_failures is in JSON format. For more information on JSON, see <http://www.json.org>.

Note



The diagnostic bitmap file reports logical failure information but not physical failure information. This applies to ESOE and SOE.

[Example 7-5](#) shows the format of the diagnostic bitmap file.

Example 7-5. Bitmap File Format

```
{  
    "CreatedWith": "<tool_name_and_version>",  
    "TrackingInfo": {"<tracking_info>"},  
}  
"Header": "FailureIndex ControllerName Memory PhysicalExpected \  
          TestPort PhaseOrInstruction BitPosition PhysicalBank \  
          PhysicalRow PhysicalColumn",  
"Failures": [  
    "<fail_index_number> <ctrl_name> <memory_name> <phys_exp_value> \  
     <port_number> <algorithm> <bit_position> <phys_bank> \  
     <phys_row> <phys_column>",  
    "<fail_index_number> <ctrl_name> <memory_name> <phys_exp_value> \  
     <port_number> <algorithm> <bit_position> <phys_bank> \  
     <phys_row> <phys_column>",  
]  
}
```

The bitmap file contains a field named “Header” that defines the data that appears in the Failures data array. By default, the Failures data array contains the information in the order shown in [Table 7-1](#).

Table 7-1. Default Failures Data Array Fields

Field Name	Description
FailureIndex	Failure number for each bitmap string, starting with 0. The failure counter increases by 1 for each found failure. This field always appears in the bitmap file.
ControllerName	Controller name for the failed memory. This field always appears in the bitmap file.
Memory	Name of the failed memory. This is a customizable field.

Table 7-1. Default Failures Data Array Fields

Field Name	Description
PhysicalExpected	Expected value (0 or 1) for the physical cell. This is a customizable field.
TestPort	Failing port number. This is a customizable field.
PhaseOrInstruction	Failing algorithm phase or instruction. This is a customizable field.
BitPosition	Failing bit position. This is a customizable field.
PhysicalBank	Failing physical bank. This is a customizable field.
PhysicalRow	Failing physical row. This is a customizable field.
PhysicalColumn	Failing physical column. This is a customizable field.

You can customize the data that appears in the Failures data array by adding a Header field to the raw STIL or raw SVF ESOE failure log file. When you add a Header field to the ESOE failure log file, only the fields you specify will appear in the output bitmap file in addition to the FailureIndex and the ControllerName fields (which always appear in the output bitmap file).

In addition to the customizable fields listed in [Table 7-1](#), you can add the following fields to the Header field in the raw STIL or raw SVF ESOE failure log file.

Table 7-2. Optional Failures Data Array Fields

Field Name	Description
MemoryModule	Name of the memory library module.
PhysicalAddress	Failing physical address.
LogicalBank	Failing logical bank.
LogicalRow	Failing logical row.
LogicalColumn	Failing logical column.
LogicalAddress	Failing logical address.
LogicalExpected	Expected value (0 or 1) at the port data line.
PortDataLine	Failing port data line.

For example, suppose you add the following Header field to your raw STIL ESOE failure log file:

```
{
    "Version": 1,
    "Type": "ESOE",
    "TrackingInfo": {
        "Design": "Top",
        "DeviceId": "0556x8952"
    }
}
```

```
},
"Header" : "Column PhaseOrInstruction Memory PhysicalRow \
PhysicalExpected TestPort BitPosition PhysicalBank \
LogicalBank PhysicalRow LogicalRow",

"FailDataType" : "RawSTIL",
"RawSTIL": [
{
  "UserTestName" : "membistpv_1",
  "StartingSOEID": 1,
  "FailingCycles":
  ["4884,4892,4908,4916,4924,367824,367840,369336,371352", "4900,4884,4892,
  4908,4916,4924,367824,367840,369336,371352,371112"] }
]
```

The output bitmap file would appear as follows:

```
{
  "CreatedWith" : "process_memory_failures version: 2013.2",
  "TrackingInfo" : {
    "Design" : "Top",
    "DeviceId" : "0556x8952"
  },
  "Header" : "FailureIndex ControllerName Column PhaseOrInstruction \
Memory PhysicalRow PhysicalExpected TestPort BitPosition \
PhysicalBank LogicalBank PhysicalRow LogicalRow",
  "Failures" : [
    "0 BP0 0 1 MEM3 0 0 0 1 0 0 0 0 0",
    "1 BP1 1 1 MEM4 0 0 0 7 0 0 0 0 0",
    "2 BP1 1 1 MEM4 0 0 0 7 0 0 0 0 0"
  ]
}
```

Validating ESOE Test Diagnostic Patterns in a Simulated Environment

You can use the Tessent SiliconInsight SimDUT tool to simulate the application of ESOE test diagnostic patterns on a Tessent SiliconInsight Desktop tester. SimDUT is a software package that simulates the DUT and provides responses as if you are interacting with a real tester. The simulator converts the responses to failures that you can then diagnose with Tessent SiliconInsight Desktop.

The validation process described in this section targets top-level designs for manufacturing pattern validation. SimDUT requires the ModelSim or Questa Verilog simulator from Mentor Graphics.

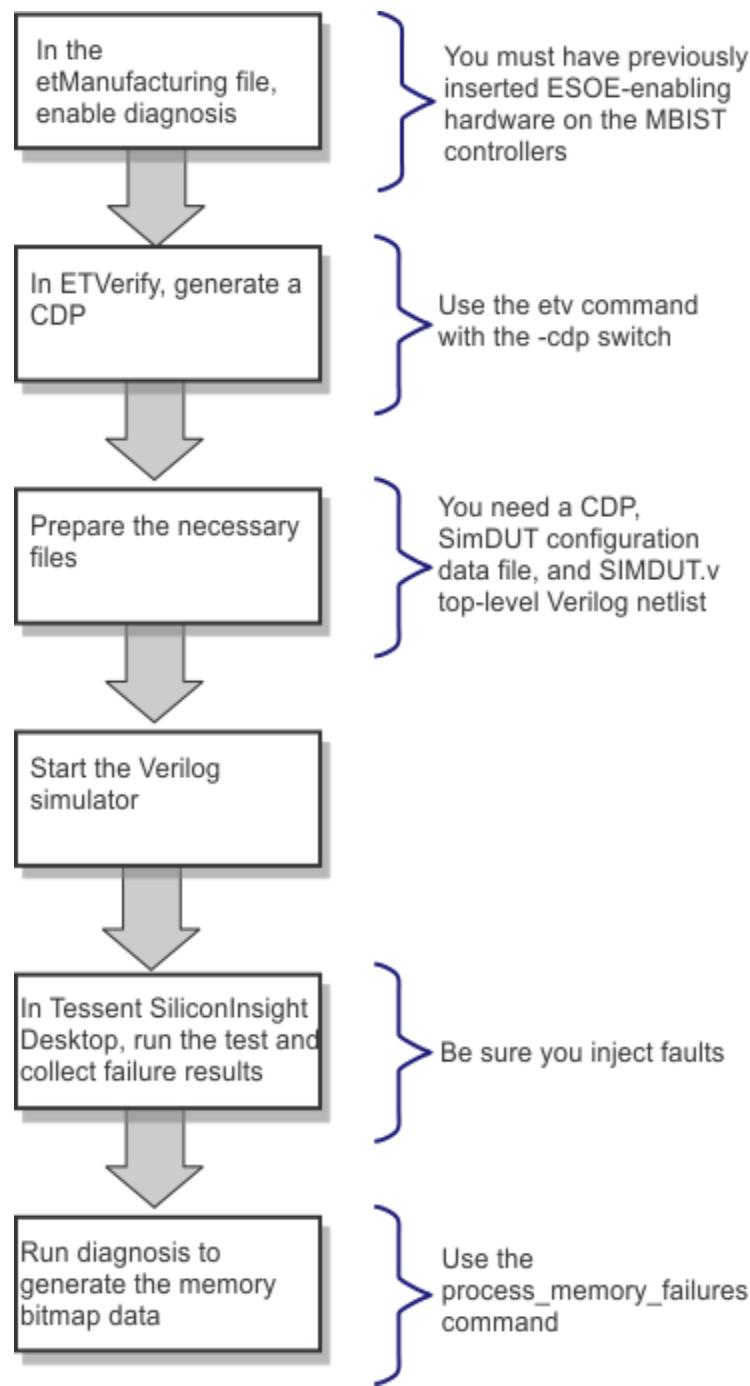
[Figure 7-1](#) shows the high-level flow for simulating ESOE test patterns.

Note



The first two steps are not specific to simulating ESOE test patterns. They reflect what you would need to do even if you were not planning to perform simulation.

Figure 7-2. High-Level Flow for Simulating ESOE Test Patterns



Prerequisites

- You have inserted the required ESOE-enabling hardware into the MBIST controller as described in “[Creating Stop-On-Nth-Error Test Benches for Bitmap Applications](#)” in the *Tessent MemoryBIST User’s and Reference Manual*.

- You have an LVDB.
- You have an RTL or gate-level Verilog netlist from Tessent MemoryBIST.
- You have a Verilog library ready for simulation with the ModelSim or Questa Verilog simulator. This procedure only supports ModelSim or Questa simulation.
- Ensure that your simulator build is prepared. Optimally, for Questa you should use Questa build 10.2d or later.

Procedure

1. Prepare the ETVerify etManufacturing file and generate a CDP from an existing LVDB as described in section “[Generating a CDP That Contains ESOE Test Patterns](#).”

As a result of this step, ETVerify generates a CDP named *design_name.cdp* at the same directory level as your LVDB. For example, if your design is called “top,” the cdp is named “top.cdp.”

2. Prepare a configuration data file for SimDUT as described in “[The Configuration Data File for SimDUT](#)” in the *Tessent SiliconInsight User’s Manual for Tessent Shell*.

The selected_tester must be the name of the tester that has an adaptor of type SIMDUT. The selected_tester launches SimDUT.

3. Prepare a SIMDUT.v top-level Verilog netlist file as described in “[The SIMDUT.v Top-Level Verilog Netlist File](#)” in the *Tessent SiliconInsight User’s Manual for Tessent Shell*.

4. Compile the Verilog netlist and Verilog library using the ModelSim or Questa simulator. For example:

```
vlib work
vlog design.v memory.v -y verilog_lib -64 -timescale "1ns / 1ps" \
+libext+.ilm+.scan_shell+.v+.vb+.vb +librescan
```

5. Invoke the ModelSim or Questa Verilog simulator, ensuring that in the invocation you:

- Link the libSimdutVpi.so library to the simulator. The library contains SimDUT functions based on standard Verilog Procedural Interface functions. This library receives the test stimuli from the SID tester process and returns the failing cycle data to the SID tester process.

Specify the pathname. For example:

```
$TESSENT_HOME/share/SiliconInsight/Simdut/lnx-x86/ \
[lib64 | lib32]
```

- Specify the module name as defined in the SIMDUT.v top-level netlist file.
- Specify the port name if you are not using the default 2111 port. Do this by specifying the following argument when you invoke the Verilog simulator:

```
+simdutport:<N> // where N is the port number
```

For example, for the Mentor Graphics Questa simulator, suppose you are using port 5555 as defined in your configuration data file. You want to simulate the TB module as defined in your SIMDUT.v file. Invoke the simulator as follows:

```
vsim -64 -c +nospecify -voptargs="+acc" -do "run -all" TB
-voptargs="+acc" +nowarnTFMPC -pli
$TESSENT_HOME/share/SiliconInsight/Simdut/lnx-
x86/lib64/libSimdutVpi.so +simdutport:5555
```

Prior to invocation, be sure that you have set your \$TESSENT_HOME variable.

Refer to the Mentor Graphics Questa documentation for details.

6. In Tessent Shell, use Tessent SiliconInsight to execute and simulate a test pattern for the DUT and return the simulated failure results. For example, the following command launches Tessent Shell with a dofile called “cdp_simulate.tcl”:

```
tessent -shell -dofile dofiles/cdp_simulate.tcl -log tsi_shell.log -rep
```

The following sample “cdp_simulate.tcl” dofile executes and simulates a test pattern for the DUT and returns the simulated failure results.

For more information about (optionally) using the add_simdut_fault command as shown below, see “[SimDUT Fault Injection for Memory Models](#)” in the *Tessent SiliconInsight User’s Manual for Tessent Shell*.

```
set_dofile_abort off

# Context set to SiliconInsight
set_context patterns -silicon_insight

# Tells SI not to verify the pattern against a design since \
# there is no design
set_si_options -cdp_verification off

# Read in the configuration data file for SimDUT so that it \
# defines SI desktop as the tester
read_config_data ./data/SidSetup.cfg

# Remove the old Tessent Shell-based CDP, if any, since the
# following step is going to create a ts_top.cdp directory as a
# holder to store Tessent Shell-based cdp related info
system rm -fr ts_top.cdp

# Launch sid tester
launch_sid_tester -cdp ts_top.cdp -new

# Add ESOE patterns
add_cdp_test InitFailLimit -pattern
./top.cdp/PPDIR/patterns/DLV_IP0_lvmarchx_0_25MHz.stil
add_cdp_test SOERun -pattern
./top.cdp/PPDIR/patterns/DLV_EP0_lvmarchx_0_25MHz.stil
add_cdp_test IncrementFailLimit -pattern
./top.cdp/PPDIR/patterns/DLV_NP0_lvmarchx_0_25MHz.stil
```

```
# optionally, inject memory failures
add_simdut_fault -signal { /TB/dut/navigation_INST/sample_ram1/A[2]
} -fault 0

# execute ESOE flow and start simulation on the vsim source
$::env(TESSENT_HOME)/share/SiliconInsight/Utilities/write_pmf_fail_
file.tcl

# source
# $TESSENT_HOME/libs/liblivate/src/Utilities/write_pmf_fail_file.tcl
FailLogWriter writer

# set up SOE failure limit
set StopOnErrorHandler 150

# execute the test
execute_cdp_test InitFailLimit
for {set i 0} {$i < $StopOnErrorHandler} {incr i} {
    puts "iteration $i"

    # If the SOE run passes, it means there are no more failures
    set exec_status [execute_cdp_test SOERun -collect_data_type_list
variable]
    if { $exec_status == 0 } {
        break;
    }
    # the mismatch information will be written out
    writer collect_failures
    execute_cdp_test IncrementFailLimit
}

shutdown_sid_tester

# Write failure log for process_memory_failures utility
writer write_pmf_faillog -user_test_name "lvmarchx_0_25MHz" -
output_file memory.fail
```

Tessent SiliconInsight simulates the ESOE test patterns with injected faults and returns the mismatch failure information in terms of the cycles and pins.

7. In the mismatch failure log, check that memory.fail, the failure file in JSON format, was created. The log message is shown in bold in the sample mismatch failure log shown below.

Check the memory.fail file to ensure that the tool logged the failing cycles.

Refer to [Example 7-3](#) and [Example 7-4](#) for more details about the JSON failure file format.

```
// Test 'SOERun' failed.
// Variable failures and unmapped failures of pattern
'DLV_EP0_lvmarchx_0_25MHz.stil' :
//
// Cycle Pin
// ----- ---
```

```
// 75098 TDO
// -----
// 81418 TDO
...
// -----
// 81890 TDO
// -----
// 81962 TDO
// -----
// sub-command: execute_cdp_test IncrementFailLimit
// Test 'IncrementFailLimit' passed.
iteration 1
// sub-command: execute_cdp_test SOERun -collect_data_type_list
// variable
// Test 'SOERun' failed.
// Variable failures and unmapped failures of pattern
'DLV_EP0_lvmarchx_0_25MHz.stil' :
//
// Cycle Pin
// -----
// 75098 TDO
// -----
// 81418 TDO
// -----
...
// -----
// 81906 TDO
// -----
// -----
// sub-command: execute_cdp_test IncrementFailLimit
// Test 'IncrementFailLimit' passed.
iteration 2
... // -----
// sub-command: execute_cdp_test IncrementFailLimit
// Test 'IncrementFailLimit' passed.
iteration 64
// sub-command: execute_cdp_test SOERun -collect_data_type_list
// variable
// Test 'SOERun' passed.
// command: writer write_pmf_faillog -user_test_name
"lvmarchx_0_25MHz" -output_file memory.fail
// Writing failure file memory.fail for user test lvmarchx_0_25MHz.
// Note: Failure file memory.fail for 'process_memory_failures' has
// been created.
```

8. Using the process_memory_failures command, run diagnosis as described in “[Running Diagnosis to Generate Diagnostic Bitmap Files](#).”

Your diagnosis results should match the faults that you injected using the add_simdut_fault -signal command.

Results

When you run diagnosis, the tool generates a diagnostic bitmap file, which is in JSON format. See section “[The Diagnostic Bitmap File](#)” for more information.

Chapter 8

Setting Up and Using Tesson SiliconInsight Desktop

This chapter provides instructions on how to install and use Tesson SiliconInsight Desktop. Tesson SiliconInsight Desktop enables test and diagnosis of a device containing Mentor Graphics BIST capabilities connected to an adaptor through a USB port of a laptop/desktop computer.

Additionally, this chapter describes how to set up and use Tesson SiliconInsight Desktop to test and diagnose devices in a multi-site environment.

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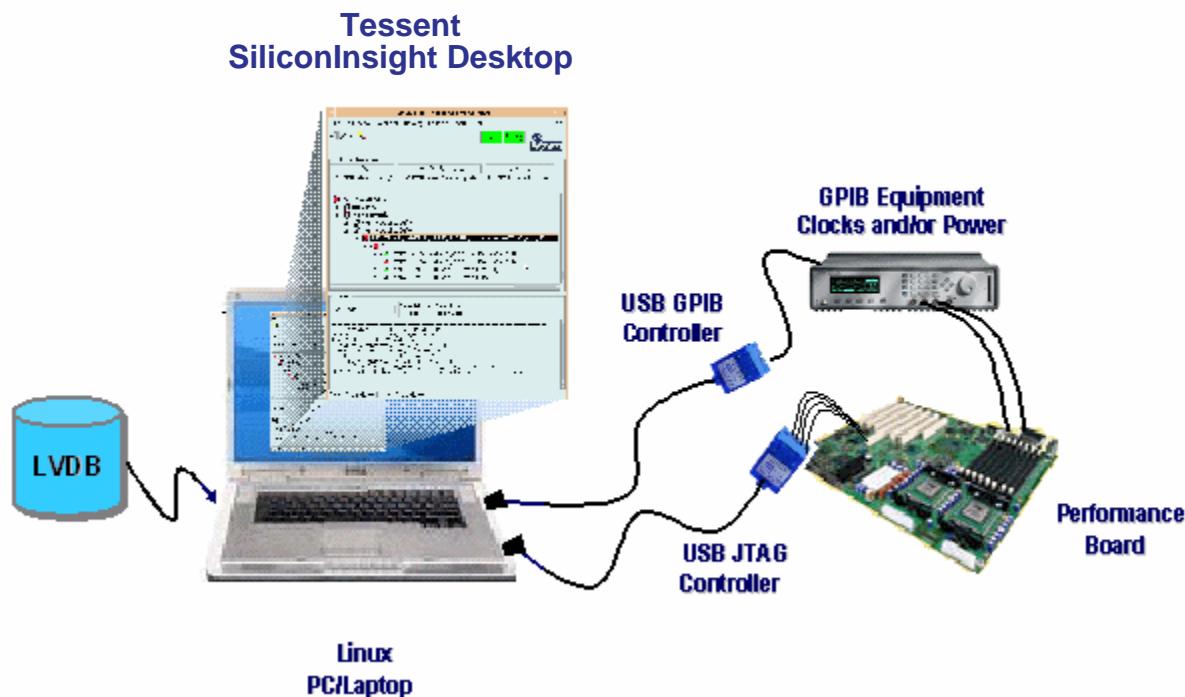
Overview

Tesson SiliconInsight Desktop is a version of the Tesson SiliconInsight software that runs on any Linux PC or laptop. All communication to the device under test is performed through a

standard USB cable and simple adaptor that connects to standard IEEE 1149.1 pins on a performance board. Details on how to wire the pins on the board to properly connect to the adaptor are provided in “[Setting Up the Adaptor](#).”

Tessian SiliconInsight Desktop also supports the ability to control external clocks and/or power supplies connected to the board for more detailed characterization activities. This control is accomplished using an optional USB-to-GPIB adaptor. Details on how to properly connect this adaptor are provided in “[Setting Up the USB-to-GPIB Adaptor](#).” A sample Tessian SiliconInsight Desktop setup using both adaptors is illustrated in [Figure 8-5](#).

Figure 8-1. Tessian SiliconInsight Desktop Hardware Set-Up



Details on how to install the Tessian SiliconInsight Desktop software on a Linux platform and the related system requirements are fully described in this document.

Setting Up the Adaptor

Mentor Graphics currently supports adaptors that are described in the following sections:

- [Olimex ARM-USB-OCD and ARM-USB-OCD-H Adaptors](#)
- [Tin Can Tools Flyswatter2 Adaptor](#)
- [Xverve SignalizerSHA40 and SignalizerH2/H4 Adaptors](#)
- [Xverve Signalizer Adaptor](#)

- Xverve Signalizer SP Adaptor
- Amontec Adaptors

Olimex ARM-USB-OCD and ARM-USB-OCD-H Adaptors

Mentor Graphics supports two adaptors manufactured by Olimex Ltd.—the ARM-USB-OCD and ARM-USB-OCD-H adaptors as shown in [Figure 8-2](#).

Figure 8-2. Olimex ARM-USB-OCD and OCD-H Adaptors



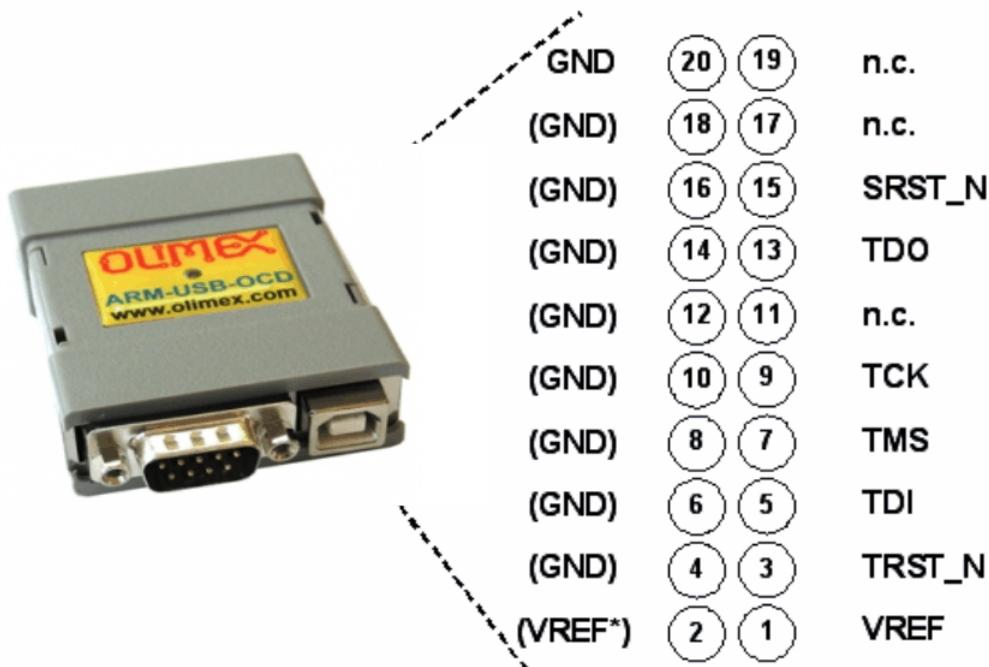
Both adaptors have the same pinout, which is provided in [Figure 8-3](#). The only adaptor pins that you must connect to the performance board signals are listed below in [Table 8-1](#).

Table 8-1. Olimex Adaptor Connections

Pin Name	Pin Number	Description
<i>TDI</i>	5	Test Data Input (to DUT)
<i>TMS</i>	7	Test Mode Select (to DUT)
<i>TCK</i>	9	Test Clock (to DUT)
<i>TDO</i>	13	Test Data Output (from DUT)
<i>VREF</i>	1	Voltage Reference
<i>GND</i>	20	Ground

Note  Ensure that all ground pins (4, 6, 8, 10, 12, 14, 16, 18, 20) are grounded for good signal fidelity.

Figure 8-3. Olimex Adaptor Pinout



Note

The Adaptor TRST_N (Test Reset) pin is not used. Tesson SiliconInsight Desktop performs a test reset using the 1149.1 standard's reset sequence. The DUT's TRST pin must be pulled low on the board to ensure that the device can operate in normal functional mode when the adaptor is not being used.

The adaptor's SRST_N pin is not used and need not be connected to the DUT.

For detailed information about these adaptors, refer to the Olimex Ltd. website at the following URL:

<http://www.olimex.com>

The devices are available through several distributors world-wide:

<https://www.olimex.com/Distributors/>

Tin Can Tools Flyswatter2 Adaptor

Mentor Graphics supports the Tin Can Tools Flyswatter2 adaptor as shown in Figure 8-4.

Figure 8-4. Tin Can Tools Flyswatter2 Adaptor



The pin connections and pinout for the Flyswatter2 adaptor are the same as that for the Olimex ARM-USB-OCD and ARM-USB-OCD-H adaptors. Refer to [Table 8-1](#) and [Figure 8-3](#) for details.

For detailed information about this adaptor, refer to the Tin Can Tools website at the following URL:

<http://www.tincantools.com>

Xverve SignalyzerSHA40 and SignalyzerH2/H4 Adaptors

The SignalyzerSHA40 and SignalyzerH2/H4 adaptors ([Figure 8-5](#)) are produced by Xverve Technologies, Inc. Signalyzer H2 and Signalyzer H4 are no longer available. They have been replaced by the Signalyzer SHA40.

Figure 8-5. SignalyzerSHA40 and SignalyzerH2/H4 Adaptors



SignalyzerSHA40 and SignalyzerH4 support up to 32 I/O pins divided into 4 channels of 8 pins while SignalyzerH2 supports up to 16 I/O pins divided into 2 channels of 8 pins. Since these

adaptors are based on the USB 2.0 “high speed” protocol, they are at least 5 times faster than plain Signalyzer which is based on “full speed” version of USB 2.0.

For the adaptors’ operating parameters, refer to the Xverve Technologies website at the following URL:

<http://www.xverve.com>

Caution

-  For the SignalyzerSHA40 and SignalyzerH2/H4 adaptors, Pin 2 (VEXT) and Pin 26 (VEXT) are 5.0V DC supply pins from the USB port of the computer. These pins, in contrast to older Signalyzer models, are not for VREF input and could damage the Signalyzer device if you use them as such.
-

SignalizerH2 Pin Map

[Figure 8-6](#) shows the SignalizerH2 channel pin map. Tesson SiliconInsight Desktop can only simultaneously drive the pins on the same channel. In the SignalizerH2, these channels are A and B.

Figure 8-6. SignalizerH2 Channels Pin Map

GND(A)	1	2	VEXT(A)	GND(B)	1	2	VEXT(B)
A0	3	4	A1	B0	3	4	B1
A2	5	6	A3	B2	5	6	B3
A4	7	8	A5	B4	7	8	B5
A6	9	10	A7	B6	9	10	B7
NC	11	12	NC	NC	11	12	NC
NC	13	14	NC	NC	13	14	NC
NC	15	16	NC	NC	15	16	NC
NC	17	18	NC	NC	17	18	NC
NC	19	20	NC	NC	19	20	NC
NC	21	22	NC	NC	21	22	NC
NC	23	24	NC	NC	23	24	NC
NC	25	26	VEXT(C)	NC	25	26	VEXT(D)

Channel A

Channel B

Signalizer SignalizerSHA40 and SignalizerH4 Pin Map

[Figure 8-7](#) shows the SignalizerSHA40 and SignalizerH4 channel pin map. Tesson SiliconInsight Desktop can only simultaneously drive the pins on the same channel. In the SignalizerSHA40 and SignalizerH4 adaptors, these channels are A, B, C, and D.

Figure 8-7. Signalizer SHA40 and SignalizerH4 Channels Pin Map

GND(A)	1	2	VEXT(A)	GND(B)	1	2	VEXT(B)
A0	3	4	A1	B0	3	4	B1
A2	5	6	A3	B2	5	6	B3
A4	7	8	A5	B4	7	8	B5
A6	9	10	A7	B6	9	10	B7
C0	11	12	C1	D0	11	12	D1
C2	13	14	C3	D2	13	14	D3
C4	15	16	C5	D4	15	16	D5
C6	17	18	C7	D6	17	18	D7
NC	19	20	NC	NC	19	20	NC
NC	21	22	NC	NC	21	22	NC
NC	23	24	NC	NC	23	24	NC
GND(C)	25	26	VEXT(C)	GND(D)	25	26	VEXT(D)

Port A

Port B

Xverve Signalyzer Adaptor

The Xverve Signalyzer is no longer available. It has been replaced by SignalyzerSHA4. The following section is intended for existing Xverve Signalyzer users.

The Xverve Signalyzer shown in [Figure 8-8](#) is produced by Xverve Technologies.

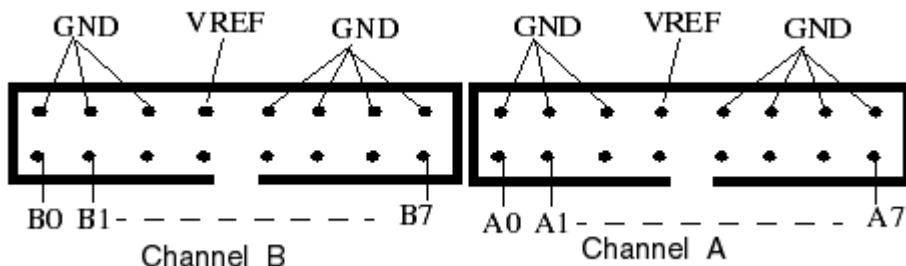
Figure 8-8. Xverve Signalyzer



This Signalyzer supports up to 16 IO pins divided in two pin groups (i.e., Channel A, Channel B), each channel supporting 8 IO pins. Only one channel pins might be burst in a single pattern.

[Figure 8-9](#) is displays the Xverve Signalyzer channel pin map.

Figure 8-9. Signalyzer Channels Pin Map



So, while *Channel A* might connect to 4/5 TAP pins (depending if TRST is contacted) and 3/4 other dynamic/static pins, *Channel B* might be used to control other user pins which are not used by LVDB.

The other channel (i.e., *Channel B*) pins might be used as well to toggle a user sequence to allow access of Mentor Graphics TAP which will then be accessed through *Channel A*.

Note



For best signal Fidelity, make sure all Ground pins are grounded.

Xverve Signalyzer SP Adaptor

The Signalyzer SP has 64 general purpose I/O pins. All pins may be toggled at the same time. Each pin may be independently assigned to be input or output. The Signalyzer SP adaptor is produced by Xverve Technologies.

Signalyzer SP Pinout for Tesson SiliconInsight Desktop

- For a complete pinout of the Signalyzer SP pins, see the manufacturer's website at the following URL:
www.xverve.com
- The Signalyzer SP hardware can be configured in two independent, or one expanded GPIO port. Tesson SiliconInsight only uses the Signalyzer SP as one expanded 64-pin port. You can set voltage levels for each of the two ports independently.
- You only need to connect one of the Signalyzer SP GND pins on each Signalyzer SP port to ground (1, 11, 21, 31, 41, 49). These pins are connected together internally inside the Signalyzer SP.
- Pin 2 is a Signalyzer SP output that can be used to validate the I/O level (controlled by invocation switch). Pin 2 is otherwise not used by Tesson SiliconInsight Desktop.
- Pins 12, 22, 32, and 42 are unused by Tesson SiliconInsight Desktop.

To support Signalyzer SP, the Tesson SiliconInsight software tree contains a new HW definition called *default.hwdef.signalizerSP*. This file describes the names of the HW channels that are specified in your pin map file for multi-site testing—see “[Creating the Tesson SiliconInsight Pin Map File for Signalyzer SP](#).”

[Figure 8-10](#) shows the Signalyzer SP pinout for Tesson SiliconInsight Desktop described in the *default.hwdef.signalizerSP* file.

Figure 8-10. HW Definition File Signalizer SP Pinout

Port A GPIO00				Port B GPIO00			
# Signalizer SP Port A				# Signalizer SP port B			
# Name Pin# ----- Pin# Name				# Name Pin# ----- Pin# Name			
# GND 1 2 NC				# GND 1 2 NC			
# P0 3 4 P1				# P32 3 4 P33			
# P2 5 6 P3				# P34 5 6 P35			
# P4 7 8 P5				# P36 7 8 P37			
# P6 9 10 P7				# P38 9 10 P39			
# GND 11 12 NC				# GND 11 12 NC			
# P8 13 14 P9				# P40 13 14 P41			
# P10 15 16 P11				# P42 15 16 P43			
# P12 17 18 P13				# P44 17 18 P45			
# P14 19 20 P15				# P46 19 20 P47			
# GND 21 22 NC				# GND 21 22 NC			
# P16 23 # 24 P17				# P48 23 # 24 P49			
# P18 25 # 26 P19				# P50 25 # 26 P51			
# P20 27 # 28 P21				# P52 27 # 28 P53			
# P22 29 30 P23				# P54 29 30 P55			
# GND 31 32 NC				# GND 31 32 NC			
# P24 33 34 P25				# P56 33 34 P57			
# P26 35 36 P27				# P58 35 36 P59			
# P28 37 38 P29				# P60 37 38 P61			
# P30 39 40 P31				# P62 39 40 P63			
# GND 41 42 NC				# GND 41 42 NC			
# NC 43 44 NC				# NC 43 44 NC			
# NC 45 46 NC				# NC 45 46 NC			
# NC 47 48 NC				# NC 47 48 NC			
# NC 49 50 NC				# NC 49 50 NC			
# -----				# -----			

This file is located in the Tessian SiliconInsight software tree at the following directory path:

Tessian_software_tree/lib/tools/etas_usb

For the adaptor's operating parameters, refer to the Xverve Technologies website at the following URL:

<http://www.xverve.com>

Debugging Voltage Level Issue in Setting Up Signalizer SP

During the Signalizer SP setup, it is usually a good idea to measure the GPIO pin voltages after the Signalizer SP has been connected to DUT. If the measured voltage for any GPIO pins is below the preset voltage, then it means the setting may not be done correctly.

All the GPIO pins are referenced to two power pins: portA GPIO pins are referenced to pin2 (VA) and portB pins pin22 (VB). Both of the power pins have a reference voltage defined by the user and are usually between 1.2v and 3.3v. In order to debug, perform the following steps:

1. Set up reference voltage level during invoking Tesson SiliconInsight from a Linux shell as in the following example:

```
tesson -siliconinsight -desktop -cable signalizerSP -pioLevelsA 1.8v -pioLevelsB 1.8v -  
numberOfSites 61
```

 **Note**

The -pioLevelsA sets up reference voltage pin2 and -pioLevelsB pin22. They can have different voltages.

2. For any GPIO portA pin problem, start measuring voltage level at pin2 of Port A connector (similarly for GPIO portB pins, measure pin 2 of Port B connector). Make sure the power pins are at the requested level (that is, specified by flags -pioLevelsA and -pioLevelsB), if not, repeat steps 1 and 2 with Signalizer SP disconnected from target device(s). If problem persists with nothing connected to Signalizer SP GPIO, contact the Signalizer SP manufacturer.
3. Assume you are debugging issues for portA pins. If the pin2 has the voltage at the requested level (that is, specified by flags -pioLevelsA and -pioLevelsB), which is good, then disconnect all the other GPIO pins (including portB GPIO pins) from the DUT except just one GPIO portA pin. Measure it to make sure it is 1.8v. If it works fine, then connect more GPIO portA pins to DUT and do measurement.
4. If a certain pin has partial voltage, the do the following:
 - a. Measure between this problematic GPIO pin and other GPIO pins to see whether there are any shortage.
 - b. Check whether the DUT board is set up right. Especially if there is any interposer board placed on top of DUT board.
 - c. The next thing to check is whether there are any pull-up or pull-downs for the associated pin on the DUT board
 - d. Whether the design itself has pull-up or pull-down for this particular signal which connects to the problematic GPIO pin.
5. If all the GPIO pins having consistent partial voltage, please reset the DUT board and the interposer board if any. If the problems are still there, please try a different Signalizer SP and if again the problem is there, then please contact Signalizer SP manufacturer.

Amontec Adaptors

The Amontec adaptors are no longer available. The following section is intended for existing users. The Olimex and Tin Can Tools adapters described in “[Olimex ARM-USB-OCD and ARM-USB-OCD-H Adaptors](#)” and “[Tin Can Tools Flyswatter2 Adaptor](#)” offer comparable capabilities.

Mentor Graphics currently supports two adaptors manufactured by Amontec—the JTAGkey and JTAGkey-Tiny adaptors that are shown in [Figure 8-11](#). The JTAGkey adaptor has a few more features than the JTAGkey-Tiny, but these are not used by Tesson SiliconInsight Desktop. Therefore, either adaptor can be used.

Any number of adaptors can be purchased directly from Amontec at www.amontec.com.

Figure 8-11. Amontec Adaptors



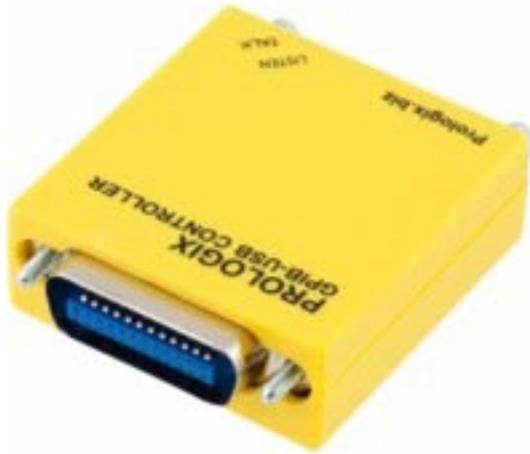
The pin connections and pinout for the Amontec adaptors are the same as those for the Olimex ARM-USB-OCD and ARM-USB-OCD-H adaptors. Refer to [Table 8-1](#) and [Figure 8-3](#) for details.

Setting Up the USB-to-GPIB Adaptor

The GPIB (General Purpose Interface Bus) option to Tesson SiliconInsight Desktop supports the seamless integration and usage of any GPIB-enabled instrument with Tesson SiliconInsight Desktop in a plug and play manner. Examples of these instruments include clock generators, power supplies and parametric measurement units (PMUs).

For GPIB integration, Tesson SiliconInsight Desktop currently supports the Prologix 6.0 adaptor manufactured by Prologix as shown in [Figure 8-12](#).

Figure 8-12. Prologix 6.0 Adaptor



This adaptor can be purchased directly from Prologix online at the following URL:

www.prologix.biz

All GPIB instruments may be daisy chained together through a single Prologix adaptor using standard GPIB cables.

-
- Note** When multiple GPIB instruments (for example, 20 power supplies are connected to SID in serial) through the GPIB bus, a “wait” statement (normally in Tcl scripts) is needed in order to have SID gain control of multiple GPIB instruments correctly.
-

Tesson SiliconInsight Desktop currently comes with built-in support for several instruments. Two of the GPIB instruments are:

- Stanford Research Systems CG635 shown in [Figure 8-13](#)
- Keithley 2602 PMU shown in [Figure 8-14](#).

Tesson SiliconInsight’s open architecture allows support for additional GPIB instruments to be added using a Tcl/Tk-based definition file. The step-by-step instructions on how to create such

file are documented in the Tessian SiliconInsight Desktop resource file. The resource file is located in <SI Install Directory>/lib/tools/etas_usb/default.hwdef.usb_jtag.

Figure 8-13. Stanford Research Systems CG635 Specifications

STANFORD RESEARCH SYSTEMS CG635

Frequency Range	1uHz – 2.05 GHz
Timing Resolution	16 digits ($f > 10$ kHz)
RMS jitter	< 1 ps (1 kHz to 5 MHz)
Wander (p-p)	< 20 ps (10 s persistence)
Amplitude Range	200 mV to 6.00 V
Level Resolution	10 mV
Transition Time	< 100 ps (20% to 80%)
Source Impedance	50 Ohms



Figure 8-14. Keithley 2602 PMU Specifications

KEITHLEY 2602 PMY

Output Ratings

Voltage	5 uV to 40V
Current	5 pA to 3 A



Programming Accuracy

Voltage	0.02%
Current	0.03%

Programming Resolution

Voltage	50 uV
Current	100 nA – 1 uA

The currently supported Instrument plug-ins are located in directory:

<SI Install Dir>/share/SiliconInsight/ATE/USB/Instruments.

System Requirements

You can find complete hardware and operating system requirements for Tessian SiliconInsight Desktop in the “[Tessian SiliconInsight Configuration](#)” section of the *Managing Mentor Graphics Tessian Software* manual.

Configuring Your Computer to Access the Adaptor

To configure your laptop or desktop computer to access the adaptor, perform the following steps:

- [Allow access to all users](#)
- [Allow Access to Users of the Prologix Adaptor](#)
- [Install the Motif library](#)

Allow access to all users

To allow access of Tesson SiliconInsight Desktop for all users in addition to *root*, perform the following operations when logged on as *root*:

For a Red Hat ES 5 Machine

1. Copy file *<SI Install Dir>/share/SiliconInsight/ATE/USB/Drivers/10-sid.rules* to directory */etc/udev/rules.d*
2. Enter *udevcontrol reload_rules*

For a Red Hat EL 6 Machine

1. The tool uses RPC communication so the *rpcbind* daemon on the computer must be running with the *-i* flag.
 - Run command *ps -ef | grep rpcbind* and check the flag on the running *rpcbind*.
 - If it is not running with the *-i* flag, kill it. You may have to login as root to do this.
 - Restart as root with the following command *rpcbind -i &*
2. Copy file *<SI Install Dir>/share/SiliconInsight/ATE/USB/Drivers/10-sid.rules* to the */etc/udev/rules.d* directory
3. Enter *udevadm control --reload-rules*

Allow Access to Users of the Prologix Adaptor

To allow access of the GPIB instruments to all users on a Red Hat ES 5 machine, you do not need to do anything.

Install the Motif library

Refer to “[Open Motif Requirements for Tesson SiliconInsight in the LV Flow](#)” in the *Managing Mentor Graphics Tesson Software* for complete information and instructions.

Running Tesson SiliconInsight Desktop

You invoke Tesson SiliconInsight Desktop with the following runtime options on the Linux command line:

```
tesson -siliconinsight -desktop \
[-cable <olimex_arm_usb_ocd | flyswatter2 | signalizerSP | signalizerH2 |
 | signalizerSHA40 | signalizerH4 | signalizer | jtagkey>] \
[-lvdb <LVDBName> \
-pinmapFile <pinmapFileName> \
-configFile <testConfigFileName>] | [-lvpd <LVPDName> ] | [-tclshOnly] \
[-numberOfSites <siteCount> ] [-bondingOption <bonding_option>]
```

SID may be started in one of these modes:

1. GUI mode with LVDB using the -lvdb option.
2. LVPD mode with -lvpd option and a full Tcl shell for interactive interface.
3. Plain Tcl shell where the user can combine SVF and Tcl commands to design a full test program.

When running with LVPD or Tcl shell, you need to have a file named .si.config located at the user's home directory that contains the following three lines for the interactive Tcl shell to pop up:

```
configure useTkcon 1
configure showTkcon 1
configure iconifyTkcon 0
```

The valid option flag values are as follows:

- **-cable** <olimex_arm_usb_ocd | flyswatter2 | signalizerSP | signalizerH2 | signalizerSHA40 | signalizerH4 | signalizer | jtagkey> — specifies what type of cable (i.e., adaptor) is used. If none is specified, jtagkey (from Amontec) would be the default.

Note

 The literals for the **-cable** switch are case sensitive, and you must enter these literals as shown.

- **-lvdb** <LVDBName> — specifies the path to the LVDB. This is an optional argument, as the LVDB can be specified from the Tesson SiliconInsight Desktop GUI as well.
- **-pinmapFile** <pinmapFileName> — specifies the path to the Pin Map file. If you are using an asynchronous clock, see “[Asynchronous Clock Setup](#).” If using JTAGKey cable only the TAP pins must be mapped. The rest of the pins of the device must be explicitly declared as un-contacted (i.e., do not remove them from the pin map file).

If using Signalyzer, there are up to 16 pins may be mapped including the TAP pins. The rest of the pins must be explicitly declared as not contacted.

- **-configFile <testConfigFileName>** — specifies the path to the test configuration file. This is an optional argument, as the configuration file can be specified from the Tessian SiliconInsight Desktop GUI as well.
- **-lvpd <LVPDName>** — specifies the path to the SID LVPD to be used
- **-numberOfSites <siteCount>** — specifies the number of sites to be tested in parallel. Please refer to application note *Multi-Site Testing Using Silicon Insight Desktop* for more detail.
- **-tclShOnly** — instructs SID to just start a plain Tcl shell. The user may use the Tcl shell interactively to design and run full test programs using SVF and Tcl commands.
- **-bondingOption <bonding_option>** — Specifies one of the bonding options, as they appear in the *tcm* file, when the LVDB has multiple bonding options.

For additional information, refer to “[Diagnosing Device Failures](#)” for details about using GUI interactive Tessian SiliconInsight.

Asynchronous Clock Setup

The asynchronous clock setup is dependent on whether or not you declare a pin map file at tool start as follows:

- If you start the tool without a pin map file, the Tessian SiliconInsight Desktop sets the asynchronous clocks to OFF.
- Conversely, if you start the tool with a pin map file (-pinmapFile <pinmapFileName>), the Tessian SiliconInsight Desktop sets the asynchronous clocks to ON, provided that the clock pins are un-contacted.

Multi-Site Testing Using Tessian SiliconInsight Desktop

Tessian SiliconInsight Desktop currently supports multi-site testing using the following adaptors manufactured by Xerve Technologies Inc:

- [Multi-Site Testing with Signalyzer SP](#)
- [Multi-Site Testing with Signalyzer](#)

Multi-Site Testing with Signalyzer SP

You can use each Signalyzer SP adaptor to test up to 61 sites in parallel. Automatic diagnosis of failures may also be accomplished one site at a time. To specify a multi-site environment for Signalyzer SP, you must create a pin map file and hardware definition file.

Creating the Tesson SiliconInsight Pin Map File for Signalyzer SP

You configure multi-site testing by creating a pin map file, which specifies the mapping of the pins for the master site (specifically, site 1) only.

You subsequently create a hardware definition file (see “[Creating a Hardware Definition File for Signalyzer SP](#)”) to list all of the Signalyzer SP adaptors used. You can have more than one adaptor to support testing of more than 61 sites in parallel.

[Figure 8-15](#) shows an example Signalyzer SP pin map file:

Figure 8-15. Sample Tesson SiliconInsight Pin Map File for Signalyzer SP

```
PinMap (ROUTER) {  
    Pins {  
        // <design name> : <ATE name> <Tester channeltype>;  
        CLKA : -;  
        TDI : P0 ctl;  
        TRST : -;  
        TCK : P1 ctl;  
        TMS : P5 ctl;  
        TDO : P3 obs;  
        DATA_IN[7] : -;  
        DATA_IN[6] : -;  
        DATA_IN[5] : -;  
        DATA_IN[4] : -;  
        DATA_IN[3] : -;  
        DATA_IN[2] : -;  
        DATA_IN[1] : -;  
        DATA_IN[0] : -;  
        CTRL_IN[7] : -;  
        CTRL_IN[6] : -;  
        CTRL_IN[5] : -;  
        CTRL_IN[4] : -;  
        CTRL_IN[3] : -;  
        CTRL_IN[2] : -;  
        CTRL_IN[1] : -;  
        CTRL_IN[0] : -;  
        ENABLE_MEM : -;  
    }  
}
```

Creating a Hardware Definition File for Signalyzer SP

In the HW definition file, you must define the Signalyzer SP using the following syntax:

```
DIGITAL_IO XVERVE_SIGNALYZER_SP IO:<Serial No.> P0 P1 P2 .....P63
```

[Figure 8-16](#) shows an example hardware definition file for Signalyzer SP.

Figure 8-16. Sample Signalyzer SP Hardware Definition File

```
VERSION 1.0
# Type of adaptor Name:SN List of pins
#-----
DIGITAL_IO XVERVE_SIGNALYZER_SP IO:0100282 P0 P1 P2 .....P63
```

The master site is considered site 1 and TDO for the subsequent sites you assign sequentially to unused pins starting from P0.

For the example pin map file above, the site No.'s is as follows:

Site	TDO pin
====	=====
1 master)	P3
2	P2
3	P4
4	P6
5	P7
6	P8
.	.
.	.
.	.
61	P63

If you want to use more Signalyzer SP adaptors to test more than 61 DUTs in parallel, you specify the adaptors in the HW definition file as follows:

```
VERSION 1.0
# Type of adaptor Name:SN List of pins
#-----
DIGITAL_IO XVERVE_SIGNALYZER_SP IO1:0100282 P0 P1 P2 .....P63
DIGITAL_IO XVERVE_SIGNALYZER_SP IO2:0100295
DIGITAL_IO XVERVE_SIGNALYZER_SP IO3:0100303
```

For example, assume the pin map file for the same DUT looks as follows because you need to control additional pins (specifically, CTRL_IN[0-7]) to pre-condition the device (i.e. preamble) for testing:

```
PinMap (ROUTER) {
    Pins {
        // <design name> : <ATE name> <Tester channeltype>;
        CLKA : -;
        TDI : P0 ctl;
        TRST : -;
        TCK : P1 ctl;
```

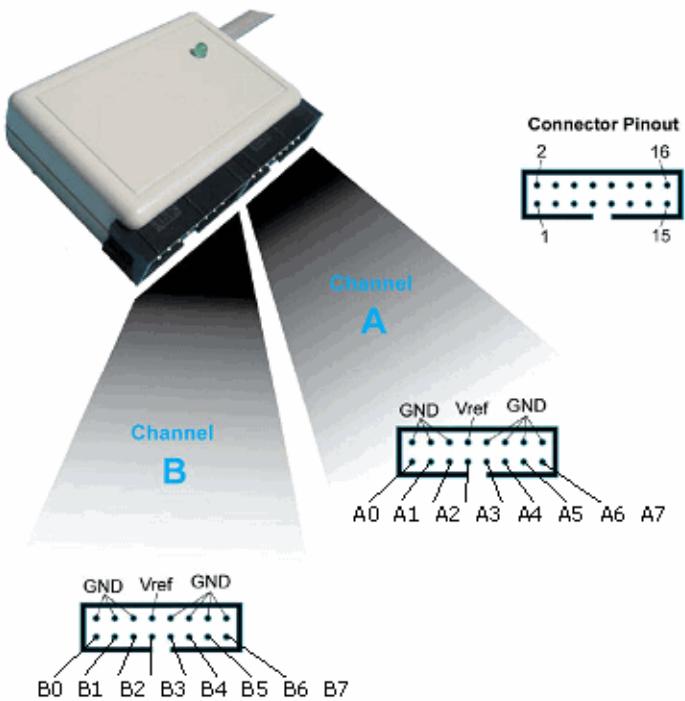
```
TMS : P5 ctl;
TDO : P3 obs;
DATA_IN[7] : -;
DATA_IN[6] : -;
DATA_IN[5] : -;
DATA_IN[4] : -;
DATA_IN[3] : -;
DATA_IN[2] : -;
DATA_IN[1] : -;
DATA_IN[0] : -;
CTRL_IN[7] : P2 ctl;
CTRL_IN[6] : P4 ctl;
CTRL_IN[5] : p6 ctl;
CTRL_IN[4] : p7 ctl;
CTRL_IN[3] : p8 ctl;
CTRL_IN[2] : p9 ctl;
CTRL_IN[1] : p10 ctl;
CTRL_IN[0] : p11 ctl;
ENABLE_MEM : -;
}
}
```

This means that due to the additional 8 used pins, you can only test 53 DUTS in parallel per Signalizer SP. Because you are using 3 adaptors, we can test 159 (that is, 3X53) DUTs in parallel.

Multi-Site Testing with Signalizer

The Signalizer tool offers two independent configurable channels: *Channel A* and *Channel B*. Each channel can be individually configured, and each makes use of a dedicated *Vref* pin to set the logic level for the channel (1.2 – 5.5 VDC). Pinouts for the two channels are shown in [Figure 8-17](#).

Figure 8-17. Signalizer Channel Pinouts



Multi-site testing is accomplished by creating a pin map file which specifies the mapping of the pins for the master site (i.e., Site 1). Then, a hardware definition file must be created to list all Signalizer adaptors used.

Creating the Tesson SiliconInsight Pin Map File for Signalizer

Each Signalizer adaptor will support up to 10 sites (5 on *Channel A* and 5 on *Channel B*). This is assuming that TAP input pins might be shared for all sites and pins left over in a Signalizer channel might be used as TDO for the additional sites.

You must only specify the pin mapping for *Site 1* (i.e., the master site). The master site pins (i.e., 4 TAP pins) must use the pins (A0-A3) of the first (according to the Hardware Definition file) Signalizer adaptor. You can map *TMS*, *TDI*, *TDO*, and *TCK* to Pins A0-A3. Then the rest of the pins leftover in *Channel A* (i.e., A4-A7) will be assumed to be *TDO*'s from *Sites 2, 3, 4, and 5*. So, *Channel A* will support 5 sites. *Channel B* will be assumed to have the exact copy of the *Channel A* supporting the next 5 sites (i.e., 6, 7, 8, 9, and 10).

A sample Tesson SiliconInsight Desktop pin map file is shown in [Figure 8-18](#).

Figure 8-18. Sample Tesson SiliconInsight Pin Map File for Signalizer

```
PinMap (ROUTER) {
```

```

Pins {
    // <design name> : <ATE name> <Tester channeltype>;
    CLKA : -;
    TDI : A0 ctl;
    TRST : -;
    TCK : A2 ctl;
    TMS : A1 ctl;
    TDO : A3 obs;
    DATA_IN[7] : -;
    DATA_IN[6] : -;
    DATA_IN[5] : -;
    DATA_IN[4] : -;
    DATA_IN[3] : -;
    DATA_IN[2] : -;
    DATA_IN[1] : -;
    DATA_IN[0] : -;
    CTRL_IN[7] : -;
    CTRL_IN[6] : -;
    CTRL_IN[5] : -;
    CTRL_IN[4] : -;
    CTRL_IN[3] : -;
    CTRL_IN[2] : -;
    CTRL_IN[1] : -;
    CTRL_IN[0] : -;
    ENABLE_MEM : -;
}
}

```

Creating a Hardware Definition File for Signalyzer

SID supports the use of multiple Signalyzer Adaptors. The number of adaptors required will depend on the number of sites to be tested. All adaptors must be specified using their serial numbers. The order of the adaptors specified in the Hardware Definition file determines the sites they support. The first adaptor will support the first group (including the master site which is *Site 1*).

An example of a multi-site Hardware Definition file is shown in [Figure 8-19](#).

Figure 8-19. Sample Signalyzer Hardware Definition File

VERSION 1.0		Type of adaptor	Name:SN	List of pins
#-----				
DIGITAL_IO	A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7	XVERVE_SIGNALYZER	IO1:0100282	A0 A1 A2 A3 A4
DIGITAL_IO		XVERVE_SIGNALYZER	IO2:0100265	
DIGITAL_IO		XVERVE_SIGNALYZER	IO3:0100315	

Assuming every site uses only the TAP pins with the pin map file specified in [Figure 8-18](#), the first adaptor (i.e., *IO1*) will support the first 10 sites (i.e. 1-10), the second adaptor (i.e. *IO2*) will support *Sites 11-20*, and, finally, the third adaptor (i.e., *IO3*) will support *Sites 21-30*.

The list of pins might only appear for the first card.

Additional IO Pins

If additional I/O pins, other than TAP pins, are to be used, they must be connected to Signalyzer pins A4 through A7, allowing a maximum of 4 additional pins. Any Signalyzer pins not used in the range A4-A7 will be assumed to be additional *TDO* pins for subsequent sites.

As an example, assume the pin map file shown in [Figure 8-20](#) is specified.

Figure 8-20. Example Signalyzer Pin Map File with Additional User Pins Specified

```
PinMap(ROUTER) {
    Pins {
        // <design name> : <ATE name> <Tester channeltype>;
        CLKA : -;
        TDI : A0 ctl;
        TRST : -;
        TCK : A2 ctl;
        TMS : A1 ctl;
        TDO : A3 obs;
        DATA_IN[7] : -;
        DATA_IN[6] : -;
        DATA_IN[5] : -;
        DATA_IN[4] : -;
        DATA_IN[3] : -;
        DATA_IN[2] : -;
        DATA_IN[1] : -;
        DATA_IN[0] : -;
        CTRL_IN[7] : -;
        CTRL_IN[6] : -;
        CTRL_IN[5] : -;
        CTRL_IN[4] : -;
        CTRL_IN[3] : -;
        CTRL_IN[2] : -;
        CTRL_IN[1] : -;
        CTRL_IN[0] : A7 ctl;
        ENABLE_MEM : A5 ctl;
    }
}
```

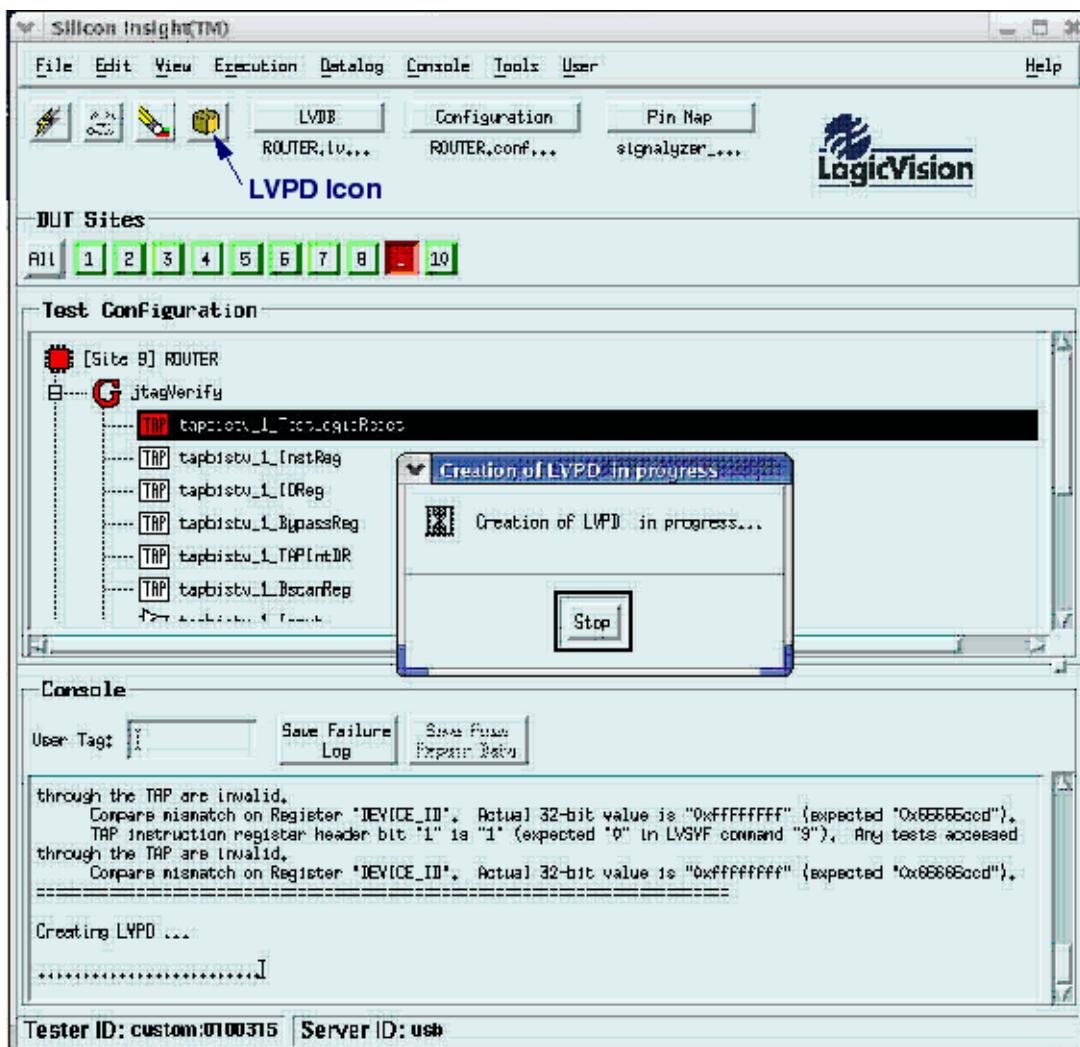
Signalyzer *Channel A* Pins A0-A7 will support 3 sites, the master site (i.e., *Site 1*) and two other sites (*Sites 2* and *3*) with *TDO* of *Site 2* connected to *Pin A4* and *TDO* of *Site 3* connected to *A6*. Signalyzer *Channel B* will then support *Sites 4-6*, where *Site 4* is connected to *Pins B0-B3, B5, and B7*, while *Sites 5* and *6* will reuse input pins from *Site 4* and their *TDO* pins will be *Pins B4* (for *Site 5*) and *B6* (for *Site 6*).

Generating a SiliconInsight Desktop LVPD

You might want to send a “sanitized” copy of the LVDB to a third party location to be used by Tessent SiliconInsight Desktop. For those occasions, you can generate and use an Tessent SiliconInsight Desktop LVPD (Mentor Graphics Production Database) which will have no design-specific data. The limitation of a Tessent SiliconInsight Desktop LVPD is that it does not support logic diagnostics.

Once the test configuration (i.e., test flow) to be used in the production environment has been created and validated, an LVPD can be created by clicking on the *LVPD* icon in the Tessent SiliconInsight Desktop GUI (Refer to [Figure 8-21](#)). The LVPD will be generated in a new package (a directory with extension *.lvpd*). This directory will contain a sanitized copy of the LVDB, the configuration file, and the pin map file.

Figure 8-21. Generating an LVPD from the Tessent SiliconInsight Desktop



To invoke Tessent SiliconInsight Desktop with an LVPD (rather than with an LVDB), execute the following command:

```
tessent -siliconinsight -desktop -lvpd <path to SID LVPD>
```

Optionally, a specific output directory can be specified using the **-outdir** runtime option.

Chapter 9

Setting Up Tesson SiliconInsight ATE

This chapter provides step-by-step instructions on how to use the Tesson SiliconInsight software with different ATE platforms. This chapter includes reference information about the relevant API calls, runtime options, and files that are used in Tesson SiliconInsight ATE.

Chapter topics follow this sequence:

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Introducing Tesson SiliconInsight ATE

Embedded test is a natural evolution of two distinct test approaches—External ATE and the conventional Design for Test (DFT).

Built on conventional DFT approaches such as scan and Built-In Self-Test (BIST), embedded test integrates the high-speed and high-bandwidth portions of the external ATE directly into the ICs. This integration facilitates chip-, board-, and system-level tests, diagnosis, and debug. Embedded test consists of user-configurable IP (intellectual property), in the form of design objects delivered as Register Transfer Language (RTL) soft cores. These IP design objects implement pattern generators (either random or algorithmic), results' compression, collection of diagnostic data, and precision timing for at-speed delivery of the tests.

With the right software application, embedded test is particularly helpful during silicon debug and bring-up. However, it can also be effectively used to replace the conventional WGL¹ based

manufacturing flow. In the conventional manufacturing flow (Refer to [Figure 9-1](#)), WGL patterns are generated by the design engineers and are handed off to the test engineer. The test engineer then spends considerable effort to translate and compile the WGL patterns into the ATE platform specific binary patterns. These patterns are then applied during the production flow via the test program to perform the Go/No-Go testing.

When the Go/No-Go testing is performed on the ATE, a faulty device under test generates miscompares, which are reported in terms of the cycle numbers and the failing pins in the tester datalog. However, this miscompare information does not provide any further details such as the failing embedded memory or logical block. Even though the device is capable of providing richer diagnostic information due to the embedded test, the tester software is incapable of extracting this information. In order to extract this information from the failing pin datalog, a test engineer often must consult the design engineer and devise complex and time-consuming programs to map the failures to the design data.

Knowing precisely which memory or which logical block and under what test conditions is causing the yield loss is extremely valuable during the yield ramp. This data can be used for setting the margins on the failing blocks only instead of affecting the entire device. The same data is also helpful in the production stage to be used in yield monitoring or for failure analysis.

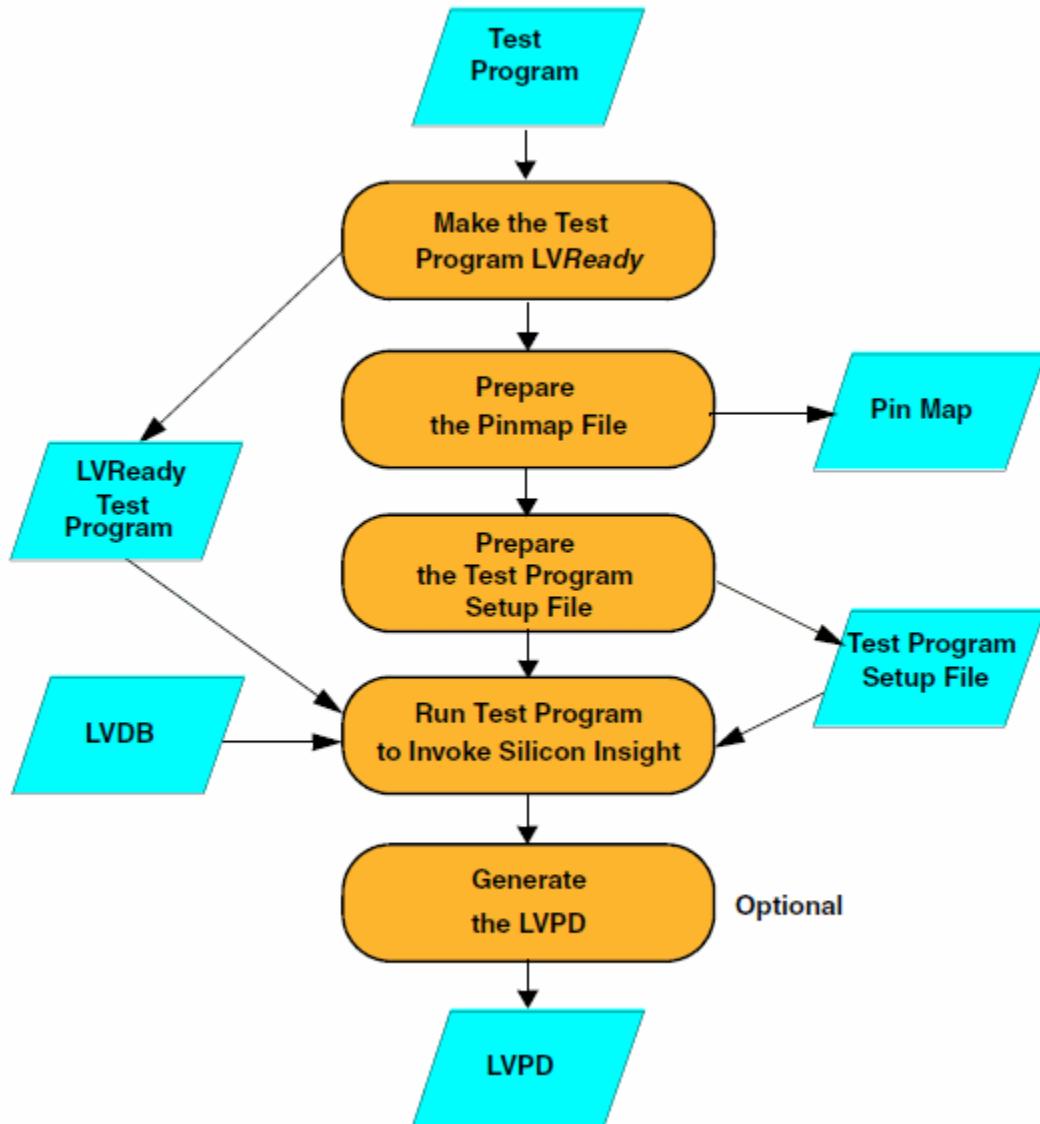
Tesson SiliconInsight ATE Setup Flow

The Tesson SiliconInsight ATE setup flow consists of the following four steps:

1. ***Making Your User Test Program LVReady***—During this step, you modify your test program to API calls that are specific to Tesson SiliconInsight.
2. ***Preparing the Pin Map File***—The Pin Map File specifies the mapping between the design pin names and the device pin names (also known as the *package* pin names). During this step, you will copy the starter Pin Map file template from the LVDB and modify this file in a text editor as needed.
3. ***Preparing the Test Program Setup File***—In this step you set up the Tesson SiliconInsight runtime environment using the *Test Program Setup (.eta_tp_setup)* file, so that the LVReady test program can interact with the Tesson SiliconInsight software.
4. ***Running Test Program to Invoke Tesson SiliconInsight***—At this point, you are ready to run your test program to invoke the Tesson SiliconInsight software.

1. Though only WGL is mentioned, the discussion applies equally to the STIL patterns.

Figure 9-1. Steps of the Tesson SiliconInsight ATE Setup Flow



In addition, optionally you can generate the LVDB. Once Tesson SiliconInsight is up and running, you have the option of creating an LVPD for use in Production Datalogging. For details on the LVPD, refer to Chapter 10, “[Setting Up Tesson SiliconInsight Production Datalogging](#).”

To create an LVPD, you simply need to click on the tool bar button **Create LVPD** from the Tesson SiliconInsight GUI as illustrated in [Figure 9-2](#).

Figure 9-2. Generating an LVPD from the Tessent SiliconInsight GUI



When you click on the **Create LVPD** button on the tool bar, a dialog box will prompt you for the location of the LVPD on the file system. Always choose a location which is either in the directory called *lv_setup* in the same directory as the Test Program (i.e. if the Test Program is a single file) or in the Test Program directory.

Making Your User Test Program LVReady

In *Setup Step 1* for Tessent SiliconInsight ATE, you make the user test program LVReady by editing the program to call one or more Tessent SiliconInsight APIs. In most cases, you need to invoke just two APIs at the appropriate point in your test program.

You must call the Tessent SiliconInsight API [ETAStart\(\) API](#) from your test program.

Note  Teh APIs might not be directly usable in your test program, depending on the ATE platform. For example, on the Agilent 93000 platform running SmarTest, the ETAStrt() API has to be invoked via a user procedure attached to a Flow Node. Mentor Graphics has already integrated the ETAStrt() and ETAExecuteStep() APIs into the test program flow for all LVReady ATE platforms. For detailed ATE platform-specific instructions, refer to the section “[User Test Program Changes for Specific Platforms](#).”

[ETAStart\(\) API](#)

In order to run with Tessent SiliconInsight from your test program, you must insert the *ETAStart()* API into the User Test Program to enable it to invoke Tessent SiliconInsight.

The *ETAStart()* API starts the Tessent SiliconInsight sub-system. This API uses the data in the *.eta_tp_setup* file, which is specified as an input to the API, to launch the Tessent SiliconInsight

server and initiate communication between the Test Program and the Tesson SiliconInsight server. You need to provide a Tesson SiliconInsight Test Program Setup file name while calling this API, even if the file does not exist yet during the Test Program file edit process.

This API should be placed in your User Test Program so that it is called when the Test Program is initializing, after the device has been powered up.

Note

 When you operate the ATE through the Windows platform, you must use a runtime library to provide real-time communication between Windows and Linux. Tesson SiliconInsight supports the Distinct Windows-based RPC system, versions RPC-46-RT and RPC-63-RT.

The Default Test Step File

The default test step file, *default.testStep*, is generated when ETVerify creates the Mentor Graphics database (LVDB). This file contains all test steps in the default test configuration file, *default.config_eta*, generated by the ETVerify tool. Use this file during test program generation to extract the test step names from this file and add support in the test program to execute and diagnose each test step in the default test configuration.

[Figure 9-3](#) provides an example of the *default.testStep* file populated with test steps for BIST controllers.

Figure 9-3. Example *default.testStep* File

```
-----  
// This file created by: embeddedTestVerify  
// Software version: 6.0a SP2 Build 20070226.330  
// Created on: 03/12/07 13:34:55  
-----  
tapbistv_1_TestLogicReset  
tapbistv_1_InstReg  
tapbistv_1_IDReg  
tapbistv_1_BypassReg  
tapbistv_1_TAPIntDR  
tapbistv_1_BscanReg  
tapbistv_1_Input  
tapbistv_1_Sample  
tapbistv_1_HighZ  
tapbistv_1_OutputClamp  
membistv_1  
GainForceDown  
GainForceUp  
LockRangeMaxFreq  
LockTimeFromMaxFreq  
LockRangeMinFreq  
LockTimeFromMinFreq  
JitterLongTerm  
multi_asyncTest_retentionTest_1
```

```
multi_asyncTest_retentionTest_2
multi_asyncTest_retentionTest_3
logicbistv_1
logicbistv_2
logicbistv_3
```

User Test Program Changes for Specific Platforms

This section details the changes that you must make to your User Test Program on the following specific LVReady ATE Platforms:

- [Teradyne ATE \(IG-XL\)](#)
- [Verigy ATE \(SmarTest\)](#)
- [LTX ATE](#)

Teradyne ATE (IG-XL)

This section describes how to prepare an IG-XL Test Program to use Tesson SiliconInsight software to test and diagnose devices on the Teradyne UltraFlex (or compatible) ATE Platforms running the IG-XL software.

Prerequisites

Before modifying the Test Program on a Teradyne ATE, you must ensure the following:

- The Tesson SiliconInsight software LV2005 or higher is installed on a Solaris (version 7 or higher) host. The Tesson SiliconInsight software installation directory must be accessible by the Test Program (TP) host machine running IG-XL (i.e. tester). This Tesson SiliconInsight software installation directory will be referred to as `<ETA_INSTALL_DIR_ON_TP_HOST>` in the subsequent steps.
- A third-party vendor software package from *Distinct RPC* must have been installed on the TP host machine. This is required so that the Solaris based Tesson SiliconInsight software and Windows-based Test Program can communicate with each other.
 - Purchase, download, and install “Distinct ONC RPC / XDR for C or C++” Toolkit version 4.0 from www.distinct.com.
- A third-party vendor software package for Xserver for the Windows platform must have been installed on the TP host machine. This is required so that Solaris-based Tesson SiliconInsight GUI window can be displayed on the Windows-based TP host.
 - For example, you can install any Xserver for Windows such as Exceed from the Hummingbird Corp.
 - Make sure you set the DISPLAY environment variable appropriately on your TP host.

- A Tesson SiliconInsight Tester File map has been created and installed at a central location, and the user environment variable **ETA_TESTER_FILE** on the TP host machine is set to point to that file. An example of this file can be found in the following location relative to the Tesson SiliconInsight installation directory:

```
<ETA_INSTALL_DIR_ON_TP_HOST>\share\SiliconInsight\examples\  
LV_FPGA_demo1\Teradyne\lv_fpga_igxl\ETATesterFile.map
```

When modifying the Tesson SiliconInsight Tester File, the valid range for tester RPC addresses is 0x20100201 - 0x2FFFFFFF.

- Add the following directory path to the PATH environment variable on the test program host machine:

```
<ETA_INSTALL_DIR_ON_TP_HOST>\share\SiliconInsight\ATE\  
Teradyne\lib\win-x86
```

Contact Mentor Graphics Support personnel for further help with any of the above steps. You must follow the above steps and validate the Tesson SiliconInsight runtime environment before proceeding further.

Modifications to the Test Program

You must make the following changes to the IG-XL Test Program to make it LVReady:

Add Tesson SiliconInsight Timing Set

To add Tesson SiliconInsight timing set to your TimeSheet (TSB tab), follow these steps. The Timing set *must* be named as **ETA_TS**.

- Set **Timing Mode** to “Dual”.
- TimeSet ETA_TS will include all of the device signals (all those defined in ChannelMap Sheet) and will be set as follows for all pins:

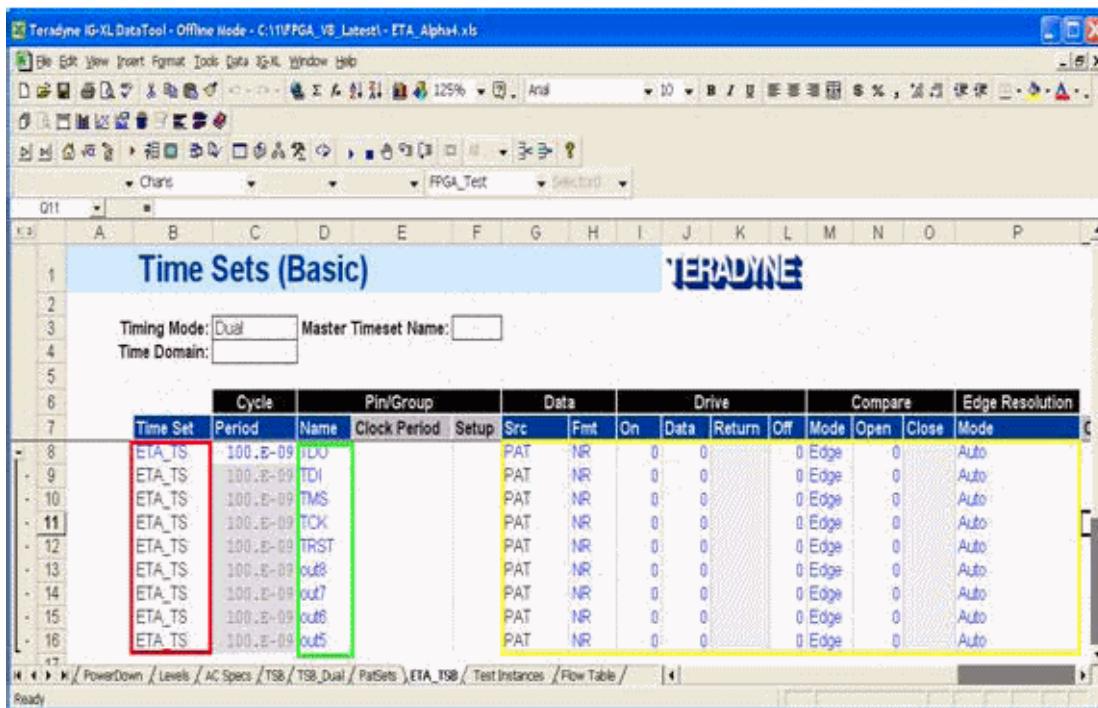
```
Data Src: Pat
Data Fmt: Fmt
Drive On: 0
Drive Data: 0
Drive Off: 0
Drive Return: 0
CompareMode: Edge
Compare Open: 0
Compare Close: (Grayed Out)
Mode: Machine (only for UltraFlex and Flex)
```

Note



Some fields might not be required (i.e. grayed out depending on the type of the signal).

Figure 9-4. Tessent SiliconInsight Timing Set

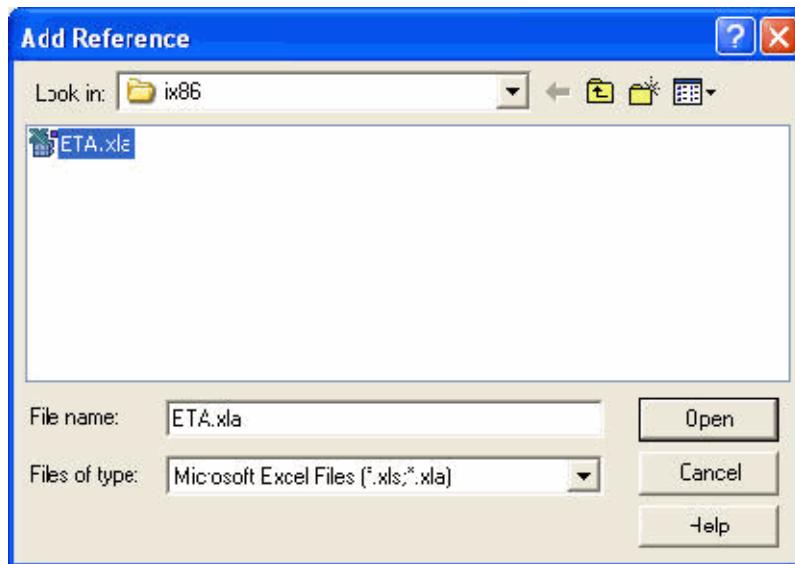


“Refer” to the Tessent SiliconInsight Add-in

To refer to the Tessent SiliconInsight add-in, follow these steps:

1. From IG-XL press **Alt-F11** to bring up the Microsoft Visual Basic work environment.
2. Click on any sheet under the Test Program VBA project (i.e. <test program>.xls) and from the menu **Tools** click on menu item **References** to bring up the References dialog window.
3. Click on **Browse** and navigate to the following directory
<ETA_INSTALL_DIR_ON_TP_HOST>\share\SiliconInsight\ATE\
Teradyne\lib\win-x86 and Open the add-in file:
 - o ETA.xla or ETA_ULTRAFLEX.xla for an UltraFlex job
 - o ETA_FLEX.xla for a Flex job
 - o ETA_J750.xla for a J750 job

Figure 9-5. Adding Reference to Tessian SiliconInsight Add-in



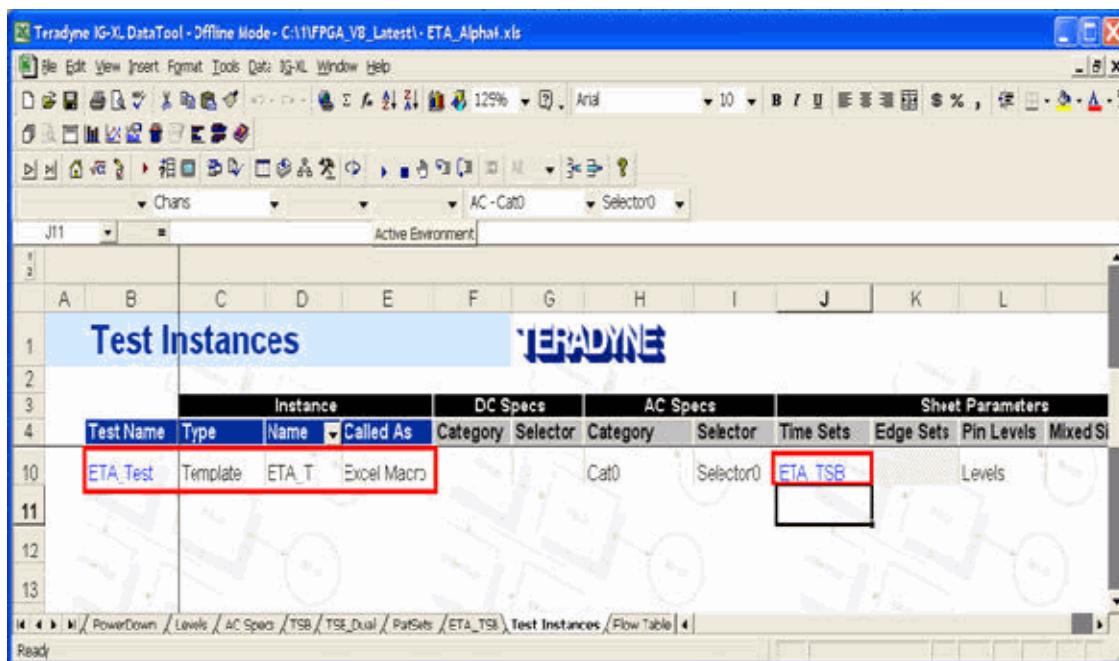
4. Make sure that the add-in *EmbeddedTestAccess* is clicked in the references list. This will also appear as a VBA project in the VBA Project list.

Add a Tessian SiliconInsight Test Instance

To add a Tessian SiliconInsight test instance, follow these steps:

1. Select the **Test Instances** sheet from IG-XL by clicking on the **Test Instances** tab at the bottom of the IG-XL main window.
2. In the **Test Name** field for the Tessian SiliconInsight test choose a name (for example, *ETA_Test*).
3. In the **Type** field, choose *VBT for UltraFlex/Flex. Template for J750*.
4. In the **Name** field, type in *ETA_T*.
5. In the **Called As** field, choose **Excel Macro** for J750. It is greyed out on *UltraFlex/Flex*.
6. For DC Spec, choose the *Specs* you want to run with.
7. For AC Specs, choose the Timing Sheet which contains the Timing Set (i.e., *ETA_TS*) added for Tessian SiliconInsight in the previous steps.

Figure 9-6. Tessent SiliconInsight Test Instance



Add Tessent SiliconInsight Test to the Flow Table

To add a node to execute the Tessent SiliconInsight test just created in the Flow Table, follow these steps:

1. Click on the **Flow Table** tab in the bottom of the IG-XL main window to bring up the Flow Table.
2. Insert a new row in the flow.
3. Select **Test** in the **Opcode** field.
4. Type in the name of the Tessent SiliconInsight test created before (i.e. *ETA_Test*) in the **Parameter** field.
5. Click the right-mouse-button on the **Parameter** field, click on the **Edit** sub-menu, and choose **Instance** to edit the parameters for the Tessent SiliconInsight test.
6. The Tessent SiliconInsight test dialog box will pop up where you type in the path (relative or absolute) to the Tessent SiliconInsight Setup file created in previous steps.
7. Now Tessent SiliconInsight test is ready for execution.

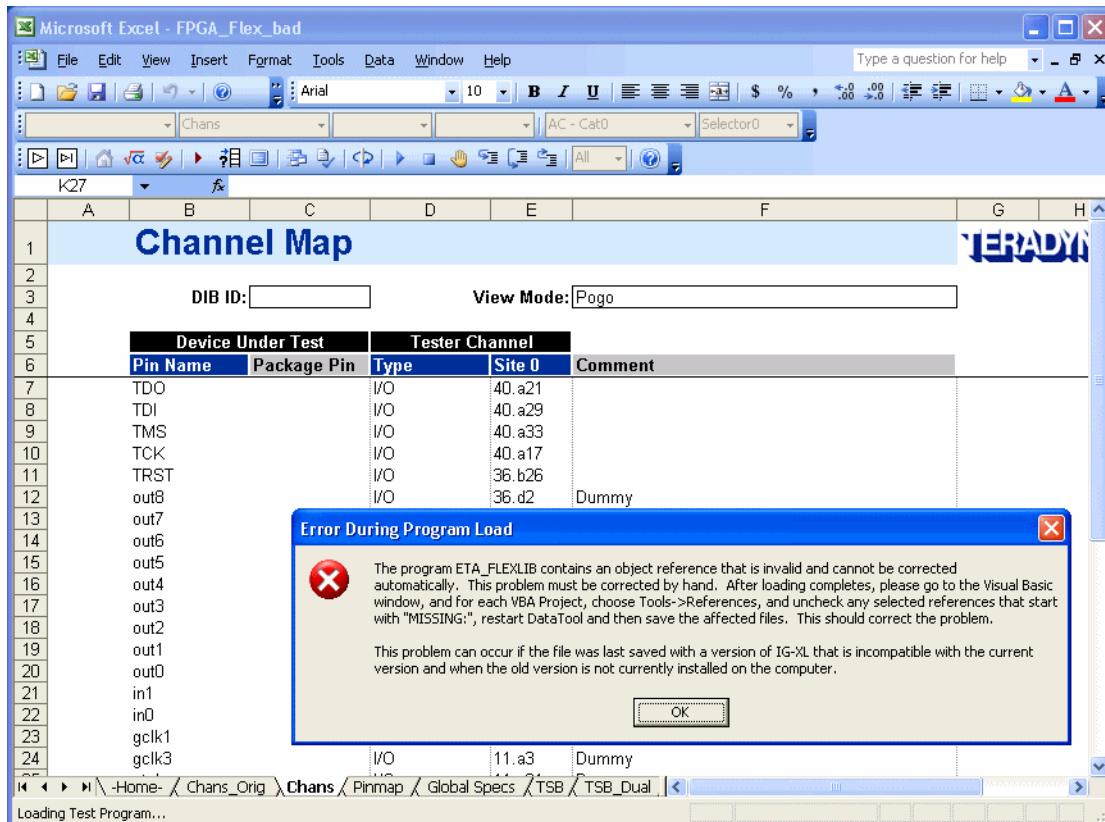
Figure 9-7. Tessent SiliconInsight Test in the Job Test Flow

Migrating an IG-XL Test Program to a Newer Release

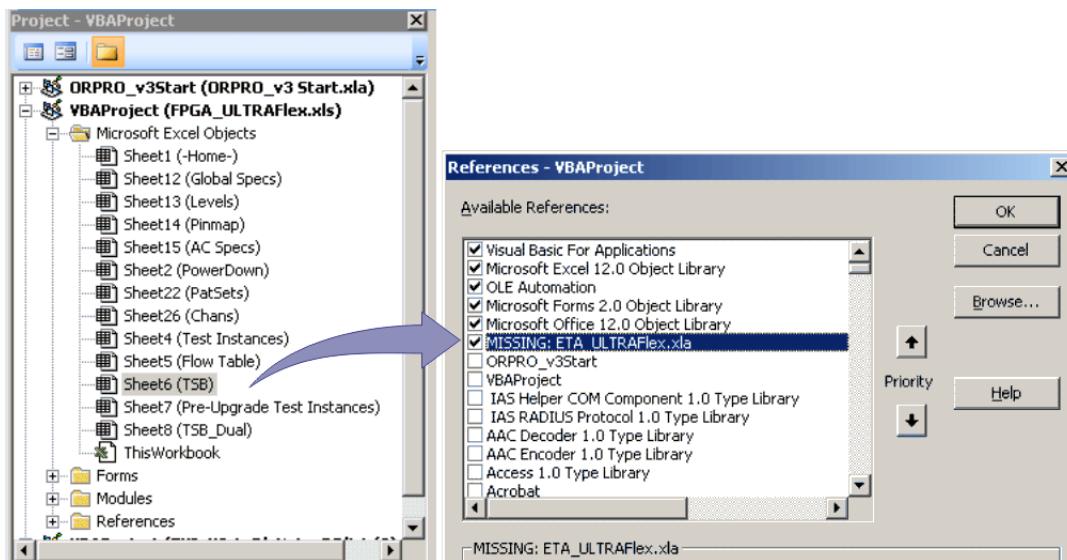
If a test program was generated in a previous version of IG-XL, for example, 7.10, then loading it into a new version of IG-XL, such as 7.30, will cause error. This is due to the fact that the .xla file contains object references that are not available in the current IG-XL (7.30) version.

Follow the steps outlined in the ETA_FLEXLIB dialog box, as shown in [Figure 9-8](#). The steps are repeated here for your convenience:

Figure 9-8. Error During IG-XL Test Program Load

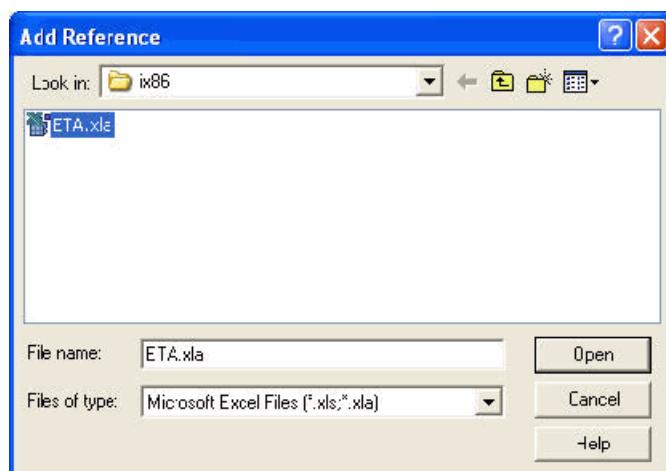


1. Open the Microsoft Visual Basic window within your Excel session (press **Alt-F11**).
2. Click on any sheet under the Test Program VBA project (that is, <test program>.xls) and from the menu item **Tools > References** to bring up the References dialog window.



3. Unselect any of the checked references that start with “MISSING:” and close the References dialog box using **OK**.
4. Click on **Browse** and navigate to the following directory
`<ETA_INSTALL_DIR_ON_TP_HOST>\share\SiliconInsight\ATE\Teradyne\lib\win-x86` and Open the add-in file:
 - o ETA.xla or ETA_ULTRAFLEX.xla for an UltraFlex job
 - o ETA_FLEX.xla for a Flex job
 - o ETA_J750.xla for a J750 job

Refer to the Tessian SiliconInsight add-in, and follow these steps:



5. Make sure that the add-in *EmbeddedTestAccess* is clicked in the references list. This will also appear as a VBA project in the VBA Project list.
6. *The Teradyne IG-XL add-in will pop-up a dialog -- Info requested.*
7. De-select any missing library, then close the reference list by choosing **OK**.
8. Reload the test program. Select a sheet (spreadsheet tab).
9. Close the Excel **Tools > References** window so that Excel will then update the .xla file, and the .xla file's related libraries will then reference the new IG-XL version (7.30 in this example).

Verigy ATE (SmarTest)

This section describes how to prepare a SmarTest Test Program to use Tessian SiliconInsight software to test and diagnose devices on the Agilent 93K ATE Platform.

Prerequisites

Before modifying the Test Program on an Agilent ATE, you must ensure that the Tessonnt SiliconInsight software Version LV2005 or higher has been installed on your system and is accessible by the Test Program host.

If you have questions about this step, or if the Test Program cannot access the Tessonnt SiliconInsight software, refer to *Installation and Release Notes LV2005, Version 6.0a SP02*.

Modifications to the Test Program

You must make the following changes to the Agilent Test Program:

1. Run the *makeLVReady_93K* script on your test program to make it LVReady.
2. Add specific test suites to the testflow. For detailed instructions, refer to “[TestFlow](#).”

Make TP LVReady

You will run the script

`<INSTALL_PATH>/share/SiliconInsight/Agilent/bin/makeLVReady_93K` and pass the test program directory as argument to make the test program LVReady. This tool enhances the user test program as follows:

- Updates the user timing file with the timing waveforms used by Tessonnt SiliconInsight
- Adds the Tessonnt SiliconInsight User Functions file (*lv_system_calls.c*) to *userproc_libs* directory of the test program

Run *makeLVReady_93K*

The tool syntax is as follows:

```
makeLVReady_93K -timing <user timing file>
-replaceTiming -pinConfig <user configuration file> <user test program
directory>
```

The above command will update the timing file *<user timing file>* in the directory *<user test program directory>/timing* with Tessonnt SiliconInsight waveform. The new timing file will replace the old one (i.e., *-replaceTiming* command). The user pin configuration file *<user configuration file>* in the directory *<user test program directory>/configuration* will be used to create the Tessonnt SiliconInsight waveforms.

 **Note** If *makeLVReady_93K* is executed without any arguments, the man page for it is displayed. This man page describes all available commands and functions.

Compile Tesson SiliconInsight User Functions

The following example describes the changes that are required to the makefile for SmarTest 93K to compile the user functions in the file *lv_system_calls.c*:

```
ETA_INSTALL_DIR = <INSTALL_PATH>
```

Note

 The <INSTALL_PATH> points to the actual path where the Tesson SiliconInsight software is installed.

```
ETA_INCLUDE_DIR =
${ETA_INSTALL_DIR}/share/SiliconInsight/ATE/common/include
ETA_LIB_DIR =
${ETA_INSTALL_DIR}/share/SiliconInsight/ATE/Agilent/lib/hpux-hppa

PLATFROM = 93K
SRCS   = lv_system_calls.c
OBJS   = lv_system_calls.o
LDFLAGS = -L $(HP93000_ROOT)/hp83000/prod_com/C++/lib -
          L$(HP93000_ROOT)/hp93000/mix_sgn1/lib -L $(HP83000_ROOT)/com/lib -L
          $(HP93000_ROOT)/pws/lib -L${ETA_LIB_DIR} -leta_agilent_${PLATFROM}
HP93000_ROOT=/opy/hp93000/soc
```

Once the makefile is enhanced to compile the Tesson SiliconInsight user functions in addition to other user functions, it might be used as before to compile the user procedure library.

TestFlow

The testflow might be enhanced to add Tesson SiliconInsight nodes to start Tesson SiliconInsight and, optionally, add nodes to execute different test steps. For all Tesson SiliconInsight nodes in the flow, you must select ETA_SPEC (i.e., equation set #99) for the timing, appropriate levels, and any seed pattern.

Flow Node to Start/Initialize Using `start_eta`

You might add this test node in the flow and execute user procedure `start_eta` and pass the path to TP setup file to it. This node might be used to initialize Tesson SiliconInsight and pass control back to Tesson SiliconInsight GUI (if in Debug mode).

Flow Node to Execute a Step

You might add a node to execute a specific test step from the loaded Tesson SiliconInsight test configuration. This is done by calling `execute_step <teststep name>`. If `execute_step` is called without an argument, it will provide a list of test steps which can be executed.

Flow Node to Exit Tesson SiliconInsight Server

This node may be added to command Tesson SiliconInsight server to exit once all of the patterns are loaded (**exit_eta_server**). This is to free up computing resources on the Tesson SiliconInsight server host machine.

Flow Node to Save BIRA Data

This node might be added (usually at the end of the SmarTest test program flow) to save accumulated BIRA data for a given DUT in a file. **save_and_clear_bira_data <file name> <X-coordinate> <Y-coordinate>** will save/append the accumulated BIRA data for DUT at X and Y coordinate in the file *<file name>*.

Flow Node to Provide Help Instructions on All Available Tesson SiliconInsight User Functions

Node **eta_help** (with no arguments) might be executed to provide instructions and directions for all available Tesson SiliconInsight user functions, including the ones described in the previous sections.

Using the TestMethod instead of the UseProcedure — RHEL 3

You can use the TestMethod instead of the UseProcedure when you run SmarTest Version 4.3.6 or later on Red Hat Enterprise Linux 3.

To install the TestMethod for Tesson SiliconInsight, find the file *<ETA_INSTALL_PATH>/share/SiliconInsight/examples/LV_FPGA_demo1/Agilent/common/LV_TestMethod_lnx.tgz* and open (tar xzf) under your *<device_dir/TestMethod>* directory.

To build the TestMethod, open the makefiles of the TestMethod and modify the following variables:

- **ETA_INSTALL_DIR**: set to the absolute path to the Tesson installation root directory
- **ETA_LINK_LVPD_LIB**: set to 0

Then, build (or rebuild) the TestMethod in the regular SmarTest flow.

To use the SmarTest test flow, the methods are identical to the UseProcedure functions, and you can also refer to explanations about parameters in the TestMethod GUI.

Using the TestMethod instead of the UseProcedure — RHEL 5

You can use the TestMethod instead of the UseProcedure when you run SmarTest Version 6.5.2 or later on Red Hat Enterprise Linux 5.

To install the TestMethod for Tesson SiliconInsight, find the file `<ETA_INSTALL_PATH>/share/SiliconInsight/examples/LV_FPGA_demo1/Agilent/common/LV_TestMethod_lnx-el5.tgz` and open (tar xzf) under your `<device_dir/TestMethod>` directory.

To build the TestMethod, open the makefiles of the TestMethod and modify the following variables:

- `ETA_INSTALL_DIR`: set to the absolute path to the Tesson installation root directory
- `ETA_LINK_LVPD_LIB`: set to 0

Then, build (or rebuild) the TestMethod in the regular SmarTest flow.

To use the SmarTest test flow, the methods are identical to the UserProcedure functions, and you can also refer to explanations about parameters the in the TestMethod GUI.

LTX ATE

This section describes how to prepare an Envision Test Program to use Tesson SiliconInsight software to test and diagnose devices on the LTX ATE Platform.

Prerequisites

Before modifying the Test Program on an LTX ATE, you must ensure that the Tesson SiliconInsight software Version LV2005 or higher has been installed on your system and is accessible by the Test Program host.

Modifications to the Test Program

You add Tesson SiliconInsight to a virgin program (enVision program which does not include Mentor Graphics support). If you need to compile the patterns, perform the following steps:

- cd to the test program directory (directory with the .eva file)
- Execute the following command:
`epc -t VX500 -c <filename.eva>.`

Add ETASTart to Flow

You load the test program in enVision by performing these steps:

1. Start enVision

`$Launcher`

2. Press the **Program** button and select the .eva file for the test program to be loaded, and press **OK** to load the program.

3. After the program is loaded, execute the following shell command. Note that the *tcid* number is usually *31*. It is displayed in the BinTool on the window frame.

```
$LVCommand +C<tcid> AddETAStrat
```

This command will add a test called **ETAStrat** to the test program.

4. Bring up the FlowTool by clicking on the **Tools** menu and select **Flow** in the **Flow** submenu.

5. Add the test to the flow:

- o Right-click on the FlowTool and select the **NewNode/C++Test**. This will bring up a dialog box where you can select **ETAStrat** test. Select **OK** to add it to the flow.

Once the test is in the flow, connect the following:

- i. Port 0 to the **PASS** bin.
- ii. Port 0 of the previous test to the **ETAStrat** test. To select Port 0 of the previous test, left-click and drag the line onto the **ETAStrat** test.
- iii. Port 1 of **ETAStrat** to the **FAIL** bin in the flow.

6. Fill in some test program specific parameters in the **ETAStrat** test. To do this double-click on **ETAStrat**—this will bring up the **Test Tool**. In the **Test Tool**, right-click on **Spec Objects Cell** and select **FindMask**. This brings up a dialog. Select **AC_Nominal** and **OK**.

7. Right-click **Entry Objects** on a blank **Cell** and select **Find Levels**. In the dialog box, select **functional_levels**. Select a blank cell in **Entry Objects** and select the **Find MicroFlow** entry. In the dialog box, choose **open_fpga_tap** and **OK**. Select a blank cell in **Exit Objects** and select the **Find MicroFlow** entry. In the dialog box, select **close_fpga_tap** and **OK**.

8. Note that these setups are dependent on the test program. This is what is required for the **lv_fpga** test program.

9. Execute the test program by pressing **Start** on the **OpTool** or execute the flow by pressing **Test** on the **FlowTool**. This will cause the Tessent SiliconInsight server to start and then will start the GUI (if **LAUNCH_GUI** is true in the setup file).

10. Save your program. Left-click on **File/SaveAs**.

Add Execution of a Step To Flow

To add an execute test, you load a test program which has Mentor Graphics support—**ETAStrat** test has been added to it. You execute the steps that you want in the production test with the following shell command:

```
$ LVCommand +C<tcid> CommitSteps <production test name> [<stepname1> ... <stepnamen>]
```

For example:

```
$ LVCommand +C31 CommitSteps LVProdTest tapbistv_1__Default_InstReg  
tapbistv_1__Default_ByPassReg
```

When the command completes, you open the FlowTool and add the new test into the flow. This test does not require any modifications—simply connect ports to put it into your flow. After that you run the program from the OpTool and FlowTool and save your program.

Preparing the Pin Map File

In *Setup Step 2* of Tesson SiliconInsight ATE, you prepare the Pin Map file as described in “[Creating a Tesson SiliconInsight Pin Map File](#).”

[Figure 9-9](#) provides an example of the Tesson SiliconInsight pin map file.

Figure 9-9. Example Tesson SiliconInsight Pin Map File

```
PinMap (snip) {  
// DESIGN NAME      : ATE PinName  
trst_n           : TRST;  
tck              : TCK;  
tms              : TMS;  
tdi              : TDI;  
tdo              : TDO;  
rst_n            : in1;  
reset_n          : in2;  
p11106_lock     : out1;  
ptest(14)         : out2;  
ewrap_a          : out3;  
ptest(15)         : out4;  
ewrap_b          : out5;  
clk              : clk1;  
fclk106          : clk2;  
}  
..  
}
```

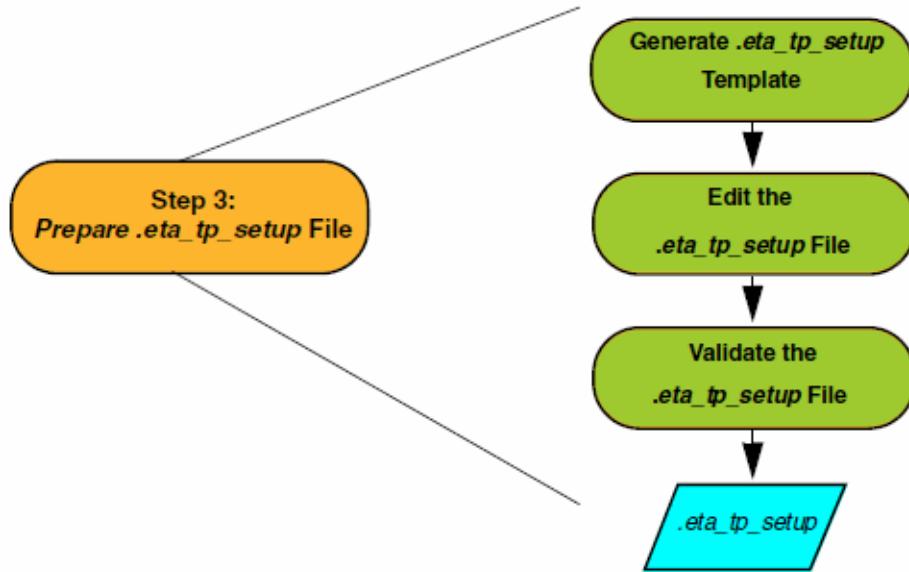
Preparing the Test Program Setup File

In *Setup Step 3* of Tesson SiliconInsight ATE, you set up the Tesson SiliconInsight runtime environment using the *Test Program Setup (.eta_tp_setup)* file, so that the *LVReady* test program can interact with the Tesson SiliconInsight software.

Using the *eta_tp_setup* tool, you create an Test Program Setup file—*.eta_tp_setup*. This file provides network setup and test program information that facilitates the smooth integration of your Test Program with Tesson SiliconInsight. You can edit and validate this file to customize it to your specific ATE platform and IT environment.

Figure 9-10 summarizes the operations performed in this step.

Figure 9-10. Operations Performed in Setup Step 3 for Tessent SiliconInsight ATE



The operations performed in this step are as follows:

1. Generate an *.eta_tp_setup* file template using the *eta_tp_setup* command. You can execute the *eta_tp_setup* command on either the Tessent SiliconInsight server host or the Test Program host.
For more information, refer to “[Generating the Test Program Setup File Template](#).” In addition, You can use a template as described in “[Generating the Test Program Setup File Template](#).”
2. Edit the *.eta_tp_setup* file template using a text editor such as *vi* or *emacs*. For more information, refer to “[Editing the Test Program Setup File](#).”
3. Validate the *.eta_tp_setup* file. Validation must take place on the Test Program host. For more information, refer to “[Validating the Test Program Setup File](#).”

Before proceeding to the detailed description of the operations for setting up Tessent SiliconInsight environment, review the next section, “[Generating the Test Program Setup File](#).” This section outlines the Tessent SiliconInsight runtime environment that is described in the *.eta_tp_setup* file.

Generating the Test Program Setup File

The *.eta_tp_setup* file provides the following information that is required to run the Test Program with Tessent SiliconInsight software:

- Network setup information that is required for communication between the Test Program and the Tessent SiliconInsight server. This information includes the server host names, license information, and so on.
- Test program environment information and device-specific data that is required to test the device. This information includes the Mentor Graphics database (LVDB) name, pattern directories, and so on.

The *.eta_tp_setup* file should be stored in the Test Program directory, enabling you to tar the Test Program and the Setup file into a single entity for ease of portability.

Sample *.eta_tp_setup* File

[Figure 9-11](#) shows a sample *.eta_tp_setup* file. Note that not all properties are shown in this example; certain optional properties have been omitted.

The contents of the *.eta_tp_setup* file are described in detail in the sections following the example.

Figure 9-11. Sample Tessent SiliconInsight Test Program File

```
#####
# This file generated by eta_tp_setup on:      Sun Jan 23 15:08:16 2005
# eta_tp_setup version : 4.2aBeta-Build20050119.002
#
#=====
#
# Please edit this file so that all required parameters have a value.
# In particular, the string:
#
#       <value>
#
# must be replaced by a real value, otherwise there will be a syntax error
# when this setup file is validated.
#
# Some optional parameters are commented out because their default values
# depend on your execution path or an ATE API. These parameters need not be
# specified unless your execution path does not contain the appropriate
# directory.
#
# Detailed explanations for each property are available in file:
#
#       ETASetupFile.readme
#
#=====

#define base = /Teradyne/ETA;
#define base_on_tp_host = h:\Teradyne\ETA;

#define lv_fpga =
%(base)/share/SiliconInsight/examples/LV_FPGA_demo1/Teradyne/lv_fpga_igxl;
#define lv_fpga_on_tp_host =
%(base_on_tp_host)\share\SiliconInsight\examples\LV_FPGA_demo1\Teradyne\lv_fpga_i
gxl;

#####
# IT Parameters
#####
```

```
# Optional:      path of Tessent SiliconInsight installation directory, without the
/bin part.
# From your execution path, if not specified.
ETA_INSTALL_DIR = %(base);
ETA_INSTALL_DIR_ON_TP_HOST = %(base_on_tp_host);

# Required:      license info file or server: <file>, @<host>, <port>@<host>

LICENSE_INFO = @sjlic001;

# Required:      host name or IP address of Tessent SiliconInsight server host
SERVER_HOST = xena;
#####
# User Parameters
#####

# Required:      directory where generated ASCII patterns will be placed
ASCII_PATTERN_DIR = %(lv_fpga)/eta_vec_dir;
ASCII_PATTERN_DIR_ON_TP_HOST = %(lv_fpga_on_tp_host)\eta_vec_dir;

BINARY_PATTERN_DIR = %(lv_fpga_on_tp_host)\eta_vec_dir;

TEST_CONFIGURATION_FILE = %(lv_fpga)/FPGA.config_eta;

# Required:      path of Tessent SiliconInsight pinmap file
ETA_PINMAP_FILE = %(lv_fpga)/FPGA.pinmap;
ETA_PINMAP_FILE_ON_TP_HOST = %(lv_fpga_on_tp_host)\FPGA.pinmap;

# Required:      directory of ETA lvdb for the DUT
LVDB_DIR =
%(base)/share/SiliconInsight/examples/LV_FPGA_demo1/LV_FPGA_demo1.lvdb;

# Required:      directory where Tessent SiliconInsight server files are placed
SERVER_LOG_DIR = %(lv_fpga)/outdir;

# Required:      path of Test Program pinmap file
TP_PINMAP_FILE = %(lv_fpga_on_tp_host)\FPGA.pinmap;
```

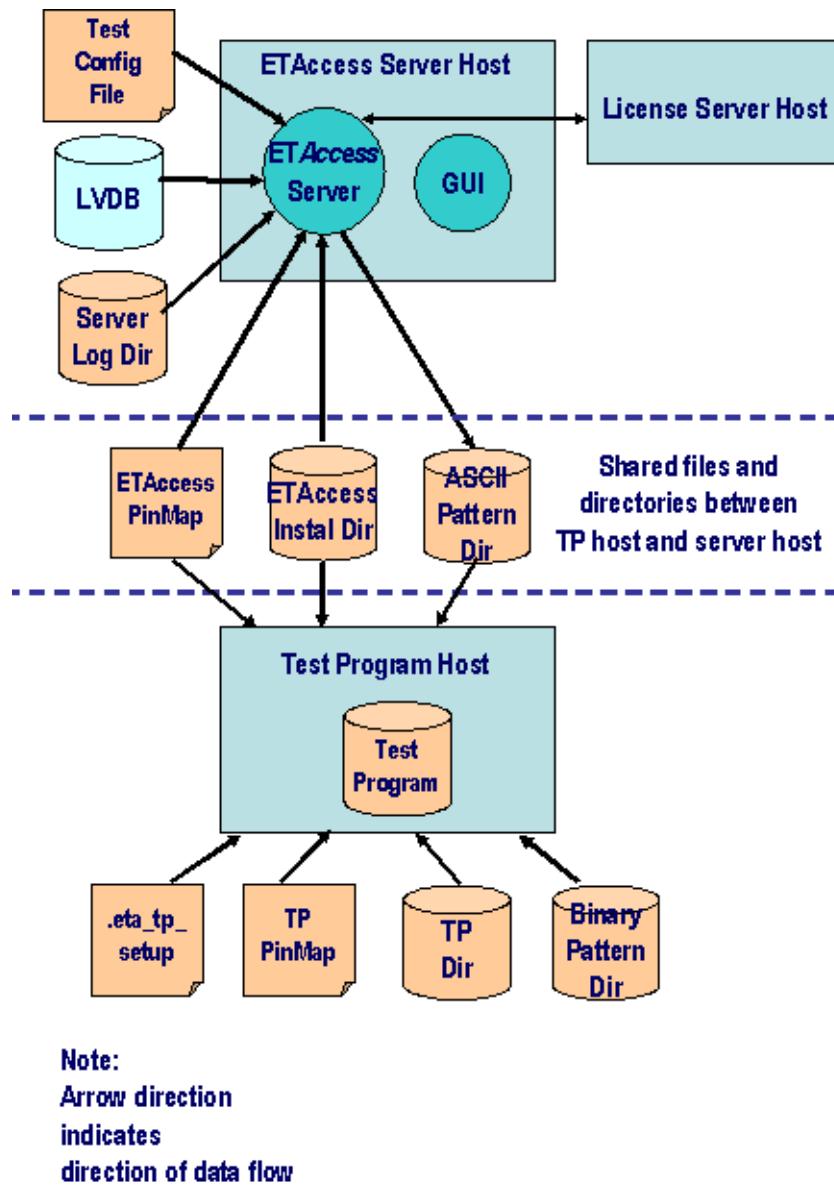
Test Program Setup File Contents

The *.eta_tp_setup* file can contain the following runtime environment components:

- [Properties](#)
- [Comments](#)
- [Include Statements](#)
- [Macros](#)

These runtime environment components are illustrated in [Figure 9-12](#).

Figure 9-12. Tessian SiliconInsight Runtime Environment Components



Each of these components is described in the following sections.

Properties

Properties use the following syntax in the **.eta_tp_setup** file:

```
property_name = <property_value>; #optional comments
```

Properties can be required or optional. Properties can also be specific to a particular ATE platform.

The properties can be listed in any order. If there are duplicate entries for the same property, then the last entry is used, and a warning is generated.

The following sections list all required and optional IT and user properties. For detailed information about each of these properties, refer to “[Test Program Setup File Properties Reference](#).”

Required IT Properties

The following are the *required IT* properties:

- The **ETA_INSTALL_DIR** property defines the directory where the Tesson SiliconInsight software is installed. This property is used to find Tesson SiliconInsight executables.
- The **LICENSE_INFO** property specifies the license server host or file that is required to run the Tesson SiliconInsight server, run the Tesson SiliconInsight GUI, and access certain Tesson SiliconInsight features from the Tesson SiliconInsight Test Program.
- The **SERVER_HOST** property specifies the name or the IP address of the machine on which the Tesson SiliconInsight server software is running. Remember that the Tesson SiliconInsight server can only run on a Solaris platform.

Optional IT Properties

The following are the *optional IT* properties.

- The **ETA_INSTALL_DIR_ON_TP_HOST** property defines the directory where the Tesson SiliconInsight software is installed as seen from the Test Program host. This property is used to find Tesson SiliconInsight executables from the Test Program host.

Required User Properties

The following are the *required user* properties:

- The **ASCII_PATTERN_DIR** property defines the directory where the ASCII patterns generated by the Tesson SiliconInsight server are stored.
- The **ASCII_PATTERN_DIR_ON_TP_HOST** property defines the directory where the ASCII patterns generated by the Tesson SiliconInsight server are stored as seen on the Test Program host. This property is required only if the directory paths on the Test Program host are different from those on the Tesson SiliconInsight Server host.
- The **BINARY_PATTERN_DIR** property defines the directory where the binary patterns compiled by the Test Program are placed.
- The **SERVER_LOG_DIR** property defines the log directory where log files created by the Tesson SiliconInsight server are placed.
- The **TP_PINMAP_FILE** property defines the path to the location of the Test Program pin map file. This ASCII file maps the device pin names to the tester channels.

Optional User Properties

The following are the *optional user* properties:

- The **TEST_CONFIGURATION_FILE** property specifies the Tesson SiliconInsight test configuration to be loaded.
- The **ETA_PINMAP_FILE** property identifies the path to the pin map file. The Tesson SiliconInsight Pin Map file defines the mapping between the ATE pin names and the design pin names.
- The **ETA_PINMAP_FILE_ON_TP_HOST** property identifies the path to the pin map file as seen on the Test Program host. The Tesson SiliconInsight Pin Map file defines the mapping between the ATE pin names and the design pin names.
- The **LVDB_DIR** property specifies the Mentor Graphics database (LVDB) for the device under test.

Comments

You can insert comments into your *.eta_tp_setup* file.

Insert comments into the file by prefacing the comment with an octothorpe (#), as shown in the following example:

```
#this property defines the location of the Tesson SiliconInsight Server
```

Block comments are not supported.

Include Statements

You can include other setup files in your *.eta_tp_setup* file.

Include other Setup files by using the following syntax:

```
%include <filename1>
%include <filename2>
.
.
.
```

where *filename* is the name of the Setup file you wish to include.

The filename must be specified by one of the following:

- The absolute path
- A path relative to a base directory defined as a macro in the setup file
- A path relative to the setup file that is currently being defined
- A macro name

You can incorporate multiple include statements, each containing a setup file. Any property defined in the “included” setup file is overridden by that property (if any) as defined in the *.eta_tp_setup* file.

Macros

You can define macros within the *.eta_tp_setup* file itself. These macros can then be referenced in the Setup file to compute the directory and file paths.

Macros must conform to the following rules:

- Macro definitions must be simple character strings.
- They cannot contain logical or arithmetic expressions.
- They can be defined anywhere in the Setup file but they must be defined before they are used.
- Nested macros are not supported. However, macro definitions can contain other macros.

You can define a macro using the following syntax:

```
%define <macroname>=<macrovalue>; #optional comments
```

where valid values are as follows:

- *macroname* is the name assigned to the macro
- *macrovalue* is the value assigned to the macro, for example, a path name.
- *#optional comments* are any comments you want to record about this macro

For example, to define a base directory for Mentor Graphics software, you could use the following syntax:

```
%define LVID=/home/user/eta; #LV sw location
```

In this example, the macro is named LVID; it defines the location of the Mentor Graphics software as */home/user/eta*. A comment is provided indicating this information.

Macros are invoked in the *.eta_tp_setup* file using the following syntax:

```
%(<macro_name>)
```

For example,

```
<property_name> =%(<macro_name>);
```

or

```
%include%(<macro_name>)/Current;
```

or

```
%define macro2 =%(<macro_name>)/bin_dir;
```

Generating the Test Program Setup File Template

For your convenience, the Tesson SiliconInsight software includes a utility that can automatically generate an *.eta_tp_setup* starter file template.

To generate the setup file template, enter the following command:

```
eta_tp_setup <setupFile> -mode genTemplate  
[-incFile <incFile> [-incFile <incFile>...]]  
[-logFile <logFile>]
```

where valid values are as follows:

- *setupFile*—specifies the path of the *.eta_tp_setup* file to be generated. If a file extension is not specified, the default extension (*.eta_tp_setup*) is automatically appended. When generating a template, if the file already exists, the existing file is renamed to *<setupFile>.bak* first, and a new *.eta_tp_setup* file is created.
- *incFile*—specifies a file to be added at the beginning of the *.eta_tp_setup* file as *%include* statements.
- *logFile*—specifies a path for the script log file.

This operation outputs these files:

- *<setupFile>.eta_tp_setup*—the *.eta_tp_setup* starter file template.
- *<setupFile>.readme*—a file that contains detailed information about each property in the *.eta_tp_setup* file. You can use this file along with the information in “[Test Program Setup File Properties Reference](#)” to guide you through filling in the Setup file.
- *<setupFile>.log*—a file that contains the log information.

Editing the Test Program Setup File

Once the template is generated, you can use a text editor, such as *vi* or *emacs*, to edit the *.eta_tp_setup* file to suit your individual system and platform requirements. For detailed information on this file, refer to “[Test Program Setup File Properties Reference](#).”

Validating the Test Program Setup File

Once you have edited the starter template and modified the properties in the desired fashion, you can begin validating the *.eta_tp_setup* file.

Note



Validation must be performed on the Test Program host before loading the test program on the tester.

You can ask the IT engineer to validate the IT-only properties, by using the following syntax:

```
eta_tp_setup <setupFile> -mode ITvalidate \
    -servertype \
    < image | igxl | smartest | toolbox |
        envision | offline >
```

where valid values are as follows:

- *setupFile*— is the name of the *.eta_tp_setup* file being validated.
- *image*—is used for Teradyne (Image) ATE.
- *igxl*—is used for Teradyne (UltraFlex) ATE.
- *smartest*—is used for Verigy ATE.
- *toolbox*—is used for Credence ATE.
- *envision*—is used for LTX (Envision) ATE.
- *offline*—is ATE-independent.

Optionally, you can validate the entire setup file yourself, using the following command:

```
eta_tp_setup <setupFile> -mode validate\
    -servertype \
    < image | igxl | smartest | toolbox |
        envision | offline >
```

where valid values are as follows:

- *image*—is used for Teradyne (Image) ATE.
- *igxl*—is used for Teradyne (UltraFlex) ATE.
- *smartest*—is used for Verigy ATE.
- *toolbox*—is used for Credence ATE.
- *envision*—is used for LTX (Envision) ATE.
- *offline*—is ATE-independent.

Test Program Setup File Properties Reference

The Tesson SiliconInsight Test Program Setup file supports the following properties as described in this section:

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Summary of Test Program Setup File Properties

The Tesson SiliconInsight Test Program Setup (*.eta_tp_setup*) file contains properties required for communication and integration of a User Test Program with the Tesson SiliconInsight software.

Properties can categorized as follows:

- *Required*—the property is mandatory
- *Optional*—the property is not mandatory
- *IT*—the property is IT (Information Technology)-related
- *User*—the property is related to the user Test Program
- *Platform-specific*—the property is specific to a particular ATE platform.

Properties can fall into more than one category, as [Table 9-1](#) shows:

Table 9-1. Summary of Test Program Setup File Properties

PropertyName	Category
SERVER_HOST	Required IT
LICENSE_INFO	Required IT

Table 9-1. Summary of Test Program Setup File Properties (cont.)

PropertyName	Category
ETA_INSTALL_DIR ETA_INSTALL_DIR_ON_TP_HOST	Required IT Optional IT
ETA_STDF_FILE	Optional User
ASCII_PATTERN_DIR ASCII_PATTERN_DIR_ON_TP_HOST	Required User Optional User
BINARY_PATTERN_DIR	Required User
SERVER_LOG_DIR	Required User
LVDB_DIR	Optional User
TEST_CONFIGURATION_FILE	Optional User
ETA_PINMAP_FILE ETA_PINMAP_FILE_ON_TP_HOST	Optional User Optional User
TP_PINMAP_FILE	Required User
LASER_REPAIR_FILE_FORMAT	Optional User
NUMBER_OF_SITES	Optional User
IMAGE_TMODE	Optional User (Teradyne-specific)

The descriptions of all available properties are described in the following sections and listed in alphabetic order.

ASCII_PATTERN_DIR

The required **ASCII_PATTERN_DIR** property defines the directory where the ASCII patterns generated by the Tesson SiliconInsight server are stored.

Syntax

The following syntax specifies this property:

```
ASCII_PATTERN_DIR = <path> ;
```

where *path* is the path to the directory where the patterns are placed.

Default Value

None

Usage Conditions

The following usage conditions apply:

- The specified directory must exist.
- You must have write permissions to the directory specified by the **ASCII_PATTERN_DIR** property on the Tesson SiliconInsight server host.
- The directory specified by the **ASCII_PATTERN_DIR** must be visible from the Test Program host. If the directory path naming conventions are different between the Tesson SiliconInsight server host and the Test Program host, then you must also define [**ASCII_PATTERN_DIR_ON_TP_HOST**](#) property.

Example

In the following example, the ASCII patterns are placed in the */home/etaengr/Teradyne/ENG_VALIDATION/ascii_dir* directory.

```
ASCII_PATTERN_DIR = /home/etaengr/Teradyne/ENG_VALIDATION/ascii_dir ;
```

Related Information

[**ASCII_PATTERN_DIR_ON_TP_HOST**](#)

ASCII_PATTERN_DIR_ON_TP_HOST

The required **ASCII_PATTERN_DIR_ON_TP_HOST** property defines the directory where the ASCII patterns generated by the Tessent SiliconInsight server are stored. The directory path specified follows the file path naming conventions suitable for the Test Program host.

Syntax

The following syntax specifies this property:

ASCII_PATTERN_DIR_ON_TP_HOST = <path>;

where *path* is the path to the directory where the patterns are placed.

Default Value

None

Usage Conditions

The following usage conditions apply:

- You need to specify this property only if the value specified for the [ASCII_PATTERN_DIR](#) is not visible from the Test Program host. For example, if the Test Program host is a Windows-based operating system (as is the case for Teradyne UltraFlex running IG-XL), then the directory path naming conventions are different from those of the Solaris-based Tessent SiliconInsight server.
- You must specify **ASCII_PATTERN_DIR_ON_TP_HOST** in addition to the [ASCII_PATTERN_DIR](#) property.
- The specified directory must exist.

Example

In the following example, the ASCII patterns are placed in the *h:\unixhome\Teradyne\MyTestProgram\mypatterns* directory.

```
%define tp_dir_on_tp_host = h:\unixhome\Teradyne\MyTestProgram;
ASCII_PATTERN_DIR_ON_TP_HOST = %(tp_dir_on_tp_host)\mypatterns;
```

Related Information

[ASCII_PATTERN_DIR](#)

BINARY_PATTERN_DIR

The required **BINARY_PATTERN_DIR** property defines the directory where the binary patterns compiled by the Test Program are placed.

Syntax

The following syntax specifies this property:

```
BINARY_PATTERN_DIR = <path> ;
```

where *path* is the path to the directory where the patterns are placed. This path MUST always be visible from the Test Program on the Test Program host machine.

Default Value

None

Usage Conditions

The following usage conditions apply:

- You must follow the Test Program host directory path naming conventions to specify a value for this property.
- The specified directory must exist.
- You must have read and write permissions to the specified directory on the Test Program host.

Example

In the following example, the patterns placed in the /home/etaengr/Teradyne/ENG_VALIDATION/bin_dir directory.

```
BINARY_PATTERN_DIR = /home/etaengr/Teradyne/ENG_VALIDATION/bin_dir ;
```

Related Information

None

BONDING_OPTION

The BONDING_OPTION property specifies the bounding option when launching the server through the Test Program Setup file.

Syntax

```
BONDING_OPTION = <option_name>;
```

Default Value

None

Usage Conditions

For an LVDB with multiple bonding options, this defines the bonding option to be used, as it appears in the *tcm* file. The server will error out if the design has multiple bonding options and this option is not specified.

ETA_INSTALL_DIR

The optional **ETA_INSTALL_DIR** property defines the directory where the Tesson SiliconInsight software is installed. This property is used to find Tesson SiliconInsight executables.

This is an IT property.

Syntax

The following syntax specifies this property:

ETA_INSTALL_DIR = <path> ;

where *path* is the path to the directory where Tesson SiliconInsight software is installed

Default Value

By default, it is assumed that the Tesson SiliconInsight executables are in your execution path.

Usage Conditions

The following usage conditions apply:

- If the **ETA_INSTALL_DIR** property is not specified, the Tesson SiliconInsight Test Program assumes that the */bin* directory of the current Tesson SiliconInsight release is in your execution path. If the property is specified, that location overrides your execution path.
- The Tesson SiliconInsight installation path must be specified *without* the */bin* directory. If */bin* is specified, an error message is generated.
- The specified directory must be visible by both the Test Program host and the SERVER_HOST using the same directory path. Therefore, the disk on both the Tesson SiliconInsight Server Host and the Test Program Host must use the same mount point. If this condition can not be satisfied, you must specify the additional property [ETA_INSTALL_DIR_ON_TP_HOST](#).
- You must have execute permission for all required executables for the Tesson SiliconInsight server and the scripts in the directory specified by the **ETA_INSTALL_DIR** property.

Example

In the following example, the executables are found in the */software/tesson_software_tree/bin* directory.

ETA_INSTALL_DIR = /software/tesson_software_tree;

Related Information

[ETA_INSTALL_DIR_ON_TP_HOST](#)

ETA_INSTALL_DIR_ON_TP_HOST

The optional **ETA_INSTALL_DIR_ON_TP_HOST** property defines the directory where the Tesson SiliconInsight software is installed. This property is used to find Tesson SiliconInsight executables.

This is an IT property.

Syntax

The following syntax specifies this property:

ETA_INSTALL_DIR_ON_TP_HOST = <path>;

where *path* is the path to the directory where Tesson SiliconInsight software is installed as seen on the test program host.

Default Value

By default, it is assumed that the Tesson SiliconInsight executables are in your execution path.

Usage Conditions

The following usage conditions apply:

- You need to specify this property only if the value specified for the [ETA_INSTALL_DIR](#) property is not visible from the Test Program host. For example, if the Test Program host is a Windows-based operating system (as is the case for Teradyne UltraFlex running IG-XL), then the directory path naming conventions are different from those of the Solaris-based Tesson SiliconInsight server.
- If the **ETA_INSTALL_DIR_ON_TP_HOST** property is not specified, the Tesson SiliconInsight Test Program first checks for the value of the property [ETA_INSTALL_DIR](#). If the **ETA_INSTALL_DIR** property is also not specified, then it assumes that the */bin* directory of the current Tesson SiliconInsight release is in your execution path. If the property is specified, that location overrides your execution path.
- The Tesson SiliconInsight installation path must be specified without the */bin* directory. If */bin* is specified, an error message is generated.
- You must have execute permission for all required executables for the Tesson SiliconInsight server and the scripts in the directory specified by the [ETA_INSTALL_DIR](#) property.

Example

In the following example, the executables are found in the *h:\unixhome\LV2005.0b.SP2\ETAccess\bin* directory.

ETA_INSTALL_DIR_ON_TP_HOST= h:\unixhome\LV2005.0b.SP2\ETAccess;

Related Information

[ETA_INSTALL_DIR](#)

ETA_PINMAP_FILE

The optional **ETA_PINMAP_FILE** property identifies the file defining mapping between the ATE pin names and the design pin names.

Syntax

The following syntax specifies this property:

```
ETA_PINMAP_FILE = <path>;
```

where *path* is the path for the Tesson SiliconInsight pin map

Default Value

None

Usage Conditions

The following usage conditions apply:

- The path must be specified as an absolute path or as a path relative to a base directory defined as a macro.
- The specified file must exist.
- The user must have read permissions to the file from both the **SERVER_HOST** and the Test Program server host using the same path. If this condition can not be satisfied, then you must specify the additional property **ETA_PINMAP_FILE_ON_TP_HOST**.
- The specified file is validated, if required, by the platform against the **TP_PINMAP_FILE** property to ensure that all ATE names specified in the **ETA_PINMAP_FILE** are present in the **TP_PINMAP_FILE**.

Example

In the following example, the mapping file is called *demo_eta_tdyne.pinmap*.

```
ETA_PINMAP_FILE =
/home/etaengr/Teradyne/ENG_VALIDATION/demo_eta_tdyne.pinmap;
```

Related Information

[ETA_PINMAP_FILE_ON_TP_HOST](#)

[TP_PINMAP_FILE](#)

[SERVER_HOST](#)

ETA_PINMAP_FILE_ON_TP_HOST

The optional **ETA_PINMAP_FILE_ON_TP_HOST** property identifies the file defining mapping between the ATE pin names and the design pin names.

Syntax

The following syntax specifies this property:

```
ETA_PINMAP_FILE_ON_TP_HOST = <path>;
```

where *path* is the path for the Tesson SiliconInsight pin map file.

Default Value

None

Usage Conditions

The following usage conditions apply:

- You need to specify this property only if the value specified for the **ETA_PINMAP_FILE** property is not visible from the Test Program host. For example, if the Test Program host is a Windows-based operating system (as is the case for Teradyne UltraFlex running IG-XL), then the file path naming conventions are different from those of the Solaris-based Tesson SiliconInsight server.
- The path must be specified as an absolute path or as a path relative to a base directory defined as a macro.
- The specified file must exist.
- You must have read permissions to the file from the Test Program server host using the same path.
- The specified file is validated, if required, by the platform against the **TP_PINMAP_FILE** property to ensure that all ATE names specified in the **ETA_PINMAP_FILE** are present in the **TP_PINMAP_FILE**.

Example

In the following example, the mapping file is called *mytp.pinmap*.

```
%define tp_dir_on_tp_host = h:\unixhome\Teradyne\MyTestProgram;  
ETA_PINMAP_FILE_ON_TP_HOST = % (tp_dir_on_tp_host)\pinmap\mytp.pinmap;
```

Related Information

[ETA_PINMAP_FILE](#)

[TP_PINMAP_FILE](#)

[SERVER_HOST](#)

ETA_STDF_FILE

The optional **ETA_STDF_FILE** property enables Tesson SiliconInsight datalog to be generated in STDF format and identifies the file to contain it.

Syntax

The following syntax specifies this property:

```
ETA_STDF_FILE = <fileName>;
```

where *fileName* is the name of the file to contain the Tesson SiliconInsight datalog in STDF format.

Default Value

None

Usage Conditions

These usage conditions apply:

- The path must be specified as an absolute path or as a path relative to the location of the test program.
- Support for Tesson SiliconInsight datalog generation in STDF format is only supported when using an LVPD

Example

In the following example, the mapping file is called *my_device.stdf*.

```
ETA_STDF_FILE = my_device.stdf;
```

Related Information

None

IMAGE_TMODE

The optional **IMAGE_TMODE** property specifies the TMode to be used for Image on the Tiger platform.

This property is specific to the Teradyne ATE.

Syntax

The following syntax specifies this property:

```
IMAGE_TMODE = (T100) | T200 | T400 | T800
```

Default Value

The default value is *T100*.

Usage Conditions

None

Example

In the following example, the TMode to be used for Image is *T200*.

```
IMAGE_TMODE = T200 ;
```

Related Information

None

LASER_REPAIR_FILE_FORMAT

The optional **LASER_REPAIR_FILE_FORMAT** property defines the file format in which the accumulated BIRA data will be saved by the *ETAEExtractSaveAndClearBIRAData()* API.

Syntax

The following syntax specifies this property:

```
LASER_REPAIR_FILE_FORMAT = TSMC | (LVDEF) ;
```

where valid values are as follows:

- *TSMC*—corresponds to the TSMC laser repair file format.
- *LVDEF*—corresponds to the Mentor Graphics file format.

Default Value

The default value is *LVDEF*.

Usage Conditions

None

Example

In the following example, the laser repair file format is set to *TSMC*.

```
LASER_REPAIR_FILE_FORMAT = TSMC ;
```

Related Information

None

LICENSE_INFO

The required **LICENSE_INFO** property specifies the license server host or file which is required to run the Tessent SiliconInsight server, the Tessent SiliconInsight GUI, and to access certain Tessent SiliconInsight features from the LVReady Test Program.

This is an IT property.

Syntax

The following syntax specifies this property:

```
LICENSE_INFO = <location> ;
```

where valid values are as follows:

- <*absolute file path*>—used when the license file is known and it is comprised of a single file
- <*absolute file path1*>: <*absolute file path2*>...—used when the license file is known and it is comprised of a list of files
- @<*hostname*>—used when the unique license server hostname is known
- <*port_number*>@<*hostname*>—used when the unique license server hostname and port name is known
- <*port_number*>@<*hostname1*>:<*port_number*>@<*hostname2*>—
used when the redundant license server hostnames and unique port names are known

Default Value

None

Usage Conditions

The following usage conditions apply:

- When the license file or files are specified, the file or files must be specified using the absolute path. The specified file or files must be readable from the SERVER_HOST.
- When the license server host is specified, it must be specified with an @ symbol as the first character in the hostname. The host must be accessible from the SERVER_HOST.
- The license server host can be a SUN host running Solaris or a machine running Linux on which the license server is installed and running.

Example

In the following example, the license server is defined running at host *utopia*:

```
LICENSE_INFO = @utopia ;
```

Related Information

None

LVDB_DIR

The optional **LVDB_DIR** property specifies the Mentor Graphics database (LVDB) for the device under test.

Syntax

The following syntax specifies this property:

LVDB_DIR = <path> ;

where *path* is the path to the directory where the LVDB is located

Default Value

None

Usage Conditions

The specified directory path must exist and be readable by the user from the SERVER_HOST.

Example

In the following example, the LVDB is located in

/home/etaengr/Teradyne/ENG_VALIDATION/demo_lvdb/:

LVDB_DIR = /home/etaengr/Teradyne/ENG_VALIDATION/demo_lvdb;

Related Information

None

NUMBER_OF_SITES

The optional **NUMBER_OF_SITES** property defines the number of sites on the tester.

Syntax

The following syntax specifies this property:

```
NUMBER_OF_SITES = x ;
```

where *x* is an integer greater than 0 indicating the number of sites

Default Value

The default value is *1*.

Usage Conditions

None

Example

In the following example, the number of sites on the tester is 4:

```
NUMBER_OF_SITES = 4 ;
```

Related Information

None

SERVER_HOST

The required **SERVER_HOST** property specifies the name or the IP address of the machine on which the Tessian SiliconInsight server software is running.

This is an IT property.

Syntax

The following syntax specifies this property:

SERVER_HOST = <hostname> ;

where *hostname* is the name of the host machine or the IP address

Default Value

None

Usage Conditions

The server must be a Sun host running Solaris 5.7 or later. The server must be accessible from the Test Program host machine.

Example

In the following example, the server is defined as *utopia*:

SERVER_HOST = *utopia* ;

Related Information

None

SERVER_LOG_DIR

The required **SERVER_LOG_DIR** property defines the log directory where log files created by the Tesson SiliconInsight server are placed.

Syntax

The following syntax specifies this property:

SERVER_LOG_DIR = <path> ;

where *path* is the path to the directory where the log files are placed

Default Value

None

Usage Conditions

The following usage conditions apply:

- The specified directory must exist.
- The user on the SERVER_HOST must have write permission to the directory.

Example

In the following example, the log files are placed in
/home/etaengr/Teradyne/ENG_VALIDATION/log/:

SERVER_LOG_DIR = /home/etaengr/Teradyne/ENG_VALIDATION/log/ ;

Related Information

None

TEST_CONFIGURATION_FILE

The optional **TEST_CONFIGURATION_FILE** property specifies the Tesson SiliconInsight test configuration to be loaded.

Syntax

The following syntax specifies this property:

```
TEST_CONFIGURATION_FILE = <path> ;
```

where *path* is the path of the Tesson SiliconInsight Test Configuration file

Default Value

None

Usage Conditions

The following usage conditions apply:

- You will typically start with the default test configuration file that is part of the LVDB and is called <designName>.config_eta.
- The path must be specified as either an absolute path or a path relative to a base directory defined as a macro.
- The specified file must exist on the Tesson SiliconInsight server.
- The user must have read permissions to the specified file.

Example

In the following example, the Tesson SiliconInsight configuration file is located in /home/etaengr/Teradyne/ENG_VALIDATION/test.config_eta:

```
TEST_CONFIGURATION_FILE =  
/home/etaengr/Teradyne/ENG_VALIDATION/test.config_eta ;
```

Related Information

[LVDB_DIR](#)

TP_PINMAP_FILE

The required **TP_PINMAP_FILE** property defines the path to the location of the Test Program pin map file. This ASCII file maps the device pin names to the tester channels.

Syntax

The following syntax specifies this property:

```
TP_PINMAP_FILE = <path> ;
```

where *path* is the path to the directory containing the Test Program pin map file

Default Value

None

Usage Conditions

The following usage conditions apply:

- The pin configuration information in the specified file can be part of the Test Program source file on some platforms (such as Credence).
- The path must be defined as an absolute path or as a path relative to a base directory defined as a macro.
- The specified file must be readable by the Test Program.

Example

In the following example, the pin map file, *demo1_pinmap.h*, is located in the *demo* directory:

```
TP_PINMAP_FILE =
/home/etaengr/Teradyne/ENG_VALIDATION/demo/demo1_pinmap.h ;
```

Related Information

[ETA_PINMAP_FILE](#)

Chapter 10

Setting Up Tessent SiliconInsight Production Datalogging

This chapter explains how to set up the Tessent SiliconInsight production datalogging. It provides step-by-step instructions on how to use the Tessent SiliconInsight software to direct the embedded test resources on the DUT to perform production go/no-go and detailed diagnosis of memories, logic, PLLs, and I/Os. This chapter includes complete reference information on the relevant API calls, runtime options, and files that are used in production datalogging.

Chapter topics follow this sequence:

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In particular, this chapter provides the following information:

- **Introducing Production Datalogging** introduces Mentor Graphics' embedded test-based approach to manufacturing test. This chapter also provides descriptions of the various forms of embedded test and how these forms can be used to decrease manufacturing test costs, improve quality, and time to market.
- **Preparing the Pin Map File** explains the purpose and content of the Pin Map file and provides details on how to prepare this file.
- **Generating the Vector Files** explains how to generate the vector files if your test configuration is set up to generate datalog for failing flip-flops.

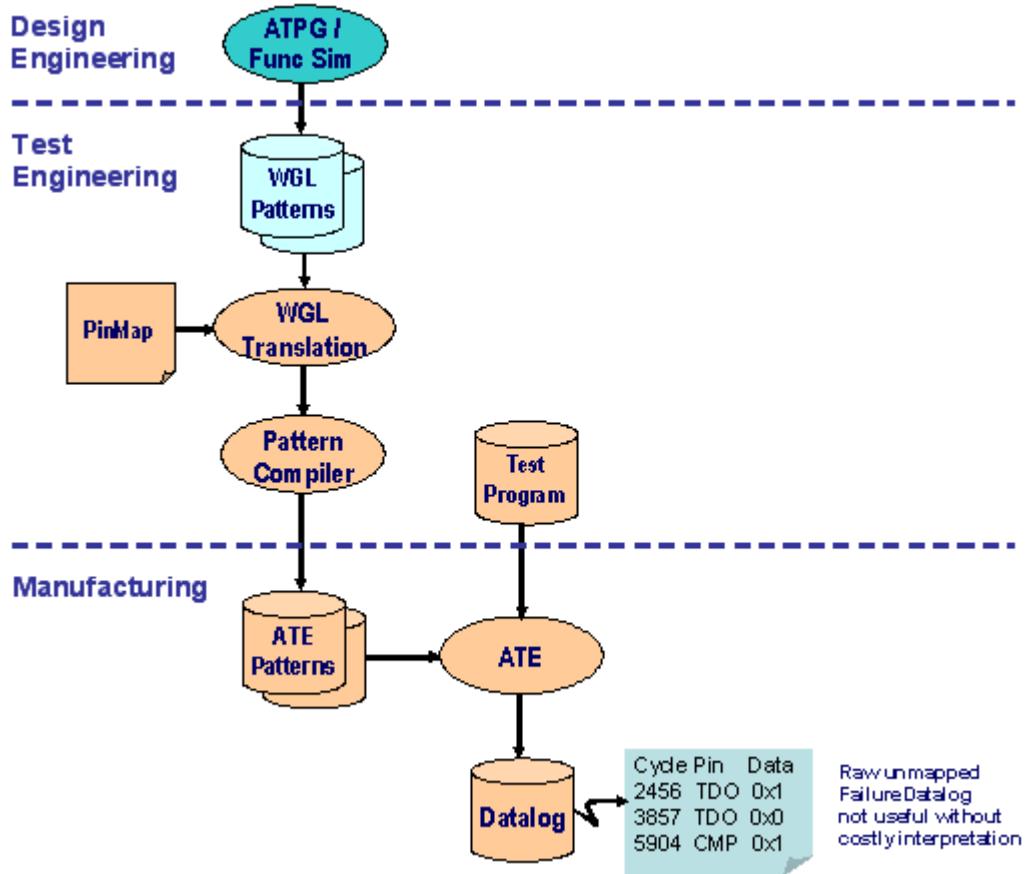
- **Generating the LVPD** explains how to generate the LVPD using the data you prepared in the previous steps.
- **Making Your User Test Program LVReady** explains how to make your test program LVReady and provides the specific ATE platform information for Teradyne (IG-XL) and Verigy (SmarTest).
- **Validating the LVPD** explains how to validate the LVPD for the final hand-off to manufacturing engineering.

Introducing Production Datalogging

A conventional manufacturing test flow is shown in [Figure 10-1](#). In this flow, WGL or STIL patterns are generated by the design engineers and are handed off to the test engineer. The test engineer then spends considerable effort to translate and compile these patterns into the ATE platform specific binary patterns. These patterns are then applied during the production flow via the test program to perform the Go/No-Go testing.

When the Go/No-Go testing is performed on the ATE, a faulty device under test generates miscompares, which are reported in terms of the cycle numbers and the failing pins in the tester datalog. However, this miscompare information does not provide any further details such as failing embedded memory addresses or failing flip-flops. In order to extract this information from the failing pin datalog, a test engineer often must consult the design engineer and devise complex and time-consuming programs to map the failures to the design data.

Figure 10-1. Conventional Manufacturing Test Flow

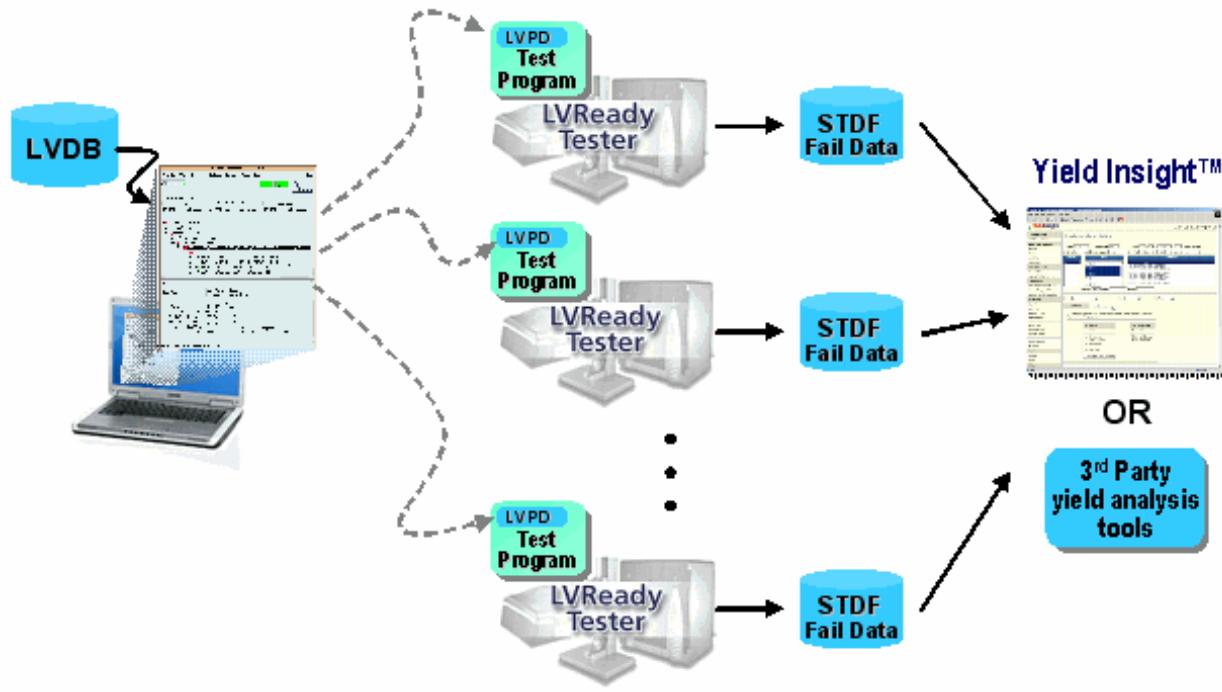


Knowing precisely which memory addresses or which flip-flops or gates and under what test conditions these are causing yield loss is extremely valuable during the yield ramp. The same data is also helpful in the production stage to be used in yield monitoring or for failure analysis.

Mentor Graphics' BIST solutions not only provide significant test quality and test cost benefits but also provide unique support for product and yield enhancement through a fully vectorless and production datalogging flow illustrated in [Figure 10-2](#).

Designers use Mentor Graphics' design automation tools to create and integrate BIST resources into a design. As part of the final sign-off process, the tools generate a Mentor Graphics database (LVDB) which contains extensive information on the BIST resources and the design itself. The LVDB provides Mentor Graphics' automated diagnostic software, Tessent SiliconInsight, with the information it needs to control and interpret results from the BIST within the DUT. In addition to being used interactively, the Tessent SiliconInsight software can also be used to create customized libraries that provide the same functionality as the Tessent SiliconInsight software. These libraries together with other BIST related data are called a Mentor Graphics Production Database (LVPD). Copies of an LVPD can be shipped to any number of testers and linked into the DUT's production test program.

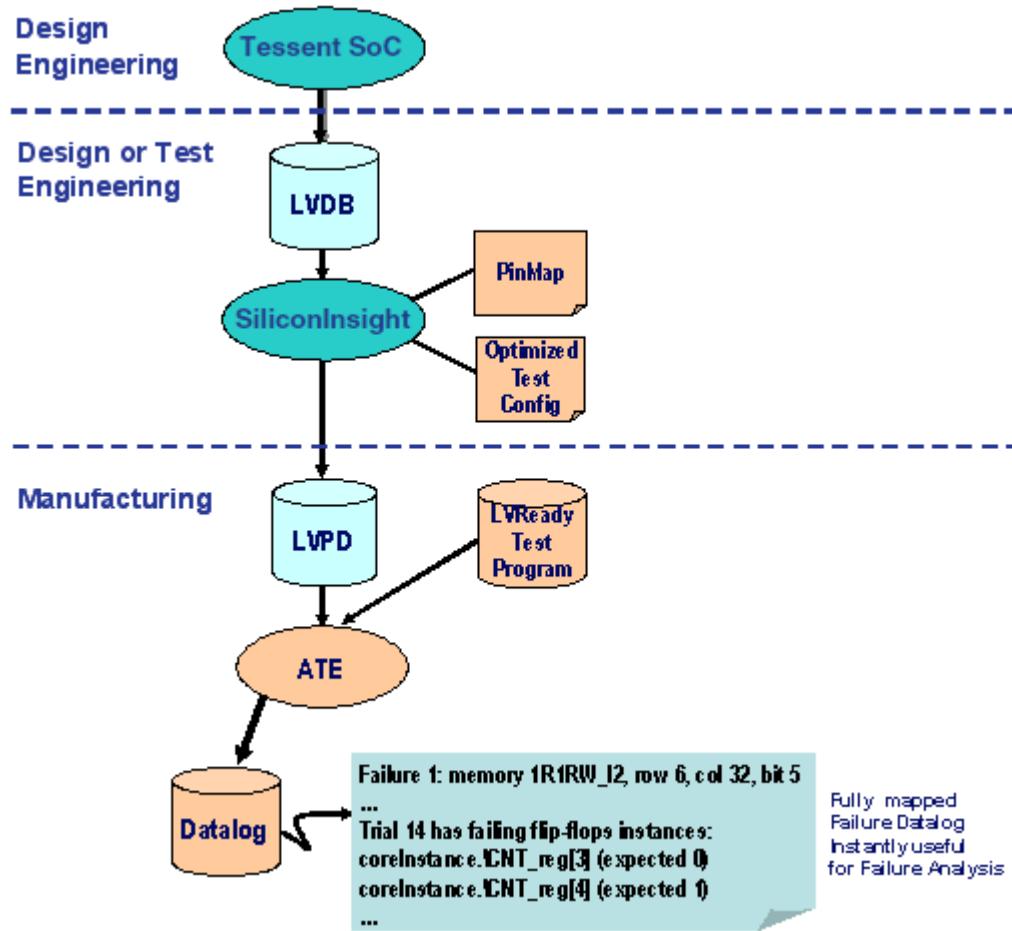
Figure 10-2. Mentor Graphics Production Datalogging Flow



Function calls are then placed within the test program to invoke the LVPD libraries as needed to drive diagnosis and subsequent datalogging of detected failures. This mechanism allows any level of datalogging, from simple pass/fail to detailed performance measurements and diagnostics, to be performed seamlessly during production testing. The results of this detailed datalogging (stored in STDF format or in readable ASCII) can be analyzed over time to detect and analyze systematic issues effecting performance and yield. This analysis can be performed using Mentor Graphics' Tessent SiliconInsight tool, or the logged data can be processed by other 3rd party yield analysis tools.

A more detailed illustration of Mentor Graphics' LVPD-based production datalogging flow is shown in [Figure 10-3](#).

Figure 10-3. LVPD-Based Manufacturing Test Flow



The LVDB contains the default configuration used to run the BIST tests as conceived by the design engineer. This serves as the starting point for the test engineer to create one or more optimized BIST test configurations. The test engineer will make minimal modifications to the test program to make it *LVReady*. Using the LVDB, an optimized test configuration, and the pin map specifications, a test engineer can create an LVPD which will be loaded and accessed by the test program.

The vector translation and compilation steps required in the traditional flow are eliminated. Instead, ATE specific test patterns are automatically generated and embedded into the LVPD. At the same time, data required to back map the raw ATE failures to the design data is generated and stored in the LVPD as well. The test program is still loaded and executed as before. It is still required to perform basic initialization actions like setting relays and any needed default I/O timings. After initialization, the test program can, based on the function calls, load the vectors from the LVPD and apply them to the device in order to initialize and run one or more BIST controllers and extract subsequent failure information. The generated datalog will contain sub-die failure information that is readily used for yield learning purposes.

Benefits of Production Datalogging

The Mentor Graphics production datalogging flow provides the following benefits:

- Eliminates the time consuming vector translation process from WGL or STIL to your target ATE platform. Using the data in the LVDB, Tessent SiliconInsight generates ATE specific vectors as part of the LVPD.
- Is completely compatible with the existing WGL-based or STIL-based production flows. The licensed Tessent SiliconInsight software is required for generation of the LVPD only. However, once on the production floor, you do not need to install any additional software or licensing.
- Generates detailed datalog information for failed devices that includes the following information (depending on how the BIST controllers are configured for the device):
 - For memories, failures down to the specific physical or logical row, column and bit position are logged.
 - For memories with redundant elements, fuse repair data can be logged.
 - For logic blocks/cores, failing patterns (logic BIST trials) and the failing flip-flops per pattern are logged.
- Simplifies the archiving and hand-off requirements for both the design engineer and the test engineer. The design engineer just needs to hand-off the LVDB to the test engineer. The test engineer, in turn, needs to hand-off only the test program and the LVPD to the manufacturing facility.

Production Datalogging Prerequisites

This section describes the prerequisites and restrictions on using the production datalogging flow. Please review the following prerequisites and verify that your test environment satisfies these requirements:

- Creation of a LVPD using Tessent SiliconInsight requires a special software license. Verify that you are licensed to use this feature or contact Mentor Graphics support personnel for details on the licensing requirements.
- Your target ATE platform must be *LVReady*—that is, one of those supported by Tessent SiliconInsight. The Tessent SiliconInsight software has been integrated and qualified on many leading ATE platforms. Refer to the *Install and Release Notes* for a list of all ATE platforms and software versions that are supported by Tessent SiliconInsight.
- Your user test program must be *LVReady*. This means—modifying your user test program to make a call to at least one Tessent SiliconInsight Test Program API. For more information on making your user test program *LVReady*, refer to “[Making Your User Test Program LVReady](#).”

- Your test configuration must be finalized. You must prepare to create the LVPD using Tesson SiliconInsight only after you have optimized and verified the test configuration.
- If your test configuration is setup to generate datalog for failing flip-flops, you must generate the vector files required to identify the failing flip-flop instances for datalog and to provide appropriate failing flip-flop identification to the gateDiagnose tool for gate-level diagnosis. For more information on how to generate the vector files, refer to “[Generating the Vector Files](#).”

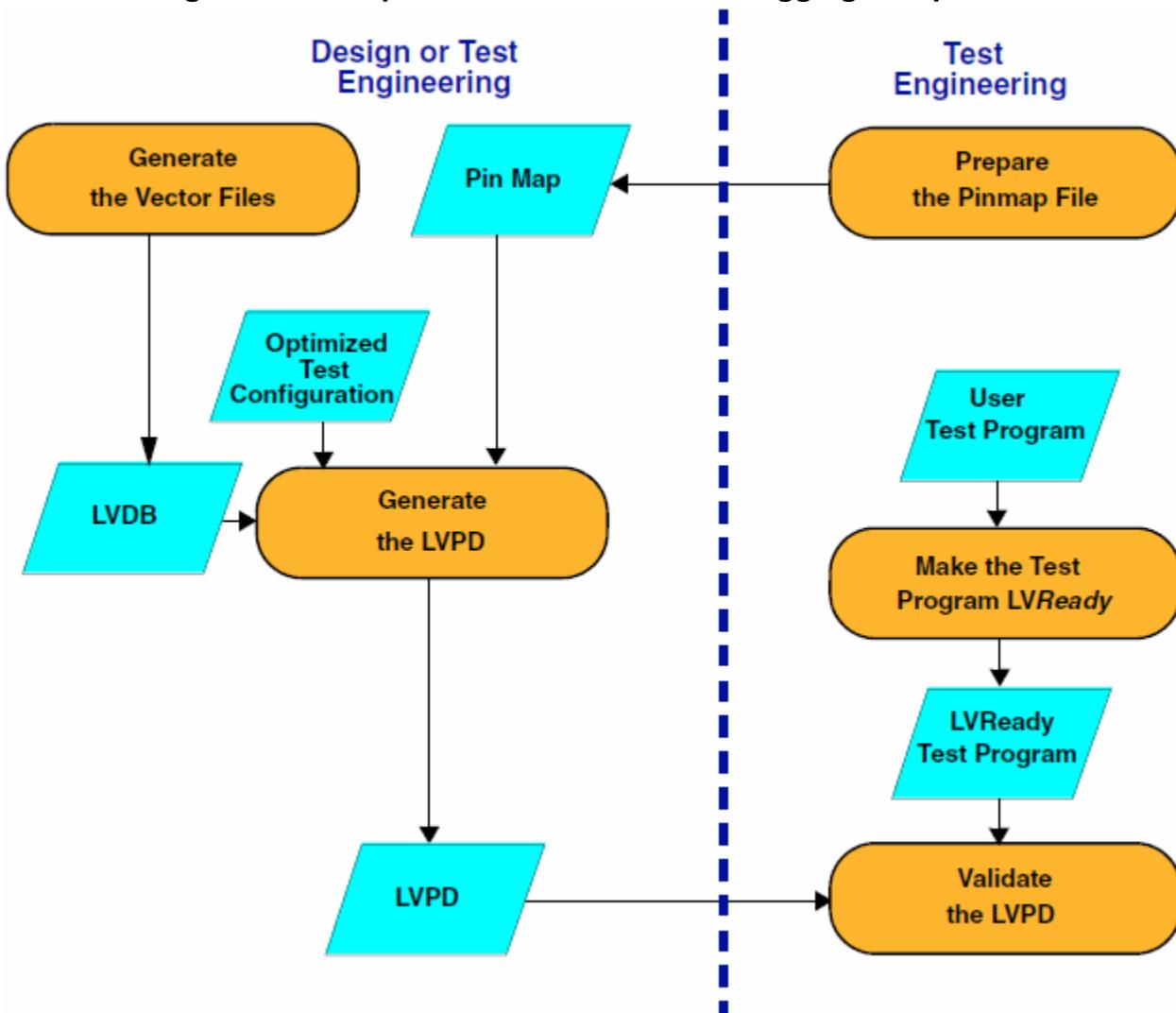
An error message is generated if your test configuration violates the above rules during the LVPD creation, and no LVPD is created.

Production Datalogging Setup Flow

The flow for setting up Production Datalogging is shown in [Figure 10-4](#). Although the entire flow is often performed by Test Engineering, it is sometimes desirable to have *Steps Generate Vector Files and Generate LVPD* performed by Design Engineering as they might have better insight in how to optimize the BIST tests.

In this flow, it is assumed that Tesson SiliconInsight software is not installed and available on the target test platform. If Tesson SiliconInsight software is running on the target test platform, then a different Production Datalogging setup flow can be used. For more details, refer to Chapter 9, “[Setting Up Tesson SiliconInsight ATE](#).”

Figure 10-4. Steps of the Production Datalogging Setup Flow



The Production Datalogging setup flow consists of the following four steps:

1. **Preparing the Pin Map File**—The Pin Map File specifies the mapping between the design pin names and the device pin names (also known as the *package* pin names). During this step, you will copy the starter Pin Map file template from the LVDB and modify this file in a text editor as needed.
2. **Generating the Vector Files**—In this step, you generate the vector files if your test configuration is set up to generate datalog for failing flip-flops.
3. **Generating the LVPD**—
4. **Making Your User Test Program LVReady**—In this step, you generate the LVPD using the Pin Map file and an optional Optimized Test Configuration file as inputs.
5. **Validating the LVPD**—In this step you load the test program and the LVPD on to the tester and run with an *open socket* device. This will generate the failure datalog that you

can examine. Once all components are validated, the LVPD and the *LVReady* test program can be handed off to manufacturing.

Once the LVPD is generated you are ready to run production test with the LVPD—Running production test with a LVPD on the test floor is no different than running the flow without it. Since the software routines that access the LVPD are embedded within the *LVReady* test program, you simply load the test program and execute the test flow. For the failing devices, detailed datalog is generated and stored on the disk for further processing for yield learning or failure analysis purposes.

Preparing the Pin Map File

The first step in setting up the Production Datalogging flow consists of preparing the Pin Map file as described in “[Creating a Tesson SiliconInsight Pin Map File](#).”

[Figure 10-5](#) provides an example of the Tesson SiliconInsight pin map file.

Figure 10-5. Example Tesson SiliconInsight Pin Map File

```
PinMap (snipp) {
    // DESIGN NAME      : ATE PinName
    trst_n           : TRST;
    tck              : TCK;
    tms              : TMS;
    tdi              : TDI;
    tdo              : TDO;
    rst_n            : in1;
    reset_n          : in2;
    p11106_lock     : out1;
    ptest(14)         : out2;
    ewrap_a          : out3;
    ptest(15)         : out4;
    ewrap_b          : out5;
    clk              : clk1;
    fclk106          : clk2;
}
..
```

Generating the Vector Files

This step of setting up the Production Datalogging flow is only required if the test configuration is setup to generate datalog for failing flip-flops. The vector files are needed to identify the failing flip-flop instances for datalog and to provide appropriate failing flip-flop identification outputs to the gateDiagnose tool for gate-level diagnostic.

To generate the vector files for a given LVDB, you call the ETVerify tool with the following arguments:

```
etv <design_name> -inputLVDBName <path to the LVDB> \
    -configFile <path to the etManufacturing File> \
    -lbistVectorDump On
```

The vector files (*.lbist_diag_vectors, *.lbist_flop_names, *.lbist_misr_vectors, *.lbist_prpg_vectors) will be generated in the **LV_WORKDIR** sub-directory located in the LVDB.

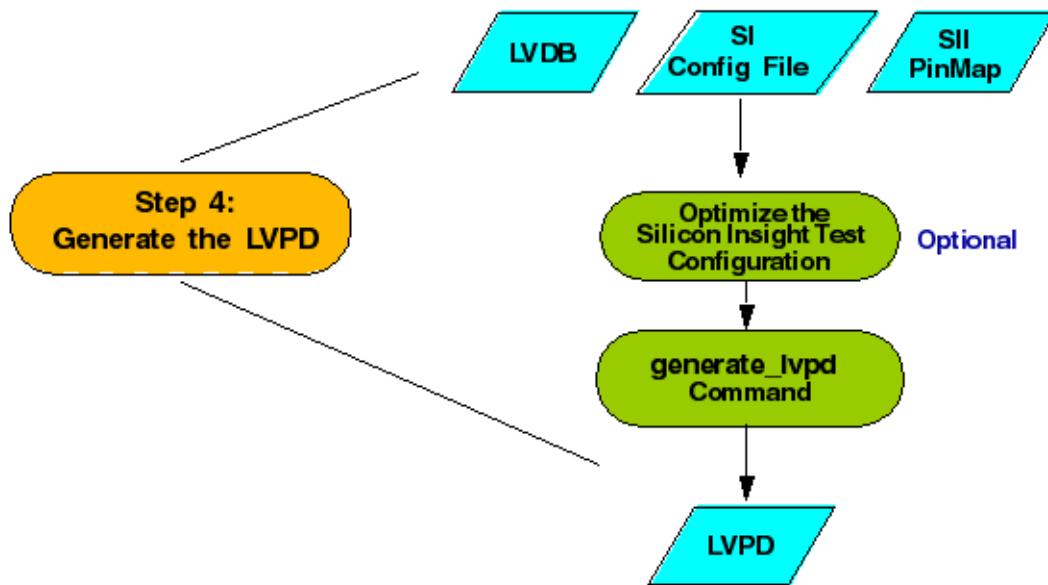
Generating the LVPD

In this step of setting up the Production Datalogging flow, you generate the LVPD using the data you have prepared in the earlier steps.

The operations you perform in this step are shown in [Figure 10-6](#) and summarized in the descriptions that follow the figure. An LVPD generated using the generate_lvpd command will not contain compiled binary ATE patterns since the ATE software is not used. Binary ATE patterns will be generated in the LVPD when the LVPD is used the first time.

An LVPD can also be generated directly from the Tessent SiliconInsight ATE software if you have this installed and running on your tester or tester emulator. For more details, refer to Chapter 9, “[Setting Up Tessent SiliconInsight ATE](#).”

Figure 10-6. Operations for Generating LVPD



Optimizing the Tesson SiliconInsight Test Configuration

During this *optional* operation, you can modify the test configuration so as to optimize the trade-off between test time and data collection needs. You will use the Tesson SiliconInsight GUI to optimize the test configuration. Refer to “[Editing Test Configurations](#)” for more information on how to create and edit a test configuration. The most common operations you might perform to optimize your test configuration are as follows:

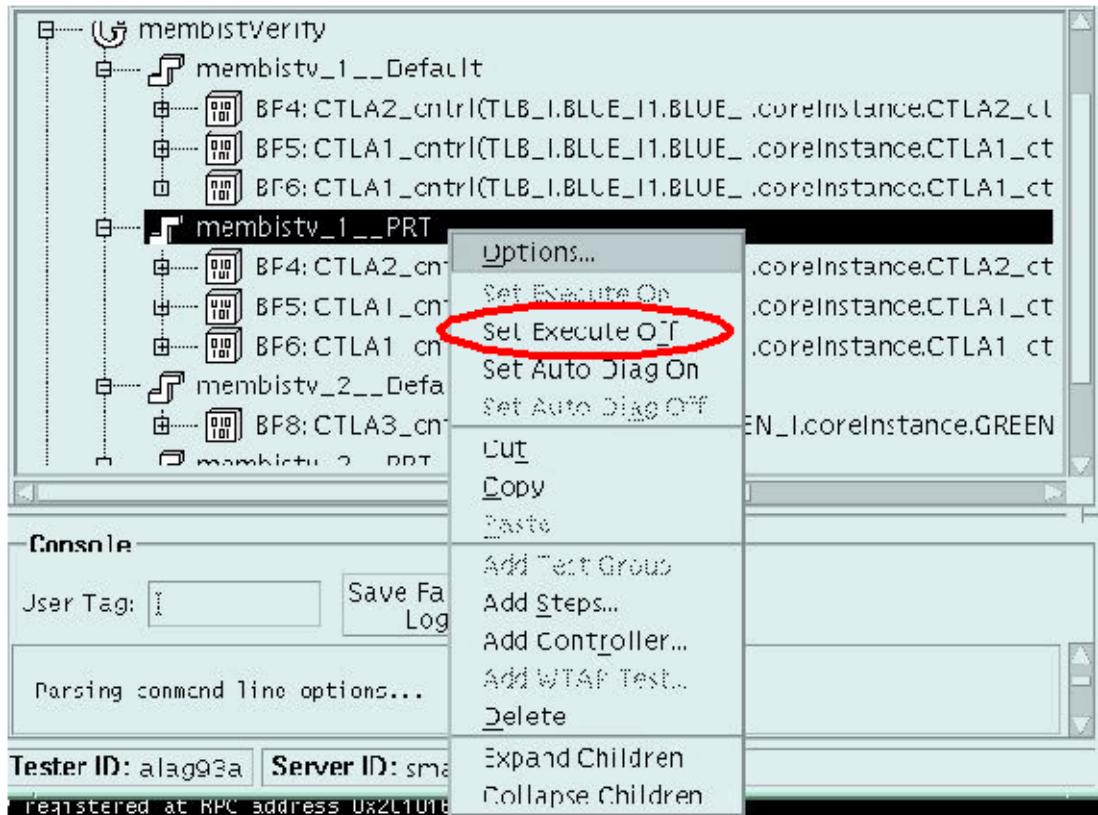
- [Disabling Test Steps](#)
- [Changing the BIST Controller Grouping](#)

Disabling Test Steps

It is not uncommon to include test steps in the Tesson SiliconInsight Test Configuration to only perform certain diagnostic functions. Disabling some of these steps when they are not needed can save test time.

To disable a particular test step, you need to select the test step with a left-mouse button click (LMB) and then click on the right-mouse button (RMB) to bring up the **Options** menu as shown in [Figure 10-7](#). You select the menu item **Set Execute Off** to disable a test step.

Figure 10-7. Disabling Execution of Test Steps

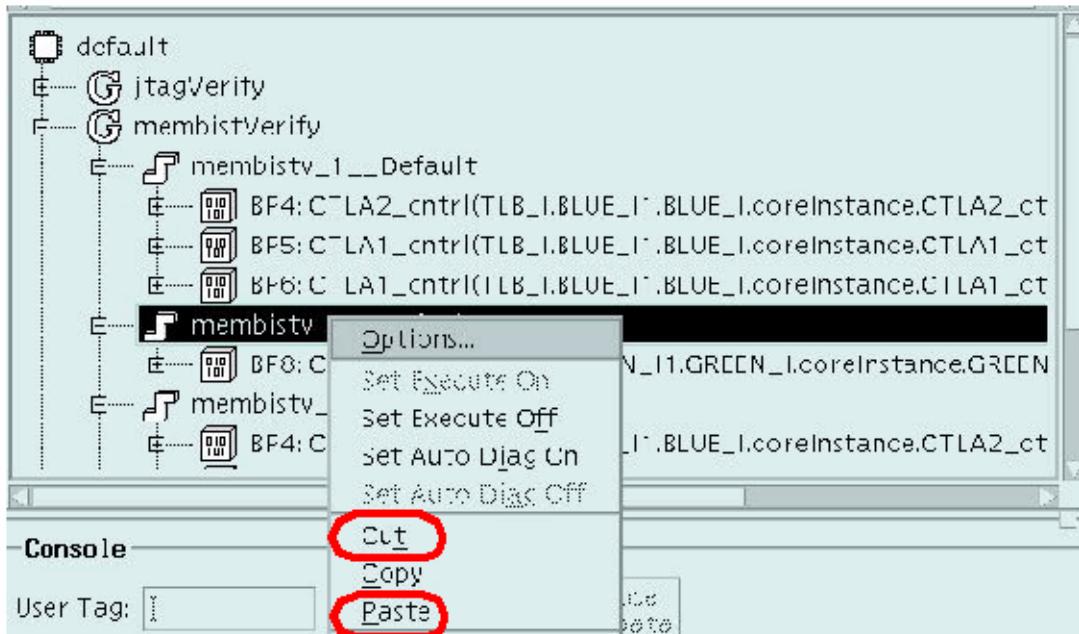


Changing the BIST Controller Grouping

Mentor Graphics' infrastructure allows you to run multiple BIST controllers in parallel in the same test step. Grouping many compatible controllers under a single test step allows you to minimize test time at the expense of increasing the chip's power consumption. You can use the **Cut** and **Paste** options of the Tessent SiliconInsight GUI to change the controller ordering. The **Cut** and **Paste** options can be found on the menu by clicking the RMB on any test step as shown in [Figure 10-8](#).

Alternatively, you might edit the *.etManufacturing* file, which is an ASCII (text) file that contains the controller grouping, in a text editor. Once you edit the *.etManufacturing* file, you can read that file into the Tessent SiliconInsight GUI by using the **File > Open Config** menu options. For detailed information on the *.etManufacturing* file, refer to the *ETVerify Tool Reference*.

Figure 10-8. Using the Cut and Paste Features of the Tessent SiliconInsight GUI



Using the generate_LVPD command

To generate an LVPD, you call the `generate_lvpd` command with the following arguments:

```
generate_lvpd -testerType <Flex/UltraFlex/J750/93000/...> \
    -lvdb <path to LVPD> \
    -configFile <path to the SI Config File> \
    -pinmapFile <path to the SI pinmap file>
```

The LVPD will be generated in a directory named by the following convention:

`<design name>_<SI Config name>_<ATE tester SW type>.lvpd`

Default Test Step File Example

The default test step file, `default.testStep`, is generated when ETVerify creates the Mentor Graphics database (LVDB). This file contains all test steps in the default test configuration file, `default.config_eta`, generated by the ETVerify tool. Use this file during test program generation to extract the test step names from this file and add support in the test program to execute and diagnose each test step in the default test configuration.

Figure 10-9 provides an example of the `default.testStep` file populated with test steps for BIST controllers.

Figure 10-9. Example `default.testStep` File

```
-----  
// This file created by: embeddedTestVerify  
// Software version: 6.0a SP2 Build 20070226.330  
// Created on: 03/12/07 13:34:55  
-----  
tapbistv_1_TestLogicReset  
tapbistv_1_InstReg  
tapbistv_1_IDReg  
tapbistv_1_BypassReg  
tapbistv_1_TAPIntDR  
tapbistv_1_BscanReg  
tapbistv_1_Input  
tapbistv_1_Sample  
tapbistv_1_HighZ  
tapbistv_1_OutputClamp  
membistv_1  
GainForceDown  
GainForceUp  
LockRangeMaxFreq  
LockTimeFromMaxFreq  
LockRangeMinFreq  
LockTimeFromMinFreq  
JitterLongTerm  
multi_asyncTest_retentionTest_1  
multi_asyncTest_retentionTest_2  
multi_asyncTest_retentionTest_3  
logicbistv_1  
logicbistv_2  
logicbistv_3
```

Making Your User Test Program LVReady

In this step of setting up the Remote Datalog flow, you make your user test program *LVReady* by editing the program to call one or more Tesson SiliconInsight APIs. In most cases, you need to invoke just two Tesson SiliconInsight APIs at the appropriate point in your test program.

1. *ETAStart()* API. This API is mandatory and must be the first API that is called from your test program before any other Tesson SiliconInsight APIs.
2. *ETAExecuteStep()* API and *ETAExecuteTestConfig()* API. You will then use a combination of calls to these APIs to build a flow using the tests in the LVPD.

The way in which the above APIs are accessed depends on the target tester platform. Detailed instructions on how to include and call these APIs are provided in “[User Test Program Changes for Specific Platforms](#).”

ETAStart() API

In order to invoke the Tesson SiliconInsight routines within the LVPD from your test program, you must first insert the *ETAStart()* API. This must be the first Tesson SiliconInsight API that the test program calls before calling any other.

The *ETAStart()* API sets up the link to the Tesson SiliconInsight routines. You need to provide the path to an LVPD when calling this API, even if the directory does not yet exist during the test program file edit process.

Note

 The LVPD directory path you provide must be a relative path, since the test program will typically be run on different locations during the manufacturing test. Specifically, you should not use absolute directory path for this argument.

This API should be placed in your test program so that it is called when the test program is initializing, after the device has been powered up.

ETAExecuteStep() API

The *ETAExecuteStep()* API can be called any time after the *ETAStart()* API has been called. The *ETAExecuteStep()* API allows you to execute a single test step in the Tesson SiliconInsight Test Configuration file. You must ensure that the device is powered up before this API is called. You can examine the results of the step execution returned by this API and take the appropriate action. For example, you might want to send the device to an appropriate bin or simply datalog the results to a file in a specific format.

The *ETAExecuteStep()* API should be called for every step in the Tesson SiliconInsight Test Configuration. You can determine the names of all the Test Steps in the default Test Configuration by referring to the *default.testStep* file in the LVDB of the device. For more information, refer to “[The Default Test Step File](#).”

ETAExecuteTestConfig() API

The *ETAExecuteTestConfig()* can be called any time after the *ETAStart()* API has been called. The *ETAExecuteTestConfig()* API allows you to execute all test steps in the Tesson SiliconInsight Test Configuration file and datalog the failures. You must ensure that the device is powered up before this API is called.

User Test Program Changes for Specific Platforms

This section details the changes that you must make to your test program to run with an LVPD for these ATE platforms:

- [Teradyne ATE \(IG-XL\)](#)
- [Verigy ATE \(SmarTest\)](#)

Teradyne ATE (IG-XL)

This section describes how to enhance an IG-XL Test Program to run on the Teradyne UltraFlex/Flex/J750 ATE Platforms running the IG-XL software:

- If the LVPD was generated using the command “generate_lvpd,” the test program is not *LVReady* yet. You must modify the test program as described in the next section.
- If the LVPD was generated through IG-XL, the test program is already *LVReady*, and you can proceed to “[Add Tesson SiliconInsight Test to the Flow Table](#)” to specify the path to the LVPD.

Modifying the Test Program

You must make the following changes to the IG-XL Test Program to make it *LVReady*:

Add Tesson SiliconInsight Timing Set

To add Tesson SiliconInsight timing set to your TimeSheet, follow these steps. The Timing set *must* be named as **ETA_TS**.

1. TimeSet ETA_TS will include all of the device signals (all those defined in ChannelMap Sheet) and will be set as follows for all pins:

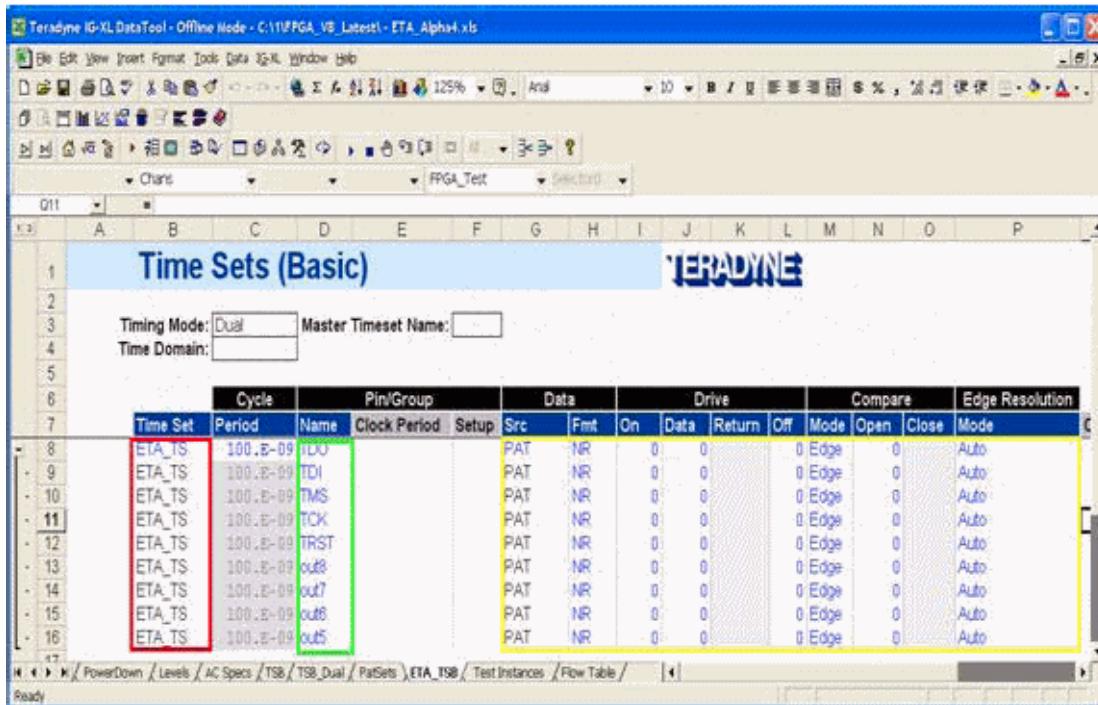
```
Data Src: Pat
Data Fmt: Fmt
Drive On: 0
Drive Data: 0
Drive Off: 0
Drive Return: 0
CompareMode: Edge
Compare Open: 0
Compare Close: (Grayed Out)
Mode: Machine (only for UltraFlex and Flex)
```



Note

Some fields might not be required (i.e., grayed out depending on the type of the signal).

Figure 10-10. Tessent SiliconInsight Timing Set

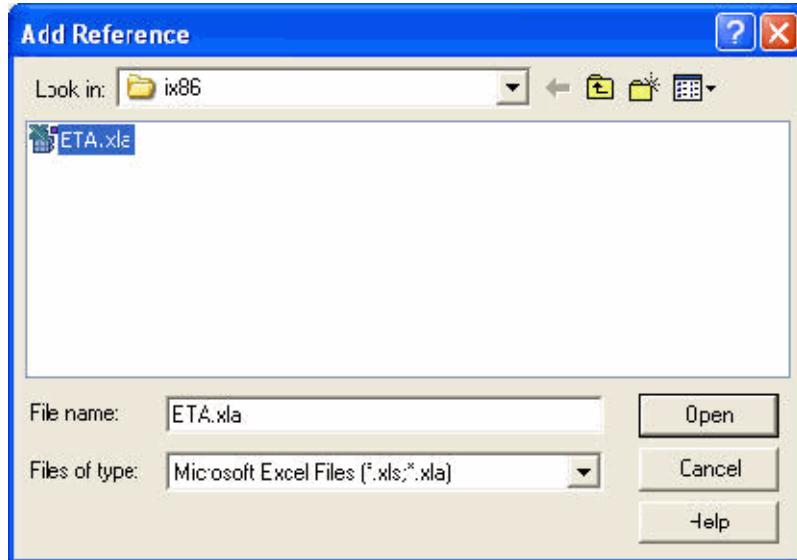


“Refer” to the Tessent SiliconInsight Add-in

To refer to the Tessent SiliconInsight add-in, follow these steps:

1. From IG-XL press **Alt-F11** to bring up the Visual Basic work environment.
2. Click on any sheet under the Test Program VBA project (i.e., <test program>.xls) and from the menu **Tools** click on menu item **References** to bring up the **References** dialog window.
3. Click on **Browse** and navigate to the following directory *<TP_DIR>/<design>.lvpd* and open the add-in file (*TP_DIR* is the directory which contains the test program):
 - o *ETA.xla* or *ETA_ULTRAFLEX.xla* for an UltraFlex job
 - o *ETA_FLEX.xla* for a Flex job
 - o *ETA_J750.xla* for a J750 job

Figure 10-11. Adding Reference to Tessian SiliconInsight Add-in



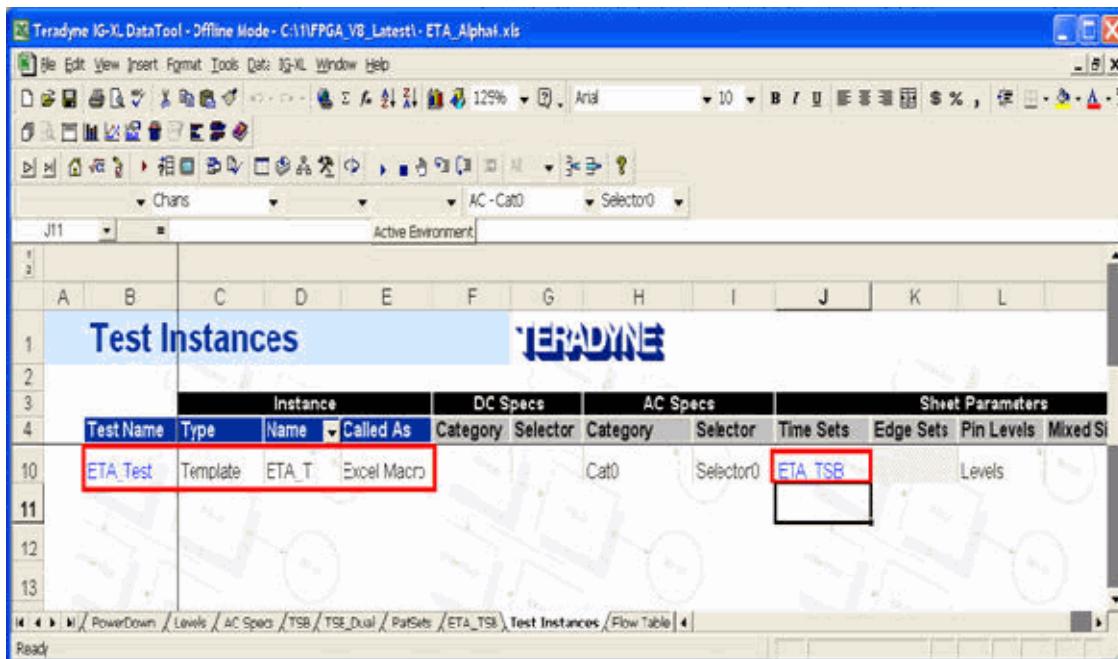
4. Make sure that the add-in is clicked in the references list. This will also appear as a VBA project in the VBA Project list.

Add a Tessian SiliconInsight Test Instance

To add a Tessian SiliconInsight test instance, perform the following steps:

1. Select the **Test Instances** sheet from IG-XL by clicking on the **Test Instances** tab at the bottom of the IG-XL main window.
2. In the **Test Name** field for the Tessian SiliconInsight test choose a name (for example, *ETA_Test*).
3. In the **Type** field, choose *VBT for UltraFlex/Flex. Template for J750*.
4. In the **Name** field, type in *ETA_T*.
5. In the **Called As** field, choose **Excel Macro** for J750. It is grayed out on *UltraFlex/Flex*.
6. For DCSpec, choose the *Specs* you want to run with.
7. For ACSpecs, choose the Timing Sheet which contains the Timing Set (i.e., *ETA_TS*) added for Tessian SiliconInsight in the previous steps.

Figure 10-12. Tessent SiliconInsight Test Instance

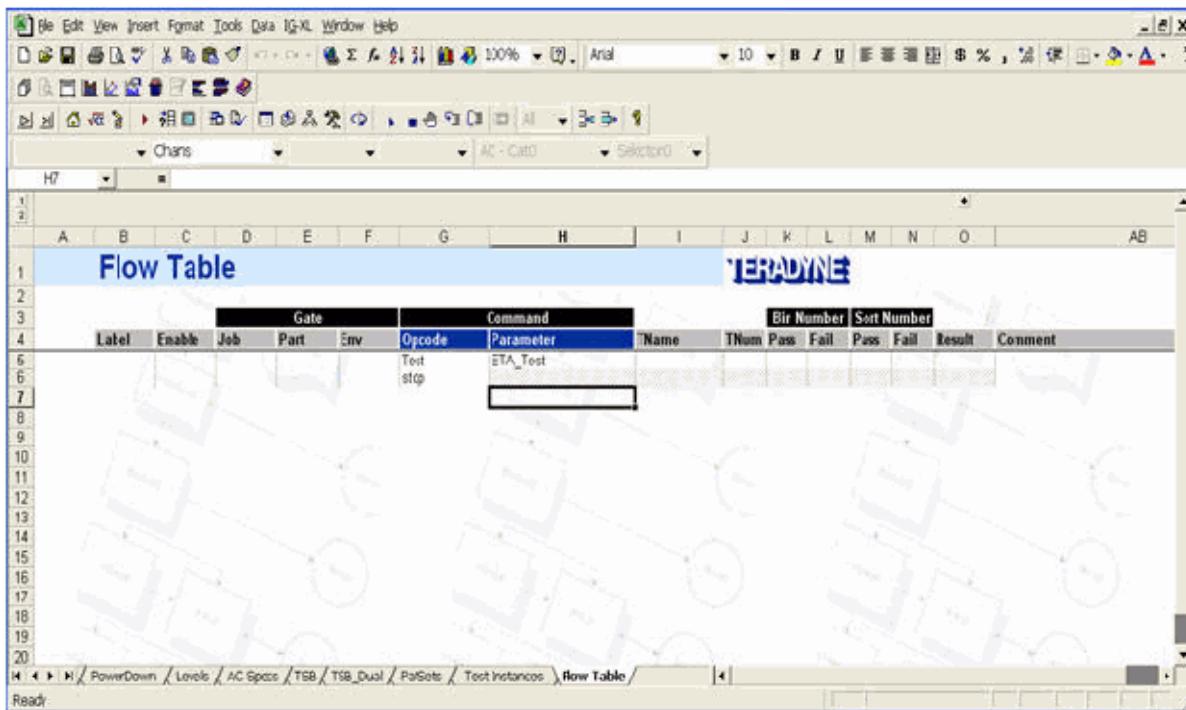


Add Tessent SiliconInsight Test to the Flow Table

To add a node to execute the Tessent SiliconInsight test just created in the Flow Table, perform the following steps:

1. Click on the **Flow Table** tab in the bottom of the IG-XL main window to bring up the Flow Table.
2. Insert a new row in the flow.
3. Select **Test** in the **Opcode** field.
4. Type in the name of the Tessent SiliconInsight test created before (i.e. *ETA_Test*) in the **Parameter** field.
5. Click the right-mouse button on the **Parameter** field for *ETA_Test*, click on the **Edit** sub-menu, and choose **Instance** to edit the parameters for the Tessent SiliconInsight test.
6. The Tessent SiliconInsight test dialog box will pop up where you type in the path (relative or absolute) to the LVPD.
7. Now Tessent SiliconInsight test is ready for execution.

Figure 10-13. Tessent SiliconInsight Test in the Job Test Flow



Verigy ATE (SmarTest)

This section describes how to enhance a SmarTest Test Program for Agilent 93k to use an LVPD:

If the LVPD was generated through the SmarTest SW, it is already *LVReady*, and you can skip to “[Making the Test Program LVReady](#).”

Otherwise, the LVPD was generated using the command “`generate_lvpd`”, the test program is not *LVReady*, and you must follow instructions starting with the section “[Enhancing the TestFlow](#).”

Making the Test Program LVReady

You run the script

`<ETA_INSTALL_PATH>/share/SiliconInsight/ATE/Agilent/bin/makeLVReady_93K` and pass the test program directory as argument to make the test program *LVReady*. This tool enhances the user test program as follows:

- Updates the user timing file with the timing waveforms used by Tessent SiliconInsight.
- Adds the Tessent SiliconInsight User Functions file (`lv_system_calls.c`) to `userproc_libs` directory of the test program.

Run makeLVReady_93K

The tool syntax is as follows:

```
makeLVReady_93K -timing <user timing file>
-replaceTiming -pinConfig <user configuration file> <user test program
directory>
```

The above command will update the timing file *<user timing file>* in the directory *<user test program directory>/timing* with the Tessian SiliconInsight waveform. The new timing file will replace the old one (i.e., *-replaceTiming* command). The user pin configuration file *<user configuration file>* in the directory *<user test program directory>/configuration* will be used to create the Tessian SiliconInsight waveforms.

Note

 If *makeLVReady_93K* is executed without any arguments, the manpage for it is displayed. This manpage provides information on all available commands and functions.

Compile Tessian SiliconInsight User Functions

Modify ONLY the parameter *ETA_LIB_DIR* in the Make file of the *<TP_DIR>/userproc_libs* to be “*..lv_setup/<LVPD_name>.lvpd*”. *LVPD_name* is the name of the LVPD in the *lv_setup* directory of the test program.

The following line is an example in the Makefile:

```
ETA_LIB_DIR = ..lv_setup/TOP_agilent_smallest.lvpd
```

Do not modify any other line.

Once the MakeFile is enhanced to compile the Tessian SiliconInsight user functions in addition to other user functions, it might be used as before to compile the user procedure library (i.e., “make clean all”).

Enhancing the TestFlow

The **TestFlow** might be enhanced to add Tessian SiliconInsight nodes to start Tessian SiliconInsight and, optionally, add nodes to execute different test steps. For all Tessian SiliconInsight nodes in the flow, you must select *ETA_SPEC* (i.e., equation set #99) for the timing, appropriate levels, and any seed pattern.

Flow Node to Start/Initialize Tessian SiliconInsight

You might add this test node in the flow and execute user procedure **start_eta** and pass the path to Test Program setup file. This node can be used to initialize Tessian SiliconInsight and pass control back to Tessian SiliconInsight GUI (if in Debug mode).

Flow Node to Execute ALL Tests in the Configuration

You might add a node to execute ALL the tests in the loaded Tesson SiliconInsight test configuration. This is done by calling **execute_config**.

Flow Node to Execute a Step

You might add a node to execute a specific test step from the loaded Tesson SiliconInsight test configuration. This is done by calling **execute_step <teststep name>**. If **execute_step** is called without an argument, it will provide a list of test steps that can be executed.

Flow Node to Save BIRA Data

You might add this node (usually at the end of the *Smartest* test program flow) to save accumulated BIRA data for a given DUT in a file. **save_and_clear_bira_data <file name> <X-coordinate> <Y-coordinate>** will save/append the accumulated BIRA data for DUT at X and Y coordinate in the file *<file name>*.

Flow Node to Provide Help Instructions on All Available Tesson SiliconInsight User Functions

You might execute the node **eta_help** (with no arguments) to provide instructions and directions for all available Tesson SiliconInsight user functions, including the ones described in the previous sections.

Using the TestMethod instead of using the UseProcedure — RHEL 3

You can use the TestMethod instead of the UseProcedure when you run SmarTest Version 4.3.6 or later on Red Hat Enterprise Linux 3.

Install the TestMethod for Tesson SiliconInsight

You find the file
<ETA_INSTALL_PATH>/share/SiliconInsight/examples/LV_FPGA_demo1/Agilent/common/LV_TestMethod_lnx.tgz and open (tar xzf) under your *<device_dir/TestMethod>* directory.

Build the TestMethod

Open the makefiles of the TestMethod and modify the following variables:

- **ETA_LVPD_DIR**: set to the absolute path to the LVPD directory
- **ETA_LINK_LVPD_LIB**: set to 1

Then, build (or rebuild) the TestMethod in the regular SmarTest flow.

How to Use in the SmarTest TestFlow

The methods are identical to the UserProcedure functions, and you can also refer to explanations about parameters the in the TestMethod GUI.

Using the TestMethod instead of the UseProcedure — RHEL 5

You can use the TestMethod instead of the UseProcedure when you run SmarTest Version 6.5.2 or later on Red Hat Enterprise Linux 5.

Install the TestMethod for Tesson SiliconInsight

You find the file

`<ETA_INSTALL_PATH>/share/SiliconInsight/examples/LV_FPGA_demo1/Agilent/common/LV_TestMethod_lnx-el5.tgz` and open (tar xzf) under your `<device_dir/TestMethod>` directory.

Build the TestMethod

Open the makefiles of the TestMethod and modify the following variables:

- `ETA_LVPD_DIR`: set to the absolute path to the LVPD directory
- `ETA_LINK_LVPD_LIB`: set to 1

Then, build (or rebuild) the TestMethod in the regular SmarTest flow.

How to Use in the SmarTest TestFlow

The methods are identical to the UserProcedure functions, and you can also refer to explanations about parameters the in the TestMethod GUI.

Validating the LVPD

In this final step of setting up the Production Datalogging flow, you load the test program on to the ATE to execute and validate that the LVPD contains all the data needed during manufacturing test.

This step should be run with actual silicon on the ATE platform. If the silicon is not yet available, you can run the test program “open socket” so that all the test steps in the test configuration will return failures. This helps you test your failure datalog scheme as well.

To validate your LVPD, perform the following operations:

1. Load your test program on to the ATE that has the actual silicon on the test head. If you do not have actual silicon at this point, you can leave it “open socket”.
2. Run the test program as you would normally do for a non-LVReady test program.
3. The test program will execute all the test steps in the test configuration and will create a failure datalog.
4. Examine the datalog output. If you plan to process the datalog for failure analysis or yield analysis purposes, you can use this output to verify your post-processing software.
5. You can then hand off the test program along with the LVPD to manufacturing.

6. For detailed failure analysis of any silicon coming off the production, you might use the interactive Tessent SiliconInsight software. Since your test program is already **LVReady**, there is only a minimal effort involved to use Tessent SiliconInsight to perform detailed diagnostics. For more details, refer to Chapter 9, “[Setting Up Tessent SiliconInsight ATE](#).”

Appendix A

Memory BIST Algorithms

Mentor Graphics provides a library of test patterns or algorithms for testing your memories. These algorithms represent some algorithms that you may perform on your memories using Tessent MemoryBIST **Programmable** and **Non-Programmable** controllers. You can use the detailed algorithm examples provided in this appendix as a basis for creating your own algorithms.

This appendix provides the following information about each algorithm:

- A brief description of the algorithm
- Algorithm length
- The controller address and data setup for the algorithm
- The algorithm sequence of instructions
- An example of the algorithm programming syntax
- Identifies the detected faults
- Identifies the availability of the algorithm

Any abbreviations used in this appendix are described in “[Notation Describing Memory BIST Algorithms](#).”

This appendix covers the following topics:

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LVMarchY Algorithm	347
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LVMarchLA Algorithm	358

LVRowBar Algorithm	364
LVColumnBar Algorithm	369
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LVGalColumn Algorithm	381
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LVCheckerboard1X1 Algorithm	397
LVCheckerboard4X4 Algorithm	402
LVWalkingPat Algorithm	407
LVBitSurroundDisturb Algorithm	413
LVAddressInterconnect Algorithm	429
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Notation Describing Memory BIST Algorithms

This appendix uses the notation described below for the memory BIST algorithms.

R0

Read current location and compare most significant output bit to *0*

R1

Read current location and compare most significant output bit to *1*

Rc

Read current location and compress contents into a MISR

W0

Write to current location, applying *0* to the least significant input bit

W1

Write to current location, applying *1* to the least significant input bit

(ROW1)B

A succession of read and write operations repeated for each bit in the data word slice

((FPROW1)B)C

A succession of read and write operations repeated for each bit in the data word slice in every column address location. Memory BIST uses fast page access to perform these read and write operations.

M

Multi-cycle delay (always equal to 4)

B

Number of bits per data slice

A

Number of address locations

R

Number of row address locations

C

Number of column address locations

BRC

Begin row cycle

ERC

End row cycle

Rx*

A succession of read operations that for calculation of the total test time becomes 2 idle clock cycles if the dynamic retention time does not require extra read operations.

%operationType

Number of clock cycles specified for an operation

Number of Instructions Required for Algorithms

Below is a list of required numbers of instructions for each of Mentor Graphics library algorithm. This information is useful if you are using *SoftProgramming* controllers and want to shift in a Mentor Graphics library algorithm.

- **LVAddressInterconnect** — 5 instructions

- **LVBitSurroundDisturb** — 7 instructions
- **LVCheckerboard1X1** — 2 instructions
- **LVCheckerboard4X4** — 2 instructions
- **LVColumnBar** — 2 instructions
- **LVDataInterconnect** — 16 instructions
- **LVGalColumn** — 6 instructions
- **LVGalPat** — 5 instructions
- **LVGalRow** — 6 instructions
- **LVMarchCMinus** — 3 instructions
- **LVMarchLA** — 5 instructions
- **LVMarchX** — 3 instructions
- **LVMarchY** — 4 instructions
- **LVRowBar** — 2 instructions
- **LWWalkingPat** — 4 instructions
- **ReadOnly** — 3 instructions
- **SMarch** — 14 instructions
- **SMarchCHKB** — 19 instructions
- **SMarchCHKBci** — 27 instructions
- **SMarchCHKBcil** — 49 instructions
- **SMarchCHKBvcd** — 90 instructions

The number of instructions are specified by the *NumberOfInstructions* property in the ETPlanner configuration file.

Correlating the Reported Instruction to the Algorithmic Phase

Tessent SiliconInsight Desktop issues failure reports similar to the following:

```
Failure#7: Expected 1 (<DATA_OUTPUT_PORT>[10] = 1), TestPort 1, Algorithm
T2_SMARCHCHKBCIL Instruction 38, row <ROW_NUM>, column <COLUMN_NUM>
(<ADDRESS_PORT>[12:0] = 0x05c9)
    Memory MEM1 (<MEMORY_CELL_NAME>),
    MemoryInstancePath (<MEMORY_INSTANCE_PATH>), Comparator 11
```

You can correlate the returned instruction, in this case Instruction 38, to an algorithmic phase by looking at the etassemble.log file. For example, the following log file indicates that Instruction 38 corresponds to phase 18. The "_PH_n" portion of the the instruction identifier indicates the algorithmic phase.

```
Including Algorithms from the Test Pattern Library...
Including the Library Test Pattern SMARCHCHKBCIL.

Validating all user specified algorithms and any included algorithms
from the library of test patterns...

Calculating the run length for algorithm SMARCHCHKBCIL...
Run Length Summary for the Algorithm SMARCHCHKBCIL used in Step 0
with BitSlice 1
    Instruction(INST0_IDLE_PH_1)
        Total Instruction Executions:      1.0
        Total Clocks:                      4.0
        ...
    Instruction(INS37_PH_18.1)
        Total Instruction Executions:      62.0
        Total Clocks:                      124.0
    Instruction(INS38_PH_18.2)
        Total Instruction Executions:      62.0
        Total Clocks:                      124.0
    Instruction(INS39_PH_18.3)
        Total Instruction Executions:      62.0
        Total Clocks:                      124.0
    ...
    ...
```

Available Library Algorithms

The following describes each algorithm in the Mentor Graphics algorithm library.

SMarch Algorithm

The SMarch algorithm is applicable to both **Programmable** and **Non-Programmable** controllers.

The SMarch algorithm is the default test algorithm that the memory BIST controller uses to test RAMs. The memory BIST controller performs all operations using fast row accesses. In a fast row count sequence, the column address remains constant until the memory BIST controller accesses all rows.

Table A-1 describes the SMarch algorithm per test port.

Table A-1. Description of SMarch Test Algorithm per Test Port

Phase	Address Sequence	Sequence	Operations Used	Description
1		Idle	None	Performs multi-cycle initialization.
2	1	(RxW1) ^B (R1W1)	ReadModifyWrite	Scans 1s through first word.
3	1	(R1W0) ^B (R0Rx)	ReadModifyWrite ReadRead	Scans 0s through first word.
4	2 to W Fast row	(W0Rx)	Write	Writes 0s in all other words.
5	1 to W Fast row	(R0W1) ^B (R1W1)	ReadModifyWrite	Reads 0s and replaces with 1s.
6	1 to w fast row	(R1W0) ^B (R0W0)	ReadModifyWrite	Reads 1s and replaces with 0s.
7	w to 1 fast row	(R0W1) ^B (R1Rx)	ReadModifyWrite ReadRead	Reads 0s and replaces with 1s, reverse address sequence. Does back-to-back reads before changing address.
8	W to 1 Fast row	(R1W0) ^B (R0Rx)	ReadModifyWrite ReadRead	Reads 1s and replace with 0s. Does back-to-back reads before changing address.
9	1 to W Fast row	(R0Wx) ^B (RxRx)	ReadModifyWrite ReadRead	Only the first read operation is significant. You can program the final RAM state using MemoryContents in the memory BIST configuration file.

Detected Faults

The SMarch algorithm detects the following failure modes:

- Stuck-at cell faults. A stuck-at fault is a single memory cell stuck at either a *logic 1* or a *logic 0*.
- Transition faults. A transition fault is a single memory cell that fails to transition from a *logic 0* to a *logic 1*, (or from a *logic 1* to a *logic 0*), when written with a *logic 1* (*logic 0*). Transition faults also include stuck-open access transistors.
- Unlinked dynamic coupling faults. One example of an unlinked coupling fault is a transition in one memory cell that causes a transition in a second memory cell.
- Address decoder faults. These faults result in any of the following: any given address does not access any cells; any given address simultaneously accesses multiple cells; and multiple addresses access a single cell.
- Read/Write logic faults. A Read/Write logic fault is a stuck-at fault in the Read/Write control logic.
- Parametric faults. Parametric faults include faults relating to access and cycle time, write recovery time, and some leakage faults that lead to data retention problems.
- Destructive Read faults. Destructive Read faults cause the contents of memory cell to be changed during a read access.
- Write recovery faults.
- Leakage faults leading to insufficient data retention.
- Multi-port specific faults. These faults include shorts between bit lines of different ports and shorts between different word lines of different ports. Specify **ShadowRead On** in the memory library file, to detect multi-port specific faults.

Test Time

The time required for the memory BIST controller to test your design using the SMarch algorithm depends on various factors: the number of clock cycles per operation, the number of bits per data slice, the number of row address locations, the number of column address locations, and the value specified for **ParallelRetentionTime**. You can calculate the test time using the equations in [Table A-2](#).

Table A-2. Test Time Calculation for SMarch Algorithm

Phase	Type	Time
1	Idle	4
2	Idle	$\% \text{ReadModifyWrite} * B + \% \text{ReadModifyWrite}$
3	Idle	$\% \text{ReadModifyWrite} * B + \% \text{ReadRead}$
4	Idle	$\% \text{WriteRead} * (R * C - 1)$
	Wait	Determined by ParallelRetentionTime in the ETVerify configuration file.
5		$\% \text{ReadModifyWrite} * B * R * C + (\% \text{ReadModifyWrite} * R * C)$
	Wait	Determined by ParallelRetentionTime in the ETVerify configuration file.

Table A-2. Test Time Calculation for SMarch Algorithm (cont.)

Phase	Type	Time
6		%ReadModifyWrite*B*R*C+(%ReadModifyWrite*R*C)
7		%ReadModifyWrite*B*R*C+(%ReadRead*R*C)
8		%ReadModifyWrite*B*R*C+(%ReadRead*R*C)
9		%ReadModifyWrite*B*R*C+(%ReadRead*R*C)

Specification

To test SRAMs using the SMarch algorithm, specify **Algorithm** SMarch in the memory library file.

Related Information

[Notation Describing Memory BIST Algorithms](#)

ReadOnly Algorithm

The ReadOnly algorithm is applicable to both **Programmable** and **Non-Programmable** controllers.

The ReadOnly algorithm is the default test algorithm that the memory BIST controller uses to test ROMs. The ReadOnly algorithm is a simple two-pass algorithm that reads and compresses the ROM contents by traversing the address space in both ascending and descending order.

For ROMs with multiple read ports, memory BIST provides separate MISRs for each port and repeats the test for each port while performing shadow reads on the inactive ports. Shadow reads perform normal read operations to strategic addresses but do not compress the results.

The memory BIST controller performs all operations using fast row accesses. In a fast row count sequence, the column address remains constant until the memory BIST controller accesses all rows.

[Table A-3](#) describes the ReadOnly algorithm per test port.

Table A-3. Description of ReadOnly Test Algorithm per Test Port

Phase	Address Sequence	Sequence	Operations Used	Description
1		Idle	None	Performs multi-cycle initialization.
2	1 to W Fast column	(Rc)	<i>Read</i>	Reads and compresses the ROM contents.
3	W to 1 Fast column	(Rc)	<i>Read</i>	Reads and compresses the ROM contents in reverse address sequence.
4	N/A	(MISR Compare)	<i>CompareMISR</i>	Compares the GO bit based on the final signature.

Detected Faults

The ReadOnly algorithm detects the following failure modes:

- Stuck to opposite value cell faults. A stuck to opposite value fault is a single memory cell stuck at a *logic 1* when the expected value is a *logic 0* (or stuck at a *logic 0* when the expected value is a *logic 1*).
- Address decoder faults. These faults result in any of the following: any given address does not access any cells, any given address simultaneously accesses multiple cells, and multiple addresses access a single cell.

Test Time

The time required for the memory BIST controller to test your design using the ReadOnly algorithm depends on two factors: the number of clock cycles per operation and the number of address locations. You can calculate the test time using the equations in [Table A-4](#).

Table A-4. Test Time Calculation for ReadOnly Algorithm

Phase	Type	Time
1	Idle	M (always=4)
2		%Read*A
3		%Read*A
4		%CompareMISR

Specification

To test ROMs using the ReadOnly algorithm, specify **Algorithm** as ReadOnly in the memory library file.

Related Information

[Notation Describing Memory BIST Algorithms](#)

SMarchCHKB Algorithm

The SMarchCHKB algorithm is applicable to both **Programmable** and **Non-Programmable** controllers.

When you specify **Algorithm** equal to SMarchCHKB, the memory BIST controller performs all operations using either fast column or fast row accesses. In a fast row count sequence, the column address remains constant until the memory BIST controller accesses all of the rows. In a fast column count sequence, the row address remains constant until the memory BIST controller accesses all of the columns.

In the algorithm description, Phases 2 and 3 ensure that the memory BIST controller can access the memory by writing and reading to the first address location. Phases 5, 6, and 7 use normal cycles with a checkerboard pattern. The *0s* and *1s* in the other phases refer to solid zero and solid one patterns.

Table A-5 describes the SMarchCHKB algorithm per test port.

Table A-5. Description of SMarchCHKB Test Algorithm per Test Port

Phase	Address Sequence	Sequence	Operations Used	Description
1		Idle	None	Performs multi-cycle initialization.
2	1	$(RxW1)^B$ ($R1W1$)	ReadModifyWrite	Scans <i>1s</i> through first word.
3	1	$(R1W0)^B$ ($R0Rx$)	ReadModifyWrite ReadRead	Scans <i>0s</i> through first word.
4		Idle	None	Performs multi-cycle initialization.
5	1 to R fast column	$((RxW0)^B)^C + (Rx^*)$	ReadModifyWrite	Writes checkerboard background data.
	-	Optional Wait	None	Pauses the test bench to perform the static retention test. (There is no hardware in the controller that performs the static retention test.)
6	1 to R fast column	$((R0W1)^B)^C + (Rx^*)$	ReadModifyWrite	Reads checkerboard background, and replaces it with inverse checkerboard data.

Table A-5. Description of SMarchCHKB Test Algorithm per Test Port (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
	-	Optional Wait	None	Pauses the test bench to perform the static retention test. (There is no hardware in the controller that performs the static retention test.)
7	1 to R fast column	$((R1W0)^B)^C + (Rx^*)$	ReadModifyWrite	Reads inverse checkerboard data. Memory contents are now a don't care.
8	-	Idle	None	Performs multi-cycle initialization.
9	1	$(RxW0)^B (R0Rx)$	ReadModifyWrite ReadRead	Scans 0s through first word.
10	2 to W fast row	$(W0R0)$	Write	Writes 0s in all other words.
11	1 to W fast row	$(R0W1)^B (R1W1)$	ReadModifyWrite	Reads 0s and replaces with 1s.
12	1 to W fast row	$(R1W0)^B (R0W0)$	ReadModifyWrite	Reads 1s and replaces with 0s.
13	W to 1 fast row	$(R0W1)^B (R1Rx)$	ReadModifyWrite ReadRead	Reads 0s and replaces with 1s. Does back-to-back reads before changing address.
14	W to 1 fast row	$(R1W0)^B (R0Rx)$	ReadModifyWrite ReadRead	Reads 1s and replaces with 0s. Does back-to-back reads before changing address.
15	1 to W fast row	$(R0Wx)^B$	ReadModifyWrite	Only the first read operation is significant. You can program the final RAM state using MemoryContents in the memory BIST configuration file.

Detected Faults

The SMarchCHKB algorithm detects the following failure modes:

- Stuck-at cell faults. A stuck-at fault is a single memory cell stuck at either a logic “1” or a logic “0”.
- Transition faults. A transition fault is a single memory cell that fails to transition from a *logic 0* to a *logic 1*, (or from a *logic 1* to a *logic 0*), when written with a *logic 1* (*logic 0*). Transition faults also include stuck-open access transistors.
- Unlinked dynamic coupling faults. One example of an unlinked coupling fault is a transition in one memory cell that causes a transition in a second memory cell.
- Address decoder faults. These faults result in any of the following: any given address does not access any cells; any given address simultaneously accesses multiple cells; and multiple addresses access a single cell.
- Read/Write logic faults. A Read/Write logic fault is a stuck-at fault in the Read/Write control logic.
- Parametric faults. Parametric faults include faults relating to access and cycle time, write recovery time, and some leakage faults that lead to data retention problems.
- Destructive Read faults. Destructive Read faults cause the contents of a memory cell to be changed during a read access.
- Write recovery faults.
- Leakage faults leading to insufficient data retention.
- Multi-port specific faults. These faults include shorts between bit lines of different ports and shorts between different word lines of different ports. Specify **ShadowRead On** in the memory library file, to detect multi-port specific faults.
- Neighborhood Pattern Sensitive Faults (NPSF). These faults are caused when the content of a cell is influenced by the content of other cells in their neighborhood.

Test Time

The time required for the memory BIST controller to test your design using the SMarchCHKB algorithm depends on various factors: the number of clock cycles per operation, the number of bits per data slice, the number of row address locations, the number of column address locations, and the value specified for **ParallelRetentionTime**. You can calculate the test time using the equations in [Table A-6](#).

Table A-6. Test Time Calculation for SMarchCHKB Algorithm

Phase	Type	Time
1	Idle	4
2	Idle	%ReadModifyWrite*B+%ReadModifyWrite
3	Idle	%ReadModifyWrite*B+%ReadRead
4		4

Table A-6. Test Time Calculation for SMarchCHKB Algorithm (cont.)

Phase	Type	Time
5		$\% \text{ReadModifyWrite} * B * R * C + R$
	Wait	Determined by ParallelRetentionTime in the ETVerify configuration file.
6		$\% \text{ReadModifyWrite} * B * R * C + R$
	Wait	Determined by ParallelRetentionTime in the ETVerify configuration file.
7		$\% \text{ReadModifyWrite} * B * R * C + R$
8		4
9		$\% \text{ReadModifyWrite} * B + \% \text{ReadRead}$
10	Idle	$\% \text{WriteRead} * (R * C - 1)$
11		$\% \text{ReadModifyWrite} * B * R * C + (\% \text{ReadModifyWrite} * R * C)$
12		$\% \text{ReadModifyWrite} * B * R * C + (\% \text{ReadModifyWrite} * R * C)$
13		$\% \text{ReadModifyWrite} * B * R * C + (\% \text{ReadRead} * R * C)$
14		$\% \text{ReadModifyWrite} * B * R * C + (\% \text{ReadRead} * R * C)$
15		$\% \text{ReadModifyWrite} * B * R * C$

Specification

To test SRAMs using the SMarchCHKB algorithm, specify **Algorithm SMarchCHKB** in the memory library file.

Related Information

Notation Describing Memory BIST Algorithms	ShadowRead
Algorithm	OperationSet
MemoryType	MemoryContents
ROMContentsFile	

SMarchCHKBci Algorithm

The SMarchCHKBci algorithm is applicable to both **Programmable** and **Non-Programmable** controllers.

This algorithm is similar to the SMarchCHKB test algorithm, and accommodates synchronous and asynchronous SRAMs with single or multiple ReadWrite ports. The algorithm is capable of detecting signal coupling between bitlines of adjacent columns and port interference faults that are caused by high resistance ground connections to one of the N-channel source terminals.

A few steps are added to the current algorithm to make sure that the appropriate data combinations are applied to every cell. The entire algorithm is shown in [Table A-7](#).

Table A-7. Description of SMarchCHKBci Test Algorithm per Test Port

Phase	Address Sequence	Sequence	Operations Used	Description
1		Idle	<i>None</i>	
2	1	$(RxW1)^B$ ($R1W1$)	<i>ReadModifyWrite</i>	Scans 1s through First word.
3	1	$(R1W0)^B(R0Rx)$	<i>ReadModifyWrite</i> <i>ReadRead</i>	Scans 0s through First word. A back to back reads is performed before changing address.
4		Idle	<i>None</i>	Performs Multi-Cycle Initialization
5	1 to R Fast column	$((RxW0)^B)^C$	<i>ReadModifyWrite</i>	Writes Checkerboard background data.
5.5	1 to R Fast column	$(R0W0)^B$ C (Rx^*)	<i>ShadowWrite</i>	Reads the checkerboard background. Writes checkerboard data.
	-	Optional Wait	<i>None</i>	Pauses the test to perform the static retention test.
6	1 to R Fast column	$((R0W1)^B)^C$	<i>ReadModifyWrite</i>	Reads checkerboard background. Replaces it with inverse-Checkerboard.
6.5	1 to R Fast column	$((R1W1)^B)^C + (Rx^*)$	<i>ShadowWrite</i>	Reads Inverse Checkerboard Pattern, Write Inverse Checkerboard Pattern.

Table A-7. Description of SMarchCHKBci Test Algorithm per Test Port (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
	-	Optional Wait	<i>None</i>	Pauses the test to perform the static retention test.
7	1 to R Fast column	$((R1W0)^B)^C + (Rx^*)$	<i>ReadModifyWrite</i>	Reads Inverse Checkerboard data, replaces it with checkerboard data.
8	-	Idle	<i>None</i>	Performs Multi-cycle initialization.
9	1	$(RxW0)^B (R0Rx)$	<i>ReadModifyWrite</i> <i>ReadRead</i>	Scans 0s through the first word. A back to back reads is performed before changing address.
10	2 to W Fast row	$(W0R0)$	<i>Write</i>	Writes 0s in all words.
11	1 to W Fast row	$(R0W1)^B (R1W1)$	<i>ReadModifyWrite</i>	Reads all 0s replaces them with 1s.
12	1 to W Fast row	$(R1W0)^B (R0W0)$	<i>ReadModifyWrite</i>	Reads 1s, and replaces them with 0s.
13	w to 1 Fast row	$(R0W1)^B (R1Rx)$	<i>ReadModifyWrite</i> <i>ReadRead</i>	Reads 0s, and replaces them with 1s. A back to back reads is performed before changing address.
14	w to 1 Fast row	$(R1W0)^B (R0Rx)$	<i>ReadModifyWrite</i> <i>ReadRead</i>	Reads 1s, and replaces them with 0s. A back to back reads is performed before changing address.
15	w to 1	$(R0W0)^B$	<i>ShadowWrite</i>	Reads 0. Writes 0.
16	1 Fast row	$(RxW1)^B (R1Rx)$	<i>ReadModifyWrite</i> <i>ReadRead</i>	Writes 1 through the first word. A back to back reads is performed before changing address.

Table A-7. Description of SMarchCHKBci Test Algorithm per Test Port (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
17	2 to W Fast row	(W1R1)	<i>Write</i>	Writes 1 to all locations.
18	1 to W Fast row	(R1W1) ^B	<i>ShadowWrite</i>	Reads 1 and write it back.
19	1	(R1Wmemcontents) ^B (WmemcontentsRx)	<i>ReadModifyWrite</i> <i>Write</i>	Writes the memory content into the first word (default 0), and writes it back.
20	2 to W Fast row	(Wmemcontents Rmemcontents)	<i>Write</i>	Writes memory contents to the rest of the memory (default 0).

Detected Faults

The SMarchCHKBci algorithm detects the following failure modes:

- Stuck-at cell faults. A stuck-at fault is a single memory cell stuck at either a logic 1 or a logic 0.
- Transition faults. A transition fault is a single memory cell that fails to transition from a logic 0 to a logic 1, (or from a logic 1 to a logic 0), when written with a logic 1 (logic 0). Transition faults also include stuck-open access transistors.
- Unlinked dynamic coupling faults. One example of an unlinked coupling fault is a transition in one memory cell that causes a transition in a second memory cell.
- Address decoder faults. These faults result in any of the following: any given address does not access any cells; any given address simultaneously accesses multiple cells; and multiple addresses access a single cell.
- Read/Write logic faults. A Read/Write logic fault is a stuck-at fault in the Read/Write control logic.
- Parametric faults. Parametric faults include faults relating to access and cycle time, write recovery time, and some leakage faults that lead to data retention problems.
- Destructive Read faults. Destructive Read faults cause the contents of a memory cell to be changed during a read access.
- Write recovery faults.
- Leakage faults leading to insufficient data retention.
- Single-port bitline coupling. Coupling between bitlines of adjacent columns that causes read errors when accessing cells with minor manufacturing defects.
- Multi-port specific. Bitline shorts and wordline shorts. Shorts between bit lines of different ports and shorts between wordlines of different ports. Specify **ShadowRead On** in the memory library file to detect these faults. Note that some restrictions apply.
- Multi-port specific. Port-interference faults. This fault can be caused by high resistance ground connections to one of the N-channel source terminals.
- Multi-port specific. Inter-port bitline coupling. Coupling between bitlines of different ports and within the same column. Specify **ShadowWrite On** and **ShadowWriteOK On** in the memory library file to detect these faults. Note that some restrictions apply.
- Neighborhood Pattern Sensitive Faults (NPSF). These faults are caused when the content of a cell is influenced by the content of other cells in their neighborhood.

Test Time

The time required for the memory BIST controller to test your design using the SMarchCHKBci algorithm depends on various factors: the number of clock cycles per operation, the number of bits per data slice, the number of row address locations and the number of column address locations. You calculate the test time using the equations in [Table A-8](#).

Table A-8. Test Time Calculation for SMarchCHKBci Algorithm Specification

Phase	Type	Time
1	Idle	4

Table A-8. Test Time Calculation for SMarchCHKBci Algorithm Specification (cont.)

Phase	Type	Time
2	Idle	$\% \text{ReadModifyWrite}^* B + \% \text{ReadModifyWrite}$
3	Idle	$\% \text{ReadModifyWrite} * B + \% \text{ReadRead}$
4		4
5		$\% \text{ReadModifyWrite} * B * R * C$
5.5		$\% \text{ReadModifyWrite}^* B^* R^* C + 2 * R + R$
	wait	Determined by ParallelRetentionTime in the ETVerify configuration file.
6		$\% \text{ReadModifyWrite} * B * R * C$
6.5		$\% \text{ReadModifyWrite}^* B^* R^* C + 2 * R + R$
	wait	Determined by ParallelRetentionTime in the ETVerify configuration file.
7		$\% \text{ReadModifyWrite}^* B^* R^* C + R$
8		4
9		$\% \text{ReadModifyWrite}^* B + \% \text{ReadRead}$
10	Idle	$\% \text{WriteRead}^*(R^*C - 1)$
11		$\% \text{ReadModifyWrite}^* B^* R^* C + (\% \text{ReadModifyWrite}^* R^* C)$
12		$\% \text{ReadModifyWrite}^* B^* R^* C + (\% \text{ReadModifyWrite}^* R^* C)$
13		$\% \text{ReadModifyWrite}^* B^* R^* C + (\% \text{ReadRead}^* R^* C)$
14		$\% \text{ReadModifyWrite}^* B^* R^* C + (\% \text{ReadRead}^* R^* C)$
15		$\% \text{ReadModifyWrite}^* B^* R^* C$
16		$\% \text{ReadModifyWrite}^* B + \% \text{ReadRead}$
17		$\% \text{Write} * B * (R * C - 1)$
18		$\% \text{ReadModifyWrite}^* B^* R^* C$
19		$\% \text{ReadModifyWrite}^* B + \% \text{Write}$
20		$\% \text{Write}^*(R^*C - 1)$

Specification

To test SRAMs using the SMarchCHKBci algorithm, specify **Algorithm SMarchCHKBci** in the memory library file.

Related Information

[Notation Describing Memory BIST Algorithms](#) [Algorithm](#)

SMarchCHKBcil Algorithm

The SMarchCHKBcil algorithm is applicable to both **Programmable** and **Non-Programmable** controllers.

This algorithm is similar to the *SMarchCHKBci* test algorithm and accommodates synchronous and asynchronous memories with single or multiple *ReadWrite* ports. The algorithm is capable of detecting bitline and wordline current leakage defects in single and multi-port memories.

A few steps are added to the current algorithm to make sure that the appropriate data combinations are applied to every cell. The Table A-9 shows the entire algorithm.

Table A-9. Description of SMarchCHKBcil Test Algorithm per Test Port

Phase	Address Sequence	Sequence	Operations Used	Description
1		Idle	<i>None</i>	
2	1	$(RxW1)^B$ ($R1W1$)	<i>ReadModifyWrite</i>	Scans 1s through First word.
3	1	$(R1W0)^B(R0Rx)$	<i>ReadModifyWrite</i> <i>ReadRead</i>	Scans 0s through First word. A back to back reads is performed before changing address.
4		Idle	<i>None</i>	Performs Multi-Cycle Initialization
5	1 to R Fast column	$((RxW0)^B)^C$	<i>ReadModifyWrite</i>	Writes Checkerboard background data.
5.5	1 to R Fast column	$(R0W0)^B$ (Rx^*)	<i>ReadModifyWrite</i> <i>ShadowWrite</i>	Reads the checkerboard background. Writes checkerboard data.
	-	Optional Wait	<i>None</i>	Pauses the test to perform the static retention test.
6	1 to R Fast column	$((R0W1)^B)^C$	<i>ReadModifyWrite</i>	Reads checkerboard background. Replaces it with inverse-Checkerboard.
6.5	1 to R Fast column	$((R1W1)^B)^C +$ (Rx^*)	<i>ReadModifyWrite</i> <i>ShadowWrite</i>	Reads Inverse Checkerboard Pattern. Writes Inverse Checkerboard Pattern.

Table A-9. Description of SMarchCHKBcil Test Algorithm per Test Port (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
	-	Optional Wait	<i>None</i>	Pauses the test to perform the static retention test.
7	1 to R Fast column	$((R1W0)^B)^C + (Rx^*)$	<i>ReadModifyWrite</i>	Reads Inverse Checkerboard data, replaces it with checkerboard data.
8	-	Idle	<i>None</i>	Performs Multi-cycle initialization.
9	1	$(RxW0)^B$ ($R0Rx$)	<i>ReadModifyWrite</i> <i>ReadRead</i>	Scans 0s through the first word. A back to back reads is performed before changing address.
10	2 to w Fast row	$(W0R0)$	<i>Write</i>	Writes 0s in all words.
11	1 to w Fast row	$(R0W1)^B$ ($R1W1$)	<i>ReadModifyWrite</i>	Reads all 0s, replaces them with 1s.
12	1 to w Fast row	$(R1W0)^B$ ($R0W0$)	<i>ReadModifyWrite</i>	Reads 1s, and replaces them with 0s.
13	w to 1 Fast row	$(R0W1)^B$ ($R1Rx$)	<i>ReadModifyWrite</i> <i>ReadRead</i>	Reads 0s, and replaces them with 1s. A back to back reads is performed before changing address.
14	w to 1 Fast row	$(R1W0)^B$ ($R0Rx$)	<i>ReadModifyWrite</i> <i>ReadRead</i>	Reads 1s, and replaces them with 0s. A back to back reads is performed before changing address.

Table A-9. Description of SMarchCHKBcil Test Algorithm per Test Port (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
15	1 to w Fast row	$(R0W1)^B(R0Rx)$ $(R1W0)^B$	<i>ReadModifyWrite</i> <i>ReadRead</i> <i>ReadModifyWrite</i> <i>ShadowWrite</i>	This phase is composed of three operations. For all operations, the column address is constant. The first set of operations is a Read 0, followed by a Write 1. The second set of operations is to perform two back to back Read 0 from a different row (on the same column). However, the result of the second read operation is not compared. The third set of operations is to Read a 1 from the current row and then restore its value to 0.
16	1	$(RxW1)^B(R1Rx)$	<i>ReadModifyWrite</i> <i>ReadRead</i>	Writes 1 through the first word. A back to back reads is performed before changing address.
17	2 to w	$(W1R1)$	<i>Write</i>	Writes 1 to all locations.

Table A-9. Description of SMarchCHKBcil Test Algorithm per Test Port (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
18	1 to w fast row	$(R1W0)^B(R1Rx)$ $(R0W1)^B$	<i>ReadModifyWrite</i> <i>ReadRead</i> <i>ReadModifyWrite</i> <i>ShadowWrite</i>	This phase is composed of three operations. For all operations, the column address is constant. The first set of operations is a Read 1 followed by a Write 0. The second set of operations is to perform two back to back Read 1 from a different row. However, the result of the second read operation is not compared. The third set of operations is to Read a 0 from the current row and then restore its value to 1.
19	1	$(RxWmemcontents)^B$ $(WmemcontentsRx)$	<i>ReadModifyWrite</i> <i>Write</i>	Writes the memory content into the first word (default 0), and writes it back.
20	2 to w	Wmemcontents Rmemcontents	<i>Write</i>	Writes memory contents to the rest of the memory (default 0).

Detected Faults

The SMarchCHKBcil algorithm detects the following failure modes:

- Stuck-at cell faults. A stuck-at fault is a single memory cell stuck at either a logic 1 or a logic 0.
- Transition faults. A transition fault is a single memory cell that fails to transition from a logic 0 to a logic 1, (or from a logic 1 to a logic 0), when written with a logic 1 (logic 0). Transition faults also include stuck-open access transistors.
- Unlinked dynamic coupling faults. One example of an unlinked coupling fault is a transition in one memory cell that causes a transition in a second memory cell.
- Address decoder faults. These faults result in any of the following: any given address does not access any cells; any given address simultaneously accesses multiple cells; and multiple addresses access a single cell.
- Read/Write logic faults. A Read/Write logic fault is a stuck-at fault in the Read/Write control logic.
- Parametric faults. Parametric faults include faults relating to access and cycle time, write recovery time, and some leakage faults that lead to data retention problems.
- Destructive Read faults. Destructive Read faults cause the contents of a memory cell to be changed during a read access.
- Write recovery faults.
- Leakage faults leading to insufficient data retention.
- Single-port bitline coupling. Coupling between bitlines of adjacent columns that causes read errors when accessing cells with minor manufacturing defects.
- Multi-port specific. Bitline shorts and wordline shorts. Shorts between bitlines of different ports and shorts between wordlines of different ports. Specify **ShadowRead On** in the memory library file to detect these faults. Note that some restrictions apply.
- Multi-port specific. Port-interference faults. This fault can be caused by high resistance ground connections to one of the N-channel source terminals.
- Multi-port specific. Inter-port bitline coupling. Coupling between bitlines of different ports and within the same column. Specify **ShadowWrite On** and **ShadowWriteOK On** in the memory library file to detect these faults. Note that some restrictions apply.
- Bitline access transistor leakage faults and wordline access transistor leakage faults.
- Neighborhood Pattern Sensitive Faults (NPSF). These faults are caused when the content of a cell is influenced by the content of other cells in their neighborhood.

Test Time

The time required for the memory BIST controller to test your design using the **SMarchCHKBcil** algorithm depends on various factors: the number of clock cycles per

operation, the number of bits per data slice, the number of row address locations and the number of column address locations. You can calculate the test time using the equations in [Table A-10](#).

Table A-10. Test Time Calculation for SMarchCHKBcil Algorithm Specification

Phase	Type	Time
1	Idle	4
2	Idle	$\% \text{ReadModifyWrite} * B + \% \text{ReadModifyWrite}$
3	Idle	$\% \text{ReadModifyWrite} * B + \% \text{ReadRead}$
4		4
5		$\% \text{ReadModifyWrite} * B * R * C$
5.5		$\% \text{ReadModifyWrite} * B * R * C + 2 * R + R$
	Wait	Determined by ParallelRetentionTime in the ETVerify configuration file.
6		$\% \text{ReadModifyWrite} * B * R * C$
6.5		$\% \text{ReadModifyWrite} * B * R * C + 2 * R + R$
	Wait	Determined by ParallelRetentionTime in the ETVerify configuration file.
7		$\% \text{ReadModifyWrite} * B * R * C + R$
8		4
9		$\% \text{ReadModifyWrite} * B + \% \text{ReadRead}$
10	Idle	$\% \text{WriteRead} * (R * C - 1)$
11		$\% \text{ReadModifyWrite} * B * R * C + (\% \text{ReadModifyWrite} * R * C)$
12		$\% \text{ReadModifyWrite} * B * R * C + (\% \text{ReadModifyWrite} * R * C)$
13		$\% \text{ReadModifyWrite} * B * R * C + (\% \text{ReadRead} * R * C)$
14		$\% \text{ReadModifyWrite} * B * R * C + (\% \text{ReadRead} * R * C)$
15		$\% \text{ReadModifyWrite} * B * R * C + (\% \text{ReadRead} * R * C) + (\% \text{ReadModifyWrite} * B * R * C)$
16		$\% \text{ReadModifyWrite} * B + \% \text{ReadRead}$
17		$\% \text{Write} * B * (R * C - 1)$
18		$\% \text{ReadModifyWrite} * B * R * C + (\% \text{ReadRead} * R * C) + (\% \text{ReadModifyWrite} * B * R * C)$
19		$\% \text{ReadModifyWrite} * B + \% \text{Write}$
20		$\% \text{Write} * (R * C - 1)$

Specification

To test SRAMs using the SMarchCHKBcil algorithm, specify **Algorithm** *SMarchCHKBcil* in the memory library file.

Related Information

[Notation Describing Memory BIST Algorithms](#) [Algorithm](#)

SMarchCHKBvcd Algorithm

This algorithm is an enhanced SMarchCHKBcil test algorithm to detect datapath shorts as well as enable the detection of voltage drop on cells in multi-port memories.

A few steps are added to the SMarchCHKBcil algorithm to make sure that the appropriate data combinations are applied to every cell. However, this algorithm only can be used with full parallel data access (serial interfacing is not supported).

The SMarchCHKBvcd algorithm is applicable to both **Programmable** and **Non-Programmable** controllers.

Non-Programmable Controller Usage

[Table A-11](#) shows the entire SMarchCHKBvcd algorithm for non-programmable controllers.

Table A-11. Description of SMarchCHKBvcd Test Algorithm per Test Port — Non-Programmable Controllers

Phase	Address Sequence	Sequence	Operations Used	Description
1		Idle	<i>None</i>	
2	1 to C Row 1	$((RxW1) (R1W1))^C$	<i>ReadModifyWrite</i>	Writes 1s to all words in the first row.

Table A-11. Description of SMarchCHKBvcd Test Algorithm per Test Port — Non-Programmable Controllers (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
3	1 to C Row 1	$((R1W0)(R1W_{m0}))^{B^*}$ $(R0W0)$ $((R0W_{m1})(R0W1))^{B^*}$ $(R1W1))^C$	<i>ReadModifyWrite</i>	This phase is used to detect bit/group write enable faults (stuck-at and shorts) and datapath shorts. Specific write enable masks (generated from the read data) are used to test for these faults. Test data is scanned from the <i>least</i> significant bit to the <i>most</i> significant bit of the datapath. The first portion of the phase reads 1 and <i>attempts</i> to write 0 to the datapath while all bit/group write enables are <i>Off</i> . This is followed by reading 1 and writing 0 to the datapath while the write enable mask is <i>On</i> before moving to the next bit. The last operation reads 0s and writes 0s to the word. The second portion of the phase reads 0 and <i>attempts</i> to write 1 to the datapath while the write enable mask is <i>On</i> . This is followed by reading 0 and writing 1 to the datapath while the write enable mask is <i>Off</i> before moving to the next bit. The last operation reads 1s and writes 1s to the word. The first portion of the phase detects all combinations of wired-AND shorts between write enables (bit and global). The second portion of the phase detects wired-OR shorts. Bit slice B^* is the full word length. W_{m0} or W_{m1} indicates a write operation performed using the write enable mask.

Table A-11. Description of SMarchCHKBvcd Test Algorithm per Test Port — Non-Programmable Controllers (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
3.5	1 to C Row 1	$((R1W0)(R1W_{m0}))^{B^*}$ $(R0W0)$ $((R0W_{m1})(R0W1))^{B^*}$ $(R1W1))^C$	<i>ReadModifyWrite</i>	<p>This phase is used to detect bit/group write enable faults (stuck-at and shorts) and datapath shorts. Specific write enable masks (generated from the read data) are used to test for these faults. Test data is scanned from the <i>most</i> significant bit to the <i>least</i> significant bit of the datapath. The first portion of the phase reads 1 and <i>attempts</i> to write 0 to the datapath while all bit/group write enables are <i>Off</i>. This is followed by reading 1 and writing 0 to the datapath while the write enable mask is <i>On</i> before moving to the next bit. The last operation reads 0s and writes 0s to the word. The second portion of the phase reads 0 and <i>attempts</i> to write 1 to the datapath while the write enable mask is <i>On</i>. This is followed by reading 0 and writing 1 to the datapath while the write enable mask is <i>Off</i> before moving to the next bit. The last operation reads 1s and writes 1s to the word.</p> <p>The first portion of the phase detects all combinations of wired-AND shorts between write enables (bit and global). The second portion of the phase detects wired-OR shorts. Bit slice B^* is the full word length. W_{m0} or W_{m1} indicates a write operation performed using the write enable mask.</p>

Table A-11. Description of SMarchCHKBvcd Test Algorithm per Test Port — Non-Programmable Controllers (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
3.6	(2,2) (1,2) (2,1)	((RxW0)(R0W0)) ((R1Rx)(R1Rx)) ((R0Rx)(R0Rx))	<i>ReadModifyWrite</i> <i>ReadRead</i> <i>ReadRead</i>	<p>This phase is used to detect Read Enable stuck-active faults.</p> <p>The first portion of the phase initializes Address 2 to all 0s. Note that address 1 is already initialized to all 1s.</p> <p>The second portion of the phase reads 1s from Address 1 while ReadEnable is <i>On</i>. This is followed by attempting to read 0s from Address 2 while ReadEnable is <i>Off</i>.</p> <p>The third portion of the phase reads 0s from Address 2 while <i>ReadEnable</i> is <i>On</i>. This is followed by attempting to read 1s from Address 1 while ReadEnable is <i>Off</i>.</p> <p>Note that ShadowRead is <i>Off</i> during this phase.</p>
3.7	(1) (1) (2) (2)	(R0W0) (R1Rx) (R1W1) (R0Rx)	<i>ReadModifyWrite</i> <i>ReadRead</i>	<p>This phase is used to detect Chip Select stuck-active faults.</p> <p>The first portion of the phase occurs at Address 1. The operation attempts to read 1s and write 0s while ChipSelect is <i>Off</i>. This is followed by reading 1s while ChipSelect is <i>On</i>.</p> <p>The second portion of the phase occurs at Address 2. The operation attempts to read 0s and write 1s while ChipSelect is <i>Off</i>. This is followed by reading 0s while ChipSelect is <i>On</i>.</p>
4		Idle	<i>None</i>	Performs Multi-Cycle Initialization.
5	1 to R Fast column	$(RxW0)^C$	<i>ReadModifyWrite</i>	Writes Checkerboard background data.

Table A-11. Description of SMarchCHKBvcd Test Algorithm per Test Port — Non-Programmable Controllers (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
5.1	1 to C Fast row	$((R0W1)(W0R0))^R$	<i>ReadModifyWrite</i> <i>WriteRead</i>	<p>Reads the checkerboard from the reference cell and writes inverse checkerboard data. This is followed by writing the checkerboard data restoring the original background that was started with and reading it back.</p> <p>During the Read portion of the operation a ColumnShadowWrite operation is performed on the adjacent column of inactive write port.</p> <p>During the Write portion of the operation, a ColumnShadowRead operation is performed on the adjacent column of inactive read port.</p> <p>This phase is only useful for multi-port memories.</p>
5.2	1 to C Fast row	$(R0W1)^R$	<i>ReadModifyWrite</i>	Reads the checkerboard background and replaces it with inverse checkerboard data.
5.3	1 to C Fast Row	$((W0R0) (R0W0))^R$	<i>WriteRead</i> <i>ReadModifyWrite</i>	<p>Writes checkerboard data to the reference cell and read it back. This is followed by reading the checkerboard data and writing it back before changing the address.</p> <p>The back-to-back Write operations occur at the end of the last Write operation on the current cell and the Write operation on the cell in the next row address.</p>

Table A-11. Description of SMarchCHKBvcd Test Algorithm per Test Port — Non-Programmable Controllers (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
5.5	1 to R Fast column	(R0W0) ^C (Rx*)	<i>ReadModifyWrite</i>	Reads the checkerboard background while ShadowWrite is <i>On</i> , and ShadowRead is <i>Off</i> (Read is performed at the address specified by the test algorithm from all inactive R/W ports). Writes checkerboard patterns with ShadowRead <i>On</i> and ShadowWrite <i>Off</i> .
	-	Optional Wait	<i>None</i>	Pauses the test to perform the static retention test.
6	1 to R Fast column	(R0Rx)	<i>ReadRead</i>	Reads checkerboard data at all locations.
6.1	1 to R Fast column	(R0W1) ^C	<i>ReadModifyWrite</i>	Reads checkerboard background while ShadowRead is <i>Off</i> . Replaces it with inverse checkerboard data while ShadowRead is <i>On</i> , and (ShadowWrite is <i>Off</i> in both cases).

Table A-11. Description of SMarchCHKBvcd Test Algorithm per Test Port — Non-Programmable Controllers (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
6.2	1 to C Fast row	$((R1W0) (W1R1))^R$	<i>ReadModifyWrite</i> <i>WriteRead</i>	<p>Reads the inverse checkerboard from the reference cell and writes checkerboard data. This is followed by writing the inverse checkerboard data restoring the original background that was started with and reading it back.</p> <p>During the read portion of the operation, a ColumnShadowWrite operation is performed on the adjacent column of the inactive write port.</p> <p>During the write portion of the operation, a ColumnShadowRead operation is performed on the adjacent column of the inactive read port.</p> <p>This phase is only useful for multi-port memories.</p>
6.3	1 to C Fast Row	$(R1W0)^R$	<i>ReadModifyWrite</i>	Reads the inverse checkerboard background and replaces it with checkerboard data.
6.4	1 to C Fast Row	$((W1R1) (R1W1))^R$	<i>WriteRead</i> <i>ReadModifyWrite</i>	<p>Writes inverse checkerboard data to the reference cell and reads it back. This is followed by reading the inverse checkerboard data and writing it back before changing the address.</p> <p>The back-to-back Write operations occur at the end of the last Write operation on the current cell and the write operation on the cell in the next row address.</p>

Table A-11. Description of SMarchCHKBvcd Test Algorithm per Test Port — Non-Programmable Controllers (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
6.5	1 to R Fast column	(R1W1) ^C (Rx*)	<i>ReadModifyWrite</i>	Reads Inverse Checkerboard Pattern while ShadowWrite is <i>On</i> and ShadowRead is <i>Off</i> (Read is performed at the address specified by the test algorithm from all inactive R/W ports), writes the same patterns with ShadowRead <i>On</i> and ShadowWrite is <i>Off</i> .
	-	Optional Wait	<i>None</i>	Pauses the test to perform the static retention test.
7	1 to R Fast column	(R1Rx)	<i>ReadRead</i>	Reads Inverse Checkerboard data at all locations.
7.1	1 to R Fast column	(R1W0) ^C (Rx*)	<i>ReadModifyWrite</i>	Reads Inverse Checkerboard data while ShadowRead is <i>Off</i> . Replaces it with checkerboard data while ShadowRead is <i>On</i> .
8	-	Idle	<i>None</i>	Perform Multi-cycle initialization.
9	1	(RxW0) (R0Rx)	<i>ReadModifyWrite</i> <i>ReadRead</i>	Writes 0s to the first word, and reads it back.
10	2 to W Fast row	(W0R0)	<i>WriteRead</i>	Writes 0s to all words.
11	1 to W Fast row	(R0W1) (R1W1)	<i>ReadModifyWrite</i>	Reads all 0s, and replaces them with 1s.
12	1 to W Fast row	(R1W0) (R0W0)	<i>ReadModifyWrite</i>	Reads 1s, and replaces them with 0s.
13	W to 1 Fast row	(R0W1) (R1W1)	<i>ReadModifyWrite</i> <i>ReadModifyWrite</i>	Reads 0s, and replaces them with 1s. Reads 1s, and writes them back before decrementing the address.
14	W to 1 Fast row	(R1W0) (R0W0)	<i>ReadModifyWrite</i> <i>ReadModifyWrite</i>	Reads 1s and replaces them with 0s. Reads 0s, and writes them back before decrementing the address.

Table A-11. Description of SMarchCHKBvcd Test Algorithm per Test Port — Non-Programmable Controllers (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
15	1 to W Fast row	(R0W1) (R0W0) (R1W0)	<i>ReadModifyWrite</i> <i>ReadModifyWrite</i> <i>ReadModifyWrite</i>	This phase is composed of three operations. For all operations, the column address is constant. The first is a Read 0 followed by a Write 1. The second set of operations is to Read 0 from a different row (on the same column), and write it back. The third set of operations is to Read a 1 from the current row and restoring its value to 0.
16	1 Fast row	(RxW1) (R1Rx)	<i>ReadModifyWrite</i> <i>ReadRead</i>	Writes 1 through the first word. A back-to-back Read is performed before changing address.
17	2 to W Fast row	(W1R1)	<i>WriteRead</i>	Write 1 to all locations.
18	1 to W Fast row	(R1W0) (R1W1) (R0W1)	<i>ReadModifyWrite</i> <i>ReadModifyWrite</i> <i>ReadModifyWrite</i>	This phase is composed of three operations. For all operations, the column address is constant. The first set of operations is a Read 1 followed by a Write 0. The second set of operations is to Read 1 from a different row and write it back. The third set of operations is to Read a 0 from the current row and restoring its value to 1.
19	1	(RxWmemcontents) (WmemcontentsRx)	<i>ReadModifyWrite</i> <i>Write</i>	Writes the memory content into the first word (default 0), and writes it back before changing address.
20	2 to W	WmemcontentsRx	<i>WriteRead</i>	Writes memory contents to the rest of the memory (default 0).

Detected Faults

The SMarchCHKBvcd algorithm detects the following failure modes:

- Stuck-at cell faults. A stuck-at fault is a single memory cell stuck at either a logic 1 or a logic 0.
- Transition faults. A transition fault is a single memory cell that fails to transition from a logic 0 to a logic 1, (or from a logic 1 to a logic 0), when written with a logic 1 (logic 0). Transition faults also include stuck-open access transistors.
- Unlinked dynamic coupling faults. One example of an unlinked coupling fault is a transition in one memory cell that causes a transition in a second memory cell.
- Address decoder faults. These faults result in any of the following: any given address does not access any cells; any given address simultaneously accesses multiple cells; and multiple addresses access a single cell.
- Read/Write logic faults. A Read/Write logic fault is a stuck-at fault in the Read/Write control logic.
- Parametric faults. Parametric faults include faults relating to access and cycle time, write recovery time, and some leakage faults that lead to data retention problems.
- Destructive Read faults. Destructive Read faults cause the contents of a memory cell to be changed during a read access.
- Write recovery faults. This algorithm additionally performs this test twice for each reference cell, whenever it is possible, once using a row address that is higher than the reference address, and once using the row address that is lower than the reference address.
- Leakage faults leading to insufficient data retention.
- Single-port bitline coupling. Coupling between bitlines of adjacent columns that causes read errors when accessing cells with minor manufacturing defects.
- Multi-port specific. Bitline shorts and wordline shorts. Shorts between bitlines of different ports and shorts between wordlines of different ports. Specify *ShadowRead On* in the memory library file to detect these faults.
- This type of fault can occur outside the write circuitry and sense amplifiers. In all other Mentor Graphics algorithms, datapath short detection requires a bit slice of 2 or more for

odd bit groupings. Additionally, the *SMarchCHKBvcd* algorithm is able to use a bit slice of 1 (for parallel test) as well.

- Multi-port specific. Port-interference faults. This fault can be caused by high resistance ground connections to one of the N-channel source terminals.
- Multi-port specific. Inter-port bitline coupling. Coupling between bitlines of different ports and within the same column. Specify *ShadowWrite On* and *ShadowWriteOK On* in the memory library file to detect these faults. Note that some restrictions apply.
- Bitline access transistor leakage faults and wordline access transistor leakage faults.
- Neighborhood Pattern Sensitive Faults (NPSF). These faults are caused when the content of a cell is influenced by the content of other cells in their neighborhood.
- Datapath Shorts in memories with odd number of bit-grouping when full parallel test is used.
- Cell Voltage Drop Faults. These faults are mainly caused by charge sharing.
- Bit/Group/Global write enable faults. Stuck-active and short between the bit/byte write enable ports and the global write enable ports are tested.
- Read enable stuck-active faults.
- Chip select stuck-active faults.

Test Time

The time required for the memory BIST controller to test your design using the *SMarchCHKBvcd* algorithm depends on various factors: the number of clock cycles per operation, the number of bits per data slice, the number of row address locations and the number of column address locations. You can calculate the test time using the equations in [Table A-12](#).

Table A-12. Test Time Calculation for SMarchCHKBvcd Algorithm Specification — Non-Programmable Controllers

Phase	Type	Time
1	Idle	4
2	Idle	(%ReadModifyWrite * 2 * C)
3		(%ReadModifyWrite * d * 4 * C) + (%ReadModifyWrite * 2 * C)
3.5		(%ReadModifyWrite * d * 4 * C) + (%ReadModifyWrite * 2 * C)
3.6		(%ReadModifyWrite * 2) + (%ReadRead * 4)
3.7		(%ReadModifyWrite * 2) + (%ReadRead * 2)
4		4
5		(%WriteRead) + %ReadModifyWrite * R * C
5.1		(%ReadModifyWrite*R*C) + (%WriteRead*R*C)

Table A-12. Test Time Calculation for SMarchCHKBvcd Algorithm Specification — Non-Programmable Controllers (cont.)

Phase	Type	Time
5.2		$\% \text{ReadModifyWrite} * R * C$
5.3		$(\% \text{WriteRead} * R * C) + (\% \text{ReadModifyWrite} * R * C)$
5.5		$\% \text{ReadModifyWrite} * R * C + (2 * R)$
	wait	Determined by ParallelRetentionTime in the ETVerify configuration file.
6		$\% \text{ReadRead} * R * C$
6.1		$\% \text{ReadModifyWrite} * R * C$
6.2		$(\% \text{ReadModifyWrite} * R * C) + (\% \text{WriteRead} * R * C)$
6.3		$\% \text{ReadModifyWrite} * R * C$
6.4		$(\% \text{WriteRead} * R * C) + (\% \text{ReadModifyWrite} * R * C)$
6.5		$(\% \text{ReadModifyWrite} * R * C) + (2 * R)$
	wait	Determined by ParallelRetentionTime in the ETVerify configuration file.
7		$\% \text{ReadRead} * R * C$
7.1		$(\% \text{ReadModifyWrite} * R * C) + R$
8		4
9	Idle	$\% \text{ReadModifyWrite} + \% \text{ReadRead}$
10	Idle	$\% \text{WriteRead} * (R * C - 1)$
11		$(\% \text{ReadModifyWrite} * R * C) + (\% \text{ReadModifyWrite} * R * C)$
12		$(\% \text{ReadModifyWrite} * R * C) + (\% \text{ReadModifyWrite} * R * C)$
13		$(\% \text{ReadModifyWrite} * R * C) + (\% \text{ReadModifyWrite} * R * C)$
14		$(\% \text{ReadModifyWrite} * R * C) + (\% \text{ReadModifyWrite} * R * C)$
15		$(\% \text{ReadModifyWrite} * R * C) + (\% \text{ReadModifyWrite} * R * C) + (\% \text{ReadModifyWrite} * R * C)$
16		$\% \text{ReadModifyWrite} + \% \text{ReadRead}$
17		$\% \text{Write} * (R * C - 1)$
18		$(\% \text{ReadModifyWrite} * R * C) + (\% \text{ReadModifyWrite} * R * C) + (\% \text{ReadModifyWrite} * R * C)$
19		$\% \text{ReadModifyWrite} + \% \text{Write}$
20		$\% \text{Write} * (R * C - 1)$

Specification

To test SRAMs using the SMarchCHKBvcd algorithm, specify [Algorithm SMarchCHKBvcd](#) in the memory library file.

Usage Conditions

The [*OperationSet*](#) property of the memory library file must be the Mentor Graphics built-in *SyncWR* or a compatible *OperationSet*.

This algorithm is only applicable when full parallel testing is used (bit-slice = 1). An error message will be issued if this rule is not satisfied. Note that the bit-slice value cannot be greater than 1.

The SMarchCHKBvcd algorithm performs specialized tests on the chip select and read enable ports. To use this algorithm, the memory data output value must be preserved when the chip select or read enable port is deasserted.

Programmable Controller Usage

The implementation is enhanced to remove operations that require reading the memory and writing the memory in the next cycle. These operations have caused timing closure issues. The algorithm makes the assumption that data inputs are physically laid out so that even-index inputs are interleaved with odd-index inputs when testing for shorts between bits of the internal memory data bus. The algorithm makes the same assumption for group write enable inputs.

Each phase of the algorithm is described for the case of a single bank. If more than one bank exists, the phase repeats for each bank. The address counter in a phase determines whether the banks are addressed in ascending or descending order.

The algorithm requires a special operation set. Additional operations perform the specialized test sequences. [Table A-13](#) lists the operations that the algorithm requires. The library operation set *SyncWRvcd* is compatible with this algorithm. If you create a custom operation set, you must define all necessary operations.

Table A-13 shows the entire SMarchCHKBvcd algorithm for programmable controllers. The codes in the *Operations Used* and *Description* columns map to [Table A-14](#), which gives the corresponding operation names that are defined in the *SyncWRvcd* operation set.

Table A-13. Description of SMarchCHKBvcd Test Algorithm per Test Port — Programmable Controllers

Phase	Address Sequence	Sequence	Operations Used	Description
1		Idle	OP0	

**Table A-13. Description of SMarchCHKBvcd Test Algorithm per Test Port —
Programmable Controllers (cont.)**

Phase	Address Sequence	Sequence	Operations Used	Description
2	1 to C, Row 1 1 to C, Row 1	$(W0R0Rx)^C$ $(W1R1Rx)^C$	OP5	<p>This phase is used to detect datapath shorts.</p> <p>The same pattern is written to all words with no data mapping applied.</p> <p>Step 1 — (OP5) Write checkerboard to the datapath and read it back for all words in the first row.</p> <p>Step 2 — (OP5) Write inverse checkerboard to the datapath and read it back for all words in the first row.</p>

**Table A-13. Description of SMarchCHKBvcd Test Algorithm per Test Port —
Programmable Controllers (cont.)**

Phase	Address Sequence	Sequence	Operations Used	Description
3	1 to C, Row 1 1 to C, Row 1 1 to C, Row 1 1 to C, Row 1	$((W0R0Rx)(W1R1Rx))^C$ $((W0R0Rx)(W1R1Rx))^C$ $((W0R0Rx)(W1R1 Rx))^C$ $((W1R1Rx)(W0R1Rx))^C$	OP5 OP6 OP7 OP8	<p>This phase is used to detect bit/group write enable faults.</p> <p>Repeat all groups of operations for all words in the first row.</p> <p>Step 1 — (OP5) Write and read 0s for the word. Step 2 * (OP6) Write 1s while Even Group Write Enables are <i>On</i> followed by reading data pattern 0101 ... 0101. Step 3 — (OP5) Write and read 0s for the word. Step 4 * (OP7) Write 1s while Odd Group Write Enables are <i>On</i> followed by reading data pattern 1010 ... 1010. Step 5 — (OP5) Write and read 0s for the word. Step 6 — (OP5) Write 1s while all Group Write Enables are <i>On</i> followed by reading 1s. Step 7 — (OP5) Write and read 1s for the word. Step 8 * (OP8) Attempt to write 0s while all Group Write Enables are <i>Off</i> followed by reading 1s.</p> <p>Note: Steps marked with * indicate that memories without the feature under test are disabled to avoid corruption of their content.</p>

**Table A-13. Description of SMarchCHKBvcd Test Algorithm per Test Port —
Programmable Controllers (cont.)**

Phase	Address Sequence	Sequence	Operations Used	Description
3.6	1 to C, Row 1 1 to C, Row 2 1 to C, Row 1 1 to C, Row 2 1 to C, Row 2 1 to C, Row 1	$(W1Rx)^C$ $(W0Rx)^C$ $(R1Rx)^C$ $(R1Rx)^C$ $(R0Rx)^C$ $(R0Rx)^C$	OP1 OP2 OP9	<p>This phase is used to detect Read Enable stuck-active faults.</p> <p>Step 1 — (OP1) Write <i>1s</i> to all words in the first row. Step 2 — (OP1) Write <i>0s</i> to all words in the second row. Step 3 — (OP2) Read <i>1s</i> from all words in the first row. Step 4 * (OP9) Attempt to read <i>0s</i> from all words in the second row while Read Enable is <i>Off</i>. Step 5 — (OP2) Read <i>0s</i> from all words in the second row. Step 6 * (OP9) Attempt to read <i>1s</i> from all words in the first row while Read Enable is <i>Off</i>.</p> <p>Note: Steps marked with * indicate that memories without the feature under test are disabled to avoid corruption of their content.</p>

**Table A-13. Description of SMarchCHKBvcd Test Algorithm per Test Port —
Programmable Controllers (cont.)**

Phase	Address Sequence	Sequence	Operations Used	Description
3.7	1 to C, Row 1 1 to C, Row 2 1 to C, Row 1 1 to C, Row 1 1 to C, Row 2 1 to C, Row 2	$(R1Rx)^C$ $(R0Rx)^C$ $(R0W0)^C$ $(R1Rx)^C$ $(R1W1)^C$ $(R0Rx)^C$	OP2 OP4	<p>This phase is used to detect Chip Select stuck-active faults.</p> <p>Step 1 — (OP2) Read <i>1s</i> from all words in the first row.</p> <p>Step 2 — (OP2) Read <i>0s</i> from all words in the second row.</p> <p>Step 3 * (OP4) Attempt to read <i>1s</i> and write <i>0s</i> for all words in the first row while Chip Select is <i>Off</i>.</p> <p>Step 4 — (OP2) Read <i>1s</i> from all words in the first row.</p> <p>Step 5 * (OP4) Attempt to read <i>0s</i> and write <i>1s</i> for all words in the second row while Chip Select is <i>Off</i>.</p> <p>Step 6 — (OP2) Read <i>0s</i> from all words in the second row.</p> <p>Note: Steps marked with * indicate that memories without the feature under test are disabled to avoid corruption of their content.</p>
4		Idle	OP0	
5	1 to R Fast column	$(RxW0)^C$	OP3	Write checkerboard background data.

**Table A-13. Description of SMarchCHKBvcd Test Algorithm per Test Port —
Programmable Controllers (cont.)**

Phase	Address Sequence	Sequence	Operations Used	Description
5.1	1 to C Fast row	$((R0W1)(W0Rx))^R$	OP3 OP1	<p>This phase is only useful for multi-port memories.</p> <p>Step 1 — (OP3) Read checkerboard and write inverse checkerboard data.</p> <p>Step 2 — (OP1) Write checkerboard data restoring the original background and reading it back.</p> <p>During the Read portion of the operation, a ColumnShadowWrite operation is performed on the adjacent column of inactive write port.</p> <p>During the Write portion of the operation, a ColumnShadowRead operation is performed on the adjacent column of inactive read port.</p>
5.2	1 to C Fast row	$(R0W1)^R$	OP3	Read checkerboard background and replace it with inverse checkerboard data.
5.3	1 to C Fast row	$((W0Rx) (R0W0))^R$	OP1 OP3	<p>Step 1 — (OP1) Write checkerboard data and read it back.</p> <p>Step 2 — (OP3) Read checkerboard data and write it back before changing the address.</p> <p>The back-to-back Write operations occur at the end of the last Write operation on the current cell and the Write operation on the cell in the next row address.</p>

**Table A-13. Description of SMarchCHKBvcd Test Algorithm per Test Port —
Programmable Controllers (cont.)**

Phase	Address Sequence	Sequence	Operations Used	Description
5.5	1 to R Fast column	$(R0W0)^C$	OP3	Read checkerboard background while ShadowWrite is <i>On</i> , and ShadowRead is <i>Off</i> (Read is performed at the address specified by the test algorithm from all inactive R/W ports). Write checkerboard with ShadowRead <i>On</i> and ShadowWrite <i>Off</i> .
		Optional Wait	None	Pause the test to perform the static retention test.
6	1 to R Fast column	$(R0Rx)^C$	OP2	Read checkerboard background data followed by a read operation whose data out will not be compared.
6.1	1 to R Fast column	$(R0W1)^C$	OP3	Read checkerboard background while ShadowRead is <i>Off</i> . Replace it with inverse checkerboard data while ShadowRead is <i>On</i> . ShadowWrite is <i>Off</i> in both cases.

**Table A-13. Description of SMarchCHKBvcd Test Algorithm per Test Port —
Programmable Controllers (cont.)**

Phase	Address Sequence	Sequence	Operations Used	Description
6.2	1 to C Fast row	$((R1W0)(W1Rx))^R$	OP3 OP1	<p>This phase is only useful for multi-port memories.</p> <p>Step 1 — (OP3) Read inverse checkerboard and write checkerboard data.</p> <p>Step 2 — (OP1) Write inverse checkerboard data restoring the original background and reading it back.</p> <p>During the Read portion of the operation, a ColumnShadowWrite operation is performed on the adjacent column of inactive write port.</p> <p>During the Write portion of the operation, a ColumnShadowRead operation is performed on the adjacent column of inactive read port.</p>
6.3	1 to C Fast row	$(R1W0)^R$	OP3	Read inverse checkerboard background and replace it with checkerboard data.
6.4	1 to C Fast row	$((W1Rx) (R1W1))^R$	OP1 OP3	<p>Step 1 — (OP1) Write inverse checkerboard data and read it back.</p> <p>Step 2 — (OP3) Read inverse checkerboard data and write it back before changing the address.</p> <p>The back-to-back Write operations occur at the end of the last Write operation on the current cell and the Write operation on the cell in the next row address.</p>

Table A-13. Description of SMarchCHKBvcd Test Algorithm per Test Port — Programmable Controllers (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
6.5	1 to R Fast column	(R1W1) ^C	OP3	Read inverse checkerboard background while ShadowWrite is <i>On</i> , and ShadowRead is <i>Off</i> (Read is performed at the address specified by the test algorithm from all inactive R/W ports). Write inverse checkerboard with ShadowRead <i>On</i> and ShadowWrite <i>Off</i> .
		Optional Wait	None	Pause the test to perform the static retention test.
7	1 to R Fast column	(R1Rx) ^C	OP2	Read inverse checkerboard background data followed by a read operation whose data out will not be compared.
7.1	1 to R Fast column	(R1W0) ^C	OP3	Read inverse checkerboard data while ShadowRead is <i>Off</i> . Replace it with checkerboard data while ShadowRead is <i>On</i> .
8		Idle	OP0	Perform multi-cycle initialization.
10	1 to W Fast row	(W0Rx) ^R	OP1	Write 0s to all words.
11	1 to W Fast row	((R0W1)(R1W1)) ^R	OP3	Step 1 — (OP3) Read 0 followed by write 1. Step 2 — (OP3) Read 1 and write it back.
12	1 to W Fast row	((R1W0)(R0W0)) ^R	OP3	Step 1 — (OP3) Read 1 followed by write 0. Step 2 — (OP3) Read 0 and write it back.
13	W to 1 Fast row	((R0W1)(R1W1)) ^R	OP3	Step 1 — (OP3) Read 0 followed by write 1. Step 2 — (OP3) Read 1 and write it back before decrementing the address.

Table A-13. Description of SMarchCHKBvcd Test Algorithm per Test Port — Programmable Controllers (cont.)

Phase	Address Sequence	Sequence	Operations Used	Description
14	W to 1 Fast row	$((R1W0)(R0W0))^R$	OP3	Step 1 — (OP3) Read 1 followed by write 0. Step 2 — (OP3) Read 0 and write it back before decrementing the address.
15	1 to W Fast row	$((R0W1)(R0W0) (R1W0))^R$	OP3	Step 1 — (OP3) Read 0 followed by write 1. Step 2 — (OP3) Read 0 from adjacent row on the same column and write it back. Step 3 — (OP3) Read 1 from the current row and restore its value to 0.
17	1 to W Fast row	$(W1Rx)^R$	OP1	Write 1s to all words.
18	1 to W Fast row	$((R1W0)(R1W1) (R0W1))^R$	OP3	Step 1 — (OP3) Read 1 followed by write 0. Step 2 — (OP3) Read 1 from adjacent row on the same column and write it back. Step 3 — (OP3) Read 0 from the current row and restore its value to 1.
20	1 to W Fast row	$(WmemcontentsRx)^R$	OP1	Write the memory content to all words (default 0).

Table A-14 shows the mapping of operation names to the codes used in the *Operation Used* and *Description* columns of Table A-13.

Table A-14. Mapping of Operation Code to Operation Name

Code	Operation Name
OP0	NoOperation
OP1	Write
OP2	Read
OP3	ReadModifyWrite
OP4	ReadModifyWrite_WithSelectOff

Table A-14. Mapping of Operation Code to Operation Name (cont.)

Code	Operation Name
OP5	WriteReadCompare
OP6	WriteReadCompare_EvenGWE_On
OP7	WriteReadCompare_OddGWE_On
OP8	WriteReadCompare_AllGWE_Off
OP9	ReadWithReadEnableOff
OP10	ReadModifyWrite_Column_ShadowWriteRead
OP11	ReadModifyWrite_Row_ShadowWriteRead
OP12	WriteRead_Column_ShadowReadWrite

Detected Faults

The SMarchCHKBvcd algorithm detects the following failure modes:

- Stuck-at cell faults. A stuck-at fault is a single memory cell stuck at either a logic 1 or a logic 0.
- Transition faults. A transition fault is a single memory cell that fails to transition from a logic 0 to a logic 1, (or from a logic 1 to a logic 0), when written with a logic 1 (logic 0). Transition faults also include stuck-open access transistors.
- Unlinked dynamic coupling faults. One example of an unlinked coupling fault is a transition in one memory cell that causes a transition in a second memory cell.
- Address decoder faults. These faults result in any of the following: any given address does not access any cells; any given address simultaneously accesses multiple cells; and multiple addresses access a single cell.
- Read/Write logic faults. A Read/Write logic fault is a stuck-at fault in the Read/Write control logic.
- Parametric faults. Parametric faults include faults relating to access and cycle time, write recovery time, and some leakage faults that lead to data retention problems.
- Destructive Read faults. Destructive Read faults cause the contents of a memory cell to be changed during a read access.
- Write recovery faults. This algorithm additionally performs this test twice for each reference cell, whenever it is possible, once using a row address that is higher than the reference address, and once using the row address that is lower than the reference address.
- Leakage faults leading to insufficient data retention.
- Single-port bitline coupling. Coupling between bitlines of adjacent columns that causes read errors when accessing cells with minor manufacturing defects.
- Multi-port specific. Bitline shorts and wordline shorts. Shorts between bitlines of different ports and shorts between wordlines of different ports. Specify **ShadowRead On** in the memory library file to detect these faults.

- This type of fault can occur outside the write circuitry and sense amplifiers. In all other Mentor Graphics algorithms, datapath short detection requires a bit slice of 2 or more for odd bit groupings. Additionally, the SMarchCHKBvcd algorithm is able to use a bit slice of 1 (for parallel test) as well.
- Multi-port specific. Port-interference faults. This fault can be caused by high resistance ground connections to one of the N-channel source terminals.
- Multi-port specific. Inter-port bitline coupling. Coupling between bitlines of different ports and within the same column. Specify **ShadowWrite On** and **ShadowWriteOK On** in the memory library file to detect these faults. Note that some restrictions apply.
- Bitline access transistor leakage faults and wordline access transistor leakage faults.
- Neighborhood Pattern Sensitive Faults (NPSF). These faults are caused when the content of a cell is influenced by the content of other cells in their neighborhood.
- Datapath Shorts in memories with odd number of bit-grouping when full parallel test is used.
- Cell Voltage Drop Faults. These faults are mainly caused by charge sharing.
- Bit/Group/Global write enable faults. Stuck-active and short between the bit/byte write enable ports and the global write enable ports are tested.
- Read enable stuck-active faults.
- Chip select stuck-active faults.

Test Time

The time required for the memory BIST controller to test your design using the SMarchCHKBvcd algorithm depends on various factors: the number of clock cycles per operation, the number of bits per data slice, the number of row address locations, and the number of column address locations. You can calculate the test time using the equations in Table A-15.

Table A-15. Test Time Calculation for SMarchCHKBvcd Algorithm Specification — Programmable Controllers

Phase	Type	Time
1	Idle	%NoOperation
2		%WriteReadCompare*2*C*Banks + %NoOperation*Banks
3		(%WriteReadCompare+%WriteReadCompare_EvenGWE_On)*C*Banks + (%WriteReadCompare+%WriteReadCompare_OddGWE_On)*C*Banks + %WriteReadCompare*2*C*Banks + (%WriteReadCompare+%WriteReadCompare_AllGWE_Off)*C*Banks + %NoOperation*Banks
3.6		%Write*2*C*Banks + (%Read+%ReadWithReadEnableOff)*2*C*Banks + %NoOperation*Banks

Table A-15. Test Time Calculation for SMarchCHKBvcd Algorithm Specification — Programmable Controllers (cont.)

Phase	Type	Time
3.7		%Read*2*C*Banks + (%ReadModifyWrite_WithSelectOff+%Read)*2*C*Banks + %NoOperation*Banks
4		%NoOperation
5		%ReadModifyWrite*R*C*Banks + %NoOperation*Banks
5.1		%ReadModifyWrite*R*C*Banks + %Write*R*C*Banks
5.2		%ReadModifyWrite*R*C*Banks
5.3		%Write*R*C*Banks + %ReadModifyWrite*R*C*Banks
5.5		%ReadModifyWrite*R*C*Banks + %NoOperation*Banks
	Wait	Determined by ParallelRetentionTime in the ETVerify configuration file.
6		%Read*R*C*Banks + %NoOperation*Banks
6.1		%ReadModifyWrite*R*C*Banks + %NoOperation*Banks
6.2		%ReadModifyWrite*R*C*Banks + %Write*R*C*Banks
6.3		%ReadModifyWrite*R*C*Banks
6.4		%Write*R*C*Banks + %ReadModifyWrite*R*C*Banks
6.5		%ReadModifyWrite*R*C*Banks + %NoOperation*Banks
	Wait	Determined by ParallelRetentionTime in the ETVerify configuration file.
7		%Read*R*C*Banks + %NoOperation*Banks
7.1		%ReadModifyWrite*R*C*Banks + %NoOperation*Banks
8		%NoOperation
10		%Write*R*C*Banks
11		%ReadModifyWrite*R*C*Banks*2
12		%ReadModifyWrite*R*C*Banks*2
13		%ReadModifyWrite*R*C*Banks*2
14		%ReadModifyWrite*R*C*Banks*2

Table A-15. Test Time Calculation for SMarchCHKBvcd Algorithm Specification — Programmable Controllers (cont.)

Phase	Type	Time
15		%ReadModifyWrite*R*C*Banks*3 + %NoOperation*Banks
17		%Write*R*C*Banks
18		%ReadModifyWrite*R*C*Banks*3 + %NoOperation*Banks
20		%Write*R*C*Banks

Specification

To test SRAMs using the SMarchCHKBvcd algorithm, specify **Algorithm** SMarchCHKBvcd in the memory library file.

Usage Conditions

The **OperationSet** property of the memory library file must be the Mentor Graphics built-in *SyncWRvcd*.

This algorithm is only applicable when full parallel testing is used (**BitSliceWidth=1**). An error message will be issued if this rule is not satisfied.

The SMarchCHKBvcd algorithm performs specialized tests on the chip select and read enable ports, if they are present. To use this algorithm, the memory data output value must be preserved when the chip select or read enable port is deasserted. If the memory data output value is not preserved in these cases, in the **MemoryTemplate** wrapper of the memory library file, set the **MemoryHoldWithInactiveSelect** or **DataOutHoldWithInactiveReadEnable** properties to *Off*, as appropriate for your memory.

Related Information

[Notation Describing Memory BIST Algorithms](#)

[Algorithm](#)

LVMarchX Algorithm

The LVMarchX algorithm is only applicable to **Programmable** controllers.

The LVMarchX algorithm is a test algorithm that is available for loading into the memory controller to perform a March X algorithm. The March X algorithm is performed as follows:

1. Write background of D-data incrementing from address minimum to address maximum.
2. Read D-data and write \bar{D} -data incrementing from address minimum to address maximum.
3. Read \bar{D} -data and write D-data decrementing from address maximum to address minimum.
4. Read D-data decrementing from address maximum to address minimum.

Test Length

$6 N_{xyz}$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$Z \Leftarrow Y1 \Leftarrow X1$

where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed and a carry out from the X1 address segment is generated. An X1CarryOut is generated when:
 - The X1 address segment is incrementing and has reached the maximum OR.
 - The X1 address segment is decrementing and has reached the minimum.
- The bank address segment Z counts when instructed and a carry out from the Y1 address segment is generated. An Y1CarryOut is generated when:
 - The Y1 address segment is incrementing and has reached the maximum AND a X1CarryOut is generated OR.
 - The Y1 address segment is decrementing and has reached the minimum AND a X1CarryOut is generated.

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

Algorithm Sequence

[Table A-16](#) describes the LVMarchX algorithm sequence.

Table A-16. Description of LVMarchX Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast row	W _D	Write	Write background of D-data.
1	1	-	-	min to max, fast row	R _D W _{D̄}	ReadModify Write	Read D-data and Write data D̄-data. After all addresses have been accessed branch to instruction 1 and repeat one time as follows with RepeatLoop(A): Repeat #1 - repeat instructions with inverted the address sequencing, write data sequencing, and expect data sequencing
2	1	Repeat #1	-	max to min, fast row	R _{D̄} W _D	ReadModify Write	Read D̄-data and Write D-data.
3	2	-	-	max to min, fast row	R _D	Read	Read D-data.

Example Algorithm Wrapper

[Figure A-1](#) illustrates the **Algorithm** wrapper for the example memory.

Figure A-1. LVMarchX Example Algorithm Wrapper

```

Algorithm (LVMarchX){
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b000000;
                NumberY0Bits : 0;
                NumberX0Bits : 0;
            }
        }
    }
}

```

```

        ZCarryIn : Y1CarryOut;
        Y1CarryIn : X1CarryOut;
        X1CarryIn : none;
    }
}
DataGenerator {
    LoadWriteData : 8'b00000000;
    LoadExpectData : 8'b00000000;
}
}
MicroProgram {
    Instruction (M0_W0) {
        OperationSelect : Write;
        AddressSelectCmd : Select_A;
        ZAddressCmd : Increment;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        WriteDataCmd : DataReg;
        NextConditions {
            Z_EndCount : On;
            X1_EndCount : On;
            Y1_EndCount : On;
        }
    }
    Instruction (M1_R0_W1) {
        OperationSelect : ReadModifyWrite;
        AddressSelectCmd : Select_A;
        ZAddressCmd : Increment;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        ExpectDataCmd : DataReg;
        WriteDataCmd : InverseDataReg;
        InhibitLastAddressCount : On;
        NextConditions {
            Z_EndCount : On;
            X1_EndCount : On;
            Y1_EndCount : On;
            RepeatLoop (A) {
                BranchToInstruction : M1_R0_W1;
                Repeat {
                    WriteDataSequence : Inverse;
                    ExpectDataSequence : Inverse;
                    AddressSequence : Inverse;
                }
            }
        }
    }
    Instruction (M3_R0) {
        OperationSelect : Read;
        AddressSelectCmd : Select_A;
        ZAddressCmd : Decrement;
        X1AddressCmd : Decrement;
        Y1AddressCmd : Decrement;
        ExpectDataCmd : DataReg;
        InhibitLastAddressCount : On;
        NextConditions {
            Z_EndCount : On;
            X1_EndCount : On;
        }
    }
}

```

```

        Y1_EndCount : On;
    }
}
}
```

Fault Coverage

Table A-17 identifies the faults detected by the LVMarchX algorithm.

Table A-17. LVMarchX Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes
Transition Faults	Yes
Address Decoder Faults	Yes
Data Retention Faults	No
Inversion Coupling Faults	Yes
Idempotent Coupling Faults	No
Dynamic Coupling Faults	No
Transition Faults linked to Inversion Coupling Faults	No
Linked Idempotent Coupling Faults	No
Linked Dynamic Coupling Faults	No
Parametric Faults	Yes
Write Recovery Faults	Yes
Read Disturb Faults	Yes
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

Specification

The following specifications apply to the LVMarchX algorithm:

- To use the LVMarchX algorithm for the default algorithm, specify LVMarchX for the *HardCodedAlgorithm* property of the ETVerify configuration file.
 - To download the *LVMarchX* algorithm to the controller, specify LVMarchX for the *SelectLibraryAlgorithm* property in the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVMarchX algorithm:

- Operations named Write, ReadModifyWrite, and Read must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The *MemBistControllerOptions: NumberOfInstructions* property of the *.etplan* file must be greater than or equal to three.

Related Information

Notation Describing Memory BIST Algorithms	Algorithm
<i>HardCodedAlgorithm</i> in the <i>ETVerify Tool Reference</i>	<i>NumberOfInstructions</i>
<i>SelectLibraryAlgorithm</i> in the <i>ETVerify Tool Reference</i>	

LVMarchY Algorithm

The LVMarchY algorithm is only applicable to **Programmable** controllers.

The LVMarchY algorithm is a test algorithm that is available for loading into the memory controller to perform a March Y algorithm. The March Y algorithm is performed as follows:

1. Write background of D-data incrementing from address minimum to address maximum.
2. Read D-data, write \bar{D} -data, and read \bar{D} -data incrementing from address minimum to address maximum.
3. Read \bar{D} -data, write D-data, and read D-data decrementing from address maximum to address minimum.
4. Read D-data decrementing from address maximum to address minimum.

Test Length

$8N_{xyz}$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$Z \Leftarrow Y1 \Leftarrow X1$

where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed and a carry out from the X1 address segment is generated. An X1CarryOut is generated when:
 - The X1 address segment is incrementing and has reached the maximum OR
 - The X1 address segment is decrementing and has reached the minimum
- The bank address segment Z counts when instructed and a carry out from the Y1 address segment is generated. An Y1CarryOut is generated when:
 - The Y1 address segment is incrementing and has reached the maximum AND a X1CarryOut is generated OR.
 - The Y1 address segment is decrementing and has reached the minimum AND a X1CarryOut is generated.

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

Algorithm Sequence

[Table A-18](#) describes the **LVMarchY** algorithm sequence.

Table A-18. Description of LVMarchY Algorithm

Phase	Inst #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast row	W _D	Write	Write background of D-data.
1	1	-	-	-	R _D W _{D̄}	ReadModify Write	Read D-data and Write data D̄-data.
	2	-	-	min to max, fast row	R _{D̄}	Read	Read D̄-data. Branch back to Instruction 1 until all addresses are accessed. After all addresses have been accessed branch to instruction 1 and repeat one time as follows with RepeatLoop(A): Repeat #1 - repeat instructions with inverted the address sequencing, write data sequencing, and expect data sequencing
2	1	Repeat #1	-	-	R _{D̄} W _D	ReadModify Write	Read D̄-data and Write data D-data.
	2	Repeat #1	-	max to min, fast row	R _D	Read	Read D-data. Branch back to Instruction 1 until all addresses are accessed.
3	3	-	-	max to min, fast row	R _D	Read	Read D-data.

Example Algorithm Wrapper

[Figure A-2](#) illustrates the **Algorithm** wrapper for the example memory.

Figure A-2. LVMarchY Example Algorithm Wrapper

```

Algorithm (LVMarchY) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b0000000;
                NumberY0Bits : 0;
                NumberX0Bits : 0;
                ZCarryIn : Y1CarryOut;
                Y1CarryIn : X1CarryOut;
                X1CarryIn : None;
            }
        }
        DataGenerator {
            LoadWriteData : 8'b00000000;
            LoadExpectData : 8'b00000000;
        }
    }
    MicroProgram {
        Instruction (M0_W0) {
            OperationSelect : Write;
            AddressSelectCmd : Select_A;
            ZAddressCmd : Increment;
            X1AddressCmd : Increment;
            Y1AddressCmd : Increment;
            WriteDataCmd : DataReg;
            NextConditions {
                Z_EndCount : On;
                X1_EndCount : On;
                Y1_EndCount : On;
            }
        }
        Instruction (M1_R0_W1) {
            OperationSelect : ReadModifyWrite;
            AddressSelectCmd : Select_A;
            ExpectDataCmd : DataReg;
            WriteDataCmd : InverseDataReg;
            NextConditions {
            }
        }
        Instruction (M1_R1) {
            OperationSelect : Read;
            AddressSelectCmd : Select_A;
            ZAddressCmd : Increment;
            X1AddressCmd : Increment;
            Y1AddressCmd : Increment;
            ExpectDataCmd : InverseDataReg;
            InhibitLastAddressCount : On;
            BranchToInstruction : M1_R0_W1;
            NextConditions {
                Z_EndCount : On;
                X1_EndCount : On;
                Y1_EndCount : On;
            }
        }
    }
}

```

Fault Coverage

Table A-19 identifies the faults detected by the LVMarchY algorithm.

Table A-19. LVMarchY Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes
Transition Faults	Yes
Address Decoder Faults	Yes
Data Retention Faults	No
Inversion Coupling Faults	Yes
Idempotent Coupling Faults	No
Dynamic Coupling Faults	No
Transition Faults linked to Inversion Coupling Faults	Yes
Linked Idempotent Coupling Faults	No
Linked Dynamic Coupling Faults	No
Parametric Faults	Yes
Write Recovery Faults	Yes

Table A-19. LVMarchY Algorithm Fault Coverage (cont.)

Fault Type	Fault Coverage
Read Disturb Faults	Yes
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

Specification

The following specifications apply to the *LVMarchY* algorithm:

- To use the LVMarchY algorithm for the default algorithm, specify LVMarchY for the *HardCodedAlgorithm* property of the ETVerify configuration file.
- To download the LVMarchY algorithm to the controller, specify LVMarchY for the *SelectLibraryAlgorithm* property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the *LVMarchY* algorithm:

- Operations named Write, ReadModifyWrite, and Read must exist or be mapped to another operation in **OperationSet** specified in the memory library file.
- The *NumberOfInstructions* property of the .etplan file must be greater than or equal to four.

Related Information

[Notation Describing Memory BIST Algorithms](#) [Algorithm](#)

[HardCodedAlgorithm in the ETVerify Tool Reference](#) [NumberOfInstructions](#)

[SelectLibraryAlgorithm in the ETVerify Tool Reference](#)

LVMarchCMinus Algorithm

The LVMarchCMinus algorithm is only applicable to **Programmable** controllers.

The LVMarchCMinus algorithm is a test algorithm that is available for loading into the memory controller to perform a March C- algorithm. The March C- algorithm is performed as follows:

1. Write background of D-data incrementing from address minimum to address maximum.
2. Read D-data and write \bar{D} -data incrementing from address minimum to address maximum.
3. Read \bar{D} -data and write D-data incrementing from address minimum to address maximum.
4. Read D-data and write \bar{D} -data decrementing from address maximum to address minimum.
5. Read \bar{D} -data and write D-data decrementing from address maximum to address minimum.
6. Read D-data decrementing from address maximum to address minimum.

Test Length

$10N_{xyz}$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$Z \Leftarrow Y1 \Leftarrow X1$

where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed and a carry out from the X1 address segment is generated. An X1CarryOut is generated when:
 - The X1 address segment is incrementing and has reached the maximum OR.
 - The X1 address segment is decrementing and has reached the minimum.
- The bank address segment Z counts when instructed and a carry out from the Y1 address segment is generated. An Y1CarryOut is generated when:
 - The Y1 address segment is incrementing and has reached the maximum AND a X1CarryOut is generated OR.

- o The Y1 address segment is decrementing and has reached the minimum AND a X1CarryOut is generated.

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

Algorithm Sequence

[Table A-20](#) describes the LVMarchCMinus algorithm sequence.

Table A-20. Description of LVMarchCMinus Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast row	W _D	Write	Write background of D-data.
1	1	-	-	min to max, fast row	R _D W _{̄D}	ReadModify Write	Read D-data and Write data \overline{D} -data. After all addresses have been accessed branch to instruction 1 and repeat three times as follows with RepeatLoop(A): Repeat #1 - repeat instructions with inverted write data sequencing and expect data sequencing Repeat #2 - repeat instructions with inverted the address sequencing Repeat #3 - repeat instructions with inverted the address sequencing, write data sequencing, and expect data sequencing
2	1	Repeat #1	-	min to max, fast row	R _{̄D} W _D	ReadModify Write	Read \overline{D} -data and Write data D-data.
3	1	Repeat #2	-	max to min, fast row	R _D W _{̄D}	ReadModify Write	Read D-data and Write data \overline{D} -data.

Table A-20. Description of LVMarchCMinus Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
4	1	Repeat #3	-	max to min, fast row	R _D W _D	ReadModify Write	Read \bar{D} -data and Write data D-data.
5	2	-	-	max to min, fast row	R _D	Read	Read D-data.

Example Algorithm Wrapper

Figure A-3 illustrates the **Algorithm** wrapper for the example memory.

Figure A-3. LVMarchCMinus Example Algorithm Wrapper

```

algorithm (LVMarchCMinus) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b0000000;
                NumberY0Bits : 0;
                NumberX0Bits : 0;
                ZCarryIn : Y1CarryOut;
                Y1CarryIn : X1CarryOut;
                X1CarryIn : None;
            }
        }
        DataGenerator {
            LoadWriteData : 8'b00000000;
            LoadExpectData : 8'b00000000;
        }
    }
    MicroProgram {
        Instruction (M0_W0) {
            OperationSelect : Write;
            AddressSelectCmd : Select_A;
            ZAddressCmd : Increment;
            X1AddressCmd : Increment;
            Y1AddressCmd : Increment;
            WriteDataCmd : DataReg;
            NextConditions {
                Z_EndCount : On;
                X1_EndCount : On;
                Y1_EndCount : On;
            }
        }
    }
}

```

```

Instruction (M1_R0_W1) {
    OperationSelect : Readmodifywrite;
    AddressSelectCmd : Select_A;
    ZAddressCmd : Increment;
    X1AddressCmd : Increment;
    Y1AddressCmd : Increment;
    ExpectDataCmd : DataReg;
    WriteDataCmd : InverseDataReg;
    NextConditions {
        Z_EndCount : On;
        X1_EndCount : On;
        Y1_EndCount : On;
        RepeatLoop (a) {
            BranchToInstruction : M1_R0_W1;
            Repeat {
                WriteDataSequence : Inverse;
                ExpectDataSequence : Inverse;
                InhibitLastAddressCount : On;
            }
            Repeat {
                AddressSequence : Inverse;
            }
            Repeat {
                AddressSequence : Inverse;
                ExpectDataSequence : Inverse;
                WriteDataSequence : Inverse;
            }
        }
    }
}

Instruction (M5_R0) {
    OperationSelect : Read;
    AddressSelectCmd : Select_A;
    ZAddressCmd : Decrement;
    X1AddressCmd : Decrement;
    Y1AddressCmd : Decrement;
    ExpectDataCmd : DataReg;
    InhibitLastAddressCount : On;
    NextConditions {
        Z_EndCount : On;
        X1_EndCount : On;
        Y1_EndCount : On;
    }
}
}

```

Fault Coverage

Table A-21 identifies the faults detected by the LVMarchCMinus algorithm.

Table A-21. LVMarchCMinus Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes

Table A-21. LVMarchCMinus Algorithm Fault Coverage (cont.)

Fault Type	Fault Coverage
Transition Faults	Yes
Address Decoder Faults	Yes
Data Retention Faults	No
Inversion Coupling Faults	Yes
Idempotent Coupling Faults	Yes
Dynamic Coupling Faults	Yes
Transition Faults linked to Inversion Coupling Faults	No
Linked Idempotent Coupling Faults	No
Linked Dynamic Coupling Faults	No
Parametric Faults	Yes
Write Recovery Faults	Yes
Read Disturb Faults	Yes
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

Specification

The following specifications apply to the *LVMarchCMinus* algorithm:

- To use the LVMarchCMinus algorithm for the default algorithm, specify LVMarchCMinus for the *HardCodedAlgorithm* property of the ETVerify configuration file.
- To download the LVMarchCMinus algorithm to the controller, specify LVMarchCMinus for the *SelectLibraryAlgorithm* property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the *LVMarchCMinus* algorithm:

- Operations named Write, ReadModifyWrite, and Read must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The *MemBistControllerOptions: NumberOfInstructions* property of the .etplan file must be greater than or equal to three.

Related Information

[Notation Describing Memory BIST Algorithms](#) [Algorithm](#)

[HardCodedAlgorithm in the ETVerify Tool Reference](#) [NumberOfInstructions](#)

[*SelectLibraryAlgorithm*](#) in the *ETVerify Tool Reference*

LVMarchLA Algorithm

The LVMarchLA algorithm is only applicable to **Programmable** controllers.

The LVMarchLA algorithm is a test algorithm that is available for loading into the memory controller to perform a March LA algorithm. The March LA algorithm is performed as follows:

1. Write background of D-data incrementing from address minimum to address maximum.
2. Read D-data, write \bar{D} -data, write D-data, write \bar{D} -data, and read \bar{D} -data incrementing from address minimum to address maximum.
3. Read \bar{D} -data, write D-data, write \bar{D} -data, write D-data, and read D-data incrementing from address minimum to address maximum.
4. Read D-data, write \bar{D} -data, write D-data, write \bar{D} -data, and read \bar{D} -data decrementing from address maximum to address minimum.
5. Read \bar{D} -data, write D-data, write \bar{D} -data, write D-data, and read D-data decrementing from address maximum to address minimum.
6. Read D-data decrementing from address maximum to address minimum.

Test Length

$22N_{xyz}$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$Z \Leftarrow Y1 \Leftarrow X1$

where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed and a carry out from the X1 address segment is generated. An X1CarryOut is generated when:
 - The X1 address segment is incrementing and has reached the maximum OR.
 - The X1 address segment is decrementing and has reached the minimum.
- The bank address segment Z counts when instructed and a carry out from the Y1 address segment is generated. An Y1CarryOut is generated when:
 - The Y1 address segment is incrementing and has reached the maximum AND a X1CarryOut is generated OR.

- The Y1 address segment is decrementing and has reached the minimum AND a X1CarryOut is generated.

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

Algorithm Sequence

[Table A-22](#) describes the LVMarchLA algorithm sequence.

Table A-22. Description of LVMarchLA Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast row	W _D	Write	Write background of D-data.
1	1	-	-	-	R _D W _{̄D}	ReadModify Write	Read D-data and Write data \overline{D} -data.
	2	-	-		W _D	Write	Write \overline{D} -data.
	3	-	-	min to max, fast row	W _{̄D} R _{̄D}	WriteRead	Write \overline{D} -data and Read data \overline{D} -data. Branch back to Instruction 1 until all addresses are accessed. After all addresses have been accessed branch to instruction 1 and repeat three times as follows with RepeatLoop(A): Repeat #1 - repeat instructions with inverted write data sequencing and expect data sequencing Repeat #2 - repeat instructions with inverted the address sequencing Repeat #3 - repeat instructions with inverted the address sequencing, write data sequencing, and expect data sequencing

Table A-22. Description of LVMarchLA Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
2	1	Repeat #1	-	-	R _{D̄} W _D	ReadModify Write	Read D̄-data and Write data D-data.
	2	Repeat #1	-		W _{D̄}	Write	Write D-data.
	3	Repeat #1	-	min to max, fast row	W _D R _D	WriteRead	Write D-data and Read data D-data. Branch back to Instruction 1 until all addresses are accessed.
3	1	Repeat #2	-	-	R _D W _{D̄}	ReadModify Write	Read D-data and Write data D̄-data.
	2	Repeat #2	-		W _D	Write	Write D̄-data.
	3	Repeat #2	-	max to min, fast row	W _{D̄} R _{D̄}	WriteRead	Write D̄-data and Read data D̄-data. Branch back to Instruction 1 until all addresses are accessed.
4	1	Repeat #3	-	-	R _{D̄} W _D	ReadModify Write	Read D̄-data and Write data D-data.
	2	Repeat #3	-	-	W _{D̄}	Write	Write D-data.
	3	Repeat #3	-	max to min, fast row	W _D R _D	WriteRead	Write D-data and Read data D-data. Branch back to Instruction 1 until all addresses are accessed.
5	4	-	-	max to min, fast row	R _D	Read	Read D-data.

Example Algorithm Wrapper

Figure A-4 illustrates the **Algorithm** wrapper for the example memory.

Figure A-4. LVMarchLA Example Algorithm Wrapper

```
Algorithm (LVMarchLA) {
    TestRegisterSetup {
```

```

OperationSetSelect LVMarchLA :
    ReadLatency_RL11;
AddressGenerator {
    AddressRegister (A) {
        LoadBankAddress : 2'b00;
        LoadRowAddress : 4'b0000;
        LoadColumnAddress : 6'b0000000;
        NumberY0Bits : 0;
        NumberX0Bits : 0;
        ZCarryIn : Y1CarryOut;
        Y1CarryIn : X1CarryOut;
        X1CarryIn : none;
    }
}
DataGenerator {
    LoadWriteData : 8'b00000000;
    LoadExpectData : 8'b00000000;
}
MicroProgram {
    Instruction (M0_W0) {
        OperationSelect : Write;
        AddressSelectCmd : Select_A;
        ZAddressCmd : Increment;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        WriteDataCmd : DataReg;
        NextConditions {
            Z_EndCount : On;
            X1_EndCount : On;
            Y1_EndCount : On;
        }
    }
    Instruction (M1_R0_W1) {
        OperationSelect : ReadModifyWrite;
        AddressSelectCmd : Select_A;
        ExpectDataCmd : DataReg;
        WriteDataCmd : InverseDataReg;
        NextConditions {
        }
    }
    Instruction (M1_W0) {
        OperationSelect : Write;
        AddressSelectCmd : Select_A;
        WriteDataCmd : DataReg;
        NextConditions {
        }
    }
    Instruction (M1_W1_R1) {
        OperationSelect : Write_read_operation;
        AddressSelectCmd : Select_A;
        ZAddressCmd : Increment;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        WriteDataCmd : InverseDataReg;
        ExpectDataCmd : InverseDataReg;
        BranchToInstruction : M1_R0_W1;
        NextConditions {
    }
}

```

```

Z_EndCount : On;
X1_EndCount : On;
Y1_EndCount : On;
RepeatLoop (a) {
    BranchToInstruction : M1_R0_W1;
    Repeat {
        WriteDataSequence : Inverse;
        ExpectDataSequence : Inverse;
        InhibitLastAddressCount : On;
    }
    Repeat {
        AddressSequence : Inverse;
    }
    Repeat {
        AddressSequence : Inverse;
        WriteDataSequence : Inverse;
        ExpectDataSequence : Inverse;
    }
}
}

Instruction (M5_R0) {
    OperationSelect : Read;
    AddressSelectCmd : Select_A;
    ZAddressCmd : Decrement;
    X1AddressCmd : Decrement;
    Y1AddressCmd : Decrement;
    ExpectDataCmd : DataReg;
    InhibitLastAddressCount : On;
    NextConditions {
        Z_EndCount : On;
        X1_EndCount : On;
        Y1_EndCount : On;
    }
}

```

Fault Coverage

Table A-23 identifies the faults detected by the LVMarchLA algorithm.

Table A-23. LVMarchLA Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes
Transition Faults	Yes
Address Decoder Faults	Yes
Data Retention Faults	No
Inversion Coupling Faults	Yes
Idempotent Coupling Faults	Yes

Table A-23. LVMarchLA Algorithm Fault Coverage (cont.)

Fault Type	Fault Coverage
Dynamic Coupling Faults	Yes
Transition Faults linked to Inversion Coupling Faults	Yes
Linked Idempotent Coupling Faults	Yes
Linked Dynamic Coupling Faults	Yes
Parametric Faults	Yes
Write Recovery Faults	Yes
Read Disturb Faults	Yes
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

Specification

The following specifications apply to the LVMarchLA algorithm:

- To use the LVMarchLA algorithm for the default algorithm, specify LVMarchLA for the *HardCodedAlgorithm* property of the ETVerify configuration file.
- To download the LVMarchLA algorithm to the controller, specify LVMarchLA for the *SelectLibraryAlgorithm* property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVMarchLA algorithm:

- Operations named Write, ReadModifyWrite, *WriteRead*, and Read must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The *MemBistControllerOptions: NumberOfInstructions* property of the .etplan file must be greater than or equal to five.

Related Information

[Notation Describing Memory BIST Algorithms](#) [Algorithm](#)

[HardCodedAlgorithm in the ETVerify Tool Reference](#) [NumberOfInstructions](#)

[SelectLibraryAlgorithm in the ETVerify Tool Reference](#)

LVRowBar Algorithm

The LVRowBar algorithm is only applicable to **Programmable** controllers.

The LVRowBar algorithm is a test algorithm that is available for loading into the memory controller to perform a row bar algorithm. The row bar algorithm is performed as follows:

- Write background of D-data to even columns and \bar{D} -data to odd columns incrementing from address minimum to address maximum for a single bank.
- Read D-data from even columns and \bar{D} -data from odd columns incrementing from address minimum to address maximum for a single bank.
- Re-execute 1.) and 2.) incrementing the bank address from minimum to maximum.
- Repeat 1.) to 3.) with inverted data.

Test Length

$$4N_{xyz}$$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast columns as follows:

$$Z \quad X1 \leftarrow Y1$$

where:

- The column address segment Y1 counts when instructed.
- The row address segment X1 counts when instructed and a carry out from the Y1 address segment is generated. An Y1CarryOut is generated when:
 - The Y1 address segment is incrementing and has reached the maximum OR.
 - The Y1 address segment is decrementing and has reached the minimum.
- The bank address segment Z counts when instructed.

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

The logical data pattern applied is inverted with each column. That is the logical data pattern applied is D for even columns and \bar{D} for odd columns.

Algorithm Sequence

[Table A-24](#) describes the LVRowBar algorithm sequence.

Table A-24. Description of LVRowBar Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast column	W_{D_e}, \bar{D}_o	Write	Write background of D-data to even column addresses and \bar{D} -data to odd column addresses.
1	1	-	-	max to min, fast column	R_{D_e}, \bar{D}_o	Read	Read background of D-data from even column addresses and \bar{D} -data from odd column addresses.
2	2	-	-	min to max, bank addresses	-	NoOperation	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed branch to instruction 0 and repeat one time as follows with RepeatLoop(B): Repeat #1 - repeat instructions with inverted write data sequencing and expect data sequencing
3	0	-	Repeat #1	min to max, fast column	$W_{\bar{D}_e}, D_o$	Write	Write background of \bar{D} -data to even column addresses and D-data to odd column addresses.
4	1	-	Repeat #1	max to min, fast column	$R_{\bar{D}_e}, D_o$	Read	Read background of \bar{D} -data from even column addresses and D-data from odd column addresses.
5	2	-	Repeat #1	min to max, bank addresses	-	NoOperation	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses.

Example Algorithm Wrapper

Figure A-5 illustrates the **Algorithm** wrapper for the example memory.

Figure A-5. LVRowBar Example Algorithm Wrapper

```
Algorithm (LVRowBar) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b0000000;
                NumberY0Bits : 0;
                NumberX0Bits : 0;
                ZCarryIn : None;
                X1CarryIn : Y1CarryOut;
                Y1CarryIn : None;
            }
        }
        DataGenerator {
            InvertDataWithColumnBit : c[0];
            LoadWriteData : 8'b00000000;
            LoadExpectData : 8'b00000000;
        }
    }
    MicroProgram {
        Instruction (W0) {
            OperationSelect : Write;
            AddressSelectCmd : Select_A;
            X1AddressCmd : Increment;
            Y1AddressCmd : Increment;
            WriteDataCmd : Zero;
            NextConditions {
                X1_EndCount : On;
                Y1_EndCount : On;
            }
        }
        Instruction (R0) {
            OperationSelect : Read;
            AddressSelectCmd : Select_A;
            X1AddressCmd : Increment;
            Y1AddressCmd : Increment;
            ExpectDataCmd : Zero;
            NextConditions {
                X1_EndCount : On;
                Y1_EndCount : On;
            }
        }
        Instruction (GOTO_NEXT_BANKADDRESS) {
            OperationSelect : NoOperation;
            AddressSelectCmd : Select_A;
            ZAddressCmd : Increment;
            BranchToInstruction : W0;
            NextConditions {
                Z_EndCount : On;
            }
        }
    }
}
```

```
    RepeatLoop (B) {
        BranchToInstruction: W0;
        Repeat {
            WriteDataSequence: Inverse;
            ExpectDataSequence: Inverse;
        }
    }
}
```

Fault Coverage

Table A-25 identifies the faults detected by the *LVRowBar* algorithm.

Table A-25. LVRowBar Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes ¹
Transition Faults	No
Address Decoder Faults	No
Data Retention Faults	No
Inversion Coupling Faults	No
Idempotent Coupling Faults	No
Dynamic Coupling Faults	No
Transition Faults linked to Inversion Coupling Faults	No
Linked Idempotent Coupling Faults	No
Linked Dynamic Coupling Faults	No
Parametric Faults	No
Write Recovery Faults	No
Read Disturb Faults	No
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

1. Stuck-At faults are detected correctly when there are no address decoder faults.

Specification

The following specifications apply to the LVRowBar algorithm:

- To use the LVRowBar algorithm for the default algorithm, specify LVRowBar for the *HardCodedAlgorithm* property of the ETVerify configuration file.
- To download the LVRowBar algorithm to the controller, specify LVRowBar for the *SelectLibraryAlgorithm* property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVRowBar algorithm:

- Operations named Write and Read must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The *MemBistControllerOptions: NumberOfInstructions* property of the .etplan file must be greater than or equal to three.

Related Information

Notation Describing Memory BIST Algorithms	Algorithm
<i>HardCodedAlgorithm</i> in the <i>ETVerify Tool Reference</i>	<i>NumberOfInstructions</i>
<i>SelectLibraryAlgorithm</i> in the <i>ETVerify Tool Reference</i>	

LVColumnBar Algorithm

The LVColumnBar algorithm is only applicable to **Programmable** controllers.

The LVColumnBar algorithm is a test algorithm that is available for loading into the memory controller to perform a column bar algorithm. The column bar algorithm is performed as follows:

1. Write background of D-data to even rows and \bar{D} -data to odd rows incrementing from address minimum to address maximum for a single bank.
2. Read D-data from even rows and \bar{D} -data from odd rows incrementing from address minimum to address maximum for a single bank.
3. Re-execute 1 and 2 incrementing the bank address from minimum to maximum.
4. Repeat 1 to 3 with inverted data.

Test Length

$$4N_{xyz}$$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$$Z \quad Y1 \Leftarrow X1$$

where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed and a carry out from the X1 address segment is generated. An X1CarryOut is generated when:
 - The X1 address segment is incrementing and has reached the maximum OR.
 - The X1 address segment is decrementing and has reached the minimum.
- The bank address segment Z counts when instructed.

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

The logical data pattern applied is inverted with each row. That is the logical data pattern applied is D for even rows and \bar{D} for odd rows.

Algorithm Sequence

[Table A-26](#) describes the LVColumnBar algorithm sequence.

Table A-26. Description of LVColumnBar Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast row	W_{D_e}, \bar{D}_o	Write	Write background of D-data to even row addresses and \bar{D} -data to odd row addresses.
1	1	-	-	max to min, fast row	R_{D_e}, \bar{D}_o	Read	Read background of D-data from even row addresses and \bar{D} -data from odd row addresses.
2	2	-	-	min to max, bank addresses	-	NoOperation	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed branch to instruction 0 and repeat one time as follows with RepeatLoop(B): Repeat #1 - repeat instructions with inverted write data sequencing and expect data sequencing
3	0	-	Repeat #1	min to max, fast row	$W_{\bar{D}_e}, D_o$	Write	Write background of \bar{D} -data to even row addresses and D-data to odd row addresses.
4	1	-	Repeat #1	max to min, fast row	$R_{\bar{D}_e}, D_o$	Read	Read background of \bar{D} -data from even row addresses and D-data from odd row addresses.
5	2	-	Repeat #1	min to max, bank addresses	-	NoOperation	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses.

Example Algorithm Wrapper

[Figure A-6](#) illustrates the **Algorithm** wrapper for the example memory.

Figure A-6. LVColumnBar Example Algorithm Wrapper

```

Algorithm (LVColumnBar) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b0000000;
                NumberY0Bits : 0;
                NumberX0Bits : 0;
                ZCarryIn : None;
                Y1CarryIn : X1CarryOut;
                X1CarryIn : None;
            }
        }
        DataGenerator {
            InvertDataWithRowBit : r[0];
            LoadWriteData : 8'b00000000;
            LoadExpectData : 8'b00000000;
        }
    }
    MicroProgram {
        Instruction (W0) {
            OperationSelect : Write;
            AddressSelectCmd : Select_A;
            X1AddressCmd : Increment;
            Y1AddressCmd : Increment;
            WriteDataCmd : Zero;
            NextConditions {
                X1_EndCount : On;
                Y1_EndCount : On;
            }
        }
        Instruction (R0) {
            OperationSelect : Read;
            AddressSelectCmd : Select_A;
            X1AddressCmd : Increment;
            Y1AddressCmd : Increment;
            ExpectDataCmd : Zero;
            NextConditions {
                X1_EndCount : On;
                Y1_EndCount : On;
            }
        }
        Instruction (GOTO_NEXT_BANKADDRESS) {
            OperationSelect : Nooperation;
            AddressSelectCmd : Select_A;
            ZAddressCmd : Increment;
            BranchToInstruction : W0;
            NextConditions {
                Z_EndCount : On;
                RepeatLoop (B) {
                    BranchToInstruction: W0;
                    Repeat {
                        WriteDataSequence: Inverse;
                    }
                }
            }
        }
    }
}

```

```
        ExpectDataSequence: Inverse;  
    }  
}  
}  
}  
}  
}  
}
```

Fault Coverage

[Table A-27](#) identifies the faults detected by the LVColumnBar algorithm.

Table A-27. LVColumnBar Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes ¹
Transition Faults	No
Address Decoder Faults	No
Data Retention Faults	No
Inversion Coupling Faults	No
Idempotent Coupling Faults	No
Dynamic Coupling Faults	No
Transition Faults linked to Inversion Coupling Faults	No
Linked Idempotent Coupling Faults	No
Linked Dynamic Coupling Faults	No
Parametric Faults	No
Write Recovery Faults	No
Read Disturb Faults	No
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

1. Stuck-At faults are detected correctly when there are no address decoder faults.

Specification

The following specifications apply to the LVColumnBar algorithm:

- To use the LVColumnBar algorithm for the default algorithm, specify LVColumnBar for the **HardCodedAlgorithm** property of the ETVerify configuration file.
- To download the LVColumnBar algorithm to the controller, specify LVColumnBar for the **SelectLibraryAlgorithm** property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVColumnBar algorithm:

- Operations named Write and Read must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The **MemBistControllerOptions: NumberOfInstructions** property of the *.etplan* file must be greater than or equal to three.

Related Information

[Notation Describing Memory BIST Algorithms](#)

LVGalPat Algorithm

The LVGalPat algorithm is only applicable to **Programmable** controllers.

The LVGalPat algorithm is a test algorithm that is available for loading into the memory controller to perform a galloping pattern algorithm. The LVGalPat algorithm is performed as follows:

1. Write background of D-data from address minimum to address maximum for a single bank.
2. Write \bar{D} -data to the “home” cell addressed by AddressRegister(A).
3. Read D-data from all “away” cells in the same bank addressed by AddressRegister(B) but following each read of the “away” cell read \bar{D} -data from the “home” cell.
4. Write D-data at the “home” cell to restore the data background.
5. Increment the “home” cell addressed by AddressRegister(A) and re-execute steps 2 to 5 until every cell in the bank has been a “home” cell.
6. Increment the bank address from minimum to maximum and re-execute steps 1 to 6.
7. Repeat steps 1 to 6 with inverted data.

Test Length

$$2 (2N_{xy}^2 + 3N_{xy}) N_z$$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$$Z \quad Y1 \Leftarrow X1$$

where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed and a carry out from the X1 address segment is generated. An X1CarryOut is generated when:
 - The X1 address segment is incrementing and has reached the maximum OR.
 - The X1 address segment is decrementing and has reached the minimum.
- The bank address segment Z counts when instructed.

AddressRegister(B)

The AddressRegister(B) segments are configured identically to AddressRegister(A).

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

The logical data pattern applied is inverted with each column. That is, the logical data pattern applied is D for even columns and \bar{D} for odd columns.

Algorithm Sequence

[Table A-28](#) describes the LVGalPat algorithm sequence.

Table A-28. Description of LVGalPat Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast row	W_D	Write	Write background of D-data.
1	1	-	-	-	$W_{\bar{D}}$	Write	Write \bar{D} -data to location addressed by AddressRegister(A).
2	2	-	-	-	$R_{\bar{D}}$	Read	Read \bar{D} -data to location addressed by AddressRegister(A).
	3	-	-	Address Register (B) min to max, fast row	R_D	Read	Read D-data from all addresses using AddressRegister(B). When AddressRegister(B) is equivalent to AddressRegister(A) the read \bar{D} -data is expected. Branch back to Instruction 2 and repeat for all AddressRegister(B) row and column addresses.
	4	-	-	Address Register (A) min to max, fast row	$R_{\bar{D}}W_D$	ReadModify Write	Read \bar{D} -data and write D-data at the location addressed by AddressRegister(A). Branch back to Instruction 2 and repeat for all AddressRegister(A) row and column addresses.

Table A-28. Description of LVGaIPat Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
3	5	-	-	min to max, bank addresses	-	NoOperation	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed branch to instruction 0 and repeat one time as follows with RepeatLoop(B): Repeat #1 - repeat instructions with inverted write data sequencing and expect data sequencing.
0	0	-	Repeat #1	min to max, fast row	$W_{\bar{D}}$	Write	Write background of D-data.
1	1	-	Repeat #1	-	W_D	Write	Write \bar{D} -data to location addressed by AddressRegister(A).

Table A-28. Description of LVGalPat Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
2	2	-	Repeat #1	-	R _D	Read	Read \bar{D} -data to location addressed by AddressRegister(A).
	3	-	Repeat #1	Address Register (B) min to max, fast row	R \bar{D}	Read	Read D-data from all addresses using AddressRegister(B). When AddressRegister(B) is equivalent to AddressRegister(A) the read \bar{D} -data is expected. Branch back to Instruction 2 and repeat for all AddressRegister(B) row and column addresses.
	4	-	Repeat #1	Address Register (A) min to max, fast row	R _D W \bar{D}	ReadModify Write	Read \bar{D} -data and write D-data at the location addressed by AddressRegister(A). Branch back to Instruction 2 and repeat for all AddressRegister(A) row and column addresses.
3	5	-	Repeat #1	min to max, bank addresses	-	NoOperation	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed repeat phase 0 and 1 with inverted write and expect data.

Example Algorithm Wrapper

Figure A-7 illustrates the **Algorithm** wrapper for the example memory.

Figure A-7. LVGalPat Example Algorithm Wrapper

```

Algorithm (LVGalPat) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;

```

```
LoadRowAddress : 4'b0000;
LoadColumnAddress : 6'b0000000;
NumberY0Bits : 0;
NumberX0Bits : 0;
ZCarryIn : None;
Y1CarryIn : X1CarryOut;
X1CarryIn : None;
}
AddressRegister (B) {
    LoadBankAddress : 2'b00;
    LoadRowAddress : 4'b0000;
    LoadColumnAddress : 6'b0000000;
    NumberY0Bits : 0;
    NumberX0Bits : 0;
    ZCarryIn : None;
    Y1CarryIn : X1CarryOut;
    X1CarryIn : None;
}
}
DataGenerator {
    LoadWriteData : 8'b00000000;
    LoadExpectData : 8'b00000000;
}
}
MicroProgram {
    Instruction (WRITE_BACKGROUND) {
        OperationSelect : Write;
        AddressSelectCmd : Select_A;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        WriteDataCmd : DataReg;
        NextConditions {
            X1_EndCount : On;
            Y1_EndCount : On;
        }
    }
    Instruction (WRITE_HOME_CELL) {
        OperationSelect : Write;
        AddressSelectCmd : Select_A;
        WriteDataCmd : InverseDataReg;
        NextConditions {
        }
    }
    Instruction (READ_HOME_CELL) {
        OperationSelect : Read;
        AddressSelectCmd : Select_A;
        ExpectDataCmd : InverseDataReg;
        NextConditions {
        }
    }
    Instruction (READ_AWAY_CELL) {
        OperationSelect : Read;
        AddressSelectCmd : Select_B;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        ExpectDataCmd : DataReg;
        Add_reg_a_equals_b : Invert_ExpectData;
        BranchToInstruction : READ_HOME_CELL;
    }
}
```

```

        NextConditions {
            X1_EndCount : On;
            Y1_EndCount : On;
        }
    }
Instruction (REWRITE_HOME_CELL_AND_ADVANCE)

    OperationSelect : ReadModifyWrite;
    AddressSelectCmd : Select_A;
    X1AddressCmd : Increment;
    Y1AddressCmd : Increment;
    WriteDataCmd : DataReg;
    ExpectDataCmd : InverseDataReg;
    BranchToInstruction : WRITE_HOME_CELL;
    NextConditions
        X1_EndCount : On;
        Y1_EndCount : On;
    }
}
Instruction (GOTO_NEXT_BANKADDRESS) {

    OperationSelect : NoOperation;
    AddressSelectCmd : Select_A_Copy_to_B;
    ZAddressCmd : Increment;
    BranchToInstruction : WRITE_BACKGROUND;
    NextConditions {
        Z_EndCount : On;
        RepeatLoop (B) {
            BranchToInstruction:
                WRITE_BACKGROUND;
            Repeat {
                WriteDataSequence: Inverse;
                ExpectDataSequence: Inverse;
            }
        }
    }
}

```

Fault Coverage

Table A-29 identifies the faults detected by the LVGalPat algorithm.

Table A-29. LVGalPat Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes
Transition Faults	Yes
Address Decoder Faults	Yes
Data Retention Faults	No
Inversion Coupling Faults	Yes

Table A-29. LVGALPAT Algorithm Fault Coverage (cont.)

Fault Type	Fault Coverage
Idempotent Coupling Faults	Yes
Dynamic Coupling Faults	Yes
Transition Faults linked to Inversion Coupling Faults	Yes
Linked Idempotent Coupling Faults	Yes
Linked Dynamic Coupling Faults	Yes
Parametric Faults	Yes
Write Recovery Faults	Yes
Read Disturb Faults	Yes
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

Specification

The following specifications apply to the LVGALPAT algorithm:

- To use the LVGALPAT algorithm for the default algorithm, specify LVGALPAT for the **HardCodedAlgorithm** property of the ETVerify configuration file.
- To download the LVGALPAT algorithm to the controller, specify LVGALPAT for the **SelectLibraryAlgorithm** property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVGALPAT algorithm:

- Operations named Write, Read, ReadModifyWrite must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The **MemBistControllerOptions: NumberOfInstructions** property of the *.etplan* file must be greater than or equal to three.
- If the **EnableAEqualsBCommand** property is set to *No* in the *.etplan* file, the LVGALPAT algorithm is not available.

Related Information

[Notation Describing Memory BIST Algorithms](#)

[*EnableAEqualsBCommand*](#)

[Algorithm](#)

[*HardCodedAlgorithm* in the *ETVerify Tool Reference*](#)

[*NumberOfInstructions*](#)

[*SelectLibraryAlgorithm* in the *ETVerify Tool Reference*](#)

LVGalColumn Algorithm

The LVGalColumn algorithm is only applicable to **Programmable** controllers.

The LVGalColumn algorithm is a test algorithm that is available for loading into the memory controller to perform a galloping column pattern algorithm. The galcolumn algorithm is performed as follows:

1. Write background of D-data from address minimum to address maximum for a single bank.
2. Write \bar{D} -data to the “home” cell addressed by AddressRegister(A).
3. Read D-data from all “away” cells in the same column (same Y address) of the same bank addressed by AddressRegister(B). Following each read of the “away” cell read \bar{D} -data from the “home” cell.
4. Write D-data at the “home” cell to restore the data background.
5. Increment the “home” cell addressed by AddressRegister(A) and re-execute steps 2 to 5 until every cell in the bank has been a “home” cell.
6. Increment the bank address from minimum to maximum and re-execute steps 1 to 6.
7. Repeat steps 1 to 6 with inverted data.

Test Length

$$2 (3N_{xy} + 2N_x (N_{xy})) N_z$$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$$Z \quad X1 \Leftarrow Y1$$

where:

- The column address segment Y1 counts when instructed.
- The row address segment X1 counts when instructed and a carry out from the Y1 address segment is generated. An Y1CarryOut is generated when:
 - The Y1 address segment is incrementing and has reached the maximum OR.
 - The Y1 address segment is decrementing and has reached the minimum.

- The bank address segment Z counts when instructed.

AddressRegister(B)

The AddressRegister(B) segments are configured to count each of the segments individually where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed.
- The bank address segment Z counts when instructed.

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

The logical data pattern applied is inverted with each column. That is the logical data pattern applied is D for even columns and \bar{D} for odd columns.

Algorithm Sequence

[Table A-30](#) describes the LVGalColumn algorithm sequence.

Table A-30. Description of LVGalColumn Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast column	W_D	<i>Write</i>	Write background of D-data.
1	1	-	-	-	$W_{\bar{D}}$	<i>Write</i>	Write \bar{D} -data to location addressed by AddressRegister(A).

Table A-30. Description of LVGalColumn Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
2	2	-	-	-	$R_{\bar{D}}$	<i>Read</i>	Read \bar{D} -data to location addressed by AddressRegister(A).
	3	-	-	Address Register (B) row address min to max	R_D	<i>Read</i>	Read D-data from all row addresses in the same column using AddressRegister(B). When AddressRegister(B) is equivalent to AddressRegister(A) the read \bar{D} -data is expected. Branch back to Instruction 2 and repeat for all AddressRegister(B) row addresses.
	4	-	-	-	-	<i>NoOperation</i>	Advance the column address by one.
	5	-	-	Address Register (A) min to max, fast column	$R_{\bar{D}}W_D$	<i>ReadModifyWrite</i>	Read \bar{D} -data and write D-data at the location addressed by AddressRegister(A). Branch back to Instruction 2 and repeat for all AddressRegister(A) row and column addresses.
3	6	-	-	min to max, bank addresses	-	<i>NoOperation</i>	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed branch to instruction 0 and repeat one time as follows with RepeatLoop(B): Repeat #1 - repeat instructions with inverted write data sequencing and expect data sequencing.

Table A-30. Description of LVGalColumn Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
4	0	-	Repeat #1	min to max, fast column	W _D	Write	Write background of D-data.
5	1	-	Repeat #1	-	W _{D̄}	Write	Write \bar{D} -data to location addressed by AddressRegister(A).
6	2	-	Repeat #1	-	R _{D̄}	Read	Read \bar{D} -data to location addressed by AddressRegister(A).
	3	-	Repeat #1	Address Register (B) row address min to max	R _D	Read	Read D-data from all row addresses in the same column using AddressRegister(B). When AddressRegister(B) is equivalent to AddressRegister(A) the read \bar{D} -data is expected. Branch back to Instruction 2 and repeat for all AddressRegister(B) row addresses.
	4	-	Repeat #1	-	-	NoOperation	Advance the column address by one.
	5	-	Repeat #1	Address Register (A) min to max, fast column	R _{D̄} W _D	ReadModifyWrite	Read \bar{D} -data and write D-data at the location addressed by AddressRegister(A). Branch back to Instruction 2 and repeat for all AddressRegister(A) row and column addresses.
7	6	-	Repeat #1	min to max, bank addresses	-	NoOperation	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed repeat phase 0 and 1 with inverted write and expect data.

Example Algorithm Wrapper

[Figure A-8](#) illustrates the **Algorithm** wrapper for the example memory.

Figure A-8. LVGAIColumn Example Algorithm Wrapper

```

Algorithm (LVGAIColumn) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b0000000;
                NumberY0Bits : 0;
                NumberX0Bits : 0;
                ZCarryIn : None;
                X1CarryIn : Y1CarryOut;
                Y1CarryIn : None;
            }
            AddressRegister (B) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b0000000;
                NumberY0Bits : 0;
                NumberX0Bits : 0;
                ZCarryIn : None;
                Y1CarryIn : None;
                X1CarryIn : None;
            }
        }
        DataGenerator {
            LoadWriteData : 8'b00000000;
            LoadExpectData : 8'b00000000;
        }
    }
    MicroProgram {
        Instruction (WRITE_BACKGROUND) {
            OperationSelect : Write;
            AddressSelectCmd : Select_A;
            X1AddressCmd : Increment;
            Y1AddressCmd : Increment;
            WriteDataCmd : DataReg;
            NextConditions {
                X1_EndCount : On;
                Y1_EndCount : On;
            }
        }
        Instruction (WRITE_HOME_CELL) {
            OperationSelect : Write;
            AddressSelectCmd : Select_A;
            WriteDataCmd : InverseDataReg;
            NextConditions {
            }
        }
        Instruction (READ_HOME_CELL) {
            OperationSelect : Read;
        }
    }
}

```


Fault Coverage

Table A-31 identifies the faults detected by the LVGalColumn algorithm.

Table A-31. LVGalColumn Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes
Transition Faults	Yes
Address Decoder Faults	Some
Data Retention Faults	No
Inversion Coupling Faults	Yes ¹
Idempotent Coupling Faults	Yes ¹
Dynamic Coupling Faults	Yes ¹
Transition Faults linked to Inversion Coupling Faults	Yes ¹
Linked Idempotent Coupling Faults	Yes ¹
Linked Dynamic Coupling Faults	Yes ¹
Parametric Faults	Yes
Write Recovery Faults	Yes
Read Disturb Faults	Yes
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

¹. Only coupling faults occurring in the same column are detected.

Specification

The following specifications apply to the LVGalColumn algorithm:

- To use the LVGalColumn algorithm for the default algorithm, specify LVGalColumn for the **HardCodedAlgorithm** property of the ETVerify configuration file.
- To download the LVGalColumn algorithm to the controller, specify LVGalColumn for the **SelectLibraryAlgorithm** property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVGalColumn algorithm:

- Operations named Write, Read, ReadModifyWrite must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The **MemBistControllerOptions: NumberOfInstructions** property of the *.etplan* file must be greater than or equal to three.
- If the **EnableAEqualsBCommand** property is set to *No* in the *.etplan* file, the LVGalColumn algorithm is not available.

Related Information

[Notation Describing Memory BIST Algorithms](#)

[EnableAEqualsBCommand](#)

LVGalRow Algorithm

The LVGalRow algorithm is only applicable to **Programmable** controllers.

The LVGalRow algorithm is a test algorithm that is available for loading into the memory controller to perform a galloping row algorithm. The galrow algorithm is performed as follows:

1. Write background of D-data from address minimum to address maximum for a single bank.
2. Write \bar{D} -data to the “home” cell addressed by AddressRegister(A).
3. Read D-data from all “away” cells in the same row (same X address) of the same bank addressed by AddressRegister(B). Following each read of the “away” cell read \bar{D} -data from the “home” cell.
4. Write D-data at the “home” cell to restore the data background.
5. Increment the “home” cell addressed by AddressRegister(A) and re-execute steps 2 to 5 until every cell in the bank has been a “home” cell.
6. Increment the bank address from minimum to maximum and re-execute steps 1 to 6.
7. Repeat steps 1.) to 6.) with inverted data.

Test Length

$$2 (3N_{xy} + 2N_y (N_{xy})) N_z$$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$$Z \quad Y1 \Leftarrow X1$$

where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed and a carry out from the X1 address segment is generated. An X1CarryOut is generated when:
 - The X1 address segment is incrementing and has reached the maximum OR.
 - The X1 address segment is decrementing and has reached the minimum.

- The bank address segment Z counts when instructed.

AddressRegister(B)

The AddressRegister(B) segments are configured to count each of the segments individually where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed.
- The bank address segment Z counts when instructed.

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

The logical data pattern applied is inverted with each column. That is the logical data pattern applied is D for even columns and \bar{D} for odd columns.

Algorithm Sequence

Table A-32 describes the LVGalRow algorithm sequence.

Table A-32. Description of LVGalRow Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast row	W_D	Write	Write background of D-data.
1	1	-	-	-	$W_{\bar{D}}$	Write	Write \bar{D} -data to location addressed by AddressRegister(A).

Table A-32. Description of LVGalRow Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
2	2	-	-	-	$R_{\bar{D}}$	<i>Read</i>	Read \bar{D} -data to location addressed by AddressRegister(A).
	3	-	-	Address Register(B) column address min to max	R_D	<i>Read</i>	Read D-data from all column addresses in the same row using AddressRegister(B). When AddressRegister(B) is equivalent to AddressRegister(A) the read \bar{D} -data is expected. Branch back to Instruction 2 and repeat for all AddressRegister(B) column addresses.
	4	-	-	-	-	<i>NoOperation</i>	Advance the row address by one.
	5	-	-	Address Register(A) min to max, fast row	$R_{\bar{D}}W_D$	<i>ReadModifyWrite</i>	Read \bar{D} -data and write D-data at the location addressed by AddressRegister(A). Branch back to Instruction 2 and repeat for all AddressRegister(A) row and column addresses.
3	6	-	-	min to max, bank addresses	-	<i>NoOperation</i>	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed branch to instruction 0 and repeat one time as follows with RepeatLoop(B): Repeat #1 - repeat instructions with inverted write data sequencing and expect data sequencing.

Table A-32. Description of LVGalRow Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
4	0	-	Repeat #1	min to max, fast row	W _D	Write	Write background of D-data.
5	1	-	Repeat #1	-	W _{D̄}	Write	Write \bar{D} -data to location addressed by AddressRegister(A).
6	2	-	Repeat #1	-	R _{D̄}	Read	Read \bar{D} -data to location addressed by AddressRegister(A).
	3	-	Repeat #1	Address Register(B) column address min to max	R _D	Read	Read D-data from all column addresses in the same row using AddressRegister(B). When AddressRegister(B) is equivalent to AddressRegister(A) the read \bar{D} -data is expected. Branch back to Instruction 2 and repeat for all AddressRegister(B) column addresses.
	4	-	Repeat #1	-	-	NoOperation	Advance the row address by one.
	5	-	Repeat #1	Address Register(A) min to max, fast row	R _{D̄} W _D	ReadModifyWrite	Read \bar{D} -data and write D-data at the location addressed by AddressRegister(A). Branch back to Instruction 2 and repeat for all AddressRegister(A) row and column addresses.
7	6	-	Repeat #1	min to max, bank addresses	-	NoOperation	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed repeat phase 0 and 1 with inverted write and expect data.

Example Algorithm Wrapper

Figure A-9 illustrates the **Algorithm** wrapper for the example memory.

Figure A-9. LVGALRow Example Algorithm Wrapper

```
Algorithm (LVGALRow) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b0000000;
                NumberY0Bits : 0;
                NumberX0Bits : 0;
                ZCarryIn : None;
                Y1CarryIn : X1CarryOut;
                X1CarryIn : None;
            }
            AddressRegister (B) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b0000000;
                NumberY0Bits : 0;
                NumberX0Bits : 0;
                ZCarryIn : none;
                Y1CarryIn : none;
                X1CarryIn : none;
            }
        }
        DataGenerator {
            LoadWriteData : 8'b00000000;
            LoadExpectData : 8'b00000000;
        }
    }
    MicroProgram {
        Instruction (WRITE_BACKGROUND) {
            OperationSelect : Write;
            AddressSelectCmd : Select_A;
            X1AddressCmd : Increment;
            Y1AddressCmd : Increment;
            WriteDataCmd : DataReg;
            NextConditions {
                X1_EndCount : On;
                Y1_EndCount : On;
            }
        }
        Instruction (WRITE_HOME_CELL) {
            OperationSelect : Write;
            AddressSelectCmd : Select_A;
            WriteDataCmd : InverseDataReg;
            NextConditions {
            }
        }
        Instruction (READ_HOME_CELL) {
            OperationSelect : Read;
```


Fault Coverage

Table A-33 identifies the faults detected by the LVGalRow algorithm.

Table A-33. LVGalRow Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes
Transition Faults	Yes
Address Decoder Faults	Some
Data Retention Faults	No
Inversion Coupling Faults	Yes ¹
Idempotent Coupling Faults	Yes ¹
Dynamic Coupling Faults	Yes ¹
Transition Faults linked to Inversion Coupling Faults	Yes ¹
Linked Idempotent Coupling Faults	Yes ¹
Linked Dynamic Coupling Faults	Yes ¹
Parametric Faults	Yes
Write Recovery Faults	Yes
Read Disturb Faults	Yes
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

¹. Only coupling faults occurring in the same row are detected.

Specification

The following specifications apply to the LVGalRow algorithm:

- To use the LVGalRow algorithm for the default algorithm, specify LVGalRow for the **HardCodedAlgorithm** property of the ETVerify configuration file.
- To download the LVGalRow algorithm to the controller, specify LVGalRow for the **SelectLibraryAlgorithm** property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVGalRow algorithm:

- Operations named Write, Read, ReadModifyWrite must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The **MemBistControllerOptions: NumberOfInstructions** property of the *.etplan* file must be greater than or equal to three.
- If the **EnableAEqualsBCommand** property is set to *No* in the *.etplan* file, the LVGalRow algorithm is not available.

Related Information

[Notation Describing Memory BIST Algorithms](#)

[EnableAEqualsBCommand](#)

LVCheckerboard1X1 Algorithm

The LVCheckerboard1X1 algorithm is only applicable to **Programmable** controllers.

The LVCheckerboard1X1 algorithm is a test algorithm that is available for loading into the memory controller to perform a 1X1 Checkerboard algorithm. The checkerboard 1x1 algorithm is described in [Table A-34](#).

Test Length

$2(2N_{xyz})$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$$Z \quad X1 \Leftarrow Y1$$

where:

- The column address segment Y1 counts when instructed.
- The row address segment X1 counts when instructed and a carry out from the Y1 address segment is generated. An Y1CarryOut is generated when:
 - The Y1 address segment is incrementing and has reached the maximum OR.
 - The Y1 address segment is decrementing and has reached the minimum.
- The bank address segment Z counts when instructed.

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

The logical data pattern applied is inverted with each column and with each row. That is the logical data pattern applied is:

- D when column address bit 0 = 1'b0 and row address bit 0 = 1'b0
- \bar{D} when column address bit 0 = 1'b1 and row address bit 0 = 1'b0
- \bar{D} when column address bit 0 = 1'b0 and row address bit 0 = 1'b1
- D when column address bit 0 = 1'b1 and row address bit 0 = 1'b1

Algorithm Sequence

[Table A-34](#) describes the LVCheckerboard1X1 algorithm sequence.

Table A-34. Description of LVCheckerboard1X1 Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast row	W _D	Write	Write 1X1 checkerboard D-data background.
1	1	-	-	min to max, fast row	R _D	Read	Read 1x1 checkerboard D-data.
2	5	-	-	min to max, bank addresses	-	<i>NoOperation</i>	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed branch to instruction 0 and repeat one time as follows with RepeatLoop(B): Repeat #1 - repeat instructions with inverted write data sequencing and expect data sequencing.
3	0	Repeat #1	-	min to max, fast row	W _{D̄}	Write	Write 1X1 checkerboard \bar{D} -data background.
4	1	Repeat #1	-	min to max, fast row	R _{D̄}	Read	Read 1x1 checkerboard \bar{D} -data.
5	5	Repeat #1	-	min to max, bank addresses	-	<i>NoOperation</i>	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses.

Example Algorithm Wrapper

Figure A-10 illustrates the **Algorithm** wrapper for the example memory.

Figure A-10. LVCheckerboard1X1 Example Algorithm Wrapper

```
Algorithm (LVCheckerboard1X1) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;
```

```

LoadRowAddress : 4'b0000;
LoadColumnAddress : 6'b0000000;
NumberY0Bits : 0;
NumberX0Bits : 0;
ZCarryIn : none;
X1CarryIn : Y1CarryOut;
Y1CarryIn : none;
}
}

DataGenerator {
    InvertDataWithRowBit : r[0];
    InvertDataWithColumnBit : c[0];
    LoadWriteData : 8'b00000000;
    LoadExpectData : 8'b00000000;
}
}

MicroProgram {
    Instruction (W_1X1_CHECKERBOARD) {
        OperationSelect : Write;
        AddressSelectCmd : Select_A;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        WriteDataCmd : Zero;
        NextConditions {
            X1_EndCount : On;
            Y1_EndCount : On;
        }
    }

    Instruction (R_1X1_CHECKERBOARD) {
        OperationSelect : Read;
        AddressSelectCmd : Select_A;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        ExpectDataCmd : Zero;
        NextConditions {
            X1_EndCount : On;
            Y1_EndCount : On;
        }
    }

    Instruction (GOTO_NEXT_BANKADDRESS) {
        OperationSelect : Nooperation;
        AddressSelectCmd : Select_A;
        ZAddressCmd : Increment;
        BranchToInstruction :
            W_1X1_CHECKERBOARD;
        NextConditions {
            Z_EndCount : On;
            RepeatLoop (A) {
                BranchToInstruction:
                    W_1X1_CHECKERBOARD;
                Repeat {
                    WriteDataSequence: Inverse;
                    ExpectDataSequence: Inverse;
                }
            }
        }
    }
}
}

```

}

Fault Coverage

Table A-35 identifies the faults detected by the LVCheckerboard1X1 algorithm.

Table A-35. LVCheckerboard1X1 Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes ¹
Transition Faults	No
Address Decoder Faults	No
Data Retention Faults	No
Inversion Coupling Faults	No
Idempotent Coupling Faults	No
Dynamic Coupling Faults	No
Transition Faults linked to Inversion Coupling Faults	No
Linked Idempotent Coupling Faults	No
Linked Dynamic Coupling Faults	No
Parametric Faults	No
Write Recovery Faults	No
Read Disturb Faults	No
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

¹. Stuck-At faults are detected correctly when there are no address decoder faults.

Specification

The following specifications apply to the LVCheckerboard1X1 algorithm:

- To use the LVCheckerboard1X1 algorithm for the default algorithm, specify LVCheckerboard1X1 for the **HardCodedAlgorithm** property of the ETVerify configuration file.
- To download the LVCheckerboard1X1 algorithm to the controller, specify LVCheckerboard1X1 for the **SelectLibraryAlgorithm** property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVCheckerboard1X1 algorithm:

- Operations named Write, ReadModifyWrite, and Read must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The **MemBistControllerOptions: NumberOfInstructions** property of the *.etplan* file must be greater than or equal to three.

Related Information

[Notation Describing Memory BIST Algorithms](#)

LVCheckerboard4X4 Algorithm

The LVCheckerboard4X4 algorithm is only applicable to **Programmable** controllers.

The LVCheckerboard4X4 algorithm is a test algorithm that is available for loading into the memory controller to perform a 4X4 Checkerboard algorithm. The checkerboard 4x4 algorithm is described in [Table A-36](#).

Test Length

$2(2N_{xyz})$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$$Z \quad X1 \Leftarrow Y1$$

where:

- The column address segment Y1 counts when instructed.
- The row address segment X1 counts when instructed and a carry out from the Y1 address segment is generated. An Y1CarryOut is generated when:
 - The Y1 address segment is incrementing and has reached the maximum OR.
 - The Y1 address segment is decrementing and has reached the minimum.
- The bank address segment Z counts when instructed.

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

The logical data pattern applied is inverted after every two columns and every two row. That is the logical data pattern applied is:

- D when column address bit 1 = 1'b0 and row address bit 1 = 1'b0
- \overline{D} when column address bit 1 = 1'b1 and row address bit 1 = 1'b0
- \overline{D} when column address bit 1 = 1'b0 and row address bit 1 = 1'b1
- D when column address bit 1 = 1'b1 and row address bit 1 = 1'b1

Algorithm Sequence

[Table A-36](#) describes the LVCheckerboard4X4 algorithm sequence.

Table A-36. Description of LVCheckerboard4X4 Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast row	W _D	Write	Write 4X4 checkerboard D-data background.
1	1	-	-	min to max, fast row	R _D	Read	Read 4X4 checkerboard D-data.
2	5	-	-	min to max, bank addresses	-	<i>NoOperation</i>	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed branch to instruction 0 and repeat one time as follows with RepeatLoop(B): Repeat #1 - repeat instructions with inverted write data sequencing and expect data sequencing.
3	0	Repeat #1	-	min to max, fast row	W _{D̄}	Write	Write 4X4 checkerboard D̄-data background.
4	1	Repeat #1	-	min to max, fast row	R _{D̄}	Read	Read 4X4 checkerboard D̄-data.
5	5	Repeat #1	-	min to max, bank addresses	-	<i>NoOperation</i>	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses.

Example Algorithm Wrapper

Figure A-11 illustrates the **Algorithm** wrapper for the example memory.

Figure A-11. LVCheckerboard4X4 Example Algorithm Wrapper

```

Algorithm (LVCheckerboard4X4) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {

```

```

        LoadBankAddress : 2'b00;
        LoadRowAddress : 4'b0000;
        LoadColumnAddress : 6'b0000000;
        NumberY0Bits : 0;
        NumberX0Bits : 0;
        ZCarryIn : None;
        X1CarryIn : Y1CarryOut;
        Y1CarryIn : None;
    }
}
DataGenerator {
    InvertDataWithRowBit : r[1];
    InvertDataWithColumnBit : c[1];
    LoadWriteData : 8'b00000000;
    LoadExpectData : 8'b00000000;
}
}
MicroProgram {
    Instruction (W_4X4_CHECKERBOARD) {
        OperationSelect : Write;
        AddressSelectCmd : Select_A;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        WriteDataCmd : Zero;
        NextConditions {
            X1_EndCount : On;
            Y1_EndCount : On;
        }
    }
    Instruction (R_4X4_CHECKERBOARD) {
        OperationSelect : Read;
        AddressSelectCmd : Select_A;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        ExpectDataCmd : Zero;
        NextConditions {
            X1_EndCount : On;
            Y1_EndCount : On;
        }
    }
    Instruction (GOTO_NEXT_BANKADDRESS) {
        OperationSelect : Nooperation;
        AddressSelectCmd : Select_A;
        ZAddressCmd : Increment;
        BranchToInstruction :
            W_4X4_CHECKERBOARD;
        NextConditions {
            Z_EndCount : On;
            RepeatLoop (A) {
                BranchToInstruction:
                    W_4X4_CHECKERBOARD;
                Repeat {
                    WriteDataSequence: Inverse;
                    ExpectDataSequence: Inverse;
                }
            }
        }
    }
}

```

}

Fault Coverage

[Table A-37](#) identifies the faults detected by the LVCheckerboard4X4 algorithm.

Table A-37. LVCheckerboard4X4 Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes ¹
Transition Faults	No
Address Decoder Faults	No
Data Retention Faults	No
Inversion Coupling Faults	No
Idempotent Coupling Faults	No
Dynamic Coupling Faults	No
Transition Faults linked to Inversion Coupling Faults	No
Linked Idempotent Coupling Faults	No
Linked Dynamic Coupling Faults	No
Parametric Faults	No
Write Recovery Faults	No
Read Disturb Faults	No
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

1. Stuck-At faults are detected correctly when there are no address decoder faults.

Specification

The following specifications apply to the LVCheckerboard4X4 algorithm:

- To use the LVCheckerboard4X4 algorithm for the default algorithm, specify LVCheckerboard4X4 for the **HardCodedAlgorithm** property of the ETVerify configuration file.
 - To download the LVCheckerboard4X4 algorithm to the controller, specify LVCheckerboard4X4 for the **SelectLibraryAlgorithm** property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVCheckerboard4X4 algorithm:

- Operations named Write, ReadModifyWrite, and Read must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The **MemBistControllerOptions: NumberOfInstructions** property of the *.etplan* file must be greater than or equal to three.
- If the **InvertDataWithAddressBitRange** property is set to *0* in the *.etplan* file, the LVCheckerboard4X4 algorithm is not available.

Related Information

[Notation Describing Memory BIST Algorithms](#)

[InvertDataWithAddressBitRange](#)

LVWalkingPat Algorithm

The LVWalkingPat algorithm is only applicable to **Programmable** controllers.

The LVWalkingPat algorithm is a test algorithm that is available for loading into the memory controller to perform a walking pattern algorithm. The LVWalkingPat algorithm is described in [Table A-38](#).

Test Length

$$2*(N_{xy}^2 + 4N_{xy}) N_z$$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$$Z \quad Y1 \Leftarrow X1$$

where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed and a carry out from the X1 address segment is generated. An X1CarryOut is generated when:
 - The X1 address segment is incrementing and has reached the maximum OR.
 - The X1 address segment is decrementing and has reached the minimum.
- The bank address segment Z counts when instructed.

AddressRegister(B)

The AddressRegister(B) segments are configured to identical to AddressRegister(A).

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

Algorithm Sequence

[Table A-38](#) describes the LVWalkingPat algorithm sequence.

Table A-38. Description of LVWalkingPat Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast row	W _D	Write	Write background of D-data.
1	1	-	-	-	W _{D̄}	Write	Write \bar{D} -data to location addressed by AddressRegister(A).
	2	-	-	Address Register (B) min to max, fast row	R _D	Read	Read D-data from the location addressed by AddressRegister(B). Read \bar{D} -data when AddressRegister(B) equal AddressRegister(A).
	3	-	-	Address Register (B) min to max, fast row	R _{D̄} W _D	ReadModifyWrite	Read \bar{D} -data and Write D-data to the location addressed by AddressRegister(A). Branch back to Instruction 1 and repeat for all AddressRegister(A) row and column addresses.
2	4	-	-	min to max, bank addresses	-	NoOperation	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed branch to instruction 0 and repeat one time as follows with RepeatLoop(B): Repeat #1 - repeat instructions with inverted write data sequencing and expect data sequencing.
3	0	-	Repeat #1	min to max, fast row	W _{D̄}	Write	Write background of \bar{D} -data.

Table A-38. Description of LVWalkingPat Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
4	1	-	Repeat #1	-	W_D	Write	Write D-data to location addressed by AddressRegister(A).
	2	-	Repeat #1	Address Register (B) min to max, fast row	$R_{\bar{D}}$	Read	Read \bar{D} -data from the location addressed by AddressRegister(B). Read D-data when AddressRegister(B) equal AddressRegister(A).
	3	-	Repeat #1	Address Register (B) min to max, fast row	$R_D W_{\bar{D}}$	<i>ReadModifyWrite</i>	Read D-data and Write \bar{D} -data to the location addressed by AddressRegister(A). Branch back to Instruction 1 for all AddressRegister(A) row and column addresses.
5	4	-	Repeat #1	min to max, bank addresses	-	NoOperation	Increment the Bank Address counting from min to max. Branch back to Instruction 0 and repeat the test for all bank addresses. After all bank addresses have been accessed repeat phase 0,1, and 2 with inverted write and expect data.

Example Algorithm Wrapper

Figure A-12 illustrates the **Algorithm** wrapper for the example memory.

Figure A-12. LVWalkingPat Example Algorithm Wrapper.

```

Algorithm (LVWalkingPat) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b000000;
                NumberY0Bits : 0;
                NumberX0Bits : 0;
                ZCarryIn : None;
                Y1CarryIn : X1CarryOut;
                X1CarryIn : None;
            }
        }
    }
}

```

```

        }
    AddressRegister (B) {
        LoadBankAddress : 2'b00;
        LoadRowAddress : 4'b0000;
        LoadColumnAddress : 6'b0000000;
        NumberY0Bits : 0;
        NumberX0Bits : 0;
        ZCarryIn : None;
        Y1CarryIn : X1CarryOut;
        X1CarryIn : none;
    }
}
DataGenerator {
    LoadWriteData : 8'b00000000;
    LoadExpectData : 8'b00000000;
}
}
MicroProgram {
    Instruction (WRITE_BACKGROUND) {
        OperationSelect : Write;
        AddressSelectCmd : Select_A;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        WriteDataCmd : DataReg;
        NextConditions {
            X1_EndCount : On;
            Y1_EndCount : On;
        }
    }
    Instruction (WRITE_HOME_CELL) {
        OperationSelect : Write;
        AddressSelectCmd : Select_A;
        WriteDataCmd : InverseDataReg;
        NextConditions {
        }
    }
    Instruction (READ_AWAY_CELL) {
        OperationSelect : Read;
        AddressSelectCmd : Select_B;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        ExpectDataCmd : DataReg;
        Add_reg_a_equals_b : Invert_ExpectData;
        NextConditions {
            X1_EndCount : On;
            Y1_EndCount : On;
        }
    }
    Instruction (REWRITE_HOME_CELL_AND_ADVANCE)
    {
        OperationSelect : ReadModifyWrite;
        AddressSelectCmd : Select_A;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        WriteDataCmd : DataReg;
        ExpectDataCmd : InverseDataReg;
        BranchToInstruction : WRITE_HOME_CELL;
        NextConditions {
    }
}

```

Fault Coverage

Table A-39 identifies the faults detected by the LVWalkingPat algorithm.

Table A-39. LVWalkingPat Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes
Transition Faults	Yes
Address Decoder Faults	No
Data Retention Faults	No
Inversion Coupling Faults	No
Idempotent Coupling Faults	No
Dynamic Coupling Faults	No
Transition Faults linked to Inversion Coupling Faults	No
Linked Idempotent Coupling Faults	No
Linked Dynamic Coupling Faults	No
Parametric Faults	Yes
Write Recovery Faults	Yes
Read Disturb Faults	Yes

Table A-39. LVWalkingPat Algorithm Fault Coverage (cont.)

Fault Type	Fault Coverage
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	No

Specification

The following specifications apply to the LVWalkingPat algorithm:

- To use the LVWalkingPat algorithm for the default algorithm, specify LVWalkingPat for the **HardCodedAlgorithm** property of the ETVerify configuration file.
- To download the LVWalkingPat algorithm to the controller, specify LVWalkingPat for the **SelectLibraryAlgorithm** property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVWalkingPat algorithm:

- Operations named Write, Read, ReadModifyWrite must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The **MemBistControllerOptions: NumberOfInstructions** property of the .etplan file must be greater than or equal to three.
- If the **EnableAEqualsBCommand** property is set to *No* in the .etplan file, the LVWalkingPat algorithm is not available.

Related Information

[Notation Describing Memory BIST Algorithms](#)

EnableAEqualsBCommand

LVBitSurroundDisturb Algorithm

The LVBitSurroundDisturb algorithm is only applicable to **Programmable** controllers.

The LVBitSurroundDisturb algorithm is a test algorithm that is available for loading into the memory controller to perform a bit surround disturb algorithm. The LVBitSurroundDisturb algorithm is described in [Table A-40](#).

Test Length

$66 N_{xyz}$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to sequence the address counting with fast rows as follows:

$$Z \quad Y1 \Leftarrow X1$$

where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed and a carry out from the X1 address segment is generated. An X1CarryOut is generated when:
 - The X1 address segment is incrementing and has reached the maximum OR.
 - The X1 address segment is decrementing and has reached the minimum.
- The bank address segment Z counts when instructed.
- Initial value of a AddressRegister(A) is Z = 0, Y = 0, X = 0.

AddressRegister(B)

The AddressRegister(B) segments are configured to independently count each address segment as follows:

$$Z \quad X1 \quad Y1$$

where:

- The row address segment X1 counts when instructed.
- The column address segment Y1 counts when instructed.
- The bank address segment Z counts when instructed.
- Initial value of a AddressRegister(B) is Z = 0, Y = 0, X = 0.

DataRegister

The logical data pattern D is loaded into both the write and expect data registers and is a word of all zeroes.

CounterA EndCount Register

The Counter A EndCount register is loaded with the binary equivalent to the decimal value ‘1’.

Algorithm Sequence

Table A-40 describes the LVBitSurroundDisturb algorithm sequence.

Table A-40. Description of LVBitSurroundDisturb Algorithm

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
0	0	-	-	min to max, fast row	W _D	Write	Write background of D-data.
1	1	-	-	-	-	NoOperation	Offset AddressRegister(B) by decrementing one Row Address and decrementing one Column Address.

Table A-40. Description of LVBitSurroundDisturb Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
2	2	-	-	Address Register (B), increment column address	$W_{\bar{D}}$	Write	Write \bar{D} -data at the location addressed by AddressRegister(B). Increment AddressRegister(B) column address by one.
	3	-	-	Address Register (A)	R_D	Read	Read D-data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice).
	4	-	-	Address Register (B), increment row address	$W_{\bar{D}}$	Write	Write \bar{D} -data at the location addressed by AddressRegister(B). Increment AddressRegister(B) row address by one.
	5	-	-	Address Register (A)	R_D	<i>Read</i>	Read D-data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice). Repeat instructions 2-5 three times as follows with RepeatLoop(B): Repeat #1 - branch to instruction 2 and repeat instructions with inverted the address sequencing Repeat #2 - branch to instruction 2 and repeat instructions with inverted the write data sequencing. Repeat #3 -branch to instruction 2 and repeat instructions with inverted the address and write data sequencing.

Table A-40. Description of LVBitSurroundDisturb Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
3	2	-	Re-pete #1	Address Register (B), decrement column address	$W_{\bar{D}}$	Write	Write \bar{D} -data at the location addressed by AddressRegister(B). Decrement AddressRegister(B) column address by one.
	3	-	Re-pete #1	Address Register (A)	R_D	Read	Read D-data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice).
	4	-	Re-pete #1	Address Register (B), decrement row address	$W_{\bar{D}}$	Write	Write \bar{D} -data at the location addressed by AddressRegister(B). Decrement AddressRegister(B) row address by one.
	5	-	Re-pete #1	Address Register (A)	R_D	<i>Read</i>	Read D-data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counter counts from zero to CounterA endcount(twice). Repeat instructions 2-5 three times as follows with RepeatLoop(B): Repeat #1 - branch to instruction 2 and repeat instructions with inverted the address sequencing Repeat #2 - branch to instruction 2 and repeat instructions with inverted the write data sequencing. Repeat #3 -branch to instruction 2 and repeat instructions with inverted the address and write data sequencing.

Table A-40. Description of LVBitSurroundDisturb Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
4	2	-	Re-pete #2	Address Register (B), increment column address	W _D	Write	Write D-data at the location addressed by AddressRegister(B). Increment AddressRegister(B) column address by one.
	3	-	Re-pete #2	Address Register (A)	R _D	Read	Read D-data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice).
	4	-	Re-pete #2	Address Register (B), increment row address	W _D	Write	Write D-data at the location addressed by AddressRegister(B). Increment AddressRegister(B) row address by one.
	5	-	Re-pete #2	Address Register (A)	R _D	<i>Read</i>	Read D-data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice). Repeat instructions 2-5 three times as follows with RepeatLoop(B): Repeat #1 - branch to instruction 2 and repeat instructions with inverted the address sequencing Repeat #2 - branch to instruction 2 and repeat instructions with inverted the write data sequencing. Repeat #3 -branch to instruction 2 and repeat instructions with inverted the address and write data sequencing.

Table A-40. Description of LVBitSurroundDisturb Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
5	2	-	Re-peteat #3	Address Register (B), decrement the column address	W _D	Write	Write D-data at the location addressed by AddressRegister(B). Decrement AddressRegister(B) column address by one.
	3	-	Re-peteat #3	Address Register (A)	R _D	Read	Read D-data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice).
	4	-	Re-peteat #3	Address Register (B), decrement the row address	W _D	Write	Write D-data at the location addressed by AddressRegister(B). Decrement AddressRegister(B) row address by one.
	5	-	Re-peteat #3	Address Register (A)	R _D	<i>Read</i>	Read D-data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice). Repeat instructions 2-5 three times as follows with RepeatLoop(B): Repeat #1 - branch to instruction 2 and repeat instructions with inverted the address sequencing Repeat #2 - branch to instruction 2 and repeat instructions with inverted the write data sequencing. Repeat #3 -branch to instruction 2 and repeat instructions with inverted the address and write data sequencing.

Table A-40. Description of LVBitSurroundDisturb Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
6	6	-	-	Address Register (A), increment min to max, fast rows	-	<i>NoOperation</i>	Increment AddressRegister(A) and copy the result to AddressRegister(B). Branch back to Instruction 1 and re-execute phases 1 through 5 for all AddressRegister(A) row and column addresses.
7	7	-	-	Address Register (A), bank addresses, min to max	-	<i>NoOperation</i>	Increment the bank address for AddressRegister(A) and copy the result to AddressRegister(B). Branch back to Instruction 0 and re-execute phases 1 through 7 for all bank addresses. Repeat instructions 0-7 once as follows with RepeatLoop(A): Repeat #1 - branch to instruction 0 and repeat instructions with inverted the write and expect data sequencing
0	0	Re-repeat #1	-	min to max, fast row	$W_{\bar{D}}$	<i>Write</i>	Write background of \bar{D} -data.
1	1	Re-repeat #1	-	-	-	NoOperation	Offset AddressRegister(B) by decrementing one Row Address and decrementing one Column Address.

Table A-40. Description of LVBitSurroundDisturb Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
2	2	Re-peat #1	-	Address Register (B), increment column address	W _D	Write	Write D-data at the location addressed by AddressRegister(B). Increment AddressRegister(B) column address by one.
	3	Re-peat #1	-	Address Register (A)	R _{D̄}	Read	Read \bar{D} -data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice).
	4	Re-peat #1	-	Address Register (B), increment row address	W _D	Write	Write D-data at the location addressed by AddressRegister(B). Increment AddressRegister(B) row address by one.
	5	Re-peat #1	-	Address Register (A)	R _{D̄}	<i>Read</i>	Read \bar{D} -data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice). Repeat instructions 2-5 three times as follows with RepeatLoop(B): Repeat #1 - branch to instruction 2 and repeat instructions with inverted the address sequencing Repeat #2 - branch to instruction 2 and repeat instructions with inverted the write data sequencing. Repeat #3 -branch to instruction 2 and repeat instructions with inverted the address and write data sequencing.

Table A-40. Description of LVBitSurroundDisturb Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
3	2	Re-peat #1	Re-peat #1	Address Register (B), decrement column address	W _D	Write	Write D-data at the location addressed by AddressRegister(B). Decrement AddressRegister(B) column address by one.
	3	Re-peat #1	Re-peat #1	Address Register (A)	R _{D̄}	Read	Read \bar{D} -data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to counterA endcount(twice).
	4	Re-peat #1	Re-peat #1	Address Register (B), decrement row address	W _D	Write	Write D-data at the location addressed by AddressRegister(B). Decrement AddressRegister(B) row address by one.
	5	Re-peat #1	Re-peat #1	Address Register (A)	R _{D̄}	<i>Read</i>	Read \bar{D} -data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice). Repeat instructions 2-5 three times as follows with RepeatLoop(B): Repeat #1 - branch to instruction 2 and repeat instructions with inverted the address sequencing Repeat #2 - branch to instruction 2 and repeat instructions with inverted the write data sequencing. Repeat #3 -branch to instruction 2 and repeat instructions with inverted the address and write data sequencing.

Table A-40. Description of LVBitSurroundDisturb Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
4	2	Re-peat #1	Re-peat #2	Address Register (B), increment column address	$W_{\bar{D}}$	Write	Write \bar{D} -data at the location addressed by AddressRegister(B). Increment AddressRegister(B) column address by one.
	3	Re-peat #1	Re-peat #2	Address Register (A)	$R_{\bar{D}}$	Read	Read \bar{D} -data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice).
	4	Re-peat #1	Re-peat #2	Address Register (B), increment row address	$W_{\bar{D}}$	Write	Write \bar{D} -data at the location addressed by AddressRegister(B). Increment AddressRegister(B) row address by one.
	5	Re-peat #1	Re-peat #2	Address Register (A)	$R_{\bar{D}}$	<i>Read</i>	Read \bar{D} -data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice). Repeat instructions 2-5 three times as follows with RepeatLoop(B): Repeat #1 - branch to instruction 2 and repeat instructions with inverted the address sequencing Repeat #2 - branch to instruction 2 and repeat instructions with inverted the write data sequencing. Repeat #3 -branch to instruction 2 and repeat instructions with inverted the address and write data sequencing.

Table A-40. Description of LVBitSurroundDisturb Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
5	2	Re-peat #1	Re-peat #3	Address Register (B), decrement column address	$W_{\bar{D}}$	Write	Write \bar{D} -data at the location addressed by AddressRegister (B). Decrement AddressRegister(B) column address by one.
	3	Re-peat #1	Re-peat #3	Address Register (A)	$R_{\bar{D}}$	Read	Read \bar{D} -data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice).
	4	Re-peat #1	Re-peat #3	Address Register (B), decrement row address	$W_{\bar{D}}$	Write	Write \bar{D} -data at the location addressed by AddressRegister(B). Decrement AddressRegister(B) row address by one.
	5	Re-peat #1	Re-peat #3	Address Register (A)	$R_{\bar{D}}$	<i>Read</i>	Read \bar{D} -data at the location addressed by AddressRegister(A). Increment CounterA. Branch back to Instruction 2 and repeat until CounterA counts from zero to CounterA endcount(twice). Repeat instructions 2-5 three times as follows with RepeatLoop(B): Repeat #1 - branch to instruction 2 and repeat instructions with inverted the address sequencing Repeat #2 - branch to instruction 2 and repeat instructions with inverted the write data sequencing. Repeat #3 -branch to instruction 2 and repeat instructions with inverted the address and write data sequencing.

Table A-40. Description of LVBitSurroundDisturb Algorithm (cont.)

Phase	Instruction #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
6	6	Re-peat #1	-	Address Register (A), increment min to max, fast rows	-	NoOperation	Increment AddressRegister(A) and copy the result to AddressRegister(B). Branch back to Instruction 1 and re-execute phases 1 through 5 for all AddressRegister(A) row and column addresses.
7	7	Re-peat #1	-	Address Register (A), bank addresses, min to max	-	NoOperation	Increment the bank address for AddressRegister(A) and copy the result to AddressRegister (B). Branch back to Instruction 0 and re-execute phases 1 through 7 for all bank addresses. Repeat instructions 0-7 once as follows with RepeatLoop(A): Repeat #1 - branch to instruction 0 and repeat instructions with inverted the write and expect data sequencing

Example Algorithm Wrapper

Figure A-13 illustrates the **Algorithm** wrapper for the example memory.

Figure A-13. LVBitSurroundDisturb Example Algorithm Wrapper

```

algorithm (LVBitSurroundDisturb) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        LoadCounterA_EndCount : 1;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b000000;
                NumberY0Bits : 0;
                NumberX0Bits : 0;
                ZCarryIn : None;
                Y1CarryIn : X1CarryOut;
                X1CarryIn : None;
            }
            AddressRegister (B) {
                LoadBankAddress : 2'b00;
                LoadRowAddress : 4'b0000;
                LoadColumnAddress : 6'b000000;
            }
        }
    }
}

```

```

        NumberY0Bits : 0;
        NumberX0Bits : 0;
        ZCarryIn : None;
        Y1CarryIn : None;
        X1CarryIn : None;
    }
}
DataGenerator {
    LoadWriteData : 8'b00000000;
    LoadExpectData : 8'b00000000;
}
}
MicroProgram {
    Instruction (WRITE_BACKGROUND) {
        OperationSelect : Write;
        AddressSelectCmd : Select_A;
        X1AddressCmd : Increment;
        Y1AddressCmd : Increment;
        WriteDataCmd : DataReg;
        NextConditions {
            X1_EndCount : On;
            Y1_EndCount : On;
        }
    }
    Instruction (OFFSET_AWAY_CELL) {
        OperationSelect : NoOperation;
        AddressSelectCmd : Select_B;
        X1AddressCmd : Decrement;
        Y1AddressCmd : Decrement;
        NextConditions {
        }
    }
    Instruction (WRITE_AWAY_CELL1) {
        OperationSelect : Write;
        AddressSelectCmd : Select_B;
        Y1AddressCmd : Increment;
        WriteDataCmd : InverseDataReg;
        NextConditions {
        }
    }
    Instruction (READ_HOME_CELL1) {
        OperationSelect : Read;
        CounterACmd : Increment;
        AddressSelectCmd : Select_A;
        ExpectDataCmd : DataReg;
        BranchToInstruction : WRITE_AWAY_CELL1;
        NextConditions {
            CounterAEndCount : On;
        }
    }
    Instruction (WRITE_AWAY_CELL2) {
        OperationSelect : Write;
        AddressSelectCmd : Select_B;
        X1AddressCmd : Increment;
        WriteDataCmd : InverseDataReg;
        NextConditions {
        }
    }
}

```

```
Instruction (READ_HOME_CELL2) {
    OperationSelect : read;
    CounterACmd : Increment;
    AddressSelectCmd : Select_A;
    ExpectDataCmd : DataReg;
    BranchToInstruction : WRITE_AWAY_CELL2;
    NextConditions {
        CounterAEndCount : On;
        RepeatLoop (B) {
            BranchToInstruction :
                WRITE_AWAY_CELL1;
            Repeat {
                AddressSequence : Inverse;
            }
            Repeat {
                WriteDataSequence : Inverse;
            }
            Repeat {
                AddressSequence : Inverse;
                WriteDataSequence : Inverse;
            }
        }
    }
}
Instruction (MOVE_HOME_CELL) {
    OperationSelect : NoOperation;
    AddressSelectCmd : Select_A_Copy_To_B;
    X1AddressCmd : Increment;
    Y1AddressCmd : Increment;
    BranchToInstruction : OFFSET_AWAY_CELL;
    NextConditions {
        X1_EndCount : On;
        Y1_EndCount : On;
    }
}
Instruction (GOTO_NEXT_BANKADDRESS) {
    OperationSelect : NoOperation;
    AddressSelectCmd : Select_A_Copy_to_B;
    ZAddressCmd : Increment;
    BranchToInstruction : WRITE_BACKGROUND;
    NextConditions {
        Z_EndCount : On;
        RepeatLoop (A) {
            BranchToInstruction:
                WRITE_BACKGROUND;
            Repeat {
                WriteDataSequence: Inverse;
                ExpectDataSequence: Inverse;
            }
        }
    }
}
```

Fault Coverage

Table A-41 identifies the faults detected by the LVBitSurroundDisturb algorithm.

Table A-41. LVBitSurroundDisturb Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Faults	Yes
Transition Faults	Yes
Address Decoder Faults	Yes
Data Retention Faults	No
Inversion Coupling Faults	Some
Idempotent Coupling Faults	Some
Dynamic Coupling Faults	No
Transition Faults linked to Inversion Coupling Faults	No
Linked Idempotent Coupling Faults	No
Linked Dynamic Coupling Faults	No
Parametric Faults	Yes
Write Recovery Faults	Yes
Read Disturb Faults	No
Read/Write Logic Faults	Yes
Neighborhood Pattern Sensitive Faults	Some

Specification

The following specifications apply to the LVBitSurroundDisturb algorithm:

- To use the LVBitSurroundDisturb algorithm for the default algorithm, specify LVBitSurroundDisturb for the **HardCodedAlgorithm** property of the ETVerify configuration file.
- To download the LVBitSurroundDisturb algorithm to the controller, specify LVBitSurroundDisturb for the **SelectLibraryAlgorithm** property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVBitSurroundDisturb algorithm:

- Operations named Write, Read, ReadModifyWrite must exist or be mapped to another operation in **OperationSet** of the memory library file.
- The **MemBistControllerOptions: NumberOfInstructions** property of the *.etplan* file must be set to 8 if the Z address bank is defined, otherwise, it should be 7.

Related Information

[Notation Describing Memory BIST Algorithms](#)

LVAddressInterconnect Algorithm

The LVAddressInterconnect algorithm provides coverage of defects that occur on the board-level memory address bus lines: stuck-at, open, delay, and bridging faults. The interconnect algorithm is very fast, typically requiring less than a millisecond. LVAddressInterconnect is performed as follows:

1. Write 0 in low or the base cell.
2. Write 1 to the address where the first address line is logic 1 and the rest is logic zero.
3. Read 0, then write 0 in the base cell.
4. Walk a 1 across the address lines (in a field of zeros) and repeat steps 2 and 3.
5. Walk a 0 across the address lines (in a field of ones) and repeat steps 2 and 3.

Note



Step 5 can be applied only if the memory uses the full address range.

The LVAddressInterconnect algorithm is described in [Table A-42](#).

Test Length

Assuming that the memory has a full address range, the test length of this algorithm is:

$$1 + 6 \log_2 N_{xyz}$$

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to hold the address for the base cell, which is normally the low address.

AddressRegister(B)

The AddressRegister(B) segments are configured to hold the binary value <#of AddressLines'b1>.

CounterA EndCount Register

The Counter A EndCount register is used to count the steps to walk the one or the zero across the address bus and should be loaded with the value equal to <AddressBusWidth> - 1.

Algorithm Sequence

Table A-42 describes the LVAddressInterconnect algorithm sequence.

Table A-42. Description of LVAddressInterconnect Algorithm

Phase	Inst #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
1	0	-	-	Base cell address	W0	Write	Write zero in the base cell.
2	1	-	-	One address line only is set to logic 1	W1	Write	Write one to the address specified.
3	2	-	-	Base cell address	R0W0	ReadModify Write	Read zero from base cell address, then write zero. This operation will pass if there is no stuck-at or stuck-open fault on the address line set to logic 1 in Ins1. Walk the logic 1 across the address lines and repeat from Ins1.
4	3	-	-	Set the address for walk zero	-	NoOperation	Set the AddressRegister for walk logic zero.
5	4	-	-	One address line only set to logic 0.	-	NoOperation	Repeat from Ins2.

Example Algorithm Wrapper

Figure A-14 illustrates the *Algorithm* wrapper for the example memory.

Figure A-14. LVAddressInterconnect Example Algorithm Wrapper

```
Algorithm (LVAddressInterconnect) {
    TestRegisterSetup {
        OperationSetSelect : ReadLatency_RL11;
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 2'b00;
```

```

LoadRowAddress : 3'b000;
LoadColumnAddress : 3'b000;
ZCarryIn : None;
Y1CarryIn : None;
X1CarryIn : None;
}
AddressRegister (B) {
    LoadBankAddress : 2'b00;
    LoadRowAddress : 3'b000;
    LoadColumnAddress : 3'b001;
    ZCarryIn : None;
    Y1CarryIn : None;
    X1CarryIn : None;
}
} //End of AddressGenerator wrapper
LoadCounterA_EndCount : 7;
DataGenerator {
}
} //End of TestRegisterSetup wrapper
MicroProgram {
Instruction (WRITE0_BASE_CELL) {
    OperationSelect : Write;
    AddressSelectCmd : Select_A;
    WriteDataCmd : Zero;
    NextConditions {
    }
}
Instruction (WRITE1_BASE_CELL) {
    OperationSelect : Write;
    AddressSelectCmd : Select_B;
    WriteDataCmd : One;
    NextConditions {
    }
}
Instruction (READ0_WRITE_0_BASE_CELL) {
    OperationSelect : ReadModifyWrite;
    AddressSelectCmd : Select_A_Rotate_B;
    CounterACmd : Increment;
    BranchToInstruction : WRITE0_BASE_CELL;
    NextConditions {
        CounterAEndCount : On;
    }
}
Instruction (SET_ADDRESS_WALK0) {
    OperationSelect : NoOperation;
    AddressSelectCmd : Select_A_Copy_To_B;
    Y1AddressCmd : Decrement;
    X1AddressCmd : Decrement;
    ZAddressCmd : Decrement;
    NextConditions {
    }
}
Instruction (EXECUTE_WALK0) {
    OperationSelect : NoOperation;
    AddressSelectCmd : Select_B;
    Y1AddressCmd : Decrement;
    NextConditions {
        RepeatLoop (A) {

```

```
    BranchToInstruction : WRITE0_BASE_CELL;
    Repeat {
        }
    }
}
} // End of MicroProgram wrapper
} // End of Algorithm (LVAddressInterconnect) wrapper
```

Fault Coverage

Table A-43 identifies the faults detected by the LVAddressInterconnect algorithm.

Table A-43. LVAddressInterconnect Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Fault on a single address line at either a logic 1 or logic 0.	Yes
Stuck-Open Faults on address line. A stuck-open fault is a single data line that contains an open (break).	Yes
Bridging Faults. A bridging fault is two or more address lines shorted together. The short can result in either a Wired-AND (0 dominant) or Wired_OR (1 dominant).	Yes

Specification

The following specifications apply to the LVAddressInterconnect algorithm:

- To use the LVAddressInterconnect algorithm for the default algorithm, specify LVAddressInterconnect for the **HardCodedAlgorithm** property of the ETVerify configuration file.
- To download the LVAddressInterconnect algorithm to the controller, specify LVAddressInterconnect for the **SelectLibraryAlgorithm** property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVAddressInterconnect algorithm:

- A full binary count value for the min and max should be assigned to CountRange(BankAddress), CountRange(RowAddress), and/or CountRange(ColumnAddress) in the memory library file if coverage of the Wired-OR fault model is desired for address-line shorts.
- All the physical address lines cannot be mapped to bank address only. The memory configuration should have at least two logical addresses.

Related Information

[Notation Describing Memory BIST Algorithms](#)

[HardCodedAlgorithm in the *ETVerify Tool Reference*](#)

[Algorithm in the *ETAssemble Tool Reference*](#)

[SelectLibraryAlgorithm in the *ETVerify Tool Reference*](#)

[NumberOfInstructions in the *ETPlanner Tool Reference*](#)

LVDataInterconnect Algorithm

The LVDataInterconnect algorithm provides coverage of defects that occur on the board-level memory data bus lines: stuck-at, open, delay, and bridging faults. The interconnect algorithm is very fast, typically requiring less than a millisecond. LVDataInterconnect is performed as follows:

1. Initialize the minimum and maximum addresses of all memory banks with 0.
2. Apply read 0, write 1, read 1 to every minimum and maximum address of all memory banks, bank addresses ascending.
3. Repeat step 2 with the inversed data.
4. Repeat steps 2 and 3 with bank addresses descending.
5. Walk and write and read a single 1 (in a field of zeros) across the data lines. Repeat for all minimum and maximum addresses of all memory banks, bank addresses ascending.
6. Walk and write and read a single 0 (in a field of ones) across the data lines. Repeat for all minimum and maximum addresses of all memory banks, bank addresses ascending.

The LVDataInterconnect algorithm is described in [Table A-44](#).

Test Length

$$(26 + 8DW)Z$$

where DW is the datapath width of the memory and Z is the number of memory banks.

TestRegisterSetup

The test register setup describes the controller test register values to be initialized for the address and data prior to execution of the algorithm.

AddressRegister(A)

The AddressRegister(A) segments are configured to hold the low address.

AddressRegister(B)

The AddressRegister(B) segments are configured to hold the high address.

DataRegister

The logical data pattern D (<DataBusWidth>'b1) is loaded into both the write and expect data registers.

CounterA Register

The CounterA register is used to count the steps to walk the one or the zero across the data path and should be loaded with the value equal to <DataBusWidth> -1.

Algorithm Sequence

Table A-44 describes the LVDataInterconnect algorithm sequence.

Table A-44. Description of LVDataInterconnect Algorithm

Phase	Inst #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
1	0	-	-	min address for every bank starting from lowest	W0	Write	Write zero.
1	1	-	-	max address for every bank starting from lowest	W0	Write	Write zero.
2	2	-	-	min address for every bank starting from lowest	R0 W1	ReadModify Write	Read zero from low address, then write one to the same address.
2	3	-	-	min address for every bank starting from lowest	R1	Read	Read one from low address.
2	4	-	-	max address for every bank starting from lowest	R0 W1	ReadModify Write	Read zero from high address and write one.

Table A-44. Description of LVDataInterconnect Algorithm (cont.)

Phase	Inst #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
3	5	Repeat from #Ins 2	-	max address for every bank starting from lowest	R1	Read	Read one from the max address for every bank. Repeat from instruction 2 with the inverse of data .
4	6	-	-	max address for every bank starting from highest	R0 W1	ReadModify Write	Read zero from high address, then write one to the same address.
4	7	-	-	max address for every bank starting from highest	R1	Read	Read one from high address.
4	8	-	-	min address for every bank starting from highest	R0 W1	ReadModify Write	Read zero from low address, then write one to the same address.
5	9	-	Repeat from #Ins 6	min address for every bank starting from highest	R1	Read	Read one from low address. Repeat from Ins#6 with the inverse of data .

Table A-44. Description of LVDataInterconnect Algorithm (cont.)

Phase	Inst #	Repeat Loop(A)	Repeat Loop(B)	Address Sequence	Sequence	Operation	Description
6	10	-	-	min address	W_D R_D	WriteRead	Write D-data, then read D-data the low address. Walk the one across the whole data register and repeat the write read operation.
6	11	-	-	max address	W_D R_D	WriteRead	Write D-data, then read D-data to the high address. Walk the one across the whole data bus and repeat the write read operations.
6	12	-	-	Increment the bank address	-	NoOperation	Increment the bank address and repeat from Ins#10.
7	13	-	-	min address	$W_{\bar{D}}$ $R_{\bar{D}}$	WriteRead	Write \bar{D} -data register, then read \bar{D} -data register from the low address. Walk the zero across the whole data bus and repeat the write read operation.
7	14	-	-	max address	$W_{\bar{D}}$ $R_{\bar{D}}$	WriteRead	Write \bar{D} -data register, then read \bar{D} -data register from the high address. Walk the zero across the whole data bus and repeat the write read operation.
7	15	-	-	Increment the bank address	-	NoOperation	Increment the bank address and repeat from Ins#13.

Example Algorithm Wrapper

Figure A-15 illustrates the **Algorithm** wrapper for the example memory.

Figure A-15. LVDataInterconnect Example Algorithm Wrapper

```
Algorithm (LVDATAINTERCONNECT) {
    TestRegisterSetup {
        AddressGenerator {
            AddressRegister (A) {
                LoadBankAddress : 3'b000;
```

```
    LoadRowAddress : 3'b000;
    LoadColumnAddress : 2'b00;
    NumberX0Bits : 0;
    NumberY0Bits : 0;
    ZCarryIn : NONE;
    X1CarryIn : NONE;
    Y1CarryIn : NONE;
}
AddressRegister (B) {
    LoadBankAddress : 3'b000;
    LoadRowAddress : 3'b111;
    LoadColumnAddress : 2'b11;
    NumberX0Bits : 0;
    NumberY0Bits : 0;
    ZCarryIn : NONE;
    X1CarryIn : NONE;
    Y1CarryIn : NONE;
}
} // End of AddressGenerator wrapper
DataGenerator {
    LoadWriteData : 8'b00000001;
    LoadExpectData : 8'b00000001;
}
LoadCounterA_EndCount : 7;
OperationSetSelect : SYNC;
} // End of TestRegisterSetup wrapper
MicroProgram {
    Instruction (PHASE_2_LADDR_WRITE) {
        AddressSelectCmd : Select_A;
        ExpectDataCmd : Zero;
        OperationSelect : WRITE;
        WriteDataCmd : Zero;
        NextConditions {
        }
    }
    Instruction (PHASE_2_HADDR_WRITE) {
        AddressSelectCmd : A_Xor_B;
        BranchToInstruction : PHASE_2_LADDR_WRITE;
        ExpectDataCmd : Zero;
        OperationSelect : WRITE;
        WriteDataCmd : Zero;
        ZAddressCmd : Increment;
        NextConditions {
            Z_EndCount : On;
        }
    }
    Instruction (PHASE_3_4_LADDR_RMW) {
        AddressSelectCmd : Select_A;
        ExpectDataCmd : Zero;
        OperationSelect : READMODIFYWRITE;
        WriteDataCmd : One;
        NextConditions {
        }
    }
    Instruction (PHASE_3_4_LADDR_R) {
        AddressSelectCmd : Select_A;
        ExpectDataCmd : One;
        OperationSelect : READ;
```

```

WriteDataCmd : Zero;
NextConditions {
}
}
Instruction (PHASE_3_4_HADDR_RMW) {
AddressSelectCmd : A_Xor_B;
ExpectDataCmd : Zero;
OperationSelect : READMODIFYWRITE;
WriteDataCmd : One;
NextConditions {
}
}
Instruction (PHASE_3_4_HADDR_R) {
AddressSelectCmd : A_Xor_B;
BranchToInstruction : PHASE_3_4_LADDR_RMW;
ExpectDataCmd : One;
OperationSelect : READ;
WriteDataCmd : Zero;
ZAddressCmd : Increment;
NextConditions {
Z_EndCount : On;
RepeatLoop (A) {
    BranchToInstruction : PHASE_3_4_LADDR_RMW;
    Repeat {
        AddressSequence : NoChange;
        WriteDataSequence : Inverse;
        ExpectDataSequence : Inverse;
        InhibitLastAddressCount : On;
    }
}
}
}
Instruction (PHASE_5_6_HADDR_RMW) {
AddressSelectCmd : A_Xor_B;
ExpectDataCmd : Zero;
OperationSelect : READMODIFYWRITE;
WriteDataCmd : One;
NextConditions {
}
}
Instruction (PHASE_5_6_HADDR_R) {
AddressSelectCmd : A_Xor_B;
ExpectDataCmd : One;
OperationSelect : READ;
WriteDataCmd : Zero;
NextConditions {
}
}
Instruction (PHASE_5_6_LADDR_RMW) {
AddressSelectCmd : Select_A;
ExpectDataCmd : Zero;
OperationSelect : READMODIFYWRITE;
WriteDataCmd : One;
NextConditions {
}
}
Instruction (PHASE_5_6_LADDR_R) {
AddressSelectCmd : Select_A;

```

```
BranchToInstruction : PHASE_5_6_HADDR_RMW;
ExpectDataCmd : One;
OperationSelect : READ;
WriteDataCmd : Zero;
ZAddressCmd : Decrement;
NextConditions {
    Z_EndCount : On;
    RepeatLoop (B) {
        BranchToInstruction : PHASE_5_6_HADDR_RMW;
        Repeat {
            AddressSequence : NoChange;
            WriteDataSequence : Inverse;
            ExpectDataSequence : Inverse;
            InhibitLastAddressCount : On;
        }
    }
}
Instruction (PHASE_7_LADDR_WR) {
    AddressSelectCmd : Select_A;
    CounterACmd : Increment;
    ExpectDataCmd : DataReg_Rotate;
    OperationSelect : WRITEREAD;
    WriteDataCmd : DataReg_Rotate;
    NextConditions {
        CounterAEndCount : On;
    }
}
Instruction (PHASE_7_HADDR_WR) {
    AddressSelectCmd : A_Xor_B;
    CounterACmd : Increment;
    ExpectDataCmd : DataReg_Rotate;
    OperationSelect : WRITEREAD;
    WriteDataCmd : DataReg_Rotate;
    NextConditions {
        CounterAEndCount : On;
    }
}
Instruction (PHASE_7_INC_BANK) {
    AddressSelectCmd : Select_A;
    BranchToInstruction : PHASE_7_LADDR_WR;
    ExpectDataCmd : Zero;
    InhibitDataCompare : On;
    OperationSelect : NOOPERATION;
    WriteDataCmd : Zero;
    ZAddressCmd : Increment;
    NextConditions {
        Z_EndCount : On;
    }
}
Instruction (PHASE_8_LADDR_WR) {
    AddressSelectCmd : Select_A;
    CounterACmd : Increment;
    ExpectDataCmd : InverseDataReg_Rotate;
    OperationSelect : WRITEREAD;
    WriteDataCmd : InverseDataReg_Rotate;
    NextConditions {
        CounterAEndCount : On;
```

```

        }
    }

Instruction (PHASE_8_HADDR_WR) {
    AddressSelectCmd : A_Xor_B;
    CounterACmd : Increment;
    ExpectDataCmd : InverseDataReg_Rotate;
    OperationSelect : WRITEREAD;
    WriteDataCmd : InverseDataReg_Rotate;
    NextConditions {
        CounterAEndCount : On;
    }
}

Instruction (PHASE_8_INC_BANK) {
    AddressSelectCmd : Select_A;
    BranchToInstruction : PHASE_8_LADDR_WR;
    ExpectDataCmd : Zero;
    OperationSelect : NOOPERATION;
    WriteDataCmd : Zero;
    ZAddressCmd : Increment;
    NextConditions {
        Z_EndCount : On;
    }
}

} // End of MicroProgram wrapper
} // End of Algorithm wrapper

```

Fault Coverage

Table A-45 identifies the faults detected by the LVDataInterconnect algorithm.

Table A-45. LVDataInterconnect Algorithm Fault Coverage

Fault Type	Fault Coverage
Stuck-At Fault on a single data line at either a logic 1 or logic 0.	Yes
Stuck-Open Faults on data line. A stuck-open fault is a single data line that contains an open (break).	Yes
Bridging Faults. A bridging fault is two or more data lines shorted together. The short can result in either an ANDing or ORing of the values on the affected lines.	Yes

Specification

The following specifications apply to the LVDataInterconnect algorithm:

- To use the LVDataInterconnect algorithm for the default algorithm, specify LVDataInterconnect for the **HardCodedAlgorithm** property of the ETVerify configuration file.
- To download the LVDataInterconnect algorithm to the controller, specify LVDataInterconnect for the **SelectLibraryAlgorithm** property of the ETVerify configuration file.

Usage Conditions

The following usage conditions apply to the LVDataInterconnect algorithm:

- A binary complement values for the min and max should be assigned to CountRange(BankAddress), CountRange(RowAddress), and/or CountRange(ColumnAddress) in the memory library file if coverage of the Wired-OR fault model is desired for address-line shorts.
- All the physical address lines cannot be mapped to bank address only. The memory configuration should have at least two logical addresses.

Related Information

[Notation Describing Memory BIST Algorithms](#)

[HardCodedAlgorithm in the ETVerify Tool Reference](#)

[Algorithm in the ETAssemble Tool Reference](#)

[SelectLibraryAlgorithm in the ETVerify Tool Reference](#)

[NumberOfInstructions in the ETPlanner Tool Reference](#)

Appendix B

Getting Help

There are several ways to get help when setting up and using Tesson software tools. Depending on your need, help is available from documentation, online command help, and Mentor Graphics Support.

Documentation

The Tesson software tree includes a complete set of documentation and help files in PDF format. Although you can view this documentation with any PDF reader, if you are viewing documentation on a Linux file server, you must use only Adobe® Reader® versions 8 or 9, and you must set one of these versions as the default using the MGC_PDF_READER variable in your *mgc_doc_options.ini* file.

For more information, refer to “[Specifying Documentation System Defaults](#)” in the *Managing Mentor Graphics Tesson Software* manual.

You can download a free copy of the latest Adobe Reader from this location:

<http://get.adobe.com/reader>

You can access the documentation in the following ways:

- **Shell Command** — On Linux platforms, enter **mgcdocs** at the shell prompt or invoke a Tesson tool with the -Manual invocation switch. This option is available only with Tesson Shell and the following classic point tools: Tesson FastScan, Tesson TestKompress, Tesson Diagnosis, and DFTAdvisor.
- **File System** — Access the Tesson bookcase directly from your file system, without invoking a Tesson tool. From your product installation, invoke Adobe Reader on the following file:

\$MGC_DFT/doc/pdfdocs/_bk_tesson.pdf

- **Application Online Help** — You can get contextual online help within most Tesson tools by using the “help -manual” tool command:

> **help dofile -manual**

This command opens the appropriate reference manual at the “dofile” command description.

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<http://supportnet.mentor.com/user/register.cfm>

All customer support contact information is available here:

<http://supportnet.mentor.com/contacts/supportcenters/index.cfm>

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12. **TERMINATION AND EFFECT OF TERMINATION.**
 - 12.1. If a Software license was provided for limited term use, such license will automatically terminate at the end of the authorized term. Mentor Graphics may terminate this Agreement and/or any license granted under this Agreement immediately upon written notice if Customer: (a) exceeds the scope of the license or otherwise fails to comply with the licensing or confidentiality provisions of this Agreement, or (b) becomes insolvent, files a bankruptcy petition, institutes proceedings for liquidation or winding up or enters into an agreement to assign its assets for the benefit of creditors. For any other material breach of any provision of this Agreement, Mentor Graphics may terminate this Agreement and/or any license granted under this Agreement upon 30 days written notice if Customer fails to cure the breach within the 30 day notice period. Termination of this Agreement or

- any license granted hereunder will not affect Customer's obligation to pay for Products shipped or licenses granted prior to the termination, which amounts shall be payable immediately upon the date of termination.
- 12.2. Upon termination of this Agreement, the rights and obligations of the parties shall cease except as expressly set forth in this Agreement. Upon termination, Customer shall ensure that all use of the affected Products ceases, and shall return hardware and either return to Mentor Graphics or destroy Software in Customer's possession, including all copies and documentation, and certify in writing to Mentor Graphics within ten business days of the termination date that Customer no longer possesses any of the affected Products or copies of Software in any form.
13. **EXPORT.** The Products provided hereunder are subject to regulation by local laws and United States ("U.S.") government agencies, which prohibit export, re-export or diversion of certain products, information about the products, and direct or indirect products thereof, to certain countries and certain persons. Customer agrees that it will not export or re-export Products in any manner without first obtaining all necessary approval from appropriate local and U.S. government agencies. If Customer wishes to disclose any information to Mentor Graphics that is subject to any U.S. or other applicable export restrictions, including without limitation the U.S. International Traffic in Arms Regulations (ITAR) or special controls under the Export Administration Regulations (EAR), Customer will notify Mentor Graphics personnel, in advance of each instance of disclosure, that such information is subject to such export restrictions.
14. **U.S. GOVERNMENT LICENSE RIGHTS.** Software was developed entirely at private expense. The parties agree that all Software is commercial computer software within the meaning of the applicable acquisition regulations. Accordingly, pursuant to U.S. FAR 48 CFR 12.212 and DFAR 48 CFR 227.7202, use, duplication and disclosure of the Software by or for the U.S. government or a U.S. government subcontractor is subject solely to the terms and conditions set forth in this Agreement, which shall supersede any conflicting terms or conditions in any government order document, except for provisions which are contrary to applicable mandatory federal laws.
15. **THIRD PARTY BENEFICIARY.** Mentor Graphics Corporation, Mentor Graphics (Ireland) Limited, Microsoft Corporation and other licensors may be third party beneficiaries of this Agreement with the right to enforce the obligations set forth herein.
16. **REVIEW OF LICENSE USAGE.** Customer will monitor the access to and use of Software. With prior written notice and during Customer's normal business hours, Mentor Graphics may engage an internationally recognized accounting firm to review Customer's software monitoring system and records deemed relevant by the internationally recognized accounting firm to confirm Customer's compliance with the terms of this Agreement or U.S. or other local export laws. Such review may include FlexNet (or successor product) report log files that Customer shall capture and provide at Mentor Graphics' request. Customer shall make records available in electronic format and shall fully cooperate with data gathering to support the license review. Mentor Graphics shall bear the expense of any such review unless a material non-compliance is revealed. Mentor Graphics shall treat as confidential information all information gained as a result of any request or review and shall only use or disclose such information as required by law or to enforce its rights under this Agreement. The provisions of this Section 16 shall survive the termination of this Agreement.
17. **CONTROLLING LAW, JURISDICTION AND DISPUTE RESOLUTION.** The owners of certain Mentor Graphics intellectual property licensed under this Agreement are located in Ireland and the U.S. To promote consistency around the world, disputes shall be resolved as follows: excluding conflict of laws rules, this Agreement shall be governed by and construed under the laws of the State of Oregon, U.S., if Customer is located in North or South America, and the laws of Ireland if Customer is located outside of North or South America. All disputes arising out of or in relation to this Agreement shall be submitted to the exclusive jurisdiction of the courts of Portland, Oregon when the laws of Oregon apply, or Dublin, Ireland when the laws of Ireland apply. Notwithstanding the foregoing, all disputes in Asia arising out of or in relation to this Agreement shall be resolved by arbitration in Singapore before a single arbitrator to be appointed by the chairman of the Singapore International Arbitration Centre ("SIAC") to be conducted in the English language, in accordance with the Arbitration Rules of the SIAC in effect at the time of the dispute, which rules are deemed to be incorporated by reference in this section. Nothing in this section shall restrict Mentor Graphics' right to bring an action (including for example a motion for injunctive relief) against Customer in the jurisdiction where Customer's place of business is located. The United Nations Convention on Contracts for the International Sale of Goods does not apply to this Agreement.
18. **SEVERABILITY.** If any provision of this Agreement is held by a court of competent jurisdiction to be void, invalid, unenforceable or illegal, such provision shall be severed from this Agreement and the remaining provisions will remain in full force and effect.
19. **MISCELLANEOUS.** This Agreement contains the parties' entire understanding relating to its subject matter and supersedes all prior or contemporaneous agreements. Some Software may contain code distributed under a third party license agreement that may provide additional rights to Customer. Please see the applicable Software documentation for details. This Agreement may only be modified in writing, signed by an authorized representative of each party. Waiver of terms or excuse of breach must be in writing and shall not constitute subsequent consent, waiver or excuse.