Peripheral pin select summary for dsPIC33FJ64MCX02/X04 and dsPIC33FJ128MCX02/X04

Peripheral pin select configuration enables peripheral set selection and placement on a wide range of I/O pins. It is carried out in different ways depending whether an input or an output is mapped.

A pin is “remappable” if it is marked as RPx, being x a number.

Inputs

The inputs of the peripheral pin select options are mapped on the basis of the peripheral. A control register associated with a peripheral (RPINRx) dictates the pin it is mapped to.

Thus, for mapping an input source to a certain pin (remappable pin RPx), number “x” must be written in the corresponding configuration bits for the peripheral.

Input Name	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<4:0>
External Interrupt 2	INT2	RPINR1	INT2R<4:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<4:0>
Timer3 External Clock	T3CK	RPINR3	T3CKR<4:0>
Timer4 External Clock	T4CK	RPINR4	T4CKR<4:0>
Timer5 External Clock	T5CK	RPINR4	T5CKR<4:0>
Input Capture 1	IC1	RPINR7	IC1R<4:0>
Input Capture 2	IC2	RPINR7	IC2R<4:0>
Input Capture 7	IC7	RPINR10	IC7R<4:0>
Input Capture 8	IC8	RPINR10	IC8R<4:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<4:0>
PWM1 Fault	$\overline{\text{FLTA1}}$	RPINR12	FLTA1R<4:0>
PWM2 Fault	$\overline{\text{FLTA2}}$	RPINR13	FLTA2R<4:0>
QEI1 Phase A	QEA1	RPINR14	QEA1R<4:0>
QEI1 Phase B	QEB1	RPINR14	QEB1R<4:0>
QEI1 Index	INDX1	RPINR15	INDX1R<4:0>
QEI2 Phase A	QEA2	RPINR16	QEA2R<4:0>
QEI2Phase B	QEB2	RPINR16	QEB2R<4:0>
QEI2 Index	INDX2	RPINR17	INDX2R<4:0>
UART1 Receive	U1RX	RPINR18	U1RXR<4:0>
UART1 Clear To Send	$\overline{\text{U1CTS}}$	RPINR18	U1CTSR<4:0>
UART2 Receive	U2RX	RPINR19	U2RXR<4:0>
UART2 Clear To Send	$\overline{\text{U2CTS}}$	RPINR19	U2CTSR<4:0>
SPI1 Data Input	SDI1	RPINR20	SDI1R<4:0>
SPI1 Clock Input	SCK1	RPINR20	SCK1R<4:0>
SPI1 Slave Select Input	$\overline{\text{SS1}}$	RPINR21	SS1R<4:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<4:0>
SPI2 Clock Input	SCK2	RPINR22	SCK2R<4:0>
SPI2 Slave Select Input	$\overline{\text{SS2}}$	RPINR23	SS2R<4:0>
ECAN1 Receive	CIRX	RPINR26	CIRXR<4:0>

For example, for remapping U2RX to pin RB6, in a dsPIC33FJ128MC802 model:

pin RB6 = RP6 → `RPINR19bits.U2RXR = 6;`

Outputs

In contrast to inputs, the outputs of the peripheral pin select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped.

The registers associated with the output pins are RPORx. The register RPORx contains two 5-bit fields: RP(2x)R and RP(2x+1)R.

For example, RP5R refers to pin RP5, and is in register RPOR2.

Each output peripheral has a specific code, which must be written in the RPnR bits of its corresponding RPORx register, where RPn is the pin where the output peripheral is going to be mapped.

Function	RPnR<4:0>	Output Name
NULL	00000	RPn tied to default port pin
C1OUT	00001	RPn tied to Comparator1 Output
C2OUT	00010	RPn tied to Comparator2 Output
U1TX	00011	RPn tied to UART1 Transmit
$\overline{\text{U1RTS}}$	00100	RPn tied to UART1 Ready To Send
U2TX	00101	RPn tied to UART2 Transmit
$\overline{\text{U2RTS}}$	00110	RPn tied to UART2 Ready To Send
SDO1	00111	RPn tied to SPI1 Data Output
SCK1	01000	RPn tied to SPI1 Clock Output
$\overline{\text{SS1}}$	01001	RPn tied to SPI1 Slave Select Output
SDO2	01010	RPn tied to SPI2 Data Output
SCK2	01011	RPn tied to SPI2 Clock Output
$\overline{\text{SS2}}$	01100	RPn tied to SPI2 Slave Select Output
C1TX	10000	RPn tied to ECAN1 Transmit
OC1	10010	RPn tied to Output Compare 1
OC2	10011	RPn tied to Output Compare 2
OC3	10100	RPn tied to Output Compare 3
OC4	10101	RPn tied to Output Compare 4
UPDN1	11010	RPn tied to QEI1 direction (UPDN) status
UPDN2	11011	RPn tied to QEI2 direction (UPDN) status

For example, remap U2TX to pin RB7 (=RP7), in a dsPIC33FJ128MC802 model:

1. RP7R is in register RPOR3

2. U2TX = 00101 = 5

→ `RPOR3bits.RP7R = 5;`

Warning: CONTROL REGISTER LOCK

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

Thus, a possible code for allowing modifications of RPINRx and RPORx registers would be:

```
__builtin_write_OSCCONL(OSCCON & 0Xbf); //unlock PPS
//remap peripherals
__builtin_write_OSCCONL(OSCCON | 0x40); //lock PPS
```

References

[1] Microchip Technology Inc., «dsPIC33FJXXXMCX02-X04 datasheet,» 2007-2012.