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# STA2HTM User Guide

Albert Li, 01/25/2021



客戶 服務 務實 互信 學習 進步

## How to install STA2HTM package



- Check STA2HTM in the Github
  - https://github.com/icdop/sta2htm/
- Download the STA2HTM package from Github and unpack it
  - □ https://github.com/icdop/sta2htm/releases
- ■Install the required Linux packages
  - gnuplot
  - □ tree
- Follow the README instruction to run the testcase run/01\_sta
  - % source setup.cshrc
  - % cd run/01\_sta
  - □ % make run

## How to setup STA2HTM run directory

- Prepare STA timing reports generated by Primetime
  - Recommended directory structure for MMMC
    - \$STA\_RPT/<Mode>/<Corner>/\$sta\_check.rpt
- Create STA2HTM setup directory .sta/ under \$STA\_RPT
- Edit Corner definition file (sta2htm.corner):
  - **\$STA\_RPT** /.sta/sta2htm.corner

- 000 000\_TT 151 151\_ML 157 157\_BC 231 231\_WCL 258 258\_WC
- ■Edit STA2HTM configuration file (sta2htm.cfg):
  - \$STA\_RPT /.sta/sta2htm.cfg

```
# STA report filename filter : $STA_RPT_PATH/$STA_RPT_FILE
set STA_RPT_PATH {$sta_mode/$corner_name}
set STA_RPT_FILE {$sta_check$sta_postfix.rpt*}

# STA mode name list
set STA_MODE_LIST "func scan"

# STA scenario table ($sta_mode,$sta_check) => "$sta_corner ...."
set STA_CORNER(func,setup) "000 157 231 258"
set STA_CORNER(func,hold) "000 151 157 258"
set STA_CORNER(scan,setup) "000 157"
set STA_CORNER(scan,hold) "000 157 258"
```



```
apr0-0122/
   func
       000 TT
          - hold.rpt
          setup.rpt
       151 ML
        └─ hold.rpt
       157 BC
         — hold.rpt
           setup.rpt
       231 WCL
         — setup.rpt
       258 WC
          - hold.rpt
           setup.rpt
    scan
       000 TT
           hold.rpt
          setup.rpt
       157 BC
        └─ hold.rpt
```

## How to generate STA2HTM reports



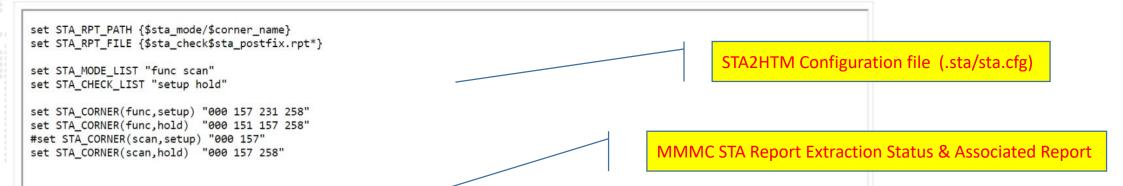
- CMD: sta\_init\_dir <STA\_RUN> <STA\_RPT>
  - Create a run directory \$(STA\_RUN)
  - Copy setup directory \$(STA\_RPT)/.sta to the rundir \$(STA\_RUN)
  - Link the report directory \$(STA\_RPT) to STA under run directory
- Modify configuration file sta2htm.cfg
  - □ Review the mode/check/corner combinations
- CMD: sta\_rpt\_uniq\_end -sum\_dir uniq\_end -sta\_check setup
- ■CMD: sta\_rpt\_uniq\_end -sum\_dir uniq\_end -sta\_check hold
  - □ Process the timing reports of specific timing check and merge multi-corners violation points
- CMD: sta\_gen\_index -sum\_dir uniq\_end
  - ☐ Generate index.htm under \$(STA\_RUN)/uniq\_end

# Dashboard of MMMC STA Reports (index.htm)



[@Index] [@Mode] [@Check] [@Corner]

### GOLDEN-0122/uniq\_end/



Mode	Check	Corner	NVP	WNS	TNS	STA Report
		000_TT	8	-57.43	-194.64	/home/ISSBG/GITHOME/sta/run/reports/apr0-0122/func/000_TT/setup.rpt
func	setun	<u>157_BC</u>	0	0.0	0.0	/home/ISSBG/GITHOME/sta/run/reports/apr0-0122/func/157_BC/setup.rpt
<u>runc</u>	<u>setup</u>	231_WCL	28	-114.56	-656.93	/home/ISSBG/GITHOME/sta/run/reports/apr0-0122/func/231_WCL/setup.rpt
		258_WC	28	-84.05	-422.68	/home/ISSBG/GITHOME/sta/run/reports/apr0-0122/func/258_WC/setup.rpt
		000_TT	13	-125.26	-580.13	/home/ISSBG/GITHOME/sta/run/reports/apr0-0122/func/000_TT/hold.rpt
func	hold	151_ML	20	-1.77	-17.65	/home/ISSBG/GITHOME/sta/run/reports/apr0-0122/func/151_ML/hold.rpt
TUTE	<u>nota</u>	<u>157_BC</u>	32	-1.48	-19.64	/home/ISSBG/GITHOME/sta/run/reports/apr0-0122/func/157_BC/hold.rpt
		258_WC	3	-50.81	-115.31	/home/ISSBG/GITHOME/sta/run/reports/apr0-0122/func/258_WC/hold.rpt

## Index Dashboard of MMMC STA Reports





[@Index] [@Mode] [@Check [@Corner

### GOLDEN-1114/uniq\_end/

Corner	func /setup	func /hold	scan /hold
000_TT	•	<u>4</u>	
151_ML	-	<u>20</u>	<u>11</u>
157_BC		<u>33</u>	-
258_WC	<u>11</u>	<u>3</u>	*

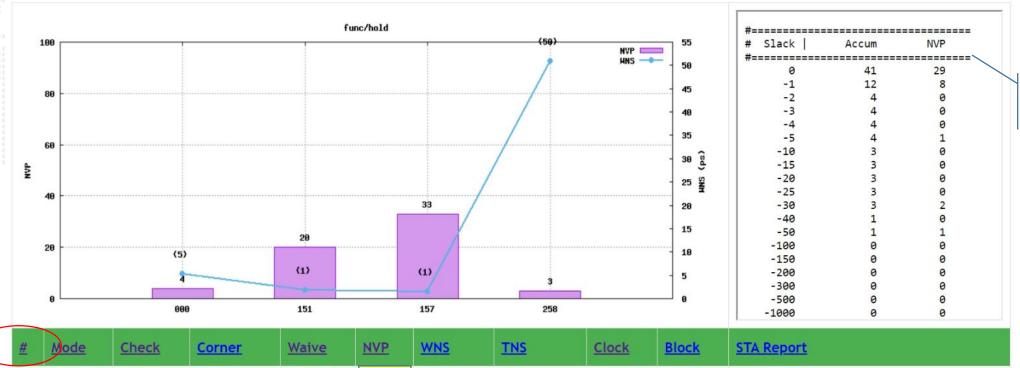
<sup>\*</sup> Missing STA report files

## One Page Summary of Multi-Corners STA Reports LYG FOXCONN



[@Index] [@Mode] [@Check] [@Corner]

### GOLDEN-1114/uniq\_end/func/hold



Slack

#		Mode	Check	Corner	<u>Waive</u>	NVP	<u>WNS</u>	TNS	Clock	Block	STA Report
1		func	hold	000_TT		4	<u>-5.26</u>	<u>-11.74</u>	<u>2</u>	1	STA/func/000_TT/hold.rpt
2	9	func	hold	151_ML		<u>20</u>	<u>-1.77</u>	<u>-17.65</u>	<u>5</u>	1	STA/func/151_ML/hold.rpt
3		func	hold	157_BC	•	<u>33</u>	<u>-1.48</u>	-20.69	<u>8</u>	1	STA/func/157_BC/hold.rpt
4	L	func	hold	258_WC		<u>3</u>	<u>-50.81</u>	<u>-115.31</u>	<u>2</u>	2	STA/func/258_WC/hold.rpt
							-50.81	-165.39			

**STA Report** Location

# Multi-Corners Uniquify Violation End Point Report LYG | FOXCO



### GOLDEN-1114/uniq\_end/func/hold

**Uniquify Violation End Point** 

No	000	151	157	258	WNS	WCorner	PathGroup	InstancePin
1			-1.05		-1.05	157	**clock_gating_default**	u_core/u_spi/u_spi_txrx/clk_gate_buf_rxd_reg/latch/E
2				-31.41	-31.41	258	CLK_DDR_PHY_pub_ctl_0	u_ddr_phy/dfi_address[1]
3				-33.09	-33.09	258	CLK_DDR_PHY_pub_ctl_0	u_ddr_phy/dfi_address[4]
4	ž	*	•	-50.81	-50.81	258	CLK_DDR_PHY_pub_ctl_0	u_ddr_phy/dfi_address[8]
5	*	-0.57	-0.76		-0.76	157	CLK_DI_ISP	u_core/u_isp_top/u_isp_exp_v2_sram_wrapper/gen_rf_128x19_u_rf_128x19/A[2]
6	ž	-0.77	-0.72		-0.77	151	CLK_DI_ISP	u_core/u_isp_top/u_r_lscram/gen_sram_512x24_u_sram_512x24/A[5]
7		-0.90	-0.82		-0.90	151	CLK_DI_ISP	u_core/u_isp_top/u_vsm_ram2a/gen_sram_960x32_u_sram_960x32/A[1]
8	9		-0.07		-0.07	157	CLK_MCU	u_core/u_ful_regd_slice/payload_reg_a_reg_21_/D
9	*	-0.47			-0.47	151	CLK_MCU	u_core/u_ful_regd_slice/payload_reg_a_reg_23_/D
10		-1.33	-0.33		-1.33	151	CLK_MCU	u_core/u_ful_regd_slice/payload_reg_a_reg_43_/D
11		-0.54	-0.24		-0.54	151	CLK_MCU	u_core/u_ful_regd_slice/payload_reg_a_reg_65_/D
12	¥	-1.20	-1.00	¥	-1.20	151	CLK_MCU	u_core/u_ful_regd_slice/payload_reg_b_reg_14_/D
13		-0.37	-0.87		-0.87	157	CLK_MCU	u_core/u_ful_regd_slice/payload_reg_b_reg_24_/D
14	*	-0.45	-0.55		-0.55	157	CLK_MCU	u_core/u_ful_regd_slice/payload_reg_b_reg_41_/D
15		-0.93	-0.13	ž	-0.93	151	CLK_MCU	u_core/u_ful_regd_slice/payload_reg_b_reg_47_/D
16	•	-0.81	-0.61		-0.81	151	CLK_MCU	u_core/u_ful_regd_slice/payload_reg_b_reg_58_/D
17		-1.57	-1.47		-1.57	151	CLK_MCU	u_core/u_ful_regd_slice/payload_reg_b_reg_65_/D
18		-0.78	-0.08	*	-0.78	151	CLK_MCU	u_core/u_rev_regd_slice/payload_reg_reg_36_/D

# Cross-Clocks Analysis of NVP & WNS



<u>#</u>	<u>Mode</u>	<u>Check</u>	Corner	<u>Waive</u>	NVP	<u>WNS</u>	TNS	Clock
1	func	hold	000_TT	•	<u>4</u>	<u>-5.26</u>	<u>-11.74</u> (	2
2	func	hold	151_ML		<u>20</u>	<u>-1.77</u>	-1 <del>7.65</del>	<u>5</u>
3	func	hold	157_BC		<u>33</u>	<u>-1.48</u>	<u>-20.69</u> (	8
4	func	hold	258_WC		3	<u>-50.81</u>	<u>-115.31</u>	2
						-50.81	-165.39	/

### GOLDEN-1114/uniq\_end/func/hold/000\_TT

#2 Clocks	WNS	-	1	2
-:-				
1 : CLK_VIP	-5.26	2	1	
2 : CLK_VIP_DIV2	-0.61	2		1

### GOLDEN-1114/uniq\_end/func/hold/157\_BC

#8 Clocks	WNS	-
1 : **clock_gating_default**	-1.05	2
-:-		
2 : CLK_DI_ISP	-0.82	3
3 : CLK_MCU	-1.47	10
4 : CLK_VAE	-0.48	1
5 : CLK_VIDEO_DIV2_ISP	-0.82	3
6 : CLK_VIDEO_ISP	-0.82	3
7 : CLK_VIP	-0.50	1
8 : CLK_XTAL_MCU	-1.48	10

### uniq\_end/func/hold

#12 Clocks	NVP	WNS	<u>000</u>	<u>151</u>	<u>157</u>	<u>258</u>
1 : **clock_gating_default**	2	-1.05			-1.05	
-:-						
2 : CLK_DDRC_0						
3 : CLK_DDR_PHY_pub_ctl_0	3	-50.81				-50.81
4 : CLK_DI_ISP	6	-0.90		-0.90	-0.82	
5 : CLK_MCU	20	-1.57		-1.57	-1.47	
6 : CLK_VAE	3	-0.58		-0.58	-0.48	
7 : CLK_VIDEO_DIV2_ISP	7	-1.77		-1.77	-0.82	
8 : CLK_VIDEO_ISP	4	-1.76		-1.76	-0.82	
9 : CLK_VIP	3	-5.26	-5.26		-0.50	
10 : CLK_VIP_DIV2	2	-0.61	-0.61			
11 : CLK_XTAL_MCU	10	-1.48			-1.48	
12 : 0CC4	11	-64.24		-64.24		

# Cross-Blocks Analysis of NVP & WNS



<u>#</u>	<u>Mode</u>	<u>Check</u>	Corner	<u>Waive</u>	<u>NVP</u>	<u>WNS</u>	TNS	Clock	Block	)
1	func	hold	000_TT	•	<u>4</u>	<u>-5.26</u>	<u>-11.74</u>	<u>2</u>	1	
2	func	hold	151_ML		<u>20</u>	<u>-1.77</u>	<u>-17.65</u>	<u>5</u>	1	
3	func	hold	157_BC	•	<u>33</u>	<u>-1.48</u>	-20.69	<u>8</u>	1	
4	func	hold	258_WC	•	<u>3</u>	<u>-50.81</u>	<u>-115.31</u>	<u>2</u>	<u>2</u>	)
						-50.81	-165.39			
	00							<u> </u>		•

## uniq\_end/func/hold

#2 Blocks	NVP	WNS	<u>000</u>	<u>151</u>	<u>157</u>	<u>258</u>
-:-						
1 : u_core	57	-5.26	-5.26	-1.77	-1.48	
2 : u_ddr_phy	3	-50.81				-50.81

### uniq\_end/func/hold/258\_WC

#2 Blocks	WNS		1	2
-:-				
1 : u_core				
2 : u_ddr_phy	-50.81	3	3	



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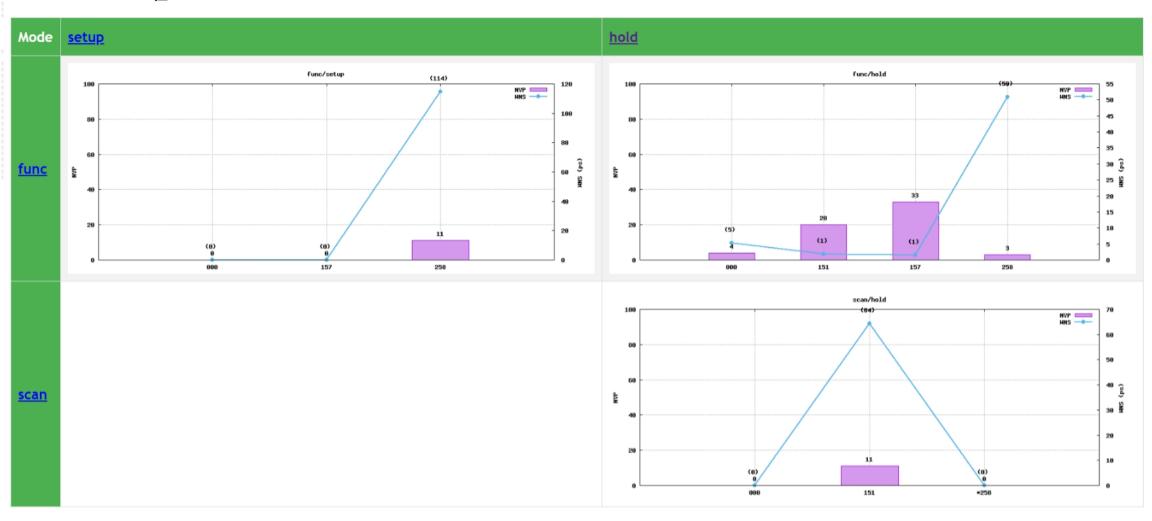


# Metrix of MMMC STA Report



[@Index [@Mode] [@Check] [@Corner]

GOLDEN-1114/uniq\_end/

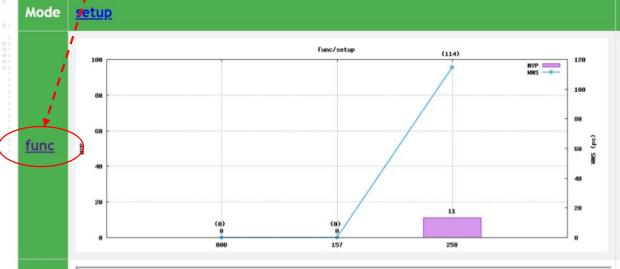


# Summary of Single Mode STA Reports



[@Index] [@Mode] [@Check] [@Corner]

GOLDEN-1114/uniq\_end/ (func) (scan)



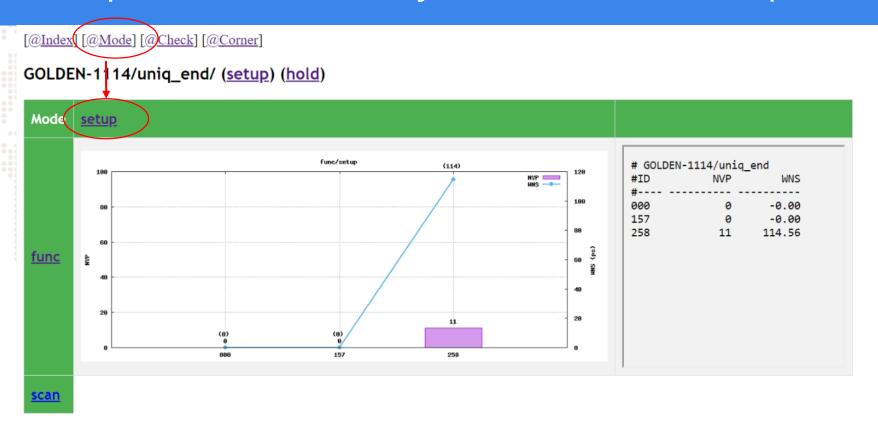


#===	======			========	
#	REAL	WAIVED	NVP	WNS	PathGroup
#===					
	1	0	1	-14.99	VCLK_APB
	2	0	2	-114.56	VCLK_CAN
	4	0	4	-9.43	VCLK_DO
	3	0	3	-97.43	VCLK_FLH
	1	0	1	-8.06	VCLK_MCU08
#===					
#	11	0	11	-114.56	5
#===	======			========	

<del> </del> ====	=====	========			
#	REAL	WAIVED	NVP	WNS	PathGroup
#====	=====				
	1	0	1	-1.05	**clock_gating_default**
	3	0	3	-50.81	CLK_DDR_PHY_pub_ctl_0
	3	0	3	-0.90	CLK_DI_ISP
	11	0	11	-1.57	CLK_MCU
	2	0	2	-0.58	CLK_VAE
	5	0	5	-1.77	CLK_VIDEO_DIV2_ISP
	3	0	3	-1.76	CLK_VIDEO_ISP
	2	0	2	-5.26	CLK_VIP
	1	0	1	-0.61	CLK_VIP_DIV2
	10	0	10	-1.48	CLK_XTAL_MCU
#====	=====	========		========	
#	41	0	41	-50.81	10
#====	=====		========	========	

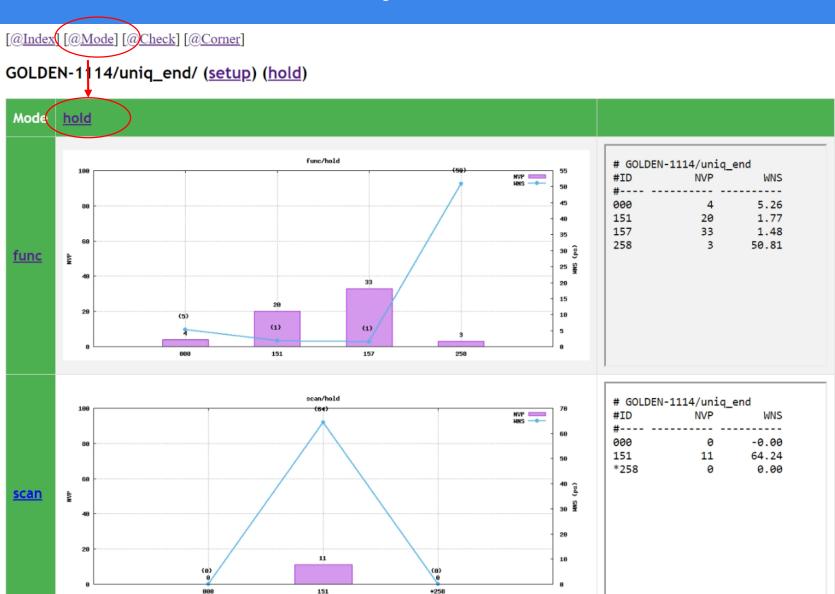
# Setup Check Summary of MMMC STA Reports





# Hold Check Summary





## Table Format Summary of MMMC STA Reports



[@Index] [@Mode] [@Check] [@Corner]

### GOLDEN-1114/uniq\_end/

Check	<u>func</u>	<u>scan</u>
<u>setup</u>	# GOLDEN-1114/uniq_end #ID NVP WNS #	
<u>hold</u>	# GOLDEN-1114/uniq_end #ID NVP WNS #	# GOLDEN-1114/uniq_end #ID NVP WNS # 000 0 -0.00 151 11 64.24 *258 0 0.00



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**Text Report Files** 

## Violation files generated with each timing corner





### <corner>.vio

```
# File : /home/ISSBG/GITHOME/sta/run/reports/apr0-0122/func/000 TT/setup.rpt
# Report : constraint -path slack_only (Line# 2)
    -54.31 VCLK APB
                                           pad_gpio_pa[0]
     -6.00 VCLK_APB
                                          pad_gpio_pa[1]
     -5.00 VCLK_APB
                                          pad_gpio_pa[2]
     -4.00 VCLK APB
                                          pad_gpio_pa[3]
    -57.43 VCLK_FLH
                                           pad_sflash_io[2]
    -42.14 VCLK_FLH
                                           pad_sflash_io[3]
    -21.70 VCLK_FLH
                                          pad_sflash_io[1]
                                          pad_gpio_pb[15]
     -4.06 VCLK_MCU08
```

#### <corner>.wns

ŧ	# Mode : f	unc			
ŧ	#======	= =======	=======	========	=======================================
ŧ	# REA	L WAIVED	NVP	WNS	PathGroup
ŧ	#======	= =======	=======	========	=======================================
		4 0	4	-54.31	VCLK_APB
		3 0	3	-57.43	VCLK_FLH
		1 0	1	-4.06	VCLK_MCU08
#	#======	= =======	========	========	
#	#	8 0	8	-57.43	3
#	#======	= =======	=======	=======	=======================================

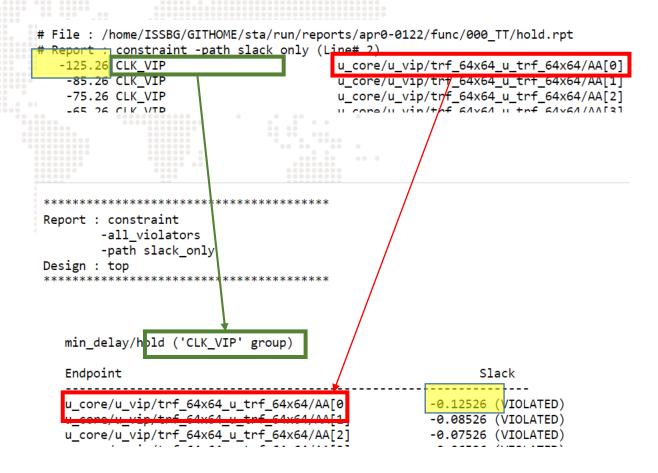
### <corner>.nvp

#======================================								
# Slack	Accum	NVP						
#===============								
0	8	0						
-1	8	0						
-2	8	0						
-3	8	0						
-4	8	2						
-5	6	2						
-10	4	0						
-15	4	0						
-20	4	1						
-25	3	0						
-30	3	0						
-40	3	1						
-50	2	2						
-100	0	0						
-150	0	0						
-200	0	0						
-300	0	0						
-500	0	0						
-1000	0	0						

## Ex1: Processing Primetime Slack Violation Report LYG FOXCONN







## Ex2: Processing Primetime Detail Violation Report LYG | FOXCOND



```
# Report : constraint -verbose (Line# 2)
*001:00050 CLK DDRC 0
                                          u core/u ddr ctrl 0/stat reg 0 /0
    -50.81 CLK DDR PHY pub ctl 0
                                          u ddr phy/dfi address[8]
*002:00095 CLK DDRC 0
                                          u_core/u_ddr_cti/1_0/stat_reg_0_/Q
   -33.09 CLK DDR PHY pub ctl 0
                                          u_ddr_phy/dfi_address[4]
                                          u_core/u_ddr_ctrl_0/BANK_x_STM/bnx_t_rCL_reg_2_/Q
*003:00141 CLK DDRC 0
   -31.41 CLK_DDR_PHY_pub_ctl_0
                                          u_ddr_phy/dfi_address[1]
Report : constraint
 -all violators
 -verbose
 -min delay
Design : top
  Startpoint: u_core/u_ddr_ctrl_0/stat_reg_0_
               (rising eage-triggerea trip-trop clocked by CLK DDRC 0)
  Endpoint: u_ddr_phy (rising edge-triggered flip-flop clocked by CLK_DDR_PHY_pub_ctl_0)
  Last common nin u core/u core gck/CTS ccl inv 480185/ZN
  Path Group: CLK DDR PHY pub ctl 0
  Path Type: min
  Point
                                                                                                                Path
  clock CLK DDRC 0 (rise edge)
                                                                                                  0.00000
                                                                                                             0.00000
  clock network delay (propagated)
                                                                                                             1.09920
                                                                                                  1.09920
  u_core/u_ddr_ctrl_0/stat_reg_0_/CP (SDFCNQOPTBD2)
                                                                                           1.09920 r
                                                                                0.00000
  u core/u ddr ctrl 0/stat reg 0 /Q (SDFCNOOPTBD2)
                                                                                0.02956 & 1.12876 r
  u core/u lpddr2 ctrl2phv/U19/ZN (ND2OPTPAD16LVT)
                                                                                0.00800 & 1.25965 f
  u_ddr_phy/dfi_address[8] (DDRPHY top)
                                                                                              0.02936 & 1.28902 f
                                                                                                             1.28902
```