Notes on reconfiguring the phase of the phase-locked loop (PLL)

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At the core of a PLL is a voltage-controlled oscillator (VCO) whose frequency is stabilized by the control loop of the PLL. The outputs of the PLL are determined by a fraction of two integers. The VCO value is set by Quartus based on the requested frequency of the outputs. The minimum phase shift (in ps) is equal to 1/8 of the VCO period. Thus, by choosing the correct combination of frequencies for the output of the PLL, you can for Quartus to set the VCO frequency as high as possible, giving the finest phase step size.

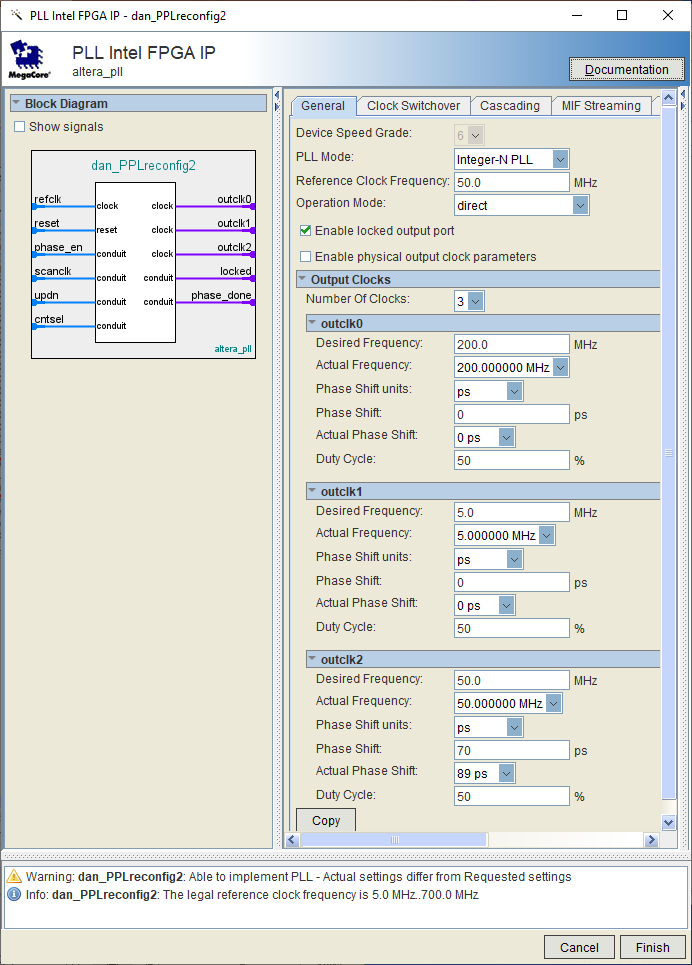
If all you want is to adjust the phase, you can do this directly in the ALTPLL Megafunction without having to use the PLL configuration Megafunction, which requires an Avalon memory manager with an associated processor such as NIOS II or an HPS with an associated bridge. To select the dynamic reconfiguration mode in the ALTPLL Megafunction, check the box in the “Settings” tab as shown in the figure.



In playing around with the various settings, it appears that the highest VCO frequency for the Cyclone V chip found on the DE10-Nano-Soc is 1,600 MHz, which gives a minimum phase shift of 78.125 ps. This should be small enough to test out the resolution of the carry-chain-based time-to-digital converter (TDC).

I will walk through an example of how to obtain the highest VCO frequency. The idea is that I want one clock that operates around 200 MHz to drive SignalTap, which I find is usually reliable at this frequency. I then want two other clock outputs that will produce digital pulses that are high for longer than we expect the delay in a single LAB carry chain, which is somewhere around 500 ps to 1 ns (assuming 50 ps delay per carry chain, and either 10 or 20 effective number of charry chains per LAB). A reasonable value is 50 MHz, which will give a digital pulse of 10 ns, much longer than the expected delay through a LAB. This will still be useful to characterize a carry-chain TDC that crosses multiple LAB boundaries if we want. I want 2 clocks around this frequency, and I want to dynamically change the phase of the second one relative to the first. Thus, I want 3 outputs from the PLL.

When I use 200 MHz, 50 MHz, 50 MHz, the low frequency clocks are fractional multiples of the first and the VCO frequency does not take on its maximum value. You can find the VCO frequency chosen in the Megafunction by going to the “Advanced Parameters” tab of the ALTPLL Megafunction (you must scroll down the menu of parameters to see the proper entry). The next figures are what I see with this requested setting in both the General tab and the Advanced Parameters tab, respectively. Notice that I put in a small phase shift request in the 3rd PLL output so I can see the minimum phase shift. (When you instantiate, you need to always have a small phase shift in any two oscillators that have the same frequency – the optimizer will just combine the two oscillators into a single output and you won’t be able to change its phase.). We see that the VCO frequency is 1,400 MHz and the minimum phase shift is 89 ps.





To force a higher frequency VCO, choose the low-frequency PLL outputs to be slightly different, say 51 MHz. In this case, the VCO frequency goes to 1,600 MHz, the minimum phase shift is 78 ps, and the closest frequency that can be synthesized for these two outputs is 51.6129 … MHz.

