Queen Mary University of London

School of Electronic Engineering and Computer Science

ECS527U: Digital System Design

Lab Test 2: Sequential Circuit Modelling & Simulation

Introduction

This specification explains the design and the requirement for your summative lab test which contributes to **25%** of your grade in this module.

When you take this test, you agree to:

- write or modify your VHDL codes completely on your own and without assistance from any other persons.
- keep your answers confidental and refuse to disclose that to anyone
- submit the final version of your work for grading by the deadline
- be questioned about your own work for originality if necessary

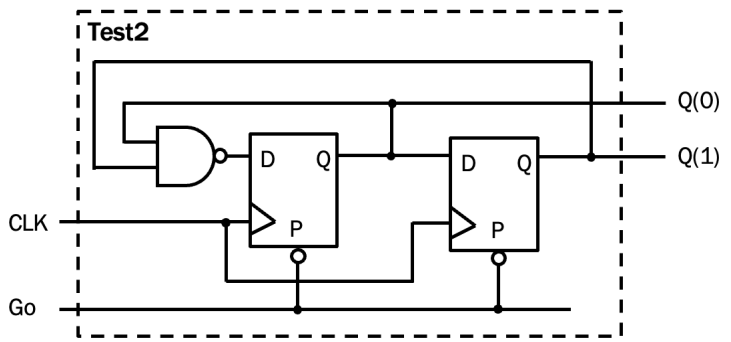
Restriction: only the following VHDL package(s) and feature(s) is/are allowed in any of your circuit model design files (testbenches excluded) for this test. *Marks will be deducted if you do not follow the rules.*

- `IEEE.std_logic_1164.all` **ONLY**
- Intermediate signals, logic operators, relational operators
- Signal assignment statements, conditional signal assignment statements (when-else, with-select)
- Port map statements
- Process statements, if-else statements, case statements

Deadline: Group 01 – **24th April, 2021** Saturday 09:00

Specification

You are asked to model the following sequential circuit `Test2` which has two inputs Go and CLK, each 1 bit, and a two-bit output Q:



Please note that P is an **active-low**, **asynchronous** control to preset Q of the positive-edge triggered flip-flop to 1.

Task 1: VHDL Modelling

- Extract the given project `ECS527U_Test2.zip` to a working folder on your working PC. The structure of the project is shown below.
- Open the project with Xilinx Vivado.
- Study the VHDL source codes provided.
- Edit the file `Test2.vhd` and write your VHDL codes based on the requirement.
- Check the syntax of your VHDL.

```
NI_DSDB_Top.vhd
       \________ NI_DSDB_demo_core.vhd
                        |
                        \_____________ (Test2.vhd) <- (Test2_tb.vhd) <testbench>

[xxx.vhd]: VHDL files for you to create and work on
(yyy.vhd): VHDL files that you may need to modify
```

Task 2: Testbench Design and Simulation

Modify the VHDL testbench `Test2_tb.vhd` for the module `Test2`. Write VHDL processes to generate the necessary stimuli, including the clock signal, to test the correctness of `Test2`.

When you have completed the testbench, run simulation in Vivado and check the waveform to confirm that the sequential circuit in Task 1 works as it intends.

(Hint: *it should produce a repeating sequence of numbers*)

Task 3: Lab Board Verification

If simulation is successful, you can run synthesis, implementation and bitstream generation. Then program the lab board using the hardware manager:

- Choose "Open Hardware Manager" and auto-detect target board.
- Program the design.

Remote access: Please note that the DIO switches are controlled using the *NI ELVISmx Digital Writer Software* which will be demonstrated during the lab session. To see the lab board in the remote session please turn on the webcam of the working PC. Once you see the lab board, you can verify your design.

The device mapping has been provided in `NI_DSDB_demo_core`, as listed in the table below.

Devices	Signal(s)
input: `elvis_dio(0)`	Go
output: `ss0`	Q (padded with 0s)

Submission

Submit to QMPlus the VHDL files `Test2.vhd` and `Test2_tb.vhd`. If you have created or modified any other design files, submit them too.

Deadline: Group 01 – **24th April, 2021** Saturday 09:00

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– End of Lab Test 2 –