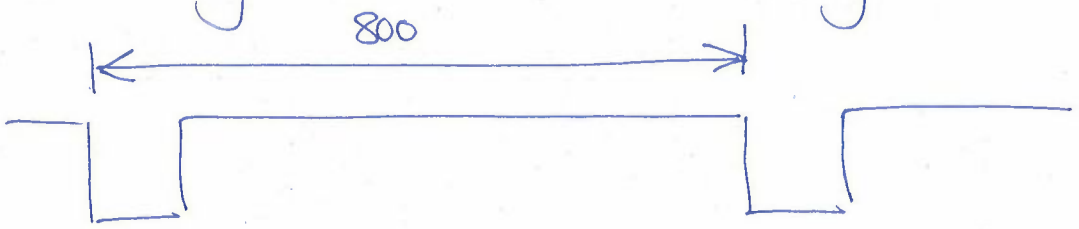
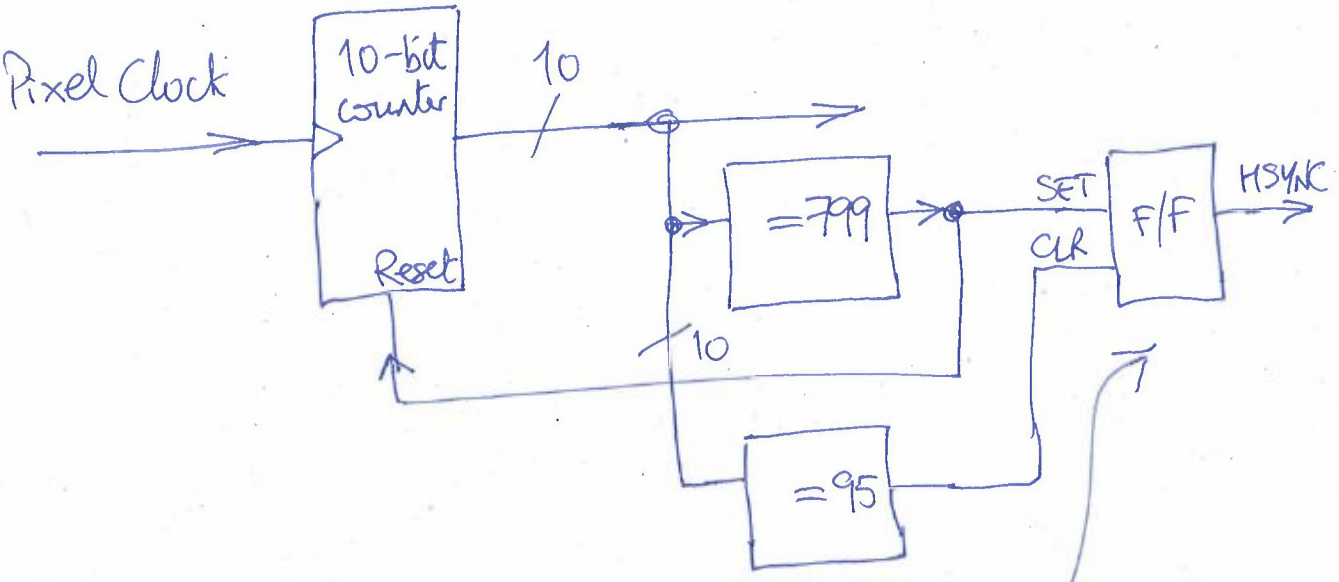
How to generate the HSYNC signal:



96 Pixel Clock cycles = 96 x 40 ns = 3.84 µs
as per Figure 14 in the Basys3 RM.



This could be a SR or JK latch or flip-flop.

How it works – the equals 799 circuit clears the counter ⇒ period of counter is 800 clocks.

The F/F is set by the =799 at the start of the cycle and cleared after 96 clock cycles. The F/F output will be the HSYNC signal (may need inverting)