Operating System Practice

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Grading

- Midterm: 20%
- Lab Exercises: ~~20%~~ ➔ 10%
  - Homework: 10%
  - Labs: N/A
- Quizzes and Attendance: ~~20%~~ ➔ 26%
  - Quizzes 1, 2: 8%, 8%
  - Attendance: 10%
- Final Exam: ~~20%~~ ➔ 22%
- Final Project: ~~20%~~ ➔ 22%

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Flash Memory and Phase Change Memory

Reference: Prof. Tei-Wei Kuo, NTU and Dr. Yuan-Hao Chang, Academia Sinica

Trends – Market and Technology

- Diversified Application Domains
  - Portable Storage Devices
  - Consumer Electronics
  - Industrial Applications
- Competitiveness in the Price
  - Dropping Rate and the Price Gap with HDDs
- Technology Trend over the Market
  - Improved density
  - Degraded performance
  - Degraded reliability

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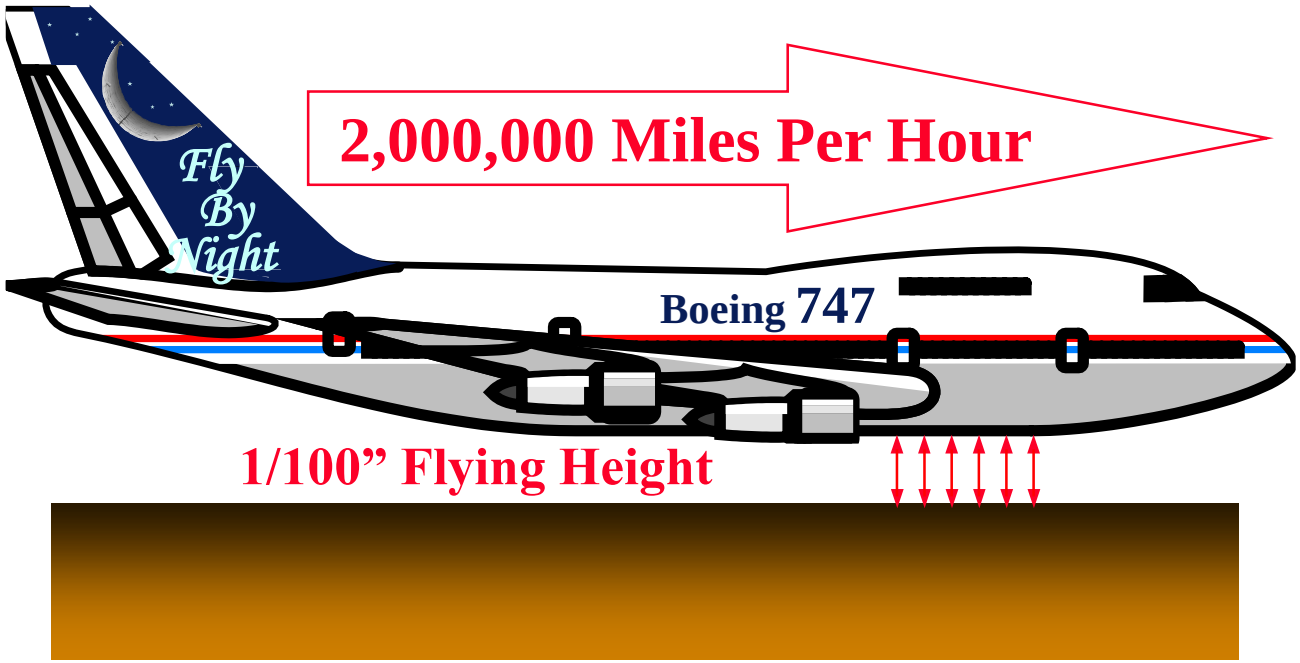
Trends – Storage Media



VS

Source: Richard Lary, The New Storage Landscape: Forces shaping the storage economy, 2003.

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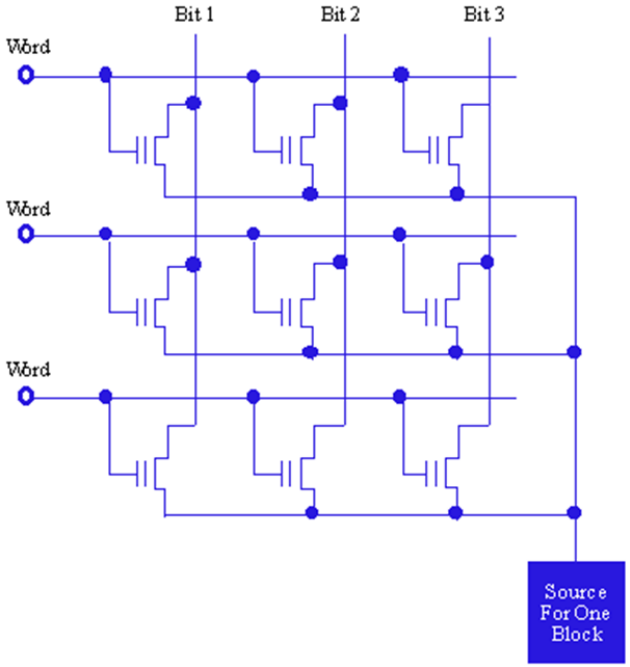
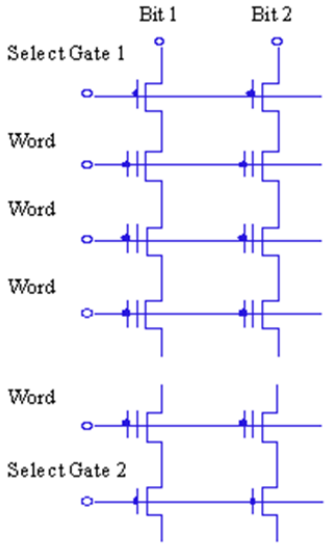
NOR and NAND Flash

- NAND accesses each cell through adjacent cells, while NOR allows for individual access to each cell
- The cell size of NAND is almost half the size of a NOR cell





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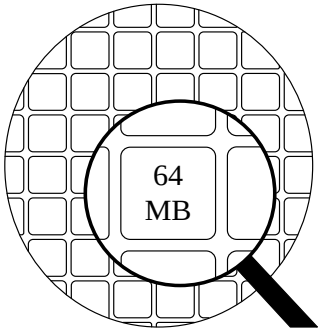
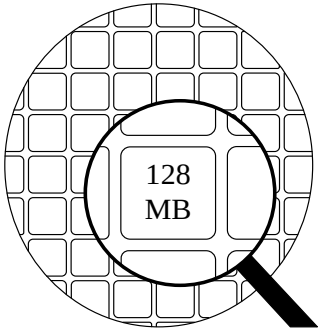
Single-Level Cell (SLC) vs Multi-Level Cell (MLC) Flash

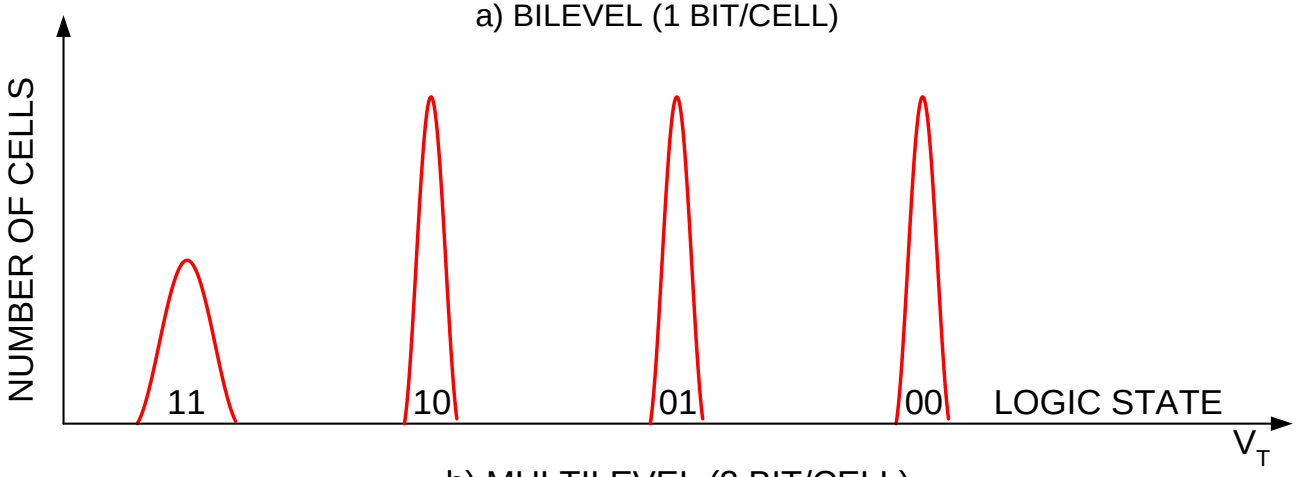
SLC Flash



a) BILEVEL (1 BIT/CELL)

MLC Flash





b) MULTILEVEL (2 BIT/CELL)

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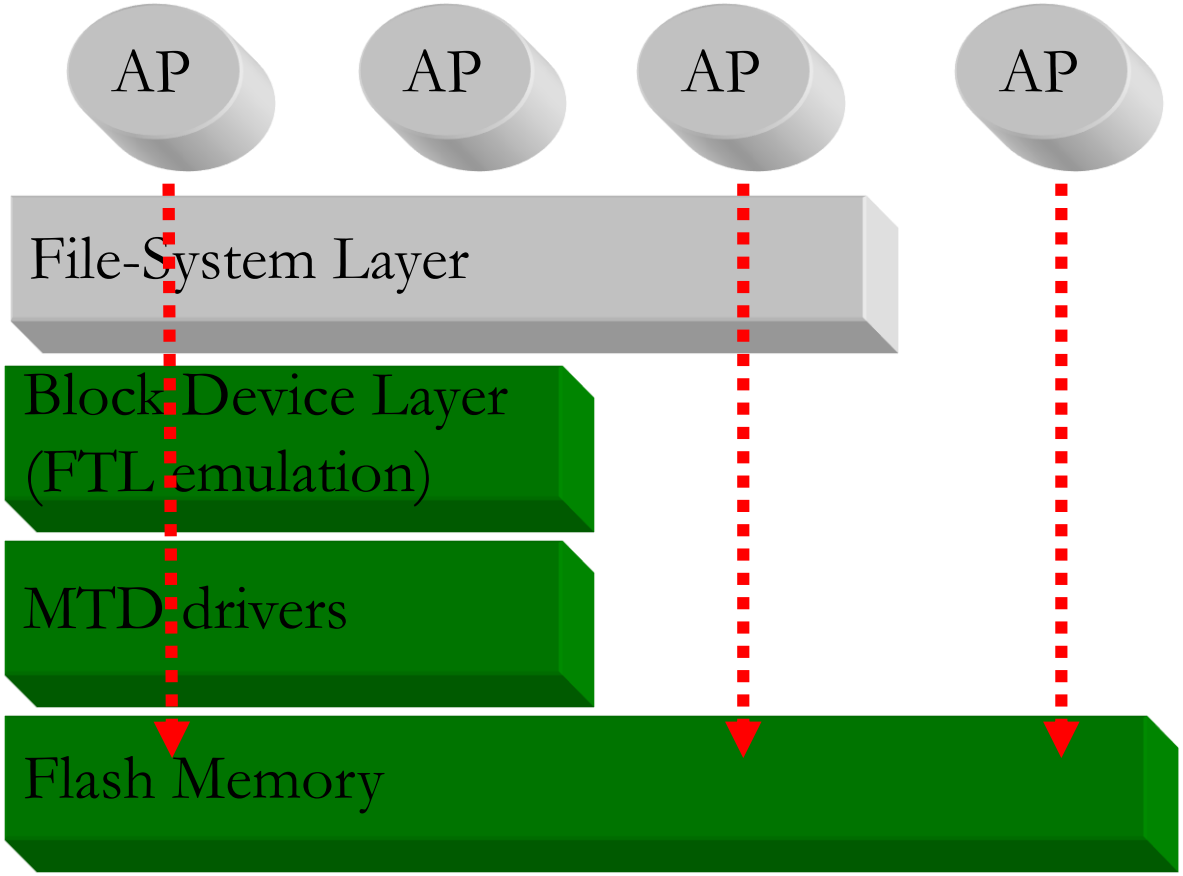
System Architectures for Flash Management



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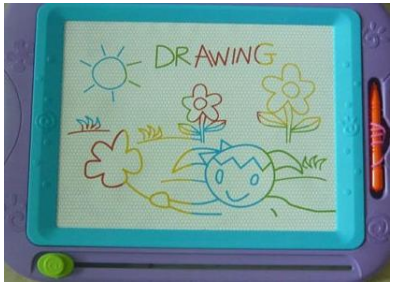
Flash-Memory Characteristics

- Write-Once
  - No writing on the same page unless its residing block is erased
  - Pages are classified into valid, invalid, and free pages
- Bulk-Erasing
  - Pages are erased in a block unit to recycle used but invalid pages



- Wear-Leveling
  - Each block has a limited lifetime in erasing counts

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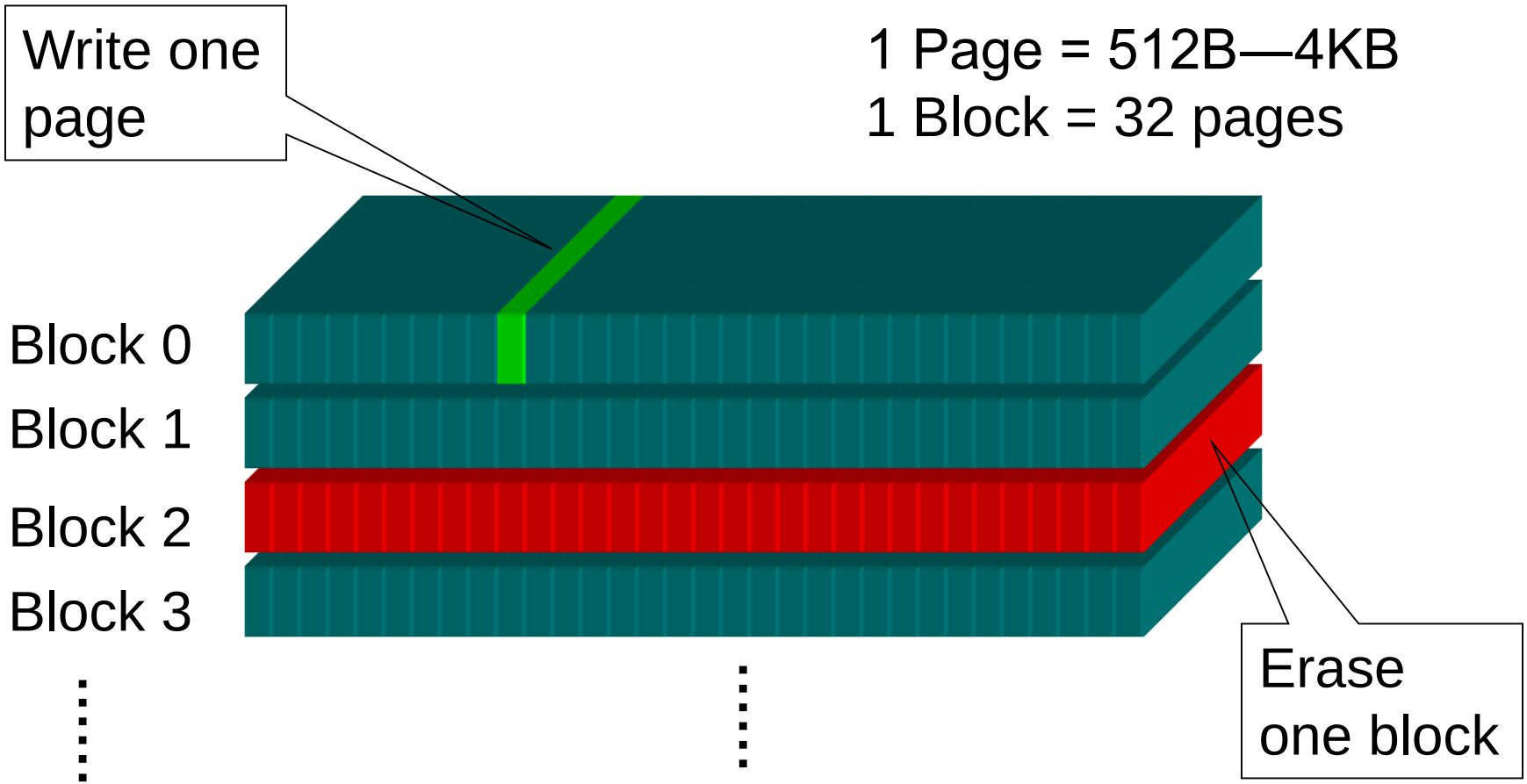
Page Write and Block Erase



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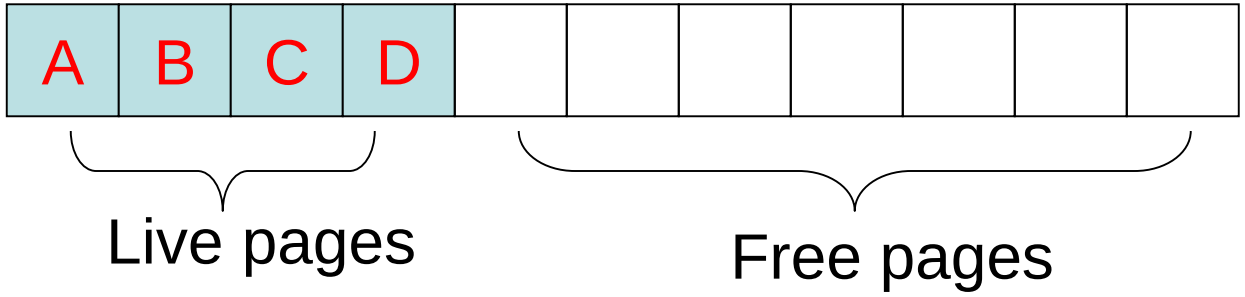
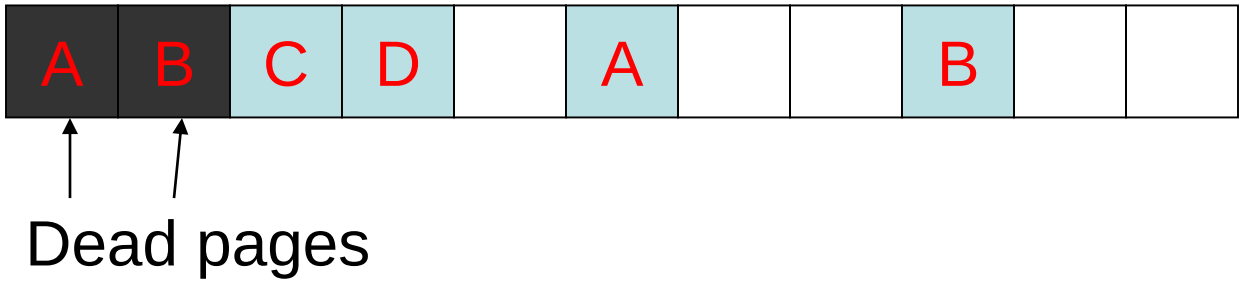
Out-Place Update



Suppose that we want to update data A and B…



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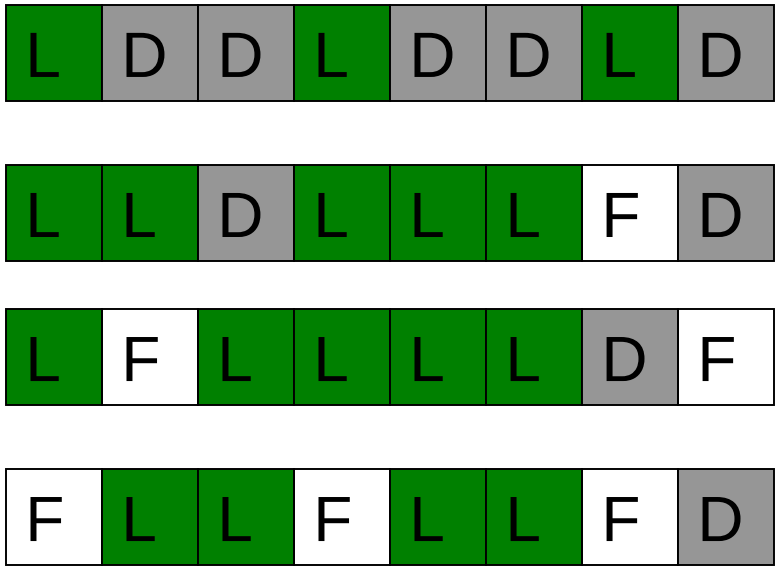
Garbage Collection (1/3)



This block is to be recycled
(3 live pages and 5 dead pages)

- A live page
- A dead page
- A free page

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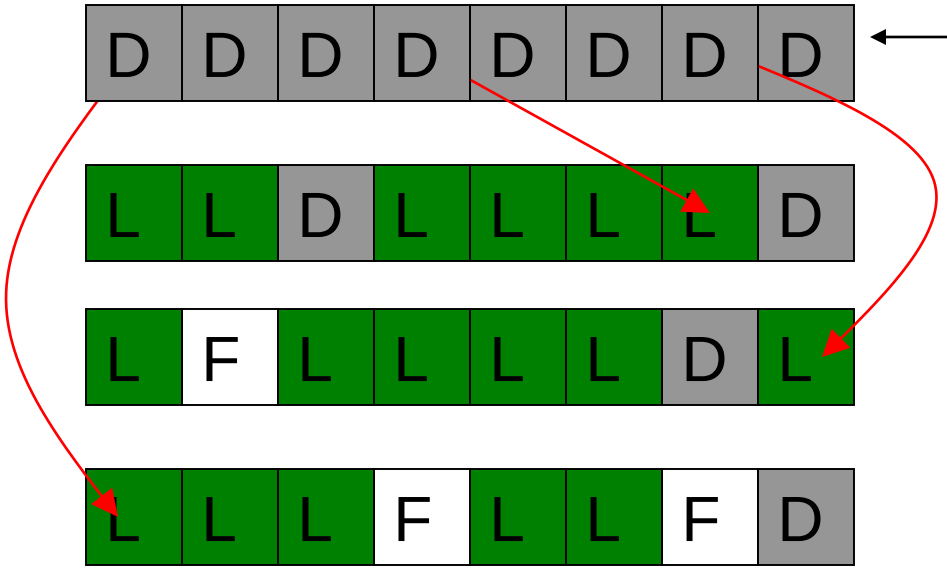
Garbage Collection (2/3)



Live data are copied to somewhere else

A live page

A dead page

A free page

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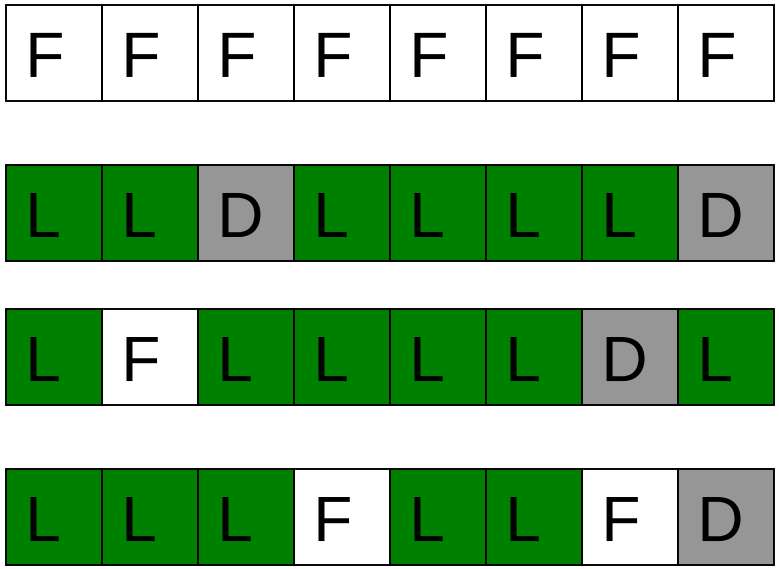
Garbage Collection (3/3)



The block is then erased

Overheads:
- live data copying
- block erasing

A live page
A dead page
A free page

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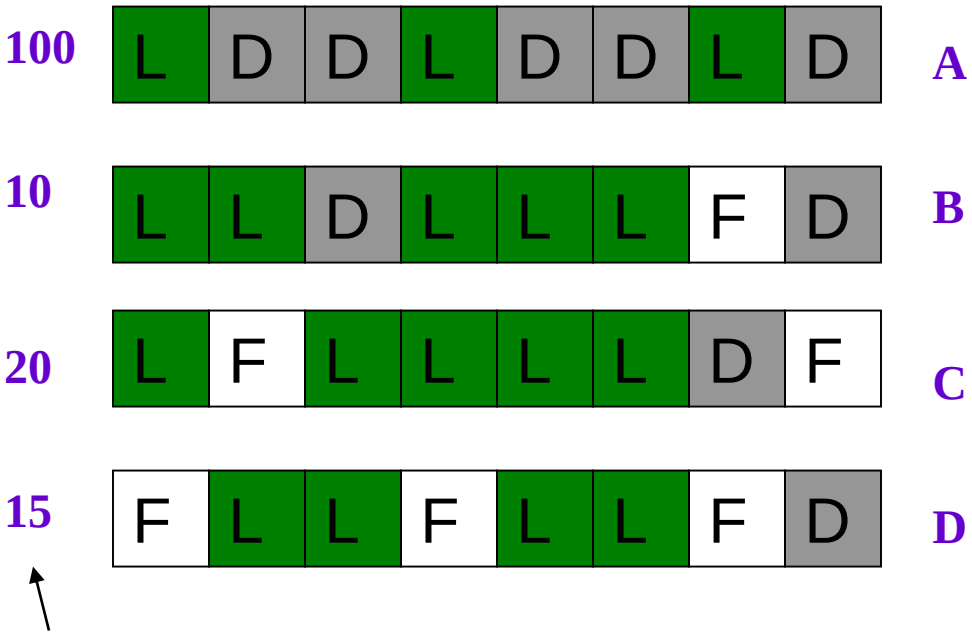
Wear-Leveling



Erase cycle counts

Wear-leveling might interfere with the decisions of the block-recycling policy

- A live page
- A dead page
- A free page

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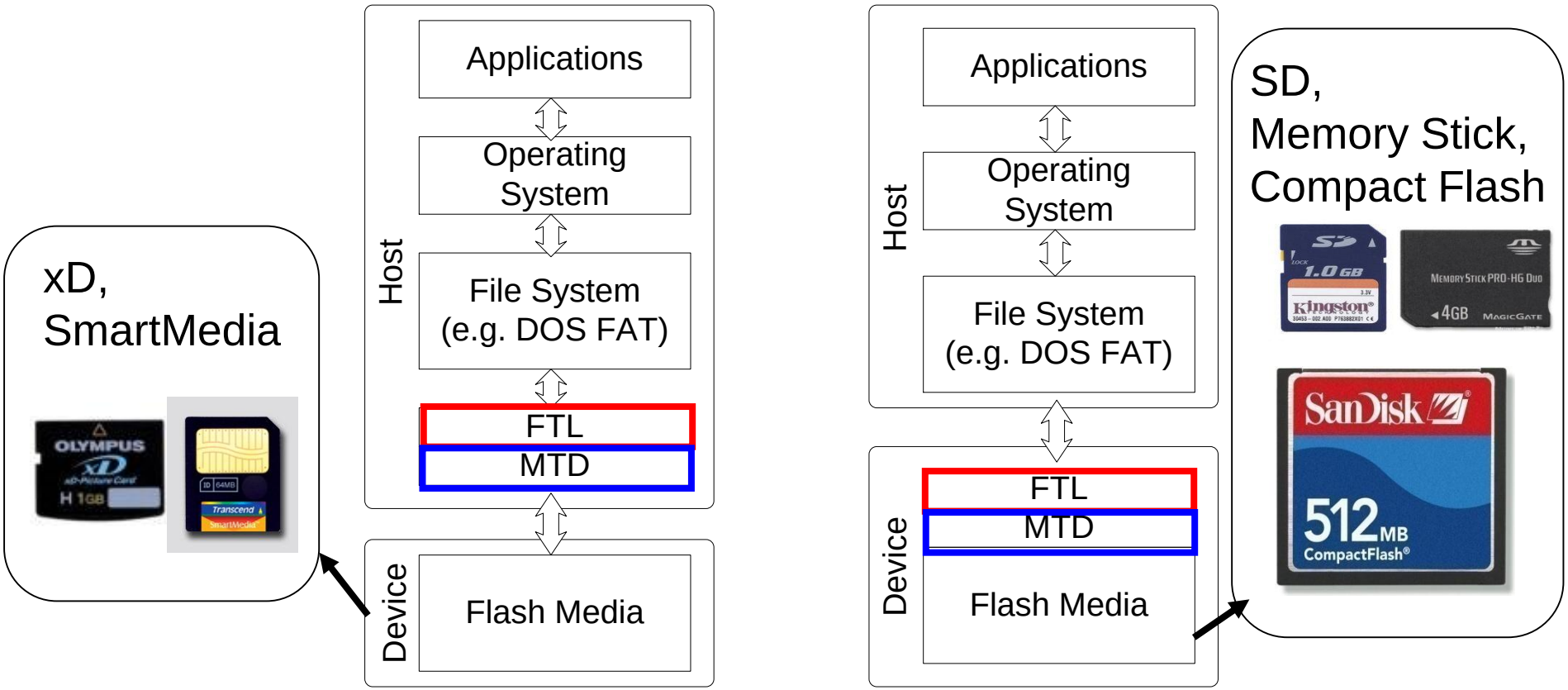
Flash Translation Layer



*FTL: Flash Translation Layer, MTD: Memory Technology Device

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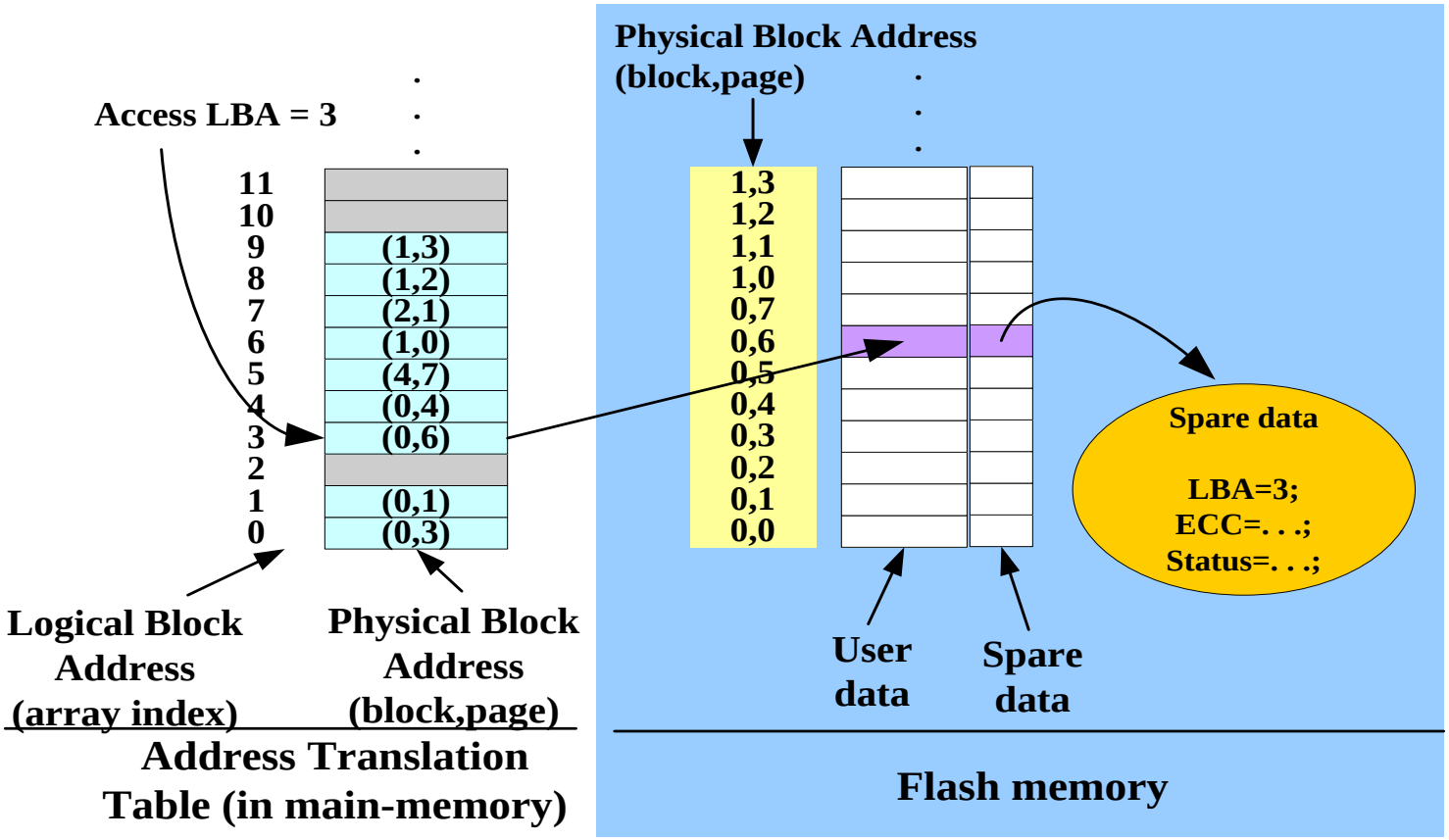
Policies – FTL

- FTL adopts a page-level address translation mechanism



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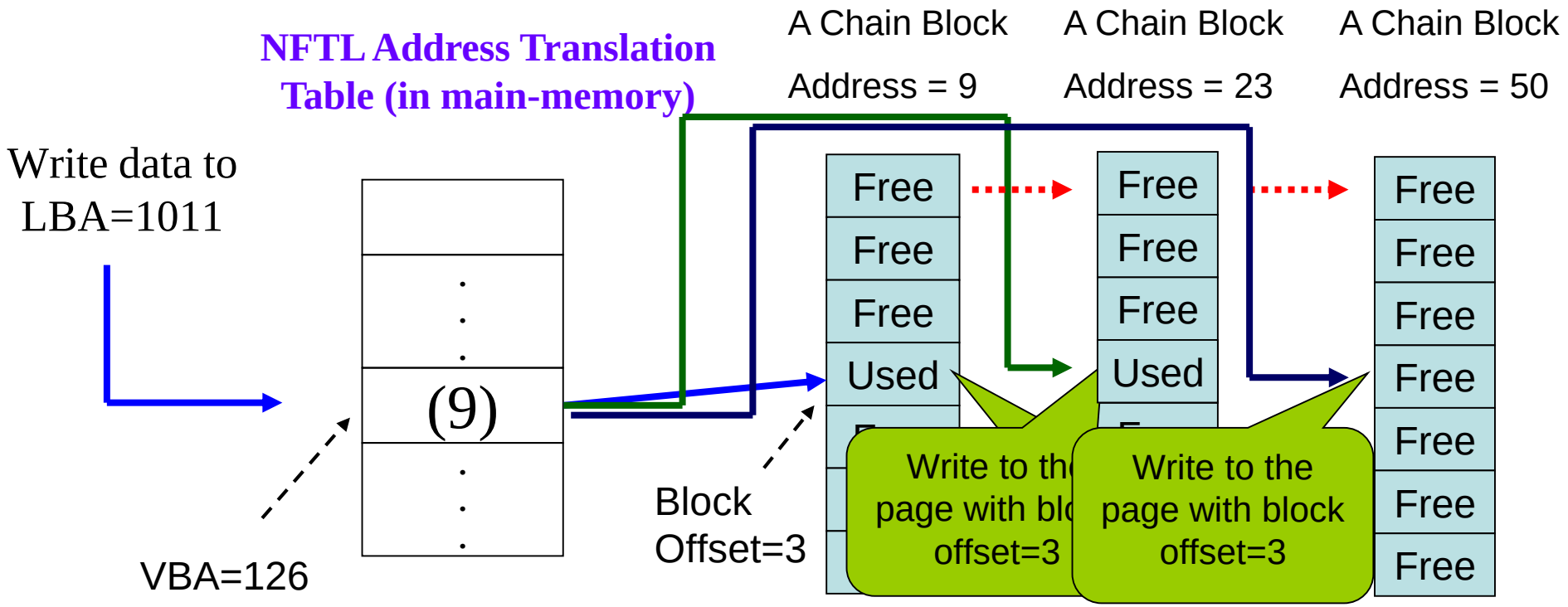
Policies – NFTL (Type 1)

- A logical address under NFTL is divided into a virtual block address and a block offset, e.g., LBA=1011 => virtual block address (VBA) = 1011 / 8 = 126 and block offset = 1011 % 8 = 3



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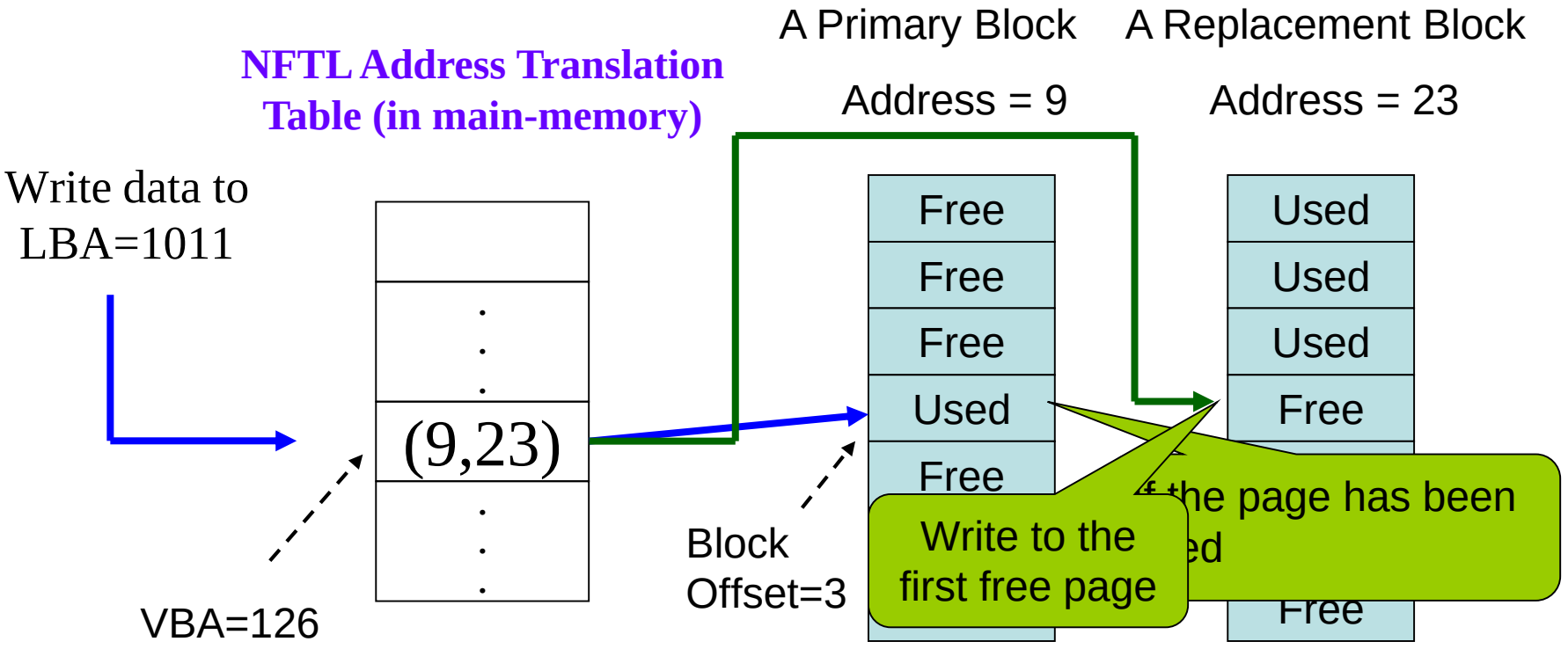
Policies – NFTL (Type 2)

- A logical address under NFTL is divided into a virtual block address and a block offset, e.g., LBA=1011 => virtual block address (VBA) = 1011 / 8 = 126 and block offset = 1011 % 8 = 3



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Challenges and Research Topics of Flash Memory Designs

- Performance
  - Reduce the overheads of Flash management
  - Reduce the access time to data
  - Reduce the garbage collection time
- Reliability
  - Error correcting codes
  - Log systems
- Endurance
  - Dynamic wear-leveling
  - Static wear-leveling

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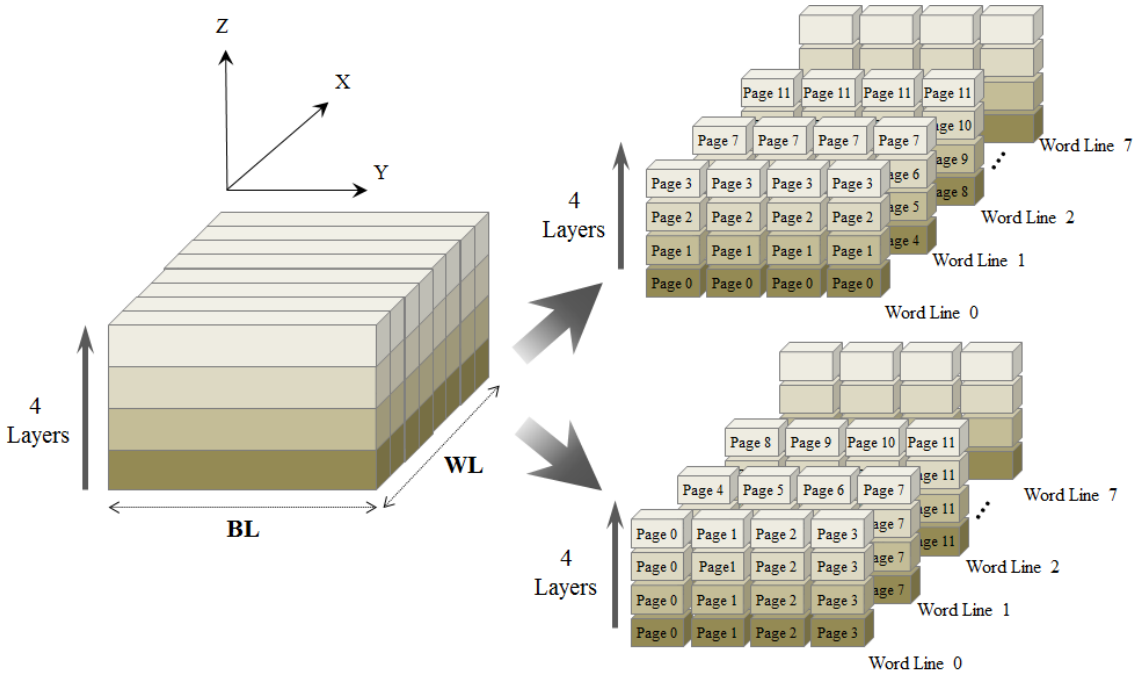
3D Flash Memory

- 3D flash memory provides a good chance to further scale down the feature size and to reduce the bit cost.
  - Deliver very large storage space
  - Worsen program disturbance



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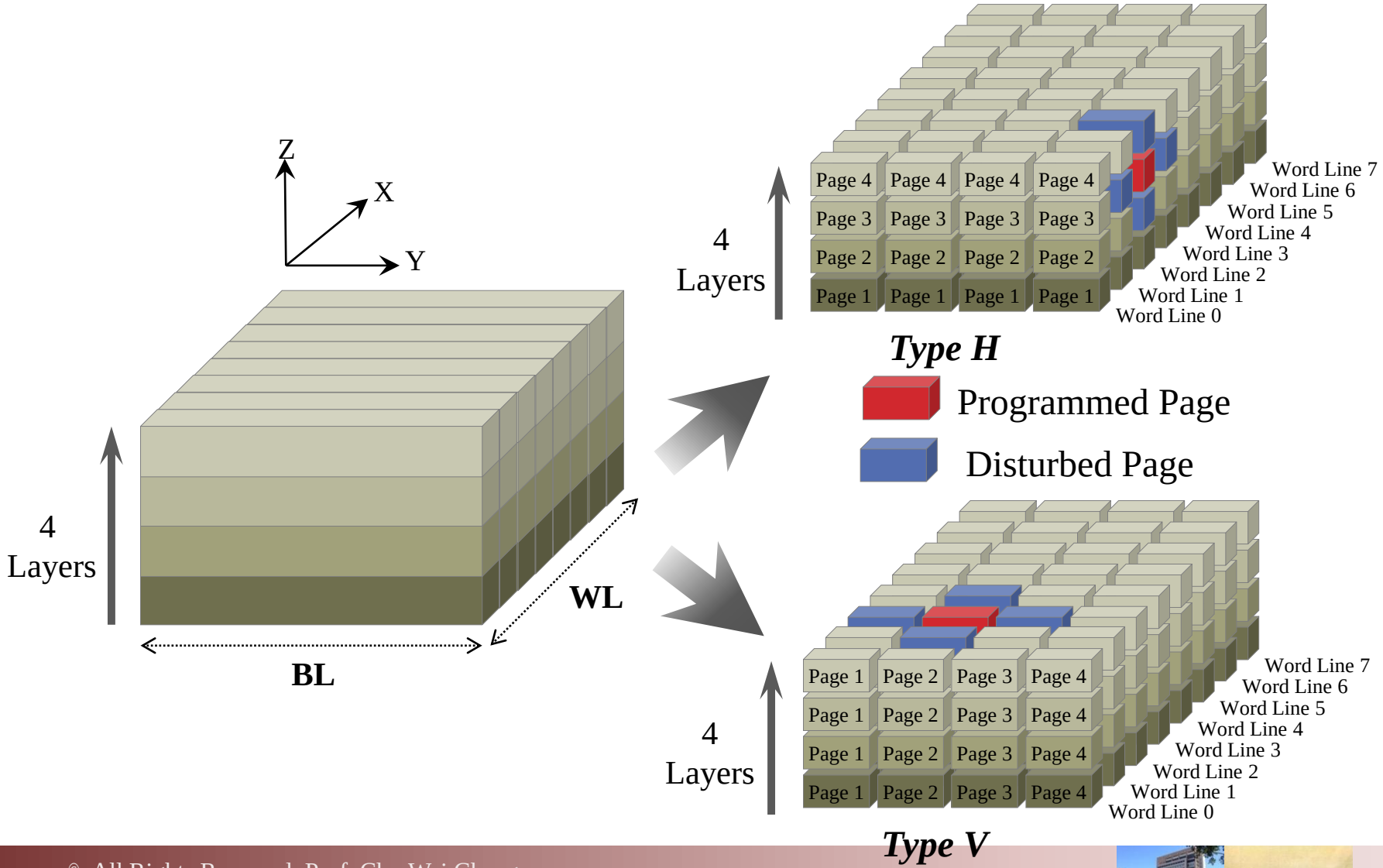
Deteriorated Disturb on 3D Flash



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