Accelerating DICe on FPGA

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1. What is done

1.1. Introduction

As it had been mentioned in the previous report, the main time consuming part of the DICe are the objective functions. The objective functions do the optimization part of the correlations. They iterate through the whole deformed frame to find the equivalent regions of the reference frame in the deformed frame and then find the displacement. It is done using two methods of fast and robust. The fast method is typically an image gradient based method and the robust method is usually simplex based. In these two functions that are called for each subset of the image frames, the intensity values of the whole pixels are compared between the reference and the deformed images. The fast method has a for loop with 25 iterations and the robust method loops through the image 100 times. We assume that there are around 15k frames (as in the sample input) and each frame has 5 subsets with 40*40 pixels. It means that the total number of iterations will be 15k*5*40*40*25=3e9 for the fast method and 12e9 for the robust method. That's why we will start from these functions to accelerate them on the FPGA to have an optimization in the execution time.

1.2. Objective functions

We have started from the fast method and rewrote this function in Verilog. Figure 1 and Figure 2 are the fast method implementation in C++ and also in Verilog. This function is implemented using an FSM-based switch case in an always block to handle the loops with an unfixed loop iteration value. Shon in Figure 3 is the simulation result of this function for a simple 4 * 4 subset. As the waveforms determine, the Correlation_Done is the output of this function that determines the status of the correlation that is done or not.

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return MAX_ITERATIONS_REACHED;
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                               catch(std::exception %e) (

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break;
      // clear up storage for lapack:
delete [] WORK:
delete [] IPIV;
      if(solve_it>max_solve_its)(
return MAX_ITERATIONS_REACHED;
        else return CORRELATION_SUCCESSFUL;
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Figure 1-C++ Code

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Figure 2-Verilog Code

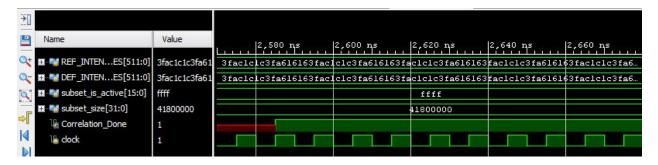


Figure 3- Simulation Results.

To synthesize the design, we have to do some initializations at the upper level modules. The problem is that we have an object oriented C++ code that it should be recoded in Verilog which is a low level language that even does not support 2D arrays as the input port or using the dynamic arrays and loops. We are working on this part now. But to be sure that the function works fine in synthesizing we have tested it with a simple test bench that the data have been initialized by hand not in a hierarchy structure as is in C++ source codes. The left most led in the Vitex 7 FPGA represents the Correlation_Done output signal (like the simulation waveforms).



Figure 4- Synthesize Results.

1.3. Arithmetic functions

Arithmetic operations of the DICe is in ieee754 single precision format. To have them in Verilog, we could use the floating point IP core of the Vivado that implements the basic arithmetic functions or use the present libraries but, most of them are sequential circuits that cannot be implemented as a function and we have to have functions because of their features compared to the modules. Therefore, we used combinational arithmetic cells like adder/subtractor, multiplier, divider, sqrt, sin, cos, asin and acos. For the trigonometric functions the Taylor series has been used to have a linear approximation of these functions. They have been worked for both the simulation and synthesizing for a simple test of reading

two inputs from the BRAM, doing the arithmetic functions and having the results on the FPGA at a 70 MHz frequency.

2. Next steps

- 1. How to have an object-oriented-based code in Verilog!
- 2. Coding the upper level functions, initializing the needed variables and then synthesizing the design.
- 3. Analyzing the execution time of the fast method (including the time of reading the data from BRAM and the execution time of the other functions)
- 4. Coding the robust method.
- 5. Test the design for larger input size data.