Aging Effects on Ring-Oscillator-Based Physical Unclonable Functions on FPGAs

Stefan Gehrer, Sebastien Leger
Robert Bosch GmbH
Stuttgart, Germany
{stefan.gehrer, sebastien.leger}(at)de.bosch.com

Georg Sigl
Institute for Security in Information Technology
Technische Universität München, Munich, Germany
sigl(at)tum.de

***Abstract*—On-Chip Physical Unclonable Functions (PUFs) are a powerful way to generate intrinsic keys by using production tolerances. Robustness of the PUF against reversible environmental changes and irreversible aging effects is crucial for its reliability. The influence of environmental changes is already studied in depth, however, there is still limited research on aging effects. We performed accelerated aging tests on 28 nm Xilinx Zynq FPGAs and compared the impact to reversible environmental fluctuations. Designs with different types of logical stress were used to amplify the effects of various aging mechanisms. The impact of accelerated life conditions on the frequency of different ring oscillator PUFs was measured and analyzed. It was shown that the aging effect is dramatically accelerated with higher temperatures and voltages. The reliability of the PUFs without error correction was still at around 96% after an effective accelerated aging duration of around 31 years. This confirmed that most of the PUFs age similarly and the variations are compensated by using differential measurements. The length of the ring oscillator had no severe influence on its reliability. Our investigations showed that aging effects reduce the reliability in the same order of magnitude as environmental variations.**

***Index Terms*—Aging, Physical Unclonable Functions (PUFs), FPGA, Reliability, Ring oscillator**

I. Introduction

Modern System-on-Chips (SoCs) process and transmit an increasing number of complex sensitive information. The confidentiality and integrity of these data, as well as the authenticity of the devices are very important. Physical unclonable functions (PUFs) are a modern way to create device unique fingerprints or keys [1]–[3]. The sources of randomness are the unpredictable production tolerances of integrated circuits (ICs). The function to extract the entropy is hard to predict, but easy to be evaluated.

Most of the PUFs on ICs are delay-based or memory-based. Delay-based PUFs use the delay variations of the delays of wires and logic directly. This can be done by introducing a race condition between two or more paths with the arbiter PUF [4] or by using frequency differences between two or more ring oscillators (ROs) [2], [5].

The stability of the generated key is crucial for the usability of PUFs. Both reversible and irreversible variations can alter the behavior of the PUF. Environmental conditions, e.g. voltage and temperature, are reversible variations. The effect of the altered conditions disappear once the cause is withdrawn.

Device aging on the other hand is an irreversible variation that leads to a permanently changed behavior.

The effects of aging on RO-based PUFs on an FPGA are analyzed in this paper. The results are then compared to the effects of reversible environmental conditions.

II. Prior Work

Stott et al. [6] analyzed the effect of aging on FPGAs. They did both experimental measurements and theoretical simulations. The FPGA was stressed under different electrical conditions. The accelerated life conditions were very high. An overvoltage of almost 80% above the nominal voltage might lead to other effects than the regular aging mechanisms. Unfortunately, the tests were not PUF specific.

Maes et al. [7] carried out aging tests on several PUFs that were implemented on their own application specific IC (ASIC). The analysis included many different PUF types, but details were missing. Only the fractional Hamming distance as a measurement of stability was given in this work.

A more detailed analysis was carried out by Maiti et al. [8]. Different FPGAs were tested under various higher voltages and temperatures. The electrical stress was induced by the PUF itself. Therefore, only high frequency stress was applied and no other stress condition was tested. The elevated stress conditions were very high with an overvoltage of 66.7%.

We contribute the testing of RO PUFs of various lengths under different elevated aging conditions. This is the first work that was being done with modern 28 nm devices. The FPGA is stressed under five distinct electrical stress types to test their influence on the RO frequency. Additionally, the effects of aging are compared to the ones of reversible environmental changes.

III. Background information

A. Aging mechanisms

Four main types of degradation are relevant for modern ICs [9].

Hot carrier injection (HCI) is the effect that a carrier, which gains sufficient energy, overcomes a potential barrier and is trapped in the oxide layer. This results in an alteration of the transistor characteristics typically increasing the threshold voltage. HCI is amplified by a high frequency switching behavior.

Negative bias temperature instability (NBTI) is a static

978-1-4673-9406-2/15/$31.00

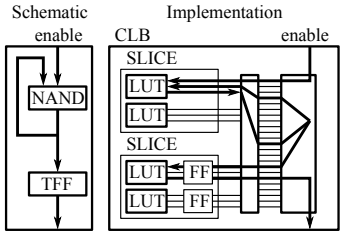


Fig. 1. Schematic and implementation of an RO PUF on an FPGA

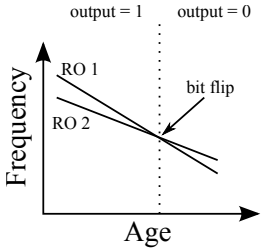


Fig. 2. Bit flip due to the aging of two ROs

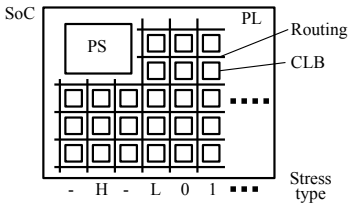


Fig. 3. SoC with PS and PL part, each column of CLBs was stressed under different conditions, H: high frequency stress, L: low frequency stress, 0: DC 0 stress, 1: DC 1 stress

mechanism. Dangling bonds at the interface of the channel and oxide layer develop by applying an electric field across the gate oxide. PMOS transistors are mainly susceptible to this type of stress. The impact on the threshold voltage is usually higher than with HCI. The equivalent mechanism for NMOS transistors, positive bias temperature instability (PBTI), is becoming a bigger concern with the introduction of high-k metal gates.

Temperature-dependent dielectric breakdown (TDDB) is a failure mechanism which is caused by an accumulation of trapped charges or defects across the gate oxide, while an electric field is applied. A conductive path through the dielectric forms, increases the leakage over time, and finally might even prevent the transistor from switching at all.

Electro-migration is an effect in which metal ions migrate over time. High current flows can lead to faulty interconnects.

B. The ring oscillator PUF

RO PUFs were used in this work. Implementing the exact same RO in two different logic blocks on the same IC will result in a slightly distinct frequency. By comparing the frequencies f_i of neighbored ROs, a bit can be produced by using the formula:

$$r(f_i, f_{i+1}) = \begin{cases} 1, & \text{if } f_i > f_{i+1} \\ 0, & \text{otherwise} \end{cases} \quad (1)$$

As the result is device specific, it differs to the exact same implementation on another IC.

The schematic and implementation of a one inverter RO PUF is shown in Fig. 1. Instead of a simple inverter, a NAND gate is used to allow the disabling of the oscillation. By connecting the output of the NAND to its own input and making sure the delay line is long enough, an oscillation will occur. As the resulting frequencies tend to be very high with over 600 MHz, a toggle flip-flop (TFF) is used right after the RO, to halve the frequency. In Fig. 1, one lookup table (LUT) of the upper slice is used to implement the NAND function. The TFF is implemented by using a LUT and a flip-flop (FF) of the lower slice. Each of the RO PUFs used in this work occupies exactly one configurable logic block (CLB).

Two important properties of PUFs are uniqueness and reliability. When measuring the same PUF on the same device, the resulting bit response should always be the same, regardless of environmental conditions or age of the IC. This is referred to as reliability. The Hamming distance (HD) is commonly used as a measure for reliability. It is defined as the number of positions in which two vectors differ. The HD can be divided by the bit width l to get the fractional Hamming distance (FHD):

$$FHD(r_x, r_y) = \frac{HD(r_x, r_y)}{l} = \frac{\sum_{i=1}^{l} [r_{x_i} \neq r_{y_i}]}{l} \quad (2)$$

Measuring the same PUFs on the same device should always yield a HD close to zero. This is referred to as intra-chip HD. Fig. 2 shows a possible effect that can occur due to the aging of a device. In the beginning, the first RO is faster than the second one, thus producing a '1' output. But as the first PUF is aging faster, it becomes slower than the second one throughout the lifetime of the device. This leads to a bit flip and the intra-chip HD rises.

In order to guarantee uniqueness of the PUF, measuring the same PUF implementation on different ICs should yield a FHD close to 0.5, i.e. they differ in exactly half of their positions. This is commonly referred to as inter-chip HD.

The distribution of ones and zeros in a PUF response is measured using the Hamming weight (HW). It is defined as the sum of all bit positions of a vector. By dividing the HW by the number of bits l, we get the fractional Hamming weight (FHW):

$$FHW(r_x) = \frac{HW(r_x)}{l} = \frac{\sum_{i=1}^{l} [r_{x_i}]}{l} \quad (3)$$

A good and random PUF output should always have a FHW close to 0.5, i.e. an equal amount of ones and zeros.

IV. Method

A. Stress design

In this work we will use an SoC consisting of a processor system (PS) part and a programmable logic (PL) part. Common examples are the Xilinx Zynq or the Altera SoCs. The

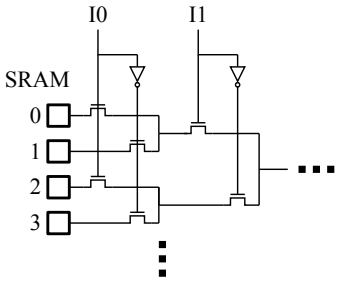


Fig. 4. Structure of a LUT using NMOS pass transistors

general structure of the SoC is shown in Fig. 3. The PL part consists of several CLBs and a complex routing structure. As previously described, the CLBs were used to implement the ROs. In order to age them in various ways, we used different electrical stress types. The SoC in Fig. 3 was separated into columns, each of which was stressed with one of the five stress types. By having the same type of stress at various positions on the FPGA, we were also able to measure spatial dependence of the aging. Five different types of electrical stress were used: *DC 0* stress (constant zero), *DC 1* stress, *low* frequency stress, *high* frequency stress, and *'no'* stress. To lower the impact of the *high* frequency stress on the other stress types, they were surrounded by *'no'* stress columns. After that followed a *low* frequency, a *DC 0* stress and a *DC 1* stress zone. This pattern was repeated on the whole FPGA. Each CLB in a column was stressed with the same electrical stress.

To understand how the stress designs work, it is important to know the rough structure of a LUT. Fig. 4 shows the implementation of a LUT using NMOS pass transistors. This is the most used implementation in modern devices because it consumes less area than using transmission gates [10]. However, the exact implementation of the LUTs are being kept secret by the vendors. Therefore, instead of modeling the aging of the LUT, we perform real measurements.

The LUT values are stored in a static random-access memory (SRAM). In this work, 6 bit LUTs are used, i.e. 64 SRAM cells are needed to store the LUT information. The SRAM values of all LUTs are usually written when loading the configuration design of the FPGA. They don't change their value during runtime unless partial reconfiguration is used. The SRAM values propagate through a multiplexer (MUX) network that is controlled by the inputs I0 to I5 for a 6 bit LUT. Measurements for the FPGA used in this work confirmed that the input pin I0 is closest to the SRAM cells and farthest from the output of the LUT. For the sake of simplicity, extra buffer stages and level restorers, which are commonly found in real implementations, are left out here. The usage of pass transistors is the reason why modern FPGAs have more NMOS than PMOS transistors. The various stress designs used both SRAM entries and the input signals in distinct ways. The *DC 0* and *DC 1* stress designs set all entries of the SRAM cells to '0' resp. '1' and had a constant input on all pins of '0' resp. '1'. The constant SRAM values were propagated all the way through the LUT. Due to the inverter sketched in Fig. 4, some of the NMOS transistors still had an inverted signal applied at their gate. The *low* and *high* frequency stress designs used alternating static entries in the SRAMs (0,1,0,1...), such that every inversion of the I0 signal led to a bit flip at the output of the LUT. A 6 bit counter was connected to the input signals I0 to I5, where I0 was connected to the least significant bit. Every time the counter was incremented, the output bit of the LUT was changed. The *'no'* stress design demonstrated an unused LUT, that was initialized by the synthesis tool. The flip-flops that followed the LUT stage were all equally stressed according to their stress type.

The various electrical stress designs accelerated different types of aging effects. The *DC 0* and *DC 1* stress had a strong static effect, but no dynamic effect. This should result in a large NBTI/PBTI and TDDB, but only a small HCI effect. As NBTI is still the dominant effect in modern ICs [11], a *DC 0* stress should have more influence on the aging than a *DC 1* stress. The *low* frequency stress balanced between a moderate static and dynamic effect. The *high* frequency stress had a large dynamic effect, but only a very small static effect. The impact of the *'no'* stress design was unknown, as it was initialized by the synthesis tool.

B. Accelerated environmental conditions

In order to accelerate the degradation of the IC significantly, elevated environmental conditions were used. In contrast to previous papers [6], [8] the accelerated conditions were kept within the absolute maximum ratings of the vendor. The temperature acceleration factor AF_T can be calculated to [9], [12]:

$$AF_T = e^{\frac{E_a}{k}(\frac{1}{T_{op}} - \frac{1}{T_{stress}})} \tag{4}$$

with T_{op} as the normal operation junction temperature, T_{stress} as the stress condition temperature, $E_a = 0.7$ the activation energy, and $k = 8.62 \cdot 10^{-5} eV/K$ the Boltzmann constant.

The acceleration factor due to higher voltage AF_V can be calculated to:

$$AF_V = e^{(\gamma(V_{stress} - V_{op}))} \tag{5}$$

with V_{op} as the normal operation voltage, V_{stress} as the elevated voltage, and $\gamma = 2.0$ as the voltage exponent factor [12]. The product of AF_T and AF_V yields the total aging factor.

V. Results

A. Implementation and setup

Four 28 nm Xilinx Zynq XC7Z020 were aged in this work [13]. The absolute maximum voltage for the PL part was 1.1V, which equals an over-voltage of 10%. The maximum junction temperature was given as $125\,^{\circ}\mathrm{C}$. Two of the devices were aged by only using an elevated ambient temperature. The junction temperature under stress was measured to $T_{stress} = 85\,^{\circ}\mathrm{C} = 358\,^{\circ}\mathrm{K}$ and the normal temperature to $T_{op} = 55\,^{\circ}\mathrm{C} = 328\,^{\circ}\mathrm{K}$. This yielded an acceleration factor of:

$$AF_{low} = AF_{T_{low}} = e^{\frac{E_a}{k}(\frac{1}{328K} - \frac{1}{358K})} = 7.96 \tag{6}$$

For a test duration of 120 days we could calculate an effective accelerated aging duration of: $120\,\mathrm{d} \cdot 7.96 = 2.61\,\mathrm{years}$.
The other two devices were aged under the maximum operating conditions of $T_{stress} = 125\,^{\circ}\mathrm{C} = 398\,^{\circ}\mathrm{K}$ and $V_{Stress} = 1.1V$. This yielded an acceleration factor of:

$$AF_{T_{high}} = e^{\frac{0.7}{k}(\frac{1}{328}-\frac{1}{398})} = 77.82 \quad (7)$$

$$AF_{V_{high}} = e^{(\gamma(1.1-1))} = 1.22 \quad (8)$$

$$AF_{high} = AF_{T_{high}} \cdot AF_{V_{high}} = 95.05 \quad (9)$$

For a test duration of 120 days we could calculate an effective accelerated aging duration of: $120\,\mathrm{d} \cdot 95.05 = 31.25\,\mathrm{years}$.
The sequence in which the devices were stressed and the PUFs measured can be separated in six steps:

1) Load stress design, elevate ambient temperature (and voltage if applicable)
2) Wait for six hours
3) Apply normal conditions of 1.0V and 25 °C ambient temperature, load blank FPGA design
4) Wait for the device to cool down
5) Measure PUFs

This cycle was performed continuously for four months, including two single day breaks to test the effect of regeneration. The ambient temperature was controlled by a climate chamber and stayed at the same levels throughout the whole test. The supervision of the test was performed by the PS part of the SoC. This included programming the FPGA, performing the measurement of the PUFs, storing the test results, changing the voltage of the FPGA, and monitoring the test.
RO PUFs of different lengths were investigated in this work. Besides the RO PUF of Fig. 1, we also implemented ROs with three and five inverters. This gave an insight whether the length of the RO was important for its reliability. A higher length would lead to a lower frequency oscillation. The PUFs were thoroughly constrained and placed on the device. This guaranteed that each PUF implementation on the FPGA was exactly the same and only the production tolerances were the reason for frequency differences. Each PUF type was placed on every of the 5328 available CLBs on the FPGA. As two ROs generate a one bit output, we measured a 2664 bit long key per PUF type. During measurement only one RO was activated at a time to avoid influences on neighbored ROs. During stress operation the *low* frequency was chosen to 100 Hz and the *high* frequency to 300 MHz.
To compare the results of the elevated degradation to the influence of reversible environmental conditions, we also measured the frequency of the oscillators at voltages from 0.9 V to 1.1 V and ambient temperatures from -30 °C to 70 °C.

B. Experimental results and discussion

Fig. 5 shows the comparison of the boards that were aged using the maximum operation conditions (high V/T), and the ones that were just aged under a higher ambient temperature (low V/T). It can be seen that the aging was significantly accelerated using the higher voltage and temperature. The frequency under high V/T stress dropped to around 99% after

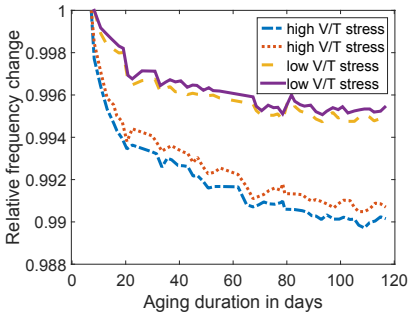


Fig. 5. Degradation of the frequency of ROs using different environmental stress conditions, median value over all tested ROs

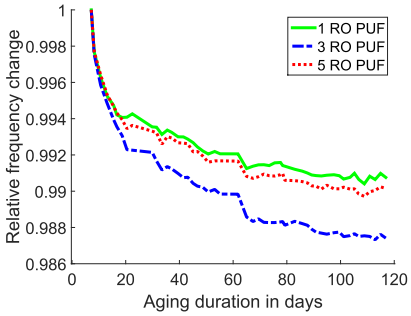


Fig. 6. Impact of amount of inverters in RO on the frequency degradation, median value over all tested ROs

4 months, whereas the low V/T stress conditions only led to a decrease to 99.5%. The degradation of the frequency was very fast during the first few days and slowed down towards the end of the experiments. The two regeneration phases led to a temporary increase of the frequency. As the devices were cooled down every six hours, the influence of a one day regeneration phase was not high. In the following analyses, only the boards aged under high V/T conditions are analyzed.
Fig. 6 shows the relative frequency change of the different PUF types. It can be seen that the degradation process was slightly different for all lengths of PUFs. In this case, it was not the shortest PUF that aged the fastest, but the 3 RO PUF. This might be due to the exact implementation of the PUF, which might use more hidden PMOS transistors than the other PUF implementations.
Fig. 7 shows a comparison of the different electrical stress types that were used. In our experiment, the *DC 1* stress led to the lowest frequency change, whereas the *low* frequency stress had the highest impact. The relatively low impact of the *DC 1* stress was consistent with the results of previous research [6]. This type of stress enabled the smallest number of PMOS transistors, which lowered the impact of the NBTI. As no dynamic effects occurred, the impact of HCI was also very low. The susceptibility of NMOS transistors to PBTI is increasing with the usage of high-k gates. Nevertheless, using this 28 nm device, we couldn't confirm this trend for this experiment. The *DC 0* stress enabled more PMOS transistors and had therefore a higher frequency degradation effect than

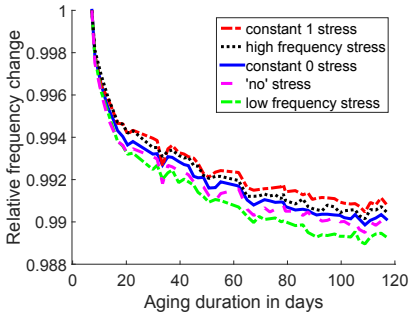


Fig. 7. Impact of the electrical stress type on the frequency degradation

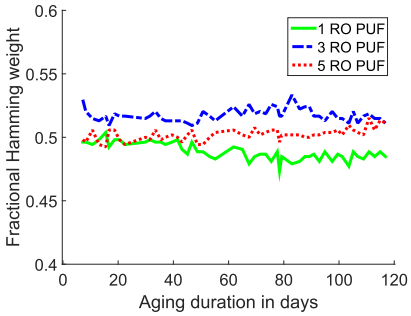


Fig. 9. Impact of the aging process on the Hamming weight of the PUFs

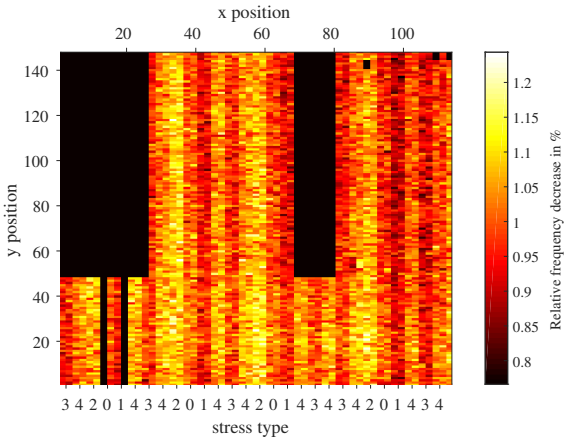


Fig. 8. Map of the FPGA illustrating the influence of different electrical stress conditions on the frequency degradation. Each column was equally stressed. 0: DC 0, 1: DC 1, 2: low frequency, 3: high frequency, 4: no stress

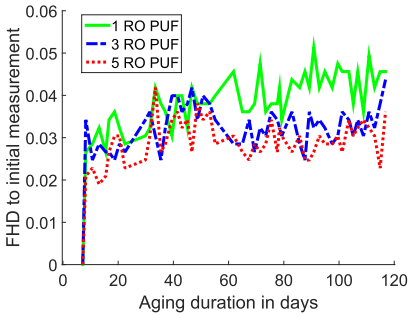


Fig. 10. Impact of the aging process on the reliability of the PUFs measured with the intra-device Hamming distance

DC 1 stress. The *low* frequency stress combined both aging effects of dynamic and static stress. It oscillated fast enough to induce HCI effects, and still spent sufficient time in stable '0' and '1' states to enable NBTI/PBTI effects. It is interesting that the *high* frequency stress showed a smaller impact than the *low* frequency stress. This might be due to the relatively high frequency, where the transistors did not spend much time in stable '1' states, thus lowering the impact of NBTI. An absolute difference of around 0.19% was measured between the most and least severe electrical stress types. The results could be confirmed on all measured boards. The relatively small difference between *DC 0* and *DC 1* stress could be explained by the structure of the LUT. Due to the inverters, half of the NMOS transistors were enabled and the other half were disabled, no matter which stress type was used. Just the inverters themselves and the buffers were differently stressed when using *DC 0* and *DC 1* stresses.

Fig. 8 visualizes the different speed of frequency degradation on the FPGA. It can be seen that the columns with the *DC 1* stress are the darkest, i.e. they had the lowest frequency change and therefore had the highest frequency. In contrary, the *low* frequency stress columns appear the brightest. It can also be seen that the areas in the upper right corner aged slower than the rest of the chip. The location of the ARM core in the upper left corner might be the reason for this, as it heated up the device additionally.

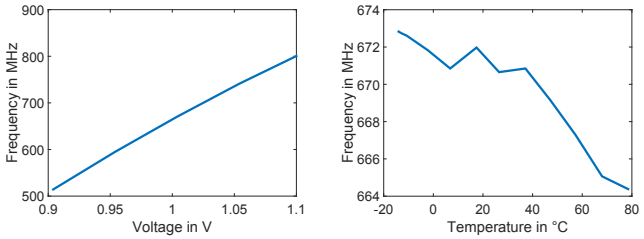
In order to achieve good uniqueness of the PUF, a FHW close to 0.5 is important. Fig. 9 shows the Hamming weight of the PUF output throughout the aging process. It can be seen that FHW remained constantly close to the ideal value 0.5 for all three PUF implementations.

An intra-device HD close to 0 is important for a stable PUF output. Fig. 10 shows the FHD of each measurement referenced to the initial measurement. The FHD reached a level of 3% very quickly for all three PUF implementations. After the burn-in phase, it stabilized at a value of around 3.5-4.5%. The shortest PUF with only 1 inverter showed a slightly higher FHD than the other implementations. This suggests that ROs with slower frequencies, due to more involved transistors, lead to slightly more stable PUF outputs. The impact of a single transistor with a large delay is being compensated.

To ensure a good inter-device HD, all PUF implementations were additionally measured on ten different devices independent from the aging experiment. The measurements showed good FHD close to the ideal value 0.5 for all PUFs between all devices. The worst value was measured to 0.47, which is still acceptable to ensure uniqueness of the PUF implementations. Aging did not affect this property as the results remained constant throughout the experiment.

C. Effects of reversible changes

Fig. 11 shows the effect of varying environmental conditions on the RO frequency. An almost linear change of frequency

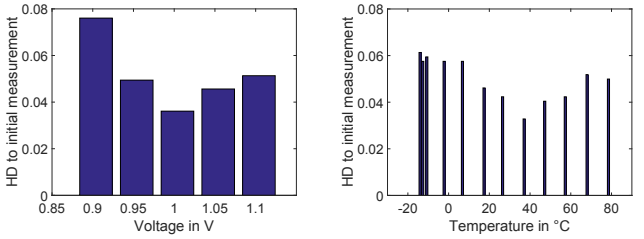


(a) Variations of voltage (b) Variations of temperature

Fig. 11. Dependence of the frequency for variations of reversible environmental conditions

can be seen for both temperature and voltage variations with some exceptions in the lower temperature areas. The frequency dropped at a junction temperature of $-13\,^{\circ}\mathrm{C}$ to $78\,^{\circ}\mathrm{C}$ by around 9 MHz. This was comparable to the frequency change induced by the aging experiment where the frequency dropped by around 10 MHz. Changing the voltage within the vendor specified ranges had a larger impact. The frequency changed by almost 300 MHz when varying the voltage from 0.9 V to 1.1 V.

Fig. 12 shows the effect of voltage and temperature variations



(a) Variations of voltage (b) Variations of temperature

Fig. 12. Dependence of the reliability for variations of reversible environmental conditions

on the reliability of the PUF. The measurements were made at the end of the aging process. The reference values were taken before the aging process. The HD of around 3.7% at 1 V in Fig. 12a and 3.5% at $37\,^{\circ}\mathrm{C}$ in Fig. 12b were caused by the aging itself. It can be seen that an additional variation of the voltage led to a FHD of almost 8%, effectively doubling the unreliability of the PUF. Applying a voltage to the FPGA below the recommended operation voltage was worse for the reliability of the PUF than applying a higher voltage. Nevertheless, the FHD was still acceptable considering that the frequency changed by around 25% from 1.0 V to 0.9 V.

The influence of temperature on the reliability of the PUF can be seen in Fig. 12b. Cooling down the device led to a slightly higher FHD than heating it up. An additional FHD of around 2.5% was measured at temperatures below the freezing point. At a temperature level of +/- $10\,^{\circ}\mathrm{C}$ around the normal operation temperature, a FHD of 1% was measured.

For the devices tested in this work, the influence of reversible environmental changes were comparable to the ones caused by the irreversible degradation process.

VI. Conclusion

We studied the impact of irreversible aging effects on the frequency of ROs in this paper. These frequencies were used to generate binary responses of PUFs and analyze their stability throughout the aging process. It was shown that four months accelerated aging, which equals an effective aging duration of around 31 years, lowered the reliability of 28 nm FPGA-based RO PUFs to around 96%. As the highest frequency degradation occurs during the beginning of the lifetime of a device, a burn-in phase before initializing the PUF can lower the instability problem. The uniqueness property of the PUFs remained valid with FHWs close to 0.5 and inter-chip distances close to 0.5. By applying reversible environmental changes like temperature or voltage to the device, an additional FHD of around 4% was measured. This lowered the reliability to a minimum of 92%. Neither the type of logical stress on the FPGA, nor the length of the PUF itself effected the reliability of the PUFs severely. In a future work, more devices should be tested to back these assumptions.

The effects of reversible and irreversible frequency variations can be completely compensated by using error correction algorithms. This ensures a reliable behavior of the PUF throughout the lifetime of the device. The results in this work can be used to choose an appropriate error correction algorithm.

References

[1] R. Pappu, B. Recht, J. Taylor, and N. Gershenfeld, "Physical one-way functions," *Science*, vol. 297, no. 5589, pp. 2026–2030, 2002.

[2] B. Gassend, D. Clarke, M. van Dijk, and S. Devadas, "Silicon physical random functions," in *Proceedings of the 9th ACM conference on Computer and communications security*, ser. CCS '02. Washington, DC, USA: ACM, 2002, pp. 148–160.

[3] G. Suh and S. Devadas, "Physical Unclonable Functions for Device Authentication and Secret Key Generation," in *Design Automation Conference, 2007. DAC '07. 44th ACM/IEEE*, 2007, pp. 9–14.

[4] J. Lee, D. Lim, B. Gassend, G. Suh, M. van Dijk, and S. Devadas, "A technique to build a secret key in integrated circuits for identification and authentication applications," in *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*, Jun. 2004, pp. 176–179.

[5] A. Maiti and P. Schaumont, "Improved Ring Oscillator PUF: An FPGA-friendly Secure Primitive," *J. Cryptol.*, vol. 24, no. 2, pp. 375–397, Apr. 2011.

[6] E. A. Stott, J. S. Wong, P. Sedcole, and P. Y. Cheung, "Degradation in FPGAs: measurement and modelling," in *Proceedings of the 18th annual ACM/SIGDA international symposium on Field programmable gate arrays*. ACM, 2010, pp. 229–238.

[7] R. Maes, V. Rozic, I. Verbauwhede, P. Koeberl, E. Van der Sluis, and V. van der Leest, "Experimental evaluation of Physically Unclonable Functions in 65 nm CMOS," in *ESSCIRC (ESSCIRC), 2012 Proceedings of the*. IEEE, 2012, pp. 486–489.

[8] A. Maiti and P. Schaumont, "The Impact of Aging on a Physical Unclonable Function," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 9, pp. 1854–1864, Sep. 2014.

[9] N. H. E. Weste and D. M. Harris, *CMOS VLSI design: a circuits and systems perspective*, 4th ed. Boston: Addison Wesley, 2011.

[10] C. Chiasson and V. Betz, "Should FPGAS abandon the pass-gate?" IEEE, Sep. 2013, pp. 1–8.

[11] S. Zafar, Y. Kim, V. Narayanan, C. Cabral, V. Paruchuri, B. Doris, J. Stathis, A. Callegari, and M. Chudzik, "A Comparative Study of NBTI and PBTI (Charge Trapping) in SiO2/HfO2 Stacks with FUSI, TiN, Re Gates." IEEE, 2006, pp. 23–25.

[12] Altera, "Reliability Report 58," 2014.

[13] "Zynq-7000 All Programmable SoC): DC and AC Switching Characteristics," Feb. 2015.