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Accelerating DICe on an FPGA

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Advisor: David Andrews
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Thank You for Supporting this Project!

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Advisor: Dr. David Andrews

Accomplishments to Date

HDL Implementation

- **Beta version nearly finished**
  - Need guidance on data output format to complete last IP
  - FPGA inputs & outputs need to be established
- **Current system processing is about 1/100th to scale**
  - Parameter/BRAM/etc scale up required to handle full image size and increased frame count
  - Core functionality complete. Not all DICe's functionality accounted for yet
- ***Not fully functional yet!***

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What We've Accomplished

Design

- **DICe software split into multiple IP's**
  - Each IP handles a specific function
  - Design Modularized to support future development
- **State machine structured IP's**
  - FSM's enable more control over operations
  - Promotes better scalability and performance
- **Floating-point function improvements**
  - Removed the "function" keyword; caused timing errors and constraints
  - Building functions as FSM's yielded major clock speedup
  - Previous clock speed: <30 MHz; Current clock speed: 150 MHz

What We've Accomplished

MicroBlaze

- **The Xilinx soft processor is the powerhouse within the system**
  - Global system controller
  - Allows introduction of operating system, middleware, device drivers
  - Helps to debug the system
- **AXI4 Lite Standard Bus**
  - MicroBlaze controls the system-wide AXI4-Lite bus
  - Allows for processor control over each individual IP
  - Speeds up testing by bypassing other IP's
- **Ethernet Driver**
  - MicroBlaze will control the Ethernet that streams the FPGA's inputs

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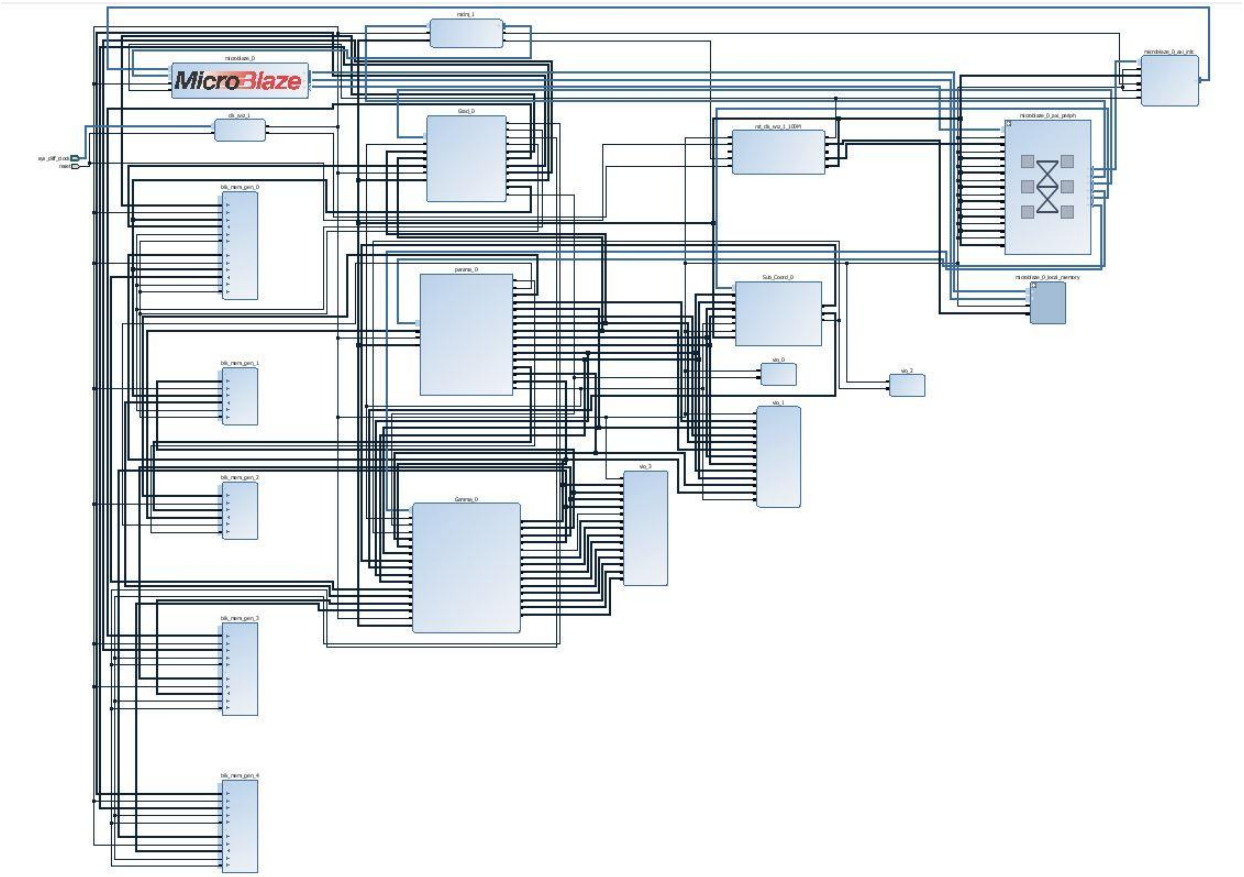
Vivado Block Design



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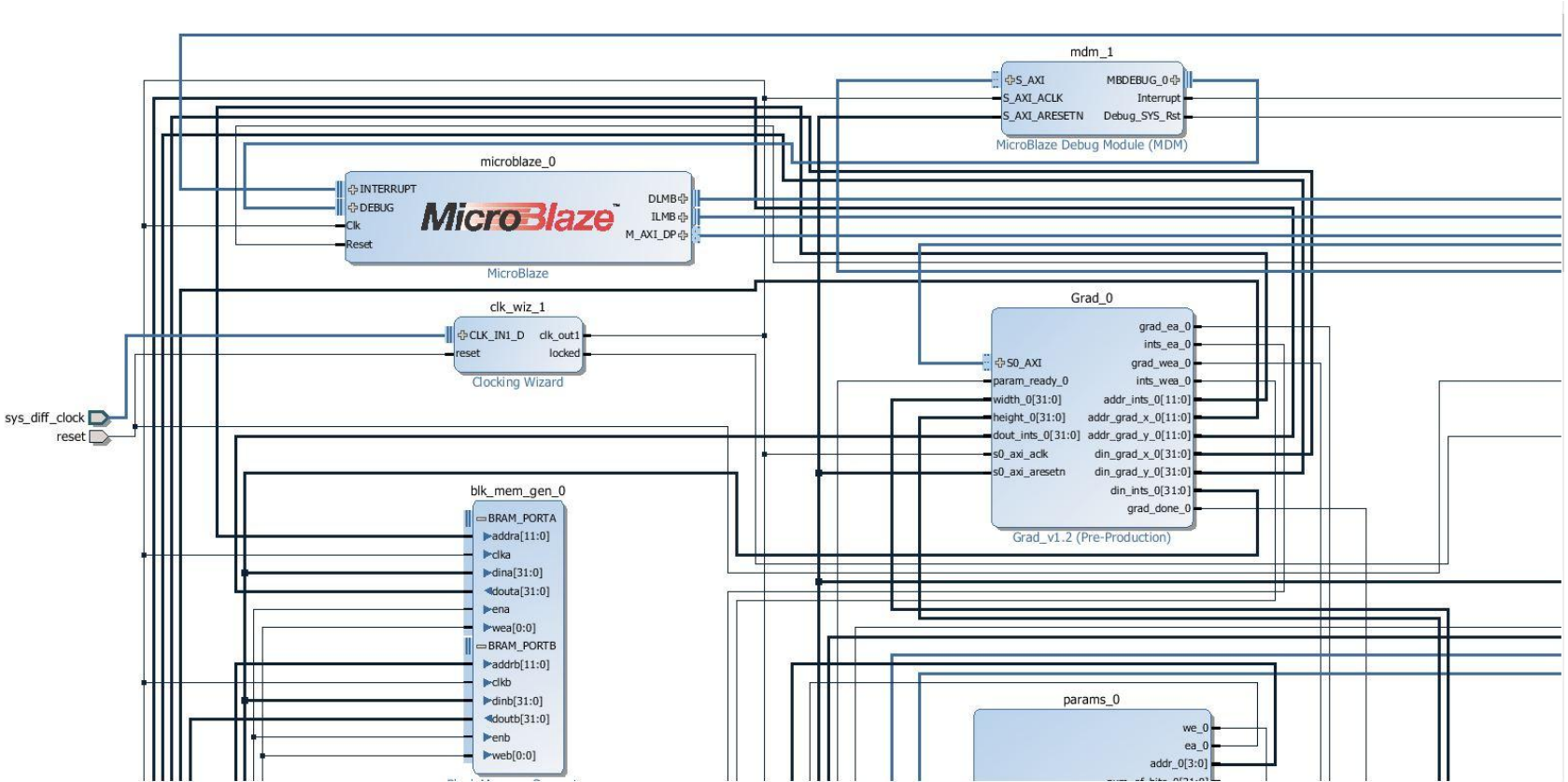
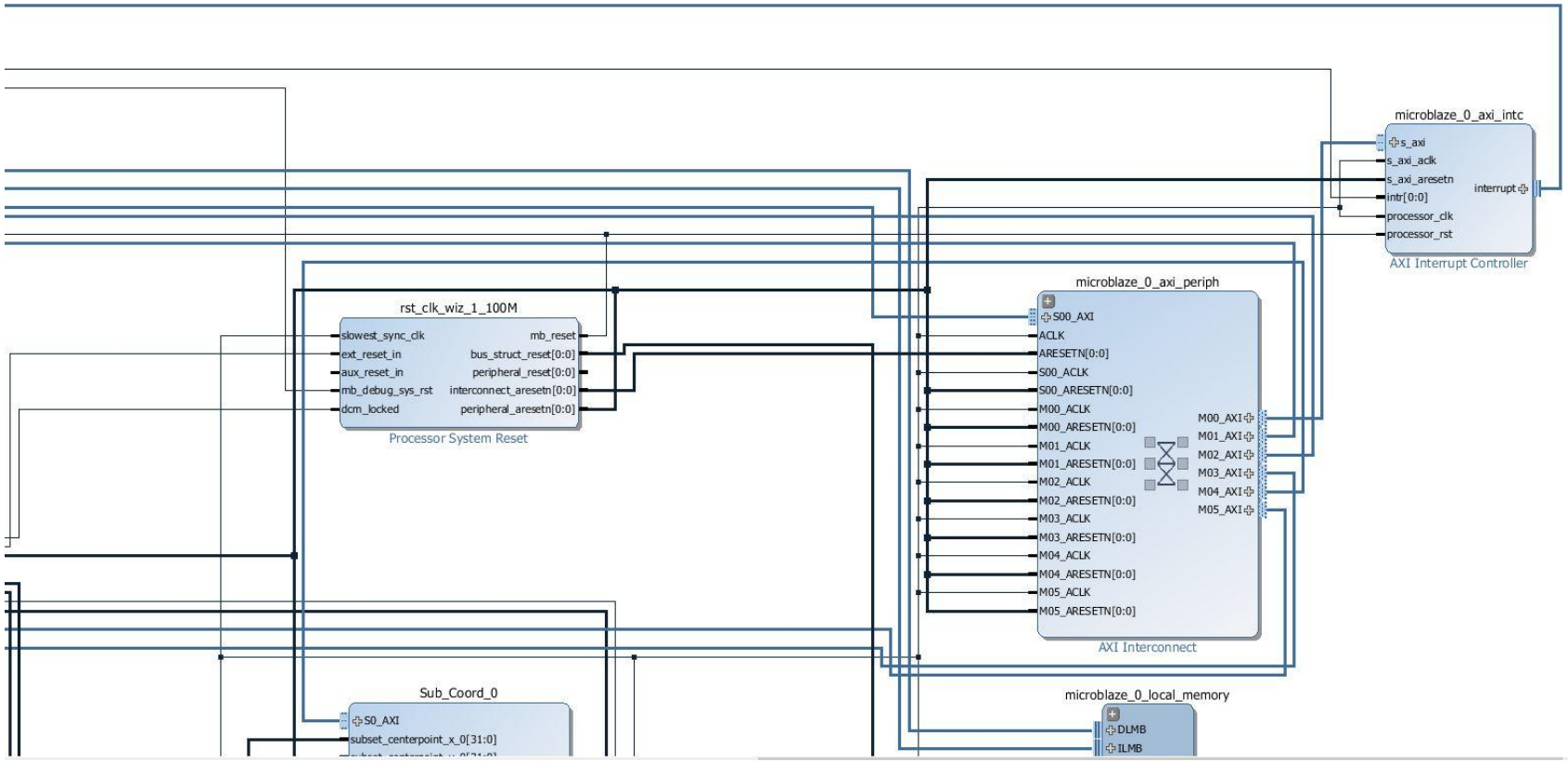
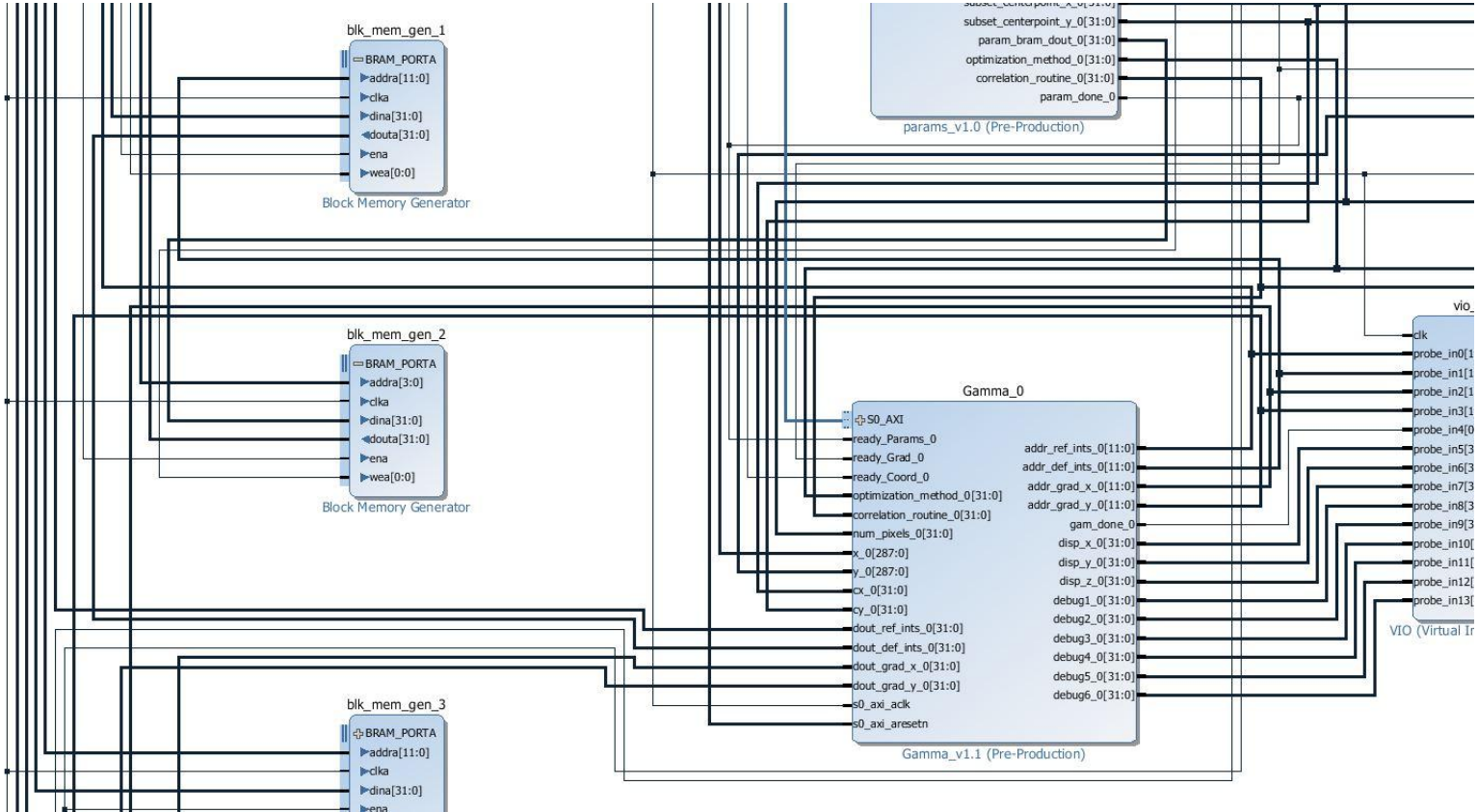
Vivado Block Design



Vivado Block Design



Vivado Block Design



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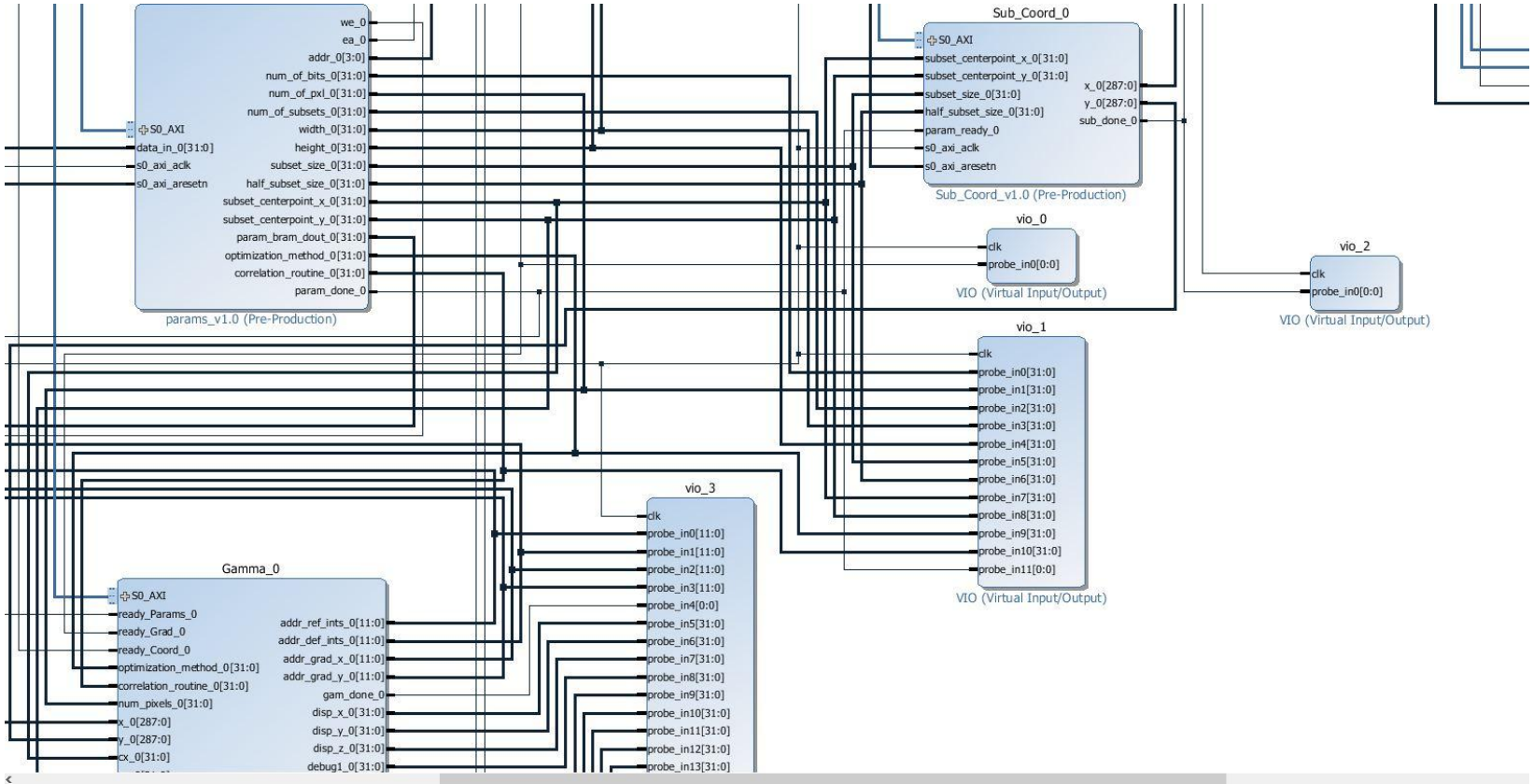
Vivado Block Design



Current Status

Design is working

- **Successful simulation and synthesis**
  - Design meets timing constraints
  - Identical outputs are produced

Testing Data

- **Design compares just 2 frames**
  - Used to verify IP functionality, buffers, end to end flow
  - Image size used (x1)
    - 64*48 = 3,072 pixels, 98,304 bits at 32 bits per pixel (IEEE format)
  - Actual image size needed (x100)
    - 640*480 = 307,200 pixels, 9,830,400 bits at 32 bits per pixel (IEEE format)
  - Scaling now only requires parameter changes, not to FSMs, system architecture

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Results

Reference image VS. Deformed image

HDL VS. GUI - Execution time comparison

Testbench	Frequency	HDL Exe Time	DICe Exe Time
64*48 – BRAM	100 MHz	3.5 ms	13 ms/ 58 ms
64*48 – BRAM	150 MHz	2.5 ms	13 ms/ 58 ms

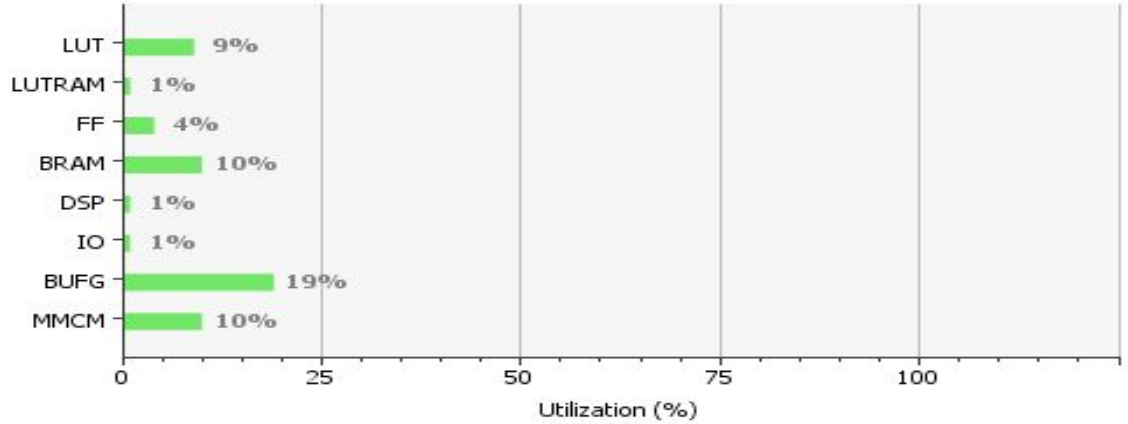
Linear growth expected!

Results

Resource Utilization

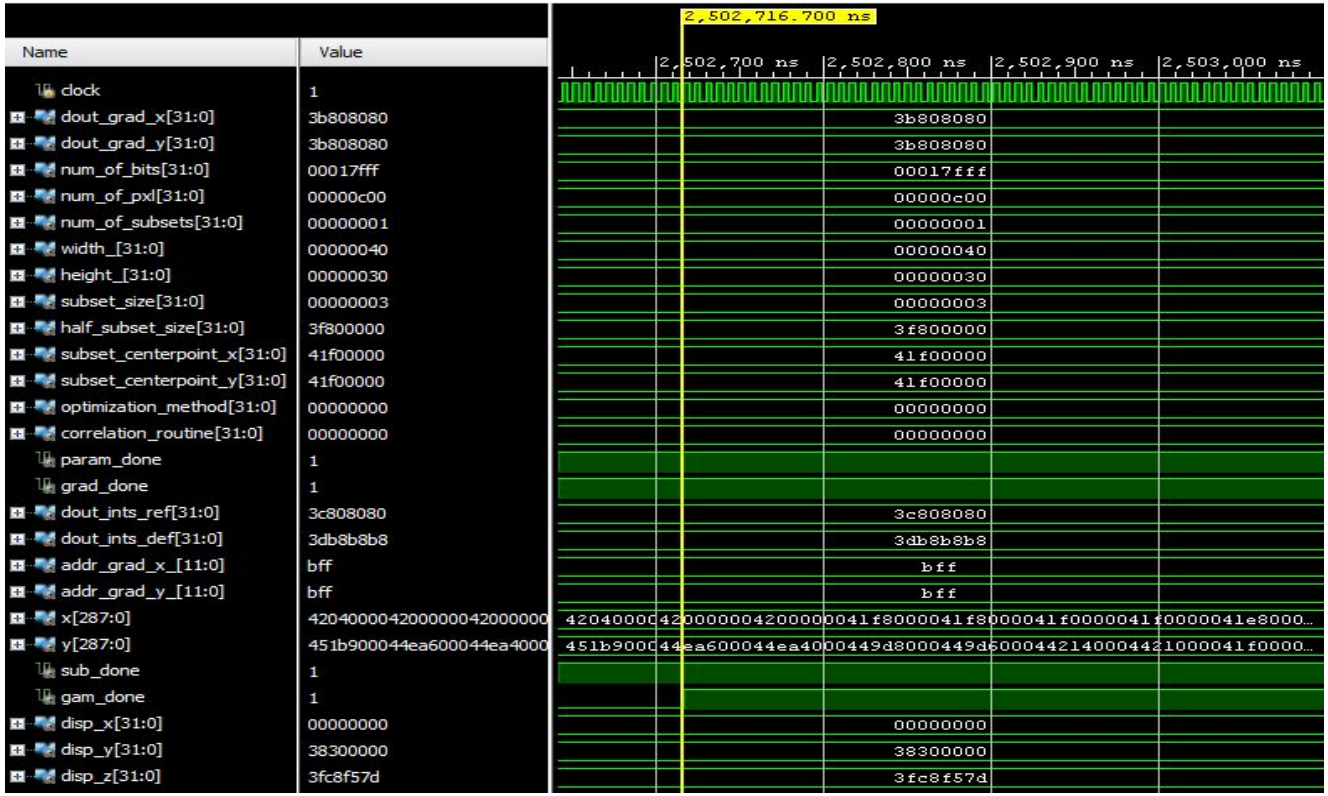
- **Reports from 150 MHz design**

Resource	Utilization	Available	Utilization %
LUT	19108	203800	9.38
LUTRAM	404	64000	0.63
FF	14821	407600	3.64
BRAM	45	445	10.11
DSP	12	840	1.43
IO	3	500	0.60
BUFG	6	32	18.75
MMCM	1	10	10.00



Results

Simulation Waveforms



Results

Synthesis Waveforms

Name	Value	Direction	Activity	VIO
design_1_i/Gamma_0_addr_def_ints_0[11:0]	[H] BF8	Input		hw_vio_4
design_1_i/Gamma_0_addr_grad_y_0[11:0]	[H] BF8	Input		hw_vio_4
design_1_i/Gamma_0_addr_ref_ints_0[11:0]	[H] BF8	Input		hw_vio_4
design_1_i/Gamma_0_debug1_0[31:0]	[H] 7F80_0000	Input		hw_vio_4
design_1_i/Gamma_0_debug2_0[31:0]	[H] 3830_0000	Input		hw_vio_4
design_1_i/Gamma_0_debug4_0[31:0]	[H] 3830_0000	Input		hw_vio_4
design_1_i/Gamma_0_debug6_0[31:0]	[H] 41F0_0000	Input		hw_vio_4
design_1_i/Gamma_0_disp_x_0[31:0]	[H] 0000_0000	Input		hw_vio_4
design_1_i/Gamma_0_gam_done_0	[B] 1	Input		hw_vio_4
design_1_i/Gamma_0_addr_grad_x_0[11:0]	[H] BF8	Input		hw_vio_4
design_1_i/Gamma_0_debug3_0[31:0]	[H] 3830_0000	Input		hw_vio_4
design_1_i/Gamma_0_debug5_0[31:0]	[H] 3830_0000	Input		hw_vio_4
design_1_i/Gamma_0_disp_y_0[31:0]	[H] 3830_0000	Input		hw_vio_4
design_1_i/Gamma_0_disp_z_0[31:0]	[H] 3FC8_F57D	Input		hw_vio_4

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Demo

Let’s show you some of our work in Vivado!

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Next Steps

Full-scale DICe HDL

- **Scale up BRAM sizing (x100)**
  - Expecting images of 640*480 = 307,200 pixels
  - Handle a much larger frame count
- **Extend Functionality**
  - Ability to have multiple subsets (currently just 1)
  - Handle various subset shapes (based on required needs)
- **Network I/O**
  - Python program to intermediate (start, video conversion, FPGA communication)
  - Ethernet IP/Drivers to stream images
  - Desired output type? Text file?

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Next Steps

Optimization & Performance

- **Memory and resources**
  - Reduce memory and resource usage to account for design scale-up
- **Increased clock speed**
  - Current design operates at 150 MHz
  - Potential to increase clock speed to 200 MHz
- **System-wide speed-up**
  - Leverage ability to parallelize multiple IP's
  - Implement various pipelining techniques
  - Compare HDL and HLS results for efficiency
- **Clean up**
  - Improve readability of Verilog code
  - Will enable ease of future development

Questions From Us…

1) Are square subsets okay, or are unique subset shapes required?
2) Can we assume we will be sticking with black & white video?
3) Do you want us to set up a GitHub repository of our work and share the link to monitor progress?
4) Would it be possible to get a screen-recorded video of how your teams use the DICe software on some sample video, along with the total execution time?
5) I/O specifics for the FPGA

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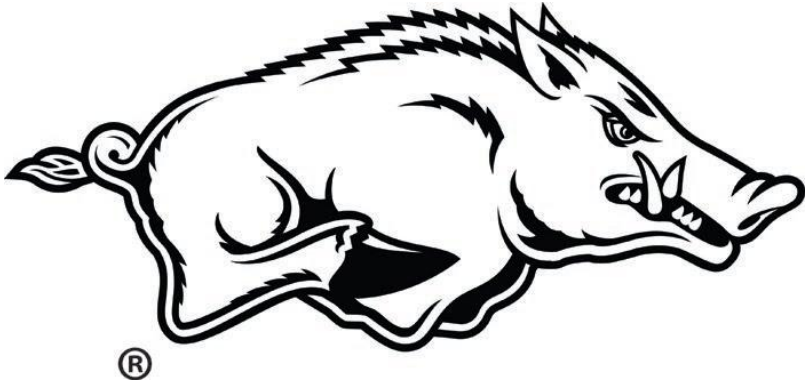
Questions For Us?



Honeywell