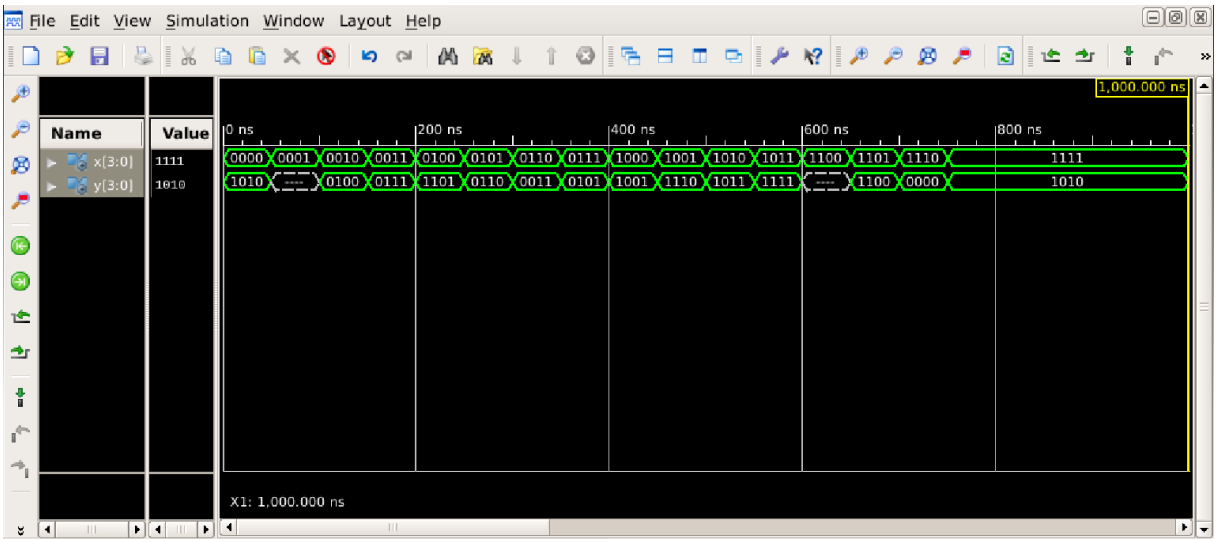
Jakub Bilski, 155865

Sprawozdanie – Podstawy Techniki Cyfrowej, laboratoria nr 5, 11.12.2023

1.



Plik VHD:

```
----------------------------------------------------------------------------------
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-- Company:
-- Engineer:
--
-- Create Date: 9:24:22 11/12/2023
-- Design Name:
-- Module Name: b4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
```

```
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:

--
----------------------------------------------------------------------
----------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity b4 is
Port ( X : in STD_LOGIC_VECTOR (3 downto 0);
Y : out STD_LOGIC_VECTOR (3 downto 0));
end b4;
architecture Behavioral of b4 is
begin
process (X)
begin
case X is
when "0000"=>Y<="1010";
when "0001"=>Y<="----";
when "0010"=>Y<="0100";
when "0011"=>Y<="0111";
when "0100"=>Y<="1101";
```

```
when "0101"=>Y<="0110";
when "0110"=>Y<="0101";
when "0111"=>Y<="0101";
when "1000"=>Y<="1001";
when "1001"=>Y<="1111";
when "1010"=>Y<="1011";
when "1011"=>Y<="1111";
when "1100"=>Y<="----";
when "1101"=>Y<="1100";
when "1110"=>Y<="0000";
when "1111"=>Y<="1010";
when others=>Y<="----";
end case;
end process;
end Behavioral;
```

Plik UCF

```
NET "X[0]" LOC="A10";
NET "X[1]" LOC="D14";
NET "X[2]" LOC="C14";
NET "X[3]" LOC="P15";

NET "Y[3]" LOC="L14";
NET "Y[2]" LOC="N14";
NET "Y[1]" LOC="M14";
NET "Y[0]" LOC="U18";
```