ICFEM 2025 Program (Hangzhou, GMT+8)

Day 0 - November 10, 2025	
8:30 - 17:30	Registration
9:00 - 12:00	**Tutorial: Analysis (Model Checking) Techniques for Markov Decision Processes (MDPs)** **Speaker: Prof. P. S. Thiagarajan**
Day 1 - November 11, 2025	
8:30 - 9:00	Registration & Opening Remark
9:00 - 10:00	**Opening Keynote 1 *by Prof. Jifeng He***
10:00 - 10:30	Coffee Break
10:30 - 12:30	**Session 1: Formal Verification of Security and Cryptographic Protocols** **[3]** *Formal Verification of Physical Layer Security Protocols for Next-Generation Communication Networks* Kangfeng Ye, Roberto Metere, Jim Woodcock and Poonam Yadav **[28]** *Formal Construction of Threat Detections from Attack Trees* Dumitru Bogdan Prelipcean, Catalin Dima and Daniele Varacca **[37]** *ZK-ProVer: Proving Programming Verification in Non-Interactive Zero-Knowledge Proofs* Haoyu Wei, Jingyu Ke, Ruibang Liu and Guoqiang Li **[45]** *Formal Modeling and Verification of Blockchain Consensus Protocols: A Case Study on ChainMaker* Minfan Xu, Shuo Zhou, Xian Xu and Huan Long
12:30 - 14:00	Lunch Break
14:00 - 15:00	**Keynote 2 *by Prof. Jim Woodcock***
15:00 - 15:30	Coffee Break
15:30 - 17:30	**Session 2: LLMs and Formal Methods** **[4]** *Automata-Based Steering Method for Diverse Structured Generation of Large Language Models* Xiaokun Luan, Zeming Wei, Yihao Zhang and Meng Sun **[8]** *LLM-SYM: Integrating Symbolic Methods and Large Language Models for Automated Theorem Proving* Yifan Wu, Yanhong Huang and Jianqi Shi **[11]** *Formalizing Requirements into Dafny Specifications with LLMs* Yi-Han Lu, Xue-Yang Zhu, Wenhui Zhang and Rongjie Yan **[36]** *A Test-Driven Approach for Refining Use Case Descriptions of Software Requirements with LLMs* Haibo Li, Lixiao Zheng and Qihang Cai

Day 2 - November 12, 2025	
9:00 - 10:00	**Keynote 3 *by Mariëlle Stoelinga***
10:00 - 10:30	Coffee Break
10:30 - 12:00	**Session 3: Runtime Verification, Control, and Robotics** **[10]** *Neural-Symbolic System Control Adjustment Based on Runtime Verification* Hongxu Zhu, Wanwei Liu and Ji Wang **[9]** *Modeling and Analysis of Cyber-Physical Systems in the Hybrid pi-Calculus Using Extended Sequence Diagrams* Xiong Xu, Jixiang Miao, Shuling Wang and Jean-Pierre Talpin **[65]** *Formal Modelling of Fault Tolerant Robotic Missions* Manon Lecart and Elena Troubitsyna
12:00 - 13:30	Lunch Break
13:30 - 15:30	**Session 4: Program Analysis and Software Reliability** **[18]** *Detecting Vector Container Errors in C++ Programs via Abstract Interpretation* Liusiyu Liu, Chen Liqian, Fan Guangsheng, Yin Banghu, Huang Chun and Wang Ji **[41]** *Synthesizing Loops from Linear Ranking Functions* Rui-Juan Jing, Yaru Yuan, Yuxing Cai, Yi Li and Changbo Chen **[25]** *MetaLogic: Robustness Evaluation of Text-to-Image Models Using Logically Equivalent Prompts* Yifan Shen, Yangyang Shu, Hye-young Paik and Yulei Sui **[48]***Model-based test case generation from UML sequence diagrams using extended fnite state machines* Maurício Rocha, Adenilso Simao and Thiago Souza
15:30 - 16:00	Coffee Break
16:00 - 17:50	**Session 5: SMT and Quantitative Verification** **[60]** *Avoiding Larger Conflict Regions in CDCL-Style Methods for Solving SMT-NRA* Xinpeng Ni, Tianyi Ding and Bican Xia **[61]** *Formal Modeling of Reinforcement Learning Systems with SMT* Tianyi Ding, Yuxin Lin and Meng Sun **[64]** *Towards High-Level SMT Program Modeling: Bounded Integers, Simplified Structs, and Metaprogramming* Xiangyu Li **[56]** *Quantitative Verification for Temporal Properties of Massive Linear Systems* Qing Liu, Yuntao Li, Sung Woo Choi, Luan Viet Nguyen and Hoang-Dung Tran
18:30 - 20:30	**Conference Banquet & Award Ceremony(Location: Jinxi Hotel)**

Day 3 - November 13, 2025	
9:00 - 10:00	**Keynote 4 *by Yongwang Zhao***
10:00 - 10:30	Coffee Break
10:30 - 12:30	**Session 6: Logic, Automata, and Concurrent Systems** **[22]** *BCCIC3: Batch Clause Construction Enhanced Generalization in IC3* Yi Chen, Liangze Yin, Xinyi Gong, Ji Wang and Ting Wang **[42]** *Modeling and Verifying Concurrent Reactive Systems Using Separation Logic* Huan Sun, David Sanán, Jun Sun and Wenhai Wang **[54]** *A Unified Method to Efficiently Verify Opacity of Discrete-Timed Automata* Julian Klein, Kuize Zhang and Sabine Glesner **[67]** *Specification and Verification of Multi-Clock Systems Using a Temporal Logic with Clock Constraints* Yuanrui Zhang, Frederic Mallet, Min Zhang and Zhiming Liu
12:30 - 14:00	Lunch Break
14:00 -15:30	**West Lake Hiking Tour**
	End

Keynotes
Invited Papers
Regular Papers
Doctoral Symposium Papers
Journal First Papers