Curriculum Vitea

Imen Chakroun

PHD and Engineer in computer science

Born on April 30, 1985 in Tunisia
Married, 1 child

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Education

- **October 2010 - June 2013** PhD in computer science at LIFL Lille 1 University and INRIA Lille Nord Europe with highest honors.
- **2008 - 2009** Second year master in networks and multimedia systems at National School of Computer Science - ENSI - Tunisia.
- **2007 - 2008** First year master in networks and multimedia systems at National School of Computer Science - ENSI - Tunisia.
- **2003 - 2008** Engineer scholarship at National School of Computer Science - ENSI - Tunisia with honors - Rank (4/256)
- **2003** Bachelor in mathematics with highest honors at Bourguiba Pionneer school - Tunisia.

Professional Experience

- **2013-Now** HPC research Engineer.
  At : Chase Information Technology Services Limited - London.
  Topic : Designing parallel voice recognition softwares.
- **2009-2010** Software Engineer. *(13 months)*
  At : Tunisie Télécom in collaboration with Capegemini France.
  Topic : Customization of BSCS iX R2's CX interface.
- **2009** Master's degree internship *(6 months)*
  At : ASAP Reasearch Team - INRIA, France.
  Supervisor : Dr Fabrice Le fessant.
  Topic : Collaborative backup on peer to peer networks.
- **2008** : Engineer's degree Internship *(4 months)*
  At : PLANETE Reasearch Team - INRIA, France.
  Supervisor : Dr Thierry Turletti.
  Topic : Improving multimedia transmission on top of hybrid wired and wireless networks.

- **2007** : Internship *(2 months)*
  At : SIEMENS - Tunisie.
  Topic : Designing solutions for merging two information systems.

Teaching

- **2012 - 2013** Initiation à la programmation: First Year Bachelor, 54h.
  Supercomputing (in english): Second year Master in Advanced Scientific Computing, 20h.
- **2011 - 2012** Codage de l'information: Second Year Bachelor, 36h.
  Recherche Opérationnelle: First year Master in Information & Knowledge Systems Engineering and Management, 30h.
- **2010 - 2011** Algorithmes et Programmation Impérative: First Year Bachelor, 48h.
  Recherche Opérationnelle: First year Master in Information & Knowledge Systems Engineering and Management, 16h.

Mentoring

- BOURGOIS Tristan - Master M2 IAGL - Lille 1.
  Innovative prototyping with Pharo. THALES SYSTEMES AEROPORTES-BREST Corporation.
- DUTHOIT Marc - Licence L3 Informatique - Lille 1.
  Design and Implementation of a mobile solution for project monitoring. SOPRA GROUP Corporation.

Awards

C3I - Certificate of expertise in Supercomputing : awarded by the CPU (Conference of Presidents of Universities), GENCI (Grand Equipement National pour le calcul Intensif) and La maison de la simulation.

Research Activities

The major objective of my Phd research work was to rethink the design and implementation of Branch and Bound algorithms (B&B) for solving challenging Combinatorial Optimization Problems on top of GPU-enhanced heterogeneous computational platforms. Our challenge was to exploit the underlying levels of parallelism provided through the today's heterogeneous computing platforms (GPUs, multi-core, grid computing) and to rethink the parallel models of B&B accordingly. The challenges and associated contributions have been addressed via an incremental design methodology: B&B for a single CPU core combined with a single GPU, B&B for a multi-core CPU combined with a single GPU,

B&B for a multi-core CPU combined with multiple GPUs, B&B for a cluster or grid of heterogeneous computational nodes.

A preliminary experimental study we have performed on some large FSP instances has revealed that the search tree is highly irregular (in shape and size) and very large (billions of billions of nodes), and the bounding operator is time-exorbitant (about 97% of B&B). Therefore, our first contribution was to propose a (single CPU core) GPU-accelerated approach (GB&B) in which only the bounding operator is performed on the GPU device. The approach deals with two issues: thread divergence [Chakroun et al., Concurrency and Computation: Practice and Experience 2012] and device hierarchical memory optimization [Melab et al., IEEE Cluster 2012]. Compared to a single CPU core-based implementation, speed-ups up to (x100) are obtained on Nvidia Tesla C2050. Although these good speed-ups, the performance analysis has shown that the overhead induced by the data transfer between CPU and GPU is high. Therefore, the aim of the second contribution [Chakroun et al., ICCS 2013] is to extend the approach (LL-GB&B) in order to minimize the CPU-GPU communication latency. Such objective is achieved through a GPU-based fine-grained parallelization of the branching and pruning operators in addition to the bounding one. The major and particularly challenging issue addressed here is thread divergence due to the strongly irregular nature of the explored tree mentioned above. Compared to a single CPU-based execution, LL-GB&B allows accelerations up to (x160) for large problem instances.

The third contribution [Chakroun et al., Journal of Parallel and Distributed Computing, 2013] consists in investigating the combination of GPU with multi-core processing. Two scenarios have been explored leading to two approaches: a concurrent (RLL-GB&B) and a cooperative one (PLL-GB&B). In the first one, the exploration process is performed concurrently by the GPU and the CPU cores. In the cooperative approach, the CPU cores prepare and off-load to GPU pools of subproblems using data streaming while the GPU performs the exploration. When combining multi-core and GPU, we figure out that using RLL-GB&B is not beneficial while PLL-GB&B enables an improvement up to (36%) compared to LL-GB&B. The fourth contribution of my thesis was to address the combination of GPU and multi-core computing with large scale distributed computing. To do that, the different revisited algorithms have been put together in a heterogeneous meta-algorithm which automatically selects the one to be deployed according to the target hardware configuration. The meta-algorithm is coupled with the B&BGrid approach proposed in [Mezmaz et al., IEEE IPDPS'2007]. B&BGrid distributes the work units (search subspaces coded by intervals) among the grid nodes while the metaalgorithm selects and applies locally a parallel B&B algorithm on the received intervals. The combined approach allowed us to solve to optimality and efficiently some Taillard's FSP instances (20 jobs on 20 machines).

Publications

International Journals

- I. Chakroun and N. Melab, "Towards an heterogeneous and adaptive parallel Branch-and-Bound algorithm.", **Journal of Computer and System Sciences (JCSS) - Elsevier**- To appear, 2014.

- I. Chakroun, N. Melab, M.Mezmaz and D. Tuyttens, " Combining multi-core and GPU computing for solving combinatorial optimization problems.", **Journal of Parallel and Distributed Computing (JPDC) - Elsevier** - Volume 73, Issue 12, December 2013, Pages 1563-1577, ISSN 0743-7315, http://dx.doi.org/10.1016/j.jpdc.2013.07.023.

- N. Melab, I. Chakroun and A.Bendjoudi, "Graphics processing unit-accelerated bounding for branch-and-bound applied to a permutation problem using data access optimization.", **Concurrency and Computation: Practice and Experience (CCPE)** - http://dx.doi.org/10.1002/cpe.3155 - (2013) - John Wiley & Sons.

- I. Chakroun, M.Mezmaz, N. Melab, and A.Bendjoudi, " Reducing thread divergence in a GPU-accelerated branch-and-bound algorithm", **Concurrency and Computation: Practice and Experience 25(8): 1121-1136 (2013) - John Wiley & Sons.**

International Conference Proceedings

- I. Chakroun and N. Melab. "Operator-level GPU-accelerated Branch and Bound algorithms." International Conference on Computational Science, ICCS 2013. Barcelona, Spain, June 5-7, 2013.
- N. Melab, I. Chakroun , M. Mezmaz and D.Tuyttens. " A GPU-accelerated Branch-and-Bound Algorithm for the Flow-Shop Scheduling Problem". 14th IEEE International Conference on Cluster Computing, CLUSTER'12. China, Beijin, September 24-28, 2012.
- I. Chakroun and N. Melab. "An Adaptative Multi-GPU based Branch-and-Bound. A Case Study: the Flow-Shop Scheduling Problem". 14th IEEE International Conference on High Performance Computing and Communications, HPCC'12. United Kingdom, Liverpool, June 24-27, 2012.
- I. Chakroun, A. Bendjoudi, and N.Melab. "Reducing Thread Divergence in GPU-based B&B Applied to the Flow-shop problem". 9th International Conference on Parallel Processing and Applied Mathematics PPAM'11, LNCS. Poland, Torun, September 11-14, 2011.

Book Chapters

- I. Chakroun and N. Melab. "GPU-accelerated Tree-based Exact Optimization Methods". Designing scientific applications on GPUs. CRC Press, Taylor & Francis Group.

Technical Skills

- **Parallel and distributed computing** : CUDA, MPI, OpenMP, Pthreads, Grid'5000.
- **Programming Languages** : C, C++ ,JAVA,CAML, XML.
- **OS** : Windows XP, UNIX, Linux, GCOS7.
- **Web** : HTML, Javascript, PHP.

Linguistic Skills

- French : Bilingual.
- English : Fluent.
- Italian : Fluent.
- Arabic : Mother tongue.

References

- **Nouredine Melab**. Professor at Lille 1 University, LIFL - Inria Lille
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