JUNGUK CHO

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EDUCATION

UNIVERSITY OF CALIFORNIA, SAN DIEGO La Jolla, CA, USA
Postdoctoral Scholar in Computer Science and Engineering March 2010

- *Major*: Hardware acceleration of object detection and color segmentation based on machine learning
- *Papers*: FPGA-based Face Detection System using Haar Classifiers, ACM/SIGDA Symposium on FPGA 2009. Parallelized Architecture of Multiple Classifiers for Face Detection, IEEE Conference on ASAP 2009.

SUNGKYUNKWAN UNIVERISTY Suwon, Korea
Doctor of Philosophy in Electronic and Electrical Engineering February 2006

- *Thesis*: A Real-Time Object Tracking System using a Particle Filter
- *Honors*: Finalist of T. J. Best Paper Award at IEEE International Conference on ROBIO, December 2007. Outstanding Paper Award at the Center for Intelligent Robotics Workshop, August 2006.

SUNGKYUNKWAN UNIVERSITY Suwon, Korea
Master of Science in Electronic and Electrical Engineering February 2003

- *Thesis*: High Performance Open Architecture Motion Controller

SUNGKYUNKWAN UNIVERSITY Suwon, Korea
Bachelor of Science in Electrical and Computer Engineering February 2001

- *Thesis*: FPGA-Based Microstep Motor Driver
- *Honors*: Excellence Award at the Samsung Electronics MCU Design Contest, March 2000.

EXPERIENCE

SAMSUNG RESEARCH, SAMSUNG ELECTRONICS Seoul, Korea
Principal Engineer March 2016 - Present

Currently conducting research in the area of neural network processing for deep learning applications.

- Designing system architectures of Neural network Processing Units (NPUs) in SoCs for Ultra HD televisions, smart phones, and consumer electronics.
- Driving silicon prototyping utilizing FPGA platforms and demonstrating deep learning applications such as object classification, object detection, and super resolution imaging in custom FPGA based PCBs.
- Responsible for analyzing design spec, developing and implementing systems integrated for major design blocks by generating system buses, interfaces, and peripherals, and analyzing performance results.
- Working closely with application engineers in order to improve the performance of deep learning applications by neural network optimization such as pruning, clustering, and quantization.

Led research in the area of virtual reality in e-commerce. (Samsung Electronics' in-house incubation program C-Lab)

- Designed UI/UX for virtual reality applications and developed an SDK capable of making VR contents easily.
- Produced a feasible application for virtual reality shopping using the developed authoring tool.
- Demonstrate a virtual reality shopping platform by cooperating with an enterprise in the VR industry.

Senior Engineer November 2013 - February 2016

Conducted research in the area of reconfigurable processor for vision processing.

- Designed hardware architectures based on multiple Samsung Reconfigurable Processors (SRPs) for video processing using Verilog HDL in SoCs for Ultra HD televisions.
- Verified the designs on simulators and FPGAs with video post-processing functions such as color space conversion, color enhancement, black level management, gamma correction, and local dimming.
- Designed and verified hardware IPs of 8K UHD display interface including video post-processing blocks in SoCs.

- Cooperating with video application engineers to improve the performance of video processing applications using software pipeline, multi-thread, SIMD (Single Instruction Multiple Data) processing, and intrinsic functions.

SAMSUNG ADVANCED INSTITUTE OF TECHNOLOGY Yongin, Korea
R&D Staff Member May 2010 - November 2013

Conducted research in the area of reconfigurable processors for image processing.

- Designed and verified hardware architectures based on Samsung Reconfigurable Processor (SRP) for image processing using Verilog HDL in SoCs for digital still/video cameras.
- Drove silicon prototyping utilizing FPGA platforms with multi-frame post-processing applications such as high dynamic range imaging, low light shot noise reduction, panoramic image stitching, and stereo imaging.
- Developed post-processing applications and improved the performance of them using software pipeline, multi-thread, SIMD processing, and intrinsic functions by gathering/analyzing performance results.
- Developed SRP based programmable video Image Signal Processors (ISPs) qualified for Skype certification for webcams installed televisions and optimized the performance of them into the restricted system environments.
- Developed vision applications such as face detection, human detection, and human pose estimation into SRP systems and improved the performance of them by optimization methods suitable for SRP architecture.

UNIVERSITY OF CALIFORNIA, SAN DIEGO La Jolla, CA, USA
Postdoctoral Scholar January 2008 - March 2010

Conducted research in the area of hardware acceleration of object detection and color segmentation based on machine learning.

- Designed hardware acceleration of Haar classifiers for objects (faces and fishes) detection using Verilog HDL and implemented the design on FPGAs. The object detection system has up to 84× performance gain over an equivalent software implementation.
- Designed color segmentation using Verilog HDL and implemented the design on an FPGA. The color segmentation system has up to 20× performance gain over an equivalent software implementation.
- Worked on FPGA based low power underwater modems. The modem's signal processing algorithm can provide a maximum of 210× and 52× decreases in energy consumption over the microcontroller and DSP implementations respectively.

SUNGKYUNKWAN UNIVERSITY Suwon, Korea
Research Instructor March 2006 - December 2007

- Involved in a Brain Korea 21 project funded by the Ministry of Education and Human Resources Development of Korea.
- Managed a 30-person research group that performed research in embedded systems, system on a chip, motion control, electronic control unit, human computer interaction, and mobile phones.
- Led a 21st Century Frontier R&D Program (vision/speech system on a chip) funded by the Ministry of Commerce, Industry and Energy of Korea, and a Lab of Excellency Project (motion-vision integrated system) funded by the Ministry of Education and Human Resources Development, the Ministry of Commerce, Industry and Energy, and the Ministry of Labor of Korea.
- Designed hardware acceleration of visual tracking system using color histograms for intelligent robots using VHDL and implemented the design on FPGAs. The visual tracking system has up to 540× performance gain over an equivalent software implementation.
- Developed a motion-vision integrated system which is based on an FPGA (includes low-level image processing and multiple axis motion control) and an ARM processor (includes operating system, user interface, and libraries).

Graduate Student Researcher March 2001 - February 2006

- Managed an 11-person research team that performed projects related to image processing and motion control.
- Designed hardware acceleration of active visual tracking (using projection profile matching and particle filter), object tracking (using particle filters), and histogram equalization with automatic gain control (using histogram distribution) using VHDL and implemented the designs on FPGAs.
- Designed and implemented FPGA based motion controller (multiple axis motion control) which has velocity profile generation, interpolation, kinematics and inverse-kinematics, PID control, and motor driver using VHDL.
- Developed a TMS320C6711 DSP based high performance motion controller which has an open architecture with flexible libraries and GUIs, velocity profile generation, interpolation, PID control, and various motor drivers.
- Developed a low-cost time controller for inspecting small components using 80C196 microprocessors.

- Designed an FPGA based motion controller for step motors which generates various velocity profiles and performs microstepping using VHDL.
- Performed teaching assistant of computer architecture, embedded system, microprocessor, and robotics classes.

REPUBLIC OF KOREA ARMY Yeoncheon, Korea
Sergeant August 1995 - September 1997

- Maintained various communication systems, and commanded a 12-person team that performed military missions.

SKILLS

Hardware Systems

- *FPGAs*: Virtex UltraScale, Kintex UltraScale, Zynq UltraScale, Virtex-7, Kintex-7, Zynq, Virtex-6, Virtex-5, Virtex-4, Virtex-II Pro, Virtex-II, Spartan-3, Spartan-IIE, Spartan-II, CoolRunner-II, FLEX 10K, MAX7000.
- *Microprocessors*: Cortx-A9, Cortex-A8, ARM9 TDMI, Pentium III, PXA270, MPC55545, MPC565, SA-1110, ATmega128, KS88, KS86, 80C296, 80C196, 80C51, 80C86.
- *Digital signal processors*: TMS320C6414, TMS320C6713, TMS320C6711, TMS320C6710, TMS320F2812, TMS320F243, TMS320C240.
- *Embedded processors*: MicroBlaze, PicoBlaze, SRP, NPU

Intellectual Property Cores

- *Deep learning*: Convolutional Neural Network (LeNet, AlexNet, VGGNet, GoogLeNet, ResNet, DenseNet) and Recurrent Neural Network (Bidirectional RNN, Deep RNN, LSTM, GRU).
- *Image processing*: object classification, object detection, post-processing, color classification, face detection, object matching, visual tracking, particle filter, shift-invariant tracing, morphology, binary large object, histogram equalization, automatic gain control, dynamic threshold, color space converter.
- *Motion control*: kinematics and inverse-kinematics, velocity profile generator, feedback encoder counter, digital delay filter, digital differential analyzer, micro step driver, AC servo amplifier driver.
- *Interface*: 8K UHD display interface, UART, USB, PCI, LVDS, Camera Link, DVI, and VGA.
- *Memory control*: FIFO, SRAM, and SDRAM.

Program Languages

- Verilog HDL, VHDL, System Verilog, SystemC, Handel-C, Assembly, C/C++, Python, Perl, and Matlab.

Development Tools

- Certify, Synplify Premier, Identify, Design Compiler, Incisive, ModelSim, Vivado Design Suite, ChipScope Pro, Xilinx SDK, ISE, EDK, Quarts II, Catapult HLS, Stratus HLS, Vivado HLS, DK Design Suite, OrCAD, Matlab, Visual Studio, TensorFlow, Caffe, PyTorch, Code Composer Studio, CodeWarrior, CodeVisionAVR, and Microsoft Micro Assembler.

PUBLICATIONS

JOURNALS

[J1] Jung Uk Cho and Jae Wook Jeon, "**A Motion-Control Chip to Generate Velocity Profiles of Desired Characteristics**," *ETRI Journal*, Vol. 27, No. 5, pp. 563-568, October 2005.

[J2] Jung Uk Cho, Quy Ngoc Le, and Jae Wook Jeon, "**An FPGA-Based Multiple Axis Motion Control Chip**," *IEEE Transactions on Industrial Electronics*, Vol. 56, No. 3, pp. 856-870, March 2009.

[J3] Seunghun Jin, Junguk Cho, Xuan Dai Pham, Kyoung Mu Lee, Sung-Kee Park, Munsang Kim, and Jae Wook Jeon, "**FPGA Design and Implementation of a Real-time Stereo Vision System**," *IEEE Transactions on Circuits and Systems for Video Technology*, Vol. 20, No. 1, pp. 15-26, January 2010.

[J4] Seunghun Jin, Junguk Cho, Key Ho Kwon, and Jae Wook Jeon, "**A Dedicated Hardware Architecture for Real-Time Auto-Focusing using an FPGA**," *Machine Vision and Applications*, Vol. 21, No. 5, pp. 727-734, August 2010.

[J5] Junguk Cho, Seunghun Jin, Key Ho Kwon, and Jae Wook Jeon, "**A Real-Time Histogram Equalization System with Automatic Gain Control using FPGA**," *KSII Transactions on Internet and Information Systems*, Vol. 4, No. 4, pp. 633-654, August 2010.

[J6] Seung-Hyun Choi, Junguk Cho, Yong-Min Tai, and Seong-Won Lee, "**A Parallel Camera Image Signal Processor for SIMD Architecture**," *EURASIP Journal on Image and Video Processing*, Vol. 2016, No. 1, pp. 29-43, January 2016.

CONFERENCES

[C1] Jung Uk Cho and Jae Wook Jeon, "**Development of A High Performance Motion Controller**," *International Conference on Control, Automation and System* (ICCAS 2002), Jeonbuk, Korea, October 16-19, 2002.

[C2] Jung Uk Cho and Jae Wook Jeon, "**Development of Chip-Based Precision Motion Controller**," *International Conference on Control, Automation and System* (ICCAS 2003), Gyeongju, Korea, October 22-25, 2003.

[C3] Jung Uk Cho and Jae Wook Jeon, "**A Low-Cost Programmable Timing Controller for Inspecting Small Components**," *IEEE / RSJ International Conference on Intelligent Robots and Systems* (IROS 2003), Las Vegas, Nevada, USA, October 27-31, 2003.

[C4] Jung Uk Cho, Seung Hun Jin, Jae Wook Jeon, Jong Tae Kim, Jun Dong Cho, Kun Myoung Lee, Jee Hyoung Lee, Jong Eun Byun, and Jong Chan Choi, "**FPGA based Dynamic Thresholding Circuit**," *International Conference on Control, Automation and System* (ICCAS 2004), Bangkok, Thailand, August 25-27, 2004.

[C5] Jung Uk Cho, Seung Hun Jin, Xuan Dai Pham, Jong Eun Byun, Hoon Kang, and Jae Wook Jeon, "**A Real-Time Object Tracking System Using a Particle Filter**," *IEEE / RSJ International Conference on Intelligent Robots and Systems* (IROS 2006), Beijing, China, October 9-15, 2006.

[C6] Jung Uk Cho, Seung Hun Jin, Xuan Dai Pham, and Jae Wook Jeon, "**Object Tracking Circuit using Particle Filter with Multiple Features**," *SICE-ICASE International Joint Conference* (SICE-ICASE 2006), Busan, Korea, October 19-21, 2006.

[C7] Seung Hun Jin, Jung Uk Cho, and Jae Wook Jeon, "**FPGA based Passive Auto Focus System using Adaptive Thresholding**," *SICE-ICASE International Joint Conference* (SICE-ICASE 2006), Busan, Korea, October 19-21, 2006.

[C8] Ngoc Quy Le, Jung Uk Cho, and Jae Wook Jeon, "**Application of Velocity Profile Generation and Closed-Loop Control in Step Motor Control System**," *SICE-ICASE International Joint Conference* (SICE-ICASE 2006), Busan, Korea, October 19-21, 2006.

[C9] Jung Uk Cho, Seung Hun Jin, Xuan Dai Pham, and Jae Wook Jeon, "**Multiple Objects Tracking Circuit using Particle Filters with Multiple Features**," *IEEE International Conference on Robotics and Automation* (ICRA 2007), Roma, Italy, April 10-14, 2007.

[C10] Jung Uk Cho, Seung Hun Jin, Xuan Dai Pham, Dongkyun Kim, and Jae Wook Jeon, "**A Real-Time Color Feature Tracking System using Color Histograms**," *International Conference on Control, Automation and Systems* (ICCAS 2007), Seoul, Korea, October 17-20, 2007.

[C11] Seung Hun Jin, Jung Uk Cho, Dae Ro Lee, Jong Hyun Park, Hyun Soon Kim, Chang Hoon Lee, Jong Suk Choi, and Jae Wook Jeon, "**An FPGA-Based Voice Signal Preprocessor for the Real-Time Cross-Correlation**," *International Conference on Control, Automation and Systems* (ICCAS 2007), Seoul, Korea, October 17-20, 2007.

[C12] Dongkyun Kim, Jung Uk Cho, Thien Cong Pham, and Jae Wook Jeon, "**Real-Time Object Boundary Tracking Circuit Based on FPGA**," *International Conference on Control, Automation and Systems* (ICCAS 2007), Seoul, Korea, October 17-20, 2007.

[C13] Byoung Yun Oh, Jung Uk Cho, Ngoc Quy Le, Key Ho Kwon, and Jae Wook Jeon, "**FPGA-Based Motion Controller using CAN**," *International Conference on Control, Automation and Systems* (ICCAS 2007), Seoul, Korea, October 17-20, 2007.

[C14] Jung Uk Cho, Seung Hun Jin, Xuan Dai Pham, Dongkyun Kim, and Jae Wook Jeon, "**FPGA-Based Real-Time Visual Tracking System using Adaptive Color Histograms**," *IEEE International Conference on Robotics and Biomimetics* (ROBIO 2007), Sanya, China, December 15-18, 2007.

[C15] Seung Hun Jin, Jung Uk Cho, and Jae Wook Jeon, "**Pipelined Virtual Camera Configuration for Real-time Image Processing based on FPGA**," *IEEE International Conference on Robotics and Biomimetics* (ROBIO 2007), Sanya, China, December 15-18, 2007.

[C16] Xuan Dai Pham, Jung Uk Cho, and Jae Wook Jeon, "**Background Compensation using Hough Transformation**," *IEEE International Conference on Robotics and Automation* (ICRA 2008), Pasadena, California, USA, May 19-23, 2008.

[C17] Bridget Benson, Ali Irturk, Junguk Cho, and Ryan Kastner, "**Survey of Hardware Platforms for an Energy Efficient Implementation of Matching Pursuits Algorithm for Shallow Water Networks**," *ACM International Workshop on Underwater Networks* (WUWNet 2008), San Francisco, California, USA, September 15, 2008.

[C18] Junguk Cho, Shahnam Mirzaei, Jason Oberg, and Ryan Kastner, "**FPGA-Based Face Detection System using Haar Classifiers**," *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays* (FPGA 2009), Monterey, California, USA, February 22-24, 2009.

[C19] Bridget Benson, Junguk Cho, Deborah Goshorn, and Ryan Kastner, "**Field Programmable Gate Array Based Fish Detection using Haar Classifiers**," *American Academy of Underwater Sciences*, Atlanta, Georgia, USA, March 10-14, 2009.

[C20] Bridget Benson, Ali Irturk, Junguk Cho, and Ryan Kastner, "**Energy Benefits of Reconfigurable Hardware for Use in Underwater Sensor Nets**," *IEEE International Symposium on Parallel & Distributed Processing* (IPDPS 2009), Rome, Italy, May 25-26, 2009.

[C21] Junguk Cho, Bridget Benson, Shahnam Mirzaei, and Ryan Kastner, "**Parallelized Architecture of Multiple Classifiers for Face Detection**," *IEEE International Conference on Application-specific Systems, Architectures and Processors* (ASAP 2009), Boston, Massachusetts, USA, July 7-9, 2009.

[C22] Junguk Cho, Bridget Benson, and Ryan Kastner, "**Hardware Acceleration of Multi-View Face Detection**," *IEEE Symposium on Application Specific Processors* (SASP 2009), San Francisco, California, USA, July 27-28, 2009.

[C23] Junguk Cho, Bridget Benson, Sunsern Cheamanukul, and Ryan Kastner, "**Increased Performance of FPGA-Based Color Classification System**," *IEEE International Symposium on Field-Programmable Custom Computing Machines* (FCCM 2010), Charlotte, North Carolina, USA, May 2-4, 2010.

[C24] Deborah Goshorn, Junguk Cho, Ryan Kastner, and Shahnam Mirzaei, "**Field Programmable Gate Array Implementation of Parts-based Object Detection for Real Time Video Applications**," *International Conference on Field Programmable Logic and Applications* (FPL 2010), Milano, Italy, August 31 - September 2, 2010.

[C25] Sunghyun Cho, Hojin Cho, Yu-Wing Tai, Young Su Moon, Junguk Cho, Shihwa Lee, and Seungyong Lee, "**Lucas-Kanade Image Registration using Camera Motions**," *IS&T/SPIE Electronic Imaging* (EI 2012), San Francisco, California, January 22, 2012.

[C26] Hojin Cho, Sunghyun Cho, Young Su Moon, Junguk Cho, Shihwa Lee, and Seungyong Lee, "**Analysis of Practical Coverage of Uniform Motions to Approximate Real Camera Shakes**," *IS&T/SPIE Electronic Imaging* (EI 2012), San Francisco, California, January 22, 2012.

[C27] Junguk Cho, Joon Hyuk Cha, Yong Min Tai, Young-Su Moon, and Shihwa Lee, "**Stereo Panoramic Image Stitching with a Single Camera**," *IEEE International Conference on Consumer Electronics* (ICCE 2013), Las Vegas, Nevada, January 11-14, 2013.

[C28] Yong Min Tai, Young-Su Moon, Junguk Cho, and Shihwa Lee, "**A Cross-channel Bilateral Filter for CFA Image Denosing**," *IEEE International Conference on Consumer Electronics* (ICCE 2013), Las Vegas, Nevada, January 11-14, 2013.

[C29] Young-Su Moon, Shi-Hwa Lee, Yong-Min Tai, and Junguk Cho, "**A Fast Low-light Multi-image Fusion with Online Image Restoration**," *IEEE International Conference on Consumer Electronics* (ICCE 2013), Las Vegas, Nevada, January 11-14, 2013.

[C30] Young-Su Moon, Jonghun Lee, Yong-Min Tai, Junguk Cho, Do-Hyung Kim, and Shi-Hwa Lee, "**A Ghost-Free Pseudo-Multiframe HDR**," *IEEE International Conference on Consumer Electronics* (ICCE 2014), Las Vegas, Nevada, January 10-13, 2014.

[C31] Jonghun Lee, Young-Su Moon, Junguk Cho, Yong-Min Tai, Do-Hyung Kim, and Shi-Hwa Lee, "**A Fast Spatiotemporal Denoising Scheme for Multi-Shot Images**," *IEEE International Conference on Consumer Electronics* (ICCE 2014), Las Vegas, Nevada, January 10-13, 2014.

[C32] Seung Hyun Choi, Junguk Cho, Yong-Min Tai, and Seong-Won Lee, "**Implementation of an Image Signal Processor for Reconfigurable Processors**," *IEEE International Conference on Consumer Electronics* (ICCE 2014), Las Vegas, Nevada, January 10-13, 2014.

[C33] Junguk Cho, Yongseok Choi, Sukjin Kim, and Shihwa Lee, "**Direct Display Interface including Video Post-processing for 8K UHD TV**," *IEEE International Conference on Consumer Electronics* (ICCE 2015), Las Vegas, Nevada, January 9-12, 2015.

PATENTS

United States Patents

[P1] Jae Wook Jeon, Seung Hun Jin, Jung Uk Cho, Sung Kee Park, Munsang Kim, Kyoung Mu Lee, and Jong Eun Byun, "**Rectification System and Method of Stereo Image in Real-Time**," Patent Number US 7,643,067 B2, USA, January 5, 2010.

[P2] Jae Wook Jeon, Seung Hun Jin, Jung Uk Cho, Sung Kee Park, Munsang Kim, Kyoung Mu Lee, and Jong Eun Byun, "**Extensible System and Method for Stereo Matching in Real-time**," Patent Number US 8,340,397 B2, USA, December 25, 2012.

[P3] Jae Wook Jeon, Dong Kyun Kim, Jung Uk Cho, Seung Hun Jin, Dae Ro Lee, Jong Hyun Park, Ki Hoon Kim, and Thien Cong Pham, "**Apparatus and Method for Generating Chain Code**," Patent Number US 8,340,446 B2, USA, December 25, 2012.

[P4] Jae Wook Jeon, Sang Jun Lee, Xuan Dai Pham, Seung Hun Jin, Dong Kyun Kim, Ki Hoon Kim, and Jung Uk Cho, "**Methods and Devices for Detecting Changes in Background of Images using Multiple Binary Images Thereof and Hough Transformation**," Patent Number US 8,355,599 B2, USA, January 15, 2013.

[P5] Young Su Moon, Yong Min Tai, Junguk Cho, and Shi Hwa Lee, "**Apparatus and method for generating high dynamic range image from which ghost blur is removed using multi-exposure fusion**," Patent Number US 8,989,484 B2, USA, March 24, 2015.

[P6] Junguk Cho, Seung Yong Lee, Young Su Moon, Shi Hwa Lee, Chi Young Lee, Sung Hyun Cho, and Ho Jin Cho, "**Method and apparatus for deblurring non-uniform motion blur using multi-frame including blurred image and noise image**," Patent Number US 8,995,781 B2, USA, March 31, 2015.

[P7] Junguk Cho, Seung Yong Lee, Young Su Moon, Shi Hwa Lee, Chi Young Lee, Sung Hyun Cho, and Ho Jin Cho, "**Method and apparatus for deblurring non-uniform motion blur in large scale input image based on tile unit**," Patent Number US 9,042,673 B2, USA, May 26, 2015.

[P8] Gengyu Ma, Young Su Moon, Wentao Mao, Junguk Cho, and Ji Yeun Kim, "**Apparatus for generating an image with defocused background and method thereof**," Patent Number US 9,118,846 B2, USA, August 25, 2015.

[P9] Yong Min Tai, Young Su Moon, Junguk Cho, Joon Hyuk Cha, Shi Hwa Lee, and Hyun Sang Park, "**Apparatus and method for calculating cumulative histogram of image**," Patent Number US 9,165,209 B2, USA, October 20, 2015.

[P10] Young Min Tai, Young Su Moon, Junguk Cho, Joon Hyuk Cha, Hyun Sang Park, and Shi Hwa Lee, "**Apparatus and method extracting feature information of a source image**," Patent Number US 9,171,227 B2, USA, October 27, 2015.

[P11] Yong Min Tai, Young Su Moon, Shi Hwa Lee, and Junguk Cho, "**Apparatus and method of reducing noise of image**," Patent Number US 9,185,376 B2, USA, November 10, 2015.

[P12] Junguk Cho, Seung Yong Lee, Young Su Moon, Shi Hwa Lee, Chi Young Lee, Sung Hyun Cho, and Ho Jin Cho, "**Method and apparatus for robust estimation of non-uniform motion blur**," Patent Number US 9,189,835 B2, USA, November 17, 2015.

[P13] Young Su Moon, Yong Min Tai, Shi Hwa Lee, Gyeong Ja Jang, and Junguk Cho, "**Method and apparatus for processing image taken under low illumination environment**," Patent Number US 9,224,190 B2, USA, December 29, 2015.

[P14] Youngsu Moon, Jonghun Lee, Junguk Cho, Yongmin Tai, Dohyung Kim, and Sihwa Lee, "**Image processing method and apparatus**," Patent Number US 9,679,223 B2, USA, June 13, 2017.

[P15] Jonghun Lee, Yongsu Moon, Junguk Cho, Yongmin Tai, Dohyung Kim, and Sihwa Lee, "**Apparatus and method of processing numeric calculation**," Patent Number US 9,760,339 B2, USA, September 12, 2017.

[P16] Junguk Cho, Youngsu Moon, Jonghun Lee, Yongmin Tai, Dohyung Kim, and Sihwa Lee, "**Image processing apparatus and method for vector data**," Patent Number US 9,892,090 B2, USA, February 13, 2018.

United States Patent Applications

[P1] Jung Uk Cho, Seung Yong Lee, Sung Hyun Cho, Shi Hwa Lee, Young Su Moon, and Ho Jin Cho, "**Method and Apparatus for Removing Non-uniform Motion Blur using Multi-frame**," Application Number US 13/415,285, USA, March 8, 2012.

[P2] Gengyu Ma, Young Su Moon, Junguk Cho, Ji Yeun Kim, and Wentao Mao, "**Three-dimensional (3d) image photographing apparatus and method**," Application Number US 2013/0258059 A1, USA, October 3, 2013.

[P3] Gengyu Ma, Xu Zhang, Jiyeun Kim, Junguk Cho, and Youngsu Moon, "**Augmented reality apparatus and method**," Application Number US 2014/0240354 A1, USA, August 28, 2014.

[P4] Yongmin Tai, Youngsu Moon, Jonghun Lee, Junguk Cho, Dohyung Kim, and Sihwa Lee, "**Method and apparatus for processing image data, and recording medium**," Application Number US 2015/0098658 A1, USA, April 9, 2015.

[P5] Junguk Cho, Sukjin Kim, and Dongkwan Shu, "**Method and apparatus for memory access**," Application Number US 2017/0344369 A1, USA, November 30, 2017.

[P6] Jaeun Park, Jonghun Lee, Kiseok Kwon, Dongkwan Suh, Kangjin Yoon, and Junguk Cho, "**Data input/output unit, electronic apparatus, and control methods thereof**," Application Number US 2018/0101357 A1, USA, April 12, 2018.