Yıldız Technical University
Computer Engineering
2023-2024 Spring
BLM2022 Computer Organization
Homework 1

Question 1) Design the 32-bit ALU defined in Table 1 and shown in Figure 1 using Verilog.

Table 1: ALU fuction table

ALUControl 2:0	**Function**
000	Add
001	Subtract
010	AND
011	XOR
101	SLT (set if less than)

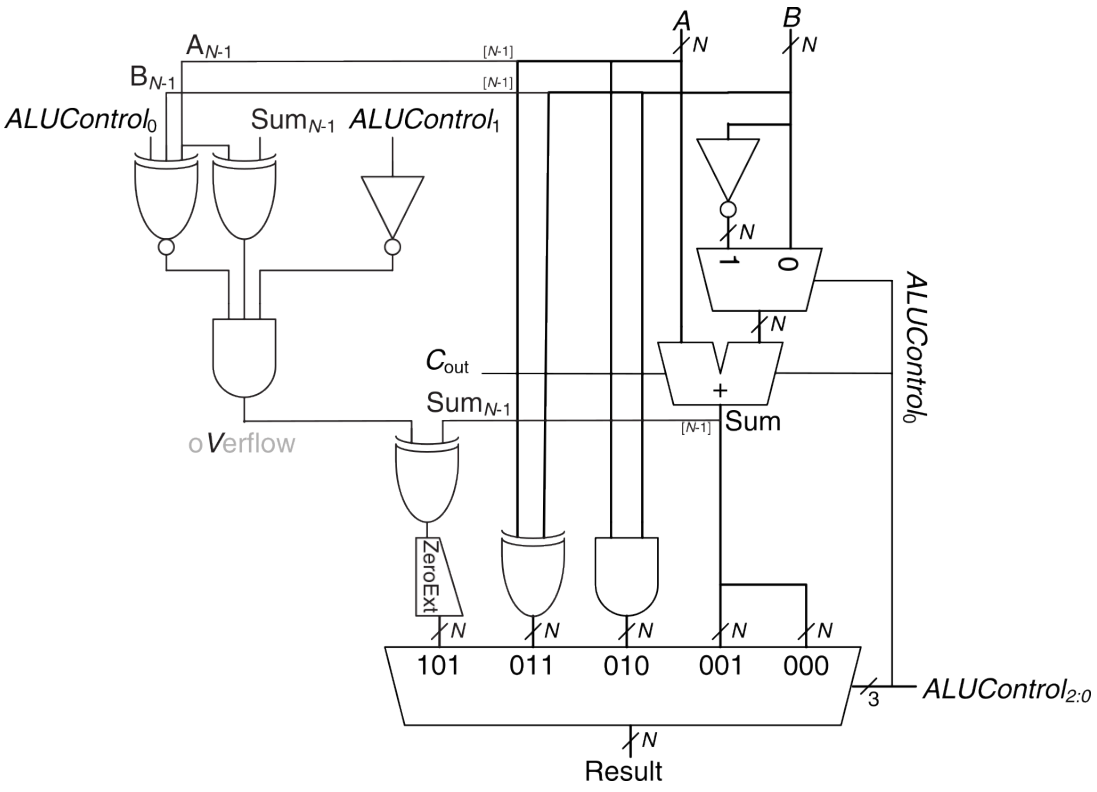


Figure 1: ALU design

Design the ALU components such as ZeroExtender, Adder, Mux in a hierarchical manner, firstly as one bit, four bits and 32 bits modules respectively using only primitive gates. Then compile all components into a top level ALU design. Higher level operators and behaviourial design should not be used.

Write a testbench and check the functionality and correctness of your design.

Submit all module and testbench Verilog files as well as the GtkWave result of the testbench.

Question 2) Using the ALU design from Question 1 and the register file design (it has four 32 bits registers, that will be referred as R0, R1, R2, R3 later on) supplied as attachment, create a Verilog datapath (by connecting corresponding ALU and register file terminals) module.

a) Firstly test yor design with the following basic operations through a testbench file:

R0 ← R1 + R2

R1 ← R2 AND R3

R3 ← R2 XOR R0

R2 ← R1 - R3

b) Then try to list a sequence of (you may reach the required result after several steps) control commands (ALUControl, addr1, addr2, addr3, wr, rst) to be applied to get the following operations through a testbench file:

R1 ← 0 (find a solution that does not use rst)

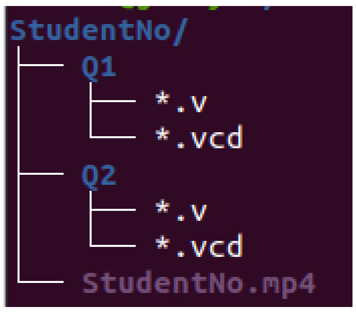
R0 ← -1

R2 ← R1 – 1

R3 ← R0 + 1

Submit all module and testbench Verilog files as well as the GtkWave result of the testbench.

Note: Turn in your answers as [StudentNo].zip file structured as follows with a maximum of 3 minute video explaining your design and testbench results.



```
StudentNo/
├── Q1
│   ├── *.v
│   └── *.vcd
├── Q2
│   ├── *.v
│   └── *.vcd
└── StudentNo.mp4
```