

ECNU

The Design and Implementation of Fast Fourier Transform (FFT) based on AIEs

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CCFSys Customized Computing Challenge 2023



CONTENTS

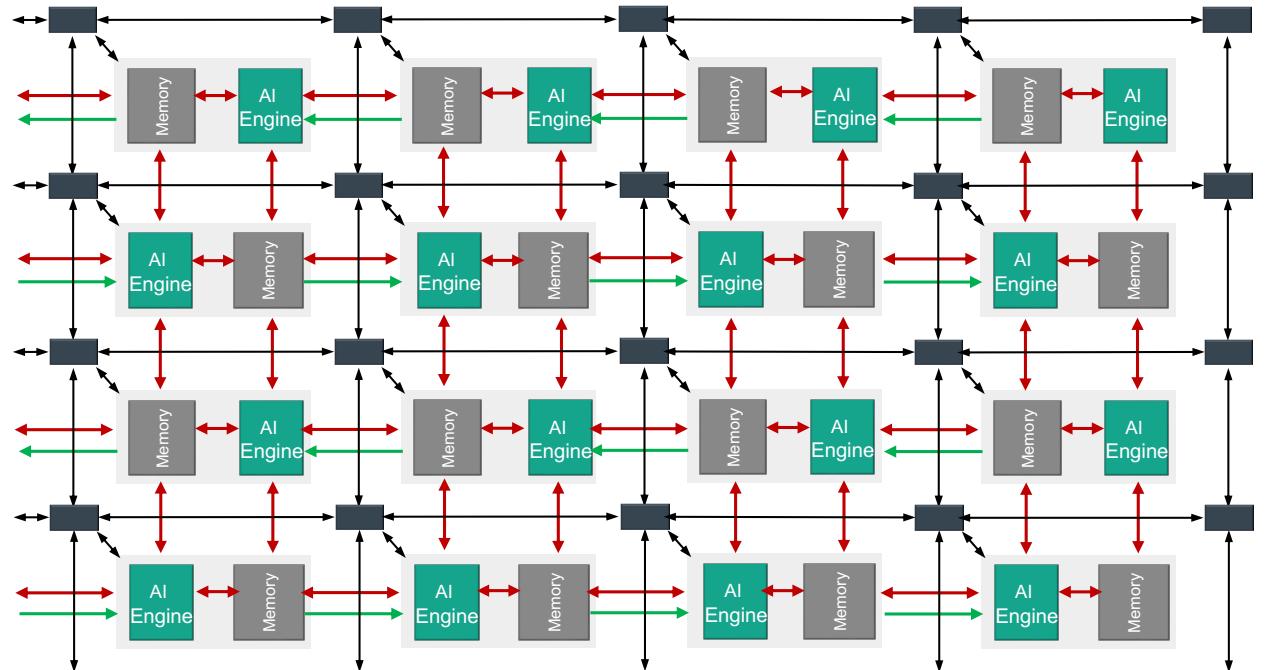
1 / Overview

2 / Algorithm

3 / Implementation

4 / Analysis





- 1 / Overview
- 2 / Algorithm
- 3 / Implementation
- 4 / Analysis



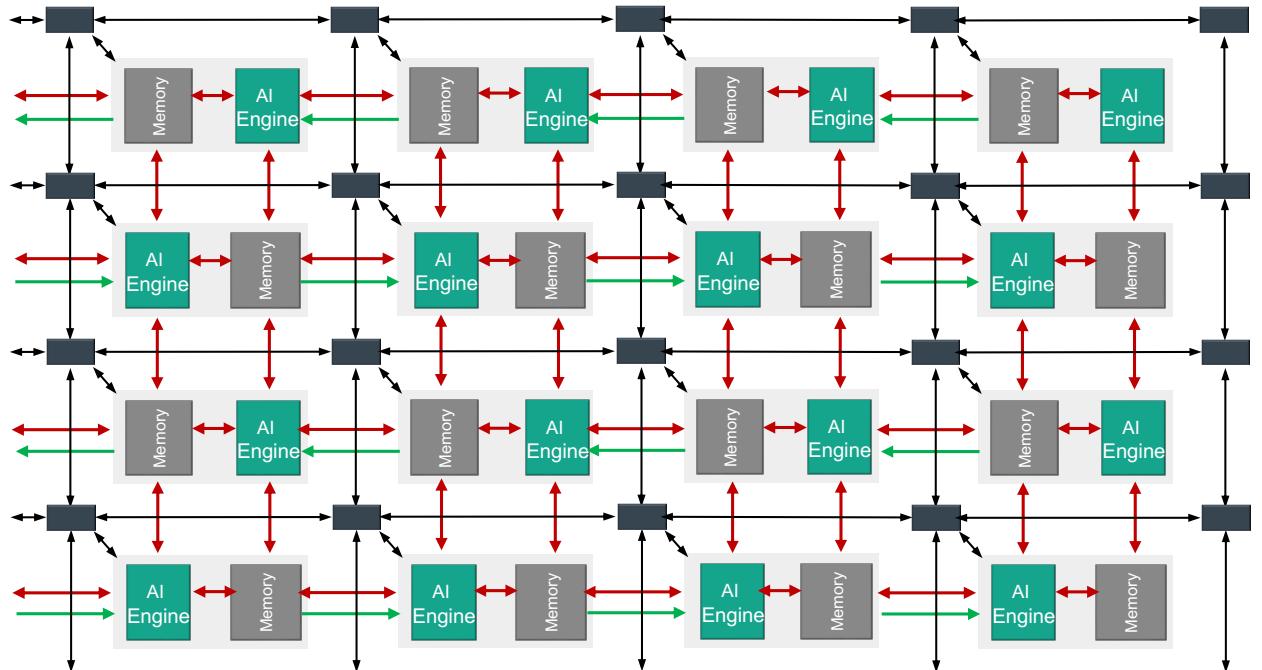


Overview

Point Size	Number of AIE	Data Type	Twiddle Type
1,024	1	cint16	cint16
		cfloat	cfloat
4,096	5	cint16	cint16
8,192	9	cint16	cint16

- Algorithm
 - ✓ **non-recursive FFT , distributed FFT**
- Kernel Design
 - ✓ **ping-pong buffer , sliding multiplication**
- Graph Design
 - ✓ **kernel connection , kernel placement**



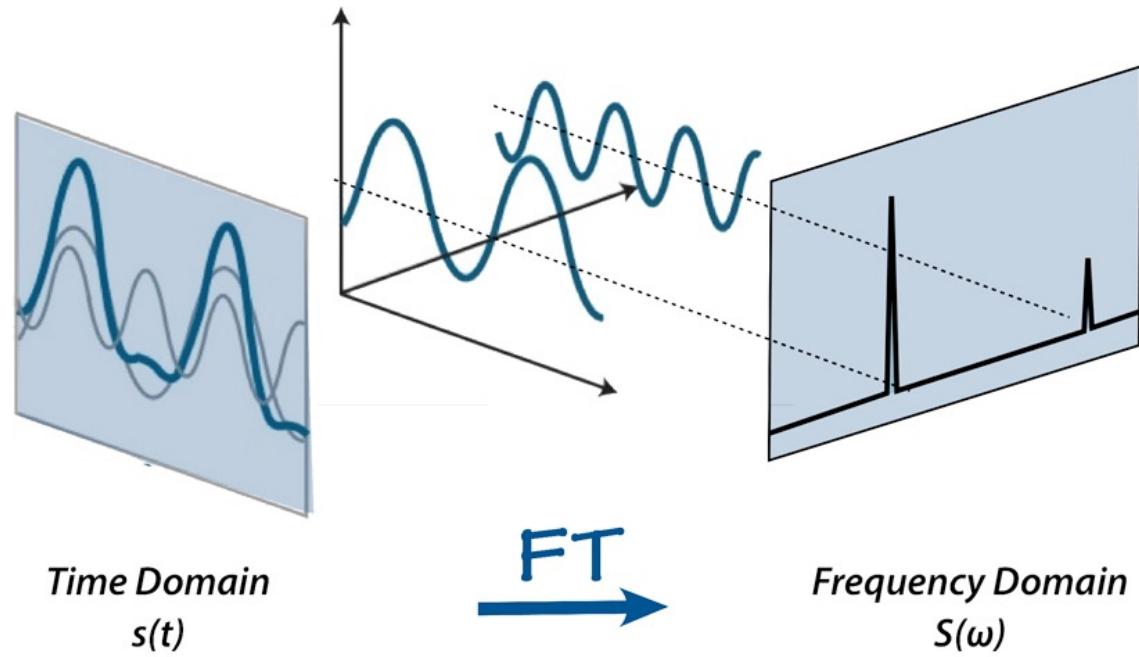


- 1 / Overview
- 2 / Algorithm
- 3 / Implementation
- 4 / Analysis





Fast Fourier Transform (FFT)



FFT : $O(N^2) \rightarrow O(N \log N)$

{ Non-recursive FFT → 1024-point
Distributed FFT → Expand point size



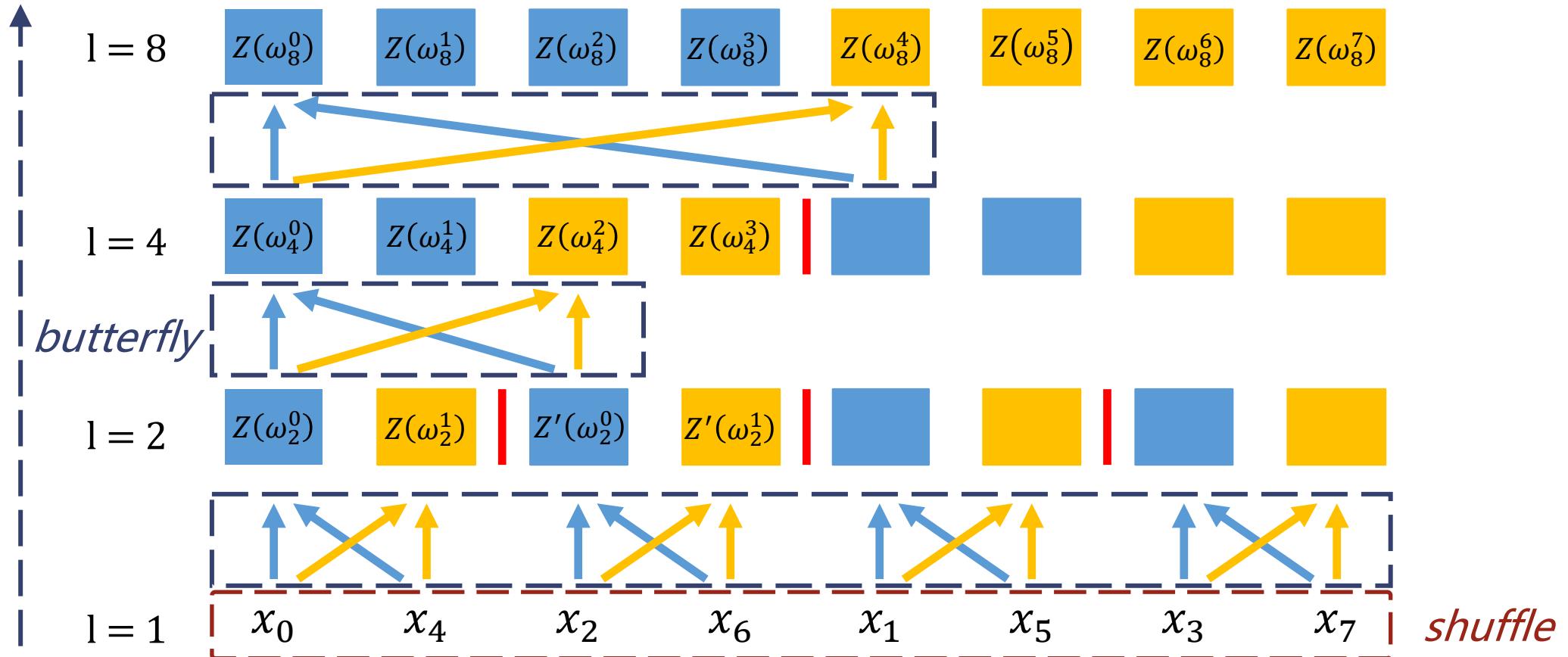


Non-recursive FFT

Key operations : shuffle and butterfly

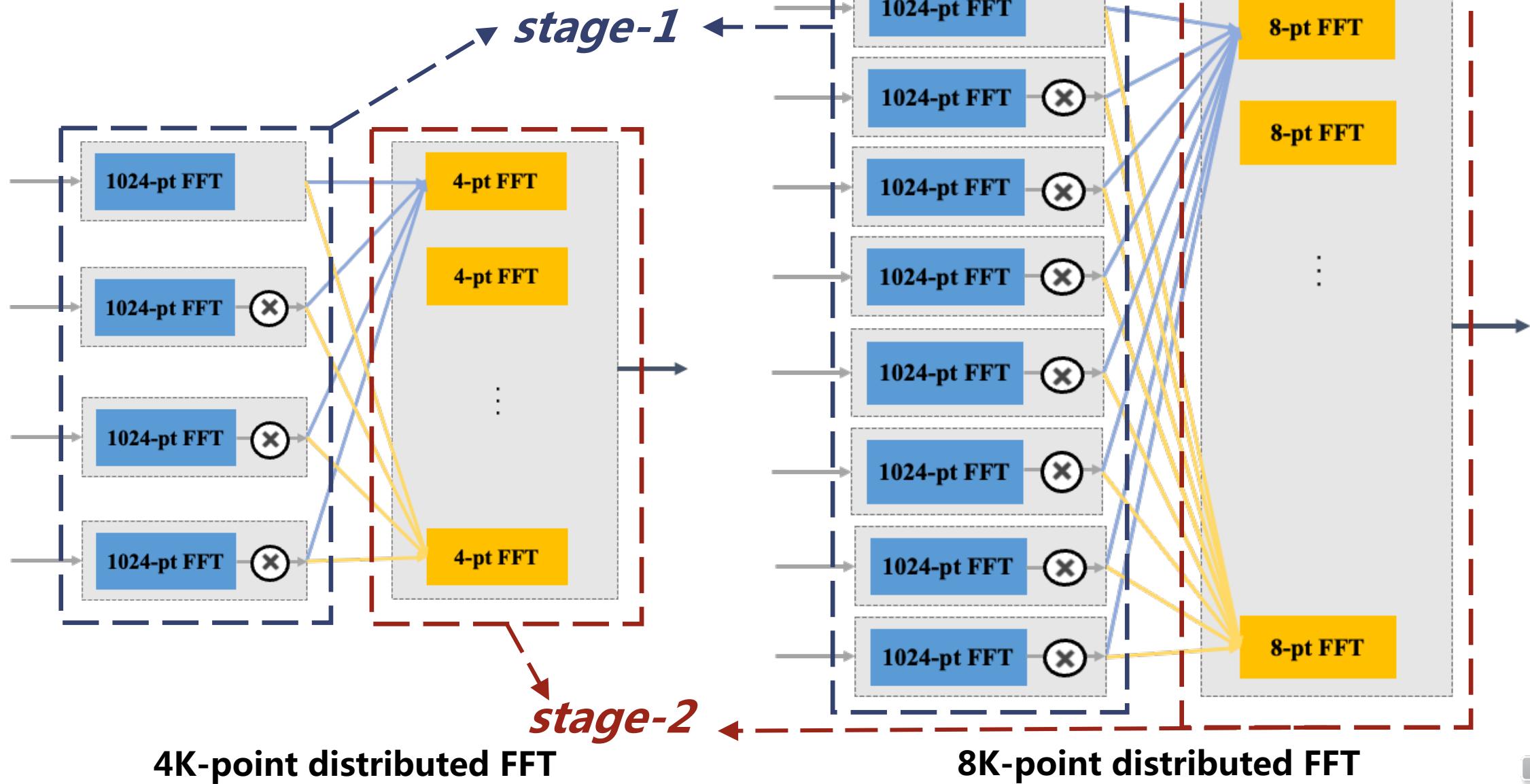
$$X_k = E_k + e^{-\frac{2\pi i}{N}k} O_k$$

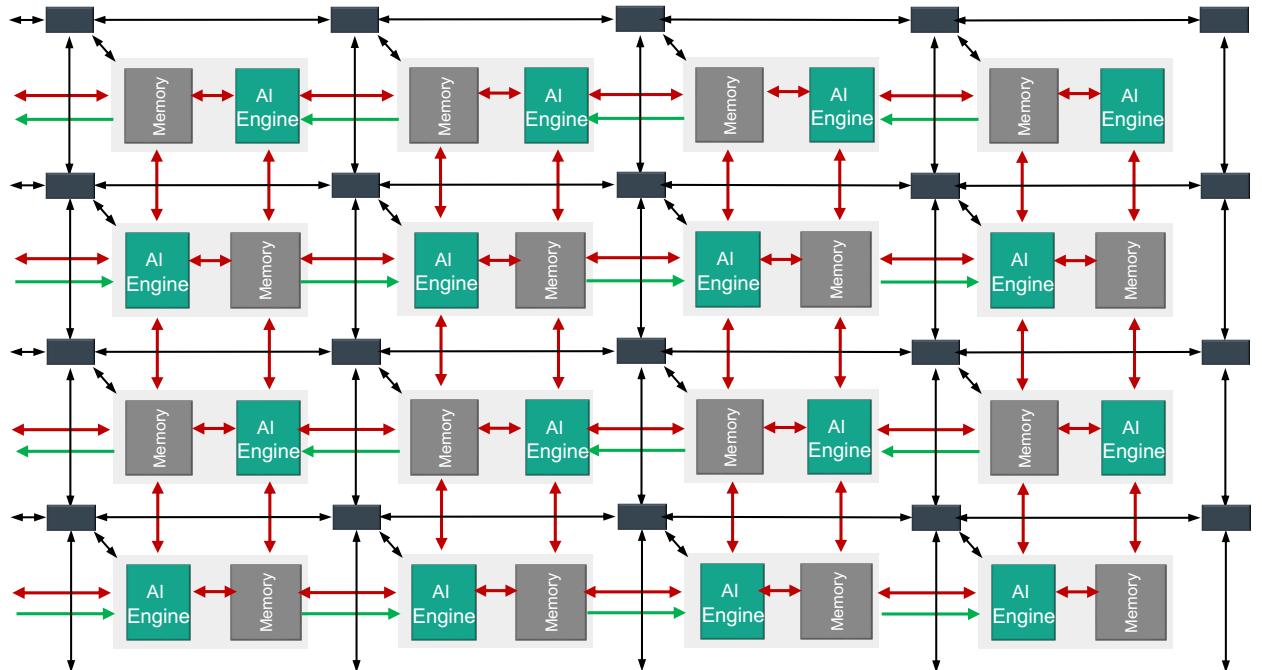
$$X_{k+N/2} = E_k - e^{-\frac{2\pi i}{N}k} O_k$$





Distributed FFT



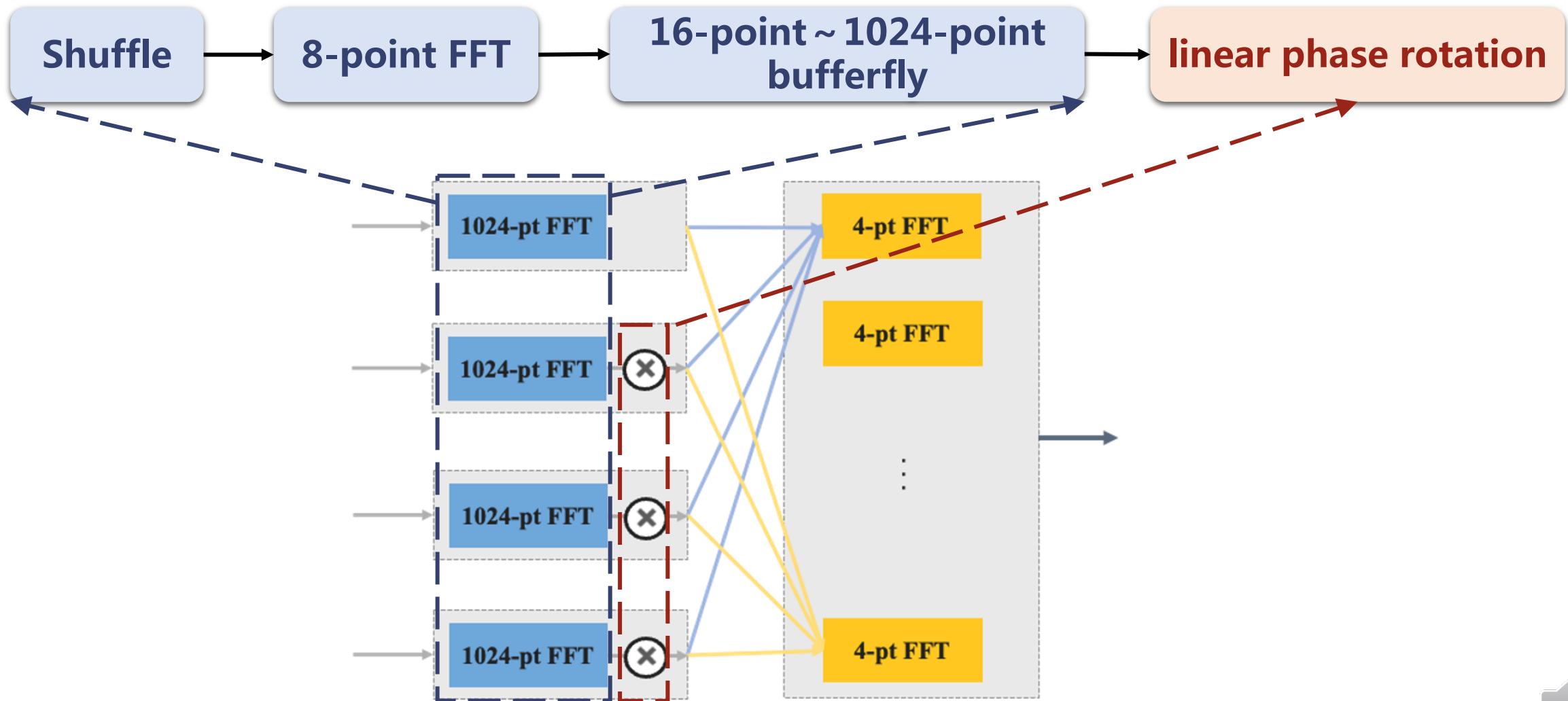


- 1 / Overview
- 2 / Algorithm
- 3 / Implementation
- 4 / Analysis





1K-point FFT (stage-1)





1K-point FFT (stage-1)



- Implement non-recursive 1K FFT based on 8-point FFT
- Shuffle to permute the order of the input signal
- Divide 1024 points into 120 sequences of length 2 and 192 sequences of length 4, and swap the data within each sequence to achieve the shuffle operation
- Use loop unroll for parallel computing



1K-point FFT (stage-1)

64 MACs  **8 instructions**



1	1	1	1	1	1	1	1	1
1	ω^1	ω^2	ω^3	ω^4	ω^5	ω^6	ω^7	
1	ω^2	ω^4	ω^6	ω^8	ω^{10}	ω^{12}	ω^{14}	
1	ω^3	ω^6	ω^9	ω^{12}	ω^{15}	ω^{18}	ω^{21}	
1	ω^4	ω^8	ω^{12}	ω^{16}	ω^{20}	ω^{24}	ω^{28}	
1	ω^5	ω^{10}	ω^{15}	ω^{20}	ω^{25}	ω^{30}	ω^{35}	
1	ω^6	ω^{12}	ω^{18}	ω^{24}	ω^{30}	ω^{36}	ω^{42}	
1	ω^7	ω^{14}	ω^{21}	ω^{28}	ω^{35}	ω^{42}	ω^{49}	

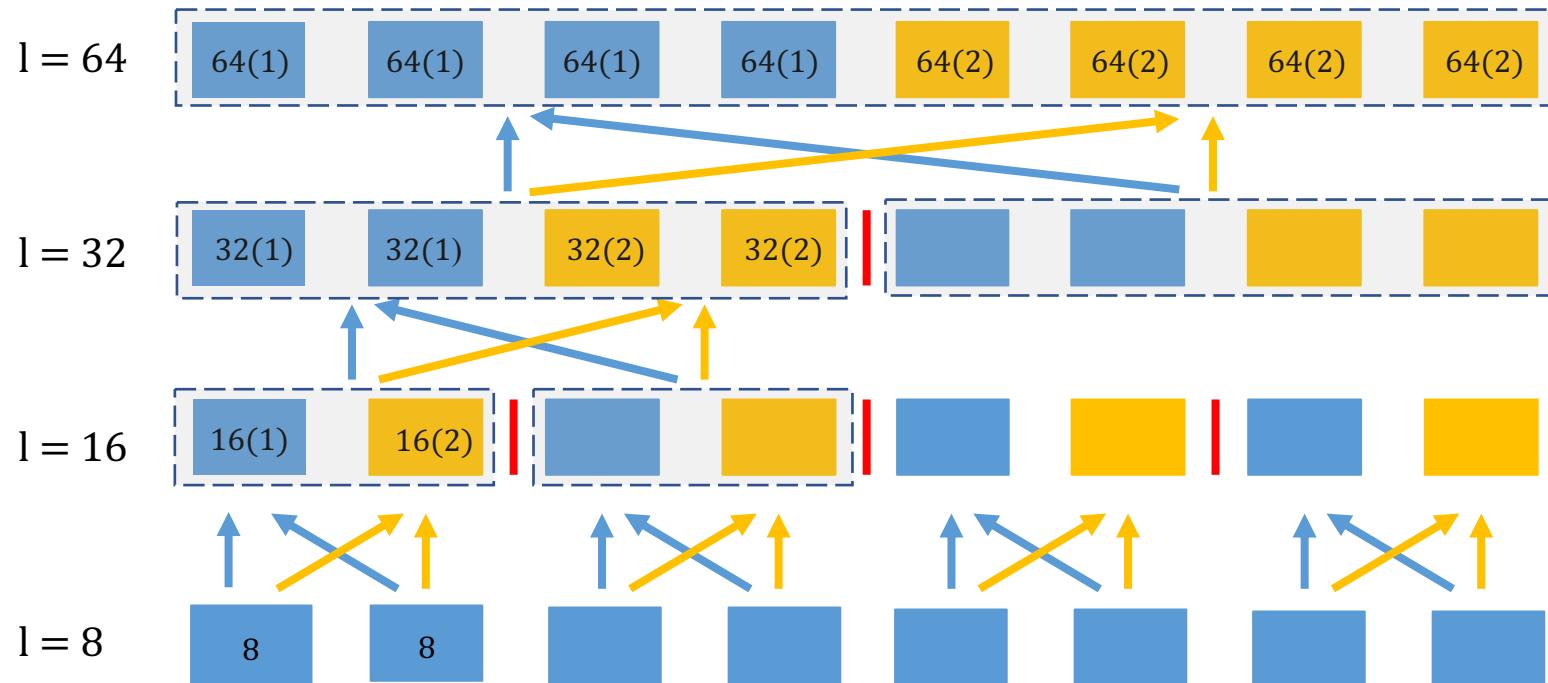
\times = $x_0 \times 1 + x_1 \times \omega^1 + \dots + x_7 \times \omega^{49}$ = $y_0 + y_1\omega + \dots + y_7\omega^{49}$





1K-point FFT (stage-1)

Load as much data as possible to maximize parallelism



$X_k = E_k + e^{-\frac{2\pi i}{N} k} O_k$
$X_{k+N/2} = E_k - e^{-\frac{2\pi i}{N} k} O_k$
Dashed box: Parallel Computing Units





1K-point FFT (stage-1)

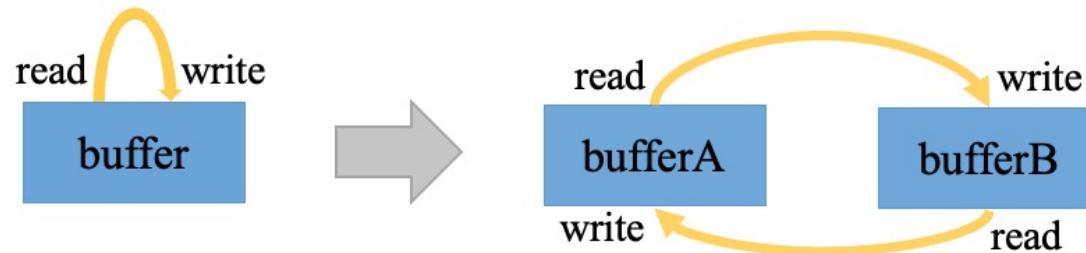
Use Ping-pong buffer to improve mem access efficiency

Shuffle

8-point FFT

**16-point ~ 1024-point
bufferfly**

linear phase rotation



Operation	Read Buffer	Write Buffer
Shuffle	bufferA	bufferB
8-point FFT	bufferB	bufferA
I=16 bufferfly	bufferA	bufferB
I=32 bufferfly	bufferB	bufferA
I=64 bufferfly	bufferA	bufferB
I=128 bufferfly	bufferB	bufferA
I=256 bufferfly	bufferA	bufferB
I=512 bufferfly	bufferB	bufferA
I=1024 bufferfly + linear phase rotation	bufferA	bufferB

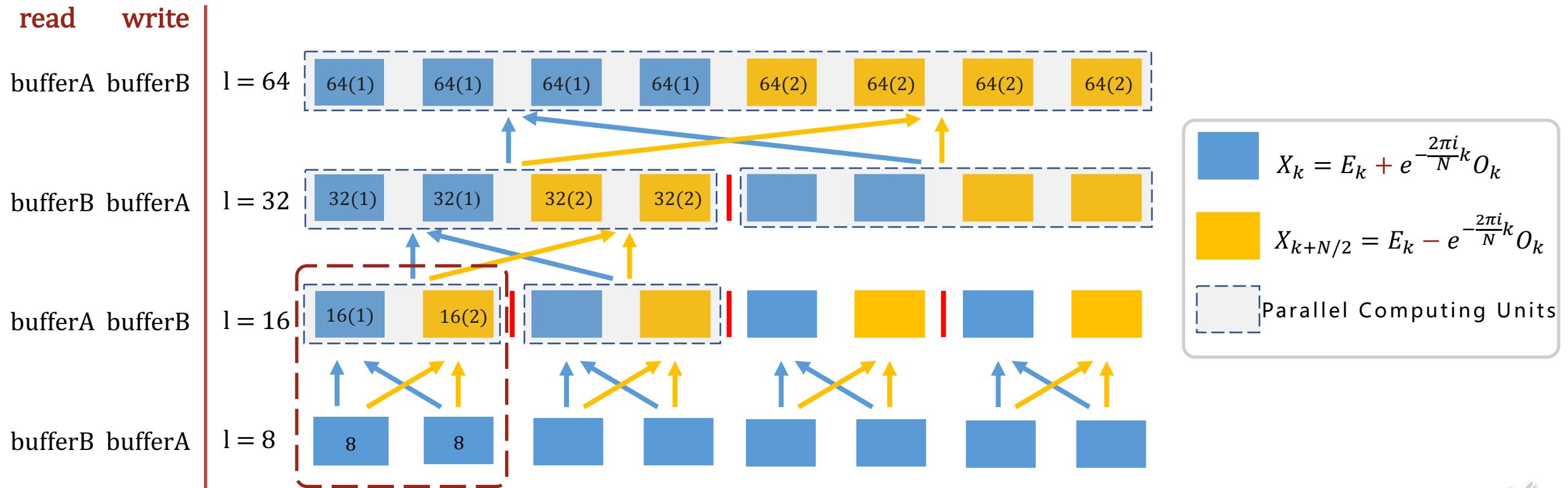




1K-point FFT (stage-1)

Use Ping-pong buffer to improve mem access efficiency

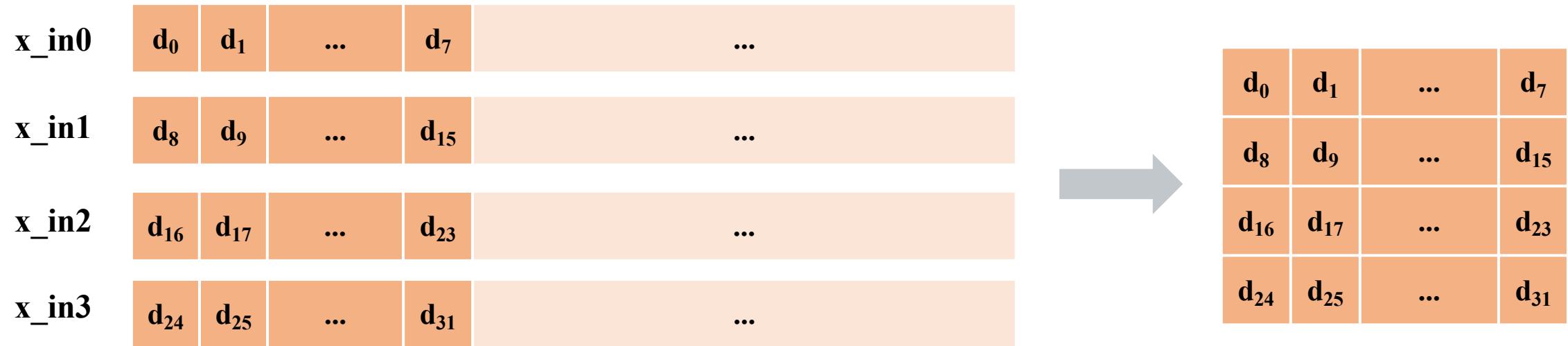
Shuffle → 8-point FFT → 16-point ~ 1024-point bufferfly → linear phase rotation





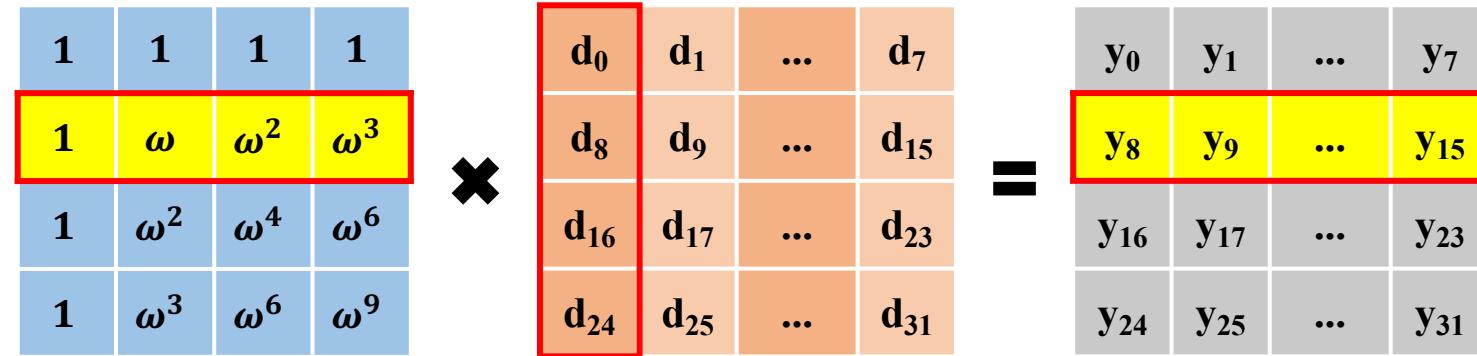
4/8K-point FFT (stage-2)

aie::sliding_mul_ops





4/8K-point FFT (stage-2)



aie::sliding_mul_ops ↓

d_0	d_1	...	d_7	d_8	d_9	...	d_{15}	d_{16}	d_{17}	...	d_{23}	d_{24}	d_{25}	...	d_{31}
1				ω				ω^2				ω^3			
	1				ω				ω^2			ω^3			
		⋮				⋮				⋮			⋮		
			1				ω				ω^2			ω^3	

$$y_8 = 1 \cdot d_0 + \omega \cdot d_8 + \omega^2 \cdot d_{16} + \omega^3 \cdot d_{24}$$

$$y_9 = 1 \cdot d_1 + \omega \cdot d_9 + \omega^2 \cdot d_{17} + \omega^3 \cdot d_{25}$$

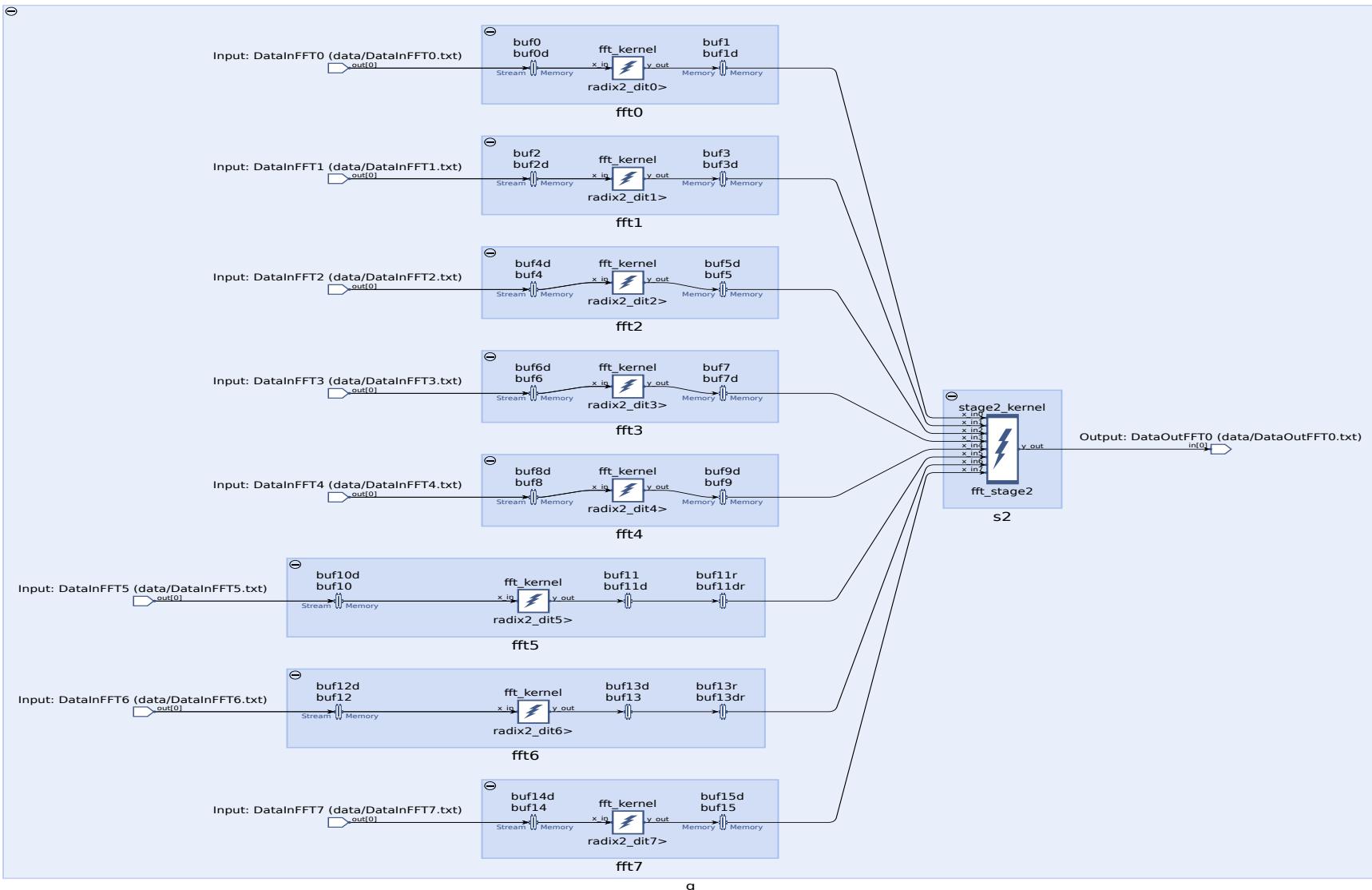
:

$$y_{15} = 1 \cdot d_7 + \omega \cdot d_{15} + \omega^2 \cdot d_{23} + \omega^3 \cdot d_{31}$$



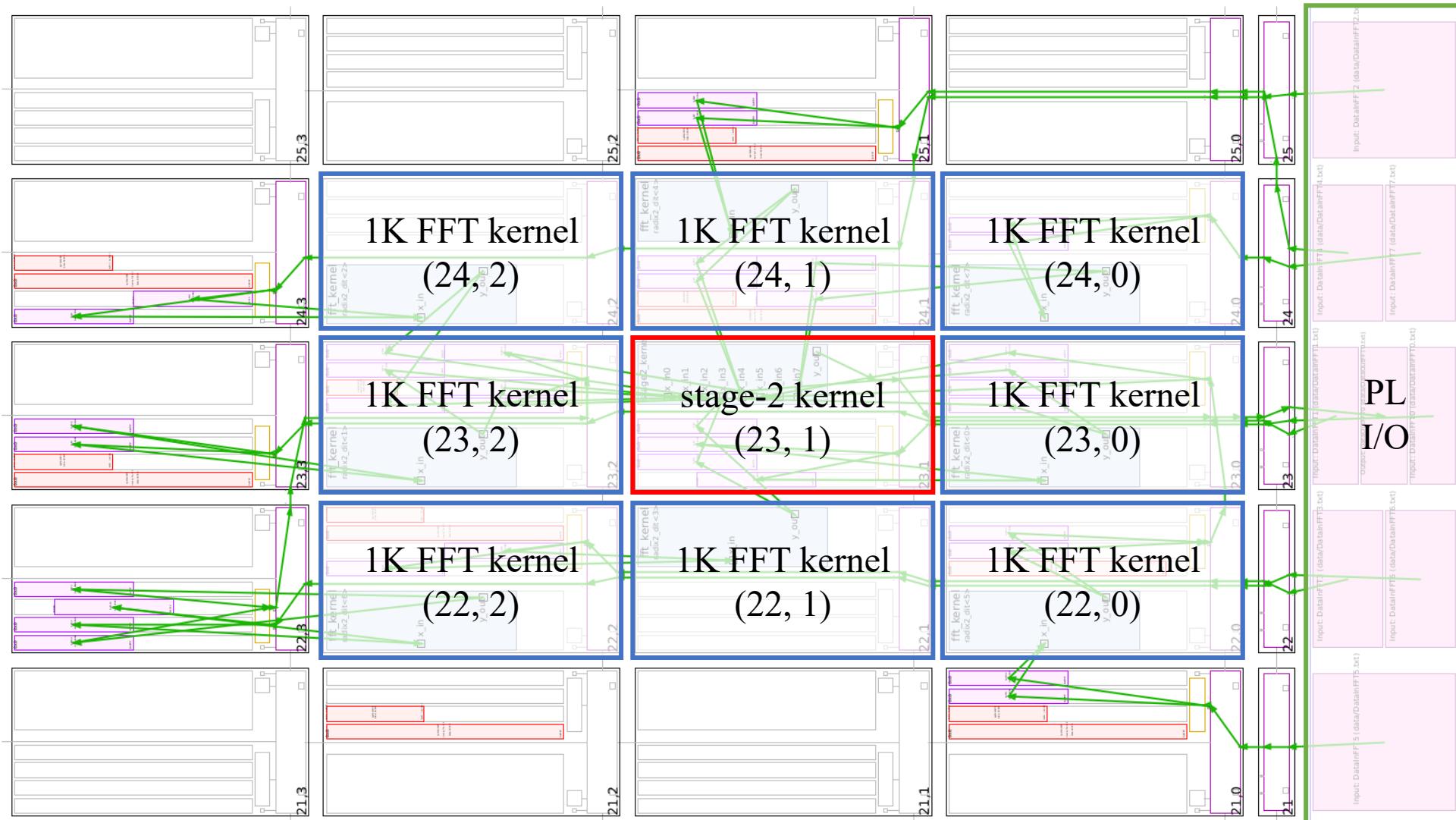


8K-point FFT Graph



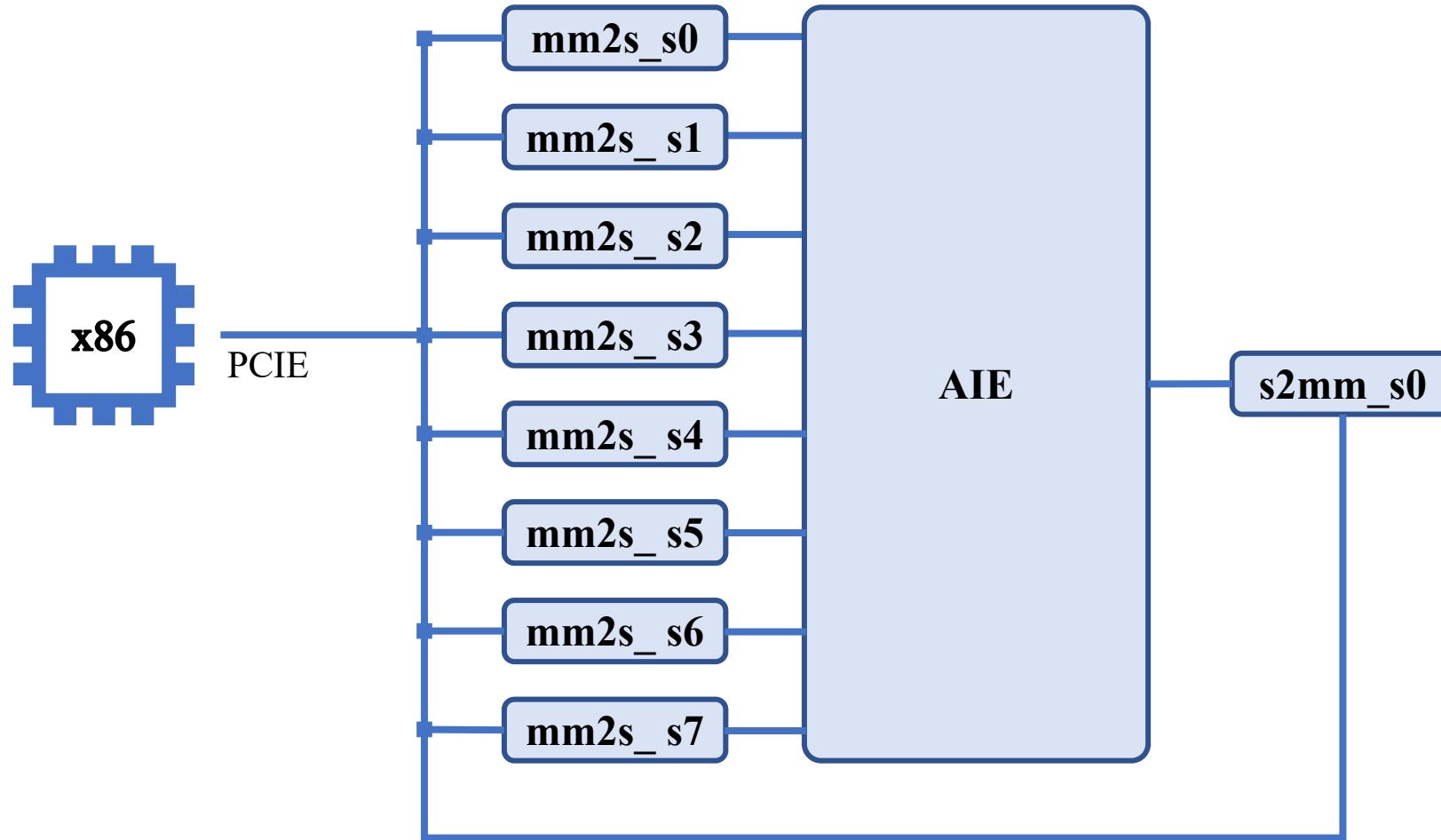


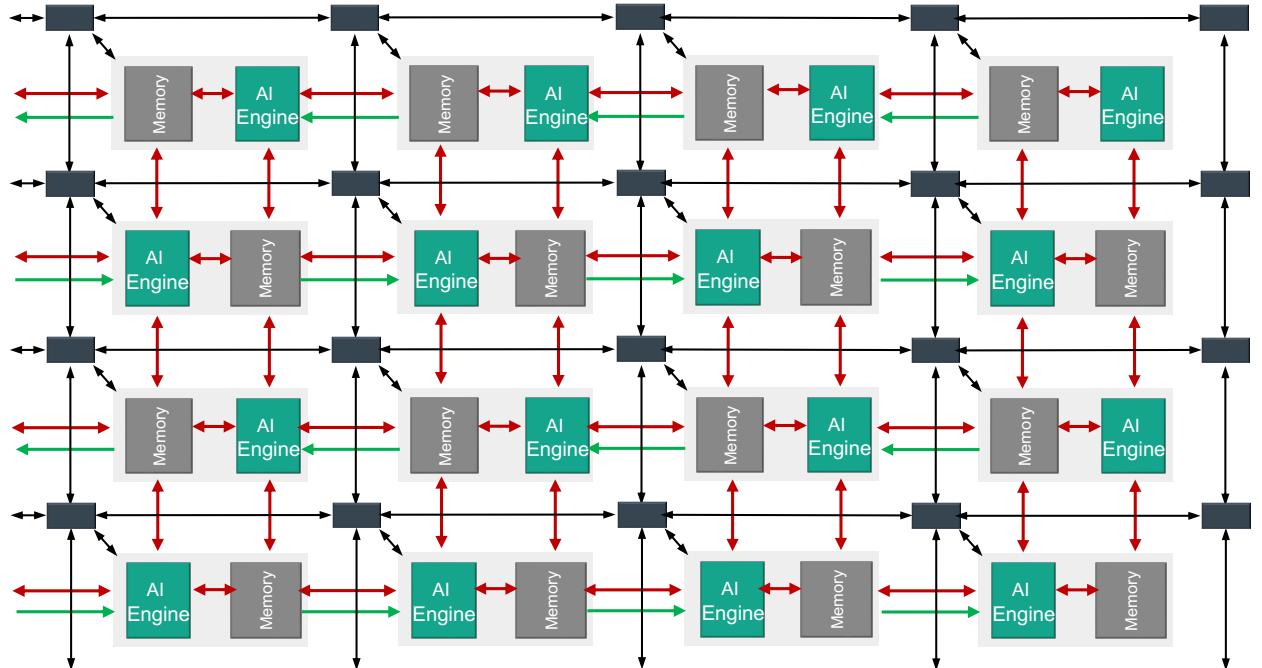
8K-point FFT Array Layout (Kernel Placement Optimization)





PL Implementation





- 1 / Overview
- 2 / Algorithm
- 3 / Implementation
- 4 / Analysis



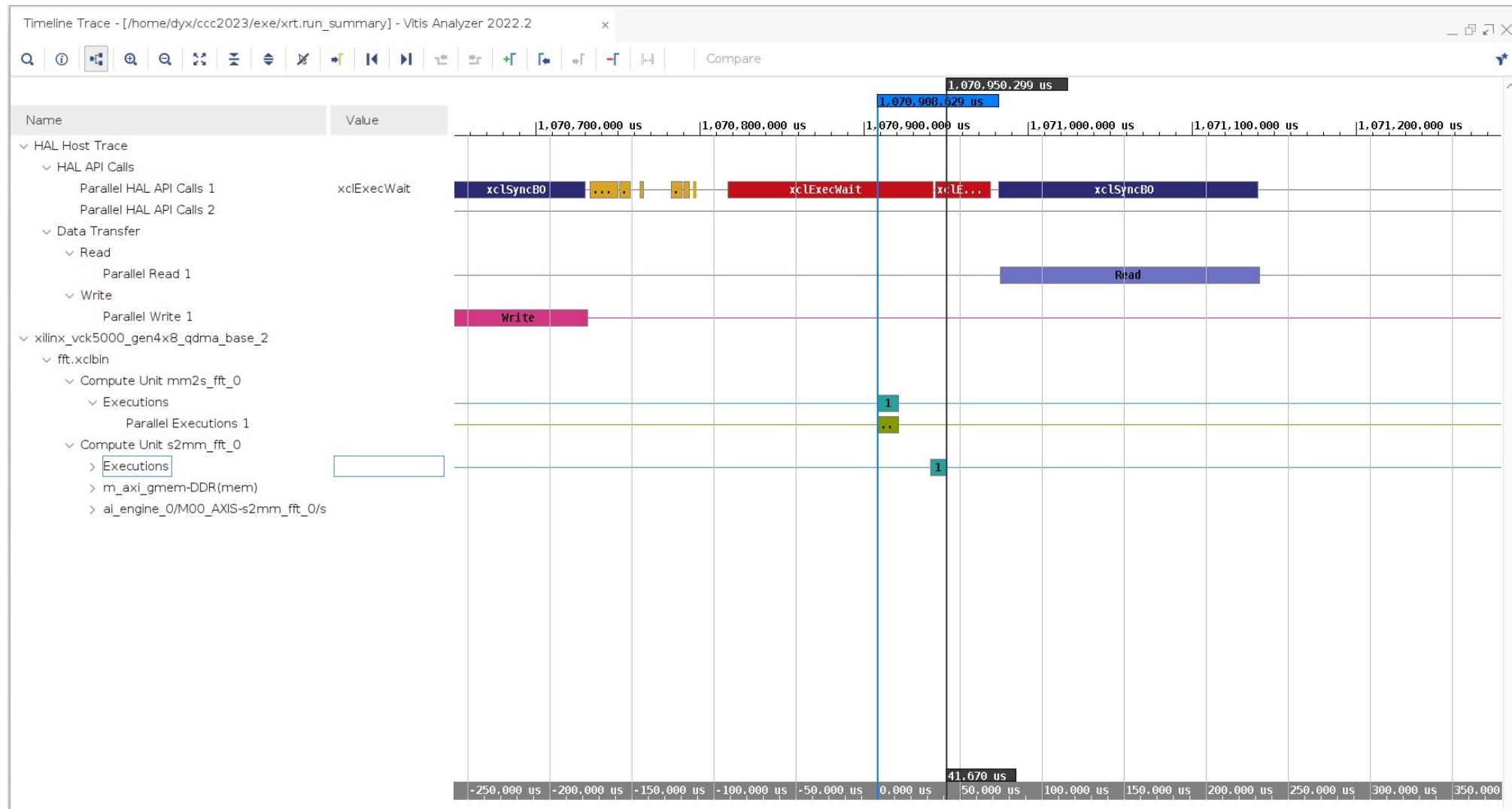


Performance Analysis

Point Size	Number of AIE	Data Type	Twiddle Type	AIE Runtime (us)	Throughput (Msps)
1,024	1	cint16	cint16	6.588	1254.90
		cfloat	cfloat	29.840	626.22
4,096	5	cint16	cint16	9.764	5009.80
8,192	9	cint16	cint16	16.174	976.73

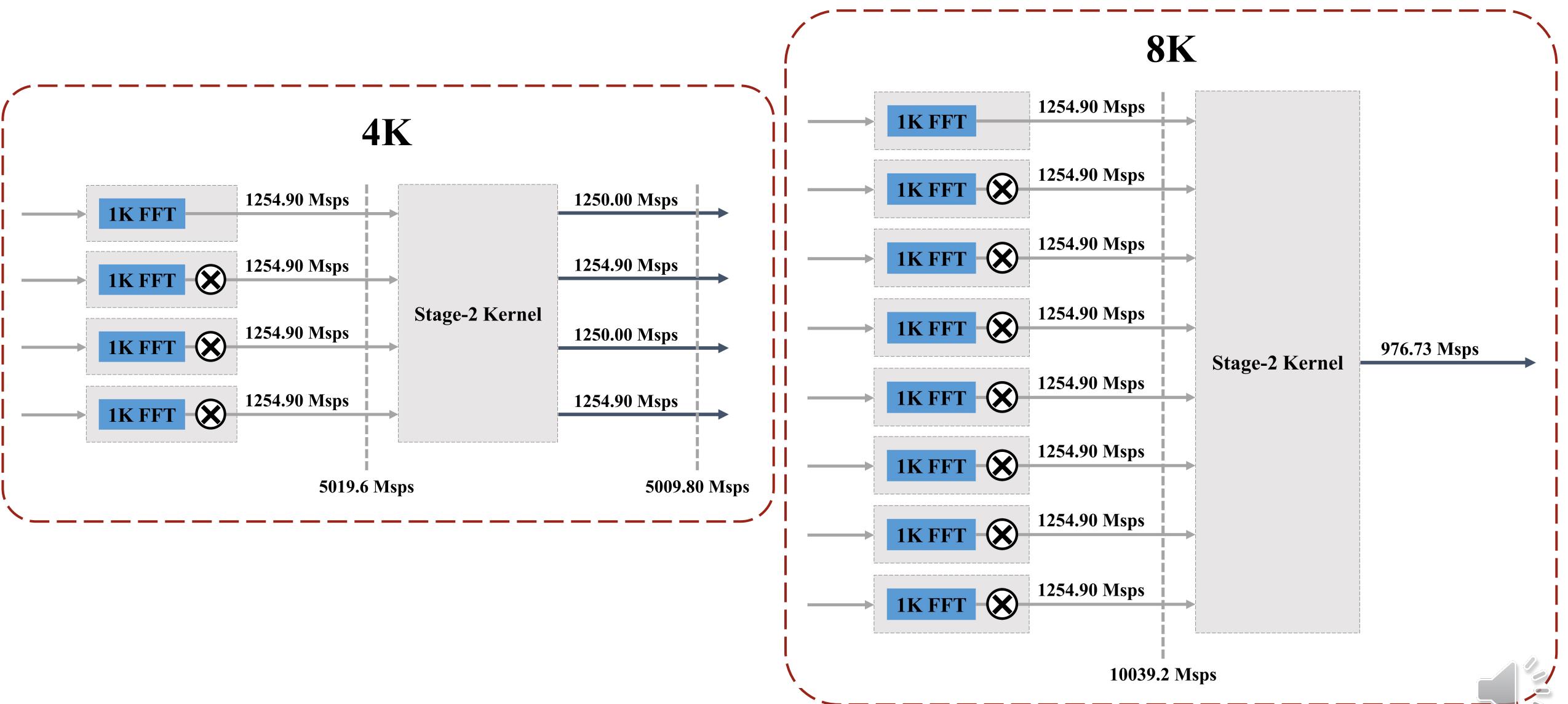


Trace





Throughput





Summary

- We implemented **non-recursive 1K FFT** and **4K/8K FFT** based on a distributed FFT algorithm.
- We implemented PL and host so that this project can run on VCK5000.

Key Optimization

- **Loop opt:** loop unroll and pipelining
- **Parallel computing:** sliding multiplication
- **Ping-Pong Buffer:** improve memory access efficiency

Future Improvement

- **Precision:** adapt to larger point size
- **Resource allocation:** explore better PL (currently used only for data transmission) and AIE resource allocation





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THANKS FOR ALL

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