PW-XXXXX	A

CHANGE LETTER	D'WN BY	CH'K BY	APP'D BY	DATE	D.C.N. & DESCRIPTION

ML605 to USRP FMC Card

Note: Designed to work on the Xilinx ML605 HPC FMC Slot

However, wired for other configurations:
ML605 HPC - Full Functionality
ML605 LPC - 1 Mictor, 1 miniSAS
SP605 LPC - 1 Mictor, 1 miniSAS
SP601 LPC - 1 Mictor

DATE	FILENAME	PCB PW#	SHEET#

USED ON

NEXT ASSEMBLY

WEIGHT

SCALE

CLASSIFICATION

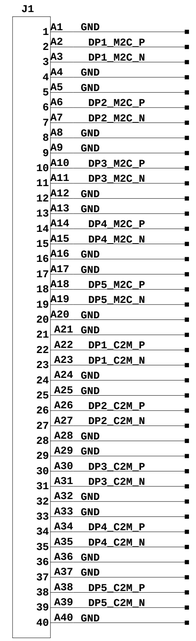
APPROVALS		DATE
	DRAWN FOR	
	DRAWN BY	
	CHECKED BY	
	PROJECT	
	ENGINEER	
	MATL & PROCESS	
	STRUCTURES	
	THERMAL	
	MECH. ANALYSIS	

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON, MASSACHUSETTS
FOR UNITED STATES GOVERNMENT USE ONLY

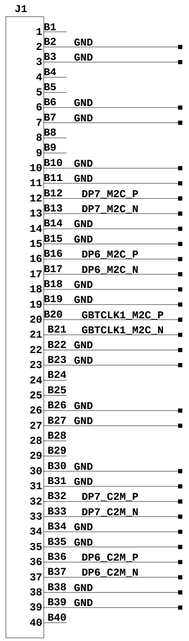
SCHEMATIC DIAGRAM
DRAWING NAME

PROG-TASK	DWG SIZE	DWG NO.	REV
	D		

FMC IO Connections



HPC Only



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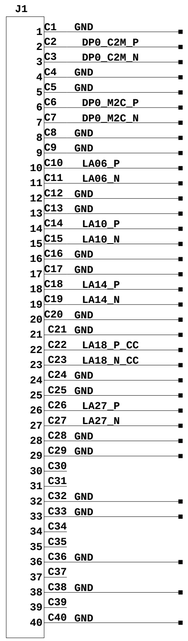
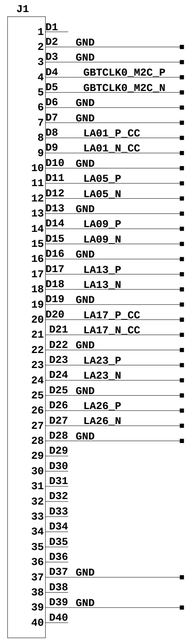
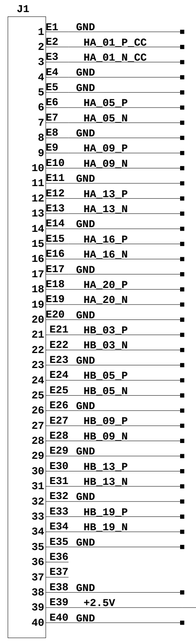


HPC & LPC



HPC & LPC



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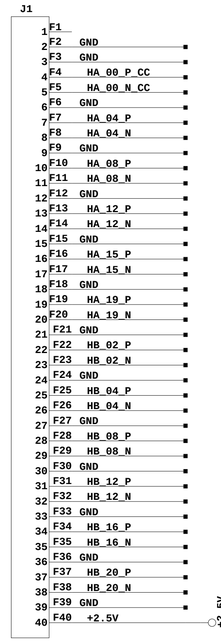

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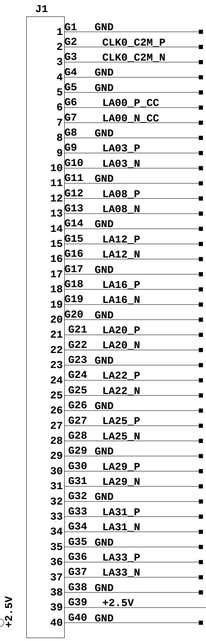
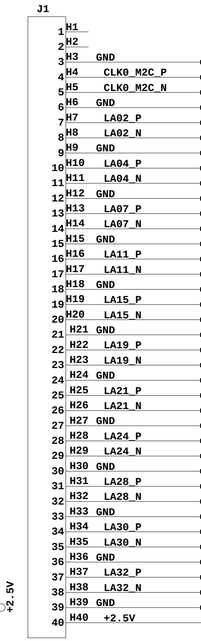
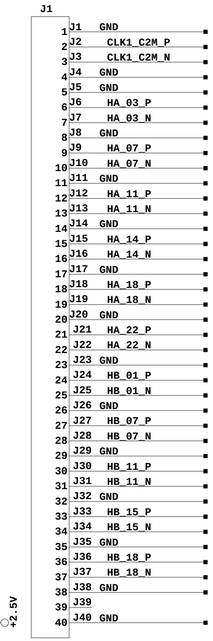


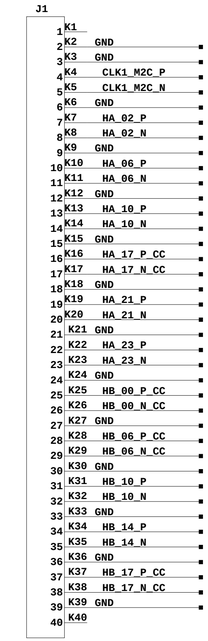
HPC & LPC



HPC & LPC



HPC Only



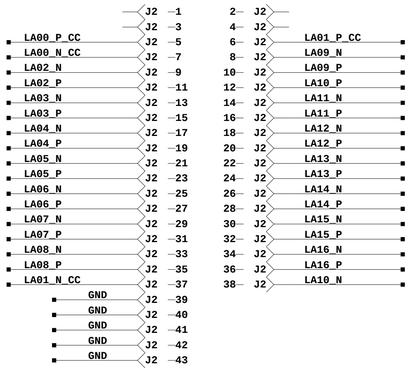
HPC Only

D		
DWG SIZE	DWG NO.	REV

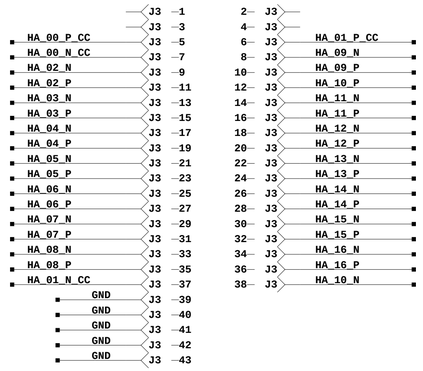
SHEET 2 OF 2

Mictor Connectors

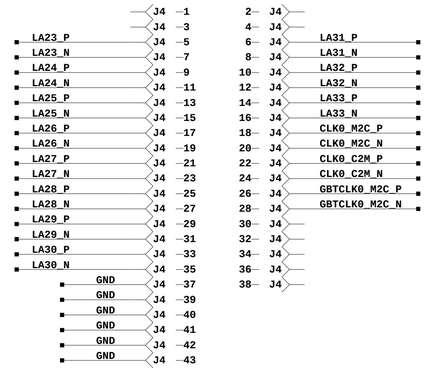
LPC USRP Mictor



HPC USRP Connector



LPC Spare IO Connector



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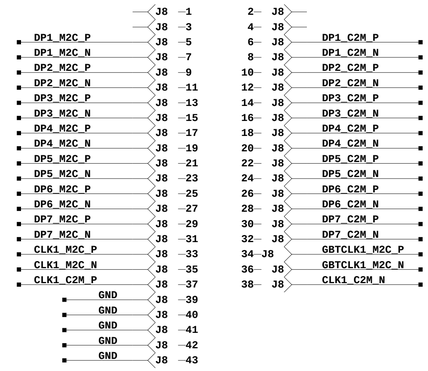
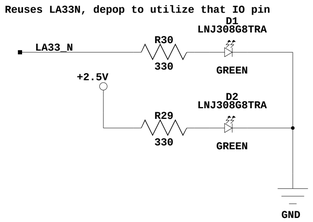


Power and IO LED, NOTE: Reuses LA33N, depop to utilize that IO pin



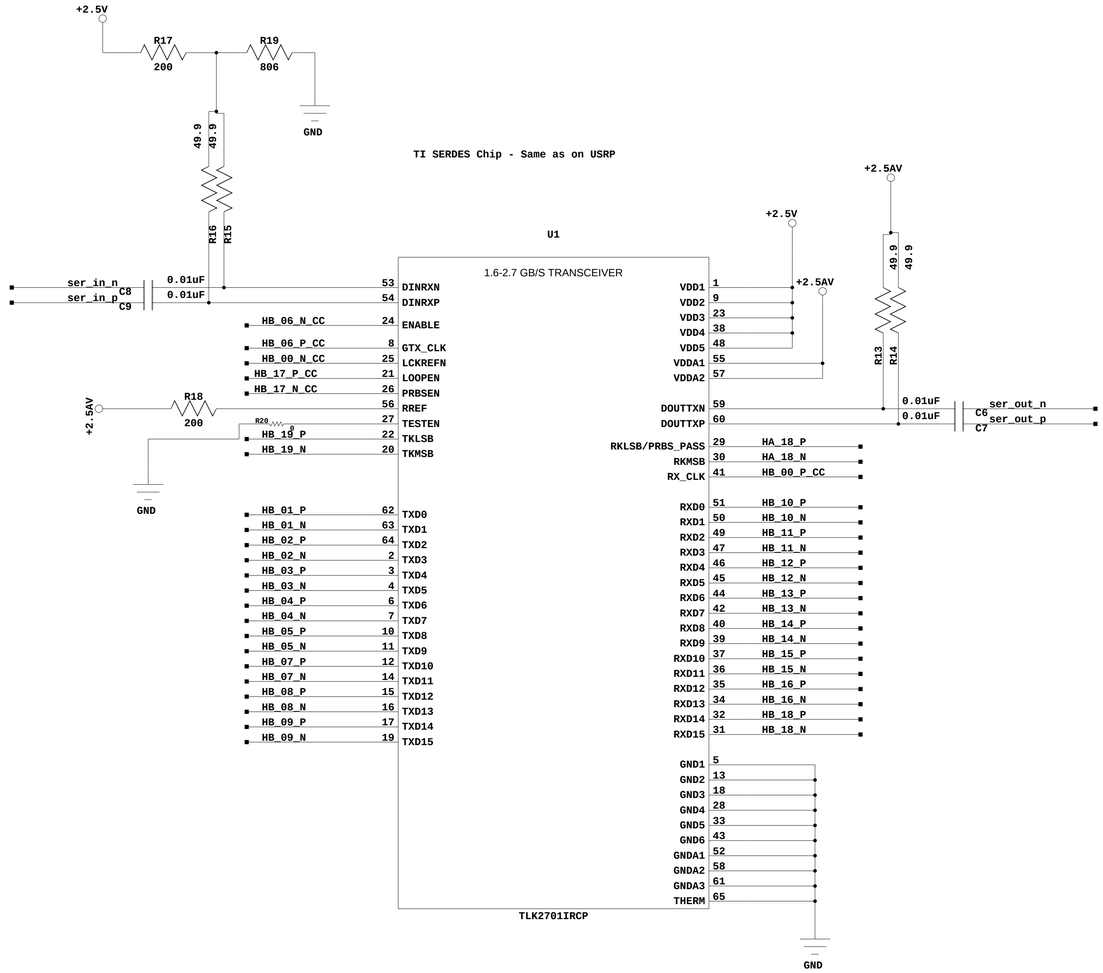
D		
DWG SIZE	DWG NO.	REV

SHEET 4 OF 4

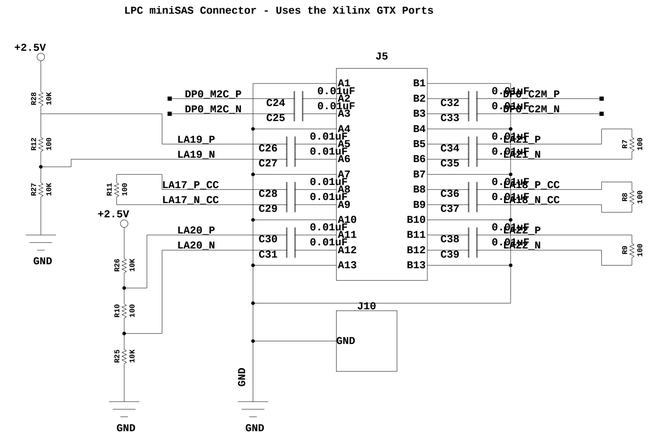
SERDES Connections

D-

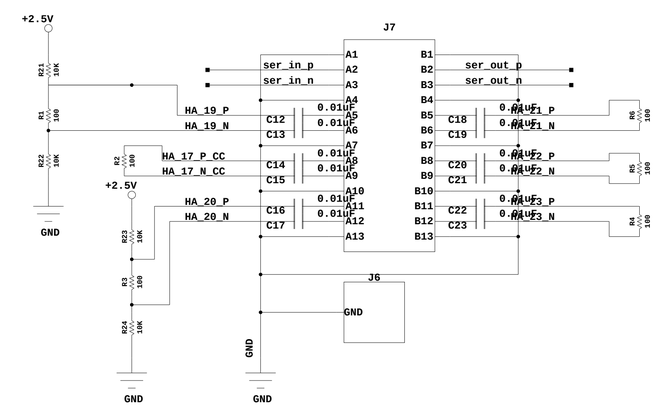
TI SERDES Chip - Same as on USRP



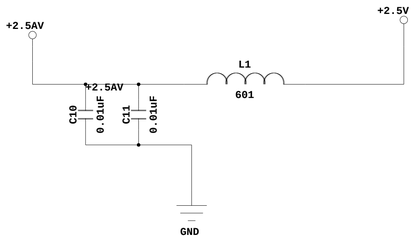
LPC miniSAS Connector - Uses the Xilinx GTX Ports



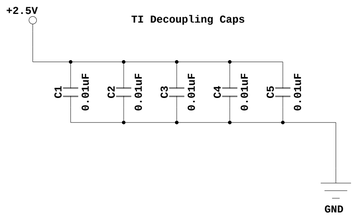
HPC miniSAS Connector - Uses USRP TI SERDES Chip



Isolate Analog Voltage



TI Decoupling Caps



D		
DWG SIZE	DWG NO.	REV

SHEET 5 OF 5