ATE305 Control Guide Part 2

Daniel 2017/4/18 Initial Version

New PEB Pin Driver (ATE305)有多種功能，本篇將會敘述之後 API 所必需的 Register 控制。

由於 ATE305 進行精確電壓/電流量測時，僅是橋接路徑，交由 Channel Board 上的 ADC 量測，故我們先說明 Channel Board 的 ADC 量測控制方式。

每一片 Channel Board 有 16 個 Channel，但只有一個 ADC。所以使用 FPGA Select 就可以選擇使用哪個 ADC 進行量測。ADC 的 resolution 為 16-bit，而且有連續量測並進行累加的功能。回讀的量測結果為 32-bit，是由 16-bit 的量測次數與每次 16-bit 資料累加(相乘)的結果。Channel FPGA 的 ADC Register Map 如下:

W	0x039	ADC_CNT[15:0]	// 啟動 ADC 量測，ADC_CNT 為連續量測次數
R	0x039	WORK_POLLING	// WORK_POLLING[0] = 0 表示量測結束
R	0x03A	ADC_DATA[31:16]	// ADC 累加器 Data MSB
R	0x03B	ADC_DATA[15:0]	// ADC 累加器 Data LSB

而 ADC 之回傳值公式如下:

ADC_DATA[31:0] / ADC_CNT[15:0] = ADC_RESULT (ADC 平均值)

Measure_Voltage = [(ADC_RESULT / 65536)x10]-2.5 (單位: V)

Measure_Current = [(Measure_Voltage – 2.5)]/(5R) (單位: A) 阻值 R 隨電流檔位不同而不同

- Range A: R = 15.5 Ohm
- Range B: R = 250 Ohm
- Range C: R = 2.5K Ohm
- Range D: R = 25K Ohm
- Range E: R = 250K Ohm

有了上面這些控制，在進行 PMU 的 Measurement 功能即可使用。每片 Channel Board 有 16CH，共 8 顆 ATE305，每顆 ATE305 有 2 Channel。同一時間只能有一個 measure pin 輸出到 ADC 量測。故每顆 ATE305 的 register 控制中，皆有控制是否輸出 measure pin、若是輸出則輸出 CH0 or CH1 的完整控制。

上面在敘述 Measure 的部分，而 Force 的部分 ATE305 究竟是輸出 VT or HZ or VH or VL 則以下面 Table 為準:

ATE305 Register控制

Registers				Signals		最後輸出結果	
PE Disable DATA[0] ADDR[4:0] = 0x0C	Force VT DATA[1] ADDR[4:0] = 0x0C	Load Enable DATA[1] ADDR[4:0] = 0x0D	Driver High-Z/VT DATA[0] ADDR[4:0] = 0x0D	DATAx	RCVx	Driver State	Load State
1	X	X	X	X	X	High-Z without clamps	Power-down
0	1	X	X	X	X	VT	Power-down
0	0	0	0	0	0	VL	Power-down
0	0	0	0	0	1	High-Z with clamps	Power-down
0	0	0	0	1	0	VH	Power-down
0	0	0	0	1	1	High-Z with clamps	Power-down
0	0	0	1	0	0	VL	Power-down
0	0	0	1	0	1	VT	Power-down
0	0	0	1	1	0	VH	Power-down
0	0	0	1	1	1	VT	Power-down
0	0	1	0	0	0	VL	Active off
0	0	1	0	0	1	High-Z with clamps	Active on
0	0	1	0	1	0	VH	Active off
0	0	1	0	1	1	High-Z with clamps	Active on
0	0	1	1	0	0	VL	Active on
0	0	1	1	0	1	High-Z with clamps	Active on
0	0	1	1	1	0	VH	Active on
0	0	1	1	1	1	High-Z with clamps	Active on

[1] X = don't care.

Channel FPGA控制

首先來敘述紅框部分，Channel FPGA 控制:

當使用 ATE305 之 PMU 功能時，Channel FPGA 必須強制將連結 ATE305 的 DATA 與 IO 設為一個定值，這個動作可以藉由將 Channel FPGA 的任意 Channel 設定為 PMU Mode 來達成:

```
W   0x3C   PMU_MODE[15:0]   // PMU_MODE[x] = 1, 表示 Channel[x] 進入 PMU Mode
R   0x3C   PMU_MODE[15:0]   // Read back Channel PMU Mode Status
```

任意 Channel 進入 PMU Mode 之後，DATA 若設為 1 則代表 ATE305 可能輸出 VH、DATA 若設為 1 則代表 ATE305 可能輸出 VL。

```
W   0x3D   PMU_DATA[15:0]   // PMU_ DATA [x] = 1, 表示 Channel[x] 進入 PMU Drive VH
                            // PMU_ DATA [x] = 0, 表示 Channel[x] 進入 PMU Drive VL
R   0x3D   PMU_DATA[15:0]   // Read back Channel PMU Drive Mode Status
```

任意 Channel 進入 PMU Mode 之後，IO 若設為 1 則代表 ATE305 可能輸出 VT 或是 High-Z、IO 若設為 0 則代表 ATE305 可能輸出 VH 或 VL。在 ATE305 的 spec 中，”IO”被稱為”RCV”。

```
W   0x3E   PMU_IO[15:0]   // PMU_ IO [x] = 1, 表示 Channel[x] 進入 PMU VT or HZ
                          // PMU_ IO [x] = 0, 表示 Channel[x] 進入 PMU VH or VL
R   0x3E   PMU_IO[15:0]   // Read back Channel PMU IO Mode Status
```

回到 ATE305 的控制(藍框部分)，下面說明除了控制各種 DAC 輸出值之外的暫存器控制方式。最後打包成 API 的方式將於 PMU Control Guide 討論說明。

ATE305 Register MAP:

Table 21. PE/PMU Enable (ADDR[4:0] = 0x0C)

Bit	Name	Description
DATA[2]	PMU enable	0 = disable PMU force output and clamps, place PMU in MV mode 1 = enable PMU force output When set to 0, the PMU state bits are ignored, except for PMU sense path (Data[7])
DATA[1]	Force VT	0 = normal driver operation 1 = force driver to V_T See Table 29 for complete functionality of this bit
DATA[0]	PE disable	0 = enable driver functions 1 = disable driver (low leakage) See Table 29 for complete functionality of this bit

Table 22. Channel State (ADDR[4:0] = 0x0D)

Bit	Name	Description
DATA[2]	HV mode select	0 = HV driver in low impedance. 1 = enable HV driver. This bit affects Channel 0 only. Ensure that the Channel 0 bit in SPI write is active. Channel 1 bit in SPI write is don't care.
DATA[1]	Load enable	0 = disable load. 1 = enable load. See Table 29 for complete functionality of this bit.
DATA[0]	Driver high-Z or VT	0 = enable Driver high-Z function. 1 = enable Driver VTERM function. See Table 29 for complete functionality of this bit.

Table 23. PMU State (ADDR[4:0] = 0x0E)[1, 2]

Bit	Name	Description
DATA[9:8]	PMU input selection	00 = V_{DUTGND} (calibrated for 0.0 V voltage reference) 01 = 2.5 V + V_{DUTGND} (calibrated for 0.0 A current reference) 1X = PMUDAC
DATA[7]	PMU sense path	0 = internal sense 1 = external sense
DATA[6]	Reserved	
DATA[5]	PMU clamp enable	0 = disable clamps 1 = enable clamps
DATA[4]	PMU measure voltage or current	0 = measure voltage mode 1 = measure current mode
DATA[3]	PMU force voltage or current	0 = force voltage mode 1 = force current mode
DATA[2:0]	PMU range	0XX = 2 µA range 100 = 20 µA range 101 = 200 µA range 110 = 2 mA range 111 = 32 mA range

[1] Note that when ADDR[4:0] = 0x0C, the PMU enable bit (DATA[2]) = 0, PMU force outputs and clamps are disabled, and the PMU is placed into measure voltage mode. PMU State DATA[9:8] and DATA[6:0] are ignored, and only the DATA[7] PMU sense path is valid.
[2] X = don't care.

Table 24. PMU Measure Enable (ADDR[4:0] = 0x0F)[1]

Bit	Name	Description
DATA[2:1]	MEASOUT01 select	00 = PMU MEASOUT Channel 0 01 – PMU MEASOUT Channel 1 10 = Temp sensor ground reference 11 = Temp sensor
DATA[0]	MEASOUT01 output enable	0 = MEASOUT01 is tristated 1 = MEASOUT01 is enabled

[1] This register is written to or read from when either of the CH[1:0] bits is 1.

Table 25. Differential Comparator Enable (ADDR[4:0] = 0x10)[1]

Bit	Name	Description
DATA[0]	Differential Comparator Enable	0 = differential comparator is disabled; the Channel 0 normal window comparator (NWC) outputs are located on Channel 0 1 = differential comparator is enabled; the differential comparator outputs are located on Channel 0

[1] This register is written to or read from when either of the CH[1:0] bits is 1.

Table 26. DAC16_MON (16-Bit DAC Monitor) (ADDR[4:0] = 0x11)[1]

Bit	Name	Description
DATA[1]	16-Bit DAC mux enable	0 = 16-bit DAC mux is tristated 1 = 16-bit DAC mux is enabled
DATA[0]	16-Bit DAC mux select	0 = 16-bit DAC Channel 0 1 = 16-bit DAC Channel 1

[1] This register is written to or read from when either of the CH[1:0] bits is 1.

Table 27. OVD_CHx Alarm Mask (ADDR[4:0] = 0x12)

Bit	Name	Description
DATA[1]	PMU mask	0 = disable PMU alarm flag 1 = enable PMU alarm flag
DATA[0]	OVD mask	0 = disable OVD alarm flag 1 = enable OVD alarm flag

Table 28. OVD_CHx Alarm State (ADDR[4:0] = 0x13)[1]

Bit	Name	Description
DATA[2]	PMU clamp flag	0 = PMU is not clamped 1 = PMU is clamped
DATA[1]	OVD high flag	0 = DUT voltage < OVD high voltage 1 = DUT voltage > OVD high voltage
DATA[0]	OVD low flag	0 = DUT voltage > OVD low voltage 1 = DUT voltage < OVD low voltage

[1] This register is a read-only register.