Section 28. RTCC with Timestamp

HIGHLIGHTS

This section of the manual contains the following major topics:

28.1 INTRODUCTION

The Real-Time Clock and Calendar (RTCC) hardware module is intended for applications where accurate time must be maintained for extended periods of time with minimum to no intervention from the CPU. The module is optimized for low-power usage in order to provide extended battery lifetime while keeping track of time.

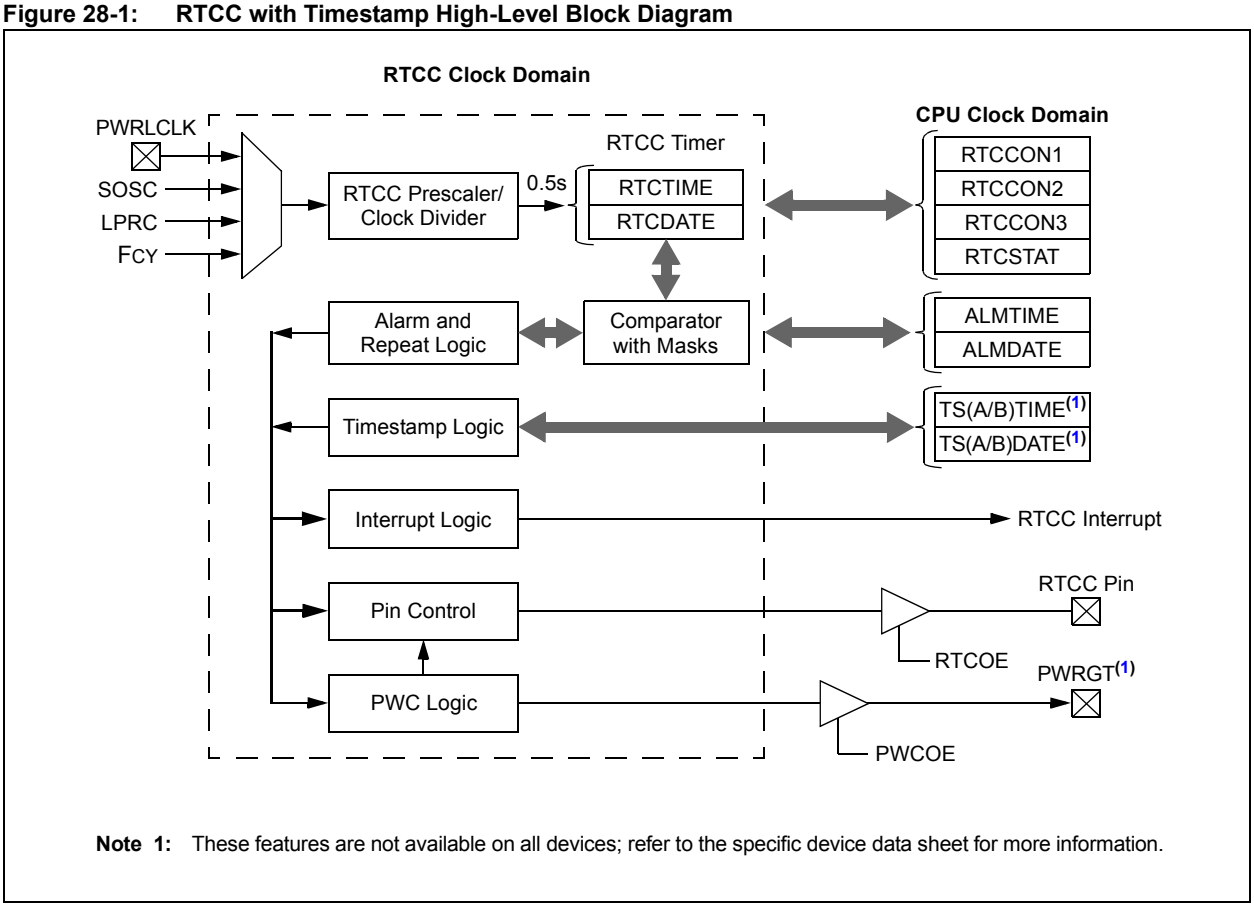
Key features of this module include:

- Time (Hours, Minutes and Seconds) in 24-Hour (Military Time) Format
- Calendar (Weekday, Date, Month and Year)
  - Year Range from 2000 to 2099 with Automatic Leap Year Correction
- Alarm with Configurable Mask and Repeat Options
- BCD Format for Compact Firmware
- Optimized for Low-Power Operation
- Multiple Clock Input Options, Including 32.768 kHz Crystal and Power Line
- User Calibration within 2 ppm when Using a 32 kHz Source
- Interrupt on Alarm and Timestamp Events
- Timestamp Feature for Date and Time Capture from Multiple Trigger Events(1)
- User-Configurable Power Control with Dedicated Output Pin to Periodically Wake External Devices(1)

Note 1: These features are not available on all devices; refer to the specific device data sheet for more information.

The RTCC module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099. The hours are available in 24-hour format. The clock provides a granularity of one second with half second visibility to the user.

Figure 28-1: RTCC with Timestamp High-Level Block Diagram



Note 1: These features are not available on all devices; refer to the specific device data sheet for more information.

28.2 REGISTERS

The RTCC module uses a total of 12 registers, which are organized into four categories.

28.2.1 Control and Status Registers

- RTCCON1 (Register 28-1) is the main control register for the RTCC. Power control features, pin control and alarm functionality are controlled through this register.
- RTCCON2 (Register 28-2) controls the RTCC prescalers; it is used to configure the prescaler to generate the 0.5s signal used to drive the timer. It also controls calibration functions and contains the value of DIV<15:0>, the 16-bit coarse clock divider; the value stored here is used by the RTCC prescaler to generate a nominal 0.5s timer signal.
- RTCCON3 (Register 28-3) controls the Sampling and Stability windows for the power control functionality.
- RTCSTAT (Register 28-4) contains the event flag status bits for timestamps, calibration and timer synchronization.

28.2.2 Time and Date Value Registers

Two registers are used to store the current time and date information in BCD format:

- RTCTIME (Register 28-5) holds the current time hours, minutes and seconds value.
- RTCDATE (Register 28-6) holds the current year, month, day and weekday value.

28.2.3 Alarm Registers

Two registers are used to store the alarm value time and date value. They are formatted identically to the RTCTIME and RTCDATE registers.

- ALMTIME (see Register 28-7 for format).
- ALMDATE (see Register 28-8 for format).

28.2.4 Timestamp Registers

Each of the timestamps (Timestamp A and Timestamp B) has a set of Time and Date registers associated with them. When timestamp data is stored in them, they assume the data formatting associated with the corresponding RTCTIME and RTCDATE registers.

- TSATIME and TSBTIME (see Register 28-9 for format).
- TSADATE and TSBDATE (see Register 28-10 for format).

28.2.5 Register Map

A summary of the registers associated with the RTCC with Timestamp module is provided in Table 28-1.

Table 28-1: RTCC with Timestamp Register Map

Name	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 118/2	Bit 17/1	Bit 16/0
RTCCON1	31:16	ALRMEN	CHIME	—	—	AMASK<3:0>				ALMRPT<7:0>							
	15:0	ON	—	—	—	WRLOCK	PWCEN	PWCPOL	PWCOE	RTCOE	OUTSEL<2:0>			—	—	TSBEN	TSAEN
RTCCON2	31:16	DIV<15:0>															
	15:0	FDIV<4:0>					—	—	—	PWCPS<1:0>		PS<1:0>		—	—	CLKSEL<1:0>	
RTCCON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	PWCSAMP<7:0>								PWCSTAB<7:0>							
RTCSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	CPLCK	—	ALMEVT	TSBEVT	TSAEVT	SYNC	ALMSYNC	HALFSEC
RTCTIME	31:16	—	—	HRTEN<1:0>		HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>			
	15:0	—	SECTEN<2:0>			SECONE<3:0>				—	—	—	—	—	—	—	—
RTCDATE	31:16	YRTEN<3:0>				YRONE<3:0>				—	—	—	MTHTEN	MTHONE<3:0>			
	15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>		
ALMTIME	31:16	—	—	HRTEN<1:0>		HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>			
	15:0	—	SECTEN<2:0>			SECONE<3:0>				—	—	—	—	—	—	—	—
ALMDATE	31:16	—	—	—	—	—	—	—	—	—	—	—	MTHTEN	MTHONE<3:0>			
	15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>		
TSATIME	31:16	—	—	HRTEN<1:0>		HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>			
	15:0	—	SECTEN<2:0>			SECONE<3:0>				—	—	—	—	—	—	—	—
TSADATE	31:16	YRTEN<3:0>				YRONE<3:0>				—	—	—	MTHTEN	MTHONE<3:0>			
	15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>		
TSBTIME	31:16	—	—	HRTEN<1:0>		HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>			
	15:0	—	SECTEN<2:0>			SECONE<3:0>				—	—	—	—	—	—	—	—
TSBDATE	31:16	YRTEN<3:0>				YRONE<3:0>				—	—	—	MTHTEN	MTHONE<3:0>			
	15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>		

28.2.6 RTCC Register Write Lock

To prevent spurious changes to the RTCC Control or RTCC Time Value registers, the WRLOCK bit (RTCCON1<11>) must be cleared first. By default, WRLOCK is cleared on any device Reset. It is recommended that WRLOCK be set after the RTCDATE and RTCTIME registers are properly initialized, and the ON bit (RTCCON1<15>) has been set.

Any attempt to write to the ON bit, the RTCCON2 register, or the RTCDATE or RTCTIME registers, will be ignored as long as WRLOCK = 1. Alarm, power control and timestamping features may be changed regardless of the state of WRLOCK.

Clearing the WRLOCK bit requires an unlock sequence, writing two words consecutively to the SYSKEY register. A sample sequence is shown in Example 28-1. If WRLOCK is already clear, it can be set (= 1) without using the unlock sequence.

Example 28-1: Clearing the WRLOCK Bit

```
SYSKEY = 0xAA996655;          // write Key1 to SYSKEY
SYSKEY = 0x556699AA;          // write Key2 to SYSKEY

RTCCON1bits.WRLOCK = 0;       // clear the lock bit

SYSKEY = 0;                   // relock SYSKEY
```

Note:	To avoid accidental writes to the timer, it is recommended that the WRLOCK bit be kept set when not writing to the Time Value registers.

28.2.7 RTCC Control Registers

Register 28-1: RTCCON1: RTCC Control 1 Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN	CHIME	—	—	AMASK<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALMRPT<7:0>(1)							
15:8	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	—	—	WRLOCK	PWCEN(2)	PWCPOL(2)	PWCOE(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	RTCOE	OUTSEL<2:0>			—	—	TSBEN(2)	TSAEN(2)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **ALRMEN:** Alarm Enable bit
1 = Alarm is enabled
0 = Alarm is disabled

bit 30 **CHIME:** Chime Enable bit
1 = Chime is enabled; ALMRPT<7:0> bits are allowed to underflow from '00' to 'FF'
0 = Alarm is disabled; ALMRPT<7:0> bits stop once they reach '00'

bit 29-28 **Unimplemented:** Read as '0'

bit 27-24 **AMASK<3:0>:** Alarm Mask Configuration bits
11xx = Reserved, do not use
101x = Reserved, do not use
1001 = Once a year (or once every 4 years when configured for February 29th)
1000 = Once a month
0111 = Once a week
0110 = Once a day
0101 = Every hour
0100 = Every 10 minutes
0011 = Every minute
0010 = Every 10 seconds
0001 = Every second
0000 = Every half second

bit 23-16 **ALMRPT<7:0>:** Alarm Repeat Counter Value bits(1)
11111111 = Alarm will repeat 255 more times
11111110 = Alarm will repeat 254 more times
• • •
00000010 = Alarm will repeat 2 more times
00000001 = Alarm will repeat 1 more time
00000000 = Alarm will not repeat

bit 15 **ON:** RTCC Enable bit
1 = RTCC is enabled and counts from selected clock source
0 = RTCC module is disabled

bit 14-12 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

2: These features are not available on all devices; refer to the specific device data sheet for more information.

Register 28-1: RTCCON1: RTCC Control 1 Register (Continued)

bit 11 **WRLOCK:** RTCC Registers Write Lock Bit
1 = Registers associated with accurate timekeeping are locked
0 = Registers associated with accurate timekeeping may be written to by user

bit 10 **PWCEN:** Power Control Enable bit(2)
1 = Power control is enabled
0 = Power control is disabled

bit 9 **PWCPOL:** Power Control Polarity bit(2)
1 = Power control output is active-high
0 = Power control output is active-low

bit 8 **PWCOE:** Power Control Output Enable bit(2)
1 = Power control output pin is enabled
0 = Power control output pin is disabled

bit 7 **RTCOE:** RTCC Output Enable bit
1 = RTCC clock output is enabled; signal selected by OUTSEL<2:0> is presented on the RTCC pin
0 = RTCC clock output is disabled

bit 6-4 **OUTSEL<2:0>:** RTCC Signal Output Selection bits
11x = Unused
101 = Timestamp B event(2)
100 = Timestamp A event(2)
011 = Power control output (PWRGT function on RTCC pin)(2)
010 = RTCC input clock source
001 = Seconds clock
000 = Alarm event

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TSBEN:** Timestamp Source B Enable bit(2)
1 = Timestamp Source B signal generates a timestamp event
0 = Timestamp Source B signal is disabled

bit 0 **TSAEN:** Timestamp Source A Enable bit(2)
1 = Timestamp Source A signal generates a timestamp event
0 = Timestamp Source A signal is disabled

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

2: These features are not available on all devices; refer to the specific device data sheet for more information.

Register 28-2: RTCCON2: RTCC Control 2 Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	DIV<15:8>							
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	DIV<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	FDIV<4:0>					—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	PWCPS<1:0>(1)		PS<1:0>(1)		—	—	CLKSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **DIV<15:0>:** Clock Divide bits
Sets the period of the clock divider counter; value should cause a nominal 1/2 second underflow.

bit 15-11 **FDIV<4:0>:** Fractional Clock Divide bits
11111 = Clock period increases by 31 RTCC input clock cycles every 16 seconds
11101 = Clock period increases by 30 RTCC input clock cycles every 16 seconds
• • •
00010 = Clock period increases by 2 RTCC input clock cycles every 16 seconds
00001 = Clock period increases by 1 RTCC input clock cycle every 16 seconds
00000 = No fractional clock division

bit 10-8 **Unimplemented:** Read as '0'

bit 7-6 **PWCPS<1:0>:** Power Control Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:16
00 = 1:1

bit 5-4 **PS<1:0>:** Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:16
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CLKSEL<1:0>:** Clock Select bits
11 = Peripheral clock (FCY)
10 = PWRLCLK input pin
01 = LPRC
00 = SOSC

Note 1: These features are not available on all devices; refer to the specific device data sheet for more information.

Register 28-3: RTCCON3: RTCC Control 3 Register(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWCSAMP<7:0>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWCSTAB<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **PWCSAMP<7:0>:** Power Control Sample Time Window bits(1)

11111111 = Sample input is always allowed (not gated)
11111110 = Sample Time window is 254 TPWC
• • •
00000010 = Sample Time window is 2 TPWC
00000001 = Sample Time window is 1 TPWC
00000000 = Sample input is always gated

bit 7-0 **PWCSTAB<7:0>:** Power Control Stability Time bits(1)

11111111 = Stability Time window is 255 TPWC
11111110 = Stability Time window is 254 TPWC
• • •
00000010 = Stability Time window is 2 TPWC
00000001 = Stability Time window is 1 TPWC
00000000 = No Stability Time window

Note 1: These features are not available on all devices; refer to the specific device data sheet for more information.

Register 28-4: RTCSTAT: RTCC Status Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HSC	U-0	R/C-0, HSC	R/W-0, HSC	R/W-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
	CPLCK(2)	—	ALMEVT	TSBEVT(1,2)	TSAEVT(1,2)	SYNC	ALMSYNC	HALFSEC

Legend:	C = Clearable Only bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **CPLCK:** Calibration PLL Lock Status bit(2)
- 1 = External calibration PLL is locked; 1 second clock output is valid
- 0 = External calibration PLL is not locked

bit 6 **Unimplemented:** Read as '0'

bit 5 **ALMEVT:** Alarm Event bit
- 1 = An alarm event has occurred
- 0 = An alarm event has not occurred

bit 4 **TSBEVT:** Timestamp B Event bit(1,2)
- 1 = A Timestamp B event has occurred
- 0 = A Timestamp B event has not occurred

bit 3 **TSAEVT:** Timestamp A Event bit(1,2)
- 1 = A Timestamp A event has occurred
- 0 = A Timestamp A event has not occurred

bit 2 **SYNC:** Synchronization Status bit
- 1 = Time registers may change during software read
- 0 = Time registers may be read safely

bit 1 **ALMSYNC:** Alarm Synchronization Status bit
- 1 = Alarm registers (ALMTIME and ALMDATE) and RTCCON1 should not be modified; ALRMEN and ALMRPT<7:0> bits may change during software read
- 0 = Alarm registers and RTCCON1 may be modified safely

bit 0 **HALFSEC:** Half Second Status bit
- 1 = Second half of 1 second period
- 0 = First half of 1 second period

Note 1: Software may write a '1' to this bit to initiate a timestamp event; the event capture is not valid until the bit reads as '1'.

2: These features are not available on all devices; refer to the specific device data sheet for more information.

Register 28-5: RTCTIME: RTCC Time Value Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	HRTEN<1:0>		HRONE<3:0>			
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	MINTEN<2:0>			MINONE<3:0>			
15:8	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	SECTEN<2:0>			SECONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **HRTEN<1:0>:** Binary Coded Decimal Value of Hours bits (10-digit)
Contains a value from 0 to 2.

bit 27-24 **HRONE<3:0>:** Binary Coded Decimal Value of Hours bits (1-digit)
Contains a value from 0 to 9.

bit 23 **Unimplemented:** Read as '0'

bit 22-20 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes bits (10-digit)
Contains a value from 0 to 5.

bit 19-16 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes bits (1-digit)
Contains a value from 0 to 9.

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SECTEN<2:0>:** Binary Coded Decimal Value of seconds bits (10-digit)
Contains a value from 0 to 5.

bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of seconds bits (1-digit)
Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as '0'

Register 28-6: RTCDATE: RTCC Date Value Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	YRTEN<3:0>				YRONE<3:0>			
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	MTHTEN	MTHONE<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DAYTEN<1:0>		DAYONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WDAY<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **YRTEN<3:0>:** Binary Coded Decimal Value of Years bits (10-digit)
Contains a value from 0 to 9.

bit 27-24 **YRONE<3:0>:** Binary Coded Decimal Value of Years bits (1-digit)
Contains a value from 0 to 9.

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **MTHTEN:** Binary Coded Decimal Value of Months bit (10-digit)
Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months bits (1-digit)
Contains a value from 0 to 9.

bit 22-20 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes bits (10-digit)
Contains a value from 0 to 5.

bit 19-16 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes bits (1-digit)
Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days bits (10-digit)
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days bits (1-digit)
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays bits (1-digit)
Contains a value from 0 to 6.

Register 28-7: ALMTIME: RTCC Alarm Time Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	HRTEN<1:0>		HRONE<3:0>			
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	MINTEN<2:0>			MINONE<3:0>			
15:8	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	SECTEN<2:0>			SECONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **HRTEN<1:0>:** Binary Coded Decimal Value of Hours bits (10-digit)
Contains a value from 0 to 2.

bit 27-24 **HRONE<3:0>:** Binary Coded Decimal Value of Hours bits (1-digit)
Contains a value from 0 to 9.

bit 23 **Unimplemented:** Read as '0'

bit 22-20 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes bits (10-digit)
Contains a value from 0 to 5.

bit 19-16 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes bits (1-digit)
Contains a value from 0 to 9.

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SECTEN<2:0>:** Binary Coded Decimal Value of Seconds bits (10-digit)
Contains a value from 0 to 5.

bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of Seconds bits (1-digit)
Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as '0'

Register 28-8: ALMDATE: RTCC Alarm Date Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	MTHTEN	MTHONE<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DAYTEN<1:0>		DAYONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WDAY<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **MTHTEN:** Binary Coded Decimal Value of Months bit (10-digit)
Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months bits (1-digit)
Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days bits (10-digit)
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days bits (1-digit)
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays bits (1-digit)
Contains a value from 0 to 6.

Register 28-9: TSxTIME: RTCC Timestamp x Alarm Time Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	HRTEN<1:0>		HRONE<3:0>			
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	MINTEN<2:0>			MINONE<3:0>			
15:8	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	SECTEN<2:0>			SECONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **HRTEN<1:0>:** Binary Coded Decimal Value of Hours bits (10-digit)
Contains a value from 0 to 2.

bit 27-24 **HRONE<3:0>:** Binary Coded Decimal Value of Hours bits (1-digit)
Contains a value from 0 to 9.

bit 23 **Unimplemented:** Read as '0'

bit 22-20 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes bits (10-digit)
Contains a value from 0 to 5.

bit 19-16 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes bits (1-digit)
Contains a value from 0 to 9.

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SECTEN<2:0>:** Binary Coded Decimal Value of Seconds bits (10-digit)
Contains a value from 0 to 5.

bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of Seconds bits (1-digit)
Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as '0'

Register 28-10: TSxDATE: RTCC Timestamp x Alarm Date Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	YRTEN<3:0>				YRONE<3:0>			
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	MTHTEN	MTHONE<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DAYTEN<1:0>		DAYONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WDAY<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **YRTEN<3:0>:** Binary Coded Decimal Value of Years bits (10-digit)
Contains a value from 0 to 9.

bit 27-24 **YRONE<3:0>:** Binary Coded Decimal Value of Years bits (1-digit)
Contains a value from 0 to 9.

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **MTHTEN:** Binary Coded Decimal Value of Months bit (10-digit)
Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months bits (1-digit)
Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days bits (10-digit)
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days bits (1-digit)
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

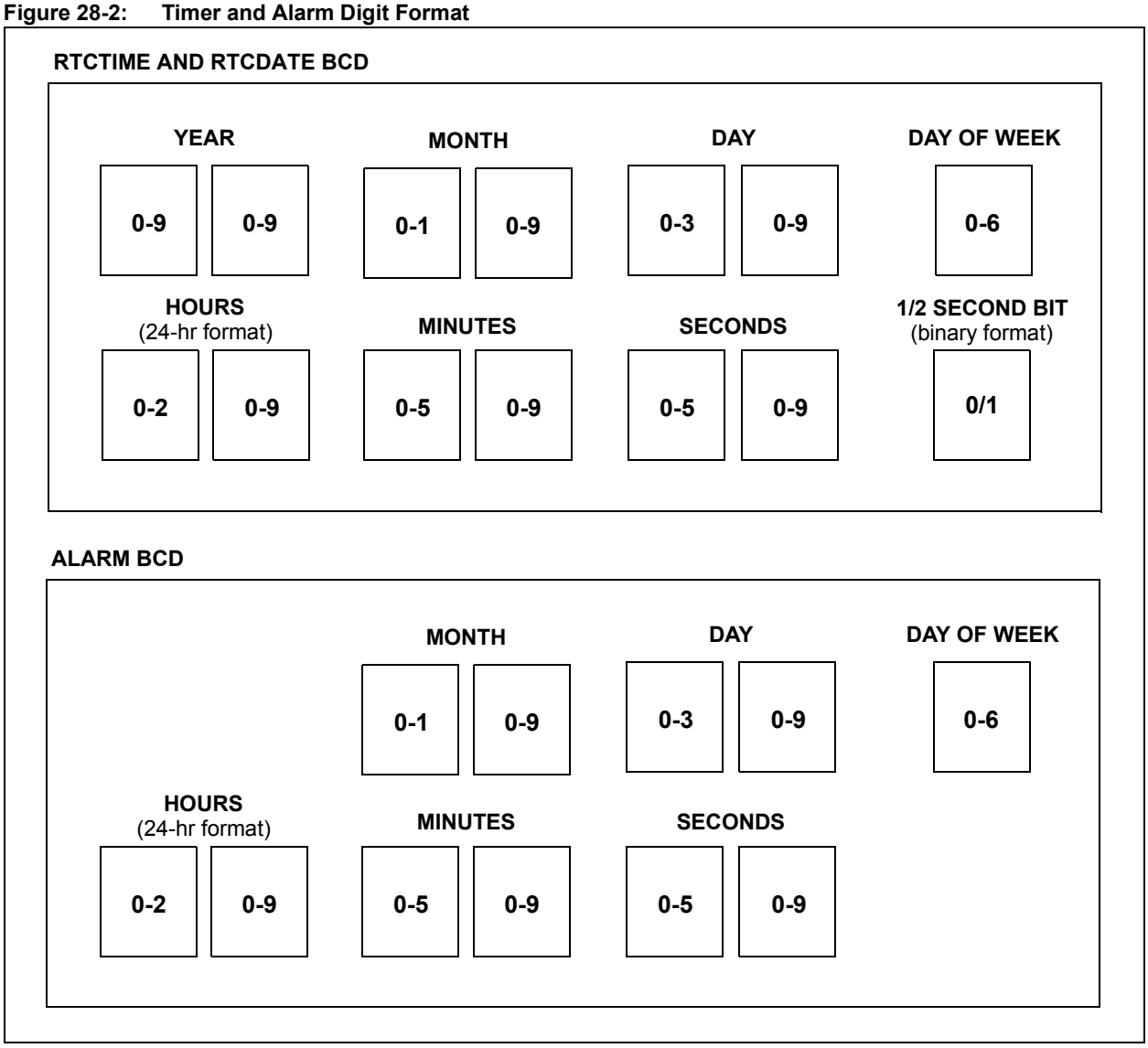
bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays bits (1-digit)
Contains a value from 0 to 6.

28.3 OPERATION

28.3.1 Register Interface

The register interface for the RTCC and alarm values is implemented using natural Binary Coded Decimal (BCD) format. This simplifies the firmware, when using the module, as each of the digit values is contained within its own 4-bit value (see Figure 28-2).

Figure 28-2: Timer and Alarm Digit Format



28.3.2 General Functionality

All Timer registers containing a time value of seconds or greater are writable. The user can configure the time by writing the desired year, month and day to the RTCDATE register; and the hour, minutes and seconds to the RTCTIME register. The timer will then use the newly written values and proceed with the count from the desired starting point. The RTCC module is enabled by setting the ON bit (RTCCON1<15>). If enabled while adjusting these registers, the timer will still continue to increment.

The user has visibility to the half second field of the counter, HALFSEC (RTCSTAT<0>). This value is read-only and can only be reset by writing to SECONE<3:0> (RTCTIME<11:8>).

28.3.3 Synchronization

Because the CPU and the RTCC operate in different clock domains, care must be taken when reading and writing the RTCC registers. The user is responsible to assure that when ON = 1, the updated registers will not be incremented at the same time. This can be accomplished in several ways:

- Checking the status of the SYNC bit (RTCSTAT<2>) before reading or writing to the RTCTIME or RTCDATE registers. Refer to Example 28-2 for example code; or
- Checking the status of the ALMSYNC bit before reading or writing to the RTCTIME or RTCDATE registers, or the AMASK<3:0> bits (RTCCON1<27:24>); or
- Checking the preceding digits from which a carry can occur; or
- Updating the registers immediately following the seconds pulse (or alarm interrupt).

The SYNC bit indicates a time window during which the RTCC Clock Domain registers can be safely read and written without concern about a rollover. When SYNC = 0, the registers can be safely accessed by the CPU. Whether SYNC = 1 or 0, the user should employ a firmware solution to assure that the data read did not fall on a rollover boundary, resulting in an invalid or partial read. This firmware solution would consist of reading each register twice and then, comparing the two values. If the two values match, then a rollover did not occur.

Example 28-2: Function to Perform a Safe Read of the RTCTIME Register

```
unsigned   int     ReadTime(void)
{
    unsigned   int     timeCopy1, timeCopy2;

    if (RTCSTATbits.SYNC == 0)
    {
            return (RTCTIME);      // return time
    }
    else
    {
            // read time twice and compare result, retry until a match occurs
            while ( (timeCopy1 = RTCTIME) != (timeCopy2 = RTCTIME) );

            return (timeCopy1);    // return time when both reads matched
    }
}
```

28.3.4 Digit Carry Rules

Certain timer values are affected when there is a rollover:

- Time of Day: From 23:59:59 to 00:00:00 with a carry to the day field
- Day of Week: From 6 to 0 with no carry (refer to Table 28-2 for values)
- Day (DAYONEx and DAYTENx fields together): From 28, 29, 30 or 31, with a carry to the month field (refer to Table 28-3 for the schedule)
- Month (MTHONEx and MTHTEN fields together): From 12/31 to 01/01, with a carry to the year field
- Year Carry: From 99 to 00; this also surpasses the use of the RTCC

Table 28-2: Day of Week Schedule

Day of Week	WDAY<2:0> Value
Sunday	0
Monday	1
Tuesday	2
Wednesday	3
Thursday	4
Friday	5
Saturday	6

Table 28-3: Day to Month Rollover Schedule

Month	Maximum Day Field	Month	Maximum Day Field
01 (January)	31	07 (July)	31
02 (February)	28 or 29(1)	08 (August)	31
03 (March)	31	09 (September)	30
04 (April)	30	10 (October)	31
05 (May)	31	11 (November)	30
06 (June)	30	12 (December)	31

Note 1: See **Section 28.3.4.1 "Leap Year"** for details.

As the module uses BCD format, the carry to the upper BCD digit occurs at a count of 10, and not a count of 16, for these fields:

- SEC
- MIN
- HR
- WDAY
- DAY
- MON

28.3.4.1 LEAP YEAR

Since the year range on the RTCC module is 2000 to 2099, the leap year calculation is determined by any year, divisible by 4, in the above range. The only month to be affected in a leap year is February. The month of February will have 29 days in a leap year, while any other year, it will have 28 days.

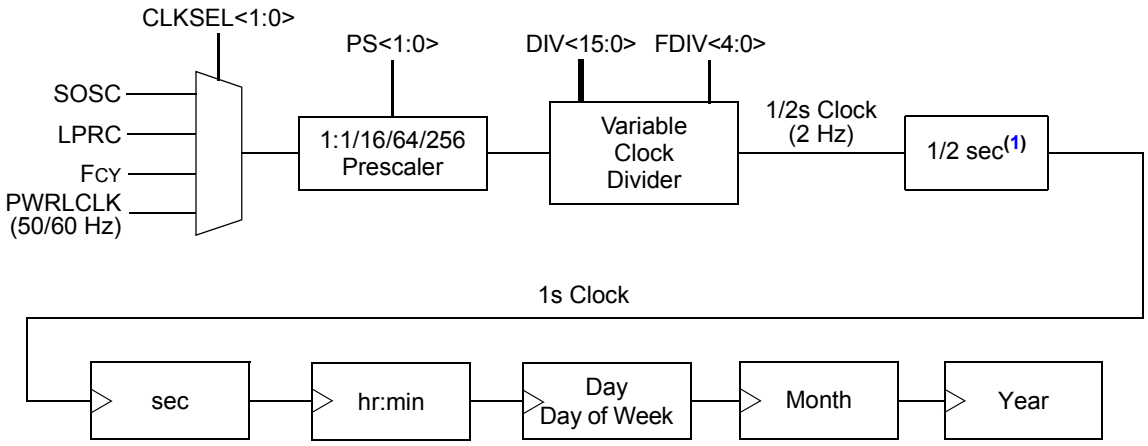
28.3.5 Clock Source

The RTCC clock source is selected with the CLKSEL<1:0> bits (RTCCON2<1:0>). It is designed to operate from any one of four clock sources:

- The crystal-controlled 32.768 kHz Secondary Oscillator (SOSC)
- The internal Low-Power RC 31 kHz Oscillator (LPRC)
- The microcontroller peripheral clock, operating at the instruction frequency (FCY)
- The PWRLCLK pin input, generally derived from the local mains frequency (50/60 Hz)

Each option provides users with choices of application component count and accuracy over time. The Secondary Oscillator (SOSC) provides the highest accuracy and lowest power consumption option. When used as the source, calibration of the crystal can be accomplished through this module, yielding an error of 3 seconds or less per month. See **Section 28.3.6 "Clock Calibration"** for further details.

Figure 28-3: Clock Source Multiplexing and Divider Chain



Note 1: Writing to the RTCTIME register resets all counters, allowing fraction of a second synchronization. Clock prescalers are held in Reset when ON = 0.

28.3.5.1 CLOCK DIVIDER

The RTCC timer must be provided with a 1/2 second (2 Hz) clock source. This is done by selecting appropriate values for the clock prescaler and the variable clock divider.

The clock prescaler divides the input clock by one of four fixed ratios. It is controlled by the PS<1:0> bits (RTCCON2<5:4>). Divider options are 1:1, 1:16, 1:64 and 1:256.

The variable coarse clock divider further divides the clock input from the prescaler. It provides the entire range of integer divisor options, from 1:1 to 1:32,768. It is controlled by the DIV<15:0> bits field (RTCCON2<31:16>).

The clock divider also has a fine divider, controlled by the FDIV<4:0> bits. This permits fine frequency adjustments to the timer output. This is discussed in **Section 28.3.6 "Clock Calibration"**.

Selection of a particular clock input with the CLKSELx bits does not automatically select an appropriate prescaler or clock divider option. It is the user's responsibility to configure the prescaler and divider correctly to provide a 2 Hz signal to the timer. Table 28-4 lists the most common combinations for typical clock sources. Equation 28-1 shows how to calculate the prescaler and DIVx values for any input frequency.

Table 28-4: Clock Divider vs. Input Frequency (Nominal Clock Frequencies)

Input Frequency	Prescaler	DIV<15:0>	FDIV<4:0>
32,768 kHz	1:1	3FFF	00000
60 Hz	1:1	1D	00000
50 Hz	1:1	18	00000
16 MHz	1:256	7A11	00000

Equation 28-1: RTCC Clock Frequency Divider Output Frequency

$$FOUT = \frac{1}{2} \bullet \left[\frac{FIN}{Prescale \bullet (DIV\langle 15:0\rangle + 1) + \frac{FDIV\langle 4:0\rangle}{32}} \right]$$

Where:

$$DIV\langle 15:0\rangle = \frac{FIN}{2 \bullet Prescale} - 1$$

and $FDIV\langle 4:0\rangle$ is the fractional remainder of $DIV\langle 15:0\rangle$, multiplied by 32

28.3.5.2 SECONDARY OSCILLATOR (SOSC) ENABLE

If the RTCC is configured to use the Secondary Oscillator, it will automatically be enabled when the RTCC is enabled. The SOSCEN bit (OSCCON<1>) does not need to be set. For more information on the Secondary Oscillator, refer to the **"Oscillator Configuration"** chapter of the device data sheet.

28.3.5.3 LOW-POWER RC OSCILLATOR ENABLE

If the RTCC is configured to be clocked by LPRC, the LPRC will automatically be enabled. Refer to the **"Oscillator Configuration"** chapter of the device data sheet for more information on the LPRC.

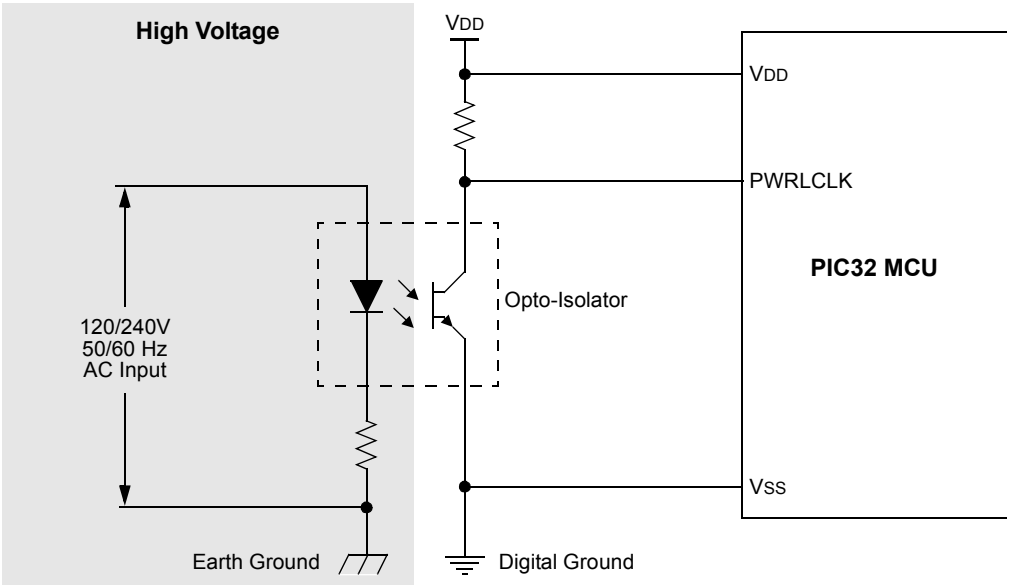
28.3.5.4 CLOCK SOURCE FROM POWER LINE (50/60 Hz SIGNAL)

It is possible to use the power mains as an external clock source for the RTCC. The module can use either 50 or 60 Hz AC to accommodate local power in most locations throughout the world.

Line voltage cannot be used directly to provide the clock reference. For safety reasons, the line voltage must be properly isolated from the digital portion of the application. Failure to properly design the circuitry that interfaces mains voltage to the microcontroller may result in a fatal shock. Figure 28-4 shows a suggested signal conditioning circuit for such a clock source.

Note:	This feature is not available on all devices; refer to the specific device data sheet for more information.

Figure 28-4: Suggested Signal Conditioning for 50/60 Hz RTCC Clock Input



28.3.6 Clock Calibration

In addition to the 16-bit coarse divider (DIV<15:0>), the variable clock divider also uses a fine clock frequency divisor to make small trim adjustments to the nominal 0.5s timer signal. This fine divider, FDIV<4:0> (RTCCON2<15:11>), acts as the fractional part of a 21-bit clock divider when used with DIV<15:0>.

The fine divider operates on the variable clock divider output every 1/2 second, optionally omitting a clock cycle. This effectively stretches the period set by the period counter by one clock cycle. When FDIV<4:0> = 01h, it takes 16 seconds to remove a clock cycle and see any effect on the output. The maximum effect is when FDIV<4:0> = 31 (decimal), which represents 31 clock cycles removed over 16 seconds. When FDIV<4:0> = 0, the clock period is not affected by the fine divider.

Deviation from the desired input frequency is adjusted by changing the values of DIVx and FDIVx accordingly, as calculated by Equation 28-1. A faster than desired oscillator generally requires increases to the value of FDIVx for small changes, or decreases to the value of DIVx for large changes. On the other hand, a slow oscillator requires decreases to the value of FDIVx, or increases to the value of DIVx. Table 28-5 shows the effect of changing DIVx and FDIVx; Example 28-3 demonstrates the calculation of FDIVx in these cases.

The fine clock divider is optimized to provide an adjustment error of less than 2 ppm when operating from a crystal-controlled 32.768 kHz oscillator. Even so, it is effective for fine-tuning the timer signal frequency, regardless of the clock input.

Note:	Before calibration, the user must determine the error of the crystal. This should be done using another timer resource on the device or an external timing reference. It is the user's responsibility to include in the error value the initial error of the crystal, drift due to temperature and drift due to crystal aging.

Table 28-5: Clock Divider vs. Input Frequency (Showing Fine-Tuning Options)

Input Frequency	Prescaler	DIV<15:0>	FDIV<4:0>
32,767.9 kHz(1)	1:1	3FFE	1E
32,768.0 kHz	1:1	3FFF	00
32.768.3 kHz(1)	1:1	3FFF	05
59.9 Hz(1)	1:1	1C	1E
60 Hz	1:1	1D	00
60.1 Hz(1)	1:1	1D	02

Note 1: These selections are provided to demonstrate settings for a clock source slightly faster or slower than the desired output frequency.

Example 28-3: Clock Divider Calculation (with FDIV<4:0>)

FIN = 32767.8 Hz (Oscillator running slow)

Prescaler = 1:1

Divide Ratio = 32767.8/2 – 1 = 16382.9

Therefore, DIV<15:0> = 16382 and FDIV<4:0> = 32(0.9) = 29

28.3.7 RTCC Pin

The RTCC pin can be configured by the OUTSEL<2:0> bits (RTCCON1<6:4>) to present any one of several outputs:

- One second clock pulse
- A direct pass-through of the RTCC input clock source
- Alarm signal (see **Section 28.4 "Alarm"** for details)
- Power control pin, in addition to or as an alternative to the PWRGT pin (see **Section 28.5 "Power Control"** for details)
- Timestamp events (see **Section 28.6 "Timestamping"** for details)

When used as an output, the RTCC Output Enable bit, RTCOE (RTCCON1<7>), must also be set.

28.4 ALARM

The RTCC alarm includes these features:

- Configurable from half second to one year
- One-time alarm and repeat alarm options available

28.4.1 Configuring the Alarm

The alarm feature is enabled by setting the ALRMEN bit (RTCCON1<31>). This bit is cleared by hardware when an alarm is issued, but is not cleared if the CHIME bit (RTCCON1<30>) = 1, or if the ALMRPT<7:0> (RTCCON1<23:16>) bits have any value other than 00h.

The interval selection of the alarm is configured through the AMASK<3:0> bits (RTCCON1<27:24>). These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur. Figure 28-5 shows the available alarm mask options.

Note: Changing any of the control bits, other than RTCOE, ALMRPT<7:0> and CHIME, while the alarm is enabled (ALRMEN = 1), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, change the timer and alarm values only while the alarm is disabled (ALRMEN = 0). It is recommended that these bits be changed when ALMSYNC = 0.

Figure 28-5: Alarm Mask Settings

Alarm Mask Setting AMASK<3:0>	Day of the Week	Month	Day	Hours	Minutes	Seconds
0000 – Every half second 0001 – Every second						
0010 – Every 10 seconds						s
0011 – Every minute						s s
0100 – Every 10 minutes					m	s s
0101 – Every hour					m m	s s
0110 – Every day				h h	m m	s s
0111 – Every week	d			h h	m m	s s
1000 – Every month			d d	h h	m m	s s
1001 – Every year(1)		m m	d d	h h	m m	s s

Note 1: Annually, except when configured for February 29.

28.4.2 Alarm Repeat and Chime

The alarm can also be configured to repeat based on a preconfigured interval. The amount of times this occurs, once the alarm is enabled, is determined by the ALMRPT<7:0> bits. The alarm can be repeated up to 255 times. When ALMRPT<7:0> = 00h and CHIME = 0, the repeat function is disabled and only a single alarm will occur.

After each alarm is issued, the ALMRPT<7:0> bits are decremented by one. Once the bit field has reached '00', the alarm will be issued one last time, after which, the ALRMEN bit is cleared automatically and the alarm is turned off.

Indefinite repetition of the alarm can occur if the CHIME bit = 1. Instead of the alarm being disabled when the ALMRPT<7:0> bits reach 00h, the value of the bit field rolls over to FFh and continues to count down indefinitely.

28.4.3 Alarm Interrupt

An interrupt is generated at every alarm event. When an event occurs, the ALMEVT bit (RTCSTAT<5>) is set. This allows the application to distinguish an alarm interrupt from other interrupt events, if necessary. The application should clear ALMEVT after an RTCC interrupt in order to distinguish additional alarm events (or other interrupts if they are enabled).

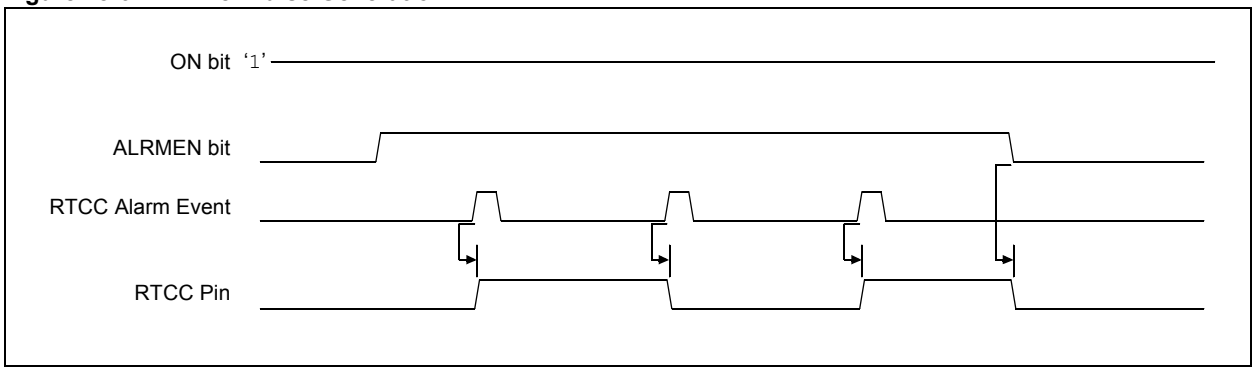
28.4.4 Alarm Output

In addition to the alarm interrupt, an alarm pulse output is provided that operates at half the frequency of the alarm. This output is completely synchronous to the RTCC clock and can be used as a trigger clock to other peripherals. This output is available on the RTCC pin. The output pulse is a clock with a 50% duty cycle and a frequency half that of the alarm event (see Figure 28-6).

The alarm output pulse is presented on the RTCC pin whenever the OUTSEL<2:0> bits (RTCCON1<6:4>) = 000. The RTCC Output Enable bit, RTCOE (RTCCON1<7>), must also be set.

Note:	When the timer value reaches that of the Alarm registers, one period of the RTCC clock will elapse before the alarm interrupt is set. As a result, the application will see the timer value at the alarm value before the interrupt has occurred.

Figure 28-6: Timer Pulse Generation



28.5 POWER CONTROL

Note: This feature is not available on all devices; refer to the specific device data sheet for more information.

The RTCC includes a power control feature that allows the device to periodically wake-up an external device, waits for the device to be stable before sampling wake-up events from that device and then shuts down the external device. This can be done completely autonomously by the RTCC without the need to wake from the current lower power mode (Sleep, Deep Sleep, etc.).

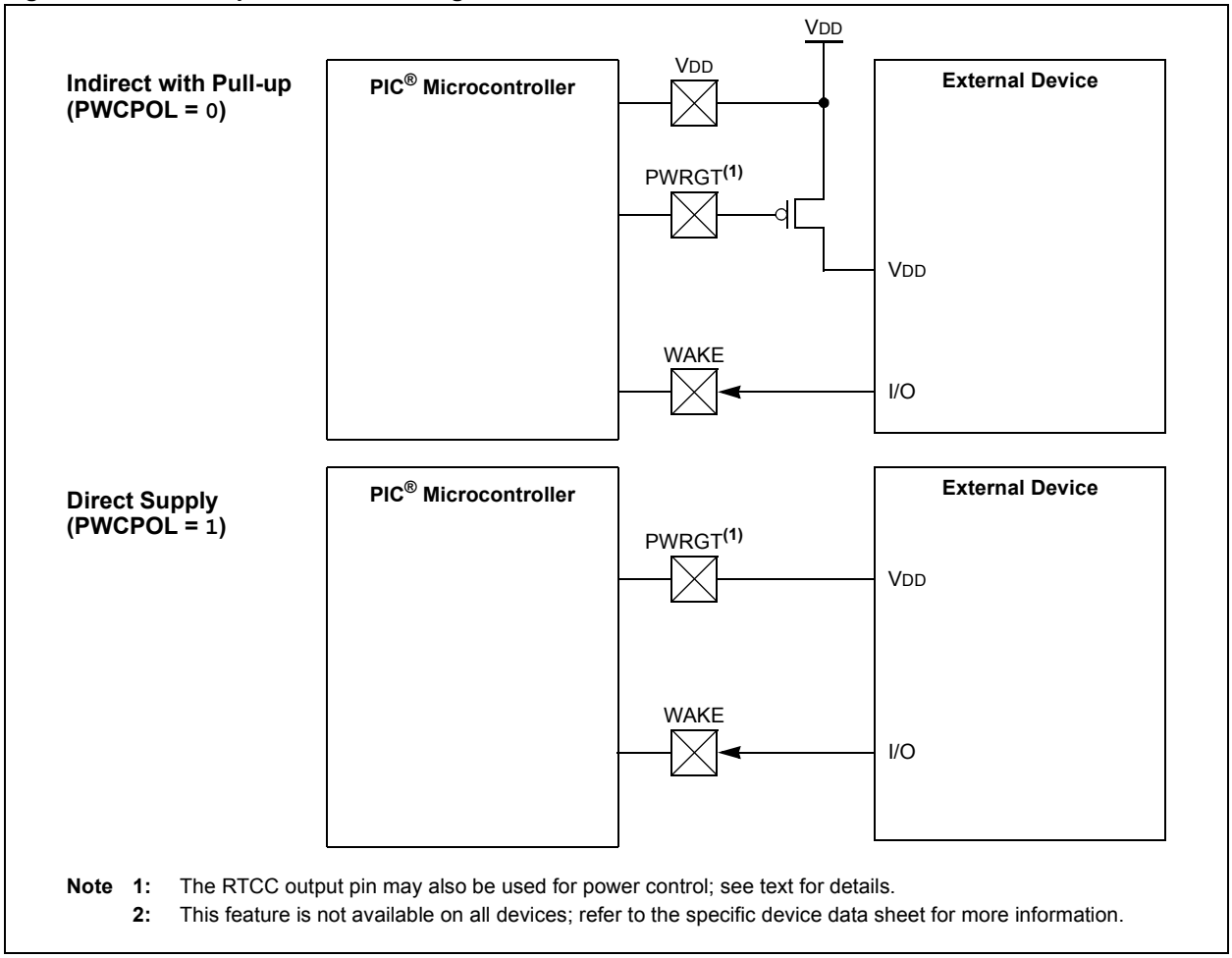
The power control feature uses the PWRGT output pin; the RTCC output pin may also be used with PWRGT or as an alternative. (Select devices may only use the RTCC pin for power control. Refer to the device data sheet for more information.) Two possible control circuits for this feature are shown in Figure 28-7. The WAKE pin in both examples represents an input that would wake-up the device in the desired circumstances (e.g., INT0 in Deep Sleep, any enabled interrupt in Sleep, etc.).

The top of the figure illustrates a situation in which the external device requires more current than the I/O pin can reliably generate. Note that the power control polarity is active-low in order to provide the external device power at the correct times.

A more straightforward approach is shown in the bottom of the figure. For external devices, whose current consumption is within the range an I/O pin can provide (approximately 20 mA), the device can be powered directly via the PWRGT or RTCC pin. If the device requires a stabilizing capacitor on V_{DD}, this method could result in a significant current load. To use this layout, the capacitor would have to be very small (0.01 µF) or allowances for a greater time to reach operating stability may be required (see **Section 28.5.2 "Power Control Operation"** for more information).

To determine the best power control configuration for any given application, refer to the data sheets for both the Microchip device and the external device.

Figure 28-7: Examples of RTCC Managed Power Control(2)



Note 1: The RTCC output pin may also be used for power control; see text for details.
2: This feature is not available on all devices; refer to the specific device data sheet for more information.

28.5.1 Initialization

To enable power control:

- The RTCC must be enabled (ON (RTCCON1<15>) = 1)
- Power control must be enabled (PWCEN (RTCCON1<10>) = 1)
- The PWRGT and/or RTCC pins must be enabled for power control:
  - For PWRGT, the pin must be enabled (PWCEN (RTCCON1<10>) = 1)
  - For RTCC, the pin must be enabled (RTCOE (RTCCON1<7> = 1) and configured for power control (RTCCON1<6:4> = 011)

In addition, set the CHIME bit (RTCCON1<30>) to enable the Power Control (PWC) periodicity.

The polarity of the PWC control signal on both pins is selected using the PWCPOL bit (RTCCON1<9>). Active-low or active-high may be used with the appropriate external switch to turn on or off the power to one or more external devices. The active-low setting may also be used in conjunction with an open-drain setting on the PWRGT or RTCC pins, in order to drive the GND or VSS pin(s) of the external device directly (with the appropriate external VDD pull-up device), without the need for external switches.

28.5.2 Power Control Operation

When the RTCC and PWC are enabled and running, the PWC logic generates a control output and a sample gate output. The control output is driven out on either the PRWGT pin or the RTCC pin, and is used to power up or down the external device.

Once the control output is asserted, the Stability window begins. During this interval, the external device is given enough time to power-up and provide a stable output. When the output is (theoretically) stable, the Sample window begins. In this interval, the RTCC monitors for the wake-up signal from the external device. Typically, a sample gate is used to mask out one or more wake-up signals from the external device.

Finally, both the Stability and Sample windows close after the expiration of the Sample window, and the external device is powered down.

28.5.2.1 STABILITY AND SAMPLE WINDOWS

The Stability and Sample windows are defined in terms of the RTCC clock source, the PWC prescaler, and the PWCSAMPx and PWCSTABx bits field in the RTCCON3 register (RTCCON3<15:8> and <7:0>, respectively).

The clock source selected for the RTCC is also used for the PWC clock source. A dedicated prescaler, controlled by the PWCPS<1:0> bits (RTCCON2<7:6>), divides the RTCC clock input. Divider options of 1:1, 1:16, 1:64 or 1:256 are available. The clock and prescaler selections determine the base value of the PWC clock period. The 8-bit magnitude of PWCSTABx and PWCSAMPx allows for a Stability/Sample window size of 0 to 255 clock periods. Table 28-6 shows the size of the windows for common RTCC clock and prescaler options.

Certain values for PWCSTABx and PWCSAMPx have specific control meanings in determining power control operations. If either field is 00h, the corresponding window is inactive. In addition, if the PWCSTABx field is FFh, the Stability window remains active continuously, even if power control is disabled.

Table 28-6: Stability and Sample Windows for Common Clock Sources

Clock Source	PWCPS<1:0>	PWCSTAB<7:0> Range	PWCSAMP<7:0> Range
SOSC (32.768 kHz)	11 (1:256)	0 ms-2s	0 ms-2s
LPRC (31 kHz)	11 (1:256)	0 ms-2.1s	0 ms-2.1s
Power Line (50 Hz)	00 (1:1)	0 ms-5.12s	0 ms-5.12s
Power Line (60 Hz)		0 ms-4.25s	0 ms-4.25s

28.5.2.2 MODES OF OPERATION

28.5.2.2.1 Normal Operation (Stability and Sample Windows Active)

When PWCSTABx is not 0 and PWCSAMPx is any value except 0 or 255, the PWC is configured for the normal mode of operation. In this mode, the external wake-up interrupt should be connected to the external device, controlled by the PWC power enable. Figure 28-8 shows operation with inverted (active-low) operation; Figure 28-9 shows normal (active-high) operation.

Figure 28-8: Power Control Timer (Normal Operation, PWCPOL = 0)

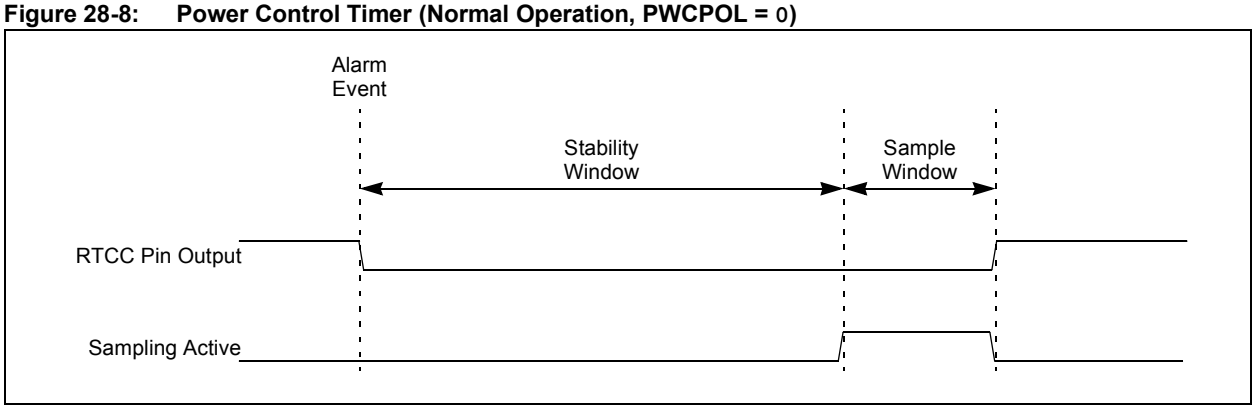
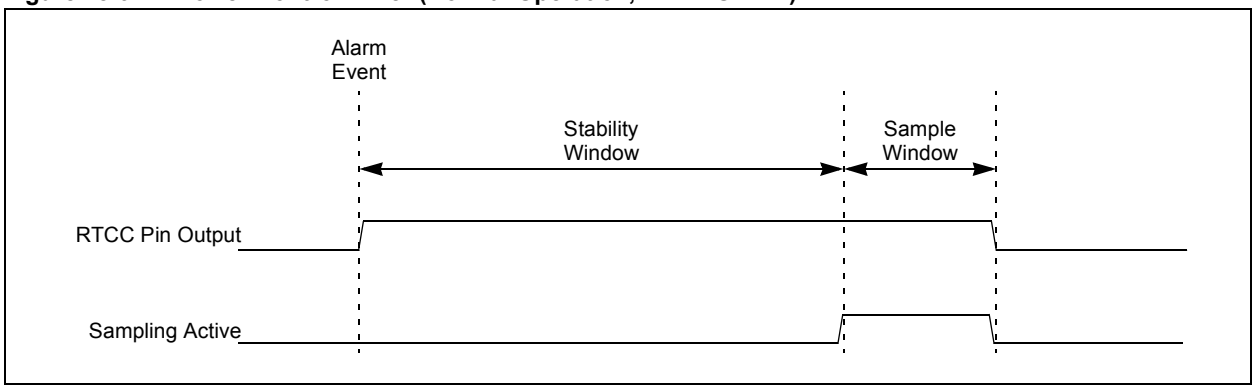


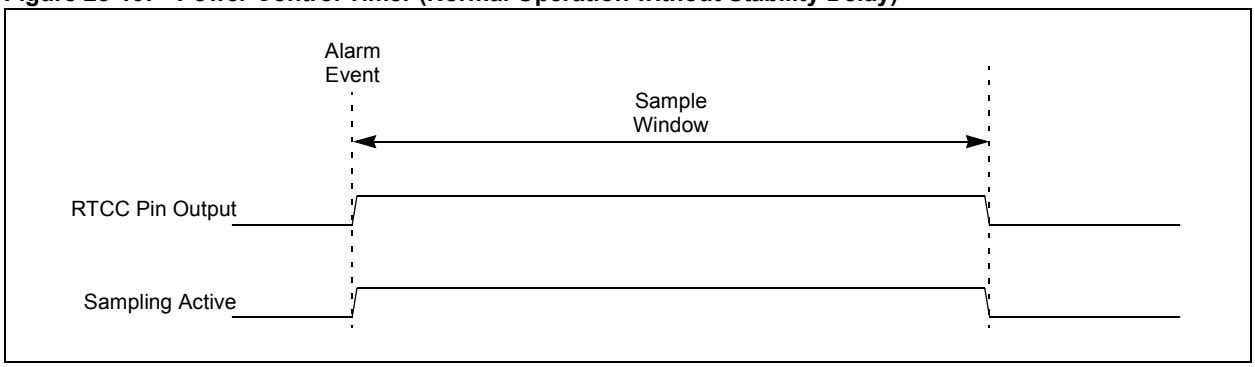
Figure 28-9: Power Control Timer (Normal Operation, PWCPOL = 1)



28.5.2.2.2 Normal Operation without Stability Delay (Stability Window Inactive)

When PWCSTABx is 0 and PWCSAMPx is any value except 0 or 255, the PWC is configured for the normal mode of operation with no stability time, as shown in Figure 28-10. This mode is recommended when the external device, controlled by the PWC power enable, requires no time between when power is applied and when its wake-up or interrupt output is valid. Although a valid option, this case is considered to be unlikely.

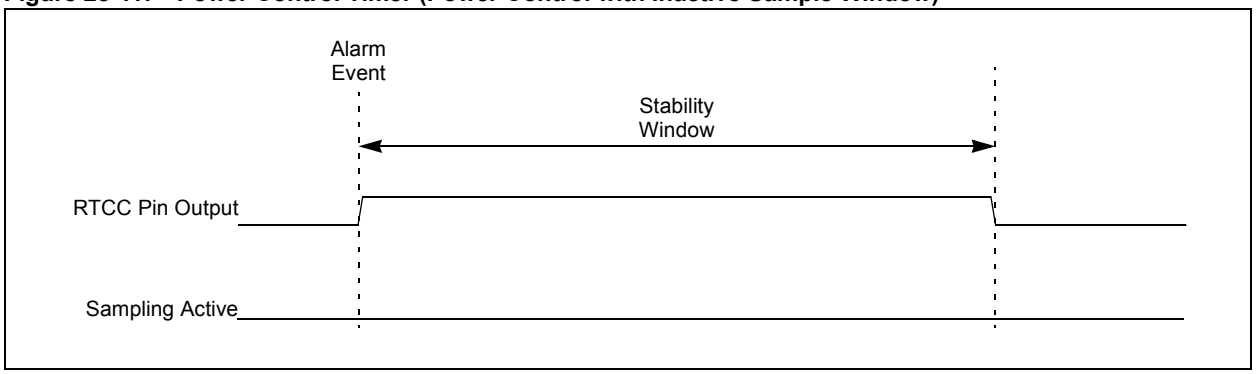
Figure 28-10: Power Control Timer (Normal Operation without Stability Delay)



28.5.2.2.3 Power Control without Sampling (Sample Window Inactive)

When PWCSTABx is any value but 0 and PWCSAMPx is 0, the PWC is configured for power control only. No wake-up or interrupt sampling occurs, as shown in Figure 28-11. This mode is generally not used.

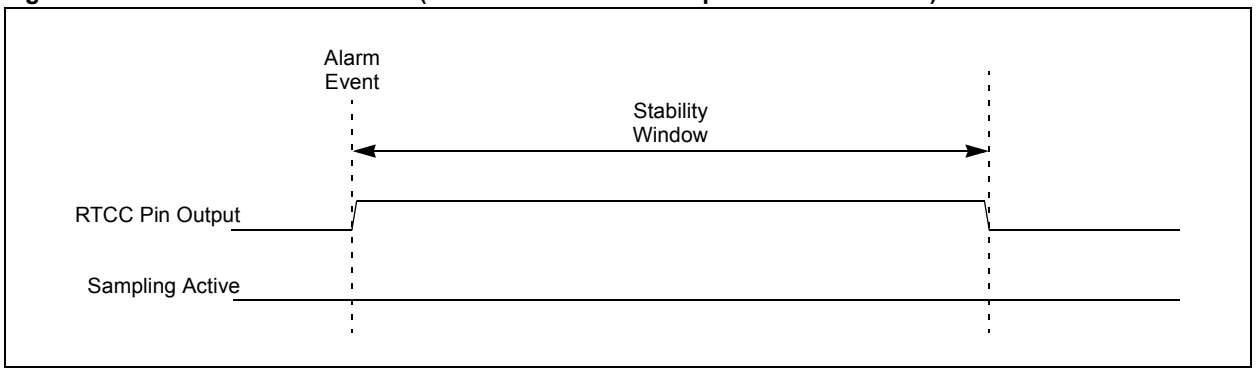
Figure 28-11: Power Control Timer (Power Control with Inactive Sample Window)



28.5.2.2.4 Power Control without Sampling (Sample Window Unused)

When PWCSTABx is any value but 0 and PWCSAMPx is 255, the PWC is configured for power control only. The Sample window, although always active, is not used. This is shown in Figure 28-12. This mode should be used when the external device, controlled by the PWC power enable, does not drive a wake-up or interrupt input directly. In this case, the sampling of external interrupts is disabled and the external interrupt may be driven by any source.

Figure 28-12: Power Control Timer (Power Control with Sample Window Unused)



28.5.2.2.5 PWC Disabled

When PWCEN is cleared (RTCPWC<15> = 0), the PWCSTABx and PWCSAMPx fields have no effect. In this case, the sampling of external interrupts is disabled; the external interrupt may be driven by any source.

28.6 TIMESTAMPING

Note: This feature is not available on all devices; refer to the specific device data sheet for more information.

The RTCC provides up to two sets of Timestamp registers that are used to capture the RTCTIME and RTCDATE register values when an external input signal is received. The RTCC has a timestamp event input assigned to each of set of Timestamp registers, Timestamp A and Timestamp B (TSATIME/TSBTIME, TSADATE/TSBDATE registers). Timestamp event sources are device dependent; please see the device data sheet for further details.

Because the Timestamp registers are all essentially “blank” 32-bit registers (i.e., all bits are implemented and do not have special Reset conditions), these registers may also be used as backup RAM during Deep Sleep and VBAT modes if the RTCC is configured for VBAT operation.

28.6.1 Operation

Each event input is enabled for timestamping using the TSBEN and TSAEN bits (RTCCON1<1:0>). If a bit is clear, the event input for the corresponding set of Timestamp registers is disabled. User software may then use the TSxTIME and TSxDATE register pairs for data storage.

When TSxEN = 1, the timestamp source is enabled. When a timestamp event is detected, the present time and date values are stored in the respective TSxTIME and TSxDATE registers. The TSxEVT status bit becomes set and an RTCC interrupt occurs. The TSxTIME and TSxDATE registers become read-only when TSxEN = 1. A new timestamp capture event cannot occur until the TSxEVT bit is cleared in software. The edge sensitivity of the timestamp event depends on the source; see the device data sheet for more information.

The data stored in the TSxTIME and TSxDATE registers is maintained throughout all Resets, except for POR and BOR.

28.6.2 Manual Timestamping

The present time and date can be captured in software by writing a ‘1’ to the TSxEVT bit. This does not immediately set the TSxEVT bit, but initiates a timestamp capture. When the capture is completed, the TSxEVT bit becomes set. The application must poll the TSxEVT bit to determine when the capture has completed.

After the Timestamp registers have been read, clear the TSxEVT bit to allow further hardware or software timestamp capture events.

28.7 INTERRUPTS

The RTCC generates a single, top-level interrupt flag, RTCCIF. This interrupt can be triggered by either a timestamp event (TSA or TSB) or by an RTCC alarm event. Setting the RTCCIE bit allows a device-level interrupt to be generated.

If the source of the interrupt is required, the application may poll the appropriate bit in the RTCSTAT register (TSAEVT, TSBEVT or ALMEVT, respectively) to see which event has occurred.

28.8 RESETS

28.8.1 Device Reset

When a device Reset, other than POR or BOR occurs, the RTCC will continue to operate if it was already enabled.

28.8.2 Power-on Reset (POR)

The RTCCONx registers, and the RTCTIME and RTCDATE registers are reset on a POR or BOR. Once the device exits the POR state, the time is reset to 12 midnight (00:00:00) on Saturday, January 1st, 2000; the correct time and date will need to be written to these registers.

The timer prescaler can only be reset by writing to the RTCTIME register. No device Reset can affect the prescalers.

28.9 OPERATION IN POWER-SAVING MODES

28.9.1 Idle Mode

Idle mode does not affect the operation of the timer or alarm.

28.9.2 Sleep Modes

The timer and alarm continue to operate while in Sleep mode, including Deep Sleep mode. The operation of the alarm is not affected by Sleep, as an alarm event can always wake-up the CPU.

28.9.3 VBAT Mode

In devices that include VBAT power-saving features, the RTCC is capable of continued operation during this mode. While the alarm still functions, it will not wake the device.

The RTCBAT Configuration bit controls this feature. By default (RTCBAT = 1), continued RTCC operation in VBAT mode is enabled.

While in VBAT mode, the RTCC clock source, selected by the CLKSEL<1:0> bits, remains active. Users should remember to include the incremental current consumption required for the clock source when calculating a power budget for VBAT operation.

Note:	VBAT features are not available on all devices; refer to the specific device data sheet for more information.

28.10 PERIPHERAL MODULE DISABLE (PMD) REGISTER

The Peripheral Module Disable (PMD) registers provide a method to disable the RTCC module by stopping all clock sources supplied to that module. When a peripheral is disabled via the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral will also be disabled, so writes to those registers will have no effect and read values will be invalid. The RTCC will only be enabled if the RTCCMD bit in the PMDx register is cleared.

28.11 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32 device families, but the concepts are pertinent and could be used with modification and possible limitations.

The current application notes related to the RTCC with Timestamp module are:

Title	Application Note #
No related application notes at this time.	

28.12 REVISION HISTORY

Revision A (August 2015)

This is the initial revision of this document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

ISBN: 978-1-63277-650-1

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

07/14/15