

Specification

Version: V1.10 Document No.: ILI9341_DS_V1.10.pdf

ILI TECHNOLOGY CORP.

8F, No. 38, Taiyuan St., Jhubei City, Hsinchu Country 302 Taiwan R.O.C. Tel.886-3-5600099; Fax.886-3-5670585 http://www.ilitek.com



Table of Contents

Sec	ction			Page
1.	Introd	uction		7
2.	Featu	res		7
3.	Block	Diagram	1	9
4.	Pin De	escriptio	ns	10
5.	Pad A	rrangem	ent and Coordination	15
6.	Block	Function	n Description	24
7.	Functi	ion Desc	ription	26
	7.1.	MCU	nterfaces	26
		7.1.1.	MCU interface selection	26
		7.1.2.	8080- I Series Parallel Interface	27
		7.1.3.	Write Cycle Sequence	28
		7.1.4.	Read Cycle Sequence	29
		7.1.5.	8080-	30
		7.1.6.	Write Cycle Sequence	31
		7.1.7.	Read Cycle Sequence	32
		7.1.8.	Serial Interface	33
		7.1.9.	Write Cycle Sequence	33
		7.1.10.	Read Cycle Sequence	36
		7.1.11.	Data Transfer Break and Recovery	40
		7.1.12.	Data Transfer Pause	42
		7.1.13.	Serial Interface Pause (3_wire)	43
		7.1.14.	Parallel Interface Pause	43
		7.1.15.	Data Transfer Mode	44
		7.1.16.	Data Transfer Method 1	44
		7.1.17.	Data Transfer Method 2	44
	7.2.	RGB I	nterface	45
		7.2.1.	RGB Interface Selection	45
		7.2.2.	RGB Interface Timing	49
	7.3.	VSYN	C Interface	52
	7.4.	Color	Depth Conversion Look Up Table	55
	7.5.	Displa	y Data RAM (DDRAM)	59
	7.6.	Displa	y Data Format	60
		7.6.1.	3-line Serial Interface	60
		7.6.2.	4-line Serial Interface	63
		7.6.3.	8-bit Parallel MCU Interface	65
		7.6.4.	9-bit Parallel MCU Interface	67
		7.6.5.	16-bit Parallel MCU Interface	70





		7.6.6.	18-bit Parallel MCU Interface	76
		7.6.7.	6-bit Parallel RGB Interface	80
		7.6.8.	16-bit Parallel RGB Interface	82
		7.6.9.	18-bit Parallel RGB Interface	82
8.	Comm	nand		83
	8.1.	Comn	nand List	83
	8.2.	Descr	iption of Level 1 Command	89
		8.2.1.	NOP (00h)	89
		8.2.2.	Software Reset (01h)	90
		8.2.3.	Read display identification information (04h)	91
		8.2.4.	Read Display Status (09h)	92
		8.2.5.	Read Display Power Mode (0Ah)	94
		8.2.6.	Read Display MADCTL (0Bh)	95
		8.2.7.	Read Display Pixel Format (0Ch)	96
		8.2.8.	Read Display Image Format (0Dh)	97
		8.2.9.	Read Display Signal Mode (0Eh)	98
		8.2.10.	Read Display Self-Diagnostic Result (0Fh)	99
		8.2.11.	Enter Sleep Mode (10h)	100
		8.2.12.	Sleep Out (11h)	101
		8.2.13.	Partial Mode ON (12h)	103
		8.2.14.	Normal Display Mode ON (13h)	104
		8.2.15.	Display Inversion OFF (20h)	105
		8.2.16.	Display Inversion ON (21h)	106
		8.2.17.	Gamma Set (26h)	107
		8.2.18.	Display OFF (28h)	108
		8.2.19.	Display ON (29h)	109
		8.2.20.	Column Address Set (2Ah)	110
		8.2.21.	Page Address Set (2Bh)	112
		8.2.22.	Memory Write (2Ch)	114
		8.2.23.	Color Set (2Dh)	115
		8.2.24.	Memory Read (2Eh)	116
		8.2.25.	Partial Area (30h)	118
		8.2.26.	Vertical Scrolling Definition (33h)	120
		8.2.27.	Tearing Effect Line OFF (34h)	124
		8.2.28.	Tearing Effect Line ON (35h)	125
		8.2.29.	Memory Access Control (36h)	127
		8.2.30.	Vertical Scrolling Start Address (37h)	129
		8.2.31.	Idle Mode OFF (38h)	131
		8.2.32.	Idle Mode ON (39h)	132



	8.2.33.	COLMOD: Pixel Format Set (3Ah)	134
	8.2.34.	Write_Memory_Continue (3Ch)	135
	8.2.35.	Read_Memory_Continue (3Eh)	137
	8.2.36.	Set_Tear_Scanline (44h)	139
	8.2.37.	Get_Scanline (45h)	140
	8.2.38.	Write Display Brightness (51h)	141
	8.2.39.	Read Display Brightness (52h)	142
	8.2.40.	Write CTRL Display (53h)	143
	8.2.41.	Read CTRL Display (54h)	145
	8.2.42.	Write Content Adaptive Brightness Control (55h)	147
	8.2.43.	Read Content Adaptive Brightness Control (56h)	148
	8.2.44.	Write CABC Minimum Brightness (5Eh)	149
	8.2.45.	Read CABC Minimum Brightness (5Fh)	150
	8.2.46.	Read ID1 (DAh)	151
	8.2.47.	Read ID2 (DBh)	152
	8.2.48.	Read ID3 (DCh)	153
8.3.	Descr	iption of Level 2 Command	154
	8.3.1.	RGB Interface Signal Control (B0h)	154
	8.3.2.	Frame Rate Control (In Normal Mode/Full Colors) (B1h)	155
	8.3.3.	Frame Rate Control (In Idle Mode/8 colors) (B2h)	157
	8.3.4.	Frame Rate control (In Partial Mode/Full Colors) (B3h)	159
	8.3.5.	Display Inversion Control (B4h)	161
	8.3.6.	Blanking Porch Control (B5h)	162
	8.3.7.	Display Function Control (B6h)	164
	8.3.8.	Entry Mode Set (B7h)	168
	8.3.9.	Backlight Control 1 (B8h)	169
	8.3.10.	Backlight Control 2 (B9h)	170
	8.3.11.	Backlight Control 3 (BAh)	172
	8.3.12.	Backlight Control 4 (BBh)	173
	8.3.13.	Backlight Control 5 (BCh)	175
	8.3.14.	Backlight Control 7 (BEh)	176
	8.3.15.	Backlight Control 8 (BFh)	177
	8.3.16.	Power Control 1 (C0h)	178
	8.3.17.	Power Control 2 (C1h)	179
	8.3.18.	VCOM Control 1(C5h)	180
	8.3.19.	VCOM Control 2(C7h)	182
	8.3.20.	NV Memory Write (D0h)	184
	8.3.21.	NV Memory Protection Key (D1h)	185
	8.3.22.	NV Memory Status Read (D2h)	186



		8.3.23.	Read ID4 (D3h)	187
		8.3.24.	Positive Gamma Correction (E0h)	188
		8.3.25.	Negative Gamma Correction (E1h)	189
		8.3.26.	Digital Gamma Control 1 (E2h)	190
		8.3.27.	Digital Gamma Control 2(E3h)	191
		8.3.28.	Interface Control (F6h)	192
	8.4	Descrip	otion of extend register command	195
		8.4.1.	Power control A (CBh)	195
		8.4.2.	Power control B (CFh)	196
		8.4.3.	Driver timing control A (E8h)	197
		8.4.4.	Driver timing control B (EAh)	198
		8.4.5.	Power on sequence control (EDh)	199
		8.4.6.	Enable 3 gamma (F2h)	200
		8.4.7.	Pump ratio control (F7h)	201
9.	Displa	ay Data F	RAM	202
	9.1.	Config	guration	202
	9.2.	Memo	ory to Display Address Mapping	203
		9.2.1.	Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF	203
		9.2.2.	Vertical Scroll Mode	204
		9.2.3.	Vertical Scroll Example	205
		9.2.4.	Case1: TFA+VSA+BFA < 320	205
		9.2.5.	Case2: TFA+VSA+BFA = 320 (Rolling Scrolling)	206
	9.3.	MCU	to memory write/read direction	207
10.	Tearin	ng Effect	Output	209
	10.1	. Tearin	g Effect Line Modes	209
	10.2	. Tearin	g Effect Line Timings	210
11.	Sleep	Out – C	ommand and Self-Diagnostic Functions of the Display Module	211
	11.1	. Regis	ter loading Detection	211
	11.2	. Funct	ionality Detection	212
12.	Powe	r ON/OF	F Sequence	213
	12.1	. Case	1 – RESX line is held High or Unstable by Host at Power ON	213
	12.2	. Case	2 – RESX line is held Low by Host at Power ON	214
	12.3	. Uncor	ntrolled Power Off	215
13.	Powe	r Level D	Definition	216
	13.1	. Powe	r Levels	216
	13.2	. Powe	r Flow Chart	217
14.	Gamr	na Curve	es Selection	218
	14.1	. Gamn	na Default Values (for NW type LC)	218
	14.2	. Gamn	na Curves	219





14.2.1. Gamma Curve 1 (GC0), applies the function y=x ^{2.2}	219
14.3. Gamma Curves	220
14.3.1. Grayscale Voltage Generation	220
14.3.2. Positive Gamma Correction	221
14.3.3. Negative Gamma Correction	222
15. Reset	223
15.1. Registers	223
15.2. Output Pins, I/O Pins	224
15.3. Input Pins	224
15.4. Reset Timing	225
16. Configuration of Power Supply Circuit	226
17. NV Memory Programming Flow	227
18. Electrical Characteristics	229
18.1. Absolute Maximum Ratings	229
18.2. DC Characteristics	230
19.2.1. General DC Characteristics	230
18.3. AC Characteristics	232
19.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)	232
19.3.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- $\rm II~$ system)	234
19.3.3. Display Serial Interface Timing Characteristics (3-line SPI system)	236
19.3.4. Display Serial Interface Timing Characteristics (4-line SPI system)	237
19.3.5. Parallel 18/16/6-bit RGB Interface Timing Characteristics	238
19. Revision History	239
20.Appendix-Application Notes	240





1. Introduction

ILI9341 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

ILI9341 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

ILI9341 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. ILI9341 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9341 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution: [240xRGB](H) x 320(V)
- Output:
 - > 720 source outputs
 - > 320 gate outputs
 - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
 - ➤ 8-bits, 9-bits, 16-bits, 18-bits interface with 8080- I /8080- II series MCU
 - ➤ 6-bits, 16-bits, 18-bits RGB interface with graphic controller
 - > 3-line / 4-line serial interface
- Display mode:
 - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
 - > Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
 - Sleep mode
- On chip functions:
 - VCOM generator and adjustment
 - Timing generator
 - Oscillator
 - DC/DC converter
 - Line/frame inversion
 - > 1 preset Gamma curve with separate RGB Gamma correction
- Content Adaptive Brightness Control
- MTP (3 times):
 - > 8-bits for ID1, ID2, ID3
 - > 7-bits for VCOM adjustment



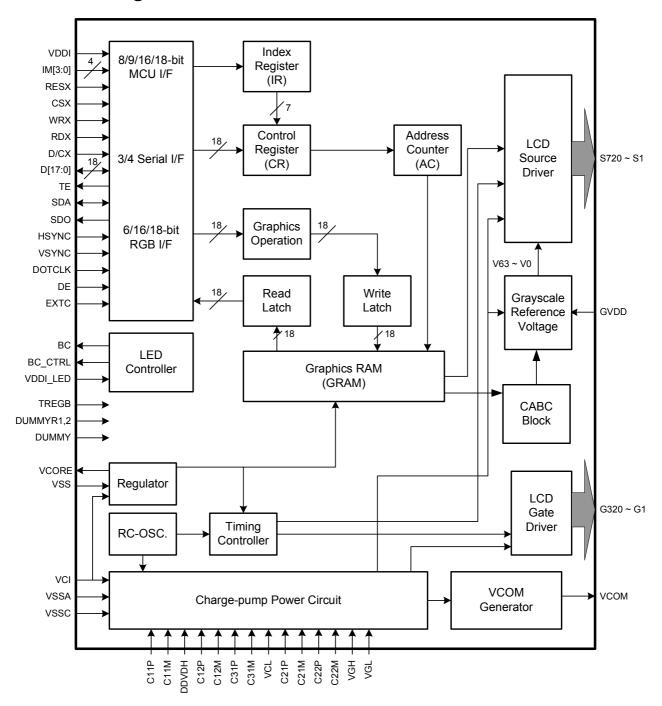


- Low -power consumption architecture
 - Low operating power supplies:
 - VDDI = 1.65V ~ 3.3V (logic)
 - VCI = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
 - Source/VCOM power supply voltage
 - DDVDH GND = 4.5V ~ 5.8V
 - VCL GND = -1.5V ~ -2.5V
 - > Gate driver output voltage
 - VGH GND = 10.0V ~ 16.0V
 - VGL GND = -5.0V ~ -10.0V
 - VGH VGL \leq 28V
 - > VCOM driver output voltage
 - VCOMH = 3.0V ~ (DDVDH 0.2)V
 - VCOML = (VCL+0.2)V ~ 0V
 - VCOMH VCOML ≤ 6.0 V
- ◆ Operate temperature range: -40°C to 85°C
- ◆ a-Si TFT LCD storage capacitor : Cst on Common structure only



ILI9341

3. Block Diagram







4. Pin Descriptions

	Power Supply Pins									
Pin Name	I/O	Туре	Descriptions							
VDDI	I	Р	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)							
VDDI_LED I			Power supply for LED driver interface. (1.65 ~ 3.3 V) If LED driver is not used, fix this pin at VDDI.							
VCI	I	Analog Power	High voltage power supply for analog circuit blocks (2.5 ~ 3.3 V)							
Vcore O		Digital Power	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization. Don't apply any external power to this pad							
VSS3	I	I/O Ground	System ground level for I/O circuits.							
VSS	I	Digital Ground	System ground level for logic blocks							
VSSA I Ar		Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.							
VSSC I Analog Ground		Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise							

Interface Logic Signals																			
Pin Name	I/O	Туре	Descriptions																
			- Select the MCU interface mode																
			IM3	IM2	IM1	IMO	MCU-Interface Mode	DB Pin in u	ise										
			IIVIS	IIVIZ	IIVII	IIVIO	MCO-interface Mode	Register/Content	GRAM										
			0	0	0	0	80 MCU 8-bit bus interface I	D[7:0]	D[7:0]										
			0	0	0	1	80 MCU 16-bit bus interface I	D[7:0]	D[15:0]										
			0	0	1	0	80 MCU 9-bit bus interface I	D[7:0]	D[8:0]										
		(VDDI/VSS)	0	0	1	1	80 MCU 18-bit bus interface I	D[7:0]	D[17:0]										
	I		(VDDI/VSS)	(VDDI/VSS)						0	1	0	1	3-wire 9-bit data serial interface I	SDA: In/O	JT			
									0	1	1	0	4-wire 8-bit data serial interface I	SDA: In/O	JT				
IM[3:0]					1	0	0	0	80 MCU 16-bit bus interface Ⅱ	D[8:1]	D[17:10], D[8:1]								
							1	0	0	1	80 MCU 8-bit bus interface II	D[17:10]	D[17:10]						
						1	0	1	0	80 MCU 18-bit bus interface II	D[8:1]	D[17:0]							
								1	0	1	1	80 MCU 9-bit bus interface II	D[17:10]	D[17:9]					
													1	1	0	1	3-wire 9-bit data serial interface II	SDI: In SDO: Ou	t
										1	1	1	0	4-wire 8-bit data serial interface II	SDI: In SDO: Ou	t			
			MPU	Paral	lel inte	erface	bus and serial inter	face select											
			If use RGB Interface must select serial interface.																
							or VSS.	niacc.											
	l		. ୮1X	เมเอ	uii al	וטטיי	UI VOO.												





			T				
RESX	_	MCU	This signal will reset the device and must be applied to properly				
TILOX	'	(VDDI/VSS)	initialize the chip.				
EXTC	1	MCU (VDDI/VSS)	Signal is active low. Extended command set enable. Low: extended command set is discarded. High: extended command set is accepted. Please connect EXTC to VDDI to read/write extended registers (RB0h~RCFh, RE0h~RFFh)				
CSX	I	MCU (VDDI/VSS)	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. * note1,2				
			This pin is used to select "Data or Command" in the parallel interface				
			or 4-wire 8-bit serial data interface.				
			When DCX = '1', data is selected.				
D/CX (SCL)	1	MCU (VDDI/VSS)	When DCX = '0', command is selected.				
		(This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit				
			serial data interface.				
			If not used, this pin should be connected to VDDI or VSS.				
RDX	1	MCU (VDDI/VSS)	8080- I /8080- II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use.				
WRX (D/CX)			- 8080- I /8080- II system (WRX): Serves as a write signal and writes data at the rising edge 4-line system (D/CX): Serves as command or parameter select. Fix to VDDI level when not in use.				
D[17:0]	I/O	MCU (VDDI/VSS)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to VSS level when not in use				
			When IM[3] : Low, Serial in/out signal.				
SDI/SDA	I/O	MCU	When IM[3]: High, Serial input signal.				
SDI/SDA	1/0	(VDDI/VSS)	The data is applied on the rising edge of the SCL signal.				
			If not used, fix this pin at VDDI or VSS.				
		MCU	Serial output signal.				
SDO	0	(VDDI/VSS)	The data is outputted on the falling edge of the SCL signal.				
			If not used, open this pin				
		MOLL	Tearing effect output pin to synchronize MPU to frame writing,				
TE	0	MCU (VDDI/VSS)	activated by S/W command. When this pin is not activated, this pin is				
		,	low. If not used, open this pin.				
DOTCLK	I	MCU (VDDI/VSS)	Dot clock signal for RGB interface operation.				
		(VDDI/VSS) MCU	Fix to VDDI or VSS level when not in use. Frame synchronizing signal for RGB interface operation.				
VSYNC	Ι	(VDDI/VSS)	Fix to VDDI or VSS level when not in use.				
HSYNC	I	MCU (VDDI/VSS)	Line synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.				
DE	I	MCU (VDDI/VSS)	Data enable signal for RGB interface operation. Fix to VDDI or VSS level when not in use.				





Note.

If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module.
 Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions.
 Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.



LCD Driver Input/Output Pins										
Pin Name	I/O	Туре	Descriptions							
S720~S1	0	Source	Source output signals Leave the pin to open when not in use.							
G320~G1	0	Gate	Gate output signals. Leave the pin to open when not in use.							
DDVDH O Stabilizing capacitor		Stabilizing	Output voltage of 1st step up circuit (2 x VCI). Input voltage to 2nd step up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization.							
VGH	0	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGH level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.							
VGL	0	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGL level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.							
VCL	0	Power Stabilizing capacitor	Power supply for VCOML. VCL = 0~ - VCI Connect this pad with a stabilizing capacitor.							
C11P, C11M C12P, C12M	Р	Stabilizing capacitor	Connect the charge-pumping capacitor for generating DDVDH level.							
C21P, C21M C22P, C22M	Р	Stabilizing capacitor	Connect the charge-pumping capacitor for generating VGH, VGL level.							
GVDD	0		High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.							
VCOM	0		Power supply pad for the TFT- display counter electrode. Charge recycling method is used with VCI and VSSA voltage. Connect this pad to the TFT-display counter electrode.							
LEDPWM	0		Output pin for PWM (Pulse Width Modulation) signal of LED driving. If not used, open this pad.							
LEDON	0		Output pin for enabling LED driving. If not used, open this pad.							

	Test Pins									
Pin Name	I/O	Type	Descriptions							
DUMMY	_	Open	Input pads used only for test purpose at IC-side.							
BOWNVIT		Ореп	During normal operation, leave these pads open.							





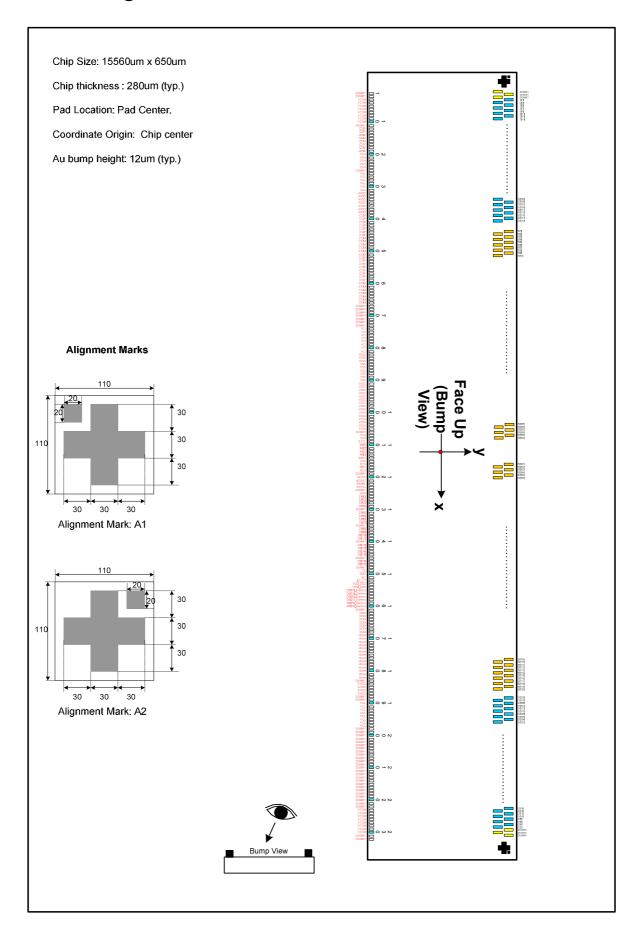
Liquid crystal power supply specifications Table

No.	Item		Description				
1	TFT Source Driver		720 pins (240 x RGB)				
2	TFT Gate Driver		320 pins				
3	TFT Display's Capacitor Structu	re	Cst structure only (Cs on Common)				
		S1 ~ S720	V0 ~ V63 grayscales				
4	Liquid Crystal Drive Output	G1 ~ G320	VGH - VGL				
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes				
5	Input Voltage	VDDI	1.65V ~ 3.30V				
5	Input Voltage	VCI	2.50V ~ 3.30V				
		DDVDH	4.5V ~ 5.8V				
		VGH	10.0V ~ 16.0V				
6	Liquid Crystal Drive Voltages	VGL	-5.0V ~ -10.0V				
		VCL	-1.5V ~ -2.5V				
		VGH - VGL	Max. 28.0V				
		DDVDH	VCI x2,				
7	Internal Step-up Circuits	VGH	VCI x6, x7				
'	internal Step-up Circuits	VGL	VCI x-3, x-4,				
		VCL	VCI x-1				



ILITEK

5. Pad Arrangement and Coordination







No.	Pad name	Χ	Υ	No.	Pad name	Χ	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
1	DUMMY	-7292.5	-248	51	C12M	-4292.5	-248	101	VSSA	-1292.5	-248	151	LEDPWM	2245	-248
2	DUMMY	-7232.5	-248	52	C12M	-4232.5	-248	102	VSSA	-1232.5	-248	152	LEDON	2330	-248
3	VCOM	-7172.5	-248	53	C11P	-4172.5	-248	103	VSSA	-1172.5	-248	153	VDDI_LED	2402.5	-248
4	VCOM	-7112.5	-248	54	C11P	-4112.5	-248	104	VSSA	-1112.5	-248	154	VDDI_LED	2462.5	-248
5	VCOM	-7052.5	-248	55	C11P	-4052.5	-248	105	VSSA	-1052.5	-248	155	DB[18]_Dummy	2535	-248
6	VCOM	-6992.5	-248	56	C11P	-3992.5	-248	106	DUMMY	-992.5	-248	156	DB[19]_Dummy	2620	-248
7	VCOM	-6932.5	-248	57	C11P	-3932.5	-248	107	VGS	-932.5	-248	157	DB[20]_Dummy	2705	-248
8	VCOM	-6872.5	-248	58	C11P	-3872.5	-248	108	VGS	-872.5	-248	158	DB[21]_Dummy	2790	-248
9	VCOM	-6812.5	-248	59	C11P	-3812.5	-248	109	EXTC	-812.5	-248	159	DB[22]_Dummy	2875	-248
10	VCOM	-6752.5	-248	60	C11M	-3752.5	-248	110	IM<3>	-752.5	-248	160	DB[23]_Dummy	2960	-248
11	DUMMY	-6692.5	-248	61	C11M	-3692.5	-248	111	IM<2>	-692.5	-248	161	DUMMY	3032.5	-248
12	C22P	-6632.5	-248	62	C11M	-3632.5	-248	112	IM<1>	-632.5	-248	162	VDDI	3092.5	-248
13	C22P	-6572.5	-248	63	C11M	-3572.5	-248	113	IM<0>	-572.5	-248	163	VDDI	3152.5	-248
14	C22M	-6512.5	-248	64	C11M	-3512.5	-248	114	RESX	-512.5	-248	164	VDDI	3212.5	-248
15	C22M	-6452.5	-248	65	C11M	-3452.5	-248	115	CSX	-452.5	-248	165	VDDI	3272.5	-248
16	C21P	-6392.5	-248	66	C11M	-3392.5	-248	116	DCX	-392.5	-248	166	VDDI	3332.5	-248
17	C21P	-6332.5	-248	67	(GND)	-3332.5	-248	117	WRX	-332.5	-248	167	VDDI	3392.5	-248
18	C21M	-6272.5	-248	68	(GND)	-3272.5	-248	118	RDX	-272.5	-248	168	VDDI	3452.5	-248
19	C21M	-6212.5	-248	69	(GND)	-3212.5	-248	119	DUMMY	-212.5	-248	169	Vcore	3512.5	-248
20	VGH	-6152.5	-248	70	(GND)	-3152.5	-248	120	VSYNC	-152.5	-248	170	Vcore	3572.5	-248
21	VGH	-6092.5	-248	71	(GND)	-3092.5	-248	121	HSYNC	-92.5	-248	171	Vcore	3632.5	-248
22	VGH	-6032.5	-248	72	(GND)	-3032.5	-248	122	ENABL	-32.5	-248	172	Vcore	3692.5	-248
23	VGH	-5972.5	-248	73	(GND)	-2972.5	-248	123	DOTCLK	27.5	-248	173	Vcore	3752.5	-248
24	VGH	-5912.5	-248	74	VCI	-2912.5	-248	124	DUMMY	87.5	-248	174	Vcore	3812.5	-248
25	DUMMY	-5852.5	-248	75	VCI	-2852.5	-248	125	SDA	160	-248	175	Vcore	3872.5	-248
26	VGL	-5792.5	-248	76	VCI	-2792.5	-248	126	DB[0]	245	-248	176	Vcore	3932.5	-248
27	VGL	-5732.5	-248	77	VCI	-2732.5	-248	127	DB[1]	330	-248	177	Vcore	3992.5	-248
28	VGL	-5672.5	-248	78	VCI	-2672.5	-248	128	DB[2]	415	-248	178	Vcore	4052.5	-248
29	VGL	-5612.5	-248	79	VCI	-2612.5	-248	129	DB[3]	500	-248	179	Vcore	4112.5	-248
30	VGL	-5552.5	-248	80	VCI	-2552.5	-248	130	DUMMY	572.5	-248	180	Vcore	4172.5	-248
31	VGL	-5492.5	-248	81	VCI	-2492.5	-248	131	DB[4]	645	-248	181	Vcore	4232.5	-248
32	DDVDH	-5432.5	-248	82	VSS3	-2432.5	-248	132	DB[5]	730	-248	182	Vcore	4292.5	-248
33	DDVDH	-5372.5	-248	83	VSS3	-2372.5	-248	133	DB[6]	815	-248	183	DUMMY	4352.5	-248
34	DDVDH	-5312.5	-248	84	VSS3	-2312.5	-248	134	DB[7]	900	-248	184	GVDD	4412.5	-248
35	DDVDH	-5252.5	-248	85	VSS	-2252.5	-248	135	DUMMY	972.5	-248	185	GVDD	4472.5	-248
36	DDVDH	-5192.5	-248	86	VSS	-2192.5	-248	136	DB[8]	1045	-248	186	GVDD	4532.5	-248
37	DDVDH	-5132.5	-248	87	VSS	-2132.5	-248	137	DB[9]	1130	-248	187	GVDD	4592.5	-248
38	DDVDH	-5072.5	-248	88	VSS	-2072.5	-248	138	DB[10]	1215	-248	188	DUMMY	4652.5	-248
39	C12P	-5012.5	-248	89	VSS	-2012.5	-248	139	DB[11]	1300	-248	189	DUMMY	4712.5	-248
40	C12P	-4952.5	-248	90	VSS	-1952.5	-248	140	DUMMY	1372.5	-248	190	VCL	4772.5	-248
41	C12P	-4892.5	-248	91	VSSC	-1892.5	-248	141	DB[12]	1445	-248	191	VCL	4832.5	-248
42	C12P	-4832.5	-248	92	VSSC	-1832.5	-248	142	DB[13]	1530	-248	192	VCL	4892.5	-248
43	C12P	-4772.5	-248	93	VSSC	-1772.5	-248	143	DB[14]	1615	-248	193	VCL	4952.5	-248
44	C12P	-4712.5	-248	94	VSSC	-1712.5	-248	144	DB[15]	1700	-248	194	VCL	5012.5	-248
45	C12P	-4652.5	-248	95	VSSC	-1652.5	-248	145	DUMMY	1772.5	-248	195	VCL	5072.5	-248
46	C12M	-4592.5	-248	96	VSSC	-1592.5	-248	146	DB[16]	1845	-248	196	VCL	5132.5	-248
47	C12M	-4532.5	-248	97	VSSC	-1532.5	-248	147	DB[17]	1930	-248	197	VCL	5192.5	-248
48	C12M	-4472.5	-248	98	VSSA	-1472.5	-248	148	DUMMY	2002.5	-248	198	DUMMY	5252.5	-248
49	C12M	-4412.5	-248	99	VSSA	-1412.5	-248	149	TE	2075	-248	199	DUMMY	5312.5	-248
50	C12M	-4352.5	-248	100	VSSA	-1352.5	-248	150	SDO	2160	-248	200	DUMMY	5372.5	-248





No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
201	DUMMY	5432.5	-248	251	G32	7147	224	301	G132	6447	224	351	G232	5747	224
202	DUMMY	5492.5	-248	252	G34	7133	93	302	G134	6433	93	352	G234	5733	93
203	DUMMY	5552.5	-248	253	G36	7119	224	303	G136	6419	224	353	G236	5719	224
204	DUMMY	5612.5	-248	254	G38	7105	93	304	G138	6405	93	354	G238	5705	93
205	DUMMY	5672.5	-248	255	G40	7091	224	305	G140	6391	224	355	G240	5691	224
206	(GND)	5732.5	-248	256	G42	7077	93	306	G142	6377	93	356	G242	5677	93
207	(GND)	5792.5	-248	257	G44	7063	224	307	G144	6363	224	357	G244	5663	224
208	(GND)	5852.5	-248	258	G46	7049	93	308	G146	6349	93	358	G246	5649	93
209	(GND)	5912.5	-248	259	G48	7035	224	309	G148	6335	224	359	G248	5635	224
210	(GND)	5972.5	-248	260	G50	7021	93	310	G150	6321	93	360	G250	5621	93
211	(GND)	6032.5	-248	261	G52	7007	224	311	G152	6307	224	361	G252	5607	224
212	(GND)	6092.5	-248	262	G54	6993	93	312	G154	6293	93	362	G254	5593	93
213	(GND)	6152.5	-248	263	G56	6979	224	313	G156	6279	224	363	G256	5579	224
214	DUMMY	6212.5	-248	264	G58	6965	93	314	G158	6265	93	364	G258	5565	93
215	DUMMY	6272.5	-248	265	G60	6951	224	315	G160	6251	224	365	G260	5551	224
216	DUMMY	6332.5	-248	266	G62	6937	93	316	G162	6237	93	366	G262	5537	93
217	DUMMY	6392.5	-248	267	G64	6923	224	317	G164	6223	224	367	G264	5523	224
218	DUMMY	6452.5	-248	268	G66	6909	93	318	G166	6209	93	368	G266	5509	93
219	DUMMY	6512.5	-248	269	G68	6895	224	319	G168	6195	224	369	G268	5495	224
220	DUMMY	6572.5	-248	270	G70	6881	93	320	G170	6181	93	370	G270	5481	93
221	DUMMY	6632.5	-248	271	G72	6867	224	321	G172	6167	224	371	G272	5467	224
222	DUMMY	6692.5	-248	272	G74	6853	93	322	G174	6153	93	372	G274	5453	93
223	VCOM	6752.5	-248	273	G76	6839	224	323	G176	6139	224	373	G276	5439	224
224	VCOM	6812.5	-248	274	G78	6825	93	324	G178	6125	93	374	G278	5425	93
225	VCOM	6872.5	-248	275	G80	6811	224	325	G180	6111	224	375	G280	5411	224
226	VCOM	6932.5	-248	276	G82	6797	93	326	G182	6097	93	376	G282	5397	93
227	VCOM	6992.5	-248	277	G84	6783	224	327	G184	6083	224	377	G284	5383	224
228	VCOM	7052.5	-248	278	G86	6769	93	328	G186	6069	93	378	G286	5369	93
229	VCOM	7112.5	-248	279	G88	6755	224	329	G188	6055	224	379	G288	5355	224
230	VCOM	7172.5	-248	280	G90	6741	93	330	G190	6041	93	380	G290	5341	93
231	DUMMY	7232.5	-248	281	G92	6727	224	331	G192	6027	224	381	G292	5327	224
232	DUMMY	7292.5	-248	282	G94	6713	93	332	G194	6013	93	382	G294	5313	93
233	DUMMY	7399	224	283	G96	6699	224	333	G196	5999	224	383	G296	5299	224
234	DUMMY	7385	93	284	G98	6685	93	334	G198	5985	93	384	G298	5285	93
235	DUMMY	7371	224	285	G100	6671	224	335	G200	5971	224	385	G300	5271	224
236	G2	7357	93	286	G102	6657	93	336	G202	5957	93	386	G302	5257	93
237	G4	7343	224	287	G104	6643	224	337	G204	5943	224	387	G304	5243	224
238	G6	7329	93	288	G106	6629	93	338	G206	5929	93	388	G306	5229	93
239	G8	7315	224	289	G108	6615	224	339	G208	5915	224	389	G308	5215	224
240	G10	7301	93	290	G110	6601	93	340	G210	5901	93	390	G310	5201	93
241	G12	7287	224	291	G112	6587	224	341	G212	5887	224	391	G312	5187	224
242	G14	7273	93	292	G114	6573	93	342	G214	5873	93	392	G314	5173	93
243	G16	7259	224	293	G116	6559	224	343	G216	5859	224	393	G316	5159	224
244	G18	7245	93	294	G118	6545	93	344	G218	5845	93	394	G318	5145	93
245	G20	7231	224	295	G120	6531	224	345	G220	5831	224	395	G320	5131	224
246	G22	7217	93	296	G122	6517	93	346	G222	5817	93	396	S720	5075	93
247	G24	7203	224	297	G124	6503	224	347	G224	5803	224	397	S719	5061	224
248	G26	7189	93	298	G126	6489	93	348	G226	5789	93	398	S718	5047	93
249	G28	7175	224	299	G128	6475	224	349	G228	5775	224	399	S717	5033	224
250	G30	7161	93	300	G130	6461	93	350	G230	5761	93	400	S716	5019	93





No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
401	S715	5005	224	451	S665	4305	224	501	S615	3605	224	551	S565	2905	224
402	S714	4991	93	452	S664	4291	93	502	S614	3591	93	552	S564	2891	93
403	S713	4977	224	453	S663	4277	224	503	S613	3577	224	553	S563	2877	224
404	S712	4963	93	454	S662	4263	93	504	S612	3563	93	554	S562	2863	93
405	S711	4949	224	455	S661	4249	224	505	S611	3549	224	555	S561	2849	224
406	S710	4935	93	456	S660	4235	93	506	S610	3535	93	556	S560	2835	93
407	S709	4921	224	457	S659	4221	224	507	S609	3521	224	557	S559	2821	224
408	S708	4907	93	458	S658	4207	93	508	S608	3507	93	558	S558	2807	93
409	S707	4893	224	459	S657	4193	224	509	S607	3493	224	559	S557	2793	224
410	S706	4879	93	460	S656	4179	93	510	S606	3479	93	560	S556	2779	93
411	S705	4865	224	461	S655	4165	224	511	S605	3465	224	561	S555	2765	224
412	S704	4851	93	462	S654	4151	93	512	S604	3451	93	562	S554	2751	93
413	S703	4837	224	463	S653	4137	224	513	S603	3437	224	563	S553	2737	224
414	S702	4823	93	464	S652	4123	93	514	S602	3423	93	564	S552	2723	93
415	S701	4809	224	465	S651	4109	224	515	S601	3409	224	565	S551	2709	224
416	S700	4795	93	466	S650	4095	93	516	S600	3395	93	566	S550	2695	93
417	S699	4781	224	467	S649	4081	224	517	S599	3381	224	567	S549	2681	224
418	S698	4767	93	468	S648	4067	93	518	S598	3367	93	568	S548	2667	93
419	S697	4753	224	469	S647	4053	224	519	S597	3353	224	569	S547	2653	224
420	S696	4739	93	470	S646	4039	93	520	S596	3339	93	570	S546	2639	93
421	S695	4725	224	471	S645	4025	224	521	S595	3325	224	571	S545	2625	224
422	S694	4711	93	472	S644	4011	93	522	S594	3311	93	572	S544	2611	93
423	S693	4697	224	473	S643	3997	224	523	S593	3297	224	573	S543	2597	224
424	S692	4683	93	474	S642	3983	93	524	S592	3283	93	574	S542	2583	93
425	S691	4669	224	475	S641	3969	224	525	S591	3269	224	575	S541	2569	224
426	S690	4655	93	476	S640	3955	93	526	S590	3255	93	576	S540	2555	93
427	S689	4641	224	477	S639	3941	224	527	S589	3241	224	577	S539	2541	224
428	S688	4627	93	478	S638	3927	93	528	S588	3227	93	578	S538	2527	93
429	S687	4613	224	479	S637	3913	224	529	S587	3213	224	579	S537	2513	224
430	S686	4599	93	480	S636	3899	93	530	S586	3199	93	580	S536	2499	93
431	S685	4585	224	481	S635	3885	224	531	S585	3185	224	581	S535	2485	224
432	S684	4571	93	482	S634	3871	93	532	S584	3171	93	582	S534	2471	93
433	S683	4557	224	483	S633	3857	224	533	S583	3157	224	583	S533	2457	224
434	S682	4543	93	484	S632	3843	93	534	S582	3143	93	584	S532	2443	93
435	S681	4529	224	485	S631	3829	224	535	S581	3129	224	585	S531	2429	224
436	S680	4515	93	486	S630	3815	93	536	S580	3115	93	586	S530	2415	93
437	S679	4501	224	487	S629	3801	224	537	S579	3101	224	587	S529	2401	224
438	S678	4487	93	488	S628	3787	93	538	S578	3087	93	588	S528	2387	93
439	S677	4473	224	489	S627	3773	224	539	S577	3073	224	589	S527	2373	224
440	S676	4459	93	490	S626	3759	93	540	S576	3059	93	590	S526	2359	93
441	S675	4445	224	491	S625	3745	224	541	S575	3045	224	591	S525	2345	224
442	S674	4431	93	492	S624	3731	93	542	S574	3031	93	592	S524	2331	93
443	S673	4417	224	493	S623	3717	224	543	S573	3017	224	593	S523	2317	224
444	S672	4403	93	494	S622	3703	93	544	S572	3003	93	594	S522	2303	93
445	S671	4389	224	495	S621	3689	224	545	S571	2989	224	595	S521	2289	224
446	S670	4375	93	496	S620	3675	93	546	S570	2975	93	596	S520	2275	93
447	S669	4361	224	497	S619	3661	224	547	S569	2961	224	597	S519	2261	224
448	S668	4347	93	498	S618	3647	93	548	S568	2947	93	598	S518	2247	93
449	S667	4333	224	499	S617	3633	224	549	S567	2933	224	599	S517	2233	224
450	S666	4319	93	500	S616	3619	93	550	S566	2919	93	600	S516	2219	93





No.	Pad name	Χ	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
601	S515	2205	224	651	S465	1505	224	701	S415	805	224	751	S365	105	224
602	S514	2191	93	652	S464	1491	93	702	S414	791	93	752	S364	91	93
603	S513	2177	224	653	S463	1477	224	703	S413	777	224	753	S363	77	224
604	S512	2163	93	654	S462	1463	93	704	S412	763	93	754	S362	63	93
		2149	224	655	S461	1449	224	705	S411	749	224	755	S361	49	224
606	S510	2135	93	656	S460	1435	93	706	S410	735	93	756	S360	-49	93
607	S509	2121	224	657	S459	1421	224	707	S409	721	224	757	S359	-63	224
608	S508	2107	93	658	S458	1407	93	708	S408	707	93	758	S358	-77	93
609	S507	2093	224	659	S457	1393	224	709	S407	693	224	759	S357	-91	224
610	S506	2079	93	660	S456	1379	93	710	S406	679	93	760	S356	-105	93
611	S505	2065	224	661	S455	1365	224	711	S405	665	224	761	S355	-119	224
612	S504	2051	93	662	S454	1351	93	712	S404	651	93	762	S354	-133	93
613	S503	2037	224	663	S453	1337	224	713	S403	637	224	763	S353	-147	224
614	S502	2023	93	664	S452	1323	93	714	S402	623	93	764	S352	-161	93
615	S501	2009	224	665	S451	1309	224	715	S401	609	224	765	S351	-175	224
616	S500	1995	93	666	S450	1295	93	716	S400	595	93	766	S350	-189	93
617	S499	1981	224	667	S449	1281	224	717	S399	581	224	767	S349	-203	224
618	S498	1967	93	668	S448	1267	93	718	S398	567	93	768	S348	-217	93
619	S497	1953	224	669	S447	1253	224	719	S397	553	224	769	S347	-231	224
620	S496	1939	93	670	S446	1239	93	720	S396	539	93	770	S346	-245	93
621	S495	1925	224	671	S445	1225	224	721	S395	525	224	771	S345	-259	224
622	S494	1911	93	672	S444	1211	93	722	S394	511	93	772	S344	-273	93
623	S493	1897	224	673	S443	1197	224	723	S393	497	224	773	S343	-287	224
624	S492	1883	93	674	S442	1183	93	724	S392	483	93	774	S342	-301	93
625	S491	1869	224	675	S441	1169	224	725	S391	469	224	775	S341	-315	224
626	S490	1855	93	676	S440	1155	93	726	S390	455	93	776	S340	-329	93
627	S489	1841	224	677	S439	1141	224	727	S389	441	224	777	S339	-343	224
628	S488	1827	93	678	S438	1127	93	728	S388	427	93	778	S338	-357	93
629	S487	1813	224	679	S437	1113	224	729	S387	413	224	779	S337	-371	224
630	S486	1799	93	680	S436	1099	93	730	S386	399	93	780	S336	-385	93
631	S485	1785	224	681	S435	1085	224	731	S385	385	224	781	S335	-399	224
632	S484	1771	93	682	S434	1071	93	732	S384	371	93	782	S334	-413	93
633	S483	1757	224	683	S433	1057	224	733	S383	357	224	783	S333	-427	224
634	S482	1743	93	684	S432	1043	93	734	S382	343	93	784	S332	-441	93
635	S481	1729	224	685	S431	1029	224	735	S381	329	224	785	S331	-455	224
636	S480	1715	93	686	S430	1015	93	736	S380	315	93	786	S330	-469	93
637	S479	1701	224	687	S429	1001	224	737	S379	301	224	787	S329	-483	224
638	S478	1687	93	688	S428	987	93	738	S378	287	93	788	S328	-497	93
639	S477	1673	224	689	S427	973	224	739	S377	273	224	789	S327	-511	224
640			93	690	S426	959	93	740	S376	259	93	790	S326	-525	93
641	S475	1645	224	691	S425	945	224	741	S375	245	224	791	S325	-539	224
642			93	692	S424	931	93	742	S374	231	93	792	S324	-553	93
	S473		224	693	S423	917	224	743	S373	217	224	793	S323	-567	224
	S472		93	694	S422	903	93	744	S372	203	93	794	S322	-581	93
	S471		224	695	S421	889	224	745	S371	189	224	795	S321	-595	224
	S470		93	696	S420	875	93	746	S370	175	93	796	S320	-609	93
	S469	1561	224	697	S419	861	224	747	S369	161	224	797	S319	-623	224
			93	698	S418	847	93	748	S368	147	93	798	S318	-637	93
	S467		224	699	S417	833	224	749	S367	133	224	799	S317	-651	224
	S466		93		S416	819	93	750	S366	119	93	800	S316	-665	93





Bot Satis Satis	No.	Pad name	Χ	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
902 8314				224		S265		224				224				224
803 \$313 707 224 853 \$283 -1407 224 903 \$213 2107 224 963 \$163 -2807 2807 2805 \$311 -725 224 855 \$261 -1435 224 905 \$211 -2135 224 965 \$161 -2835 283 286 \$85 \$260 -1448 324 905 \$211 -2135 284 965 \$161 2835 280 \$161 2835 280 \$161 2855 \$261 1448 324 906 \$210 \$214 93 966 \$150 386 \$255 \$1491 \$224 909 \$207 \$2191 224 965 \$156 286 \$255 \$1595 \$98 \$170 \$208 \$265 \$156 \$286 \$156 \$205 \$131 \$303 \$39 \$10 \$206 \$256 \$156 \$150 \$98 \$170 \$266 \$256 \$156 \$193				93		S264		93	902		-2093	93		S164		93
805 \$311 .735 224 855 \$261 .1435 224 905 \$211 .2135 .224 955 \$161 .2835 2849 \$607 \$309 .763 224 867 \$259 .1448 93 906 \$210 .2149 93 .966 \$160 .248 89 \$249 .977 \$309 .2163 .224 .967 .5199 .2883 .224 .907 .8299 .2183 .224 .967 .5199 .2283 .908 .8208 .2177 .93 .968 .5158 .22871 .2881 .2905 .909 .907 .2191 .224 .969 .917 .939 .908 .969 .917 .93 .968 .9181 .939 .908 .9205 .9191 .224 .911 .9205 .2219 .224 .961 .9516 .2905 .931 .962 .2245 .961 .931 .962 .9516 .2909 .931 .962 <td>803</td> <td>S313</td> <td>-707</td> <td>224</td> <td>853</td> <td>S263</td> <td>-1407</td> <td>224</td> <td>903</td> <td>S213</td> <td>-2107</td> <td>224</td> <td>953</td> <td>S163</td> <td>-2807</td> <td>224</td>	803	S313	-707	224	853	S263	-1407	224	903	S213	-2107	224	953	S163	-2807	224
955 S311 -735 224 855 S261 -1435 224 905 S211 -2135 224 955 S161 -2835 2806 807 5309 -763 224 867 S269 -1449 93 908 S208 -2163 224 957 S199 -888 S258 -1477 93 908 S208 -2177 93 958 S158 -2863 2287 289 830 800 S266 -1606 93 908 S208 -2177 93 958 S158 -2877 -2891 224 911 S205 -2191 224 961 S157 -2891 291 291 224 911 S205 -2191 224 961 S157 -2891 291 224 911 S205 -2219 924 961 S155 -2916 2905 93 960 S156 -2909 2905 93 961 S157 -2891	804	S312	-721	93	854	S262	-1421	93	904	S212	-2121	93	954	S162	-2821	93
907 S309 768 224 857 S259 1468 224 907 S209 2163 224 957 S159 2868 2860 858 S258 14477 93 908 S207 2191 224 899 S207 2191 224 895 S557 1491 224 909 S207 2191 224 890 S265 1450 2909 S207 2191 224 895 S557 1491 224 909 S207 2191 224 990 S156 22095 28 811 S300 80 S256 1569 30 911 S205 2219 224 961 S155 2249 92 33 962 S254 1561 33 914 S202 2261 93 966 S152 2991 290 324 865 S251 1567 224 915 S201 4759 93 966 S150 2929 93	805	S311	-735	224		S261	-1435	224	905	S211	-2135		955	S161	-2835	224
907 S309 768 224 857 S259 1468 224 907 S209 2163 224 957 S159 2868 2860 858 S258 14477 93 908 S207 2191 224 899 S207 2191 224 895 S557 1491 224 909 S207 2191 224 890 S265 1450 2909 S207 2191 224 895 S557 1491 224 909 S207 2191 224 990 S156 22095 28 811 S300 80 S256 1569 30 911 S205 2219 224 961 S155 2249 92 33 962 S254 1561 33 914 S202 2261 93 966 S152 2991 290 324 865 S251 1567 224 915 S201 4759 93 966 S150 2929 93	806	S310	-749	93	856	S260	-1449	93	906	S210	-2149	93	956	S160	-2849	93
808 \$308 -777 \$3 858 \$258 -1477 \$3 908 \$2007 -2911 224 859 \$257 -1491 224 909 \$207 -2919 22 959 \$111 \$305 -819 224 861 \$255 -1505 93 910 \$206 -2205 93 960 \$565 93 910 \$206 -2205 93 960 \$565 9295 \$93 911 \$205 -2219 224 961 \$155 -2919 2 961 \$155 -2919 2 961 \$155 -2919 2 961 \$155 -2919 2 961 \$155 -2919 2 961 \$155 -2919 2 961 \$155 -2919 2 961 \$155 -2919 2 961 \$155 -2919 2 961 \$155 -2919 2 961 \$154 -2935 3 861 -2881 8	807	S309	-763	224	857	S259	-1463	224	907		-2163	224	957	S159	-2863	224
810 \$306 -805 93 860 \$256 -1505 93 910 \$206 -2205 93 960 \$156 -2905 \$811 \$305 -819 224 861 \$255 -1519 224 911 \$206 -2219 224 963 \$156 -2919 224 963 \$252 -1533 93 91 \$200 -2233 93 962 \$154 -2933 98 813 868 \$252 -1561 93 914 \$202 -2241 963 \$153 -2947 24 963 \$155 291 -868 \$252 -1561 93 914 \$202 -2261 94 5151 -2995 95 968 \$156 \$291 -1603 224 917 \$199 -2203 224 967 \$151 -2995 924 968 \$156 -2991 968 \$156 -2993 991 \$152 -2261 93 968 \$156	808	S308	-777	93	858	S258	-1477	93	908		-2177	93	958	S158	-2877	93
811 S305 819 224 861 S255 1519 224 911 S205 2219 224 961 S155 2919 2 812 S304 -833 93 947 224 863 S253 1-157 224 813 S203 947 224 863 S153 929 928 5154 2933 864 S252 1-1561 93 914 S202 -2261 93 964 S152 -2961 861 S201 -275 224 965 S251 1-1575 224 915 S201 -2275 224 966 S151 -2976 281 818 S300 -889 93 866 S250 -1560 93 916 S201 -2275 224 966 S151 -2976 24 818 S299 -937 33 868 S248 -1617 93 917 S199 -2303 224 967 S149 -30	809	S307	-791	224	859	S257	-1491	224	909	S207	-2191	224	959	S157	-2891	224
811 \$305 \$819 \$224 861 \$255 \$1519 \$224 \$911 \$205 \$2219 \$24 \$961 \$155 \$2919 \$2883 \$233 \$947 \$248 \$83 \$253 \$1547 \$224 \$863 \$253 \$1547 \$244 \$863 \$253 \$1547 \$224 \$963 \$153 \$2947 \$249 \$963 \$153 \$2947 \$249 \$963 \$153 \$2947 \$249 \$963 \$153 \$2947 \$249 \$963 \$153 \$2947 \$249 \$963 \$153 \$2947 \$249 \$963 \$153 \$2947 \$2947 \$2401 \$968 \$153 \$2947 \$2947 \$2261 \$93 \$968 \$155 \$2947 \$2961 \$93 \$968 \$248 \$1603 \$244 \$175 \$928 \$93 \$968 \$149 \$93 \$968 \$247 \$1603 \$244 \$919 \$196 \$2345 \$93 \$968 \$144 \$9303<	810	S306	-805	93	860	S256	-1505	93	910	S206	-2205	93	960	S156	-2905	93
813 S303 -847 224 863 S253 -1547 224 913 S203 -2247 224 963 S153 -2947 2 814 S302 -861 93 866 S251 -1561 93 914 S202 -2261 93 964 S152 -2961 86 S250 -1569 93 916 S200 -2289 93 966 S151 -2975 224 865 S250 -1569 93 916 S200 -2289 93 966 S151 -2975 224 869 S248 -1603 224 917 S199 -2303 224 966 S149 3003 2 818 S298 -917 93 868 S248 -1631 224 917 S199 -2303 224 966 S149 3001 2 8231 224 969 S147 -3031 2 919 S197 231 224 968 </td <td>811</td> <td>S305</td> <td>-819</td> <td>224</td> <td>861</td> <td>S255</td> <td>-1519</td> <td>224</td> <td>911</td> <td>S205</td> <td>-2219</td> <td>224</td> <td>961</td> <td>S155</td> <td>-2919</td> <td>224</td>	811	S305	-819	224	861	S255	-1519	224	911	S205	-2219	224	961	S155	-2919	224
814 S302 -861 93 864 S252 -1561 93 914 S202 -2261 93 964 S152 2961 98 816 S300 -889 93 866 S250 -1589 93 916 S200 -2289 93 966 S150 -2989 93 966 S150 -2989 93 917 93 866 S250 -1589 93 916 S200 -2289 93 966 S150 -2989 93 918 919 S199 -2303 224 967 S149 -3003 24 917 93 868 S248 -1617 93 918 S198 -2317 93 968 S149 -0017 93 984 920 9196 9197 931 924 8197 5249 1465 93 970 5146 -1645 93 921 S197 939 924 921 S199 -2339	812	S304	-833	93	862	S254	-1533	93	912	S204	-2233	93	962	S154	-2933	93
814 S302 -861 93 864 S252 -1561 93 914 S202 -2261 93 964 S152 2961 98 816 S300 -889 93 866 S250 -1589 93 916 S200 -2289 93 966 S150 -2989 93 966 S150 -2989 93 917 93 866 S250 -1589 93 916 S200 -2289 93 966 S150 -2989 93 918 919 S199 -2303 224 967 S149 -3003 24 917 93 868 S248 -1617 93 918 S198 -2317 93 968 S149 -0017 93 984 920 9196 9197 931 924 8197 5249 1465 93 970 5146 -1645 93 921 S197 939 924 921 S199 -2339	813	S303	-847	224	863	S253	-1547	224	913	S203	-2247	224	963	S153	-2947	224
815 S301 875 224 866 S251 -1575 224 915 S201 -2275 224 965 S151 -2975 2 816 S300 -889 93 866 S250 -1589 93 916 S200 -2289 93 966 S150 -2999 903 224 867 S249 -1603 224 917 93 868 S248 -1617 93 918 S198 -2317 93 968 S148 -3017 93 986 S148 -3017 93 94 942 917 93 986 S148 -3017	814	S302	-861	93	864	S252	-1561	93	914		-2261	93	964	S152	-2961	93
816 S300 -889 93 866 S250 -1589 93 916 S200 -2289 93 966 S150 -2989 g 818 S299 -903 224 867 S249 -1603 224 917 S199 -2303 224 967 S149 -3003 2 818 S298 -917 93 868 S248 -1617 93 918 S198 -2317 93 968 S148 -3007 2 820 S296 -945 93 870 S246 -1645 93 919 S197 -2345 93 970 S146 -3045 92 821 S294 -973 93 872 S244 -1663 93 922 S194 -2373 93 972 S144 -3036 92 S293 -987 224 873 S243 -1667 924 922 S194 -2373 93	815	S301	-875	224	865	S251		224	915	S201	-2275	224	965	S151	-2975	224
818 S298 -917 93 868 S248 -1617 93 918 S198 -2317 93 968 S148 -3017 S 819 S297 -931 224 869 S247 -1631 224 919 5197 -2331 224 969 S147 -3031 2 820 S296 -945 93 868 S246 -1659 224 920 S196 -2345 93 770 S146 -3045 24 921 S195 -2359 224 971 S146 -3045 3059 224 921 S195 -2359 224 971 S146 -3045 3059 224 921 S195 -2359 224 971 S146 -3045 3059 224 921 S195 -2359 224 971 S146 -3045 3069 224 921 S195 -2359 224 971 S146 -3045 307				93			-1589	93	916		-2289		966	S150		93
819 S297 -931 224 869 S247 -1631 224 919 S197 -2331 224 969 S147 -3031 2 820 S296 -945 93 S246 -1645 93 920 S196 -2345 93 970 S146 -3045 92 821 S294 -973 93 872 S244 -1673 93 922 S194 -2373 93 972 S144 -3073 5243 -1687 224 923 S193 -2387 224 973 S143 -3087 224 923 S193 -2387 224 973 S143 -3087 224 924 S192 -2401 93 972 S144 -3073 292 S191 -2415 224 973 S143 -3087 224 923 S193 -2387 2241 928 S192 -2401 93 976 S144 -3073 93		S299	-903	224		S249	-1603	224	917	S199	-2303	224	967	S149	-3003	224
819 S297 -931 224 869 S247 -1631 224 919 S197 -2331 224 969 S147 -3031 2 821 S296 -945 93 871 S246 -1645 93 921 S196 -2345 93 970 S146 -3045 9 821 S294 -973 93 872 S244 -1673 93 922 1519 -2359 224 971 S145 -3059 224 823 S293 -987 224 875 S241 -1171 93 922 1519 -2359 224 973 S143 -3073 308 224 829 10101 93 874 S242 -1701 93 924 S192 -2401 93 974 S142 -3101 93 924 S192 -2401 93 976 S144 -3073 93 976 S141 -3115 93	818	S298	-917	93	868	S248	-1617	93	918	S198		93	968	S148	-3017	93
820 S296 -945 93 870 S246 -1645 93 920 S196 -2345 93 970 S146 -3045 821 S295 959 224 871 S245 -1667 93 921 S195 -2359 224 971 S145 -3059 2 823 S293 -987 224 873 S243 -1687 224 923 S193 -2387 922 S144 -3073 8 972 S144 -3073 8 922 S194 -2373 93 972 S144 -3073 8 922 S194 -2373 93 972 S144 -3073 8 922 S194 -2373 93 972 S144 -3073 8 23 S193 -2387 2401 93 974 S142 3011 524 8 8 2343 -1757 93 925 S191 -2415 224 975 S141			-931	224				1 1	919				969			224
821 S295 -959 224 871 S245 -1659 224 921 S195 -2359 224 971 S145 -3059 2 823 S293 -987 224 873 S243 -1687 224 923 S193 -2387 224 973 S144 -3073 9 824 S292 -1001 93 874 S242 -1701 93 924 S192 -2401 93 5142 -3011 9 826 S291 -1015 224 875 S241 -1715 224 925 S191 -2415 224 975 S141 -3115 224 925 S191 -2415 224 975 S141 -3115 224 925 S191 -2415 224 975 S141 -3115 224 925 S190 -2429 93 976 S140 -3129 926 S190 -2429 93 976 <td< td=""><td></td><td></td><td></td><td>93</td><td></td><td></td><td></td><td>93</td><td>920</td><td></td><td></td><td>93</td><td></td><td></td><td></td><td>93</td></td<>				93				93	920			93				93
822 S294 .973 93 872 S244 .1673 93 922 S194 .2373 93 972 S144 .3073 823 S293 .987 224 873 S243 .1687 224 923 S193 .2387 224 973 S143 .3087 2 824 S292 .1001 93 874 S242 .1701 93 924 S192 .2401 93 974 S142 .3101 9 826 S290 .1029 93 876 S240 .1729 93 926 S190 .2412 224 975 S141 .3115 29 5289 .1043 224 877 S239 .1743 224 927 S189 .2443 224 977 S139 .3143 2 828 S288 .1057 93 878 S238 .1757 93 928 S188 .2457 93 978 S138 </td <td></td> <td>971</td> <td></td> <td></td> <td>224</td>													971			224
823 S293 -987 224 873 S243 -1687 224 923 S193 -2387 224 973 S143 -3087 2 824 S292 -1001 93 874 S242 -1701 93 924 S192 -2401 93 974 S142 -3101 S 826 S290 -1029 93 876 S240 -1729 93 876 S141 -3115 2 827 S289 -1043 224 877 S239 -1743 224 925 S190 -2429 93 976 S140 -3129 8 288 1057 93 878 S238 -1757 93 928 S189 -2443 224 977 S139 -3143 2 8 880 S236 -1785 93 928 S188 -2457 93 978 S133 -3157 9 928 S187 -2471 224				93												93
824 \$292 -1001 93 874 \$242 -1701 93 924 \$192 -2401 93 974 \$142 -3101 \$825 \$291 -1015 224 875 \$241 -1715 224 925 \$191 -2415 224 975 \$141 -3115 2 827 \$289 -1043 224 877 \$239 -1743 224 927 \$189 -2443 224 977 \$139 -3143 2 828 \$288 -1057 93 878 \$239 -1773 224 977 \$139 -3143 2 829 \$287 -1071 224 878 \$237 -1771 224 928 \$188 -2471 24 979 \$137 -3171 2 938 \$186 -2485 93 980 \$136 -3185 \$286 -1085 93 881 \$236 -1786 93 931 \$186		S293														224
825 S291 -1015 224 875 S241 -1715 224 925 S191 -2415 224 975 S141 -3115 2 826 S290 -1029 93 877 S239 -1743 224 925 S190 -2429 93 976 S140 -3129 9 827 S289 -1043 224 878 S238 -1757 93 928 S189 -2443 224 977 S139 -3143 2 927 S189 -2443 224 977 S139 -3143 2 928 S188 -2457 93 978 S138 -3157 93 928 S188 -2457 93 978 S138 -3157 93 928 S188 -2457 93 978 S138 -3157 93 928 S188 -2457 93 978 S136 -3185 93 930 S186 -2485 93 988<				93												93
826 S290 -1029 93 876 S240 -1729 93 926 S190 -2429 93 976 S140 -3129 98 827 S289 -1043 224 877 S239 -1743 224 927 S189 -2443 224 977 S139 -3143 2 829 S287 -1071 224 878 S238 -1757 93 928 S188 -2457 93 978 S138 -3157 2 830 S286 -1085 93 880 S236 -1785 93 930 S186 -2485 93 980 S136 -3185 980 S136 -3185 980 S137 -3171 224 880 S236 -1785 93 930 S186 -2485 93 980 S137 -3171 2 933 S181 -2572 224 981 S135 -3199 2 148 932 </td <td></td> <td></td> <td></td> <td></td> <td></td> <td>_</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>224</td>						_										224
827 S289 -1043 224 877 S239 -1743 224 927 S189 -2443 224 978 S139 -3143 2 928 S188 -2457 93 978 S138 -3157 93 928 S188 -2457 93 978 S138 -3157 93 928 S188 -2457 93 978 S138 -3157 93 978 S138 -3157 93 928 S188 -2457 93 978 S138 -3157 93 930 S186 -2485 93 980 S136 -3171 224 930 S186 -2485 93 980 S136 -3185 93 931 S185 <td< td=""><td></td><td></td><td>-1029</td><td></td><td></td><td></td><td></td><td>93</td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td>93</td></td<>			-1029					93				1				93
828 S288 -1057 93 878 S238 -1757 93 928 S188 -2457 93 978 S138 -3157 93 829 S287 -1071 224 879 S237 -1771 224 929 S187 -2471 224 979 S137 -3171 2 830 S286 -1085 93 880 S236 -1785 93 930 S186 -2485 93 980 S136 -3185 98 83185 -2499 224 981 S135 -3199 224 931 S185 -2499 224 981 S135 -3199 224 931 S185 -2499 224 981 S135 -3199 224 931 S185 -2499 224 981 S135 -3199 23 931 S185 -2499 224 981 S135 -3199 23 931 S185 -2499 224 983	827	S289	-1043	224	877	S239	-1743	224	927	S189	-2443	224	977	S139	-3143	224
829 S287 -1071 224 879 S237 -1771 224 929 S187 -2471 224 979 S137 -3171 283 980 S286 -1085 93 880 S236 -1785 93 930 S186 -2485 93 980 S136 -3185 981 S135 -3199 982 S134 -3211 982 S184 -2513 93 982 S134 -3213 982 S134 -3213 983 S183 -2527 224 983 S181 -2551 983 S133 -3227 983 S181 -2551	828	S288	-1057	93	878	S238	-1757	93	928	S188	-2457		978	S138	-3157	93
831 \$285 -1099 224 881 \$235 -1799 224 931 \$185 -2499 224 981 \$135 -3199 2 832 \$284 -1113 93 882 \$234 -1813 93 932 \$184 -2513 93 982 \$134 -3213 983 \$183 -2527 224 983 \$133 -3227 224 983 \$183 -2527 224 983 \$133 -3227 224 983 \$183 -2527 224 983 \$133 -3227 224 983 \$183 -2527 224 983 \$133 -3227 224 983 \$183 -2527 224 983 \$181 -2555 224 985 \$131 -3255 224 985 \$231 -1855 224 935 \$181 -2559 93 986 \$130 -3269 985 \$131 -3255 224 987 \$129 -3283 <td>829</td> <td>S287</td> <td>-1071</td> <td>224</td> <td>879</td> <td></td> <td>-1771</td> <td>224</td> <td>929</td> <td>S187</td> <td>-2471</td> <td>224</td> <td>979</td> <td>S137</td> <td>-3171</td> <td>224</td>	829	S287	-1071	224	879		-1771	224	929	S187	-2471	224	979	S137	-3171	224
832 \$\scrip{834}\$ -1113 93 \$\scrip{882}\$ \$\scrip{224}\$ \$\scrip{883}\$ \$\scrip{233}\$ \$\scrip{184}\$ \$\scrip{2257}\$ \$224\$ \$\scrip{883}\$ \$\scrip{233}\$ \$\scrip{184}\$ \$\scrip{2555}\$ \$224\$ \$\scrip{983}\$ \$\scrip{183}\$ \$\scrip{3255}\$ \$\scrip{244}\$ \$\scrip{983}\$ \$\scrip{183}\$ \$\scrip{2577}\$ \$\scrip{244}\$ \$\scrip{884}\$ \$\scrip{232}\$ \$\scrip{184}\$ \$\scrip{2555}\$ \$\scrip{224}\$ \$\scrip{985}\$ \$\scrip{183}\$ \$\scrip{2555}\$ \$\scrip{224}\$ \$\scrip{985}\$ \$\scrip{183}\$ \$\scrip{2555}\$ \$\scrip{224}\$ \$\scrip{985}\$ \$\scrip{183}\$ \$\scrip{2555}\$ \$\scrip{224}\$ \$\scrip{985}\$ \$\scrip{183}\$ \$\scrip{3255}\$ \$\scrip{244}\$ \$\scrip{985}\$ \$\scrip{183}\$ \$\scrip{2555}\$ \$\scrip{224}\$ \$\scrip{985}\$ \$\scrip{183}\$ \$\scrip{3255}\$ \$\scrip{283}\$ \$\scrip{318}\$ \$325	830	S286	-1085	93	880	S236	-1785	93	930	S186	-2485	93	980	S136	-3185	93
832 \$284 -1113 93 \$882 \$234 -1813 93 932 \$184 -2513 93 982 \$134 -3213 983 \$313 -3227 224 983 \$133 -3227 224 983 \$133 -3227 224 983 \$133 -3227 224 983 \$133 -3227 224 983 \$133 -3227 224 983 \$133 -3227 224 983 \$133 -3227 224 983 \$133 -3227 224 983 \$133 -3227 224 983 \$133 -3227 224 983 \$133 -3227 224 985 \$131 -3255 224 985 \$131 -3255 224 985 \$131 -3255 224 985 \$131 -3255 224 985 \$131 -3255 224 985 \$131 -3255 224 985 \$131 -3255 224 985 \$131 -3	831	S285	-1099	224	881	S235	-1799	224	931	S185	-2499	224	981	S135	-3199	224
834 \$282 -1141 93 884 \$232 -1841 93 934 \$182 -2541 93 984 \$132 -3241 985 \$231 -1855 \$224 935 \$181 -2555 \$224 985 \$131 -3255 \$280 -1169 93 986 \$230 -1869 93 936 \$180 -2569 93 986 \$130 -3269 986 \$130 -3269 986 \$130 -3269 987 \$129 -3283 \$287 -1197 93 888 \$228 -1897 93 938 \$179 -2583 \$224 987 \$129 -3283 \$287 -1211 \$224 889 \$227 -1911 \$224 938 \$178 -2597 93 988 \$128 -3297 988 \$129 -3283 \$284 \$249 940 \$176 -2625 93 990 \$126 -3325 988 \$127 -3311 \$284	832	S284	-1113	93	882	S234	-1813	93	932	S184	-2513	93	982	S134	-3213	93
835 \$281 -1155 \$224 885 \$231 -1855 \$224 935 \$181 -2555 \$224 986 \$130 -3269 \$986 \$130 -3269 \$986 \$130 -3269 \$986 \$130 -3269 \$986 \$130 -3269 \$986 \$130 -3269 \$986 \$130 -3269 \$986 \$130 -3269 \$986 \$130 -3269 \$986 \$130 -3269 \$986 \$130 -3269 \$987 \$129 -3283 \$287 \$179 -2583 \$224 \$987 \$129 -3283 \$287 \$179 -2583 \$224 \$987 \$129 -3283 \$287 \$189 </td <td>833</td> <td>S283</td> <td>-1127</td> <td>224</td> <td>883</td> <td>S233</td> <td>-1827</td> <td>224</td> <td>933</td> <td>S183</td> <td>-2527</td> <td>224</td> <td>983</td> <td>S133</td> <td>-3227</td> <td>224</td>	833	S283	-1127	224	883	S233	-1827	224	933	S183	-2527	224	983	S133	-3227	224
836 S280 -1169 93 886 S230 -1869 93 936 S180 -2569 93 986 S130 -3269 987 S129 -3283 224 937 S179 -2583 224 987 S129 -3283 238 238 S278 -1197 93 888 S228 -1897 93 938 S178 -2597 93 988 S128 -3297 989 S127 -3311 289 S227 -1911 224 940 S176 -2625 93 990 S126 -3325 941 S175 -2639 224 991 S125 -3339 942 S174 -2653	834	S282	-1141	93	884	S232	-1841	93	934	S182	-2541	93	984	S132	-3241	93
836 S280 -1169 93 886 S230 -1869 93 936 S180 -2569 93 986 S130 -3269 987 S129 -3283 224 937 S179 -2583 224 987 S129 -3283 238 238 S278 -1197 93 888 S228 -1897 93 938 S178 -2597 93 988 S128 -3297 989 S127 -3311 289 S227 -1911 224 940 S176 -2625 93 990 S126 -3325 941 S175 -2639 224 991 S125 -3339 942 S174 -2653	835	S281	-1155	224	885	S231	-1855	224	935	S181	-2555	224	985	S131	-3255	224
837 S279 -1183 224 887 S229 -1883 224 937 S179 -2583 224 988 S129 -3283 224 938 S178 -2597 93 988 S128 -3297 93 938 S178 -2597 93 988 S128 -3297 93 938 S178 -2597 93 988 S128 -3297 93 938 S176 -2611 224 989 S127 -3311 29 940 S176 -2625 93 990 S126 -3325 941 S175 -2639 224 991 S125 -3339 942 S174 -2653 93	836	S280	-1169	93	886	S230		93	936			93	986	S130	-3269	93
838 \$\ \text{S278}\$ -1197 93 888 \$\ \text{S228}\$ -1897 93 938 \$\ \text{S178}\$ -2597 93 988 \$\ \text{S128}\$ -3297 989 \$\ \text{S127}\$ 989 \$\ \text{S127}\$ -3311 2 939 \$\ \text{S177}\$ -2611 224 989 \$\ \text{S127}\$ -3311 2 989 \$\ \text{S127}\$ -3311 2 989 \$\ \text{S177}\$ -3311 2 989 \$\ \text{S127}\$ -3311 2 989 \$\ \text{S128}\$ -3325 989 91 \$\ \text{S128}\$ 991	837	S279		224	887	S229	-1883	224	937	S179		224	987	S129	-3283	224
839 S277 -1211 224 889 S227 -1911 224 939 S177 -2611 224 989 S127 -3311 2 840 S276 -1225 93 890 S226 -1925 93 940 S176 -2625 93 990 S126 -3325 9 841 S275 -1239 224 891 S225 -1939 224 941 S175 -2639 224 991 S125 -3339 2 842 S274 -1253 93 892 S224 -1953 93 942 S174 -2639 224 991 S125 -3339 2 843 S273 -1267 224 893 S223 -1967 224 943 S173 -2667 224 993 S123 -3367 2 844 S272 -1281 93 894 S222 -1981 93 944 S172				93	888			93				93	988			93
840 \$276 -1225 93 841 \$275 -1239 \$224 842 \$274 -1253 93 843 \$273 -1267 \$224 844 \$272 -1281 93 845 \$271 -1295 \$224 846 \$270 -1309 93 847 \$269 -1323 \$224 897 \$219 -2023 \$224 940 \$176 -2625 93 941 \$175 -2639 \$224 941 \$175 -2639 \$224 941 \$175 -2639 \$224 942 \$174 -2653 93 943 \$173 -2667 \$224 944 \$172 -2681 93 945 \$171 -2695 \$224 946 \$170 -2709 93 896 \$220 -2009 93 897 \$219 -2023 \$224 947 \$169 -2723 \$224 997 \$119 -3423 947 \$169 -2723 \$224 997 \$119 -3423	839			224	889			1 1	939			1 1	989	1	-3311	224
841 \$275 -1239 \$224 891 \$225 -1939 \$224 941 \$175 -2639 \$224 991 \$125 -3339 \$2 842 \$274 -1253 93 892 \$224 -1953 93 942 \$174 -2653 93 992 \$124 -3353 9 843 \$273 -1267 \$224 893 \$223 -1967 \$224 943 \$173 -2667 \$224 993 \$123 -3367 \$2 844 \$272 -1281 93 894 \$222 -1981 93 944 \$172 -2681 93 994 \$122 -3381 98 845 \$271 -1295 \$224 895 \$221 -1995 \$224 945 \$171 -2695 \$224 995 \$121 -3395 \$2 846 \$270 -1309 93 896 \$220 -2009 93 946 \$170 -2709 93 996 \$120 -3409 997 847 \$269 -1323 \$224 97 \$219 -2023 \$224 947 \$169 -2723 \$224 997 \$119																93
842 S274 -1253 93 843 S273 -1267 224 844 S272 -1281 93 845 S271 -1295 224 846 S270 -1309 93 847 S269 -1323 224 897 S219 -2023 224 942 S174 -2653 93 943 S173 -2667 224 944 S172 -2681 93 944 S172 -2681 93 945 S171 -2695 224 946 S170 -2709 93 948 S120 -3409 949 S121 -3423 944 S172 -2681 93 945 S171 -2695 224 946 S170 -2709 93 946 S170 -2709 93 947 S169 -2723 224 947 S169 -2723 224 947 S169 -2723 224 948 S120 -3409 949 S120 -3409 947 S169 -2723 <td></td> <td>1</td> <td></td> <td>224</td>														1		224
843 S273 -1267 224 844 S272 -1281 93 S223 -1967 224 844 S272 -1281 93 894 S222 -1981 93 845 S271 -1295 224 846 S270 -1309 93 847 S269 -1323 224 897 S219 -2023 224 943 S173 -2667 224 944 S172 -2681 93 945 S171 -2695 224 946 S170 -2709 93 995 S121 -3395 946 S170 -2709 93 996 S120 -3409 947 S169 -2723 224 997 S119 -3423								1 1						1		93
844 \$272 -1281 93 845 \$271 -1295 224 846 \$270 -1309 93 847 \$269 -1323 \$224 894 \$222 -1981 93 895 \$221 -1995 224 896 \$220 -2009 93 897 \$219 -2023 224 944 \$172 -2681 93 945 \$171 -2695 224 946 \$170 -2709 93 996 \$120 -3409 947 \$169 -2723 224 997 \$119 -3423 224																224
845 S271 -1295 224 895 S221 -1995 224 945 S171 -2695 224 995 S121 -3395 2 846 S270 -1309 93 896 S220 -2009 93 946 S170 -2709 93 996 S120 -3409 9 847 S269 -1323 224 897 S219 -2023 224 947 S169 -2723 224 997 S119 -3423 2												1 1				93
846 S270 -1309 93 896 S220 -2009 93 946 S170 -2709 93 996 S120 -3409 989 847 S269 -1323 224 897 S219 -2023 224 947 S169 -2723 224 997 S119 -3423 224								1 1								224
847 S269 -1323 224 897 S219 -2023 224 947 S169 -2723 224 997 S119 -3423 2														1		93
												1 1		1		224
1 2 1 2 1 2 1 2 1 2 2 2 2 2 2 2 2 2 2 2								1				1 1				93
														1		224
								1				1 1		1		93





No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
1001	S115	-3479	224	1051	S65	-4179	224	1101	S15	-4879	224	1151	G249	-5621	224
1002	S114	-3493	93	1052	S64	-4193	93	1102	S14	-4893	93	1152	G247	-5635	93
1003	S113	-3507	224	1053	S63	-4207	224	1103	S13	-4907	224	1153	G245	-5649	224
1004	S112	-3521	93	1054	S62	-4221	93	1104	S12	-4921	93	1154	G243	-5663	93
1005	S111	-3535	224	1055	S61	-4235	224	1105	S11	-4935	224	1155	G241	-5677	224
1006	S110	-3549	93	1056	S60	-4249	93	1106	S10	-4949	93	1156	G239	-5691	93
1007	S109	-3563	224	1057	S59	-4263	224	1107	S9	-4963	224	1157	G237	-5705	224
1008	S108	-3577	93	1058	S58	-4277	93	1108	S8	-4977	93	1158	G235	-5719	93
1009	S107	-3591	224	1059	S57	-4291	224	1109	S7	-4991	224	1159	G233	-5733	224
1010	S106	-3605	93	1060	S56	-4305	93	1110	S6	-5005	93	1160	G231	-5747	93
1011	S105	-3619	224	1061	S55	-4319	224	1111	S5	-5019	224	1161	G229	-5761	224
1012	S104	-3633	93	1062	S54	-4333	93	1112	S4	-5033	93	1162	G227	-5775	93
1013	S103	-3647	224	1063	S53	-4347	224	1113	S3	-5047	224	1163	G225	-5789	224
1014	S102	-3661	93	1064	S52	-4361	93	1114	S2	-5061	93	1164	G223	-5803	93
1015	S101	-3675	224	1065	S51	-4375	224	1115	S1	-5075	224	1165	G221	-5817	224
1016	S100	-3689	93	1066	S50	-4389	93	1116	G319	-5131	93	1166	G219	-5831	93
1017	S99	-3703	224	1067	S49	-4403	224	1117	G317	-5145	224	1167	G217	-5845	224
1018	S98	-3717	93	1068	S48	-4417	93	1118	G315	-5159	93	1168	G215	-5859	93
1019	S97	-3731	224	1069	S47	-4431	224	1119	G313	-5173	224	1169	G213	-5873	224
1020	S96	-3745	93	1070	S46	-4445	93	1120	G311	-5187	93	1170	G211	-5887	93
1021	S95	-3759	224	1071	S45	-4459	224	1121	G309	-5201	224	1171	G209	-5901	224
1022	S94	-3773	93	1072	S44	-4473	93	1122	G307	-5215	93	1172	G207	-5915	93
1023	S93	-3787	224	1073	S43	-4487	224	1123	G305	-5229	224	1173	G205	-5929	224
1024	S92	-3801	93	1074	S42	-4501	93	1124	G303	-5243	93	1174	G203	-5943	93
1025	S91	-3815	224	1075	S41	-4515	224	1125	G301	-5257	224	1175	G201	-5957	224
1026	S90	-3829	93	1076	S40	-4529	93	1126	G299	-5271	93	1176	G199	-5971	93
1027	S89	-3843	224	1077	S39	-4543	224	1127	G297	-5285	224	1177	G197	-5985	224
1028	S88	-3857	93	1078	S38	-4557	93	1128	G295	-5299	93	1178	G195	-5999	93
1029	S87	-3871	224	1079	S37	-4571	224	1129	G293	-5313	224	1179	G193	-6013	224
1030	S86	-3885	93	1080	S36	-4585	93	1130	G291	-5327	93	1180	G191	-6027	93
1031	S85	-3899	224	1081	S35	-4599	224	1131	G289	-5341	224	1181	G189	-6041	224
1032	S84	-3913	93	1082	S34	-4613	93	1132	G287	-5355	93	1182	G187	-6055	93
1033	S83	-3927	224	1083	S33	-4627	224	1133	G285	-5369	224	1183	G185	-6069	224
1034	S82	-3941	93	1084	S32	-4641	93	1134	G283	-5383	93	1184	G183	-6083	93
1035	S81	-3955	224	1085	S31	-4655	224	1135	G281	-5397	224	1185	G181	-6097	224
1036	S80	-3969	93	1086	S30	-4669	93	1136	G279	-5411	93	1186	G179	-6111	93
1037	S79	-3983	224	1087	S29	-4683	224	1137	G277	-5425	224	1187	G177	-6125	224
1038	S78	-3997	93	1088	S28	-4697	93	1138	G275	-5439	93	1188	G175	-6139	93
1039	S77	-4011	224	1089	S27	-4711	224	1139	G273	-5453	224	1189	G173	-6153	224
1040	S76	-4025	93	1090	S26	-4725	93	1140	G271	-5467	93	1190	G171	-6167	93
1041	S75	-4039	224	1091	S25	-4739	224	1141	G269	-5481	224	1191	G169	-6181	224
1042	S74	-4053	93	1092	S24	-4753	93	1142	G267	-5495	93	1192	G167	-6195	93
1043	S73	-4067	224	1093	S23	-4767	224	1143	G265	-5509	224	1193	G165	-6209	224
1044	S72	-4081	93	1094	S22	-4781	93	1144	G263	-5523	93	1194	G163	-6223	93
1045	S71	-4095	224	1095	S21	-4795	224	1145	G261	-5537	224	1195	G161	-6237	224
1046	S70	-4109	93	1096	S20	-4809	93	1146	G259	-5551	93	1196	G159	-6251	93
1047	S69	-4123	224	1097	S19	-4823	224	1147	G257	-5565	224	1197	G157	-6265	224
1048	S68	-4137	93	1098	S18	-4837	93	1148	G255	-5579	93	1198	G155	-6279	93
1049	S67	-4151	224	1099	S17	-4851	224	1149	G253	-5593	224	1199	G153	-6293	224
1050	S66	-4165	93	1100	S16	-4865	93	1150	G251	-5607	93	1200	G151	-6307	93



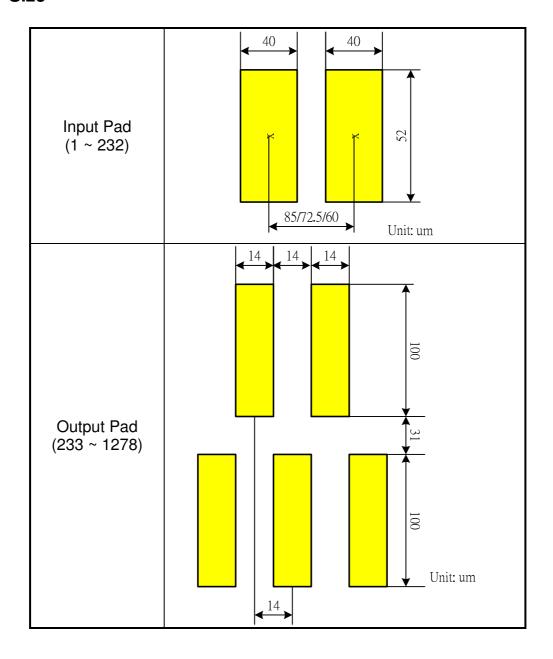
No.	Pad name	Χ	Υ	
1201	G149	-6321	224	1
1202	G147	-6335	93	1
1203	G145	-6349	224	1
1204	G143	-6363	93	1
1205	G141	-6377	224	1
1206	G139	-6391	93	1
1207	G137	-6405	224	1
1208	G135	-6419	93	1
1209	G133	-6433	224	1
1210	G131	-6447	93	1
1211	G129	-6461	224	1
1212	G127	-6475	93	1
1213	G125	-6489	224	1
1214	G123	-6503	93	1
1215	G121	-6517	224	1
1216	G119	-6531	93	1
1217	G117	-6545	224	1
1218	G115	-6559	93	1
1219	G113	-6573	224	1
1220	G111	-6587	93	1
1221	G109	-6601	224	1
1222	G107	-6615	93	1
1223	G105	-6629	224	
1224	G103	-6643	93	
1225	G101	-6657	224	1
1226	G99	-6671	93	1
1227	G97	-6685	224	
1228	G95	-6699	93	1
1229	G93	-6713	224	Ľ
1230	G91	-6727	93	
1231	G89	-6741	224	
1232	G87	-6755	93	
1233	G85	-6769	224	
1234	G83	-6783	93	
1235	G81	-6797	224	
1236	G79	-6811	93	
1237	G77	-6825	224	
1238	G75	-6839	93	
			224	
1239	G73	-6853		
1240	G71	-6867	93	
1241	G69	-6881	224	
1242	G67	-6895	93	
1243	G65	-6909	224	
1244	G63	-6923	93	
1245	G61	-6937	224	
1246	G59	-6951	93	
1247	G57	-6965	224	
1248	G55	-6979	93	
1249	G53	-6993	224	
1250	G51	-7007	93	

,	No.	Pad name	Χ	Υ
4	1251	G49	-7021	224
	1252	G47	-7035	93
4	1253	G45	-7049	224
	1254	G43	-7063	93
4	1255	G41	-7077	224
	1256	G39	-7091	93
4	1257	G37	-7105	224
	1258	G35	-7119	93
4	1259	G33	-7133	224
	1260	G31	-7147	93
4	1261	G29	-7161	224
	1262	G27	-7175	93
4	1263	G25	-7189	224
	1264	G23	-7203	93
4	1265	G21	-7217	224
	1266	G19	-7231	93
4	1267	G17	-7245	224
	1268	G15	-7259	93
4	1269	G13	-7273	224
	1270	G11	-7287	93
4	1271	G9	-7301	224
	1272	G7	-7315	93
4	1273	G5	-7329	224
	1274	G3	-7343	93
4	1275	G1	-7357	224
	1276	DUMMY	-7371	93
4	1277	DUMMY	-7385	224
	1278	DUMMY	-7399	93
4				

Alignment mark	X	Υ
Left COG Align	-7480	225
Right COG Align	7480	225



BUMP Size







6. Block Function Description

MCU System Interface

ILI9341 provides four kinds of MCU system interface with 8080- I /8080- II series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IMO	MCI I Interface Mode	nterface Mode Pins in use		
IIVIO	IIVIZ	IIVII	IIVIO	MCO-Interface Mode	Register/Content	GRAM	
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX	
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX	
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX	
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX	
0	1	0	1	3-wire 9-bit data serial interface I		SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface I		SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX	
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX	
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX	
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX	
1	1	0	1	3-wire 9-bit data serial interface II		SCL,SDI,SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface II	e Ⅱ SCL,SDI,D/CX,SDO, CSX		

In 8080- I /8080- II series parallel interface, the registers are accessed by the D[17:0] data pins.

	8080- I	Series			8080- п		Operation	
CSX	D/CX	RDX	WRX	CSX	D/CX	RDX	WRX	
"L"	"L"	"H"		"L"	"L"	"H"		Write command
"L"	"H"		"H"	"L"	"H"		"H"	Read parameter
"L"	"H"	"H"	<u> </u>	"L"	"H"	"H"		Write parameter

Parallel RGB Interface

ILI9341 also supports the RGB interface for displaying a moving picture. When the RGB interface is selected, display operation is synchronized with externally signals, VSYNC, HSYNC, and DOTCLK and input display data is written in synchronization with these signals according to the polarity of enable signal (DE).

Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 240(RGB) x320 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9341 can display maximum 262,144 colors.





Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as GVDD, VGH, VGL and VCOM for driving TFT LCD panel.

Timing controller

The timing controller generates all the timing signals for display and GRAM access.

Oscillator

ILI9341 incorporates RC oscillator circuit and output a stable output frequency for operation.

Panel Driver Circuit

Liquid crystal display driver circuit consists of 720-output source driver (S1~S720), 320-output gate driver (G1~G320), and VCOM signal.





7. Function Description

7.1. MCU interfaces

ILI9341 provides the 8-/9-/16-/18-bit parallel system interface for 8080- I /8080- II series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

7.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	11/14	IMO	MCU-Interface Mode		Pins in use	
IIVIS	IIVIZ	IM1	IIVIU	MCO-Interface Mode	Register/Content	GRAM	
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX	
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0] ,WRX,RDX,CSX,D/CX	
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0] ,WRX,RDX,CSX,D/CX	
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0] ,WRX,RDX,CSX,D/CX	
0	1	0	1	3-wire 9-bit data serial interface I		SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface I		SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX	
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX	
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX	
1	0	1	1	8080 MCU 9-bit bus interface Ⅱ	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX	
1	1	0	1	3-wire 9-bit data serial interface II		SCL,SDI,SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface II	ce II SCL,SDI,D/CX,SDO, CSX		





7.1.2. 8080- I Series Parallel Interface

ILI9341 can be accessed via 8-/9-/16-/18-bit MCU 8080- I series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9341 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9341 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080- I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080- I Interface selection is done when IM3 pin is low state (VSS level). Interface bus width can be selected by IM [2:0] bits.

The selection of 8080- I series parallel interface is shown as the table in the following.

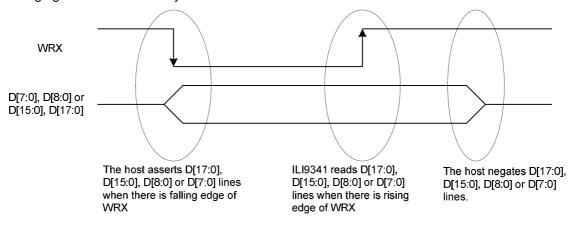
IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
					"L"	<u></u>	"H"	"L"	Write command code.
				2000 MOLLO hit hun interfere. I	"L"	"H"	ſ	"H"	Read internal status.
0	0	0	0	8080 MCU 8-bit bus interface I	"L"	$ \downarrow $	"H"	"H"	Write parameter or display data.
					"L"	"H"	ſ	"H"	Reads parameter or display data.
					"L"		"H"	"L"	Write command code.
				0000 MOLL to his hous interfered. I	"L"	"H"	ſ	"H"	Read internal status.
0	0	0	1	8080 MCU 16-bit bus interface I	"L"	$ \downarrow $	"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
					"L"	ſ	"H"	"L"	Write command code.
				0000 MOLLO hit have beterfore. T	"L"	"H"	ſ	"H"	Read internal status.
0	0	1	0	8080 MCU 9-bit bus interface I	"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"	ſ	"H"	Reads parameter or display data.
					"L"	ſ	"H"	"L"	Write command code.
			4	0000 MOLL to his hour intentage -	"L"	"H"	<u></u>	"H"	Read internal status.
0	0	1	1	8080 MCU 18-bit bus interface I	"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.



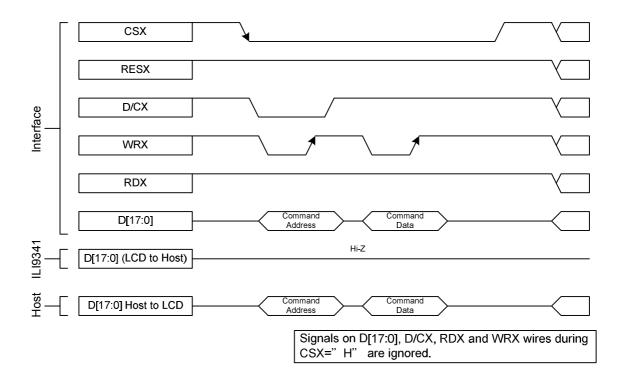
7.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080- I MCU interface.



Note: WRX is an unsynchronized signal (It can be stopped)



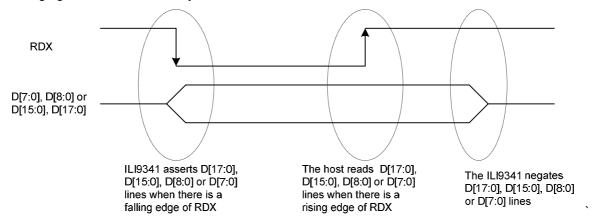




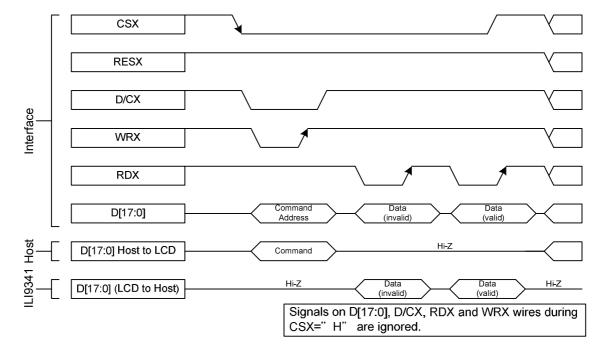
7.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080- I MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.





7.1.5. 8080- II Series Parallel Interface

ILI9341 can be accessed via 8-/9-/16-/18-bit MCU 8080- series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9341 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9341 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

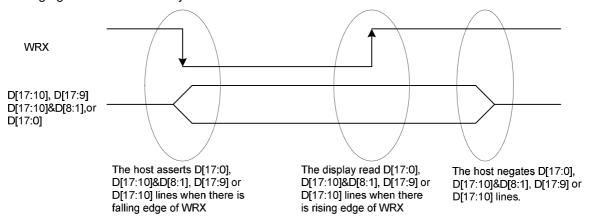
The 8080- II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080- II Interface selection is done when IM3 pin is high state (VDDI level). Interface bus width can be selected by IM [2:0] bits.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
1	0	0	0	8080 MCU 16-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"	_	"H"	Read internal status.
					"L"	\int	"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
	0	0	1	8080 MCU 8-bit bus interface II	"L"	\int	"H"	"L"	Write command code.
1					"L"	"H"		"H"	Read internal status.
					"L"	ſ	"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
	0	1	0	8080 MCU 18-bit bus interface II	"L"		"H"	"L"	Write command code.
1					"L"	"H"		"H"	Read internal status.
					"L"	\vdash	"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
1	0	1	1	8080 MCU 9-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"	ſ	"H"	Reads parameter or display data.

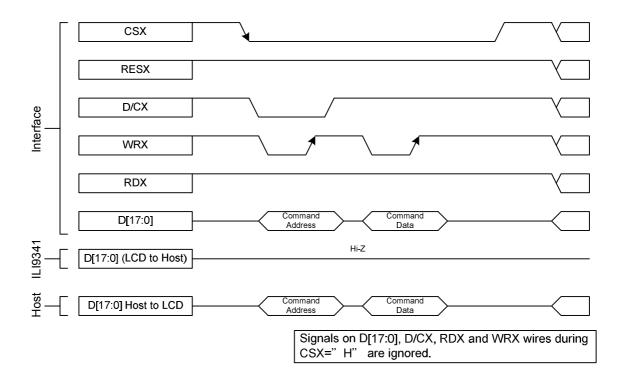


7.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.



Note: WRX is an unsynchronized signal (It can be stopped)



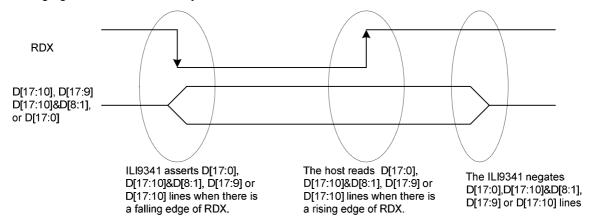




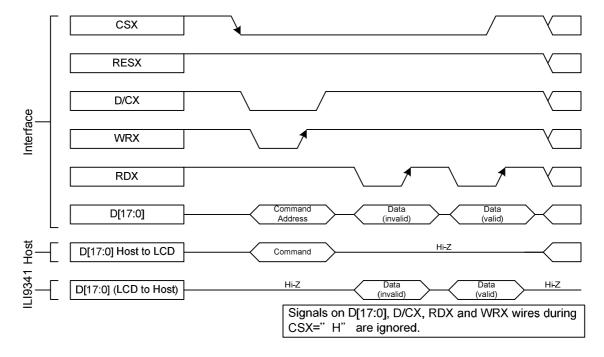
7.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080- II MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.





7.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

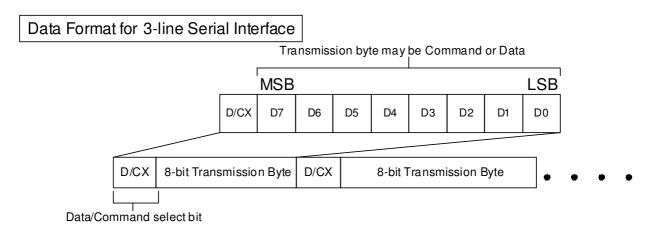
IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	1	0	1	3-line serial interface	"L"	-		Read/Write command, parameter or display data.
0	1	1	0	4-line serial interface	"L"	'H/L"	ſ	Read/Write command, parameter or display data.
1	1	0	1	3-line serial interface	"L"	-	ſ	Read/Write command, parameter or display data.
1	1	1	0	4-line serial interface	"L"	'H/L"	ſ	Read/Write command, parameter or display data.

ILI9341 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9341. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.1.9. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to ILI9341. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

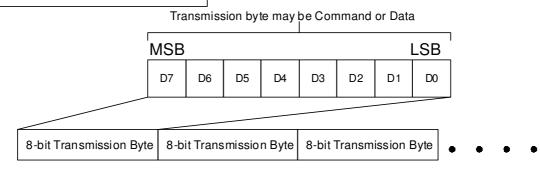
Any instruction can be sent in any order to ILI9341 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.







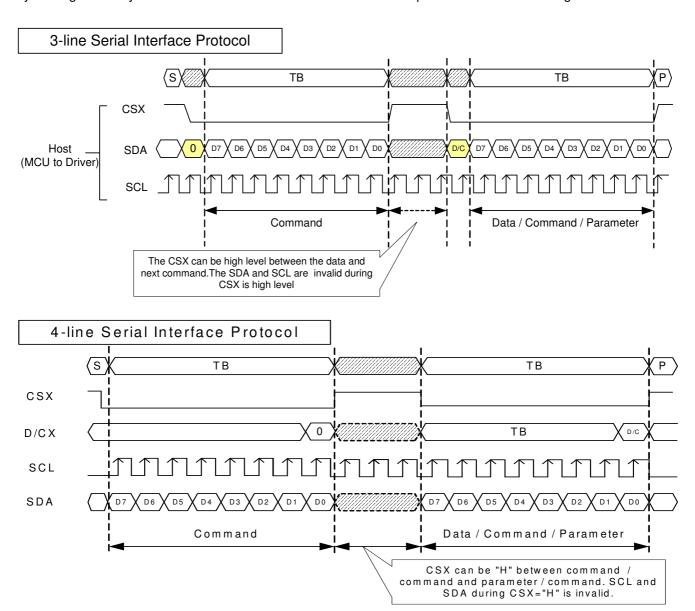
Data Format for 4-line Serial Interface







Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9341 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.



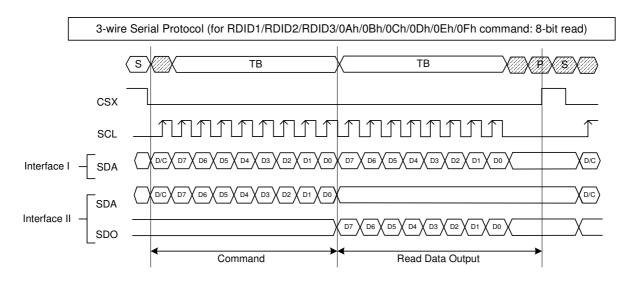


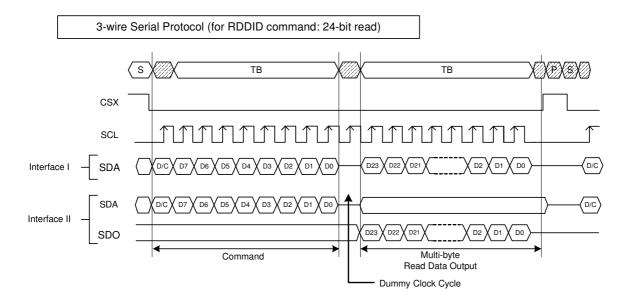


7.1.10. Read Cycle Sequence

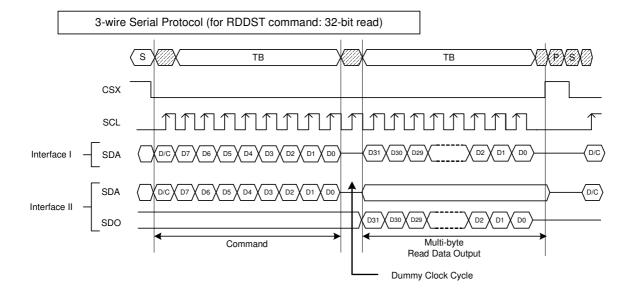
The read mode of interface means that the host reads register's parameter or display data from ILI9341. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9341 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

3-wire Serial Interface Protocol





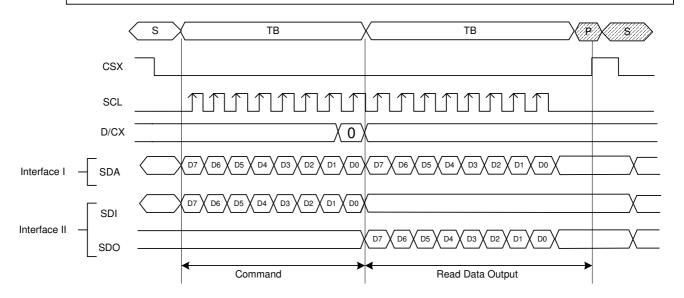




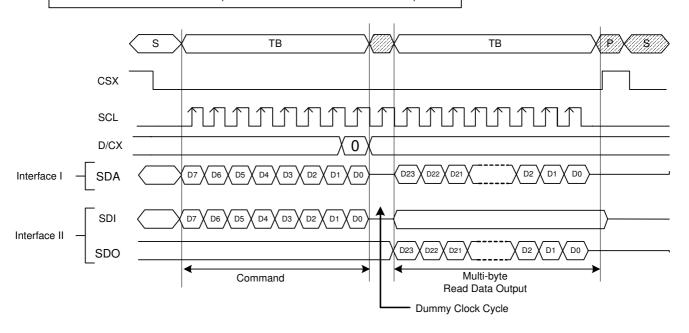


4-wire Serial Interface Protocol

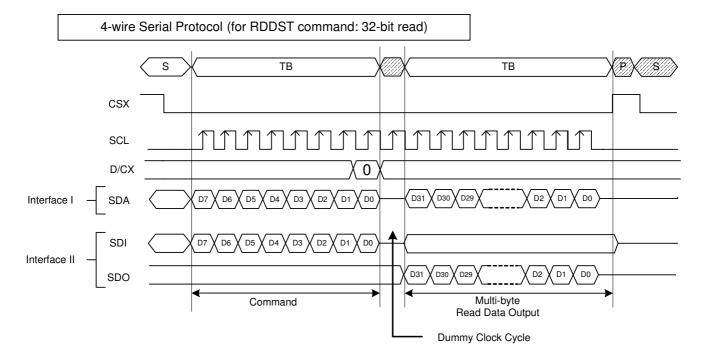
4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-wire Serial Protocol (for RDDID command: 24-bit read)





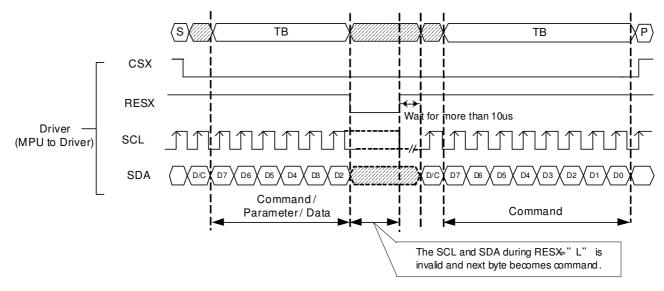




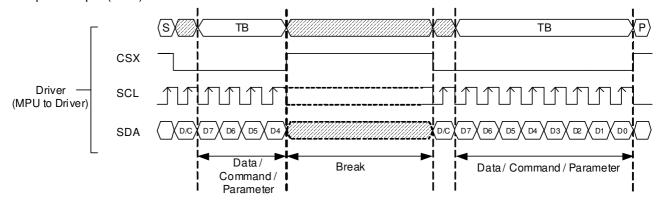


7.1.11. Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

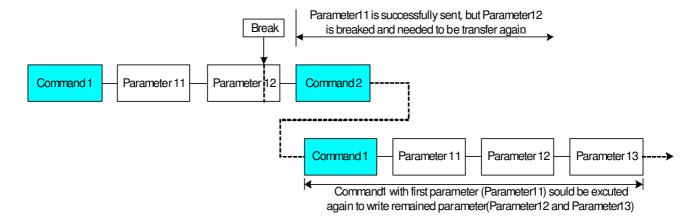


If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

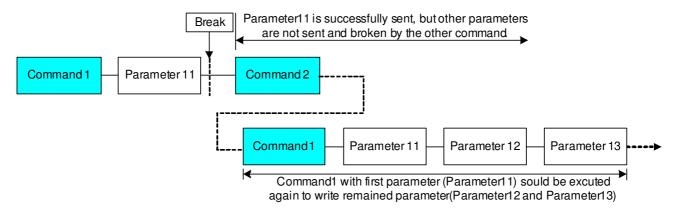


If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.





If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.





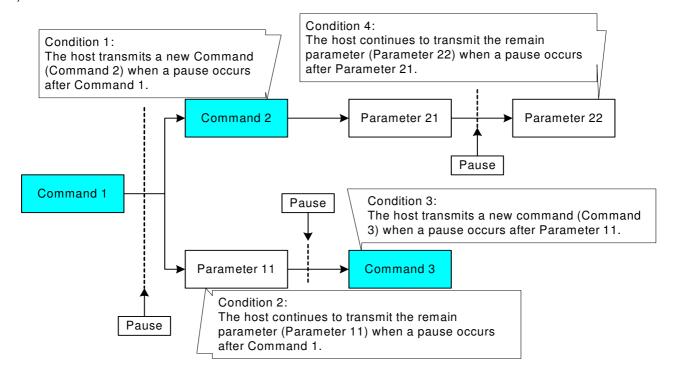


7.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9341 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

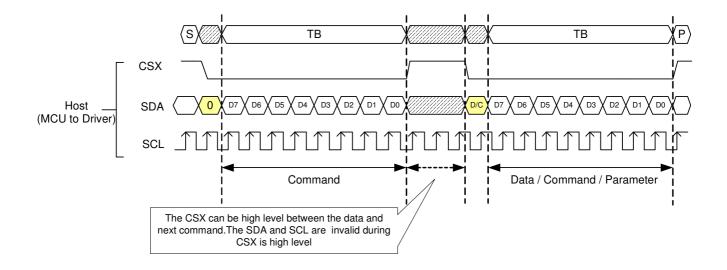
This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

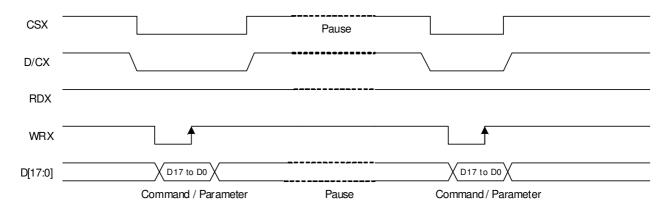




7.1.13. Serial Interface Pause (3_wire)



7.1.14. Parallel Interface Pause





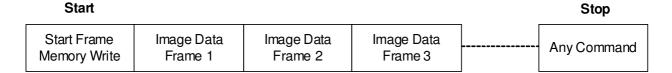


7.1.15. Data Transfer Mode

ILI9341 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

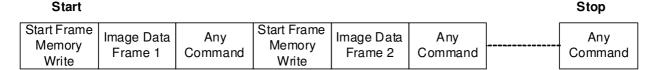
7.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.





7.2. RGB Interface

7.2.1. RGB Interface Selection

ILI9341 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to "10", the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to "11", the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.

ILI9341 supports several pixel formats that can be selected by DPI [2:0] bits of "Pixel Format Set (3Ah)" and RIM bit of RF6h command. The selection of a given interfaces is done by setting RCM [1:0] and DPI [2:0] as show in the following table.

RCM	l[1:0]	RIM	D	PI[2:	:0]	RGB Interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)		VSYNC, HSYNC, DE, DOTCLK,D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)	DE Mode	VSYNC, HSYNC, DE, DOTCLK, D[17:13] & D[11:1]
1	0	1	1	1	0	6-bit RGB interface (262K colors)	Valid data is determined by the DE signal	VSYNC, HSYNC, DE, DOTCLK, D[5:0]
1	0	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, D[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)		VSYNC, HSYNC, DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)	SYNC Mode In SYNC mode, DE signal is ignored;	VSYNC, HSYNC, DOTCLK, D[17:13] & D[11:1]
1	1	1	1	1	0	6-bit RGB interface (262K colors)	blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, D[5:0]
1	1	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, D[5:0]

18-bit data bus interface (D[17:0] is used) , DPI[2:0] = 110, and RIM=0

D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

18bpp Frame Memory Write R[5] R[4] R[3] R[2] R[1] R[0] G[5] G[4] G[3] G[2] G[1] G[0] B[5] B[4] B[3] B[2] B[1] B[0]

16-bit data bus interface (D[17:13] & D[11:1] is used) , DPI[2:0] = 101, and RIM=0

D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

16bpp Frame Memory Write R[4] R[3] R[2] R[1] R[0] G[5] G[4] G[3] G[2] G[1] G[0] B[4] B[3] B[2] B[1] B[0]

The LSB data of red/blue color depends on the EPF[1:0] setting.

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 110, and RIM=1

D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0

18bpp Frame Memory Write R[5] R[4] R[3] R[2] R[1] R[0] G[5] G[4] G[3] G[2] G[1] G[0] B[5] B[4] B[3] B[2] B[1] B[0]

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 101, and RIM=1

16bpp Frame Memory Write **R[4] R[3] R[2] R[1] R[0] G[5] G[4] G[3] G[2] G[1] G[0] B[4] B[3] B[2] B[1] B[0]**

The LSB data of red/blue color depends on the EPF[1:0] setting.

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when

D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1

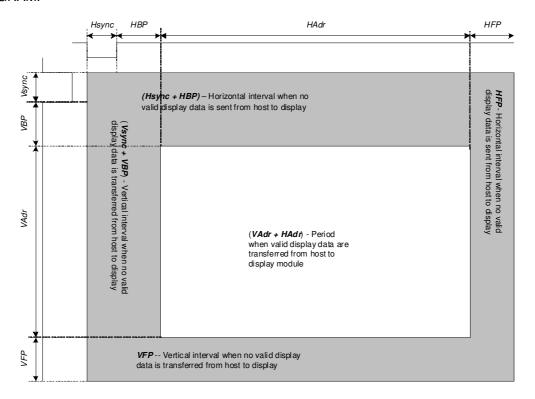




there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Тур.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Typical values are setting example when used with panel resolution 240 x 320 (QVGA), clock frequency 6.35MHz and frame





frequency about 70Hz.

Notes:

- 1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
- 2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
- 3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

Also make sure that

(Number of PCLK per 1 line) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV

Setting Example for Display Control Clock in RGB Interface Operation

Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing DOTCLK.

PCDIV [5:0]: Number of DOTCLK during internal clock PCLKD's high / low period. In units of 1 clock.

PCDIV specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 615KHz is the smallest. Set PCDIV follow the restriction (Number of PCLK in 1H) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV.

Setting Example: To set frame frequency to 70Hz:

Internal Clock

```
Internal Oscillation Clock: 615\text{KHz}
DIV[1:0] = 2'b0 \text{ (x 1/1)}
RTN[4:0] = 5'h1b \text{ (27 clocks)}
FP = 7'h2 \text{ (2 lines)}, BP = 7'h2 \text{ (2 lines)}, NL = 6'h27 \text{ (320 lines)}
Frame Rate \rightarrow 70.30Hz
```

DOTCLK

```
HSYNC = 10 CLK

HBP = 20 CLK

HFP=10 CLK

70Hz x (2 + 320 + 2) lines x (10 + 20 + 240 + 10) clocks = 6.35MHz

DOTCLK frequency = 6.35MHz

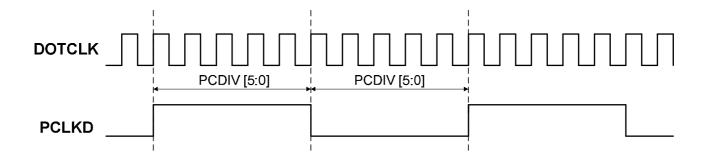
6.35 MHz / 615KHz = 10.32 \Box Set PCDIV so that PCLK is divided by 10.

external fosc = 6.35 MHz / 10 = 635KHz

PCDIV = [6.35MHz / 635KHz) / 2 ] - 1 = 4

PCDIV[5:0] = 6'h04 (10 DOTCLK)
```



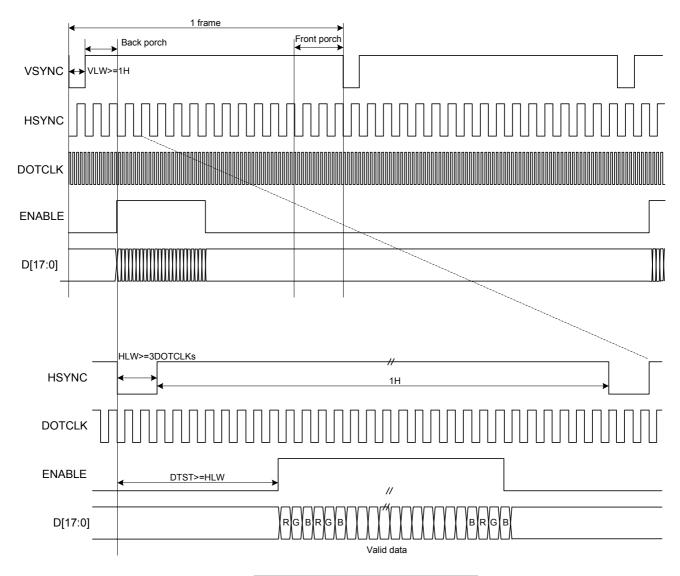






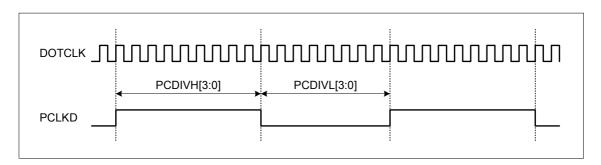
7.2.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.



VLW: VSYNC Low Width HLW: HSYNC Low Width

DTST: Data Transfer Startup Time



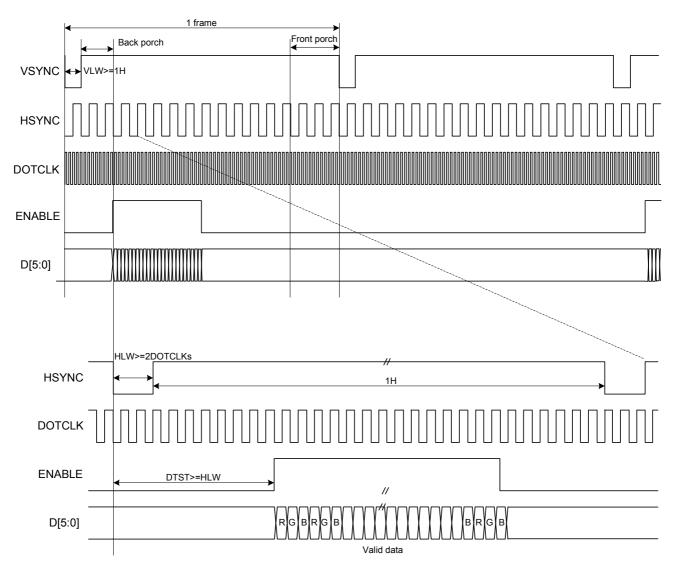
Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.



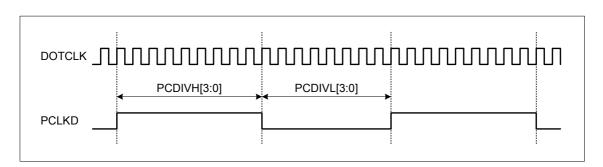


The timing chart of 6-bit RGB interface mode is shown as below:



VLW: VSYNC Low Width HLW: HSYNC Low Width

DTST: Data Transfer Startup Time



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.



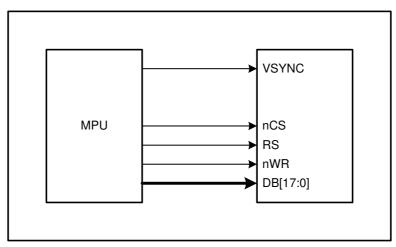


Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

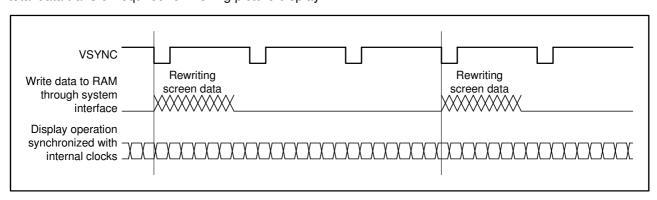


7.3. VSYNC Interface

ILI9341 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080- I /8080- I system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".

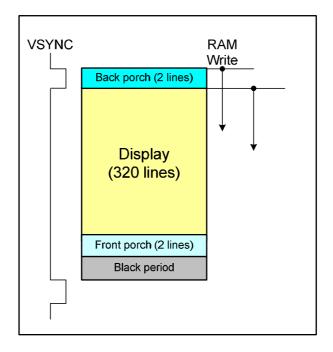


In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.









The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (VFP) + BackPorch (VBP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\textit{Minimum RAM write speed [Hz]} > \frac{240 \times \textit{DisplayLines(NL)}}{[\textit{BackPorch(VBP)} + \textit{DisplayLines(NL)} - \textit{margins]} \times \textit{Clocks per line} \times (1/\textit{fosc})}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 240 RGB × 320 lines Lines: 320 lines (NL = 100111)

Back porch: 2 lines (VBP = 0000010) Front porch: 2 lines (VFP = 0000010)

Frame frequency: 70 Hz Frequency fluctuation: 10%

Internal oscillator clock (fosc.) [Hz] = $70 \times [320+2+2] \times 27$ clocks $\times (1.1/0.9) = 748$ KHz





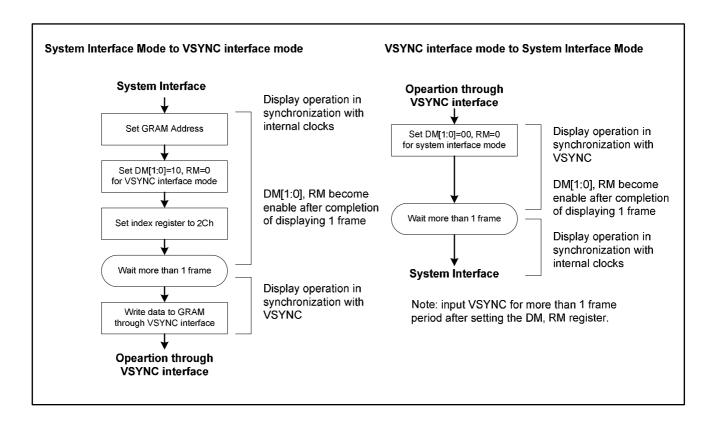
When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz] > 240 x 320 x 748K / [(2 + 320 - 2)lines x 27clocks] = 6.65 MHz

The above theoretical value is calculated based on the premise that the ILI9341 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 6.65MHz or more will guarantee the completion of GRAM write operation before the ILI9341 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

- 1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
- 2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
- 3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
- 4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.









7.4. Color Depth Conversion Look Up Table

When ILI9341 operates in parallel 16-bit interface, the color depth conversion is done by look-up table and extend input data format to 18-bit. See the detailed for look-up table of color depth conversion.

R input (5-bit) 16-bit/pixel -mode 65,536 colors	R output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	R ₀₀₅ R ₀₀₄ R ₀₀₃ R ₀₀₂ R ₀₀₁ R ₀₀₀	1
00001	R ₀₁₅ R ₀₁₄ R ₀₁₃ R ₀₁₂ R ₀₁₁ R ₀₁₀	2
00010	R ₀₂₅ R ₀₂₄ R ₀₂₃ R ₀₂₂ R ₀₂₁ R ₀₂₀	3
00011	R ₀₃₅ R ₀₃₄ R ₀₃₃ R ₀₃₂ R ₀₃₁ R ₀₃₀	4
00100	R ₀₄₅ R ₀₄₄ R ₀₄₃ R ₀₄₂ R ₀₄₁ R ₀₄₀	5
00101	R ₀₅₅ R ₀₅₄ R ₀₅₃ R ₀₅₂ R ₀₅₁ R ₀₅₀	6
00110	R ₀₆₅ R ₀₆₄ R ₀₆₃ R ₀₆₂ R ₀₆₁ R ₀₆₀	7
00111	R ₀₇₅ R ₀₇₄ R ₀₇₃ R ₀₇₂ R ₀₇₁ R ₀₇₀	8
01000	R ₀₈₅ R ₀₈₄ R ₀₈₃ R ₀₈₂ R ₀₈₁ R ₀₈₀	9
01001	R ₀₉₅ R ₀₉₄ R ₀₉₃ R ₀₉₂ R ₀₉₁ R ₀₉₀	10
01010	R ₁₀₅ R ₁₀₄ R ₁₀₃ R ₁₀₂ R ₁₀₁ R ₁₀₀	11
01011	R ₁₁₅ R ₁₁₄ R ₁₁₃ R ₁₁₂ R ₁₁₁ R ₁₁₀	12
01100	R ₁₂₅ R ₁₂₄ R ₁₂₃ R ₁₂₂ R ₁₂₁ R ₁₂₀	13
01101	R ₁₃₅ R ₁₃₄ R ₁₃₃ R ₁₃₂ R ₁₃₁ R ₁₃₀	14
01110	R ₁₄₅ R ₁₄₄ R ₁₄₃ R ₁₄₂ R ₁₄₁ R ₁₄₀	15
01111	R ₁₅₅ R ₁₅₄ R ₁₅₃ R ₁₅₂ R ₁₅₁ R ₁₅₀	16
10000	R ₁₆₅ R ₁₆₄ R ₁₆₃ R ₁₆₂ R ₁₆₁ R ₁₆₀	17
10001	R ₁₇₅ R ₁₇₄ R ₁₇₃ R ₁₇₂ R ₁₇₁ R ₁₇₀	18
10010	R ₁₈₅ R ₁₈₄ R ₁₈₃ R ₁₈₂ R ₁₈₁ R ₁₈₀	19
10011	R ₁₉₅ R ₁₉₄ R ₁₉₃ R ₁₉₂ R ₁₉₁ R ₁₉₀	20
10100	R ₂₀₅ R ₂₀₄ R ₂₀₃ R ₂₀₂ R ₂₀₁ R ₂₀₀	21
10101	R ₂₁₅ R ₂₁₄ R ₂₁₃ R ₂₁₂ R ₂₁₁ R ₂₁₀	22
10110	R ₂₂₅ R ₂₂₄ R ₂₂₃ R ₂₂₂ R ₂₂₁ R ₂₂₀	23
10111	R ₂₃₅ R ₂₃₄ R ₂₃₃ R ₂₃₂ R ₂₃₁ R ₂₃₀	24
11000	R ₂₄₅ R ₂₄₄ R ₂₄₃ R ₂₄₂ R ₂₄₁ R ₂₄₀	25
11001	R ₂₅₅ R ₂₅₄ R ₂₅₃ R ₂₅₂ R ₂₅₁ R ₂₅₀	26
11010	R ₂₆₅ R ₂₆₄ R ₂₆₃ R ₂₆₂ R ₂₆₁ R ₂₆₀	27
11011	R ₂₇₅ R ₂₇₄ R ₂₇₃ R ₂₇₂ R ₂₇₁ R ₂₇₀	28
11100	R ₂₈₅ R ₂₈₄ R ₂₈₃ R ₂₈₂ R ₂₈₁ R ₂₈₀	29
11101	R ₂₉₅ R ₂₉₄ R ₂₉₃ R ₂₉₂ R ₂₉₁ R ₂₉₀	30
11110	R ₃₀₅ R ₃₀₄ R ₃₀₃ R ₃₀₂ R ₃₀₁ R ₃₀₀	31
11111	$R_{315}R_{314}R_{313}R_{312}R_{311}R_{310}$	32



G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
000000	G ₀₀₅ G ₀₀₄ G ₀₀₃ G ₀₀₂ G ₀₀₁ G ₀₀₀	33
000001	G ₀₁₅ G ₀₁₄ G ₀₁₃ G ₀₁₂ G ₀₁₁ G ₀₁₀	34
000010	G ₀₂₅ G ₀₂₄ G ₀₂₃ G ₀₂₂ G ₀₂₁ G ₀₂₀	35
000011	G ₀₃₅ G ₀₃₄ G ₀₃₃ G ₀₃₂ G ₀₃₁ G ₀₃₀	36
000100	G ₀₄₅ G ₀₄₄ G ₀₄₃ G ₀₄₂ G ₀₄₁ G ₀₄₀	37
000101	G ₀₅₅ G ₀₅₄ G ₀₅₃ G ₀₅₂ G ₀₅₁ G ₀₅₀	38
000110	G ₀₆₅ G ₀₆₄ G ₀₆₃ G ₀₆₂ G ₀₆₁ G ₀₆₀	39
000111	$G_{075}G_{074}G_{073}G_{072}G_{071}G_{070}$	40
001000	$G_{085}G_{084}G_{083}G_{082}G_{081}G_{080}$	41
001001	$G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}$	42
001010	G ₁₀₅ G ₁₀₄ G ₁₀₃ G ₁₀₂ G ₁₀₁ G ₁₀₀	43
001011	G ₁₁₅ G ₁₁₄ G ₁₁₃ G ₁₁₂ G ₁₁₁ G ₁₁₀	44
001100	G ₁₂₅ G ₁₂₄ G ₁₂₃ G ₁₂₂ G ₁₂₁ G ₁₂₀	45
001101	$G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}$	46
001110	G ₁₄₅ G ₁₄₄ G ₁₄₃ G ₁₄₂ G ₁₄₁ G ₁₄₀	47
001111	G ₁₅₅ G ₁₅₄ G ₁₅₃ G ₁₅₂ G ₁₅₁ G ₁₅₀	48
010000	G ₁₆₅ G ₁₆₄ G ₁₆₃ G ₁₆₂ G ₁₆₁ G ₁₆₀	49
010001	G ₁₇₅ G ₁₇₄ G ₁₇₃ G ₁₇₂ G ₁₇₁ G ₁₇₀	50
010010	G ₁₈₅ G ₁₈₄ G ₁₈₃ G ₁₈₂ G ₁₈₁ G ₁₈₀	51
010011	$G_{195} G_{194} G_{193} G_{192} G_{191} G_{190}$	52
010100	$G_{205} G_{204} G_{203} G_{202} G_{201} G_{200}$	53
010101	$G_{215}G_{214}G_{213}G_{212}G_{211}G_{210}$	54
010110	G ₂₂₅ G ₂₂₄ G ₂₂₃ G ₂₂₂ G ₂₂₁ G ₂₂₀	55
010111	G ₂₃₅ G ₂₃₄ G ₂₃₃ G ₂₃₂ G ₂₃₁ G ₂₃₀	56
011000	$G_{245}G_{244}G_{243}G_{242}G_{241}G_{240}$	57
011001	$G_{255} G_{254} G_{253} G_{252} G_{251} G_{250}$	58
011010	$G_{265} G_{264} G_{263} G_{262} G_{261} G_{260}$	59
011011	$G_{275} G_{274} G_{273} G_{272} G_{271} G_{270}$	60
011100	G ₂₈₅ G ₂₈₄ G ₂₈₃ G ₂₈₂ G ₂₈₁ G ₂₈₀	61
011101	G ₂₉₅ G ₂₉₄ G ₂₉₃ G ₂₉₂ G ₂₉₁ G ₂₉₀	62
011110	G ₃₀₅ G ₃₀₄ G ₃₀₃ G ₃₀₂ G ₃₀₁ G ₃₀₀	63
011111	G ₃₁₅ G ₃₁₄ G ₃₁₃ G ₃₁₂ G ₃₁₁ G ₃₁₀	64
100000	G ₃₂₅ G ₃₂₄ G ₃₂₃ G ₃₂₂ G ₃₂₁ G ₃₂₀	65
100001	$G_{335}G_{334}G_{333}G_{332}G_{331}G_{330}$	66



G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
100010	G ₃₄₅ G ₃₄₄ G ₃₄₃ G ₃₄₂ G ₃₄₁ G ₃₄₀	67
100011	G ₃₅₅ G ₃₅₄ G ₃₅₃ G ₃₅₂ G ₃₅₁ G ₃₅₀	68
100100	G ₃₆₅ G ₃₆₄ G ₃₆₃ G ₃₆₂ G ₃₆₁ G ₃₆₀	69
100101	G ₃₇₅ G ₃₇₄ G ₃₇₃ G ₃₇₂ G ₃₇₁ G ₃₇₀	70
100110	G ₃₈₅ G ₃₈₄ G ₃₈₃ G ₃₈₂ G ₃₈₁ G ₃₈₀	71
100111	G ₃₉₅ G ₃₉₄ G ₃₉₃ G ₃₉₂ G ₃₉₁ G ₃₉₀	72
101000	G ₄₀₅ G ₄₀₄ G ₄₀₃ G ₄₀₂ G ₄₀₁ G ₄₀₀	73
101001	G ₄₁₅ G ₄₁₄ G ₄₁₃ G ₄₁₂ G ₄₁₁ G ₄₁₀	74
101010	G ₄₂₅ G ₄₂₄ G ₄₂₃ G ₄₂₂ G ₄₂₁ G ₄₂₀	75
101011	$G_{435}G_{434}G_{433}G_{432}G_{431}G_{430}$	76
101100	G ₄₄₅ G ₄₄₄ G ₄₄₃ G ₄₄₂ G ₄₄₁ G ₄₄₀	77
101101	$G_{455} \ G_{454} \ G_{453} \ G_{452} \ G_{451} \ G_{450}$	78
101110	G ₄₆₅ G ₄₆₄ G ₄₆₃ G ₄₆₂ G ₄₆₁ G ₄₆₀	79
101111	G ₄₇₅ G ₄₇₄ G ₄₇₃ G ₄₇₂ G ₄₇₁ G ₄₇₀	80
110000	G ₄₈₅ G ₄₈₄ G ₄₈₃ G ₄₈₂ G ₄₈₁ G ₄₈₀	81
110001	G ₄₉₅ G ₄₉₄ G ₄₉₃ G ₄₉₂ G ₄₉₁ G ₄₉₀	82
110010	G ₅₀₅ G ₅₀₄ G ₅₀₃ G ₅₀₂ G ₅₀₁ G ₅₀₀	83
110011	$G_{515}G_{514}G_{513}G_{512}G_{511}G_{510}$	84
110100	$G_{525}G_{524}G_{523}G_{522}G_{521}G_{520}$	85
110101	$G_{535}G_{534}G_{533}G_{532}G_{531}G_{530}$	86
110110	G ₅₄₅ G ₅₄₄ G ₅₄₃ G ₅₄₂ G ₅₄₁ G ₅₄₀	87
110111	G ₅₅₅ G ₅₅₄ G ₅₅₃ G ₅₅₂ G ₅₅₁ G ₅₅₀	88
111000	$G_{565} G_{564} G_{563} G_{562} G_{561} G_{560}$	89
111001	G ₅₇₅ G ₅₇₄ G ₅₇₃ G ₅₇₂ G ₅₇₁ G ₅₇₀	90
111010	G ₅₈₅ G ₅₈₄ G ₅₈₃ G ₅₈₂ G ₅₈₁ G ₅₈₀	91
111011	$G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}$	92
111100	G ₆₀₅ G ₆₀₄ G ₆₀₃ G ₆₀₂ G ₆₀₁ G ₆₀₀	93
111101	$G_{615}G_{614}G_{613}G_{612}G_{611}G_{610}$	94
111110	G ₆₂₅ G ₆₂₄ G ₆₂₃ G ₆₂₂ G ₆₂₁ G ₆₂₀	95
111111	G ₆₃₅ G ₆₃₄ G ₆₃₃ G ₆₃₂ G ₆₃₁ G ₆₃₀	96



B input (5-bit) 16-bit/pixel -mode 65,536 colors	B output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	B ₀₀₅ B ₀₀₄ B ₀₀₃ B ₀₀₂ B ₀₀₁ B ₀₀₀	97
00001	B ₀₁₅ B ₀₁₄ B ₀₁₃ B ₀₁₂ B ₀₁₁ B ₀₁₀	98
00010	B ₀₂₅ B ₀₂₄ B ₀₂₃ B ₀₂₂ B ₀₂₁ B ₀₂₀	99
00011	B ₀₃₅ B ₀₃₄ B ₀₃₃ B ₀₃₂ B ₀₃₁ B ₀₃₀	100
00100	B ₀₄₅ B ₀₄₄ B ₀₄₃ B ₀₄₂ B ₀₄₁ B ₀₄₀	101
00101	B ₀₅₅ B ₀₅₄ B ₀₅₃ B ₀₅₂ B ₀₅₁ B ₀₅₀	102
00110	B ₀₆₅ B ₀₆₄ B ₀₆₃ B ₀₆₂ B ₀₆₁ B ₀₆₀	103
00111	B ₀₇₅ B ₀₇₄ B ₀₇₃ B ₀₇₂ B ₀₇₁ B ₀₇₀	104
01000	B ₀₈₅ B ₀₈₄ B ₀₈₃ B ₀₈₂ B ₀₈₁ B ₀₈₀	105
01001	B ₀₉₅ B ₀₉₄ B ₀₉₃ B ₀₉₂ B ₀₉₁ B ₀₉₀	106
01010	B ₁₀₅ B ₁₀₄ B ₁₀₃ B ₁₀₂ B ₁₀₁ B ₁₀₀	107
01011	B ₁₁₅ B ₁₁₄ B ₁₁₃ B ₁₁₂ B ₁₁₁ B ₁₁₀	108
01100	B ₁₂₅ B ₁₂₄ B ₁₂₃ B ₁₂₂ B ₁₂₁ B ₁₂₀	109
01101	B ₁₃₅ B ₁₃₄ B ₁₃₃ B ₁₃₂ B ₁₃₁ B ₁₃₀	110
01110	B ₁₄₅ B ₁₄₄ B ₁₄₃ B ₁₄₂ B ₁₄₁ B ₁₄₀	111
01111	B ₁₅₅ B ₁₅₄ B ₁₅₃ B ₁₅₂ B ₁₅₁ B ₁₅₀	112
10000	B ₁₆₅ B ₁₆₄ B ₁₆₃ B ₁₆₂ B ₁₆₁ B ₁₆₀	113
10001	B ₁₇₅ B ₁₇₄ B ₁₇₃ B ₁₇₂ B ₁₇₁ B ₁₇₀	114
10010	B ₁₈₅ B ₁₈₄ B ₁₈₃ B ₁₈₂ B ₁₈₁ B ₁₈₀	115
10011	B ₁₉₅ B ₁₉₄ B ₁₉₃ B ₁₉₂ B ₁₉₁ B ₁₉₀	116
10100	B ₂₀₅ B ₂₀₄ B ₂₀₃ B ₂₀₂ B ₂₀₁ B ₂₀₀	117
10101	B ₂₁₅ B ₂₁₄ B ₂₁₃ B ₂₁₂ B ₂₁₁ B ₂₁₀	118
10110	B ₂₂₅ B ₂₂₄ B ₂₂₃ B ₂₂₂ B ₂₂₁ B ₂₂₀	119
10111	B ₂₃₅ B ₂₃₄ B ₂₃₃ B ₂₃₂ B ₂₃₁ B ₂₃₀	120
11000	B ₂₄₅ B ₂₄₄ B ₂₄₃ B ₂₄₂ B ₂₄₁ B ₂₄₀	121
11001	B ₂₅₅ B ₂₅₄ B ₂₅₃ B ₂₅₂ B ₂₅₁ B ₂₅₀	122
11010	B ₂₆₅ B ₂₆₄ B ₂₆₃ B ₂₆₂ B ₂₆₁ B ₂₆₀	123
11011	B ₂₇₅ B ₂₇₄ B ₂₇₃ B ₂₇₂ B ₂₇₁ B ₂₇₀	124
11100	B ₂₈₅ B ₂₈₄ B ₂₈₃ B ₂₈₂ B ₂₈₁ B ₂₈₀	125
11101	B ₂₉₅ B ₂₉₄ B ₂₉₃ B ₂₉₂ B ₂₉₁ B ₂₉₀	126
11110	B ₃₀₅ B ₃₀₄ B ₃₀₃ B ₃₀₂ B ₃₀₁ B ₃₀₀	127
11111	B ₃₁₅ B ₃₁₄ B ₃₁₃ B ₃₁₂ B ₃₁₁ B ₃₁₀	128





7.5. Display Data RAM (DDRAM)

ILI9341 has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.



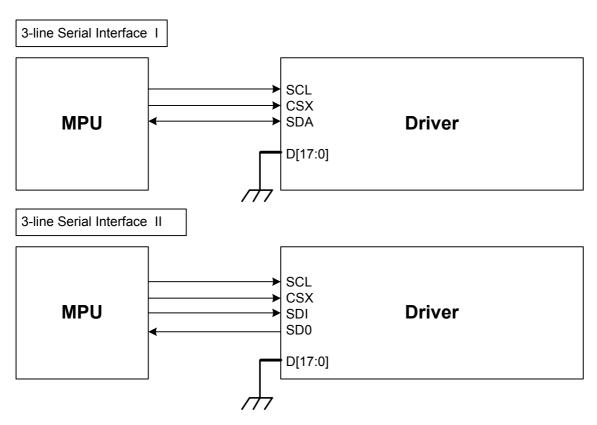


7.6. Display Data Format

ILI9341 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080- I /8080- II series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

7.6.1. 3-line Serial Interface

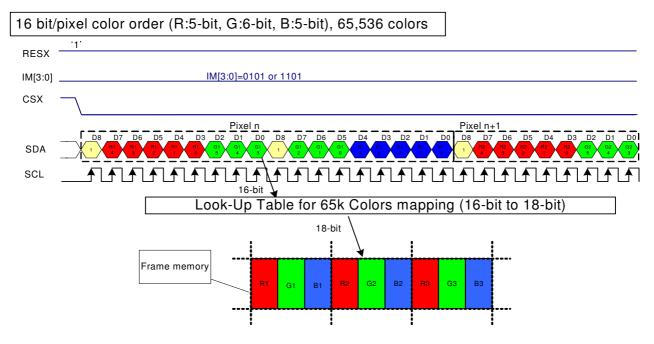
The 3-line/9-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0101" for serial interface I or IM [3:0] to "1101" for serial interface II. The shown figure is the example of 3-line SPI interface.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

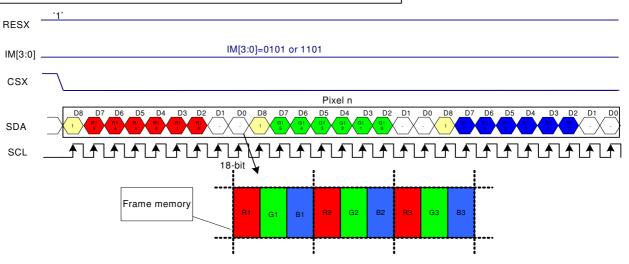
- -65k colors, RGB 5, 6, 5 -bits input
- -262k colors, RGB 6, 6, 6 -bits input.





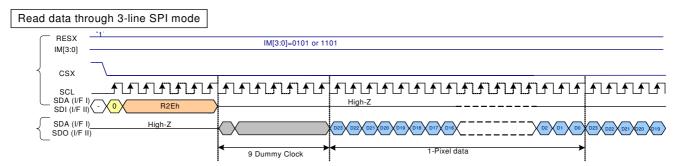
- Note 1: The pixel data with 16-bit color depth information.
- Note 2: The most significant bits are: Rx4, Gx5 and Bx4.
- Note 3: The least significant bits are: Rx0, Gx0 and Bx0.
- Note 4: '-'= Don't care -Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



- Note 1: The pixel data with 18-bit color depth information.
- Note 2: The most significant bits are: Rx5, Gx5 and Bx5.
- Note 3: The least significant bits are : Rx0, Gx0 and Bx0.
- Note 4: '-'= Don't care Can be set "0" or "1".





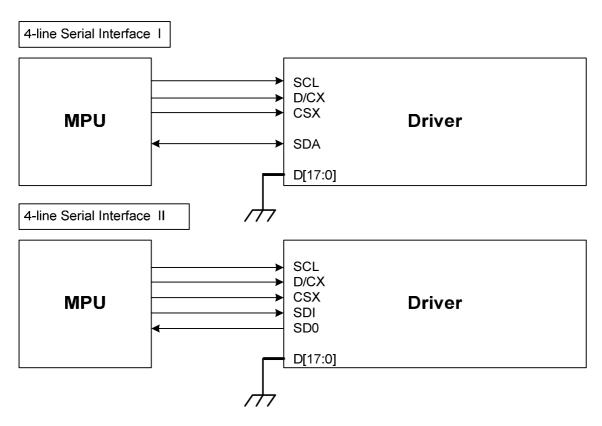
Note 1: '-'= Don't care -Can be set "0" or "1".





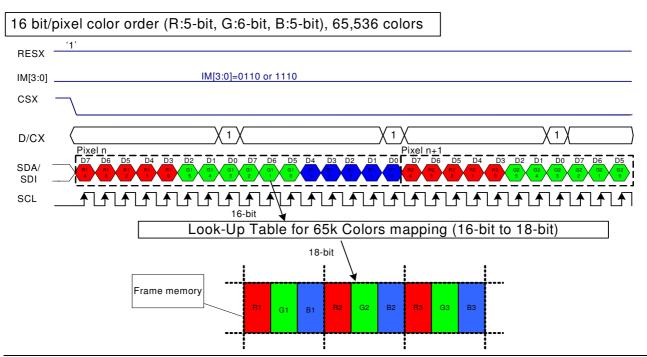
7.6.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0110" for serial interface I or IM [3:0] to "1110" for serial interface II. The shown figure is the example of 4-line SPI interface.



In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

- -65k colors, RGB 5, 6, 5 -bits input.
- -262k colors, RGB 6, 6, 6 -bits input.



The information contained herein is the exclusive property of ILI Technology Corp. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of ILI Technology Corp.





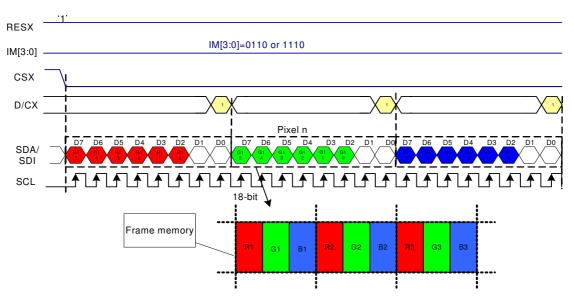
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care -Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



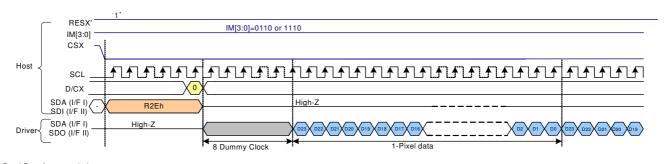
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care -Can be set "0" or "1".

Read data through 4-line SPI mode





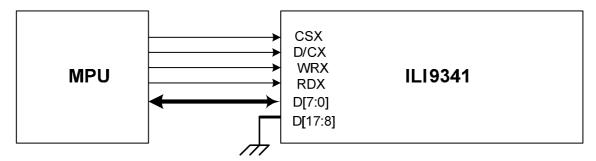
Note 1: '-'= Don't care - Can be set "0" or "1".





7.6.3. 8-bit Parallel MCU Interface

The 8080- I system 8-bit parallel bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0000". The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	 238R0		239R0	
D2	C2	0G5	0B2	1G5	1B2	 238G5		239G5	
D1	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	 238G3		239G3	

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

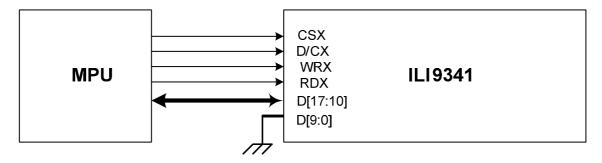
One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D7	C7	0R5	0G5	0B5	 239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	 239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	 239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	 239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	 239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	 239R0	239G0	239B0
D1	C1						
D0	C0						





The 8080- Π system 8-bit parallel bus interface of ILl9341 can be used by settings as IM [3:0] ="1001". The following shown figure is the example of interface with 8080- Π MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D13	C3	0R0		1R0	1B3	 238R0		239R0	239B3
D12	C2	0G5		1G5	1B2	 238G5		239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	 238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

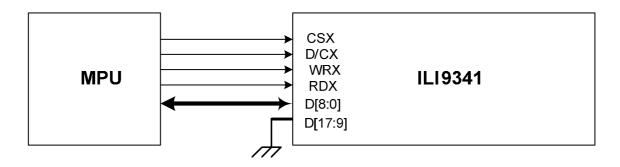
Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D17	C7	0R5	0G5	0B5	 239R5	239G5	
D16	C6	0R4	0G4	0B4	 239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	 239R3	239G3	
D14	C4	0R2	0G2	0B2	 239R2	239G2	
D13	C3	0R1	0G1	0B1	 239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	 239R0	239G0	
D11	C1						
D10	C0						





7.6.4. 9-bit Parallel MCU Interface

The 8080- I system 9-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM [3:0] to "0010". The following shown figure is the example of interface with 8080- I MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D8									
D7	C7	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D3	C3	0R0		1R0	1B3	 238R0		239R0	
D2	C2	0G5		1G5	1B2	 238G5		239G5	
D1	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D0	C0	0G3		1G3	1B0	 238G3		239G3	

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	4	 478	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D8		0R5	0G2	1R5	1G2	238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	 238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	 238R3	238G0	239R3	239G0
D5	C5	0R2		1R2	1B5	 238R2		239R2	
D4	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D3	C3	0R0		1R0	1B3	 238R0		239R0	
D2	C2	0G5		1G5	1B2	 238G5		239G5	
D1	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	 238G3	238B0	239G3	239B0

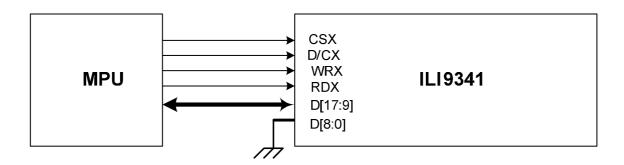




MDT[1:0]="01"

Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D8							
D7	C7	0R5	0G5		 239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	 239R4	239G4	239B4
D5	C5	0R3	0G3		 239R3	239G3	239B3
D4	C4	0R2	0G2		 239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	 239R1	239G1	239B1
D2	C2	0R0	0G0		 239R0	239G0	239B0
D1	C1						
D0	C0						

The 8080- Π system 9-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM [3:0] to "1011". The following shown figure is the example of interface with 8080- Π MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D17	C7								
D16	C6	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D15	C5	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D14	C4	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D13	C3	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D12	C2	0R0		1R0	1B3	 238R0		239R0	
D11	C1	0G5		1G5	1B2	 238G5		239G5	
D10	C0	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	 238G3	238B0	239G3	239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	4	 478	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D17	C7	0R5	0G2	1R5	1G2	238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	 238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	 238R3	238G0	239R3	239G0
D14	C4	0R2		1R2	1B5	 238R2		239R2	
D13	C3	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D12	C2	0R0		1R0	1B3	 238R0		239R0	
D11	C1	0G5		1G5	1B2	 238G5		239G5	
D10	C0	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D9		0G3		1G3	1B0	 238G3		239G3	

MDT[1:0]="01"

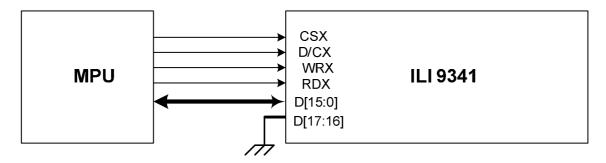
Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D17	C7						
D16	C6	0R5	0G5		 239R5	239G5	
D15	C5	0R4	0G4	0B4	 239R4	239G4	239B4
D14	C4	0R3	0G3		 239R3	239G3	
D13	C3	0R2	0G2		 239R2	239G2	
D12	C2	0R1	0G1	0B1	 239R1	239G1	239B1
D11	C1	0R0	0G0		 239R0	239G0	
D10	C0						
D9							





7.6.5. 16-bit Parallel MCU Interface

The 8080- I system 16-bit parallel bus interface of ILl9341 can be selected by setting hardware pin IM[3:0] to "0001". The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

. ,	•	, ,		•		3	
Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D15		0R4	1R4	2R4	 237R4	238R4	239R4
D14		0R3	1R3	2R3	 237R3	238R3	239R3
D13		0R2	1R2	2R2	 237R2	238R2	239R2
D12		0R1	1R1	2R1	 237R1	238R1	239R1
D11		0R0	1R0	2R0	 237R0	238R0	239R0
D10		0G5	1G5	2G5	 237G5	238G5	239G5
D9		0G4	1G4	2G4	 237G4	238G4	239G4
D8		0G3	1G3	2G3	 237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	237B4	238B4	239B4
D3	C3	0B3	1B3				
D2	C2	0B2	1B2				
D1	C1	0B1	1B1	2B1	237B1	238B1	239B1
D0	C0	0B0	1B0		 237B0	238B0	239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	 358	359	360
D/CX	0	1	1	1	 1	1	1
D15		0R5		1G5	 238R5		239G5
D14		0R4	0B4	1G4	 238R4	238B4	239G4
D13		0R3		1G3	 238R3		239G3
D12		0R2		1G2	 238R2		239G2
D11		0R1	0B1	1G1	 238R1	238B1	239G1
D10		0R0		1G0	 238R0		239G0
D9							
D8							
D7	C7	0G5	1R5	1B5	 238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	 238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	 238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	 238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	 238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	 238G0	239R0	239B0
D1	C1						
D0	C0						

MDT[1:0]="01"

[] -	_								
Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D15		0R5		1R5	1B5	 238R5		239R5	239B5
D14		0R4	0B4	1R4	1B4	 238R4	238B4	239R4	239B4
D13		0R3		1R3	1B3	 238R3		239R3	239B3
D12		0R2		1R2	1B2	 238R2		239R2	239B2
D11		0R1	0B1	1R1	1B1	 238R1	238B1	239R1	239B1
D10		0R0		1R0	1B0	 238R0		239R0	239B0
D9									
D8									
D7	C7	0G5		1G5		 238G5		239G5	
D6	C6	0G4		1G4		 238G4		239G4	
D5	C5	0G3		1G3		 238G3		239G3	
D4	C4	0G2		1G2		 238G2		239G2	
D3	C3	0G1		1G1		 238G1		239G1	
D2	C2	0G0		1G0		 238G0		239G0	
D1	C1								
D0	C0								





MDT[1:0]="10"

Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D15		0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D14		0R4		1R4	1B0	 238R4		239R4	239B0
D13		0R3		1R3		 238R3		239R3	
D12		0R2		1R2		 238R2		239R2	
D11		0R1		1R1		 238R1		239R1	
D10		0R0		1R0		 238R0		239R0	
D9		0G5		1G5		 238G5		239G5	
D8		0G4		1G4		 238G4		239G4	
D7	C7	0G3		1G3		 238G3		239G3	
D6	C6	0G2		1G2		 238G2		239G2	
D5	C5	0G1		1G1		 238G1		239G1	
D4	C4	0G0		1G0		 238G0		239G0	
D3	C3			1B5				239B5	
D2	C2	0B4		1B4		 238B4		239B4	
D1	C1			1B3				239B3	
D0	C0			1B2				239B2	

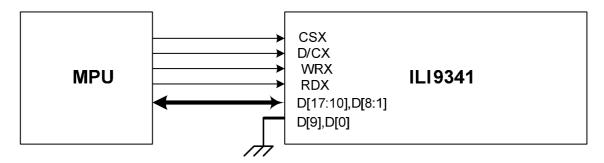
MDT[1:0]="11"

Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D15			0R3		1R3		238R3		239R3
D14			0R2		1R2		238R2		239R2
D13			0R1		1R1		238R1		239R1
D12			0R0		1R0		238R0		239R0
D11			0G5		1G5		238G5		239G5
D10			0G4		1G4		238G4		239G4
D9			0G3		1G3		238G3		239G3
D8			0G2		1G2		238G2		239G2
D7	C7		0G1		1G1		238G1		239G1
D6	C6		0G0		1G0		238G0		239G0
D5	C5				1B5				239B5
D4	C4		0B4		1B4		238B4		239B4
D3	C3				1B3				239B3
D2	C2				1B2				239B2
D1	C1	0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	 238R4	238B0	239R4	239B0





The 8080- Π system 16-bit parallel bus interface of ILI9341 can be selected by settings IM [3:0] ="1000". The following shown figure is the example of interface with 8080- Π MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17		0R4	1R4	2R4	 237R4	238R4	239R4
D16		0R3	1R3	2R3	 237R3	238R3	239R3
D15		0R2	1R2	2R2	 237R2	238R2	239R2
D14		0R1	1R1	2R1	 237R1	238R1	239R1
D13		0R0	1R0	2R0	 237R0	238R0	239R0
D12		0G5	1G5	2G5	 237G5	238G5	239G5
D11		0G4	1G4	2G4	 237G4	238G4	239G4
D10		0G3	1G3	2G3	 237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	237B4	238B4	239B4
D4	C3	0B3	1B3				239B3
D3	C2	0B2	1B2				239B2
D2	C1	0B1	1B1	2B1	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	 237B0	238B0	239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	 358	359	360
D/CX	0	1	1	1	 1	1	1
D17		0R5		1G5	 238R5		239G5
D16		0R4	0B4	1G4	 238R4	238B4	239G4
D15		0R3		1G3	 238R3		239G3
D14		0R2		1G2	 238R2		239G2
D13		0R1	0B1	1G1	 238R1	238B1	239G1
D12		0R0		1G0	 238R0		239G0
D11							
D10							
D8	C7	0G5	1R5	1B5	 238G5	239R5	239B5
D7	C6	0G4	1R4	1B4	 238G4	239R4	239B4
D6	C5	0G3	1R3	1B3	 238G3	239R3	239B3
D5	C4	0G2	1R2	1B2	 238G2	239R2	239B2
D4	C3	0G1	1R1	1B1	 238G1	239R1	239B1
D3	C2	0G0	1R0	1B0	 238G0	239R0	239B0
D2	C1						
D1	C0						

MDT[1:0]="01"

-[o. ·] · d.									
Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D17		0R5		1R5	1B5	 238R5		239R5	239B5
D16		0R4	0B4	1R4	1B4	 238R4	238B4	239R4	239B4
D15		0R3		1R3	1B3	 238R3		239R3	239B3
D14		0R2		1R2	1B2	 238R2		239R2	239B2
D13		0R1	0B1	1R1	1B1	 238R1	238B1	239R1	239B1
D12		0R0		1R0	1B0	 238R0		239R0	239B0
D11									
D10									
D8	C7	0G5		1G5		 238G5		239G5	
D7	C6	0G4		1G4		 238G4		239G4	
D6	C5	0G3		1G3		 238G3		239G3	
D5	C4	0G2		1G2		 238G2		239G2	
D4	C3	0G1		1G1		 238G1		239G1	
D3	C2	0G0		1G0		 238G0		239G0	
D2	C1				·				
D1	C0								





MDT[1:0]="10"

Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D17		0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D16		0R4		1R4	1B0	 238R4		239R4	239B0
D15		0R3		1R3		 238R3		239R3	
D14		0R2		1R2		 238R2		239R2	
D13		0R1		1R1		 238R1		239R1	
D12		0R0		1R0		 238R0		239R0	
D11		0G5		1G5		 238G5		239G5	
D10		0G4		1G4		 238G4		239G4	
D8	C7	0G3		1G3		 238G3		239G3	
D7	C6	0G2		1G2		 238G2		239G2	
D6	C5	0G1		1G1		 238G1		239G1	
D5	C4	0G0		1G0		 238G0		239G0	
D4	C3			1B5				239B5	
D3	C2	0B4		1B4		 238B4		239B4	
D2	C1			1B3				239B3	
D1	C0			1B2				239B2	

MDT[1:0]="11"

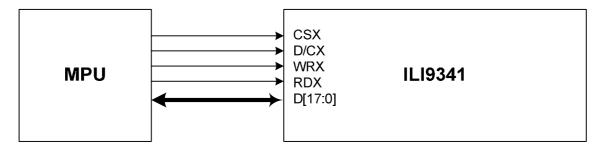
Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D17			0R3		1R3		238R3		239R3
D16			0R2		1R2		238R2		239R2
D15			0R1		1R1		238R1		239R1
D14			0R0		1R0		238R0		239R0
D13			0G5		1G5		238G5		239G5
D12			0G4		1G4		238G4		239G4
D11			0G3		1G3		238G3		239G3
D10			0G2		1G2		238G2		239G2
D8	C7		0G1		1G1		238G1		239G1
D7	C6		0G0		1G0		238G0		239G0
D6	C5				1B5				
D5	C4		0B4		1B4		238B4		239B4
D4	C3				1B3				
D3	C2				1B2				
D2	C1	0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	 238R4	238B0	239R4	239B0





7.6.6. 18-bit Parallel MCU Interface

The 8080- I system 18-bit parallel bus interface of ILl9341 can be selected by setting hardware pin IM[3:0] to "0011". The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

		· · · ·			 		
Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17							
D16							
D15		0R4	1R4	2R4	 237R4	238R4	239R4
D14		0R3	1R3	2R3	 237R3	238R3	239R3
D13		0R2	1R2	2R2	 237R2	238R2	239R2
D12		0R1	1R1	2R1	 237R1	238R1	239R1
D11		0R0	1R0	2R0	 237R0	238R0	239R0
D10		0G5	1G5	2G5	 237G5	238G5	239G5
D9		0G4	1G4	2G4	 237G4	238G4	239G4
D8		0G3	1G3	2G3	 237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	237B4	238B4	239B4
D3	C3		1B3				
D2	C2		1B2				
D1	C1	0B1	1B1	2B1	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	 237B0	238B0	239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

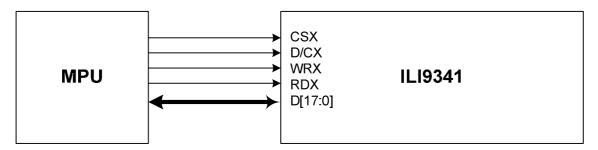
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17		0R5	1R5	2R5	 237R5	238R5	239R5
D16		0R4	1R4	2R4	 237R4	238R4	239R4
D15		0R3	1R3	2R3	 237R3	238R3	239R3
D14		0R2	1R2	2R2	 237R2	238R2	239R2
D13		0R1	1R1	2R1	 237R1	238R1	239R1
D12		0R0	1R0	2R0	 237R0	238R0	239R0
D11		0G5	1G5	2G5	 237G5	238G5	239G5
D10		0G4	1G4	2G4	 237G4	238G4	239G4
D9		0G3	1G3	2G3	 237G3	238G3	239G3
D8		0G2	1G2	2G2	 237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	 237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	 237G0	238G0	239G0
D5	C5		1B5				239B5
D4	C4	0B4	1B4	2B4	237B4	238B4	239B4
D3	C3		1B3				239B3
D2	C2		1B2				239B2
D1	C1	0B1	1B1	2B1	237B1	238B1	239B1
D0	C0		1B0				239B0





The 8080- Π system 18-bit parallel bus interface mode can be selected by settings IM [3:0] ="1010". The following shown figure is the example of interface with 8080- Π MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17							
D16							
D15		0R4	1R4	2R4	 237R4	238R4	239R4
D14		0R3	1R3	2R3	 237R3	238R3	239R3
D13		0R2	1R2	2R2	 237R2	238R2	239R2
D12		0R1	1R1	2R1	 237R1	238R1	239R1
D11		0R0	1R0	2R0	 237R0	238R0	239R0
D10		0G5	1G5	2G5	 237G5	238G5	239G5
D9		0G4	1G4	2G4	 237G4	238G4	239G4
D8	C7	0G3	1G3	2G3	 237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	 237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	 237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	 237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	237B4	238B4	239B4
D3	C2		1B3				239B3
D2	C1		1B2				239B2
D1	C0	0B1	1B1	2B1	237B1	238B1	239B1
D0		0B0	1B0	2B0	 237B0	238B0	239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17		0R5	1R5	2R5	 237R5	238R5	239R5
D16		0R4	1R4	2R4	 237R4	238R4	239R4
D15		0R3	1R3	2R3	 237R3	238R3	239R3
D14		0R2	1R2	2R2	 237R2	238R2	239R2
D13		0R1	1R1	2R1	 237R1	238R1	239R1
D12		0R0	1R0	2R0	 237R0	238R0	239R0
D11		0G5	1G5	2G5	 237G5	238G5	239G5
D10		0G4	1G4	2G4	 237G4	238G4	239G4
D9		0G3	1G3	2G3	 237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D5	C4		1B5				239B5
D4	C3	0B4	1B4	2B4	237B4	238B4	239B4
D3	C2		1B3				239B3
D2	C1		1B2				239B2
D1	C0	0B1	1B1	2B1	237B1	238B1	239B1
D0			1B0				239B0

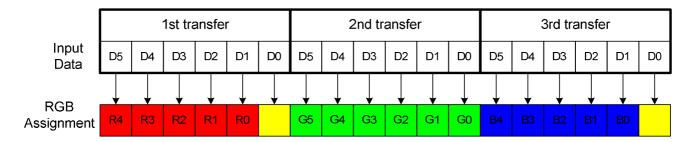




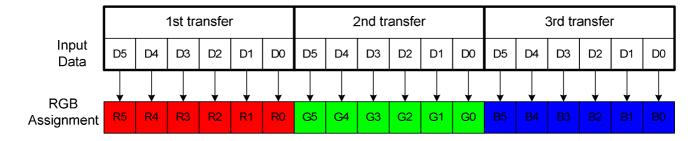
7.6.7. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the DPI [2:0] bit to "110". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to "10". The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)



262K color: 18-bit/pixel (RGB 6-6-6 bits input)



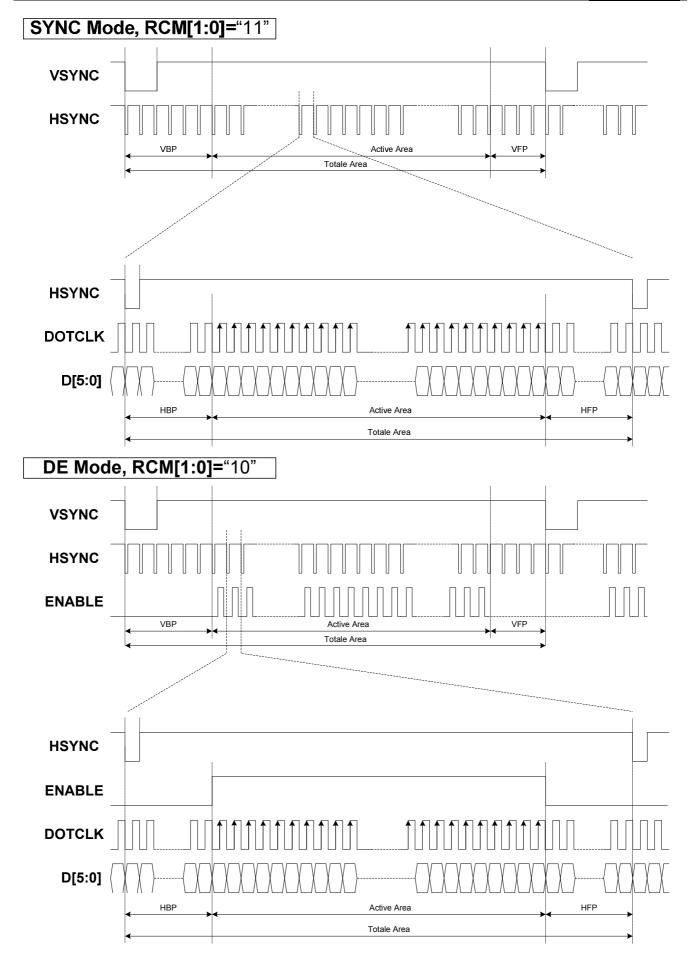
ILI9341 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.





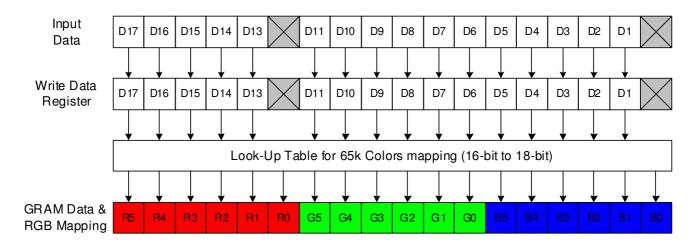






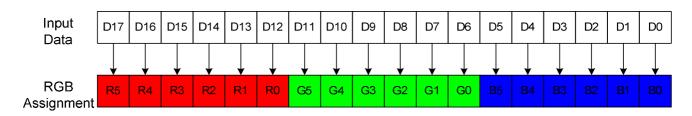
7.6.8. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to "101". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [17:13] & D [11:1]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [17:13] and D [11:1] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.



7.6.9. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to "110". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to "10". The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.







8. Command

8.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
No Operation	0	1	1	XX	0	0	0	0	0	0	0	0	00h
Software Reset	0	1	1	XX	0	0	0	0	0	0	0	1	01h
	0	1	1	XX	0	0	0	0	0	1	0	0	04h
	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Χ	XX
Read Display Identification	1	<u>†</u>	1	XX		•	•	ID1 [•		J.	XX
Information	1	1	1	XX				ID2 [XX
	1	1	1	XX				ID3 [XX
	0	1	1	XX	0	0	0	0	1	0	0	1	09h
	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
	1	<u> </u>	1	XX		1		[31:25]	1		1	Х	00
Read Display Status	1	<u> </u>	1	XX	Х		D [22:20			D [1	9:16]		61
	1	<u> </u>	1	XX	X	Х	X	Х	Х		D [10:8]		00
	1	<u> </u>	1	XX		D [7:5]		X	X	Х	X	Х	00
	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
Read Display Power Mode	1	<u> </u>	1	XX	X	X	X	X	X	X	Х	X	XX
rioda Biopidy i owoi iliodo	1	<u> </u>	1	XX			D [7				0	0	08
	0	1	·	XX	0	0	0	0	1	0	1	1	0Bh
Read Display MADCTL	1	<u>'</u>	1	XX	X	X	X	X	X	X	X	X	XX
ricad Display WADOTE	1	<u> </u>	1	XX			D [7	•			0	0	00
	0	1		XX	0	0	0	0	1	1	0	0	0Ch
Read Display Pixel Format	1	<u> </u>	1	XX	X	X	X	X	X	X	X	X	XX
nead Display Fixer Format	1	<u> </u>	1	XX	RIM			•	X		DBI [2:0]		06
			1 ↑				DPI [2:0]						0Dh
Dood Dioploy Image Formet	0	1		XX	0	0	0	0	1	1	0 X	1	
Read Display Image Format	1	↑ ↑	1	XX	X	X	X	X	X	Х		Х	XX
	1		1	XX		X	X	X	X		D [2:0]	0	00
Dood Disaless Cissed Mode	0	1	1	XX	0	0	0	0	1	1	1	0	0Eh
Read Display Signal Mode	1	1	1	XX	Х	Х	X	X	Х	Х	X	X	XX
	1	1	1	XX	_		D [7				0	0	00
Read Display Self-Diagnostic	0	1	1	XX	0	0	0	0	1	1	1	1	0Fh
Result	1	1	1	XX	X	X	X	X	X	X	X	X	XX
	1	1	1	XX	D [7	Γ.	X	X	X	X	X	X	00
Enter Sleep Mode	0	1	1	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	1	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	1	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	1	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	1	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	1	XX	0	0	1	0	0	0	0	1	21h
Gamma Set	0	1	1	XX	0	0	1	0	0	1	1	0	26h
	1	1	1	XX	_			GC [1 _	1 _	_	01
Display OFF	0	1	1	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	1	XX	0	0	1	0	1	0	0	1	29h
	0	1	1	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	1	XX				SC [1					XX
Column Address Set	1	1	1	XX				SC [XX
	1	1	1	XX				EC [1					XX
	1	1	1	XX		1	1	EC [ı			XX
	0	1	1	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	1	XX				SP [1					XX
Page Address Set	1	1	1	XX				SP [XX
	1	1	1	XX				EP [1					XX
	1	1	1	XX				EP [7:0]				XX





					1				1	ı	1		
Memory Write	0	1		XX	0	0	1	0	1	1	0	0	2Ch
•	1	1		207	1 .			0 [17:0]			1 _	· .	XX
	0	1	1	XX	0	0	1	0	1	1	0	1	2DI
	1	1	1	XX						00 [5:0]			XX
	11	1	1	XX						nn [5:0]			XX
	1	1	1	XX						31 [5:0]			XX
Color SET	11	1	1	XX		1				00 [5:0]			XX
	11	1	1	XX		1				nn [5:0]			XX
	1	1	1	XX						64 [5:0]			XX
	1	1	1	XX						00 [5:0]			XX
	1	1	1	XX						nn [5:0]			XX
	1	1	1	XX		l			В	31 [5:0]	1		XX
	0	1	1	XX	0	0	1	0	1	1	1	0	2Eh
Memory Read	1	1	1	XX	Χ	X	Χ	Х	Х	Χ	X	X	XX
	1	1	1		1	1		[17:0]		1	1		XX
	0	1	1	XX	0	0	1	1	0	0	0	0	30h
	1	1	1	XX					R [15:8]				00
Partial Area	1	1	1	XX				S	R [7:0]				00
	1	1	1	XX				E	R [15:8]				01
	1	1	1	XX		ı	ı	E	R [7:0]	ı	T		3F
	0	1	1	XX	0	0	1	1	0	0	1	1	33h
	11	1	1	XX					A [15:8]				00
	11	1	1	XX					FA [7:0]				00
Vertical Scrolling Definition	1	1	1	XX				VS	A [15:8]				01
	1	1	1	XX					SA [7:0]				40
	1	1	1	XX					A [15:8]				00
	1	1	1	XX		Г	Г	В	FA [7:0]	Г	1	1	00
Tearing Effect Line OFF	0	1	1	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	1	XX	0	0	1	1	0	1	0	1	35h
roaming Emock Emilio Ort	1	1	1	XX	Х	Х	Χ	Χ	Х	Χ	Х	М	00
Memory Access Control	0	1	1	XX	0	0	1	1	0	1	1	0	36h
Memory Addeds Control	1	1	1	XX	MY	MX	MV	ML	BGR	MH	X	Х	00
	0	1	1	XX	0	0	1	1	0	1	1	1	37h
Vertical Scrolling Start Address	1	1	1	XX				VS	P [15:8]				00
	11	1	1	XX		ı	ı	V:	SP [7:0]	ı	T		00
Idle Mode OFF	0	1	1	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	1	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	1	XX	0	0	1	1	1	0	1	0	3Ah
- morr ormat oot	1	1	1	XX	Х		DPI [2:0		Х		DBI [2:0		66
Write Memory Continue	0	1	1	XX	0	0	1	1	1	1	0	0	3Cr
Trine incincity commission	1	1	1		ı	ı		[17:0]		ı	1		XX
	0	1	1	XX	0	0	1	1	1	1	1	0	3Eh
Read Memory Continue	1	1	1	XX	Χ	X	Χ	Χ	X	Χ	Χ	Х	XX
	1	1	1		ı	ı		[17:0]		ı	1		XX
	0	1	1	XX	0	1	0	0	0	1	0	0	44h
Set Tear Scanline	1	1	1	XX	Х	Χ	Χ	Х	X	Χ	Χ	STS [8]	00
	1	1	1	XX		I	l		TS [7:0]	l	1	1	00
	0	1	1	XX	0	1	0	0	0	1	0	1	45h
Get Scanline	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	X	XX
Got Godrini	1	1	1	XX	Х	Χ	Χ	Χ	Χ	Χ	GT	S [9:8]	00
	1	1	1	XX		ı	ı	G	TS [7:0]	ı	_		00
Write Display Brightness	0	1	1	XX	0	1	0	1	0	0	0	1	51h
TTITLE DISPIRED DINGITHESS	1	1	1	XX				D	BV [7:0]				00





	0	1	1	XX	0	1	0	1	0	0	1	0	52h
Read Display Brightness	1	1	1	XX	Х	Х	Х	Χ	Х	Х	Х	Х	XX
	1	1	1	XX				DBV	' [7:0]				00
Write CTDL Display	0	1	1	XX	0	1	0	1	0	0	1	1	53h
Write CTRL Display	1	1	↑	XX	Х	Χ	BCTRL	Χ	DD	BL	Х	Χ	00
	0	1	1	XX	0	1	0	1	0	1	0	0	54h
Read CTRL Display	1	1	1	XX	Χ	Χ	Х	Χ	X	Х	X	Χ	XX
	1	1	1	XX	Х	Х	BCTRL	Х	DD	BL	Х	Χ	00
Write Content Adaptive	0	1	1	XX	0	1	0	1	0	1	0	1	55h
Brightness Control	1	1	1	XX	Х	Χ	Х	Χ	Х	Х	0 [1:0]	00
Read Content Adaptive	0	1	1	XX	0	1	0	1	0	1	1	0	56h
Brightness Control	1	1	1	XX	Х	Χ	Х	Χ	Х	Х	Х	Х	XX
2.19.11.1000 0011.101	1	1	1	XX	Χ	Х	Х	Χ	Х	Х	0 [1:0]	00
Write CABC Minimum	0	1	1	XX	0	1	0	1	1	1	1	0	5Eh
Brightness	1	1	1	XX				CME	3 [7:0]				00
Read CABC Minimum	0	1	1	XX	0	1	0	1	0	1	1	1	5Fh
Brightness	1	1	1	XX	Х	Χ	X	Χ	Х	Х	X	Χ	XX
<u> </u>	1	1	1	XX				CME	3 [7:0]				00
	0	1	1	XX	1	1	0	1	1	0	1	0	DAh
Read ID1	1	1	1	XX	Х	Χ	X	Χ	X	X	X	Χ	XX
	1	1	1	XX			Modu	ıle's Ma	nufactur	e [7:0]			XX
	0	1	1	XX	1	1	0	1	1	0	1	1	DBh
Read ID2	1	1	1	XX	Х	X	Χ	X	Х	X	Χ	Χ	XX
	1	1	1	XX			LCD Mo	dule / D	river Ver	sion [7:0)]		XX
	0	1	1	XX	1	1	0	1	1	1	0	0	DCh
Read ID3	1	1	1	XX	Х	Χ	Χ	Χ	Χ	Χ	Χ	Χ	XX
	1	1	1	XX			LCD I	Module /	Driver I	D [7:0]			XX

	T	T T	T T						T			1	
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	He
RGB Interface	0	1	1	XX	1	0	1	1	0	0	0	0	В0
Signal Control	1	1	↑	XX	ByPass_MODE	RCM	[1:0]	Χ	VSPL	HSPL	DPL	EPL	40
France Combrel	0	1	↑	XX	1	0	1	1	0	0	0	1	B1
Frame Control	1	1	↑	XX	X	Χ	Χ	Χ	Х	Х	DIVA	[1:0]	00
(In Normal Mode)	1	1	↑	XX	X	Χ	Χ		R	TNA [4:0	0]		16
F	0	1	↑	XX	1	0	1	1	0	0	1	0	B2
Frame Control	1	1	↑	XX	X	Χ	Χ	Χ	Х	Х	DIVE	8 [1:0]	0
(In Idle Mode)	1	1	↑	XX	X	Χ	Χ		R	TNB [4:0	0]		1
F	0	1	↑	XX	1	0	1	1	0	0	1	1	ВЗ
Frame Control	1	1	↑	XX	Х	Χ	Χ	Χ	Х	Х	DIVC	[1:0]	0
(In Partial Mode)	1	1	↑	XX	Х	Χ	Χ		R	TNC [4:0	0]		1
Diamles Insuranian Control	0	1	↑	XX	1	0	1	1	0	1	0	0	Β4
Display Inversion Control	1	1	↑	XX	Х	Χ	Χ	Χ	Х	NLA	NLB	NLC	0:
	0	1	↑	XX	1	0	1	1	0	1	0	1	B
	1	1	1	XX	0				VFP [6:	0]			0
Blanking Porch Control	1	1	↑	XX	0				VBP [6:	0]			0
	1	1	↑	XX	0	0	0			HFP [4:0]		0.
	1	1	↑	XX	0	0	0			HBP [4:0	1		1





1		0	1	*	XX	1	0	1	1	0	1	1	0	B6h
Display Function Control 1				<u> </u>							· -	 	1	
1	Display Function Control									110			[1.0]	
Entry Mode Set	Biopiay Failotton Control						†	- 00	Olvi			30 [0.0]		+
Entry Mode Set 0												01		
Entry Mode Set								1	1				1	
Backlight Control 1	Entry Mode Set			<u></u>						1			1	_
Backlight Control 1		0		1										B8h
1	Backlight Control 1			1		Х				Х				XX
Backlight Control 2	Ŭ	1	1	1			1	Х				I UI [3:0]	II.	04
1		0	1	1	XX	1	0	1	1	1			1	B9h
Backlight Control 3	Backlight Control 2	1	1	1		Х	Х	Х	Х	Χ	Х	Х	Х	XX
Backlight Control 3		1	1	1	XX		TH_MV	[3:0]			TH	_ST [3:0]		B8
1		0	1	1	XX	1	0	1	1	1	0	1	0	BAh
Backlight Control 4	Backlight Control 3	1	1	1	XX	Χ	Х	Χ	Х	Χ	Х	Χ	Χ	XX
Backlight Control 4		1	1	1	XX	Χ	Х	Χ	Х		DT	H_UI [3:0]		04
1		0	1	1	XX	1	0	1	1	1	0	1	1	BBh
Backlight Control 5	Backlight Control 4	1	1	1	XX	X	Х	Χ	Х	Χ	Х	Х	Х	XX
Backlight Control 5		1	1	1	XX		DTH_M	V [3:0]			DTI	1_ST [3:0]		C9
1		0	1	1	XX	1	0	1	1	1	1	0	0	BCh
Backlight Control 7	Backlight Control 5	1	1	1	XX	Χ	X	Χ	Х	Х	Х	Χ	Χ	XX
Backlight Control 8		1	1	1	XX		DIM2	[3:0]	1	Χ		DIM1 [2	:0]	44
1	Backlight Control 7	0	1	1	XX	1	0	1	1	1	1	1	0	BEh
1	Daokiight Control 7	1	1	1			_		PWM	<u> _DIV [7</u>	':0]	T		0F
Power Control 1 1	Backlight Control 8	0	1	1				1	1	1	1	1	1	BFh
Power Control 1 1			1	1								LEDONPOL	LEDPWMOPL	
Power Control 2 1	Power Control 1		1	1				0	0				0	C0h
NV Memory Protection Key 1				1					1		-			
VCOM Control 1 1	Power Control 2			1			1		•		0		1	C1h
VCOM Control 1 1 1 ↑ XX X VMH [6:0] 31 VCOM Control 2 0 1 ↑ XX 1 1 0 0 0 1 1 1 0 0 0 1 1 1 0 1 0 0 0 0 1 0 0 0 0 1 0 <							'			1				
1							1	0	0		· ·	0	1	C5h
VCOM Control 2 0 1 ↑ XXX 1 1 0 0 0 1 1 1 C7F NV Memory Write 0 1 ↑ XXX 1 1 0 1 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1	VCOM Control 1													
VCOM Control 2 1 1 ↑ XX nVM VMF [6:0] CO NV Memory Write 0 1 ↑ XX 1 1 0 1 0 0 0 0 0 DDid NV Memory Protection Key 1 1 ↑ XX XX Y Y Y Y Y Y Y Y XX Y Y Y Y Y Y Y XX Y							<u> </u>		_			1 .		
NV Memory Write 0 1 ↑ XX 1 1 0 1 0 0 0 0 0 Dof NV Memory Protection Key 1 1 ↑ XX	VCOM Control 2						1	0	0		· ·	1	1	
NV Memory Write 1 1 ↑ XX X X X X Y Y Y Y Y Y Y Y Y Y Y XX Y Y Y Y Y XX Y				1			.		l ,			1 _		
NV Memory Protection Key 1 1 ↑ XX PGM_DATA [7:0] XX NV Memory Status Read 1 1 ↑ ↑ XX 1 1 0 1 0 0 0 1 0 0 1 0 0 0 0 0 0 0 0 0	ND/ NA NA/ ''			1								1	1	D0h
NV Memory Protection Key 0	NV Memory Write					X	X	Х	•			GM_ADR	[2:0]	
NV Memory Protection Key 1 1 ↑ XX KEY [23:16] 55 1 1 ↑ XX KEY [15:8] AA 1 1 ↑ XX KEY [7:0] 66 0 1 ↑ XX 1 1 0 1 0 0 1 0														
NV Memory Protection Key 1 1 ↑ XX KEY [15:8] AA 1 1 ↑ XX KEY [7:0] 66 NV Memory Status Read 0 1 ↑ XX 1 1 0 1 0 0 1 0						1	1 1	U				U	1	
1 1 ↑ XX KEY [7:0] 66 0 1 ↑ XX 1 1 0 1 0 0 1 0	NV Memory Protection Key													
NV Memory Status Read				-										
NV Memory Status Read 1 ↑ 1 XX X X X X X X X X X X X X X X X X XX X <td></td> <td></td> <td></td> <td></td> <td></td> <td>4</td> <td>1</td> <td>_</td> <td></td> <td></td> <td>0</td> <td>1</td> <td>0</td> <td></td>						4	1	_			0	1	0	
NV Memory Status Read 1 ↑ 1 XX X ID2_CNT [2:0] X ID1_CNT [2:0] XX							1					1	1	
	NV Memory Status Read											•	1	
		1	<u> </u>	1	XX	BUSY				X				XX





	Τ.		Ι.					Ι.		l _			Dat
	0	<u> </u>	1	XX	1	1	0	1	0	0	1	1	D3h
Decil D4	1	1	1	XX	X	X	X	X	X	X	X	X	XX
Read ID4	1	1	1	XX	0	0	0	0	0	0	0	0	00
	1	1	1	XX	1	0	0	1	0	0	1	1	93
	1	1	1	XX	0	1	0	0	0	0	0	1	41
	0	1	1	XX	1	1	1	0	0	0	0	0	E0h
	1	1	1	XX	X	X	Х	Х			0 [3:0]		08
	1	1	1	XX	X	Х			VP1 [5				0E
	1	1	1	XX	Х	Х		1	VP2 [5				12
	1	1	1	XX	Х	Х	Х	Х			4 [3:0]		05
	1	1	1	XX	Х	Х	Х		V	P6 [4			03
	1	1	1	XX	Х	Х	X	Х		VP ²	13 [3:0]		09
Positive Gamma	1	1	1	XX	Х			VI	P20 [6:0]				47
Correction	1	1	1	XX		VP36	[3:0]			VP2	27 [3:0]		86
	1	1	1	XX	Х		ı	VI	P43 [6:0]				2B
	1	1	1	XX	Х	Χ	Х	Χ		VP	50 [3:0]		0B
	1	1	1	XX	Х	Χ	Х		VF	P57 [4	1:0]		04
	1	1	1	XX	Х	Χ	X	Χ		VP	59 [3:0]		00
	1	1	1	XX	Х	Χ			VP61 [5:0]			00
	1	1	1	XX	X	Х			VP62 [5	5:0]			00
	1	1	1	XX	X	Х	Х	Χ		VP	63 [3:0]		00
	0	1	1	XX	1	1	1	0	0	0	0	1	E1h
	1	1	1	XX	Х	Χ	X	Χ		VN	0 [3:0]		08
	1	1	↑	XX	Х	Χ			VN1 [5	:0]			1A
	1	1	↑	XX	Х	Χ			VN2 [5	5:0]			20
	1	1	1	XX	Х	Х	Х	Χ		VN	4 [3:0]		07
	1	1	↑	XX	Х	Х	Х		V	N6 [4	:0]		0E
	1	1	1	XX	Х	Х	Х	Х		VN.	13 [3:0]		05
Negative Gamma	1	1	1	XX	Х			VI	N20 [6:0]				3A
Correction	1	1	1	XX		VN36	[3:0]			VN2	27 [3:0]		8A
	1	1	1	XX	Х		-	VI	N43 [6:0]				40
	1	1	<u> </u>	XX	Х	Х	Х	Х		VN	50 [3:0]		04
	1	1	1	XX	Х	Χ	Х		1V	N57 [4			18
	1	1	<u> </u>	XX	Х	Х	Х	Х			59 [3:0]		0F
	1	1	1	XX	Х	Х		ı	VN61 [3F
	1	1	1	XX	Х	Х			VN62 [3F
	1	1	<u> </u>	XX	Х	Х	Х	Х			63 [3:0]		0F
Digital Gamma Control 1	0	1	1	XX	1	1	1	0	0	0	1	0	E2h
1 st Parameter	1	1	1	XX		RCA0	l				40 [3:0]	I	XX
:	1	1	1	XX		RCAx					4x [3:0]		XX
16 th Parameter	1	1	1	XX		RCA15					15 [3:0]		XX
Digital Gamma Control 2	0	1	1	XX	1	1	1	0	0	0	1	1	E3h
1 st Parameter	1	1	1	XX		RFA0	l				\0 [3:0]	· · ·	XX
	1	1	<u> </u>	XX		RFAx					Ax [3:0]		XX
64 th Parameter	1	1	↑	XX		RFA63					.63 [3:0]		XX
UT I AIAIIIEIEI	0	1	<u> </u>	XX	1	1	1	1	0	1	1	0	F6h
	1	1	1	XX		MX_EOR	MV EOR	X	BGR_EOR	X	X	WEMODE	01
Interface Control	1	1		XX	MY_EOR		EPF [X X	X		T WEMODE ОТ [1:0]	00
			_		X	X							
	1	1	<u> </u>	XX	Х	Х	ENDIAN	Χ	DM [1:	υJ	RM	RIM	00

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP





(00h).

Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9341 is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.





8.2. Description of Level 1 Command

8.2.1. NOP (00h)

00h					NOP (No	o Opera	ation)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
Parameter					No P	aramete	er.						
Description		emory Writ		nmand; it does not ha	-			-					erminate
Restriction	None												
				Normal Mode On,	Status Idle Mod	de Off, S	Sleep O		ailability Yes				
Register				Normal Mode On,	Idle Mod	de On, S	Sleep O	ut	Yes				
Availability				Partial Mode On,					Yes	4			
				Partial Mode On,		le On, S	Sleep Ou		Yes	-			
					Sleep In				Yes	_			
					Status		Default '	Value					
Default					n Seque	ence	N/A	١					
					V Reset		N/A						
				HV	V Reset		N/A	١					
Flow Chart	None												





8.2.2. Software Reset (01h)

01h					SV	VRESET							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	0	0	0	0	0	1	01h
Parameter					No F	Paramete	er.						
	When the	Software	Reset com	mand is written, it c	auses a	software	e reset.	It resets	s the co	mmands	and pa	rameter	s to their
Description	S/W Rese	et default v	alues. (See	default tables in each	ch comm	nand des	cription	.)					
Description	Note: The	Frame Me	emory conte	ents are unaffected b	y this co	ommand							
	X = Don't	care.											
	It will be n	ecessary t	o wait 5mse	ec before sending ne	w comm	and follo	owing so	oftware r	eset. Th	e displa	y modul	e loads a	ıll display
Restriction	supplier fa	actory defa	ult values to	o the registers during	this 5m	sec. If S	oftware	Reset is	s applied	during	Sleep O	ut mode	, it will be
riestriction	necessary	y to wait 12	20msec bef	ore sending Sleep o	ut comm	nand. So	ftware F	Reset Co	ommand	cannot	be sent	during S	leep Out
	sequence).											
				No mare al Mare de Cor	Status	-1- 0" (21		ailability				
Register				Normal Mode On, Normal Mode On,					Yes Yes				
Availability				Partial Mode On,					Yes				
rtvandomty				Partial Mode On,					Yes				
					Sleep In	l			Yes				
					Status		Default '						
Default				Power (N/ <i>A</i>						
					V Reset V Reset		N/A						
					_								
				SWRESET(01h)									
							ļ	 le	gend		7		
							į		,gona				
							į [Co	mmand		l I		
			Dis	play whole blank scr	een			Pai	rameter	7	İ		
				•	/	/	1 4		isplay	=	į		
Flow Chart					/				ТЭРІСУ		į		
Flow Chart				\perp			j <	<^	ction	>			
				V			į (Vlode		 		
			/	Set Commands to			`				-		
				S/W Default			1 (Sequen	tial trans	sfer	į		
				Values	/		 				<u>.</u>		
								- ·	- 		_		
			/										
				Sleep In Mode									
					/								





8.2.3. Read display identification information (04h)

04h				RDDIDIF (I	Read Disp	lay Ider	ntificatio	n Inforr	mation)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
1 st Parameter	1	1	1	XX	Х	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ
2 nd Parameter	1	1	1	XX				ID1	[7:0]				XX
3 rd Parameter	1	1	1	XX				ID2	[7:0]				XX
4 th Parameter	1	1	1	XX				ID3	[7:0]				XX
Description Restriction	The 1 st The 2 nd The 3 rd	paramete paramete paramete	r is dumm er (ID1 [7:0 er (ID2 [7:0	its display identifica y data. o]): LCD module's r o]): LCD module/dri]): LCD module/dri	nanufactui ver versior	er ID.							
Register Availability				Normal Mode Normal Mode Partial Mode Partial Mode	On, Idle I	Mode Of Mode Or Mode Off Mode Or	n, Sleep f, Sleep (Out Out Out	vailabilit Yes Yes Yes Yes Yes	У			
Default				Pow	Status er On Sec SW Rese HW Rese	et	See de	It Value scription scription scription	1				
Flow Chart			2nd Paran 3rd Param	eter: Dummy Read leter: Send LCD modu leter: Send panel type eter: Send module/driv	and LCM/dri	cturer inforver versio		ion		7	F	Command Carameter Display Action Mode	



Description

a-Si TFT LCD Single Chip Driver 240RGBx320 Resolution and 262K color



8.2.4. Read Display Status (09h)

09h				RDI	DST (Re	ad Disp	lay Stat	us)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1 st Parameter	1	↑	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	Х
2 nd Parameter	1	↑	1	XX				D [31:25]			0	00
3 rd Parameter	1	↑	1	XX	0		D [22:20]		D [1	9:16]		61
4 th Parameter	1	↑	1	XX	0 0 0				0		D [10:8]		00
5 th Parameter	1	↑	1	XX		D [7:5]		0	0	0	0	0	00

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D04		0	Booster OFF
D31	Booster voltage status	1	Booster ON
Doo	Daw address and an	0	Top to Bottom (When MADCTL B7='0')
D30	Row address order	1	Bottom to Top (When MADCTL B7='1')
D29	Calumn addraga arder	0	Left to Right (When MADCTL B6='0').
D29	Column address order	1	Right to Left (When MADCTL B6='1').
Doo	Daw/aalumn ayahanga	0	Normal Mode (When MADCTL B5='0').
D28	Row/column exchange	1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	0	LCD Refresh Top to Bottom (When MADCTL B4='0')
DZI	Vertical refresh	1	LCD Refresh Bottom to Top (When MADCTL B4='1').
D26	RGB/BGR order	0	RGB (When MADCTL B3='0')
D20	ndb/bdn oldel	1	BGR (When MADCTL B3='1')
D25	Horizontal refresh order	0	LCD Refresh Left to Right (When MADCTL B2='0')
D25	Honzontai reiresii ordei	1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	0	
D23	Not used	0	
D22		101	16 hit/nival
D01	Interface color pixel format	101	16-bit/pixel
D21	definition	110	18-bit/pixel
D20		110	10-bit/pixei
D19	Idle mode ON/OFF	0	Idle Mode OFF
DIS	idle IIIode ON/OI I	1	Idle Mode ON
D18	Partial mode ON/OFF	0	Partial Mode OFF
D10	Tartial mode ON/OTT	1	Partial Mode ON.
D17	Sleep IN/OUT	0	Sleep IN Mode
D17	Gleep II W G G I	1	Sleep OUT Mode.
D16	Display normal mode ON/OFF	0	Display Normal Mode OFF.
D10	Display normal mode ON/OTT	1	Display Normal Mode ON.
D15	Vertical scrolling status	0	Scroll OFF
D14	Not used	0	
D13	Inversion status	0	Not defined
D12	All pixel ON	0	Not defined
D11	All pixel OFF	0	Not defined
D10	Display ON/OFF	0	Display is OFF
510	Dispidy ON/OTT	1	Display is ON
D9	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
55	Totaling chock line ON/OFF	1	Tearing Effect ON
		000	GC0
		001	
D[8:6]	Gamma curve selection	010	
		011	
		other	Not defined

The information contained herein is the exclusive property of ILI Technology Corp. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of ILI Technology Corp.





		D.5	- ·	"	0		Mode 1, V-E	Blanking only
		D5	I earing	g effect line mode	1	Mode	2, both H-Blan	king and V-Blanking.
		D4		Not used	0			
		D3		Not used	0		-	
		D2		Not used	0			
		D1		Not used	0			
		D0		Not used	0		-	
	X = Don	't care						
Restriction								
					Status		Availability	
			•	Normal Mode O		Off, Sleep Out	Yes	
Register				Normal Mode O	n, Idle Mode (On, Sleep Out	Yes	
Availability				Partial Mode Or	n, Idle Mode C	Off, Sleep Out	Yes	
			_	Partial Mode Or	n, Idle Mode C	On, Sleep Out	Yes	
					Sleep In		Yes	
						Defective		
					tatus In Sequence	Default Val 32'h006100		
Default					/ Reset	32'h006100		
					/ Reset	32'h006100		
						0211000100		
				RDDST(i	09h)			Legend
								Command
						Host		
Flam Obart						Driver		Display
Flow Chart		2 3 4	rd Parameter: th Parameter: \$	Dummy Read Send D[31:25] displa Send D[19:16] displa Send D[10:8] display Send D[7:5] display s	ay status status			Action Mode
								Sequential transfer





8.2.5. Read Display Power Mode (0Ah)

0.2.5. Ne		. ,				M (Read	Display	Power	Mode					
	D/CX	RDX	WRX		D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	WHA ↑		XX	0	0	0	0	1	0	1	0	0Ah
1 st Parameter	1	<u>'</u>	1		XX	X	X	X	X	X	X	X	X	X
2 nd Parameter	1	<u> </u>	1		XX	D7	D6	D5	D4	D3	D2	D1	D0	08
	This co	mmand inc		current	status of the								_	
			ſ	Bit	Value		escriptio			Commer	nt			
			-			Booster					11			
				D7		Booster C								
			-	D.0	0		e Mode (
			<u>_</u>	D6	1	Idle	e Mode (On.						
				D5	0	Part	ial Mode	Off.						
			-	D3	1		ial Mode							
Description				D4	0		ep In Mo							
			-		1		ep Out M		_					
				D3		Display I								
			-		1	Display			1					
				D2	1		splay is (splay is (
			-	D1			ot Define			Set to '0	,			
			-	D0			ot Define			Set to '0				
	X = Dor	n't care	L		<u> </u>									
B														
Restriction														
											_			
						Status				vailability	'			
Register					rmal Mode C					Yes	-			
					rmal Mode C					Yes Yes				
Availability					artial Mode O artial Mode O					Yes	-			
				1 6	artiai Mode O	Sleep		Sieep C	,ut	Yes				
				<u> </u>		о.оор				. 00	_			
						Status		Default	: Value					
Default					Powe	r On Seq	uence	8'h(08h					
						SW Rese		8'h(4				
					l	HW Rese	et	8'h(08h					
											ŗ			
				٦							- !	L	.egend	i
					RDDPM(0Ah)							ommand	
							_ н	ost				P	arameter	7 i
							 Di	 iver			- :			=
Flow Chart	_				▼						フ!		Display	√ i
			1st Paramete								/ i	<_	Action	>
			2nd Paramet	er: Send	d D[7:2] display	power mo	de status			/			Mode	\supset \Box
											į			
											į	Seque	ential trans	sfer
											i_			





8.2.6. Read Display MADCTL (0Bh)

8.2.6. Rea	au DIS	piay iv	IADU	, i L (U										
0Bh					RDDMA	DCTL (I	Read Di	splay M	ADCTL))				
	D/CX	RDX	WR	X	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1		XX	0	0	0	0	1	0	1	1	0Bh
1 st Parameter	1	1	1		XX	Х	Х	Х	Х	Х	Х	Х	Х	Х
2 nd Parameter	1	↑	1		XX	D7	D6	D5	D4	D3	D2	D1	D0	00
	This co	mmand ind	dicates	the curre	nt status of the	display	as descr	ribed in t	he table	below:				
			Bit	Value		[Descripti	on			Com	ment		
			D7	0	Top to	Bottom	(When I	MADCTL	B7='0')			-		
			<i>D</i> ,	1	Bottom	to Top	(When N	MADCTL	B7='1')			-		
			D6	0		o Right (-		
				1		to Left (-		
			D5	0		l Mode								
Description				0	LCD Refresh	Se Mode								
Description			D4	1	LCD Refresh									
				0		GB (Wh				D T = 1).				
			D3	1		GR (Whe						-		
			D0	0	LCD Refresh					32='0').		-		
			D2	1	LCD Refresh	n Right to	Left (W	/hen MA	DCTL E	32='1').		-		
			D1		Switching	betweer	n Segme	ent outpu	its and F	RAM	Set t	o '0'		
			D0		Switching	betweer	n Segme	ent outpu	its and F	RAM	Set t	o '0'		
	X = Dor	n't care												
Restriction														
						Status			Αν	/ailability	,			
				١	Normal Mode O			Sleep C		Yes				
Register					Normal Mode Oi					Yes				
Availability					Partial Mode Or	, Idle M	ode Off,	Sleep C	ut	Yes				
					Partial Mode Or	, Idle M	ode On,	Sleep C	ut	Yes				
						Sleep I	n			Yes				
						Status		Default	t Value					
					Power	On Seq	uence	8'h(
Default						W Rese		No Ch						
					Н	IW Rese	t	8'h(
							1					L	egend	<u> </u>
					RDDMADCT	L(0Bh)					į			つ 川
								1 1			į		Command	<u> </u>
								lost 			- !	P	arameter	_/ []
Flow Chart	_						Dı	river			i		Display	_)
1 low onart			1ct Dara	motor: Du	mmy Read						/ i		Action	>
					end D[7:2] display p	oower mo	de status			/	/ į		Mode	<u> </u>
										/	į			<u> </u>
											į	Seque	ential trans	sfer
											_			





8.2.7. Read Display Pixel Format (0Ch)

0Ch		<u> </u>					RDDCO	LMOD (Read Di	spla	v Pix	xel F	orm	at)				
	D/CX	RDX	10	/RX	Т		D17-8	D7	D6	D	1	D4		D3	D2	D1	D0	HEX
Command	0	1		<u>/n∧</u> ↑			XX	0	0	0		0	+	1	1	0	0	0Ch
1 st Parameter	1	_ ' ↑		1			XX	X	X		ζ	X		X	X	X	X	X
2 nd Parameter	1	<u> </u>		1			XX	RIM		DPI				0		DBI [2:0]		06
		mmand			the c	urre	nt status of th					the t	able			22. [2.0]		
		Г						•	-							Г		
		-	RIM 0	0	PI [2:	0	RGB Int	errace F eserved	ormat		0	BI [2 0	<u>0</u>	MCC	Reser	ce Forma	lt	
		-	0	0	0	1		eserved		1	0	0	1		Reser			
		-	0	0	1	0		eserved		7	0	1	0		Reser			
			0	0	1	1		eserved			0	1	1		Reser			
			0	1	0	0	R	eserved			1	0	0		Reser			
Description			0	1	0	1	16 k	oits / pixe	el		1	0	1		16 bits /	pixel		
			0	1	1	0	18 k	oits / pixe	el	_	1	1	0		18 bits /	pixel		
			0	1	1	1		eserved		_	1	1	1		Reser	ved		
			1	1	0	1		oits / pixe										
		-					(6-bit 3 tim			_								
			1	1	1	0	18 t (6-bit 3 tim	oits / pixe										
	X = Dor	L a't caro			l .		(0-011.5 11111	es uaia	ii ai isici)									
	X = D01	i i caie																
Restriction																		
		Ctatus Augilahilitu																
		Status Availability																
Register							ormal Mode							Yes				
negistei							ormal Mode							Yes				
Availability							artial Mode							Yes				
						-	artial Mode (n, Si	еер	Out		Yes Yes				
								Sleep	ווו				<u> </u>	162				
										_						1		
						5	Status		RIM	T		It Va			1.10.01			
Default				ŀ	Pow	ıor C	n Sequence		l'b0			l [2:0 :000			l [2:0] b110			
Boldan				F	1 00		/ Reset		Chang			Chan	a		Chang			
				-			/ Reset		l'b0			000c	9		b110			
								1										
															į	L	egend	j
							RDDCOLN	MOD(0Ch)							į			$\neg \mid \mid$
										Hos					į	$\overline{}$	Command	<u> </u>
															İ	<u></u>	'arameter	_/ :
Flow Chart	_						•	7		Drive	er				i		Display)
I low onare			1 91	Para	meter	·· Dur	nmy Read								/		Action	> 11
							nd D[7:2] displa	y pixel for	mat statu	s					/		Mode	<u> </u>
														/	į			
															į	Seque	ential tran	isfer
															į.			<u> </u>
															•			





8.2.8. Read Display Image Format (0Dh)

0Dh					RDD	IM (Read	d Displa	y Image	Mode)					
	D/CX	RDX	WRX	D.	17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1)	ΚX	0	0	0	0	1	1	0	1	0Dh
1 st Parameter	1	1	1		ΚX	Х	Х	X	Х	Х	Χ	Х	Χ	Х
2 nd Parameter	1	1	1)	ΚX	0	0	0	0	0		D [2:0]		00
Description	This cor		dicates the	e current s	D [2 00 00 01 01 01 01 01 01 01 01 01 01 01	2:0] 00 11 0	Gamr	Descripe ma curve	tion e 1 (G2.2					
Restriction														
Register Availability				Norr Par	nal Mode (nal Mode (tial Mode C	On, Idle I On, Idle I	Mode Of Mode Or Mode Off Mode Or	n, Sleep f, Sleep (Out Out Out	Yes Yes Yes Yes Yes Yes Yes Yes	У			
Default				-	Power On	atus Sequen Reset Reset	ice	3'b 3'b	It Value 0000 0000					
Flow Chart			1st Parame 2nd Param		RDDIM V V P V Read D[7:0] display]	Host Driver		/	7	F C	egend Command Parameter Display Action Mode	





8.2.9. Read Display Signal Mode (0Eh)

0Eh				RDI	OSM (Re	ad Displ	ay Sign	al Mode	!)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	0	0	1	1	1	0	0Eh
1 st Parameter	1	1	1	XX	Х	Χ	Χ	Χ	Х	Х	X	Х	Х
2 nd Parameter	1	1	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00
Description	This co		ndicates t	D7 1 0 0 1 1 0 1 0 1 1 0 1 0 1 0 1 1 0 1 0 1	Tearing of Tearing of Tearing of Tearing of Tearing of Horizontal State of Tearing of Horizontal State of Tearing of Horizontal State of Tearing of Horizontal State of Tearing	effect line effect line effect line effect line effect line effect line all sync. (all sync. (RC sync. (RC ck (DOTC ck (DOTC ck (DOTC ble (DE, ble (DE,	Description OFF ON OM OM OM OM OM OM OM OM OM OM OM OM OM	erface) (erface) (ace) OF ace) ON B interfa B interfacerface)	DFF DN F ace) OFF ace) ON				
Restriction													
Register Availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes												
Default				Por		equence set	8' 8'		9				
Flow Chart	SW Reset 8'h00h HW Reset 8'h00h RDDSM(0Eh) Host Driver Display Action Action Mode Sequential transfer												





8.2.10. Read Display Self-Diagnostic Result (0Fh)

0Fh				RDDS	DR (Read	Display 9	Self-Diag	gnostic	Result)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	0	0	1	1	1	1	0Fh
1 st Parameter	1	1	1	XX	Х	Х	Х	Χ	Х	Х	Χ	Х	Χ
2 nd Parameter	1	1	1	XX	D7	D6	0	0	0	0	0	0	00
	Ві	it	Descript	on				P	Action				
	D.		ter Loading		Invert	he D7 bit	if registe	er values	loading	work pro	perly.		
	D	6 Fur	nctionality D		Invert	he D6 bit	if the dis	splay is f	unctiona	lity			
	D:	5	Not Use	ed					'0'				
Description	D.	4	Not Use	ed					'0'				
	D:		Not Use						'0'				
	D:		Not Use						'0'				
	D		Not Use						'0'				
	D	0	Not Use	ed					'0'				
Restriction													
Register Availability	Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes												
Default				-	Power Or SW	tus Sequenc Reset Reset	e 8	ault Valu 3'h00h 3'h00h 3'h00h	<u>e</u>				
Flow Chart			st Parameter: nd Parameter	Dummy Rea			Host Driver					Command Paramete Display Action Mode	





8.2.11. Enter Sleep Mode (10h)

10h					SPLIN	(Enter S	Sleep Mo	ode)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	0	1	0	0	0	0	10h
Parameter						No Para	meter						
	This comr	mand cause	es the LCD	module to e	nter the	minimur	n power	consu	mption mo	ode. In t	this mod	le e.g. th	e DC/DC
	converter i	s stopped,	Internal osci	llator is stopp	ed, and	panel sc	anning is	stoppe	ed.				
Description													
	MCU inter	face and m	emory are st	ill working an	d the me	emory ke	eps its c	ontents					
	X = Don't	care											
	This comn	nand has n	o effect whe	en module is	already	in sleep	in mode	e. Slee	o In Mode	can on	y be left	by the S	Sleep Out
	Command	(11h). It w	vill be neces	sary to wait	5msec b	efore se	nding ne	ext to c	ommand,	this is to	allow t	ime for t	ne supply
Restriction	voltages a	nd clock cir	cuits to stab	ilize. It will be	necessa	ary to wai	t 120ms	ec afte	sending S	Sleep Ou	ıt comma	and (wher	n in Sleep
	In Mode) b	efore Sleep	o In commar	ıd can be ser	nt.								
			Г		C+	atus			Availabilit	v			
				Normal Mode			Off. Sleer	o Out	Yes	У			
Register				Normal Mode					Yes				
Availability				Partial Mode	On, Idle	Mode C	ff, Sleep	Out	Yes				
			_	Partial Mode			n, Sleep	Out	Yes				
			L		Slee	ep In			Yes				
				Davi	Statu			ult Valu					
Default				Pov	SW Re	equence eset		IN Mo IN Mo					
					HW Re			IN Mo					
	It takes 12	0msec to g	et into Sleep	In mode afte	r SLPIN	commar	nd issued	d.		.—.			
										į	L	egend	İ
						▼	_			ŀ			一 !
		CDUN (10	de)							ļ	С	ommand	i
		SPLIN (10	(1)			op DC/DC onverter				į	Pa	arameter	7 ¦
										į		Display	=\
							_/			ľ			<
	D: 1			,		\downarrow					<	Action	>
Flow Chart		ly whole blar natic No effe				,				į		Mode	$\supset \ \mid$
		I/OFF comm		/	Sto	p Interna	1			į			
			/			Scillator				ļ	Seque	ential trans	fer
							_/			 _			
	/					\downarrow							
	/	Drain char	ge \										
		from LCI panel			Slee	ep In Mod	le)						
		parior											
	· ·												
	1												

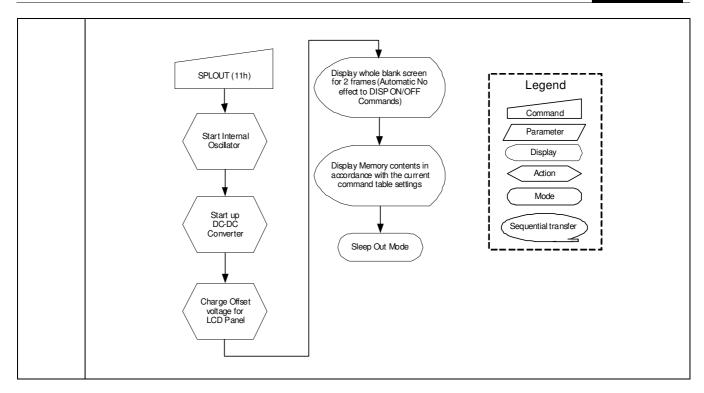




8.2.12. Sleep Out (11h)

11h					SLF	POUT (S	eep Out	:)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Parameter						No Para	meter						
Description		de e.g. the I	off sleep mo	de. erter is enabl	ed, Inter	nal oscill	ator is sta	arted, a	nd panel	scanning	j is starte	d.	
Restriction	Command and clock 5msec and when this functions of	(10h). It wi circuits stal d there can load is done during this 5	Il be necessabilize. The denoted be any are and when the	en module is ary to wait 5m isplay module abnormal visuathe display meeessar be necessar	nsec before loads a	ore sendiall displation the contract on the contract series of the contract series of the contract of the cont	ng next o y supplie display ir Gleep Ou	commarer's factor mage if t -mode	nd, this is ory defau factory do e. The dis	to allow to	time for t to the re d registe	he supply egisters d r values bing self-c	voltages uring this are same
Register Availability				Normal Mode Normal Mode Partial Mode Partial Mode	e On, Idle e On, Idle e On, Idle e On, Idle	Mode C	on, Sleep	Out Out Out	Availabili Yes Yes Yes Yes Yes	ty			
Default				Pov	Statu ver On S SW Re HW Re	equence set	Sleep	ult Valu IN Mod IN Mod IN Mod	le le				
Flow Chart	It takes 12	0msec to b	ecome Slee	p Out mode a	after SLP	OUT cor	nmand is	ssued.					









8.2.13. Partial Mode ON (12h)

12h					PTLO	N (Partia	l Mode	On)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	0	1	0	0	1	0	12h
Parameter						No Para	meter						
Description		de, the Nor	•	node The part				•	the Part	ial Area	commar	nd (30H).	To leave
Restriction	This comm	nand has no	o effect whe	n Partial mode	e is active	е.							
		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes											
Register			-						Yes				
_			_	Normal Mode Partial Mode					Yes Yes				
Availability			-	Partial Mode	· · · · · · · · · · · · · · · · · · ·				Yes				
					Slee		, стогр		Yes				
Default			L	Power Or	tatus	nce No	Defa ormal Dis ormal Dis	splay Mo	de ON de ON				
Flow Chart	See Partia	l Area (30h)										





8.2.14. Normal Display Mode ON (13h)

13h				NORON	(Norm	al Displa	ay Mode	e On)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	0	0	1	0	0	1	1	13h	
Parameter					No F	Paramete	er							
Description	Normal di	splay mode	e on means	ay to normal mode. Partial mode off. mode On command	(12h)									
Restriction	This com	his command has no effect when Normal Display mode is active.												
Register Availability				Normal Mode On, Normal Mode On, Partial Mode On, Partial Mode On,	Idle Mo	de On, S de Off, S de On, S	Sleep Ou Sleep Ou	ut ut it	Yes Yes Yes Yes Yes Yes					
Default				Status Power On Sec SW Rese	et	Norma Norma	al Displa	Value y Mode y Mode y Mode	ON					
Flow Chart	See Partia	al Area (30	h)											





8.2.15. Display Inversion OFF (20h)

	_			JII OFF (20									
20h					DIN	OFF (Dis	play Inve	rsion OF	F)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	0	0	0	0	20h
Parameter							Paramete	r					
	This co	ommand	is used t	o recover from o	display inv	ersion mo	de.						
	This co	ommand	makes n	o change of the	content c	of frame m	emory.						
	This co	mmand	doesn't	change any othe	er status.								
				Mem	nory				Display I	Panel			
					+++	+		+		+++	_		
Description											_		
						$+$ \vdash		-					
							$\neg \checkmark$				_		
						+		-			_		
						1				1 1 1 1			
	X = Do	n't care											
Restriction	This co	mmand	has no e	ffect when mode	ule alread	y is invers	ion OFF r	mode.					
						Status			Availab	ility			
Register						n, Idle Mo			Yes				
						on, Idle Mo			Yes				
Availability						n, Idle Mo n, Idle Mo			Yes Yes				
				1 ditte	ai Mode C	Sleep Ir		cop out	Yes				
				-		atus		efault Va					
Default				<u> </u>		Sequence Reset		ay Inversi ay Inversi					
						Reset		ay Inversi					
<u> </u>							•						
							l ⁻				:		
				Display In	vorsion O	n Mada	\		Legen	d	l		
				Display III	version O	II Mode	ノi				l		
				-					Comman	<u>d</u>	į		
					V		İ		Paramete	er /	i		
							į		Display		-		
Flow Chart				IN\	/OFF(20h	1)			Diopiay		į		
									Action	_>	i		
					▼		į		Mode		!		
				Display In	version ∩	ff Mode	\				-		
							/ ¦	Sequ	ıential tra	nsfer			
							į				1		
							١_				ن		





8.2.16. Display Inversion ON (21h)

0.2.10.		,		JII ON (211		VON (D	mlay lay	roice Ot	I)						
21h				1		T T	play Inve	ı							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	<u> </u>	XX	0	0	Doromoto	0	0	0	0	1	21h		
Parameter	TI-1-		lia e e li	o enter into disp	I=!		Paramete	ſ							
	This co	ommano	d makes n d doesn't d	to change of the change any other mode, the Disp	content o	f frame m	emory. Ev				rame men	nory to the	display.		
Description	X = Do	n't care				-									
Restriction	This co	mmano	l has no e	effect when mod	ıle alread	v is invers	ion ON m	ode							
Register Availability		X = Don't care This command has no effect when module already is inversion ON mode. Status Normal Mode On, Idle Mode Off, Sleep Out Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Sleep In Yes													
					Status		Г	efault Va	lue						
				Powe	r On Sequ	Jence		ay Inversi							
Default					SW Reset			ay Inversi							
					HW Reset			ay Inversi							
Flow Chart				Display Inv	/ON(21h)			Seq	Commar Paramete Display Action Mode	er /					





8.2.17. Gamma Set (26h)

0.2.17.		u OCt (2	· · · · ·										
26h					GAN	ISET (Ga	mma S	et)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	0	1	1	0	26h
Parameter	1	1	1	XX				G	C [7:0]				01
	This comn	nand is use	d to select t	he desired G	amma cı	urve for th	ne curre	nt displ	ay. A max	imum of	4 fixed o	gamma c	urves can
	be selecte	d. The curv	e is selected	d by setting th	ne approp	oriate bit i	n the pa	ramete	r as descr	ibed in th	ne Table	:	
				GC [7:	01	Cur	ve Selec	cted					
				01h		Gamma)				
Description				02h									
				04h									
				08h									
	Note: All o	ther values	are undefin	ed.									
	X = Don't	care											
5	Values of	GC [7:0] no	t shown in ta	able above ar	e invalid	and will r	not chan	ge the	current se	lected G	amma cı	urve until	valid
Restriction	value is re	ceived.											
			_										
			-			atus			Availabili	ty			
Register				Normal Mode					Yes				
_			F	Normal Mode					Yes				
Availability			F	Partial Mode					Yes Yes				
			F	T artial Wood		ep In	ii, Oloop	Out	Yes				
						'							
					0			1. 37. 1					
				Po	Stat	us Sequence		ult Valu	ie				
Default				10	SW R			<u>'h01h</u> 'h01h					
					HW R			'h01h					
							ı	-					
						\neg	!		Lege	 end			
							i) 	Logo	/11U	. !		
				GAMSET	(26h)				Comm	and			
							į				J 7		
				\forall				¦	Param	eter	/ į		
				· ·			7		Displa	nv)		
Flow Chart			/ 1	st Parameter	: GC[7:0] /	/			=	′ ¦		
		,	/					ı <	Actio	<u>n</u>	`		
							j		Mod	e	\		
				\							′ į		
				· ·			į		equential	tranefor	\		
				New Gamma Loade						u anisiel	ノi		
				20000	~		į						





8.2.18. Display OFF (28h)

Dispose for the command of the comma	0.2.10.	- 1-		11 (20	,		DIODO	- (D: :	055					
Command 0 1 1 2 XX 0 0 1 0 1 0 0 0 28h Parameter This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command has no change any other status. There will be no abnormal visible offect on the display. Description This command has no effect when module is already in display off mode. Register Availability Default Default Default Display Panel Display Panel Display Panel Display Panel Availability Display Panel Display Panel Display Panel Display Panel Availability Display Panel Display Off Mode Display Off Mode Display Off Display Off Mode Display Off Display Display Off Display Off Display Display Off Display Off Display Display Display Display Display Display Display Display Displa	28h						T		1		ı			
This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Description This command has no effect when module is already in display off mode. Restriction Register Availability Partial Mode On, Ide Mode Off, Sleep Out Yes Partial Mode On, Ide Mode On, Sleep Out Yes Partial Mode On, Ide Mode On, Sleep Out Yes Sleep In Yes Sleep In Yes Sleep In Yes Display OFF Legend Display OFF Di														1
This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible offect on the display. Memory Display Panel Memory Display Panel Normal Mode On, Ide Mode Off, Sleep Out Yes Partial Mode On, Ide Mode Off, Sleep Out Yes Partial Mode On, Ide Mode Off, Sleep Out Yes Partial Mode On, Ide Mode Off, Sleep Out Yes Partial Mode On, Ide Mode Off, Sleep Out Yes Partial Mode On, Ide Mode Off, Sleep Out Yes Partial Mode On, Ide Mode Off, Sleep Out Yes Partial Mode On, Ide Mode Off, Sleep Out Yes Sleep In Yes Status Default Display OFF HW Reset Display OFF HW Reset Display OFF Addion Mode Flow Chart Display Addion Mode		0	1	<u> </u>	XX	0				1	0	0	0	28h
page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Memory Display Panel Memory Display Panel Status Status Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes Default Default Display OFF Legend Display OFF Display OFF Display OFF Display OFF Display OFF Display OFF Display OFF Addion Mode	i arameter	This co	mmand	l is usad t	to enter into DIS	PI AV OF				tnut from	Frame Ma	emory is	ricahlad a	nd hlank
This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Memory Display Panel Memory Display Panel This command has no effect when module is already in display off mode. Status Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep in Yes Default Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Display On Mode Display On Mode Display On Mode Display On Mode Display On Mode Display On Mode Display On Mode Display On Mode Display On Mode					to criter into bio		1 111000.1		ode, the od	itput iroini	i ramo ivi	oniory is v	aioabica a	na biank
This command does not change any other status. There will be no abnormal visible effect on the display. Memory Display Panel Memory Display Panel This command has no effect when module is already in display off mode. Status Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes Sleep In Yes Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Display On Mode Parameter Display On Mode Display On Mode Display On Mode Display On Mode Display On Mode														
There will be no abnormal visible effect on the display. Memory Display Panel X = Don't care. Restriction This command has no effect when module is already in display off mode. Status Normal Mode On, Ide Mode Off, Sleep Out Yes Normal Mode On, Ide Mode Off, Sleep Out Parlial Mode On, Ide Mode Off, Sleep Out Per Parlial Mode On, Ide Mode Off, Sleep Out Per Parlial Mode On, Ide Mode Off, Sleep Out Per Parlial Mode On, Ide Mode Off, Sleep Out Per Parlial Mode On, Ide Mode Off, Sleep Out Per Parlial Mode On, Ide Mode Off, Sleep Out Per Parlial Mode On, Ide Mode On, Sleep Out Per Parlial Mode On, Ide Mode On, Sleep Out Per Parlial Mode On, Ide Mode On, Sleep Out Per Power On Sequence Display OFF SW Reset Display OFF Legend Parameter Display Display Display Addion Mode		This co	ommand	l makes r	no change of cor	itents of f	rame men	nory.						
Description X = Don't care. Restriction This command has no effect when module is already in display off mode. Status		This co	ommand	l does no	t change any oth	ner status	•							
Restriction This command has no effect when module is already in display off mode. Status		There	will be n	o abnorm	nal visible effect	on the dis	splay.							
Restriction This command has no effect when module is already in display off mode. Status					Men	nory				Display F	Panel			
Register Availability Register Availability Default Default This command has no effect when module is already in display off mode. Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Adion Display Adion Mode	Description						\perp		\perp		Ш	_		
Register Availability Register Availability Default Default This command has no effect when module is already in display off mode. Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Adion Display Adion Mode							+		-	+++	+++	_		
Register Availability Register Availability Default Default This command has no effect when module is already in display off mode. Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Adion Display Adion Mode							‡ _					_		
Register Availability Register Availability Default Default This command has no effect when module is already in display off mode. Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Adion Display Adion Mode								$\neg \nearrow$				_		
Register Availability Register Availability Default Default This command has no effect when module is already in display off mode. Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Adion Display Adion Mode									-H		+++	_		
Register Availability Register Availability Default Default This command has no effect when module is already in display off mode. Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Adion Display Adion Mode							#		#			<u> </u>		
Register Availability Register Availability Default Default This command has no effect when module is already in display off mode. Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Adion Display Adion Mode							1							
Register Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Display OFF HW Reset Display OFF Adion Display Display Adion Mode		X = Do	n't care											
Register Availability Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Legend Display On Mode Flow Chart Display On Mode Display Action Mode	Restriction	This co	ommand	l has no e	effect when mode	ule is alre	ady in dis	play off ı	mode.					
Register Availability Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF HW Reset Display OFF Legend Display On Mode Flow Chart Display On Mode Display Action Mode							Ctatua			Avoilab	ility			
Register Availability Normal Mode On, Idle Mode On, Sleep Out					Norma	al Mode (ode Off,	Sleep Out					
Default Partial Mode On, Idle Mode On, Sleep Out Yes Yes	Register													
Status Default Value Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF Legend Display On Mode Display Display Display Mode	Availability													
Default Status					Partia	al Mode C			Sleep Out					
Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF Legend Display On Mode Command Parameter Display Display Action Mode							Sieep ii	1		res				
Power On Sequence Display OFF SW Reset Display OFF HW Reset Display OFF Legend Display On Mode Command Parameter Display Display Action Mode							0: :		D (11)/					
SW Reset Display OFF HW Reset Display OFF Legend Display On Mode Parameter Display Display Action Mode						Powe		IONCO						
Flow Chart HW Reset Display OFF	Default													
Flow Chart Display On Mode Command Parameter Display Action Mode														
Flow Chart Display On Mode Command Parameter Display Action Mode									ı			- -,		
Flow Chart Display Action Mode								\	!	Leger	nd			
Flow Chart Display Action Mode					Displa	y On Mod	de					l I		
Flow Chart Display Action Mode							/	/		Commar	nd	į		
Flow Chart DISPOFF (28h) Action Mode									<u> </u>	Paramet	er/			
Flow Chart DISPOFF (28h) Action Mode										Display		 		
Mode	Flow Chart				DISP	OFF (28h)				=	İ		
							,		<	Action	_>	į		
Display Off Mode Sequential transfer						V				Mode		1 		
) J Cocquernial transier					Displa	y Off Mod	de		I Ser	nuential tr	ansfer	į		
						-	/	/		140		1		
							/		'					





8.2.19. Display ON (29h)

0.2.19.	cp	, -	14 (231	-,									
29h						T	N (Display	1					
_	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1 Paramete	0	1	0	0	1	29h
Parameter	Thio	ommore	l ic ucad t	o recover from	DIGDI VA		Paramete		Eromo Ma	mon, io o	nablad		
								from the i	rame we	emory is e	enabled.		
	This co	ommano	l makes n	o change of co	ntents of f	rame men	nory.						
	This co	ommano	d does not	change any otl	her status								
				Memory					Disp	olay Par	nel		
			+	++++	+++	_			$\perp \! \! \perp$	$\sqcup \! \! \perp$	\coprod	_	
Description			+		+++	_		\dashv			₩	_	
Description			+			_	\setminus	-			HH	-	
			\Box					コ				_	
			+			_		-			+++	-	
			+			_		-				-	
						_		コ				- -	
					1 1 1			l					
	X = Do	n't care											
Dantwinting				££ = = \$	مسام ما ماسم								
Restriction	THIS CO	Jiiiiianc	nas no e	ffect when mod	lule is aire	ady in dis	piay on m	loue.					
						Status			Availab	oility			
				Norm	al Mode C			Sleep Out	Yes				
Register					al Mode C				Yes				
Availability					<u>al Mode C</u> al Mode C				Yes				
				Faill	ai Mode C	Sleep I		ieep Out	Yes				
						Ctatus		Dofoult Ma	luc				
5 ();					Powe	Status er On Sequ		<u>Default Va</u> Display O					
Default						SW Rese		Display O					
						HW Rese	t	Display O	FF				
							- ا		Legen	 d	· -]		
				Disn	olay Off Mo	nde	\						
				Disp	nay On Ivic	de	/ ;		Comman	d	Ì		
							/ I I		Paramete		į		
							- !				İ		
Flow Chart				DI	SPON(29I	h)	į		Display		 		
					J. J. V(23)	''/	i		Action	\geq	-		
					\downarrow				Mode		į		
					▼				ivioue		ļ		
				Disp	olay On Mo	de) ;	Sagu	ential tra	nsfer	 		
							/ ¦	Ocqu			ļ		
							Ļ				ن.		
	1												

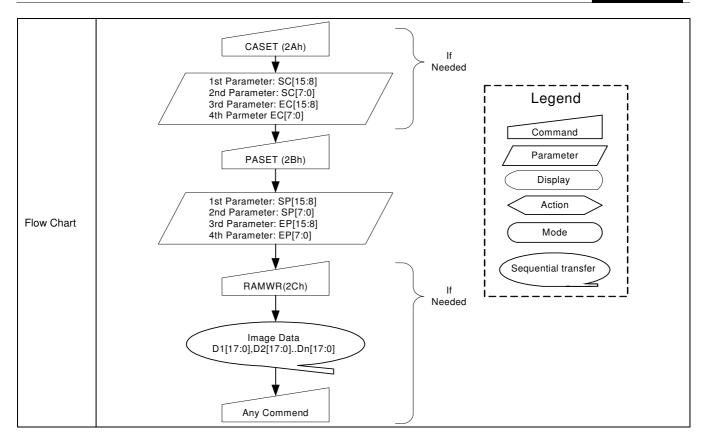




8.2.20. Column Address Set (2Ah)

				S SEL (ZAII)		OFT (O.)		-l O ·					
2Ah		ı			CA	SET (Col	lumn Add	dress Set)	•	ı	•	T
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	1	0	1	0	2Ah
1 st Parameter	1	1	1	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
2 nd Parameter	1	1	1	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3 rd Parameter 4 th Parameter	1	1	<u> </u>	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note1
4 Parameter	1			XX X	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	+
Description	other of	driver st	atus. Th	to define area of the values of SC line in the Frame	[15:0] aı	nd EC [1:			hen RAN			_	
		n't care		h	+	0 (45.0)							
	_	_	-	be equal to or les									
Restriction	Note 1	: When	SC [15:0)] or EC [15:0] is	greater th	nan 00EF	h (When	MADCTL'	s B5 = 0)	or 013Fh			
	(When	MADC	ΓL's B5 =	= 1), data of out o	of range v	vill be ign	ored						
Register Availability	Note 1: When SC [15:0] or EC [15:0] is greater than 00EFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored Status Availability Normal Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes												
Default			Por	Status wer On Sequenc SW Reset		15:0]=000 15:0]=000	00h If N	//ADCTL's	C [15:0]=0 B5 = 0: E	EC [15:0]=			
				HW Reset	_	15:0]=000	If N	MADCTL's	B5 = 1: E C [15:0]=0		=013Fh		
				TIVV NESEL	30	13.0]=000	ווטכ		<u>ا=ران.0]=(</u>	JULI II			





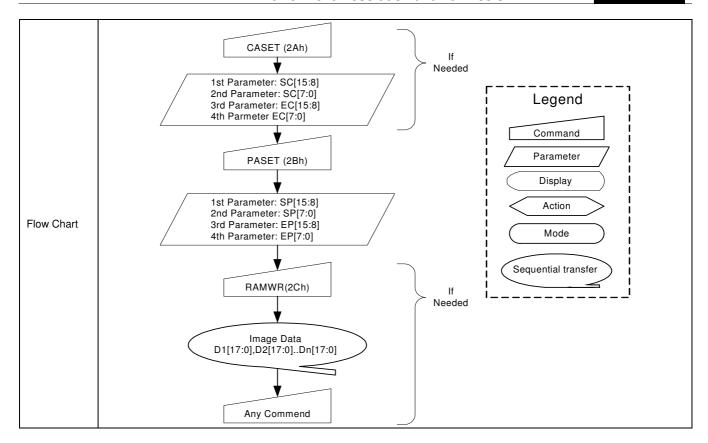




8.2.21. Page Address Set (2Bh)

Command		age /	-aui c	,33 0	et (2Bn)									
Command 0	2Bh					Р	ASET (Pa	age Add	Iress Set)					
1st Parameter 1 1 XX SP15 SP14 SP13 SP12 SP11 SP10 SP9 SP8 2°Parameter 1 1 1 1 1 1 XX SP7 SP6 SP5 SP4 SP3 SP2 SP1 SP9 SP8 3°Parameter 1 1 1 1 1 XX EP15 EP14 EP1 EP12 EP11 EP0 EP9 EP8 EP8 EP1 EP0 EP0 EP1 EP0 Image: EP0 EP1 EP0 Image: EP0 EP1 EP0 Image: EP0 Image: EP1 EP0 Image: EP1 EP0 Image: EP1 EP0 Image: EP1 EP1 Image: EP1 Image: EP1 Image: EP1 Image: EP1 Image: EP1 Image: EP1 Image: EP1		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
2ºººParameter 1 1 1 ↑ XX SP7 SP6 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 AP3 SP2 SP1 SP0 SP5 SP4 AP3 SP2 SP1 SP0 SP5 SP4 AP3 SP2 SP1 SP0 SP5 SP4 AP3 SP2 SP1 SP0 SP5 SP4 AP3 SP2 SP1 SP0 SP5 SP4 AP3 SP2 SP1 SP0 SP5 SP4 AP3 SP2 SP1 SP0 SP5 SP4 AP3 SP2 SP1 SP0 SP5 SP4 AP3 SP2 SP1 SP0 SP5 SP4 AP3 SP2 SP1 SP0 SP5 SP4 AP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP3 SP2 SP1 SP0 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP5 SP4 SP3 SP2 SP1 SP0 SP3 SP3 SP2 SP1 SP0 SP1 SP0 SP3 SP3 SP2 SP1 SP0 SP3 SP3 SP3 SP3 SP2 SP1 SP0 SP3 SP3 SP3 SP3 SP3 SP3 SP3 SP3 SP3 SP3		0	1	1	XX	0	0	1	0	1	0	1	1	2Bh
2"Parameter 1 1 1 1 XX SP7 SP6 SP6 SP5 SP1 SP0 SP2 SP1 SP0 3"Parameter 1 1 1 1 XX EP15 EP14 EP13 EP12 EP11 EP10 EP9 EP8 4" Parameter 1 1 1 1 XX EP15 EP14 EP15 EP14 EP11 EP10 EP19 EP1 EP10 SP9 EP8 4" Parameter 1 1 1 1 XX EP7 EP6 EP5 EP4 EP3 EP2 EP1 EP0 Other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each represents one Page line in the Frame Memory. SP[15:0] EP[15:0] EP[15:0] Festriction SP [15:0] always must be equal to or less than EP [15:0] Restriction Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 ala of out of range will be ignored. Register Availability Status Availability	1 st Parameter	1	1	1	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note1
This command is used to define area of frame memory where MCU can access. This command makes no change of other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each represents one Page line in the Frame Memory. SP[15:0] X = Don't care SP [15:0] X = Don't care SP [15:0] aways must be equal to or less than EP [15:0] Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 data of out of range will be ignored. Register Availability Register Availability Status Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fh MADCTL's B5 or EP [15:0]=013Fh		1	1	1	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	140101
This command is used to define area of frame memory where MCU can access. This command makes no change of other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each represents one Page line in the Frame Memory. SP[15:0] X = Don't care SP [15:0] always must be equal to or less than EP [15:0] Restriction Restriction Register Availability Register Availability Default Status Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fb, Use Mature Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fb, Use Mature Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fb, Use Mature Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fb, Use Mature Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fb, Use Mature Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fb, Use Mature Sleep In In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fb, Use Mature Sleep In In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fb, Use Mature Sleep In In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fb, Use Mature Sleep In In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fb, Use Mature Sleep In In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fb, Use Mature Sleep In In Yes Status Default Value EP [15:0]=013Fb, Use Mature Sleep In In Yes Status Default Value EP [15:0]=013Fb, Use Mature Sleep In In Yes Status Default Value EP [15:0]=013Fb, Use Mature Sleep In In Yes Status Default Value EP [15:0]=012Fb, Use Mature Sleep In In Yes Status Default Value EP [15:0]=012Fb, Use Mature Sleep In In Yes Status Default Value EP [15:0]=012Fb, Use Mature Sleep In In Yes Status Default V		1	1	<u> </u>	†	EP15	EP14	EP13		EP11	EP10	EP9	EP8	Note1
other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each represents one Page line in the Frame Memory. SP[15:0] X = Don't care SP [15:0] always must be equal to or less than EP [15:0] Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 data of out of range will be ignored. Register Availability Register Availability Status	4 th Parameter											•		
Restriction Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 data of out of range will be ignored. Status	Description	other of	driver sta	atus. Th	e values of SP ne in the Frame M SP[13	[15:0] ai	nd EP [15						_	
Register Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fh If MADCTI's B5 = 0: EP [15:0]=013Fh	Restriction	Note 1	: When \$	SP [15:0] or EP [15:0] is g			n (When	MADCTL's	s B5 = 0)	or 00EFh	(When M	ADCTL's	B5 = 1),
Register Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fh If MADCTI's B5 = 0: EP [15:0]=013Fh														
Register Availability Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fh If MADCTI's B5 = 0: EP [15:0]=013Fh							Status			Availab	oility			
Availability Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fh If MADCTI's R5 = 0: EP [15:0]=013Fh	Register													
Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value Power On Sequence SP [15:0]=0000h EP [15:0]=013Fh Default MADCTI's R5 - 0: EP [15:0]=013Fh	Ü													
Status Default Value	Availability													
Status Default Value					Partial	ivioae O			Sieep Out					
Power On Sequence SP [15:0]=0000h EP [15:0]=013Fh Default If MADCTL's R5 = 0: EP [15:0]=013Fh	Sieep III Tes													
Power On Sequence SP [15:0]=0000h EP [15:0]=013Fh Default If MADCTL's R5 = 0: EP [15:0]=013Fh														
Default If MADCTI 's B5 - 0: EP [15:0]-013Eh														
Delault	Dofoult			Po	wer On Sequence	SP[15:0]=000				-D [4 - 0]	0.105		
SW Reset SP [15:0]=0000h If MADCTL's B5 = 1: EP [15:0]=00EFh	Derauit				SW Reset			JOh If	MADCTL's	B5 = 1: E				
HW Reset SP [15:0]=0000h EP [15:0]=013Fh					HW Reset	SP[15:0]=000	00h E	P [15:0]=01	13Fh				









8.2.22. Memory Write (2Ch)

2Ch						RAMWI	R (Memory	Write)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	0	1	0	1	1	0	0	2Cł	
1 st Parameter	1	1	1		•		D1	[17:0]					XX	
:	1	1	1				Dx	[17:0]					XX	
N th Parameter	1	1	1				Dn	[17:0]					XX	
Description	status. Page p	When cositions in frame	this com	to transfer da mand is accep art Column/Sta and the colur care.	oted, the c	olumn r	egister and	I the page	e register dance wit	are rese	t to the S	Start Colu	mn/Sta	
Restriction	In all c	olor mo	des, ther	e is no restricti	on on leng	th of pa	rameters.							
Register Availability				Norm Part	al Mode C al Mode O	on, Idle M	Mode Off, S Mode On, S Mode Off, S Mode On, S	Sleep Out leep Out		6 6 8				
Default	Status Default Value Power On Sequence Contents of memory is set randomly SW Reset Contents of memory is not cleared HW Reset Contents of memory is not cleared													
Flow Chart			/ 2 3 4 4 1 2 3 3 4 4	st Parameter: \$ nd Parameter: Ith Parameter: \$ st Parameter: St Parameter: \$ st Parameter: \$ st Parameter: \$ st Parameter: \$ d Parameter: \$ st	GC[15:8] SC[7:0] EC[15:8] [[7:0] (2Bh) (2Bh) (2Ch) (2Ch)			- If Needec		Comi Paral Disp	tion	7		





8.2.23. Color Set (2Dh)

2Dh		•				RGBSE	T (Color :	Set)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	1	1	0	1	2Dh
1 st Parameter	1	1	1	XX	0	0		•	R00	[5:0]			XX
n th Parameter	1	1	1	XX	0	0			Rnn	[5:0]			XX
32 nd Parameter	1	1	1	XX	0	0			R31	[5:0]			XX
33 rd Parameter	1	1	1	XX	0	0			G00	[5:0]			XX
n th Parameter	1	1	1	XX	0	0			Gnn	[5:0]			XX
96 th Parameter	1	1	1	XX	0	0			G64	[5:0]			XX
97 th Parameter	1	1	1	XX	0	0			B00	[5:0]			XX
n th Parameter	1	1	1	XX	0	0			Bnn	[5:0]			XX
128 th Parameter	1	1	1	XX	0	0			B31	[5:0]			XX
Description	128 by	tes mus ommand	t be writt	to define the LU en to the LUT re effect on other o mory is written t	egardless	of the co	lor mode.	Only the	values in				s effect
Restriction													
						Status			Availab	lity			
				Norma	I Mode O	n, Idle Mo	de Off SI	een Out	Yes	iity			
Register						n, Idle Mo		•	Yes				
Availability						n, Idle Mo			Yes				
Availability													
								Jop Gut					
Default	Partial Mode On, Idle Mode On, Sleep Out Yes												
Flow Chart	HW Reset Random values RGBSET (2Dh) Command 1st Parameter: R00[5:0] : 32nd Parameter: R31[5:0] 33rd Parameter: G00[5:0] : 96th Parameter: G63[5:0] 97th Parameter: B00[5:0] : 128th Parameter: B31[5:0] Mode Sequential transfer												

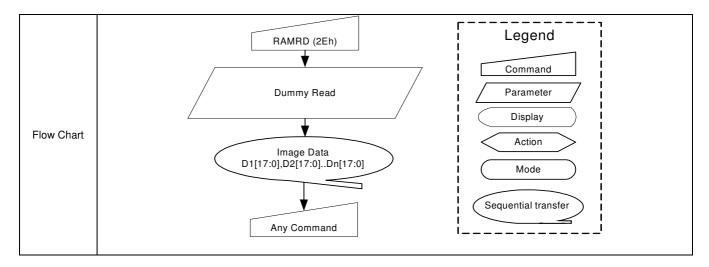




8.2.24. Memory Read (2Eh)

8.2.24. I	Memo	ry Ke	aa (2	⊏ ⊓)											
2Eh						RAMRE	(Memory	Read)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	0	0	1	0	1	1	1	0	2Eh		
1 st Parameter	1	1	1	XX	X	X	Х	X	X	X	X	Х	Х		
2 nd Parameter	1	1	1				D.	1 [17:0]					XX		
: *h	1	1	1				D	k [17:0]					XX		
(N+1) th Parameter	1	1	1				Dr	n [17:0]					XX		
	This co	ommano	transfe	rs image data	from ILI9	341's fra	ame memo	ry to the	host prod	cessor sta	irting at tl	ne pixel l	ocation		
	specifi	ed by pr	eceding	set_column_ac	ldress and	l set_pag	je_address	comman	ds.						
	If Mem	ory Acc	ess conti	rol B5 = 0:											
				egisters are re							-				
		-		SP). The colu	_				-			-			
		_	-	the End Colu e read from the				_							
					i name m	eniory u	illi tile pag	e register	equais ti	ie Liiu i a	ige (Li) (raide of the	ie nost		
Description	proces	sor send	ds anoth	er command.											
	If Mem	If Memory Access Control B5 = 1:													
	The co	If Memory Access Control B5 = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from													
	frame	memory	at (SC,	SP). The page	register is	s then in	cremented	and pixel	s read fro	m the frai	me memo	ry until th	e page		
	registe	r equals	the End	d Page (EP) va	alue. The p	page reg	ister is the	n reset to	SP and	the colum	ın register	is increr	nented.		
	Pixels	are read	d from th	e frame memo	ry until the	column	register ed	uals the	End Colur	mn (EC) v	alue or th	e host pro	cessor		
	sends	another	commar	nd.											
Restriction	There	s no res	striction o	on length of par	ameters.										
<u> </u>															
						Status	3		Availab	ility					
				Norm	al Mode O	n, Idle M	lode Off, SI	eep Out	Yes						
Register				Norm	al Mode O	n, Idle N	lode On, SI	eep Out	Yes						
Availability				Partia	al Mode Oi	n, Idle M	ode Off, Sle	eep Out	Yes						
				Partia	al Mode Oi	n, Idle M	ode On, Sle	eep Out	Yes						
						Sleep	n		Yes						
					Status		Г	Default Va	lue						
D-4				Power	On Seque	ence C	ontents of			omly					
Default					W Reset		ontents of			•					
					IW Reset		ontents of								
							<u> </u>								









8.2.25. Partial Area (30h)

8.2.25.	Partia	Partial Area (30h) PLTAR (Partial Area)													
30h						PLTAR	(Partial	Area)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	0	0	1	1	0	0	0	0	30h		
1 st Parameter	1	1	1	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00		
2 nd Parameter	1	1	1	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00		
3 rd Parameter	1	1	1	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01		
4 th Parameter		1	1 1 "	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	3F		
	I his c	ommano	defines	the partial mod	ie's displi	ay area.	There are	e 2 paran	neters as	sociated	with this	command	, the first		
	defines	s the Sta	art Row	(SR) and the se	cond the	End Row	(ER), as	illustrate	d in the fi	igures be	low. SR a	and ER re	fer to the		
	Frame	Memory	/ Line Po	ointer.											
	If End	Row>St	art Row	when MADCTL	B4=0:-										
				Start Row _						‡ 、					
				SR[15:0] →						+					
				-						Ŧ (Partial				
				_						‡ (Area				
				End Row -											
				ER[15:0] ->						+ -					
				-											
	If End	If End Row>Start Row when MADCTL B4=1:-													
				_											
				End Row _						-					
				ER[15:0] →						\perp					
Description				_							Partial				
,				<u>-</u>						\pm \nearrow	Area				
			;	Start Row -	+					-					
				SR[15:0] →						T /					
				_											
				_											
	If End	Row <st< td=""><td>art Row</td><td>when MADCTL</td><td>B4=0:-</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></st<>	art Row	when MADCTL	B4=0:-										
				_											
				-						+ \					
				End Row -						\top \succ	Partial Area				
				ER[15:0] ->_						上 ノ	, a oa				
				_											
				Start Row -						 					
				SR[15:0] →						\pm	Partial				
				_						<u> </u>	Area				
				_						\pm $^{\prime}$					
	If End	Row = S	Start Row	then the Partia	l Area will	be one r	ow deep.								
	X = Do	n't care.													
Restriction	SR [15	0] and	ER [15	0] cannot be (0000h nor	exceed (013Fh.								





Register	Status Availability
Register	
Register	I Normal Mode On Idle Mode Off Sleen Out I Voc I
	Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes
	Partial Mode On, Idle Mode Off, Sleep Out Yes
Availability	Partial Mode On, Idle Mode On, Sleep Out Yes
	Sleep In Yes
	Gloop III
Default	Default Value SR [15:0] ER [15:0] Power On Sequence 16'h0000h 16'h013Fh SW Reset 16'h 0000h 16'h 013Fh HW Reset 16'h 0000h 16'h 013Fh
	1 To Enter Partial Mode
	1st Parameter: SR[15:8] 2nd Parameter: SR[7:0] Parameter 3rd Parameter: ER[15:8] 4th Parameter: ER[7:0] Action Mode PTLON(12h) Partial Mode 2. To Leave Partial Mode
Flow Chart	Partial Mode Legend NORON(13h) Parameter Display Action Mode RAMRW(2Ch) Sequential transfer





8.2.26. Vertical Scrolling Definition (33h)

33h					VSCRDE	F (Vertic	al Scrolli	ng Defini	tion)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0 0 1 1 0 0 1 1 3 TFA [15:8]										
1 st Parameter	1	1	1	XX	TFA [15:8]										
2 nd Parameter	1	1	1	XX				TFA	[7:0]				00		
3 rd Parameter	1	↑	1	XX				VSA	[15:8]				01		
4 th Parameter	1	1	1	XX				VSA	[7:0]				40		
5 th Parameter	1	1	1	XX				BFA	[15:8]				00		
6 th Parameter	1	1	1	XX				BFA	[7:0]				00		

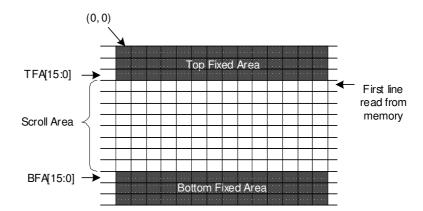
This command defines the Vertical Scrolling Area of the display.

When MADCTL B4=0

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Description

When MADCTL B4=1

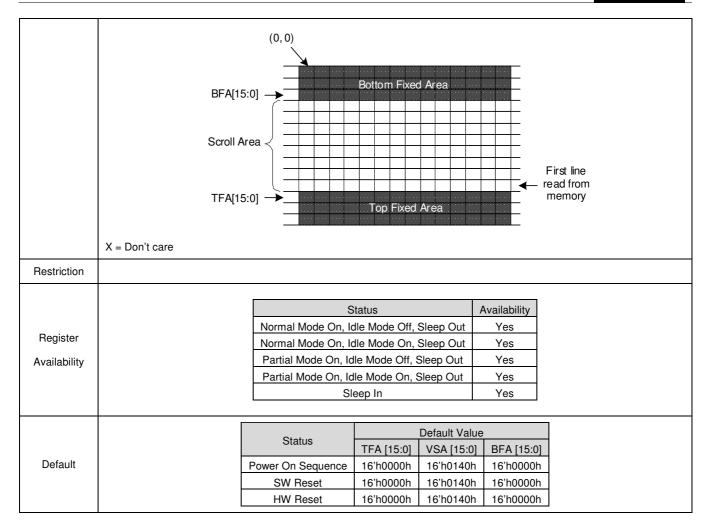
The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

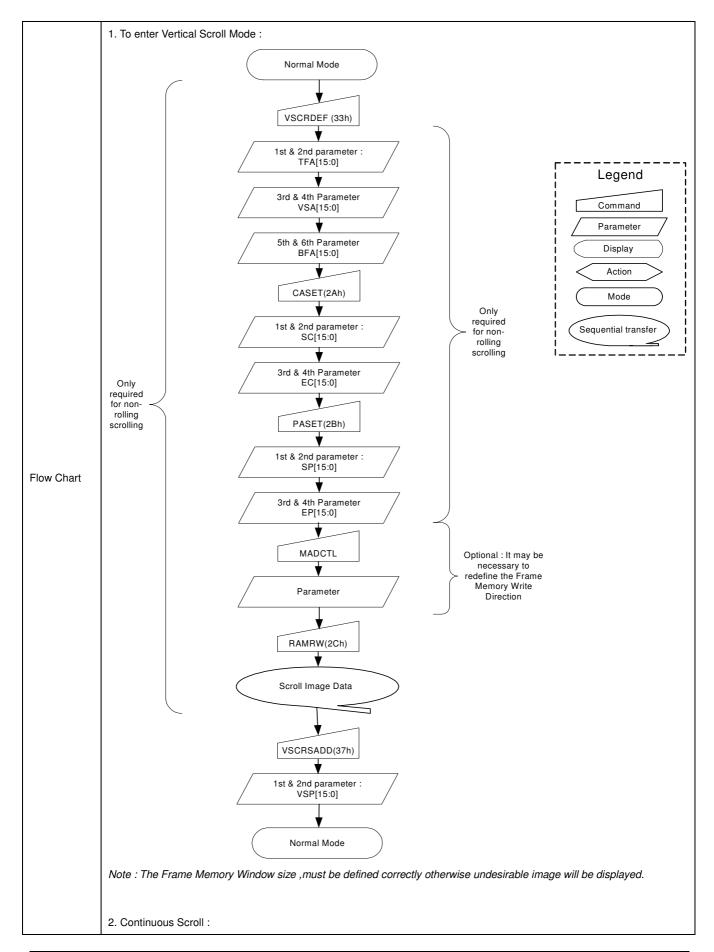
The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



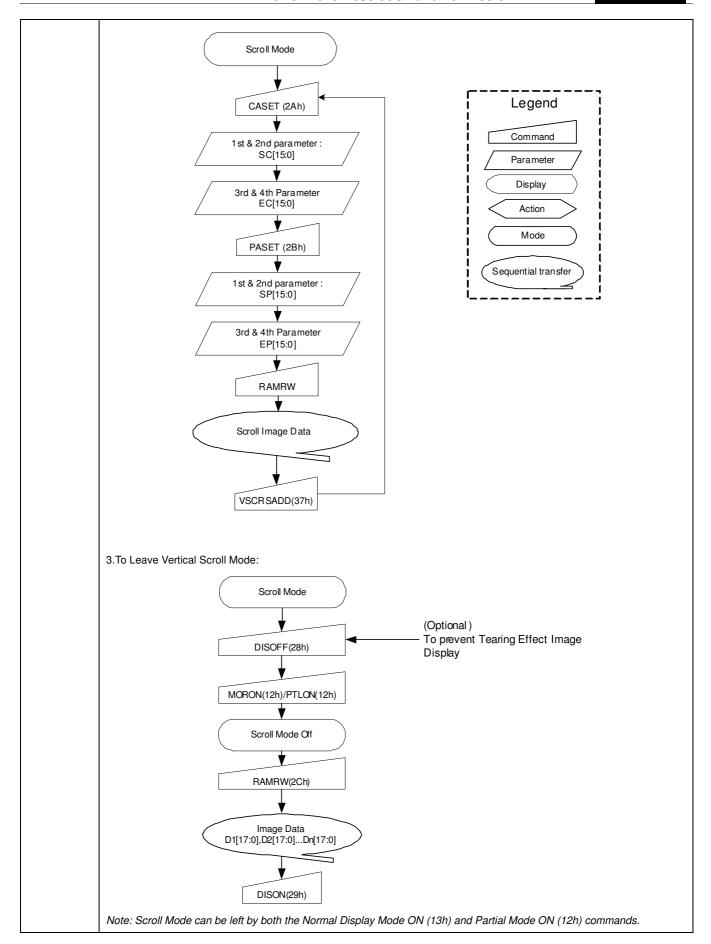
















8.2.27. Tearing Effect Line OFF (34h)

34h						TEOF	F (Tearin	g Effect	Line OFF	-)					
	D/CX	RDX	WRX	D1	7-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	Х	X	0	0	1	1	0	1	0	0	34h	
Parameter							No P	arameter							
Description		mmand n't care.		to turn O	FF (Activ	e Low) the	e Tearing	Effect ou	tput signa	al from the	TE signa	al line.			
Restriction	This co	mmand	has no e	effect whe	en Tearin	g Effect o	utput is a	lready OF	F.						
Register Availability					Normal Partial	Mode On	Status n, Idle Moo n, Idle Moo n, Idle Moo n, Idle Moo Sleep In	de On, Sle de Off, Sle	eep Out	Availabil Yes Yes Yes Yes	ity				
Default		Status Default Value Power On Sequence OFF SW Reset OFF HW Reset OFF													
Flow Chart					TEOF	Output O F(34h) V Output OF			C Pro	egend ommand arameter Display Action Mode					



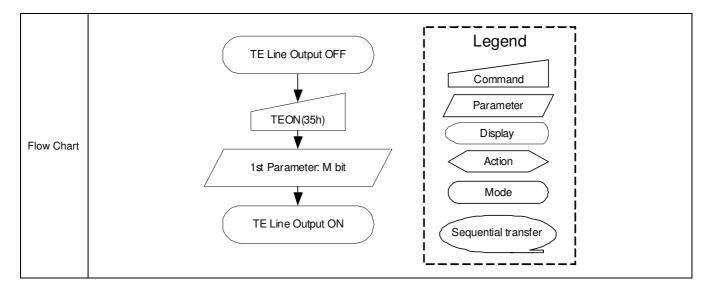


8.2.28. Tearing Effect Line ON (35h)

35h					TEO	N (Tearin	g Effect	Line ON)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	0	1	1	0	1	0	1	35h	
Parameter	1	1	↑	XX	0	0	0	0	0	0	0	М	00	
	changi Output	ng MAD Line.		to turn ON the T	_	-	_		_		-		-	
	When I	M=0:												
	The Te	aring Ef	fect Outp	out line consists of	V-Blankii	ng informa	ation onl	y:						
Description	When M=1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information: tvdl Vertical Time Scale Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low. X = Don't care.													
	X = Do	n't care.												
Restriction	This co	mmand	has no e	effect when Tearin	g Effect o	utput is a	Iready O	N						
Register Availability	This command has no effect when Tearing Effect output is already ON Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Sleep In Yes													
Default					Power	Status On Seque W Reset W Reset		Oefault Val OFF OFF OFF	lue					











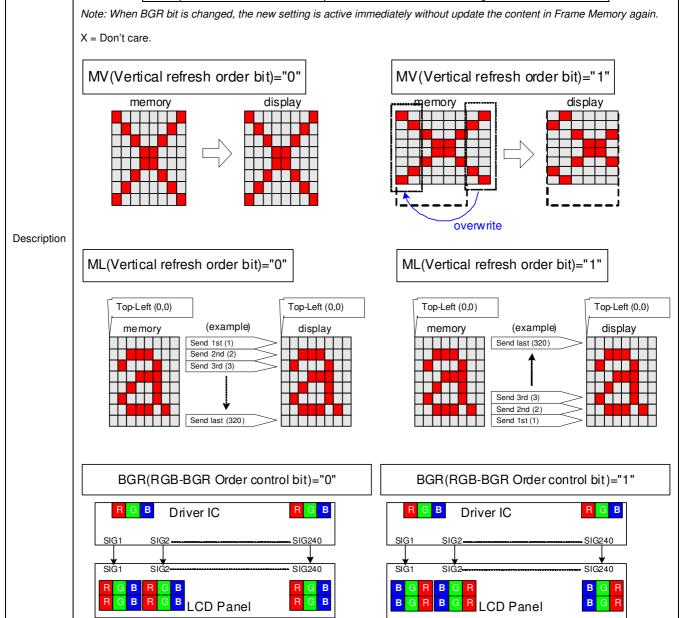
8.2.29. Memory Access Control (36h)

36h				MA	DCTL (N	lemory A	Access	Control							
	D/CX	CX RDX WRX D17-8 D7 D6 D5 D4 D3 D2 D1 D0 HEX													
Command	0	1	1	XX	0	0	1	1	0	1	1	0	36h		
Parameter	1	1	1	XX	MY	MX	MV	ML	BGR	MH	0	0	00		

This command defines read/write scanning direction of frame memory.

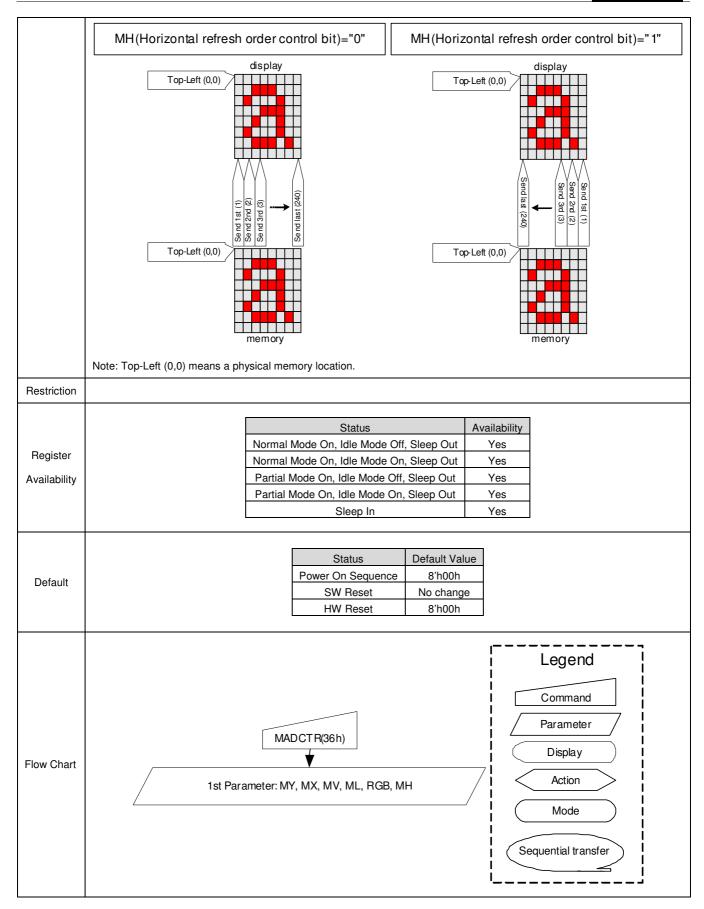
This command makes no change on the other driver status.

Bit	Name	Description
MY	Row Address Order	
MX	Column Address Order	These 3 bits control MCU to memory write/read direction.
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control
ban	NGB-BGN Older	(0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.













8.2.30. Vertical Scrolling Start Address (37h)

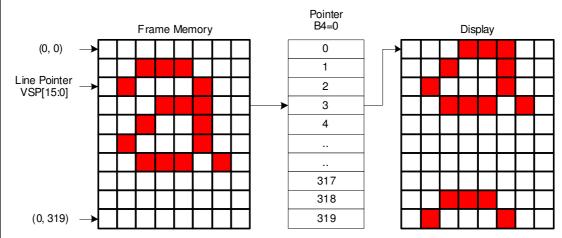
37h				VS	CRSADI	O (Vertica	l Scrollin	g Start A	ddress)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0 0 1 1 0 1 1 3										
1 st Parameter	1	↑	1	XX				VSP	[15:8]				00		
2 nd Parameter	1	1	1	XX	VSP [7:0] 00										

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL B4=0

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.

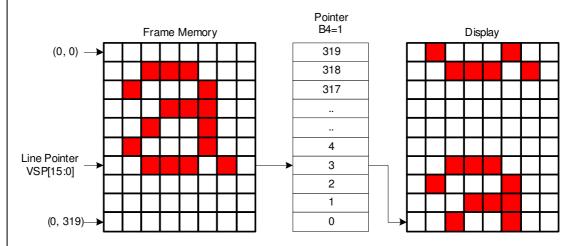


Description

When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.



Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan

to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

(2) This command is ignored when the ILI9341 enters Partial mode.

X = Don't care





Restriction					
			Status		Availability
		Norm	al Mode On, Idle Mode (Off, Sleep Out	Yes
Register		Norm	al Mode On, Idle Mode O	On, Sleep Out	Yes
Availability		Partia	al Mode On, Idle Mode C	Off, Sleep Out	No
_		Partia	al Mode On, Idle Mode C	n, Sleep Out	No
			Sleep In		Yes
			Status	Default Val	ue
			Status	VSP [15:0)]
Default			Power On Sequence	16'h0000l	1
			SW Reset	16'h0000l	ı
			HW Reset	16'h0000l	า
Flow Chart	See Vertical Scrolling Definition	(33h)	description.		





8.2.31. Idle Mode OFF (38h)

38h					IDM	OFF (Idle	Mode O	FF)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	0	0	1	1	1	0	0	0	38h		
Parameter						No Para	ameter								
	This cor	mmand is ι	used to red	over from Idl	e mode o	n.									
Description	In the id	le off mode	e, LCD car	n display max	imum 262	2,144 colo	rs.								
'	X = Don														
Restriction	This cor	nmand has	s no effect	when modul	e is alreac	dy in idle o	ff mode.								
						Status			Availabili	ty					
Register						dle Mode			Yes						
						dle Mode			Yes						
Availability						dle Mode (Yes Yes						
		Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes													
		Sieep III Tes													
						atus		ult Valu							
Default						Sequence		node OF							
						Reset Reset		node OF node OF							
						10001	Tale II	1000 01	<u>. </u>						
						_	ı				7				
							-	Le	egend		į				
			(Idle mod	de on		į,				!				
							I	Co	mmand		į				
							! /	/ Pa	rameter						
									isplay	=	!				
Flow Chart]		льргау	/	i				
				IDMOFF(38h)					Action	\geq	 				
							 		Mada		į				
						_	! '		Mode						
								0	4:-14		1				
			(Idle mod	de off		- (Sequer	ntial trans	ier	į				
							i				1				
İ	I					_									



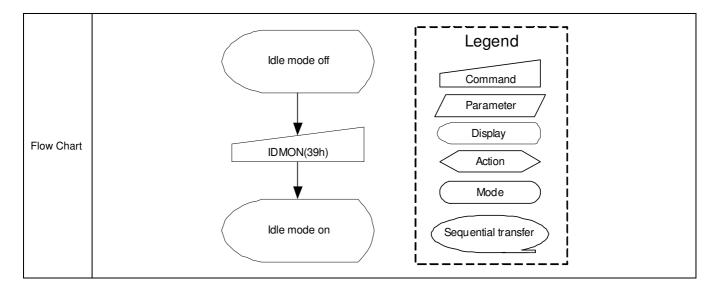


8.2.32. Idle Mode ON (39h)

39h				-		IDMON	(Idle Mo	de ON)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑ ↑	XX	0	0	1	1	1	0	0	1	39h	
Parameter							Paramet					<u> </u>		
	This co	mmand	is used t	o enter into Idle	e mode on									
	In the i	dla an n	anda anlı	or expression is	roduced	The prim	on, and t	ha aaaand	arı, oolor	uning MC	'P of oooh	D C and	N D in the	
				•		rne prim	ary and t	ne seconda	ary colors	s using ivis	ob oi eacii	i K, G and	ı b in the	
	Frame	Memory	, 8 color	depth data is d	lisplayed.									
				Memory					F	Panel Di	splav			
						_								
						_								
						_	1	_						
		-				_		> -						
December						_	L	_						
Description						_								
						_								
						_								
											_			
							Gr Gr G	Display Co	lor B _c B ₄	B ₀ B ₀ B ₄ B	lo.			
		R ₅ R ₄ R ₃ R ₂ R ₁ R ₀ G ₅ G ₄ G ₃ G ₂ G ₁ G ₀ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀ Black 0XXXXX 0XXXXX 0XXXXXX												
				Blue	0XXX 1XXX			XXXX		XXXXX				
				Red Magenta	1XXX			XXXX		XXXXX				
				Green	0XXX	XX	1X	XXXX	02	XXXXX				
				Cyan Yellow	0XXX 1XXX			XXXX		XXXXX				
				White	1XXX			XXXX		XXXXX				
	X = Do	n't care.												
Destriction	This so		h		dl.a. :a. alua		"	1_						
Restriction	This co	mmana	nas no e	effect when mod	dule is aire	ady in idi	e on mod	ie.						
						Ctatur	-		A	L :11:4				
				Norn	nal Mode C	Status		Sloop Out	Availal Ye:					
Register					nal Mode C	,	,		Yes					
Availability					ial Mode C				Yes					
Availability					ial Mode C				Ye					
						Sleep			Ye					
						Ctatus		Dofordt \/-	luo					
					Power	Status r On Sequ	ience l	Default Va						
Default						SW Rese		dle mode (
						HW Rese		dle mode (











8.2.33. COLMOD: Pixel Format Set (3Ah)

3Ah	PIXSET (Pixel Format Set)															
SAII					_		T		Т	1			T _	I _	Ι -	1
0	D/CX	RDX	WRX		D17		D7	D6	D5		D4	D3	D2	D1	D0	HEX
Command Parameter	0 1	1	<u>↑</u>		XX XX		0	0	1 DPI [2	01	1	0	0	DBI [2:0	0	3Ah 66
Farameter				ivali				ao data	•		intor	rface. DPI [2	·01 ic tho			•
			•					_	-			_	_	•		
	interface	e and DB	II [2:0] is	the p	pixel f	ormat c	of MCU int	erface. I	f a parti	cular	inte	rface, either	RGB int	erface or	MCU inte	rface, is
	not used	d then the	e corresp	ondi	ing bit	s in the	paramete	er are igr	ored. T	ne pi	xel f	ormat is sho	wn in the	e table be	low.	
			I	OPI [2:0]	RGB	Interface I	Format	DE	31 [2:0	0]	MCU Interf	ace Forn	nat		
			0	0	0		Reserved		0	0	0		erved			
			0	_			Reserved		0	0	1		erved			
Description			0				Reserved		0	1	0		erved erved			
			1				Reserved		1	0	0		erved			
			1			1	6 bits / pix		1	0	1		/ pixel			
			1	1	0	1	8 bits / pix	cel	1	1	0	18 bits	/ pixel			
			1	1	1		Reserved	ł	1	1	1	Rese	erved			
	If using	RGB Inte	erface mi	ust s	electio	on seria	l interface).								
	X = Don	't care														
Restriction																
		Status Availability														
					No	ormal M	lode On, I		Off, SI	eep (Out	Yes				
Register					No	rmal M	lode On, I	dle Mode	On, SI	еер (Out	Yes				
Availability							ode On, Id					Yes				
					Pa	artial M	ode On, Id		On, Sle	ep C	Dut	Yes				
							5	leep In				Yes				
										D	efau	ılt Value				
					St	tatus			DPI [2:				BI [2:0]			
Default			Po	wer (On Se	quence)		3'b110				b110			
						Reset		١	No Char				Change			
					HW	Reset			3'b110)] 3	'b110			
										Г				!		
										1		Leger	nd	- !		
						COLI	MOD (3Ah)			٢	Comma	nd	-		
														.		
				_						İ	L	Parame	ter	 		
Flow Chart							GB pixel fo			į	(Display)	-		
. ion onar			/	/	DB	I[2:0] M	CU pixel fo	ormat		į	<	Action	\rightarrow	-		
	Mode															
	₩ Mode															
					Γ	Anv	Command			į		Sequential tr	ansfer))		
					L	,				į				ĺ		
										١-				 '		





8.2.34. Write_Memory_Continue (3Ch)

3Ch	Write_Memory_Continue													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch	
1 St Dovementar	4	4		D1	D1	D1	D1	D1	D1	D1	D1	D1	000	
1 st Parameter	1	1	1	[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF	
X th Parameter	4	4		Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	000	
X Parameter	ļ	I	T	[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF	
Nth Davasatav	4			Dn	Dn	Dn	Dn	Dn	Dn	Dn	Dn	Dn	000	
N th Parameter	1	1	1	[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF	

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.

If set_address_mode B5 = 0:

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

If set_address_mode B5 = 1:

Description

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC - SC + 1) * (EP - SP + 1) the extra pixels are ignored.

Sending any other command can stop frame Write.

Frame Memory Access and Interface setting (B3h), WEMODE=0

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

Frame Memory Access and Interface setting (B3h), WEMODE=1

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

Restriction

A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.





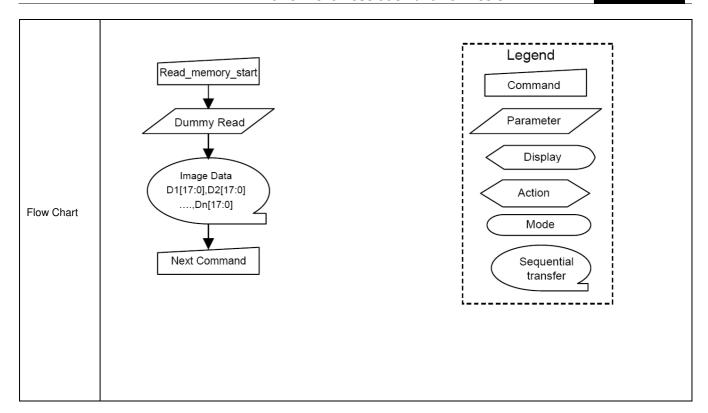
		Status		Availability	
	Non	mal Mode On, Idle Me	ode Off, Sleep Out	Yes	
Register	Non	mal Mode On, Idle Me	ode On, Sleep Out	Yes	
Availability	Par	tial Mode On, Idle Mo	ode Off, Sleep Out	Yes	
	Par	rtial Mode On, Idle Mo	de On, Sleep Out	Yes	
	Slee	ep In		No	
		Status	Default Val	III	
	P	ower On Sequence	Random va		
Default		W Reset	No chang		
		W Reset	No chang		
	<u> </u>	111111111111111111111111111111111111111	TTO OFFICE IS		
Flow Chart	Image Data D1[17:0],D2[17:0],Dn[17:0] Next Command			Pa	mmand rameter Display Action Mode Sequential transfer





		<u>j_</u>	J J 111111	ıe (3Eh)									
3Eh				ı	Read_		_Contin	ue	1 1		ı	ı	
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1		XX	0	0	1	1	1	1	1	0	3Eh
1 st Parameter	1	1	1	XX	Х	Χ	Х	Χ	Х	Χ	Х	Х	Х
2 nd Parameter	1	1	1	D1	D1	D1	D1	D1	D1	D1	D1	D1	000
	·	'		[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF
x st Parameter	1	1	1	Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	000
		'		[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF
N st Parameter	1	↑	1	Dn [178]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF
Description	If set_addre Pixels are re read_memore column regions incremented column regions If set_addre Pixels are re read_memore register equ Pixels are re equals the I	location following the previous read_memory_continue (3Eh) or read_memory_start (2Eh) command. If set_address_mode B5 = 0: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If set_address_mode B5 = 1: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command. This command makes no change to the other driver status.											
Restriction	A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined. Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Partial Mode On, Idle Mode Off, Sleep Out Yes												
Register Availability	location. Ot	nerwise, da	1	Normal Mode	Stat On, Idle On, Idle	us Mode C Mode C	n, Sleep	Out	Yes Yes	ty			
Register Availability	location. Of	nerwise, da	1	Normal Mode Normal Mode Partial Mode Partial Mode	Stat On, Idle On, Idle On, Idle On, Idle	Mode C Mode C Mode O	n, Sleep ff, Sleep n, Sleep	Out Out Out Out	Yes Yes Yes Yes Yes Yes	ty			
-	location. Of	nerwise, da	1	Normal Mode Normal Mode Partial Mode Partial Mode Sleep In	Stat On, Idle On, Idle On, Idle On, Idle	Mode C Mode C Mode O Mode O	n, Sleep ff, Sleep n, Sleep Defau	Out Out Out Out Out	Yes Yes Yes Yes Yes Yes Yes	ty			
-	location. Of	nerwise, da	1	Normal Mode Normal Mode Partial Mode Partial Mode	Stat On, Idle On, Idle On, Idle On, Idle	Mode C Mode C Mode O Mode O	n, Sleep ff, Sleep n, Sleep Defau Rand	Out Out Out Out	Yes Yes Yes Yes Yes Yes Yes	ty			









8.2.36. Set_Tear_Scanline (44h)

44h					Set	_Tear_S	canline						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
1 st Parameter	1	1	↑	XX	0	0	0	0	0	0	0	STS [8]	00
2 nd Parameter	1	1	1	XX	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	00
Description	The TE sign	nal is not a	ffected by of	ay Tearing E	_address	•		ne Tearii				e parame	
		et_tear_sc	anline with	STS=0 is equal be active					Sleep m	node.	/		
Restriction	-												
Register Availability				Normal Mode Normal Mode Partial Mode Partial Mode Sleep In	On, Idle	Mode C Mode C Mode O	n, Sleep	Out Out Out	Availabil Yes Yes Yes Yes Yes Yes Yes	ity			
Default				Star Power On SW Reset HW Reset		е	STS [8	ult Value 3:0]=000 3:0]=000 3:0]=000	0h 0h				
Flow Chart	TE Output On or Off Set_tear_scanline Parameter Parameter Display Action Mode TE Output On the Nth line Sequential transfer												





8.2.37. Get_Scanline (45h)

45h		Get_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	1	0	0	0	1	0	1	45h	
1 st Parameter	1	1	1	XX	X	Х	Х	Х	X	Х	X	Х	X	
2 nd Parameter	1	<u>†</u>	1	XX	0	0	0	0	0	0	GTS [9]	GTS [8]	00	
3 rd Parameter	1	1	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00	
Description	display devi	ice is defin	ed as VSYI	can line, GTS NC + VBP + \ eturned by ge	VACT + '	VFP. Th	e first sc	•						
Restriction	None													
					Sta	tus			Availabili	itv				
				Normal Mode			Off. Sleer		Yes	ity .				
Register				Normal Mode					Yes					
Availability				Partial Mode					Yes					
				Partial Mode					Yes					
				Sleep In	,		, ,		Yes					
Default				Power On S SW Reset HW Reset	e									
Flow Chart	get_scanline GTS [9:0]=0000h Legend Command Parameter Display Action Mode Send 2nd parameter GTS[7:0] Send 2nd parameter GTS[7:0]													





8.2.38. Write Display Brightness (51h)

51h					WR	DISBV (W	rite Displ	ay Brightr	ness)					
	D/CX	0 1 ↑ XX 0 1 0 1 0 0 0 1 51												
Command	0	1	1	XX	0	1	0	1	0	0	0	1	51h	
Parameter	1	1	1	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00	
Description	It should	be chec	ked what	is the rel	brightness ationship be ecification. value mean	etween thi	s written v	alue and o					ionship	
Restriction	None													
						Stat	us		Availab	oility				
				N	ormal Mod			Sleep Out						
Register					ormal Mod									
Availability					artial Mode									
				F	artial Mode	On, Idle	Mode On,	Sleep Out	Yes	3				
				S	leep In				Yes	3				
Default		Status Default Value DBV [7:0] Default Value Power On Sequence 8'h00h SW Reset 8'h00h HW Reset 8'h00h												
Flow Chart					DBV[70 New Displ Brightnes Value Load	lay		¥	Leger Comm Parame Displ Action Mod Seque trans	and ter ay on le ntial				





8.2.39. Read Display Brightness (52h)

52h				,	RDD	ISBV (Rea	ad Display	/ Brightne	ss Value)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	1	0	0	1	0	52h
1 st Parameter	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	Χ
2 nd Parameter	1	1	1	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00
Description	It shou	ld be ch	ecked w defined (hat the re	tness valu elationship splay modu at 00h valu	between t	his returne ation.		·			olay. This hest bright	ness.
Restriction	The display module is sending 2 nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI Mode. Only 2 nd parameter is sent on DSI (The 1st parameter is not sent).												
						St	atus		Avail	ability			
					Normal Mo			ff, Sleep O		es			
Register					Normal Mo					es			
Availability					Partial Mo					es			
					Partial Mo					es			
				:	Sleep In				Y	es			
Default					Power O	tatus n Sequenc Reset Reset	ce .	Default DBV 8'h0 8'h0	7:0] 0h 0h				
Flow Chart					Send	1 RDDISB 1 st Parame	Dis	<u>Host</u> play	Para D A See	egend mmand ameter risplay action Mode quential ransfer	7		



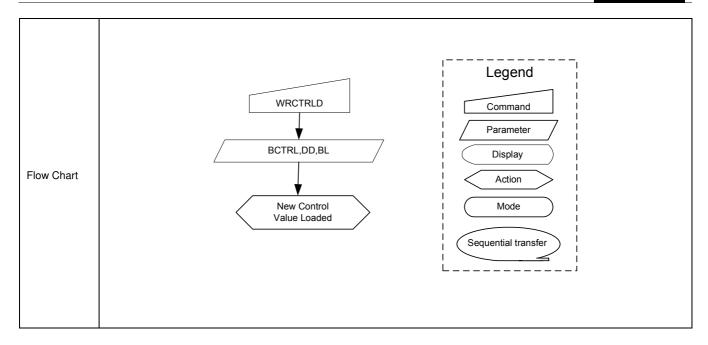


8.2.40. Write CTRL Display (53h)

53h				WR	CTRLD	(Write	Control Di	isplay)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	1	0	1	0	0	1	1	53h	
Parameter	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00	
	This command is used to control display brightness.													
	BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.													
	0 = Off (Brightness registers are 00h, DBV[70])													
			_			, to the	othor noron	matara \						
	1 = On (Brightness registers are active, according to the other parameters.)													
	DD : Display	/ Dimming,	only for ma	anual brightnes	ss setti	ng								
	DD = 0: Display Dimming is off													
	DD =	1: Display I	Dimming is	on										
Description	BL: Backlig	ht Control	On/Off											
				aaddiaht airau	it Cont	rol linos	must be le	· · · ·						
	0 = Off (Completely turn off backlight circuit. Control lines must be low.)													
	1 = On													
	Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 =													
	1 or $1 \rightarrow 0$.													
	When BL b	When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are												
	selected.													
Doctriction	None													
Restriction	None													
					Sta	ıtus		Α	vailabilit	у				
				Normal Mode (Off, Sleep		vailabilit Yes	у				
•				Normal Mode (On, Idle	Mode		Out		у				
•			١		On, Idle On, Idle	Mode Mode	On, Sleep	Out Out	Yes	у				
•			<u> </u>	Normal Mode (Partial Mode (Partial Mode (On, Idle On, Idle On, Idle	Mode Mode Mode (On, Sleep Off, Sleep O	Out Out Out	Yes Yes Yes Yes	у				
•			<u> </u>	Normal Mode (Partial Mode (On, Idle On, Idle On, Idle	Mode Mode Mode (On, Sleep Off, Sleep O	Out Out Out	Yes Yes Yes	у				
•			<u> </u>	Normal Mode (Partial Mode (Partial Mode (On, Idle On, Idle On, Idle	Mode Mode Mode (On, Sleep Off, Sleep On, Sleep O	Out Out Out Out Out	Yes Yes Yes Yes	у	1			
•			N	Normal Mode (Partial Mode (Partial Mode (On, Idle On, Idle On, Idle On, Idle	Mode Mode Mode Mode Mode Mode Mode Mode	On, Sleep Off, Sleep (On, Sleep (Defaul	Out Out Out Out Out Out	Yes Yes Yes Yes]			
Availability			1 5	Normal Mode (Partial Mode (Partial Mode (Sleep In	On, Idle On, Idle On, Idle On, Idle	Mode Mode Mode Mode Mode Mode Mode Mode	On, Sleep Off, Sleep On, Sleep On, Sleep Off	Out Out Out Out Out Out Out Out Out	Yes Yes Yes Yes Yes Yes	BL				
Register Availability Default			Power	Normal Mode (Partial Mode (Partial Mode (Sleep In Status On Sequence	On, Idle On, Idle On, Idle On, Idle	Mode Mode Mode Mode Mode Mode Mode Mode	On, Sleep (On, Sleep (On, Sleep (On, Sleep (Defaul	Out Out Out Out Out Out Out Out Out Out	Yes Yes Yes Yes Yes 1	BL //b0				
Availability			Power	Normal Mode (Partial Mode (Partial Mode (Sleep In	On, Idle On, Idle On, Idle On, Idle	Mode Mode Mode Mode Mode Mode Mode Mode	On, Sleep (On, Sl	Out Out Out Out Out Out Out Out Out	Yes Yes Yes Yes Yes 1 1 1	BL				









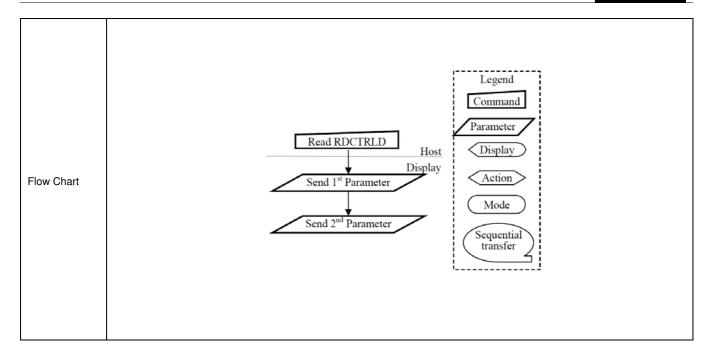


8.2.41. Read CTRL Display (54h)

54h	RDCTRLD (Read Control Display)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
1 st Parameter	1	↑	1	XX	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	XX
2 nd Parameter	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	00
	BCTRL : E	Brightness Off (Brightn	Control Blo			ing to th	e DBV[70] p:	aramet	ers.)				
Description	DD: Display Dimming '0' = Display Dimming is off '1' = Display Dimming is on												
	BL: Backlight On/Off '0' = Off (Completely turn off backlight circuit. Control lines must be low.) '1' = On												
Restriction	The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.												
				DBI. DSI (The 1st p	parame	eter is no	ot sent).						
Register Availability				Normal Mode Normal Mode Partial Mode	e On, lo	Status dle Mod dle Mod	e Off, Sleep Ce On, Sleep Ce Off, Sleep Oe On, Sleep Oe On, Sleep Oe On, Sleep O	Out Out Out	Yes Yes Yes Yes Yes Yes Yes Yes				











8.2.42. Write Content Adaptive Brightness Control (55h)

55h	WRCABC (Write Content Adaptive Brightness Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	1	0	1	0	1	55h
Parameter	1	1	<u> </u>	XX	0	0	0	0	0	0	C [1]	C [0]	00
				parameters				•				-	ble
Description				0.1	1:0]	Г	Default \	/alua					
						L							
					000		Off		_				
					001	Usei		ce Imag	В				
					010		Still Pic						
				21	011		Noving I	mage					
Restriction	None												
					ç	Status			Ava	ilability	1		
			•	Normal Mod			e Off. S	leep Ou		Yes			
Register			•	Normal Mod						Yes			
Availability			•	Partial Mod						Yes			
,			-	Partial Mod						Yes	1		
			•	Sleep In			, -			Yes	1		
Default				Power On SW	Sequer Reset Reset	nce		Default V C [1:0]=0 C [1:0]=0 C [1:0]=0	00h 00h				
Flow Chart				Ist parame New A Image	daptive		7		<u></u>	Leger Comm Parame Displ Action Mod Seque trans	lay on le ontial		





8.2.43. Read Content Adaptive Brightness Control (56h)

	RDCABC (Read Content Adaptive Brightness Control)												
56h	D/CV	DDV									D1		LIEV
Command	D/CX	RDX	WRX	D17-8 XX	D7	D6	D5	D4	D3	D2	D1	D0	HEX 56h
1 st Parameter	1	1	1	XX	0 X	1 X	0 X	1 X	0 X	1 X	1 X	0 X	XX
2 nd Parameter	1	<u> </u>	1	XX	0	0	0	0	0	0	C [1]	C [0]	00
				he settings f	_			-	_			-	w.
Description				С	[1:0]	[Default V	/alue					
				2'	b00		Off						
					b01			e Image					
					b10		Still Pict						
				2'	b11	N.	loving Ir	mage					
Restriction	(= more th	nan 2 RDX	cycle) on [2nd paramet DBI. DSI (The 1st				s if the N	1CU war	nts to rea	ad more tl	han one p	arameter
					St	atus			Availa	bility			
				Normal Mod			Off, Sle	ep Out	Ye				
Register				Normal Mod	e On, Idl	e Mode	On, Sle	ep Out	Ye	es .			
Availability				Partial Mode	On, Idle	e Mode	Off, Slee	ep Out	Ye	s			
				Partial Mode	On, Idle	e Mode	On, Slee	ep Out	Ye	s			
			_ :	Sleep In					Ye	S			
Default						ce	C	efault Va [1:0]=00 [1:0]=00)h)h				
Flow Chart				Read R Send 1 st I	Parame	eter	H Disp	ost lay	Par D	egendomman ameter Display Action Mode equenting	d > > > al		





8.2.44. Write CABC Minimum Brightness (5Eh)

5Eh	Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	1	1	1	1	0	5Eh
Parameter	1	1	1	XX	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00
	This cor	nmand is	s used to	set the mir	nimum brig	htness va	lue of the	display for	CABC fur	nction.			
	CMB[7:	0]: CABC	minimum	n brightnes	s control,	this param	eter is use	ed to avoic	l too much	brightne	ss reduction	on.	
	When C	ABC is a	active, CA	BC canno	t reduce t	he display	brightnes	s to less t	han CABO	minimur	m brightne	ss setting	. Image
	process	ing functi	ion is wor	ked as nor	mal, even	if the brigi	ntness car	not be ch	anged.				
Description	This fur	nction do	es not af	fect to the	other fun	ction, mar	nual bright	tness setti	ng. Manu	al brightn	ess can b	e set the	display
Description	brightne	orightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.											
	When c	When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is											
	ignored.	gnored.											
	In princ	iple rela	tionship is	s that 00h	n value m	eans the	lowest br	ightness f	or CABC	and FFh	value m	eans the	highest
	brightne	ss for CA	ABC.										
						Statu	S		Availab	ility			
				Nor	mal Mode	On, Idle M	lode Off, S	Sleep Out	Yes	i			
Register				Nor	mal Mode	On, Idle M	lode On, S	Sleep Out	Yes	i			
Availability				Par	tial Mode	On, Idle M	ode Off, S	Sleep Out	Yes	i			
				Par	tial Mode	On, Idle M	ode On, S	Sleep Out	Yes				
				Slee	ep In				Yes	i			
					Stat	tus		Default Va	alue				
		CMB [7:0]											
Default				<u> </u>	Power On	Sequence		8'h00h	l				
					SW Reset No Change								
1					HW F	Reset		8'h00h	<u> </u>				





8.2.45. Read CABC Minimum Brightness (5Fh)

5Fh		Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	1	0	1	1	1	1	1	5Fh	
1 st Parameter	1	1	1	XX	Х	Χ	Χ	Х	Х	Х	X	Х	Χ	
2 nd Parameter	1	1	1	xx	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00	
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (5Eh)" command. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. Status Availability													
				Norr	nal Mode	On, Idle M	lode Off, S	Sleep Out	Yes	3				
Register				Norr	nal Mode	On, Idle M	lode On, S	Sleep Out	Yes	3				
Availability				Part	ial Mode (On, Idle M	ode Off, S	Sleep Out	Yes	3				
				Part	ial Mode (On, Idle M	ode On, S	Sleep Out	Yes	3				
				Slee	p In				Yes	;				
					Sta	tus		Default Va						
						_		CMB [7:						
Default				<u> </u>		Sequence)	8'h00h		_				
					SW F			No Chan		_				
					HW F	Reset		8'h00h	1					





8.2.46. Read ID1 (DAh)

DAh						RDID1 (F	Read ID1)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	0	1	1	0	1	0	DAh
1 st Parameter	1	1	1	XX	Χ	X	Χ	Χ	X	Χ	Х	Χ	Х
2 nd Parameter	1	1	1	XX					[7:0]				00
Description	The 1 st pa	aramete aramete	r is dumr	ne LCD module's r my data. r module's manufa			nd it is s	pecified	by User				
Restriction													
Register Availability				Normal Mo Normal Mo Partial Mo Partial Mo	ode On, ode On, de On, I de On, I	ldle Mode dle Mode	On, Sle	ep Out ep Out	Availabi Yes Yes Yes Yes	lity			
Default				Status Power On Seque SW Reset HW Reset		Before MT 8'h 8'h	00h 00h	am) (A	MTP v	program alue alue)		
Flow Chart	Power On Sequence 8'h00h MTP value SW Reset 8'h00h MTP value										F	Legend Command Parameter Display Action Mode	ster





8.2.47. Read ID2 (DBh)

DBh						RDID2	(Read ID	2)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	0	1	1	0	1	1	DBh
1 st Parameter	1	1	1	XX	Х	X	Х	Χ	X	Х	Х	Х	Х
2 nd Parameter	1	1	1	XX					2 [7:0]				00
Description	changes The 1 st pa	each tin aramete aramete can be p	ne a revis r is dumi er is LCD	track the LCD not sion is made to my data. module/driver med by MTP fun	the displa	ay, materia	al or const	ruction s	specification	ons.		greement) and
Restriction													
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes											
Default				Status Power On Se SW Res HW Res	quence et	(Before I	ault Value MTP prog 3'h80h 3'h80h		Default After MTP v MTP v MTP v	program) /alue /alue			
Flow Chart						DBh) Jummy Reac					Pa D	egend rameter risplay Action Mode	7





8.2.48. Read ID3 (DCh)

DCh						RDID	3 (Read I	D3)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	0	1	1	1	0	0	DCh
1 st Parameter	1	1	1	XX	Х	Х	X	Χ	X	Х	Х	X	Х
2 nd Parameter	1	1	1	XX					3 [7:0]				00
Description Restriction	The 1 st The 2 ^{nt} The ID	parame	eter is du	s the LCD modul mmy data. CD module/drive mmed by MTP fu	r ID.	nd It is sp	ecified by	User.					
Register Availability				bility B B B B B B									
Default					equence				(After MTF MTP MTP	value value)		
Flow Chart	SW Reset 8'h00h MTP value HW Reset 8'h00h MTP value Legend Command Parameter Driver Display Action Action Mode Sequential transf												



8.3. Description of Level 2 Command

8.3.1. RGB Interface Signal Control (B0h)

B0h					IFMODE (Inte	erface M	ode Cor	ntrol)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HE	
Command	0	1	↑	XX	1	0	1	1	0	0	0	0	B0ł	
Parameter	1	1	↑	xx	ByPass_MODE	RCM [1]	RCM [0]	0	VSPL	HSPL	DPL	EPL	40	
	Sets th	e operat	ion statu	us of the display	interface. The sett	ing beco	mes effe	ective as	soon as	the comn	nand is i	received		
	EPL: D	E polari	ty ("0"= I	High enable for I	RGB interface, "1"=	Low en	able for	RGB inte	erface)					
	DPL: D	OTCLK	polarity	set ("0"= data fe	tched at the rising	time, "1"	'= data fe	etched at	t the fallin	ng time)				
	HSPL:	HSPL: HSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)												
	VSPL: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)													
5	RCM [RCM [1:0]: RGB interface selection (refer to the RGB interface section).												
Description														
	ByPas	ByPass_MODE: Select display data path whether Memory or Direct to Shift register when RGB Interface is used.												
			Γ	ByPass_MODE	:	Disp	olay Data	a Path			1			
				0	Di	rect to SI	hift Regis	ster (def	ault)					
				1			Memor	у						
Doctriction	EVIC	ما ما ما ما	a biab ta	anabla thia aan	nmand									
Restriction	EXIC	snould b	e nign to	enable this cor	nmana									
					Status				vailability					
				Normal	Mode ON, Idle Mo	de OFF,			Yes					
Register	Normal Mode ON, Idle Mode ON, Sleep OUT Yes													
Register				Norma										
Register Availability				Norma Partial	Mode ON, Idle Mo Mode ON, Idle Mo	de OFF, de ON,	Sleep O	UT	Yes Yes					
-				Norma Partial	Mode ON, Idle Mo	de OFF, de ON,	Sleep O	UT	Yes					
_				Norma Partial	Mode ON, Idle Mo Mode ON, Idle Mo	de OFF, de ON,	Sleep O	UT	Yes Yes					
_				Norma Partial Partial	Mode ON, Idle Mo Mode ON, Idle Mo Sleep I	de OFF, ode ON, S N	Sleep Ol Sleep Ol Default	UT UT Value	Yes Yes Yes					
Availability			Power	Norma Partial Partial	Mode ON, Idle Mo Mode ON, Idle Mo Sleep I	de OFF, ode ON, N	Sleep Ol Sleep Ol Default [1:0] V	UT UT Value	Yes Yes Yes	DPL 1'h0	EPL 1'b1			
_				Norma Partial Partial	Mode ON, Idle Mo Mode ON, Idle Mo Sleep I	de OFF, ode ON, S N	Sleep Ol Sleep Ol Default [1:0] V	Value (SPL H	Yes Yes Yes	DPL 1'b0 1'b0	EPL 1'b1 1'b1			





8.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h				FRMCTR1	Frame R	ate Cont	rol (In No	rmal Mo	de / Full d	colors))			
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
1 st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVA	· [1:0]	00
2 nd Parameter	1	1	1	XX	0	0	0		-	RTNA [4:0)]	•	1B

Formula to calculate frame frequency:

Frame Rate= $\frac{\text{fosc}}{\text{Clocks per line } \text{x Division ratio x (Lines + VBP + VFP)}}$

Sets the division ratio for internal clocks of Normal mode at MCU interface.

fosc: internal oscillator frequency
Clocks per line: RTNA setting
Division ratio: DIVA setting
Lines: total driving line number
VBP: back porch line number
VFP: front porch line number

	RTI	NA [4:0]		Frame Rate (Hz)
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

_					
	RTI	NA [4:0]		Frame Rate (Hz)
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

Description

DIVA [1:0]: division ratio for internal clocks when Normal mode.

DIVA	[1:0]	Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNA [4:0]: RTNA[4:0] is used to set 1H (line) period of Normal mode at MCU interface.

	RTI	NA [4:0]		Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

	RT	NA [4:0]		Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

	RTI	NA [4:0]	Clock per Line	
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks





Register Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes	Restriction	EXTC should be high to enab	le this	command				
Register Availability Normal Mode ON, Idle Mode ON, Sleep OUT Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes				Status			Availability	
Availability Partial Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes			Nor	mal Mode ON, Idle Mode	OFF, Sleep	OUT	Yes	
Partial Mode ON, Idle Mode ON, Sleep OUT Yes	Register		Normal Mode ON, Idle Mode ON, Sleep OUT Yes					
	Availability		Par	tial Mode ON, Idle Mode	OFF, Sleep (TUC	Yes	
Sleep IN Yes	-		Par	rtial Mode ON, Idle Mode	ON, Sleep C	DUT	Yes	
				Sleep IN			Yes	
2 ())					5.4			
Status Default Value				Status				
DIVA [1:0] RTNA [4:0]	Defeat						• •	
Default Power ON Sequence 2'b00 5'h1Bh	Default			Power ON Sequence	2'b00	5'ł	n1Bh	
SW Reset 2'b00 5'h1Bh				SW Reset	2'b00	5'h	n1Bh	
HW Reset 2'b00 5'h1Bh				HW Reset	2'b00	5'h	n1Bh	





8.3.3. Frame Rate Control (In Idle Mode/8 colors) (B2h)

B2h		FRMCTR2 (Frame Rate Control (In Idle Mode / 8I colors))											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
1 st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVE	3 [1:0]	00
2 nd Parameter	1	1	1	XX	0	0	0		F	RTNB [4:0)]		1B

Formula to calculate frame frequency

Frame Rate= $\frac{\text{fosc}}{\text{Clocks per line } \text{x Division ratio x (Lines + VBP + VFP)}}$

Sets the division ratio for internal clocks of Idle mode at MCU interface.

fosc: internal oscillator frequency
Clocks per line: RTNB setting
Division ratio: DIVB setting
Lines: total driving line number
VBP: back porch line number
VFP: front porch line number

	RTI	NB [4:0]		Frame Rate (Hz)
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

	RTI	NB [4:0]	Frame Rate (Hz)	
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

Description

DIVB [1:0]: division ratio for internal clocks when Idle mode.

DIVE	3 [1:0]	Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNB [4:0]: RTNB[4:0] is used to set 1H (line) period of Idle mode at MCU interface.

	RTI	NB [4:0]	Clock per	
					Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

	RTI	NB [4:0]		Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

	RTI	NB [4:0]	Clock per Line	
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks





Restriction	EXTC should be high to enable this command							
		Status		۸	vailability			
		Normal Mode ON, Idle Mod	e OFF. Sleep		Yes			
Register		Normal Mode ON, Idle Mod			Yes			
Availability		Partial Mode ON, Idle Mode	e OFF, Sleep (TUC	Yes			
		Partial Mode ON, Idle Mod	e ON, Sleep C	DUT	Yes			
		Sleep IN			Yes			
		Q; ;	Defaul	It Value				
		Status	DIVB [1:0]	RTNB [4	4:0]			
Default		Power ON Sequence	2'b00	5'h1B	h			
		SW Reset	2'b00	5'h1B	h			
		HW Reset	2'b00	5'h1B	h			





8.3.4. Frame Rate control (In Partial Mode/Full Colors) (B3h)

B3h		FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors))											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
1 st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVC	[1:0]	00
2 nd Parameter	1	1	↑	XX	0	0	0		F	RTNC [4:0)]		1B

Formula to calculate frame frequency:

Frame Rate= $\frac{\text{fosc}}{\text{Clocks per line } \text{x Division ratio x (Lines + VBP + VFP)}}$

Sets the division ratio for internal clocks of Partial mode (Idle mode off) at MCU interface.

fosc: internal oscillator frequency
Clocks per line: RTNC setting
Division ratio: DIVC setting
Lines: total driving line number
VBP: back porch line number
VFP: front porch line number

	RT	NC [4:0]	Frame Rate (Hz)	
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

	RTI	NC [4:0]	Frame Rate (Hz)	
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

Description

DIVC [1:0]: division ratio for internal clocks when Partial mode.

DIVC	[1:0]	Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

Note: 1clock unit=1.625u sec

RTNC [4:0]: RTNC [4:0] is used to set 1H (line) period of Partial mode at MCU interface.

	RTI	NC [4:0]		Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

	RTI	NC [4:0]		Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

	RTI	NC [4:0]	Clock per Line	
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks





Restriction	EXTC should be high to enable	e this	command						
			Status			Availability			
		Nor	mal Mode ON, Idle Mode	OFF, Sleep	OUT	Yes			
Register		Noi	rmal Mode ON, Idle Mod	e ON, Sleep (TUC	Yes			
Availability		Par	rtial Mode ON, Idle Mode	OFF, Sleep (TUC	Yes			
		Pa	rtial Mode ON, Idle Mode	e ON, Sleep C	DUT	Yes			
			Sleep IN Yes						
			Status	Default Valu		е			
			Glatas	DIVC [1:0]	RTN	IC [4:0]			
Default			Power ON Sequence	2'b00	5'l	n1Bh			
			SW Reset	2'b00	5'l	n1Bh			
			HW Reset	2'b00	5'l	n1Bh			





8.3.5. Display Inversion Control (B4h)

B4h	INVTR (Display Inversion Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
1 st Parameter	1	1	↑	XX	0	0	0	0	0	NLA	NLB	NLC	02
	Display	Display inversion mode set											
	NLA: Ir	LA: Inversion setting in full colors normal mode (Normal mode on)											
	NLB: Ir	nversion	setting in	Idle mode (Idle	mode on)								
Description	NLC: Ir	nversion	setting in	full colors partia	al mode (F	artial mod	e on / ld	le mode d	off)				
Description					NLA / N	ILB / NLC	Inv	version					
						0		inversion					
						1	Frame	e inversio	n				
	E)/E0												
Restriction	EXIC	should be	e high to e	nable this com	mand								
						Status			Availab	oility			
				Normal N	/lode ON,	ldle Mode	OFF, SI	ep OUT	Yes				
Register				Normal I	Mode ON,	Idle Mode	ON, Sle	ep OUT	Yes				
Availability				Partial M	lode ON, I	dle Mode	OFF, Sle	ep OUT	Yes	i			
				Partial N	/lode ON,	Idle Mode	ON, Slee	ep OUT	Yes				
						Sleep IN			Yes				
							De	efault Valu	16				
					Sta	tus	NLA		NLC				
Default				F	Power ON	Sequence		_	1'b0				
	SW Reset 1'b0 1'b1 1'b0												
					H/W F		1'b0	1'b1	1'b0				





8.3.6. Blanking Porch Control (B5h)

B5h		PRCTR (Blanking Porch)											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1 st Parameter	1	1	↑	XX	0				VFP [6:0]				02
2 nd Parameter	1	1	↑	XX	0				VBP [6:0]				02
3 rd Parameter	1	1	↑	XX	0	0	0			HFP [4:0]			0A
4 th Parameter	1	1	↑	XX	0	0	0			HBP [4:0]			14

VFP [6:0] / **VBP [6:0]**: The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
0000110	6	1000110	70
0000111	7	1000111	71
0001000	8	1001000	72
0001001	9	1001001	73
0001010	10	1001010	74
0001011	11	1001011	75
0001100	12	1001100	76
0001101	13	1001101	77
:	:	:	:
:	:	:	:
0111101	61	1111101	125
0111110	62	1111110	126
0111111	63	1111111	127

Description

Note: VFP + VBP ≤ 254 HSYNC signals

HFP [4:0] / **HBP [4:0]:** The HFP [4:0] and HBP [4:0] bits specify the line number of horizontal front and back porch period respectively.

HFP [4:0] HBP [4:0]	Number of DOTCLK of the front/back porch			
00000	Setting prohibited			
00001	Setting prohibited			
00010	2			
00011	3			
00100	4			
00101	5			
00110	6			
00111	7			
01000	8			
01001	9			
01010	10			
01011	11			
01100	12			
01101	13			
01110	14			
01111	15			

HFP [4:0] HBP [4:0]	Number of DOTCLK of front/back porch
10000	16
10001	17
10010	18
10011	19
10100	20
10101	21
10110	22
10111	23
11000	24
11001	25
11010	26
11011	27
11100	28
11101	29
11110	30
11111	31





Restriction	EXTC should be high to enable this command						
			Status		Availabi	lity	
		Normal Mod	e ON, Idle Mode	e OFF, Sleep O	UT Yes		
Register		Normal Mod	de ON, Idle Mod	e ON, Sleep Ol	JT Yes		
Availability		Partial Mod	e ON, Idle Mode	OFF, Sleep Ol	JT Yes		
		Partial Mod	e ON, Idle Mode	JT Yes			
			Sleep IN				
		0		Default	Value		
Default		Status	VFP [6:0]	VBP [6:0]	HFP [4:0]	HBP [4:0]	
		Power ON Sequence	7'h02h	7'h02h	5'h0Ah	5'h14h	
		SW Reset	7'h02h	7'h02h	5'h0Ah	5'h14h	
		HW Reset	7'h02h	7'h02h	5'h0Ah	5'h14h	





8.3.7. Display Function Control (B6h)

B6h		DISCTRL (Display Function Control)											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	0	1	1	0	B6h
1 st Parameter	1	1	1	XX	0	0	0	0	PTG	[1:0]	PT	[1:0]	0A
2 nd Parameter	1	1	1	XX	REV	GS	SS	SM		ISC	[3:0]		82
3 rd Parameter	1	1	1	XX	0	0			NL [5:0]			27
4 th Parameter	1	1	1	XX	0	0			PCDI	/ [5:0]		•	XX

PTG [1:0]: Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Set with the PT [2:0] bits	VCOMH/VCOML
0	1	Setting prohibited		
1	0	Interval scan	Set with the PT [2:0] bits	
1	1	Setting prohibited		

PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

Source output on no			non-display area	VCOM output on non-display area		
PT [1:0] Positi		Positive polarity	Negative polarity	Positive polarity	Negative polarity	
0	0	V63	V0	VCOML	VCOMH	
0	1	V0	V63	VCOML	VCOMH	
1	0	AGND	AGND	AGND	AGND	
1	1	Hi-Z	Hi-Z	AGND	AGND	

SS: Select the shift direction of outputs from the source driver.

SS	Source Output Scan Direction				
0	S1 → S720				
1	S720 → S1				

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.

Description

To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

REV: Select whether the liquid crystal type is normally white type or normally black type.

REV	Liquid crystal type
0	Normally black
1	Normally white

ISC [3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] ="10" to select interval scan.

Then scan cycle is set as odd number from $0\sim29$ frame periods. The polarity is inverted every scan cycle.

ISC [3:0]	Scan Cycle	f _{FLM} = 60Hz
0000	1 frame	17ms
0001	3 frames	51ms
0010	5 frames	85ms
0011	7 frames	119ms
0100	9 frames	153ms
0101	11 frames	187ms
0110	13 frames	221ms
0111	15 frames	255ms



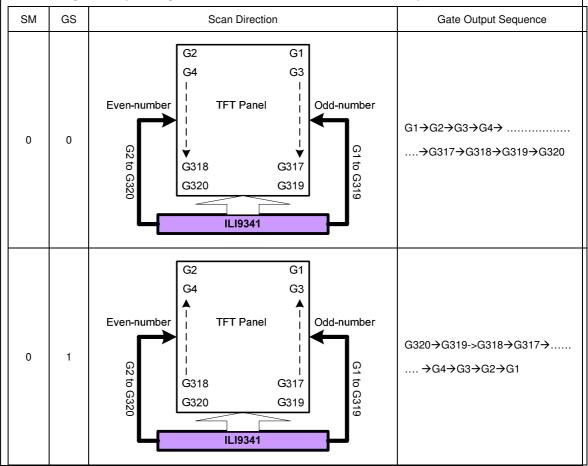


1000	17 frames	289ms
1001	19 frames	323ms
1010	21 frames	357ms
1011	23 frames	391ms
1100	25 frames	425ms
1101	27 frames	459ms
1110	29 frames	493ms
1111	31 frames	527ms

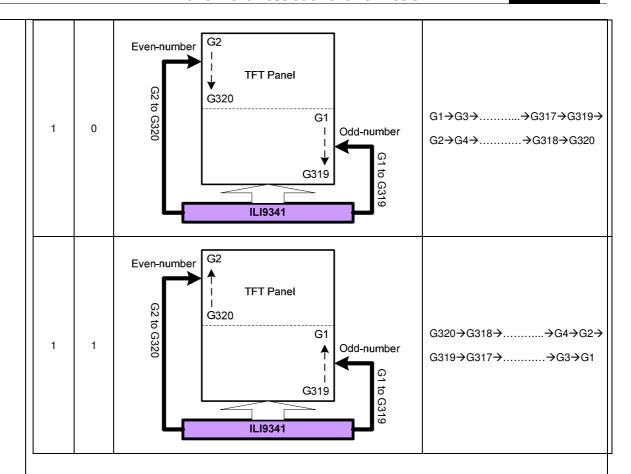
GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction
0	G1 → G320
1	G320 → G1

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.







NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

		NL	LCD Drive Line			
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines
0	0	0	1	1	0	56 lines
0	0	0	1	1	1	64 lines
0	0	1	0	0	0	72 lines
0	0	1	0	0	1	80 lines
0	0	1	0	1	0	88 lines
0	0	1	0	1	1	96 lines
0	0	1	1	0	0	104 lines
0	0	1	1	0	1	112 lines
0	0	1	1	1	0	120 lines
0	0	1	1	1	1	128 lines
0	1	0	0	0	0	136 lines
0	1	0	0	0	1	144 lines
0	1	0	0	1	0	152 lines
0	1	0	0	1	1	160 lines
0	1	0	1	0	0	168 lines

		NL	[5:0]		LCD Driver Line	
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines
0	1	1	0	1	1	224 lines
0	1	1	1	0	0	232 lines
0	1	1	1	0	1	240 lines
0	1	1	1	1	0	248 lines
0	1	1	1	1	1	256 lines
1	0	0	0	0	0	264 lines
1	0	0	0	0	1	272 lines
1	0	0	0	1	0	280 lines
1	0	0	0	1	1	288 lines
1	0	0	1	0	0	296 lines
1	0	0	1	0	1	304 lines
1	0	0	1	1	0	312 lines
1	0	0	1	1	1	320 lines
		Oth	Setting inhibited			

PCDIV [5:0]:





			exte	rnal fosc=	$\frac{DC}{2\times (P)}$	TCLK CDIV					
Restriction	EXTC should be high to en	able th	is command								
				Status				Availabi	lity		ļ
		Norn	nal Mode ON		OFF, S	leep O		Yes			
Register		Norr	mal Mode ON	I, Idle Mode	e ON, S	leep Ol	JT	Yes			
Availability			ial Mode ON					Yes			
		Par	tial Mode ON		ON, SI	eep OL	JT	Yes			
				Sleep IN				Yes			
						Default	Value				
	Status		PTG [1:0]	PT [1:0]	REV	GS	SS	SM	ISC [3:0]	NL [5:0]	
Default	Power ON Sequ	ence	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h	
	SW Reset		2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h	
	HW Reset		2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h	





Cammand	B7h	ETMOD (Entry Mode Set)													
GAS: Low voltage detection control. GAS		D/CX	RDX	WRX	D17-8	D7	D6		D5	D4	D3	D2	D1	D0	HE
GAS: Low voltage detection control. GAS Low voltage detection 0 Enable 1 Disable 1 Disable GON/DTE: Set the output level of gate driver G1 ~ G320 as follows GON DTE G1-G320 Gate Output 0 0 VGH 0 1 VGH 1 0 VGL 1 1 Normal display EXTC should be high to enable this command Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Ves Partial Mode ON, Idle Mode OFF, Sleep OUT Ves Partial Mode ON, Idle Mode OFF, Sleep OUT Ves Partial Mode ON, Idle Mode OFF, Sleep OUT Ves Sleep IN Ves Sleep IN Ves	Command	0	1	1			0								B7l
Restriction EXTC should be high to enable this command Register Availability Register Ava	Parameter	1	1	1 1	XX	0	0		0	0	0	GON	DIE	GAS	06
Restriction EXTC should be high to enable this command Register Availability Register Ava															
Restriction EXTC should be high to enable this command Register Availability Register Ava															
Restriction EXTC should be high to enable this command Register Availability Register Ava															
O Enable 1 Disable Description GON/DTE: Set the output level of gate driver G1 ~ G320 as follows GON DTE G1~G320 Gate Output 0 0 1 VGH 0 1 VGH 1 0 VGL 1 1 Normal display Restriction EXTC should be high to enable this command Fegister Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Sleep IN Yes Default Value GON DTE GAS		GAS: L	ow volta	age detec	tion control.	CAC									
Restriction EXTC should be high to enable this command Status							L	LOW V							
Restriction EXTC should be high to enable this command Status															
Restriction EXTC should be high to enable this command Status	Description	GON/E	TE: Set	the outpu	it level of gate	e driver G1	~ G320	as fo	llows						
Restriction EXTC should be high to enable this command Status						GON	DTE	G1~	·G320 G	ate Out	put				
Restriction EXTC should be high to enable this command Status															
Restriction EXTC should be high to enable this command Status															
Restriction EXTC should be high to enable this command Status															
Register Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value GON DTE GAS															
Register Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value GON DTE GAS															
Register Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value GON DTE GAS															
Register Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value GON DTE GAS															
Register Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value GON DTE GAS	Restriction	EXTC :	should b	e high to	enable this co	ommand									
Register Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value GON DTE GAS							Statu	S			Availa	ability			
Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value GON DTE GAS	D				Norma	al Mode ON			OFF, Sle	ep OUT					
Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value GON DTE GAS	Register					Normal Mode ON, Idle Mode ON, Sleep OUT									
Sleep IN Yes Status Default Value GON DTE GAS	Availability														
Status GON DTE GAS					Partia	ai Mode ON			וע, Slee	ep OUT					
Status GON DTE GAS										£					
						Sta	atus								
	Default					Power ON	I Segue	nce	1'b1	1'b1	1'b0				

SW Reset

HW Reset

1'b1

1'b1

1'b1 1'b1

1'b0

1'b0





8.3.9. Backlight Control 1 (B8h)

B8h			·	•		Ва	acklig	ht Cor	ntrol 1				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h
Parameter		1	1	XX	0	0	0	0	TH_UI [3]	TH_UI [2]	TH_UI [1]	TH_UI [0]	0C
	TH_UI [3	(UI) m		atio of max	imum					umulate histo isplay image			
I			TH_UI	[3:0]		Descr	iption		TH_UI	[3:0]	Description		
Description			4'0h			99	•		4'8		84%		
			4'11	1		98	%		4'9	h	82%		
			4'2h	1		96	%		4'A	h	80%		
I			4'3h	1	94%				4'B	4'Bh			
			4'4h			92			4'C		76%		
			4'5h			90			4'D		74%		
			4'6h			88			4'E		72%		
			4'7h	1	86%					h	70%		
						St	atus			Availability			
									Sleep Out	Yes			
Register									Sleep Out	Yes			
Availability									Sleep Out	Yes	_		
						On, Idle	e Mod	e On, s	Sleep Out	Yes			
			Sleep In Yes										
					(Status			Default Va				
Default				P	ower (On Sec	quence	Э	4'b0110				
					SV	V Res	et		No chang	je			
					Н۷	V Res	et		4'b0110				





8.3.10. Backlight Control 2 (B9h)

B9h		Backlight Control 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	1	0	1	1	1	0	0	1	B9h	
Parameter	1	1	1	XX	TH_MV [3]	TH_MV [2]	TH_MV [1]	TH_MV [0]	TH_ST [3]	TH_ST [2]	TH_ST [1]	TH_ST [0]	СС	

TH_ST [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_ST [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

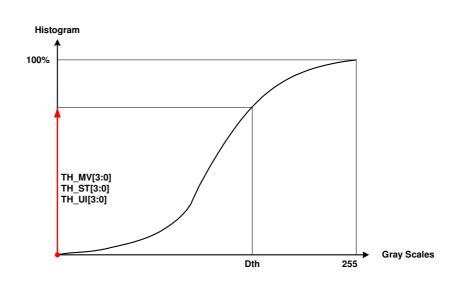
TH_ST [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

TH_MV [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the moving image mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

Description	
•	

TH_MV [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_MV [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%







		Status					
	Normal Mode On	n, Idle Mode Off, Sleep Out	Yes				
Register	Normal Mode On	n, Idle Mode On, Sleep Out	Yes				
Availability	Partial Mode On	Partial Mode On, Idle Mode Off, Sleep Out					
	Partial Mode On	Partial Mode On, Idle Mode On, Sleep Out					
	Sleep In		Yes				
	Otatus	Default Va	llue				
	Status	TH MV [3:0]	TH ST [3:0				
Default	Power On Sequence	4'b1100	4'b1100				
	SW Reset	No change	No change				
	HW Reset	4'b1100	4'b1100				





8.3.11. Backlight Control 3 (BAh)

BAh	Backlight Control 3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	1	0	1	0	BAh
Parameter	1	1	1	XX	0	0	0	0	DTH_UI [3]	DTH_UI [2]	DTH_UI [1]	DTH_UI [0]	04

 $\textbf{DTH_UI [3:0]}: This parameter is used set the minimum limitation of grayscale threshold value in User Icon (UI) image mode.$

This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

	DTH_UI [3:0]	Description
Description	4'0h	252
·	4'1h	248
	4'2h	244
	4'3h	240
	4'4h	236
	4'5h	232
	4'6h	228
	4'7h	224

DTH_UI [3:0]	Description
4'8h	220
4'9h	216
4'Ah	212
4'Bh	208
4'Ch	204
4'Dh	200
4'Eh	196
4'Fh	192

	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Register	Normal Mode On, Idle Mode On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Status	
Status	
Power On Sequence	
SW Reset	
HW Reset	





8.3.12. Backlight Control 4 (BBh)

BBh						Bacl	klight Con	trol 4					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	1	1	BBh
Parameter	1	1	1	XX	DTH_MV [3]	DTH_MV [2]	DTH_MV [1]	DTH_MV [0]	DTH_ST [3]	DTH_ST [2]	DTH_ST [1]	DTH_ST [0]	65

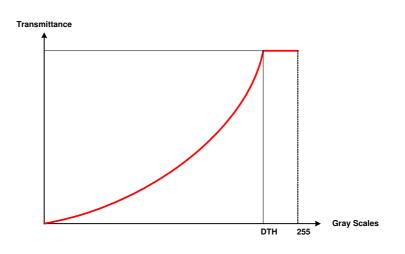
DTH_ST [3:0]/DTH_MV [3:0]: This parameter is used set the minimum limitation of grayscale threshold value. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

DTH_ST [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_ST [3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164

DTH_MV [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_MV [3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164
4′Fn	164



Register
Availability

Description

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes





		Status	Default Value		
			DTH_MV [3:0]	DTH_ST [3:0]	
Default		Power On Sequence	4'b0110	4'b0101	
		SW Reset	No change	No change	
		HW Reset	4'b0110	4'b0101	





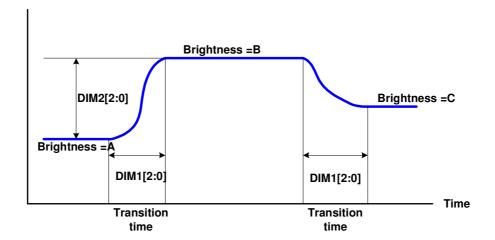
8.3.13. Backlight Control 5 (BCh)

BCh						Backl	ight Contr	ol 5					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	1	1	0	0	BCh
Parameter	1	1	1	XX	DIM2 [3]	DIM2 [2]	DIM2 [1]	DIM2 [0]	0	DIM1 [2]	DIM1 [1]	DIM1 [0]	44

DIM1 [2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision.

DIM1 [2:0]	Description
3'0h	1 frame
3'1h	1 frame
3'2h	2 frames
3'3h	4 frames
3'4h	8 frames
3'5h	16 frames
3'6h	32 frames
3'7h	64 frames

Description



DIM2 [3:0]: This parameter is used to set the threshold of brightness change.

When the brightness transition difference is smaller than DIM2 [3:0], the brightness transition will be ignored.

For example:

If | brightness B - brightness A| < DIM2 [2:0], the brightness transition will be ignored and keep the brightness A.

	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Register	Normal Mode On, Idle Mode On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

	Chahua	Default	: Value
	Status	DIM2 [3:0]	DIM1 [2:0]
Default	Power On Sequence	4'b0100	4'b0100
	SW Reset	No change	No change
	HW Reset	4'b0100	4'b0100





8.3.14. Backlight Control 7 (BEh)

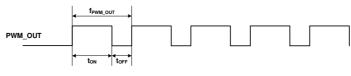
BEh						Bac	Backlight Control 7													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
Command	0	1	1	XX	1	0	1	1	1	1	1	0	BEh							
Parameter	1	1	1	XX	PWM_ DIV[7]	PWM_ DIV[6]	PWM_ DIV[5]	PWM_ DIV[4]	PWM_ DIV[3]	PWM_ DIV[2]	PWM_ DIV[1]	PWM_ DIV[0]	0F							

PWM_DIV [7:0]: PWM_OUT output frequency control. This command is used to adjust the PWM waveform frequency of

PWM_OUT. The PWM frequency can be calculated by using the following equation.

$$f_{PWM_OUT} = \frac{16MHz}{(PWM_DIV[7:0]+1)\times255}$$

PWM_DIV [7:0]	f _{PWM_OUT}
8'h0	62.74 KHz
8'h1	31.38 KHz
8'h2	20.915KHz
8'h3	15.686KHz
8'h4	12.549 KHz
8'hFB	249Hz
8'hFC	248Hz
8'hFD	247Hz
8'hFE	246Hz
8'hFF	245Hz



Note: The output frequency tolerance of internal frequency divider in CABC is ±10%

Register
Availability
Availability

Description

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Default Value
PWM_DIV [7:0]=0Fh
No change
PWM_DIV [7:0]=0Fh





8.3.15. Backlight Control 8 (BFh)

BFh				J. J (=	,, ,,		Bac	cklight Co	ntrol 2						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	1	0	1	1	1	1	1	1	BFh		
Parameter	1	1	1	XX	0	0	0	0	0	LEDONR	LEDONPO	L LEDPWMPOL	00		
	LEDF	WMPC)L: The	bit is use	d to d	efine polarit	ty of LI	EDPWM s	ignal.						
					BL	LEDPWM	POL		LEDPW	/M pin					
				-	0	0			0						
					0	<u>1</u> 0		Origina	1 polarity	of PWM si	anal				
				-	1	1				of PWM s					
	LEDO	LEDONPOL: This bit is used to control LEDON pin.													
					BL	LEDONP	OL		LEDON	l pin					
Description					0	0			0						
Description															
					1	0		lr	LEDO						
		1 1 Inversed LEDONR													
	LEDONR: This bit is used to control LEDON pin.														
						LEDONR		De	escription						
					_	0			Low						
					L	1			High						
							Sta			Availa	ability				
						nal Mode C									
Register Availability						nal Mode C tial Mode O									
Availability						tial Mode O									
					Slee		ri, idio	Wode On	, oldop ot	Y					
					C	tatua			Default	Value					
						tatus		EDONR	LEDON	POL LED	PWMPOL				
Default				Po		n Sequence		1'b0	1'b0		1'b0				
						Reset	No	change	No char	nge No	change				
					HW	Reset		1'b0	1'b0		1'b0				
	<u> </u>														





8.3.16. Power Control 1 (C0h)

C0h				(,			PW	/CTRL 1	(Power	r Co	ntro	l 1)							
	D/CX	RDX	WRX	D17	7 0	Ŧ	D7	D6	D5	- 1		4	Т г	03	Т	D2	D1	D0	HEX
Command	0	1	↑	X			1	1	0)		0		0	0	0	C0h
1 st Parameter	1	1	<u></u>	X			0	0				,		VRH	1 [5:			1 0	21
r aramotor						is			for the	VC	OM I	evel					e voltage l	evel	
	VIIII [C	7.0]. Oct		VRH [100	T	GVDD		, 	O1V1 1		RH [gray	Journ	GVDD	CVCI.	
			0			0	0 Se	tting proh	ibited	-	1	0		0 0	0	0	4.45 V		
				0 0	0			tting proh			1	0		0	0	1	4.50 V		
								tting proh		-	1	0		0	1	0	4.55 V		
				0 0			0	3.00 V 3.05 V		-	1	0		0	0	0	4.60 V 4.65 V		
				0 0		_	1	3.10 V		-	1	0		1	0	1	4.65 V 4.70 V		
							0	3.15 V		-	1	0		1	1	0	4.75 V		
			0	0 0			1	3.20 V			1	0		1	1	1	4.80 V		
				0 1		_	0	3.25 V		-	1	0		0	0	0	4.85 V		
							0	3.30 V 3.35 V		-	1	0		0	1	0	4.90 V 4.95 V		
				0 1			1	3.40 V		-	1	0		0	1	1	5.00 V		
				0 1			0	3.45 V			1	0		1	0	0	5.05 V		
				0 1			1	3.50 V			1	0		1	0	1	5.10 V		
				0 1			0	3.55 V		-	1	0	1	1	1	0	5.15 V		
Description				0 1 1 1 0	_	_	0	3.60 V 3.65 V		-	1	1		0	0	0	5.20 V 5.25 V		
							1	3.70 V		-	1	1		0	0	1	5.30 V		
			0	1 0	0	1	0	3.75 V			1	1	0	0	1	0	5.35 V		
						_	1	3.80 V		-	1	1		0	1	1	5.40 V		
				1 0		_	0 1	3.85 V		-	1	1	0	1	0	0	5.45 V		
			0		_	_	0	3.90 V 3.95 V		-	1	1		1	1	0	5.50 V 5.55 V		
				1 0			1	4.00 V		-	1	1		1	1	1	5.60 V		
			0	1 1		_	0	4.05 V			1	1	1	0	0	0	5.65 V		
							1	4.10 V		-	1	1		0	0	1	5.70 V		
			0				0	4.15 V 4.20 V		-	1	1		0	1	1	5.75 V 5.80 V		
			- t	1 1	_	_	0	4.25 V		-	1	1		1	0	0	5.85 V		
			0	1 1	1		1	4.30 V			1	1		1	0	1	5.90 V		
				1 1			0	4.35 V		-	1	1	_	1	1	0	5.95 V		
				1 1			1	4.40 V			1	1		1	1	1	6.00 V		
	Note1:	Make sı	ure that V	'C and V	'RH s	ettin	g restri	ction: GV	$DD \leq 0$	(DD	VDH	- 0.2	2) V.						
Restriction	EXTC	should h	e high to	enahle t	hie co	nmm	and												
ricotriction	LX10		- Ingrito	CHADIC I	1110 00	,,,,,,	- Idilia												
								Obstant					Ι.Δ.		L 99				
					l		- d - ON	Status	- OFF		(NIT.	A	vaila		У			
Register								, Idle Mod						Ye					
-								I, Idle Mo					-	Ye					
Availability				_				, Idle Mod , Idle Mod						Ye Ye					
					Parlia	ti ivic	ode ON	Sleep IN		Sie	ер О	UI		Ye					
								Sieep iiv					-	16	5				
								Status		De	efaul	t Val	ue						
						L				١	VRH	[5:0]]						
Default								ON Sequ			6'h								
	SW Reset 6'h21h																		
						L	H	W Reset			6'h	21h							





8.3.17. Power Control 2 (C1h)

C1h					PW	CTRL 2 (I	Power Co	ontrol 2)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
Parameter	1	1	↑	XX	0	0	0	0	0		BT [2:0]		10
Description	Select	the optin	nal step-u ure that D		operating BT [2:0] 0 0 0 0 0 1 0 1 0 0 1 1 estriction:	VOltage DDVD VCI x	H VGH VCI 2 VCI ≤ 5.8 V.	x 7 -V0 -V0 -V0 -V0		on, set a	smaller fac	ctor.	
Restriction	EXTC :	should b	e high to	enable this con	nmand								
Register Availability				Normal Partial N	Mode ON, Mode ON, Mode ON,	, Idle Mod Idle Mode	e ON, Sle OFF, Sle	eep OUT eep OUT	Availal Yes Yes Yes Yes	6 6 6			
Default					Power	Status ON Seque W Reset W Reset		efault Va BT [2:0] 3'b000 3'b000 3'b000	ue				





C5h	VMCTRL1 (VCOM Control 1)														
	D/CX	RDX	WRX	D	17-8	D7	D6		D5 D4	D3	D2	2 D1	D0	Н	
Command	0	1	↑		XX	1	1		0 0	0	1	0	1	С	
I st Parameter	1	1	↑		XX	0				VMH [6:0]				(
2 nd Parameter	1	1	↑		XX	0				VML [6:0]				3	
	VMH [6:0]: Set the VCOMH voltage.														
	l				0.01	\(\(\alpha\)	7	\/\dagger	1/001/1/0	0	\/\	1/001/	11.17		
	VMH [6:0] 0000000		2.700		01000		VCOMH(V)	<u>v)</u>	VMH [6:0]	VCOMH(V	′)	VMH [6:0]	VCON		
	0000000		2.700		01000		3.500 3.525	-	1000000	4.300 4.325		1100000 1100001	5.10 5.11		
	0000010		2.750		01000		3.550		1000001	4.350		1100001	5.1		
	0000011		2.775		01000		3.575		1000011	4.375		1100011	5.1		
	0000100		2.800		01001		3.600		1000100	4.400		1100100		5.200	
	000	0101	2.825		01001	01	3.625		1000101	4.425		1100101	5.2		
		0110	2.850		01001		3.650		1000110	4.450		1100110	5.2		
		0111	2.875		01001		3.675	4	1000111	4.475		1100111	5.2		
Description		1000	2.900 2.925		0101000		3.700	-	1001000	4.500	\dashv	1101000		5.300 5.325	
		1001	2.925		0101001 0101010		3.725 3.750	-	1001001 1001010	4.525 4.550	\dashv	1101001 1101010	5.3		
	0001010		2.950		0101010		3.775	-	1001010	4.575		1101011	5.3		
	0001100		3.000		01011100		3.800		1001110	4.600		1101110	5.40		
	0001101		3.025		0101101		3.825		1001101	4.625		1101101	5.4		
	0001110		3.050		0101110		3.850		1001110	4.650		1101110	5.4	50	
	0001111		3.075		0101111		3.875		1001111	4.675		1101111	5.4		
	0010000		3.100		0110000		3.900		1010000	4.700		1110000	5.50		
	0010001		3.125		0110001		3.925	4	1010001	4.725		1110001	5.5		
	0010010 0010011		3.150 3.175		0110010 0110011		3.950 3.975	-	1010010	4.750 4.775		1110010 1110011	5.5 5.5		
					01101		4.000		1010011	4.773		1110100	5.6		
		0010100 3.200 0010101 3.225			01101		4.025		1010101	4.825		1110101	5.6		
	0010110		3.250		01101		4.050		1010110	4.850		1110110	5.6		
	0010111		3.275	3.275		11	4.075		1010111	4.875		1110111	5.6		
	0011000			3.300		00	4.100		1011000	4.900		1111000	5.70		
	0011001		3.325		01110		4.125		1011001	4.925		1111001	5.7		
	0011010		3.350		01110		4.150	-	1011010	4.950		1111010	5.7		
	0011011 0011100		3.375	3.400		00	4.175 4.200	-	1011011	4.975 5.000		1111011	5.7		
	0011101			3.425		01	4.225	-	1011101	5.025		1111101	5.8		
		0011101				10	4.250		1011110	5.050		1111110	5.8		
		0011111			01111		4.275		1011111	5.075		1111111	5.8		
	VML [6:0] : Set the VCOML voltage VML [6:0] VCOML(V)														
		00000	-2.500		01000		-1.700	1	1000000	-0.900	,	1100000	-0.10		
		000001	-2.475		01000		-1.675	1	1000001	-0.875		1100001	-0.07		
		000010	-2.450		01000		-1.650		1000010	-0.850		1100010	-0.05		
		00011	-2.425		01000		-1.625	1	1000011	-0.825		1100011	-0.02	5	
		00100	-2.400		0100		-1.600		1000100	-0.800	_	1100100	0		
		00101	-2.375		0100		-1.575	-	1000101	-0.775	_	1100101	Reserv		
		00110	-2.350		0100		-1.550	-	1000110	-0.750	\dashv	1100110	Reserv		
	-	00111	-2.325 -2.300		0100		-1.525 -1.500	-	1000111	-0.725 -0.700	-	1100111 1101000	Reserv Reserv		
		01000	-2.300		01010		-1.500 -1.475	1	1001000	-0.700		1101000	Reserv		
		01010	-2.270		01010		-1.475	1	1001001	-0.650	1	1101001	Reserv		
	-	01011	-2.225		01010		-1.425	1	1001011	-0.625		1101011	Reserv		
		01100	-2.200		0101		-1.400	1	1001100	-0.600		1101100	Reserv		
	-	01101	-2.175		0101		-1.375		1001101	-0.575		1101101	Reserv		
		01110	2.150		0101	110	1 250	1	1001110	0.550		1101110	Doggr	I	

The information contained herein is the exclusive property of ILI Technology Corp. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of ILI Technology Corp.

-1.350

-1.325

-1.300

-1.275

-1.250

-1.225

1001110

1001111

1010000

1010001

1010010

1010011

-0.550

-0.525

-0.500

-0.475

-0.450

-0.425

1101110

1101111

1110000

1110001

1110010

1110011

Reserved

Reserved

Reserved

Reserved

Reserved

Reserved

0101110

0101111

0110000

0110001

0110010

0110011

0001110

0001111

0010000

0010001

0010010

0010011

-2.150

-2.125

-2.100

-2.075

-2.050

-2.025





	0010100 -2.0	00	0110100	-1.200		1010100	-0.400	1110100	Reserved					
	0010100 2.0		0110101	-1.175	-	1010101	-0.375	1110100	Reserved					
	0010110 -1.9		0110110	-1.150	-	1010110	-0.350	1110110	Reserved					
	0010111 -1.9		0110111	-1.125		1010111	-0.325	1110111	Reserved					
	0011000 -1.9		0111000	-1.100		1011000	-0.300	1111000	Reserved					
	0011001 -1.8		0111001	-1.075		1011001	-0.275	1111001	Reserved					
	0011010 -1.8	50	0111010	-1.050		1011010	-0.250	1111010	Reserved					
	0011011 -1.8	25	0111011	-1.025		1011011	-0.225	1111011	Reserved					
	0011100 -1.8	00	0111100	-1.000		1011100	-0.200	1111100	Reserved					
	0011101 -1.7	75	0111101	-0.975		1011101	-0.175	1111101	Reserved					
	0011110 -1.7	50	0111110	-0.950		1011110	-0.150	1111110	Reserved					
	0011111 -1.7	25	0111111	-0.925		1011111	-0.125	1111111	Reserved					
Restriction	EXTC should be high t	o enabl	e this command	d l										
		Ctatua Availability												
				Status	Availability									
Dogiator			Normal Mode	ON, Idle Mo	IT Yes									
Register			Normal Mode	ON, Idle Mo	ode C	T Yes								
Availability			Partial Mode	ON, Idle Mod	de Ol	F, Sleep OU	T Yes							
•			Partial Mode	ON, Idle Mo	de O	N, Sleep OU	Γ Yes							
				Sleep II	N	•	Yes							
		ı												
			Sta	tuo	'alue									
			Sia	เนธ	VM	VML [6:0]								
Default			Power ON Sequence 7'h31 7'h											
			SW F		7	'h31	7'h3C							
			HW			'h31	7'h3C							
				•		,								





8.3.19. VCOM Control 2(C7h)

C7h					VM	CTRL1 (\	COM Co	ontrol 1)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h		
Parameter	1	1	1	XX	nVM VMF [6:0] C0										

nVM: nVM equals to "0" after power on reset and VCOM offset equals to program MTP value. When nVM set to "1", setting of VMF [6:0] becomes valid and VCOMH/VCOML can be adjusted.

VMF [6:0]: Set the VCOM offset voltage.

	VMF [6:0]: Set the V	COM offset	voltage.				
		VMF[6:0]	VCOMH	VCOML	VMF[6:0]	VCOMH	VCOML
		0000000	VMH	VML	1000000	VMH	VML
		0000001	VMH - 63	VML – 63	1000001	VMH + 1	VML + 1
		0000010	VMH – 62	VML – 62	1000010	VMH + 2	VML + 2
		0000011	VMH – 61	VML – 61	1000011	VMH + 3	VML + 3
		0000100	VMH - 60	VML - 60	1000100	VMH + 4	VML + 4
		0000101	VMH – 58	VML – 58	1000101	VMH + 5	VML + 5
		0000110	VMH – 58	VML – 58	1000110	VMH + 6	VML + 6
		0000111	VMH – 57	VML – 57	1000111	VMH + 7	VML + 7
		0001000	VMH – 56	VML – 56	1001000	VMH + 8	VML + 8
		0001001	VMH – 55	VML – 55	1001001	VMH + 9	VML + 9
	<u> </u>	0001010	VMH – 54	VML – 54	1001010	VMH + 10	VML + 10
		0001011	VMH – 53	VML – 53	1001011	VMH + 11	VML + 11
	<u> </u>	0001100	VMH – 52	VML – 52	1001100	VMH + 12	VML + 12
	<u> </u>	0001101	VMH – 51	VML -51	1001101	VMH + 13	VML + 13
	_	0001110	VMH – 50	VML – 50	1001110	VMH + 14	VML + 14
	_	0001111	VMH – 49	VML – 49	1001111	VMH + 15	VML + 15
		0010000	VMH – 48	VML – 48	1010000	VMH + 16	VML + 16
		0010001	VMH – 47	VML – 47	1010001	VMH + 17	VML + 17
		0010010	VMH – 46	VML – 46	1010010	VMH + 18	VML + 18
		0010011	VMH – 45	VML – 45	1010011	VMH + 19	VML + 19
		0010100	VMH – 44	VML – 44	1010100	VMH + 20	VML + 20
Description		0010101	VMH – 43	VML – 43	1010101	VMH + 21	VML + 21
Description		0010110	VMH – 42 VMH – 41	VML – 42 VML – 41	1010110	VMH + 22 VMH + 23	VML + 22
		0010111	VMH – 41	VML – 41	1010111	VMH + 24	VML + 23 VML + 24
	-	0011000	VMH – 40	VML – 40	1011000	VMH + 25	VML + 25
		0011001	VMH – 38	VML – 38	1011010	VMH + 26	VML + 26
		0011010	VMH – 37	VML – 37	1011011	VMH + 27	VML + 27
		0011100	VMH – 36	VML – 36	1011100	VMH + 28	VML + 28
		0011101	VMH – 35	VML – 35	1011101	VMH + 29	VML + 29
		0011110	VMH – 34	VML – 34	1011110	VMH + 30	VML + 30
		0011111	VMH – 33	VML – 33	1011111	VMH + 31	VML + 31
		0100000	VMH - 32	VML – 32	1100000	VMH + 32	VML + 32
		0100001	VMH – 31	VML – 31	1100001	VMH + 33	VML + 33
		0100010	VMH – 30	VML – 30	1100010	VMH + 34	VML + 34
		0100011	VMH – 29	VML – 29	1100011	VMH + 35	VML + 35
		0100100	VMH – 28	VML – 28	1100100	VMH + 36	VML + 36
		0100101	VMH – 27	VML – 27	1100101	VMH + 37	VML + 37
		0100110	VMH – 26	VML – 26	1100110	VMH + 38	VML + 38
		0100111	VMH – 25	VML – 25	1100111	VMH + 39	VML + 39
	<u> </u>	0101000	VMH – 24	VML – 24	1101000	VMH + 40	VML + 40
	<u> </u>	0101001	VMH – 23	VML – 23	1101001	VMH + 41	VML + 41
	_	0101010	VMH – 22	VML – 22	1101010	VMH + 42	VML + 42
		0101011	VMH – 21	VML – 21	1101011	VMH + 43	VML + 43
		0101100	VMH – 20	VML – 20	1101100	VMH + 44	VML + 44
		0101101	VMH – 19	VML – 19	1101101	VMH + 45	VML + 45
		0101110	VMH – 18	VML - 18	1101110	VMH + 46	VML + 46
		0101111	VMH – 17	VML - 17	1101111	VMH + 47	VML + 47
		0110000	VMH – 16	VML - 16	1110000	VMH + 48	VML + 48 VML + 49
		0110001 0110010	VMH – 15 VMH – 14	VML – 15 VML – 14	1110001	VMH + 49 VMH + 50	VML + 49
		0110010	VMH – 14	VML – 14	1110010	VMH + 50	VML + 50
		0110100	VMH – 12	VML – 13	1110100	VMH + 52	VML + 51
	L	23.00	· · · · · -	, <u></u>			

The information contained herein is the exclusive property of ILI Technology Corp. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of ILI Technology Corp.





	011010	1/1/11	\/AAL 44		4440404	\ /4	411 50	\/A/I		\neg
	0110101		VML – 11	_	1110101		/IH + 53	VML + 53		
	0110110		VML – 10	1	1110110		/IH + 54	VML + 54		
	0110111		VML – 9		1110111		ЛН + 55	VML + 55		
	0111000		VML – 8		1111000		ЛН + 56	VML + 56		
	0111001		VML – 7		1111001		ЛH + 57	VML + 57		
	0111010		VML – 6		1111010		ЛH + 58	VML + 58		
	0111011		VML – 5		1111011		ЛН + 59	VML + 59		
	0111100		VML – 4		1111100		ЛH + 60	VML + 60		
	0111101	VMH – 3	VML – 3		1111101	V٨	/IH + 61	VML + 61	_	
	0111110) VMH – 2	VML – 2		1111110	V٨	ЛH + 62	VML + 62	_	
	0111111	VMH – 1	VML – 1		1111111	V٨	ИН + 63	VML + 63		
										_
Restriction	EXTC should be high to enable	e this command								
										-
	Г		Ctatu				Availabili	.		
	-		Statu				Availabili	ıy		
Dogistor		Normal Mode (ON, Idle M	ode (OFF, Sleep	OUT	Yes			
Register		Normal Mode	ON, Idle M	ode (ON, Sleep	OUT	Yes			
Availability		Partial Mode C	N, Idle Mo	de C	FF, Sleep	OUT	Yes			
		Partial Mode (ON. Idle M	ode (N. Sleep	OUT	Yes			
			Sleep		,		Yes			
	L		Sieep	IIN			168			
										\dashv
					Defa	ılt Valu	10			
		Status	;							
					nVM	VN	ИF [6:0]			
Default		Power ON Se	equence		1'b1	7	"h40h			
		SW Res	set		1'b1	7	"h40h			
		HW Res	set		1'b1	7	"h40h			
1					. ~ .			_		





8.3.20. NV Memory Write (D0h)

D0h							NVM	IWR (N	/ Memory	/ Write)					
	D/CX	RDX	WRX	D17	' -8	D7	7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	<	1		1	0	1	0	0	0	0	D0h
1 st Parameter	1	1	↑	XX	<	0		0	0	0	0	PG	M_ADR [2:0]	00
2 nd Parameter	1	1	↑	XX	<					PGM_I	DATA [7:0]				XX
	This co	mmand	is used to	progran	n the N	V mer	nory	data. Af	ter a succ	essful M	1TP operat	ion, the in	formation	of PGM_	DATA
	[7:0] w	ill progra	mmed to	NV mem	ory.										
	PGM_	ADR [2:0	0] : The se	lect bits	of ID1,	ID2, II	D3 ar	nd VMF	[6:0] prog	rammin	g.				
				Г	PGM_	ADR [[2:0]	Progra	ammed N	V Memo	ory Selection	on			
Description					0	0	0		ID1 pr	ogramm	ing				
					0	0	1			ogramm					
					0	1	0		ID3 pr	ogramm	ing				
					1	0	0		VMF [6:0] prograi	mming				
l		Others Reserved													
Restriction		PGM_DATA [7:0]: The programmed data. EXTC should be high to enable this command													
								Status			Availal	oility			
				N	ormal M	Anda (e OFF, SI	een OH					
Register									le ON, Sle						
Availability									OFF, SI						
Availability									e ON, Sle						
								leep IN	•	•	Yes				
ı					C	tatus			D	efault Va	alue				
					31	lalus		PGI	M_ADR [2	2:0] P	GM_DATA	[7:0]			
Default				Po	wer Ol	V Seq	uenc	е	3'b000		MTP valu	е			
					SW	Rese	t		3'b000		MTP valu				
					HW	Rese	t		3'b000		MTP valu	е			





8.3.21. NV Memory Protection Key (D1h)

D1h					NVMPI	KEY (NV	Memory	Protection I	(ey)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	1	1	0	1	0	0	0	1	D1h		
1 st Parameter	1	1	1	XX				KEY [2	3:16]				55h		
2 nd Parameter	1	1	1	XX				KEY [15:8]				AAh		
3 rd Parameter	1	1	↑	XX				KEY	7:0]				66h		
Description	_	- A66h to		y programming ITP programmi	•	•		•	•	Ü			ing will		
Restriction	EXTC	EXTC should be high to enable this command													
Register Availability		Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes													
Availability							ode ON,	Sleep OUT	Yes	3					
Default					Power O SW	tatus N Sequer Reset	KE	Default Valu Y [23:0]=55A Y [23:0]=55A Y [23:0]=55A	AA66h AA66h						





8.3.22. NV Memory Status Read (D2h)

Discription Discription Discription Discription Discription Discription Discription EXTC should be high to enable this command Discription EXTC should be high to enable this command Discription Discription EXTC should be high to enable this command Discription Discr	D2h					RDNVM	(NV N	Memory St	atus Read)				
1		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
1	Command	0	1	1	XX	1	1	0	1	0	0	1	0	D2h
Description The status bit of NV memory programming. Busy The status of NV memory The status bit of NV memory The status bit of NV memory The status The statu	1 st Parameter	1	1	1	XX	Х	Χ	Х	Х	Х	Х	Х	Х	
D1_CNT [2:0] / ID2_CNT [2:0] / ID3_CNT [2:0] / VMF_CNT [2:0]: NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory. D1_CNT [2:0] / ID2_CNT [2:0] Description D3_CNT [2:0] / VMF_CNT [2:0] Description D3_CNT [2:0] / VMF_CNT [2:0] Description D3_CNT [2:0] / VMF_CNT [2:0] Description D3_CNT [2:0] / VMF_CNT [2:0] Description D4_CNT [2:0] D4_C	2 nd Parameter	1	↑	1	XX	0		ID2_CNT [[2:0]	0		D1_CNT	[2:0]	XX
Description Description	3 rd Parameter	1	↑	1	XX	BUSY	١	/MF_CNT	[2:0]	0	I	D3_CNT	[2:0]	XX
Register Availability Register Availability Register Availability Register Availability Register Availability Register Availability Register Availability Partial Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Sleep IN Yes Pefault Value ID3_CNT ID2_CNT ID1_CNT VMF_CNT BUSY Power ON Sequence X X X X X X SW Reset X X X X X X	Description	automa	 utically aft	er writing	the PGM_DATA ID1_CN ID3_CN 0 0 1	T [2:0] to N T [2:0] / N Statu 0 0 1 1 1 amming. BUSY 0	D2_CN/MF_C	mory. NT [2:0] O 1 1 1 Status of N Idle	Avail No Programm Programm Programm	ription ability grammed med 1 time med 2 time med 3 time	e ess	. The bits	will increas	se "+1"
Normal Mode ON, Idle Mode OFF, Sleep OUT	Restriction	EXTC	should be	high to e	nable this comm	and								
Normal Mode ON, Idle Mode OFF, Sleep OUT							S							
Normal Mode ON, Idle Mode ON, Sleep OUT Yes					No mar al NA				La cara OLUT		ility			
Availability Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value ID3_CNT ID2_CNT ID1_CNT VMF_CNT BUSY Power ON Sequence X X X X X X X X X	Register													
Partial Mode ON, Idle Mode ON, Sleep OUT Yes	· ·													
Sleep IN Yes Status Default Value ID3_CNT ID2_CNT ID1_CNT VMF_CNT BUSY Power ON Sequence X X X X SW Reset X X X X	Availability													
Default Value					i aitiai ivid				еер ООТ					
Default Da	<u> </u>						пеер п	IN		165				
Default Da								-	Nofoult \/-					
Default Power ON Sequence X X X X X SW Reset X X X X X X					Status	ID3 C	NT				CNT	BLISY		
SW Reset X X X X X	Default			Powe	er ON Sequence		. 4 1							
				1.500										
	1			<u> </u>		1 7					<u>I</u>			





8.3.23. Read ID4 (D3h)

D3h						RDID4	(Read II	04)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	1	1	0	1	0	0	1	1	D3h		
1 st Parameter	1	↑	1	XX	Х	Х	Х	Х	Χ	Х	Χ	Χ	Χ		
2 nd Parameter	1	1	1	XX	0	0	0	0	0	0	0	0	00h		
3 rd Parameter	1	1	1	XX	1	0	0	1	0	0	1	1	93h		
4 th Parameter	1	1	1	XX	0	1	0	0	0	0	0	1	41h		
Description	The 2 nd	the 1 st parameter is dummy read period. the 2 nd parameter means the IC version. the 3 rd and 4 th parameter mean the IC model name. XTC should be high to enable this command													
Restriction	EXTC :	XTC should be high to enable this command													
Register Availability				Normal Partial N	Mode ON	, Idle Mod	de ON, SI e OFF, SI le ON, SI	leep OUT eep OUT eep OUT	Yes	S S S S					
Default					S	Status ON Sequ W Reset	ence 2	Default Val 24'h00934 4'h00934 4'h00934	1h 1h						





8.3.24. Positive Gamma Correction (E0h)

E0h					PGAM	CTRL (Po	sitive Ga	amma Con	trol)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h
1 st Parameter	1	1	1	XX	0	0	0	0		VP63	[3:0]		08
2 nd Parameter	1	1	↑	XX	0	0			VP62	[5:0]			
3 rd Parameter	1	1	↑	XX	0	0			VP61	[5:0]			
4 th Parameter	1	1	1	X	0	0	0	0		VP59	[3:0]		05
5 th Parameter	1	1	1	XX	0	0	0		\	/P57 [4:0]			
6 th Parameter	1	1	1	XX	0	0	0	0		VP50	[3:0]		09
7 th Parameter	1	1	1	XX	0			V	'P43 [6:0]				
8 th Parameter	1	1	1	XX		VP2	7 [3:0]			VP36	[3:0]		
9 th Parameter	1	1	1	XX	0			V	'P20 [6:0]				
10 th Parameter	1	1	1	XX	0	0	0	0		VP13	[3:0]		0B
11 th Parameter	1	1	1	XX	0	0	0		,	VP6 [4:0]			
12 th Parameter	1	1	1	XX	0	0	0	0		VP4	[3:0]		00
13 th Parameter	1	1	1	XX	0	0			VP2	[5:0]			
14 th Parameter	1	1	1	XX	0	0			VP1	[5:0]			
15 th Parameter	1	1	1	XX	0	0	0	0		VP0	[3:0]		00
Description	Set the	e gray scale voltage to adjust the gamma characteristics of the TFT panel.											
Restriction	EXTC	should l	be high to	o enable this co	ommand								
						Status			Availa	bility			
Desistan								Sleep OUT	Yes	S			
Register				Norma	al Mode O	N, Idle Mo	ode ON, S	Sleep OUT	Yes	S			
Availability				Partial	Mode ON	N, Idle Mo	de OFF, S	Sleep OUT	Yes	S			
				Partia	I Mode OI	N, Idle Mo	de ON, S	leep OUT	Yes	S			
						Sleep I	N		Yes	S			
Default													





8.3.25. Negative Gamma Correction (E1h)

E1h					NGAMCT	RL (Neg	ative Gar	nma Corre	ection)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	0	0	0	0	1	E1h
1 st Parameter	1	1	1	XX	0	0	0	0		VN63	[3:0]		08
2 nd Parameter	1	1	↑	XX	0	0			VN62	[5:0]			
3 rd Parameter	1	1	1	XX	0	0			VN61	[5:0]			
4 th Parameter	1	1	1	XX	0	0	0	0		VN59	[3:0]		07
5 th Parameter	1	1	1	XX	0	0	0		V	'N57 [4:0]			
6 th Parameter	1	1	1	XX	0	0	0	0		VN50	[3:0]		05
7 th Parameter	1	1	1	XX	0			,	/N43 [6:0]				
8 th Parameter	1	1	1	XX		VN3	6 [3:0]			VN27	[3:0]		
9 th Parameter	1	1	1	XX	0			,	/N20 [6:0]				
10 th Parameter	1	1	↑	XX	0	0	0	0		VN13	[3:0]		04
11 th Parameter	1	1	↑	XX	0	0	0		\	VN6 [4:0]			
12 th Parameter	1	1	1	XX	0	0	0	0		VN4	[3:0]		0F
13 th Parameter	1	1	↑	XX	0	0			VN2	[5:0]			
14 th Parameter	1	1	↑	XX	0	0			VN1	[5:0]			
15 th Parameter	1	1 1 ↑ XX 0 0 0 0 VN0 [3:0]											0F
Description Restriction		Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. EXTC should be high to enable this command											
						Status			Availal	oility			
				Normal	Mode Of			Sleep OUT	_				
Register								Sleep OUT					
Availability								Sleep OUT					
, wandomy								leep OUT	Yes				
						Sleep II			Yes	3			
						•							
Default													





8.3.26. Digital Gamma Control 1 (E2h)

E2h					DGAM	CTRL (Dig	ital Gam	ma Co	ontro	l 1)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4		D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	0		0	0	1	0	E2h
1 st Parameter	1	1	1	XX		RCA0	[3:0]				BC	A0 [3:0]		XX
:	1	1	1	XX		RCAx	[3:0]				BC	Ax [3:0]		XX
16 th Parameter	1	1	1	XX		RCA1	5 [3:0]				BCA	15 [3:0]		XX
Description				-	ment registe									
Restriction	EXTC	should b	e high to	enable this	s command									
Register Availability				Nor Par	mal Mode Of mal Mode O tial Mode Of tial Mode Of	N, Idle Mod I, Idle Mod	de ON, S e OFF, S le ON, Sl	leep C	OUT OUT	Availa Ye Ye Ye Ye	es es es			
5.6.1					Stat		RCAx		BCA	Ax [3:0]				
Default					Power ON		TB			TBD				
				ŀ	SW R		TB			ΓBD ΓBD	-			
				Į	HW F	eset	ТВ	ע	l	ΓBD	_			





8.3.27. Digital Gamma Control 2(E3h)

E3h					DGAM	CTRL (Dig	ital Gam	ma Co	ontrol	1 2)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4		D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	0		0	0	1	1	E3h
1 st Parameter	1	1	1	XX		RFA0	[3:0]				BF/	A0 [3:0]		XX
:	1	1	1	XX		RFAx	[3:0]				BF	Ax [3:0]		XX
64 rd Parameter	1	1	1	XX		RFA63	[3:0]				BFA	63 [3:0]		XX
Description		-		icro-adjustme icro-adjustme	•	-								
Restriction	EXTC:	should b	e high to	enable this o	command									
Register Availability				Norma Partia	al Mode O Il Mode ON	N, Idle Mod	de ON, S e OFF, S le ON, S	leep C leep C	TUC		98 98 98			
Default		Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Power ON Sequence Tellow Tellow Tellow												





8.3.28. Interface Control (F6h)

F6h		IFCTL (16bits Data Format Selection)													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h		
1 st Parameter	1	1	↑	XX	MY_ EOR	MX_ EOR	MV_ EOR	0	BGR_ EOR	0	0	WE MODE	01		
2 nd Parameter	1	1	1	XX	0	0	EPF [1]	EPF [0]	0	0	MDT [1]	MDT [0]	00		
3 rd Parameter	1	1	1	XX	0	0	ENDIAN	0	DM [1]	DM [0]	RM	RIM	00		

MY_EOR / MX_EOR / MV_EOR / BGR_EOR:

The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.

MDT [1:0]: Select the method of display data transferring.

WEMODE: Memory write control

WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

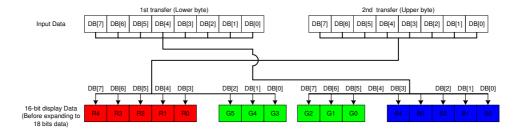
WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

ENDIAN: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

ENDIAN	Data transfer Mode
0	Normal (MSB first, default)
1	Little Endian (LSB first)

Note: Little Endian is valid on only 65K 8-bit and 9-bit MCU interface mode.

Description



DM [1:0]: Select the display operation mode.

DM [1]	DM [0]	Display Operation Mode
0	0	Internal clock operation
0	1	RGB Interface Mode
1	0	VSYNC interface mode
1	1	Setting disabled

The DM [1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.





RM: Select the interface to access the GRAM.

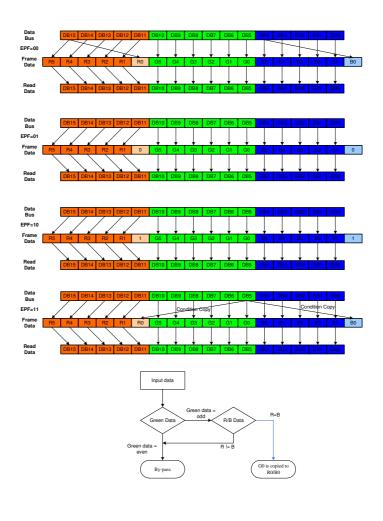
Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
_	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
0	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
	110 (262K color)	6- bit RGB interface (3 transfer/pixel)
l	101 (65K color)	6- bit RGB interface (3 transfer/pixel)

EPF [1:0]: 65K color mode data format.







EPF [1:0]										
00		EPF [-		Expand 16 bbp	(R,G,B) to	18bbp (R,G,B	3)		
1		00	$r [5:0] = \{F \\ g [5:0] = \{G \}$	R [4:0], R [4]} G [5:0]}						
"1" is inputted to LSB r [5:0] = {R [4:0], 1} g [5:0] = {R [4:0], 1} g [5:0] = {R [4:0], 1} g [5:0] = {R [4:0], 1} b [5:0] = {R [4:0], 1} b [5:0] = {R [4:0], 6 [0], 1} b [5:0] = {B [4:0], 6 [0], 1} b [5:0] = {B [4:0], 6 [0], 6 [5:0], 6 [5:0], 6 [5:0], 6 [5:0], 6 [5:0], 6 [5:0], 6 [5:0], 6 [5:0], 6 [6:0], 6 [0] c case 1: R=G=B → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [6], 6 [0]} c case 3: R=G≠B → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [6], 6 [0]} c case 3: R=G≠B → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [6], 6 [0]} c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [6], 6 [0]} c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [5:0] = {B [4:0], 8 [0]} c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [5:0] = {B [4:0], 8 [0]} c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [5:0] = {B [4:0], 8 [0]} c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [5:0] = {B [4:0], 8 [0]} c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [5:0], 6 [6] c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [6] c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [6] c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [6] c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [6] c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [6] c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [6] c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [6] c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [5:0], 6 [6] c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {G [5:0], 6 [5:0], 6 [5:0], 6 [6] c case 4: B=G≠R → r [5:0] = {R [4:0], R [4], g [5:0] = {R [4:0], R [4], g [5:0] = {R [4:0], R		01	r [5:0] = {F g [5:0] = {F b [5:0] = {F	R [4:0], 0} G [5:0]} B [4:0], 0}						
T S(0) = (R 4:0), 1} g S(0) = (B 5:0) = (B 5:0) = (B 5:0) = (B 4:0), 1} Exception: R 4:0], B 4:0] = 5*hoo → r S(0), b 5:0] = 6*hoo Compare R 4:0], G S(1), B 4:0] case: Case 1: R=G=B → r S(0) = (R 4:0), G 0]), g S(0) = (G S(0)), b S(0) = (B 4:0), G 0]) Case 2: R=B≠G → r S(0) = (R 4:0), R 4]), g S(0) = (G S(0)), b S(0) = (B 4:0), B 0]) Case 3: R=G≠B → r S(0) = (R 4:0), R 4]), g S(0) = (G S(0)), b S(0) = (B 4:0), G 0]) Case 4: B=G≠R → r S(0) = (R 4:0), R 4]), g S(0) = (G S(0)), b S(0) = (B 4:0), G 0]) Restriction EXTC should be high to enable this command Status					5:0], b[5:0] = 6'	h3F				
R (4·0) = 5/100 → r (5·0) o c c c c c c c c c		10	r [5:0] = {F g [5:0] = {0	R [4:0], 1} G [5:0]}						
Compare R [4:0], G [5:1], B [4:0] case: Case 1: R=G=B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 2: R=B≠G → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 3: R=G≠B → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} \ Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b [5:0] = {G [5:0]}, b					5:0], b[5:0] = 6'	h00				
Status		11	Compare Case 1: R Case 2: R Case 3: R	R [4:0], G [5:1], B =G=B \rightarrow r [5:0] = =B \neq G \rightarrow r [5:0] = =G \neq B \rightarrow r [5:0] =	[4:0] case: {R [4:0], G [0]}, {R [4:0], R [4]}, {R [4:0], G [0]},	g [5:0] = {G g [5:0] = {G g [5:0] = {G	[5:0]}, b [5:0] [5:0]}, b [5:0]	= {B [4:0], B = {B [4:0], B	i [0]} i [0]}	
Normal Mode ON, Idle Mode OFF, Sleep OUT	Restriction	EXTC shoul	d be high to enabl	e this command						
Normal Mode ON, Idle Mode OFF, Sleep OUT					Status		Availab	ility		
Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes				Normal Mode Ol	N, Idle Mode O	FF, Sleep O				
Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes	Register									
Sleep IN Yes Sleep IN Yes Status EPF [1:0] MDT [1:0] ENDIAN WEMODE DM [1:0] RM RIM Power ON Sequence 2'b00 2'b00 1'b0 1'b1 2'b00 1'b0 1'b0 SW Reset 2'b00 2'b00 1'b0 1'b1 2'b00 1'b0	Availability									
Status EPF [1:0] MDT [1:0] ENDIAN WEMODE DM [1:0] RM RIM				rariiai iviode Ol		іч, біеер ОС				
Status EPF [1:0] MDT [1:0] ENDIAN WEMODE DM [1:0] RM RIM		ĺ	'							
Status EPF [1:0] MDT [1:0] ENDIAN WEMODE DM [1:0] RM RIM										
Default Power ON Sequence 2'b00 2'b00 1'b0 1'b1 2'b00 1'b0 1'b0 SW Reset 2'b00 2'b00 1'b0 1'b1 2'b00 1'b0 1'b0						Default	· Value			
SW Reset 2'b00 2'b00 1'b0 1'b1 2'b00 1'b0 1'b0			Status	EPF [1:0]	MDT [1:0]			DM [1:0]	RM	RIM
HW Reset 2'b00 2'b00 1'b0 1'b1 2'b00 1'b0 1'b0	Default	Po				ENDIAN	WEMODE			
	Default	Po	wer ON Sequence	2'b00	2'b00	ENDIAN 1'b0	WEMODE 1'b1	2'b00	1'b0	1'b0





8.4 Description of Extend register command

8.4.1 Power control A (CBh)

Discription Discription Description Description Description Description Description Description EXTC should be high to enable this command Description EXTC should be high to enable this command Description EXTC should be high to enable this command Description EXTC should be high to enable this command Description Description EXTC should be high to enable this command Description Description EXTC should be high to enable this command Description Description EXTC should be high to enable this command Description Description EXTC should be high to enable this command Description Description Description EXTC should be high to enable this command Description D	CBh							Power of	ontrol A						
Command		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D	2	D1	D0	HEX
Parameter	Command	0	1	1	XX	1	1	1	1	0	1		1	0	CBh
3	1 st Parameter	1	1	1	XX	0	0	1	1	1	0		0	1	39
## Parameter		1	1	1	XX	0	0	1	0	1	1		0	0	2C
Segretaria		1	1	1	XX	0	0	0	0	0	0	-			00
REG_VD[2:0]: vcore control				1								R			
Description	^{5rd} Parameter	1	1	1	XX	0	0	0	0	0			VBC[2:0]		02
Status	Description	REG_ 000 001 010 101 100 111 VBC[2: VBC[4] 000 001 010 110 110 111 100 101 110	VD[2:0]	Vc 1.5 1.4 1.5 1.6 1.7 res res h contro DE 5.8 5.7 5.6 5.5 5.4 5.2	ore(V) 555 4 55 65 65 64 66 66 67 66 67 67 67 66 66 66 66 66 66										
Normal Mode ON, Idle Mode OFF, Sleep OUT Yes	Restriction	EXTC s	should b	e high to	enable t	his cor	nmand								
Normal Mode ON, Idle Mode OFF, Sleep OUT Yes								Status			Availabil	itv			
Availability Partial Mode ON, Idle Mode OFF, Sleep OUT Yes					١	Normal	Mode ON,		OFF, Slee	ep OUT		,			
Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes	Register					Vormal	Mode ON,	Idle Mode	ON, Slee	p OUT	Yes				
Sleep IN Yes Sleep IN Yes Default Value Parameter1 Parameter2 Parameter3 Parameter4 Parameter5 Power ON Sequence 39 2C 00 34 02 SW Reset 39 2C 00 34 02	Availability					Partial	Mode ON,	Idle Mode (OFF, Slee	p OUT	Yes				
Status Default Value Parameter Par						Partial	Mode ON,	Idle Mode	ON, Slee	p OUT	Yes				
Default Parameter Paramete								Sleep IN			Yes				
Parameter1 Parameter2 Parameter3 Parameter4 Parameter5				_					De	efault Val	ue _				
SW Reset 39 2C 00 34 02				Status		Par	ameter1	Paramet	er2 P	arameter	3 Par	amet	er4 Pa	arameter5	
	Default		Powe	r ON Se	quence		39	2C		00		34		02	
HW Reset 39 2C 00 34 02				SW Res	et		39	2C		00		34		02	
				HW Res	et		39	2C		00		34		02	





8.4.2 Power control B (CFh)

CFh	Power control B												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	0	0	1	1	1	1	CFh
1 st Parameter	1	1	1	XX	0	0	0	0	0	0	0	0	00
2 nd Parameter	1	1	1	XX	1	0	0	Power cor	trol[1:0]	0	0	1	81
3 rd Parameter	1	1	1	XX	0	0	1	DC_ena	0	0	0	0	30
Description	Only se BT [2 0 0 0 0 0 1 0 1	etting po	DDVDH	VGH VCI x T	11, the VGL VGL -VC -VC -VC -VC	X 4	VGL voltage le high for E			below.			
Restriction	EXTC :	should b	e high to	o enable	this com	mand							
							Status		Ava	ailability			
				1	Normal I	Mode ON,	Idle Mode C	FF, Sleep O		Yes			
Register					Normal	Mode ON	, Idle Mode C	ON, Sleep Ol	JT	Yes			
Availability							Idle Mode O			Yes			
					Partial I	Mode ON,	Idle Mode C	N, Sleep OL	JT	Yes			
							Sleep IN			Yes			
								Defaul	t Value				
					Status		Parameter	1 Param	neter2	Paramet	ter3		
Default				Power	ON Seq	uence	00	А	2	F0			
				S	W Rese	t	00	А	2	F0			
				H	W Rese	t	00	A	2	F0			





8.4.3 Driver timing control A (E8h)

F6h					Dri	ver timi	ng cont	rol A					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	WRX ↑	XX	1	1	1	0	1	0	0	0	E8h
1 st Parameter	1	1	<u> </u>	XX	1	0	0	0	0	1	0	NOW	84
2 nd Parameter	1	1	<u> </u>	XX	0	0	0	EQ	0	0	0	CR	11
3 rd Parameter	1	1	↑	XX	0	1	1	1	1	0	PC[1:	1	7A
Description	0:default r 1:default - 2 nd param 0: default f param 0: default f 1:default f	eter:EQ tin - 1unit EQ timing eter:CR tin - 1unit CR timing	ning control ning control arge timing		g control								
	01:default 00:default	– 1unit	e uning										
Restriction	00:default	– 1unit – 2unit	n to enable	this comma	and								
Restriction	00:default	– 1unit – 2unit		this comma	and								
Restriction	00:default	– 1unit – 2unit		this comma		tus				Avai	lability		
	00:default	– 1unit – 2unit	n to enable No	rmal Mode	Sta	Mode O				Y	'es		
Register	00:default	– 1unit – 2unit	n to enable No No	rmal Mode	Sta ON, Idle ON, Idle	Mode O Mode C	N, Slee	o OUT		Y	'es 'es		
	00:default	– 1unit – 2unit	n to enable No No Pa	rmal Mode rmal Mode rtial Mode	Sta ON, Idle ON, Idle ON, Idle	Mode O Mode C Mode Ol	N, Slee	p OUT p OUT		Y	'es 'es		
Register	00:default	– 1unit – 2unit	n to enable No No Pa	rmal Mode	Sta ON, Idle ON, Idle ON, Idle	Mode O Mode C Mode Ol Mode O	N, Slee	p OUT p OUT		Y Y Y	'es 'es 'es		
Register	00:default	– 1unit – 2unit	n to enable No No Pa	rmal Mode rmal Mode rtial Mode	Sta ON, Idle ON, Idle ON, Idle	Mode O Mode C Mode Ol	N, Slee	p OUT p OUT		Y Y Y	'es 'es		
Register	00:default	– 1unit – 2unit	No No Pa Pa	rmal Mode rmal Mode rtial Mode artial Mode	Sta ON, Idle ON, Idle ON, Idle	Mode O Mode C Mode Ol Mode O	N, Slee F, Slee N, Sleep	p OUT p OUT		Y Y Y	'es 'es 'es		
Register	00:default	– 1unit – 2unit	n to enable No No Pa	rmal Mode rmal Mode rtial Mode artial Mode	Sta ON, Idle ON, Idle ON, Idle	Mode O Mode O Mode O Mode O p IN	N, Slee FF, Slee N, Sleep Defa	OUT OUT		Y Y Y	'es 'es 'es 'es		
Register	00:default	– 1unit – 2unit	No No Pa Pa	rmal Mode rmal Mode rtial Mode artial Mode	State ON, Idle ON, Idle ON, Idle ON, Idle Slee	Mode O Mode O Mode O Mode O p IN	N, Slee FF, Slee N, Sleep Defa	p OUT p OUT OOUT		Y Y Y Y	'es 'es 'es 'es		
Register Availability	00:default	– 1unit – 2unit	No No Pa Statu	rmal Mode rmal Mode rtial Mode artial Mode ON ence	Sta ON, Idle ON, Idle ON, Idle Slee	Mode O Mode O Mode O Mode O p IN	N, Slee FF, Slee N, Sleep Defa	p OUT p OUT D OUT ult Value ameter2		Y Y Y Y	'es 'es 'es 'es		





8.4.4 Driver timing control B (EAh)

F6h						ı	Oriver timin	g control B					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	0	1	0	1	0	EAh
1 st Parameter	1	1	1	XX	VG_	SW_T4	VG_S	SW_T3	VG_S	W_T2	VG_	SW_T1	66
2 nd Parameter	1	1	1	XX	Χ	X	Χ	Х	Х	X	0	0	00
Description	VG_SV VG_SV VG_SV	V_T1[1: V_T2[1: V_T3[1: V_T4[1: nit nit	0]:EQ to 0]:EQ to	DDVDH DDVDH	control								
Restriction	EXTC	should b	e high to	o enable t	this com	nmand							
							Status			lability			
Register								OFF, Sleep O		/es			
								ON, Sleep Ol OFF, Sleep Ol		/es /es			
Availability								DFF, Sleep Ot DN, Sleep Ot		res /es			
					i aitidi	ivioue OIN,	Sleep IN	Jiv, Oleep OC		res res			
Default					5	Status ON Sequ SW Reset		Defaul arameter1 66 66 66	t Value Parame 00 00 00	eter2			





8.4.5 Power on sequence control (EDh)

D/CX 0 1	RDX	WRX	D17-	D.	7	_	Т						
1	1			_	1	D6	D5	D4	D3	D2	D1	D0	HEX
		↑	XX	1		1	1	0	1	1	0	1	EDh
	1	<u> </u>	XX	Х	(1	CP1 sof	t start	Х	1	CP23 s	soft start	55
1	1	1	XX	Х		0	En_\	/cl	Х	0	En_o	ddvdh	01
1	1	1	XX	Х		0	En_v		Х	0	En	_vgl	23
1	1	1	XX	DDVDF	I_ENH	0	0	0	0	0	0	1	1
00:soft 01:soft 11:disa 2 nd / 3 rd 00:1 st fi 01:2 nd f 11:4 th f 4 th para 0: disal	start ke start ke start ke start ke ble parame rame en frame er rame er rame er rame er	ep 2 fran ep 1 fran ter:powe able nable nable	ne ne er on sequ			ernal cap	acitors)						
EXTC :	should b	e high to	enable th	nis comma	and								
						24-4			A. add 1	lia.			
			N	ormal Mo			OFF Sleen	OLIT		iity			
									Yes				
									Yes				
									Yes				
					S	leep IN			Yes				
				t	Parame 55 55 55	ter1				3 Par	01 01 01		
	01:soft 01:soft 11:disa 2 nd / 3 rd 00:1 st fr 01:2 nd f 11:4 th f 4 th para 0: disal 1: enab	01:soft start ke 01:soft start ke 11:disable 2 nd / 3 rd parame 00:1 st frame en 01:2 nd frame en 11:4 th frame en 4 th parameter:E 0: disable 1: enable	01:soft start keep 2 fram 01:soft start keep 1 fram 11:disable 2 nd / 3 rd parameter:power 00:1 st frame enable 01:2 nd frame enable 10:3 rd frame enable 11:4 th frame enable 0: disable 1: enable EXTC should be high to	2 nd / 3 rd parameter:power on sequence of the parameter of sequence of the parameter of the parameter:DDVDH enhance of the parameter:DDVDH enhance of the parameter of the par	01:soft start keep 2 frame 01:soft start keep 1 frame 11:disable 2nd/ 3rd parameter:power on sequence confidence of the	01:soft start keep 2 frame 01:soft start keep 1 frame 11:disable 2nd/3rd parameter:power on sequence control 00:1st frame enable 01:2nd frame enable 10:3rd frame enable 11:4th frame enable 11:4th parameter:DDVDH enhance mode(only for 8 externable) 1: enable EXTC should be high to enable this command EXTC should be high to enable this command Ormal Mode ON, Id Partial Mode ON, Id Partial Mode ON, Id Partial Mode ON, Id Status Parame Power ON Sequence 55 SW Reset 55	01:soft start keep 2 frame 01:soft start keep 1 frame 11:disable 2nd/ 3rd parameter:power on sequence control 00:1st frame enable 01:2nd frame enable 10:3rd frame enable 11:4th frame enable 11:4th parameter:DDVDH enhance mode(only for 8 external cap 0: disable 1: enable EXTC should be high to enable this command Status Normal Mode ON, Idle Mode Normal Mode ON, Idle Mode Partial Mode ON, Idle Mode Partial Mode ON, Idle Mode Sleep IN Status Parameter1 Power ON Sequence 55 SW Reset 55	01:soft start keep 2 frame 01:soft start keep 1 frame 11:disable 2nd/3d parameter:power on sequence control 00:1st frame enable 01:2nd frame enable 10:3d frame enable 11:4th frame enable 11:4th frame enable 11:enable EXTC should be high to enable this command Status Normal Mode ON, Idle Mode OFF, Sleep Partial Mode ON, Idle Mode OFF, Sleep Partial Mode ON, Idle Mode ON, Sleep Partial Mode ON, Idle Mode ON, Sleep Partial Mode ON, Idle Mode ON, Sleep Sleep IN Status Status Power ON Sequence 55 01 SW Reset 55 01	01:soft start keep 2 frame 01:soft start keep 1 frame 11:disable 2 nd / 3 rd parameter:power on sequence control 00:1st frame enable 01:2 nd frame enable 10:3 rd frame enable 11:4 th frame enable 11:4 th frame enable 1: enable EXTC should be high to enable this command Status Normal Mode ON, Idle Mode OFF, Sleep OUT Partial Mode ON, Idle Mode OFF, Sleep OUT Partial Mode ON, Idle Mode ON, Sleep OUT Partial Mode ON, Idle Mode ON, Sleep OUT Sleep IN Status Default Val Parameter: Power ON Sequence 55 01 SW Reset 55 01	01:soft start keep 2 frame 01:soft start keep 1 frame 11:disable 2nd/3rd parameter:power on sequence control 00:1nd frame enable 01:2nd frame enable 10:3rd frame enable 11:4th frame enable 11:4th frame enable 11:4th parameter:DDVDH enhance mode(only for 8 external capacitors) 0: disable 1: enable EXTC should be high to enable this command Status Availabit Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Status Default Value Parameter: Param	01:soft start keep 1 frame 01:soft start keep 1 frame 11:disable 2nd/31d parameter:power on sequence control 00:1st frame enable 10:3rd frame enable 11:4th frame enable 11:4th frame enable 4th parameter:DDVDH enhance mode(only for 8 external capacitors) 0: disable 1: enable EXTC should be high to enable this command EXTC should be high to enable this command EXTC should be high to enable this command Partial Mode ON, Idle Mode OFF, Sleep OUT	01:soft start keep 1 frame 11:disable 2nd/3rd parameter:power on sequence control 00:1nd frame enable 11:2nd frame enable 11:2nd frame enable 4nd parameter:DDVDH enhance mode(only for 8 external capacitors) 0: disable 1: enable EXTC should be high to enable this command EXTC should be high to enable this command Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes Sleep IN Yes Power ON Sequence 55 01 23 01 SW Reset 55 01 23 01	01:soft start keep 2 frame 01:soft start keep 1 frame 11:disable 2 rd / 3 rd parameter:power on sequence control 00:1 rd frame enable 01:2 rd frame enable 10:3 rd frame enable 11:4 th frame enable 11:4 th frame enable 11:4 th frame enable 11:4 th frame enable 11:4 th frame enable 11:4 th parameter:DDVDH enhance mode(only for 8 external capacitors) 0: disable 1: enable EXTC should be high to enable this command Status





8.4.6 Enable 3G (F2h)

F6h		<u> </u>					Enab	le_3G	à					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	[D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1		1	0	0	1	0	F2h
1 st Parameter	1	1	↑	XX	0	0	0		0	0	0	1	3G_enb	02
Description				le 3 gam amma co										
Restriction	EXTC	should b	oe high t	o enable t	this con	nmand								
							Status			Δ.	vailability			
					Normal	Mode ON	, Idle Mode	OFF, S	Sleep C	DUT	Yes			
Register					Normal	Mode ON	I, Idle Mode	ON, S	Sleep O	UT	Yes			
Availability							Idle Mode (Yes			
				_	Partial	Mode ON	, Idle Mode	ON, S	Sleep O	UT	Yes			
							Sleep IN				Yes			
Default						S	Status ON Sequent W Reset W Reset	ce	Para	ult Value meter1 02 02 02				





8.4.7 Pump ratio control (F7h)

F6h	Pump ratio control													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	1	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	1		0	1	1	0	F7h
1 st Parameter	1	1	1	XX	Χ	Χ	Ratio	[1:0]		0	0	0	0	10
Description	00:rese	erved		trol										
Restriction	EXTC should be high to enable this command													
							Status			Ava	ilability			
Deviates				1	Normal Mode ON, Idle Mode OFF, Sleep OUT						Yes			
Register							, Idle Mode (Yes			
Availability							Idle Mode O				Yes			
					Partial	Mode ON,	Idle Mode C	N, Slee	ep OUT		Yes			
							Sleep IN			`	Yes			
Default	Status Default Value Parameter1 Power ON Sequence 10 SW Reset 10 HW Reset 10													

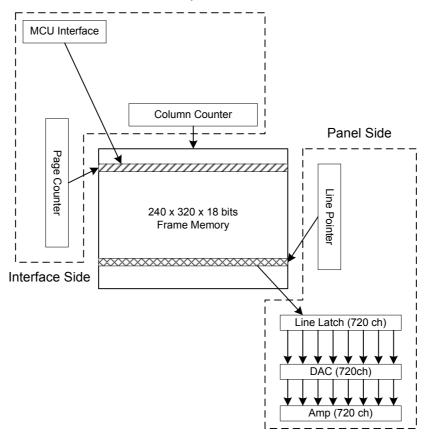




9. Display Data RAM

9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.





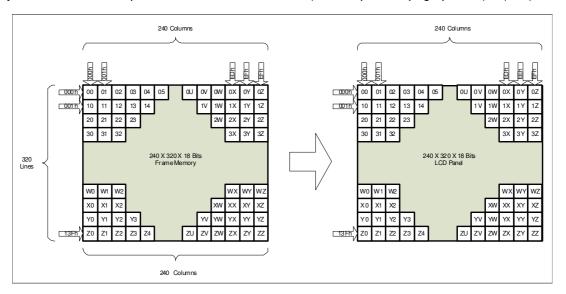


9.2. Memory to Display Address Mapping

9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)





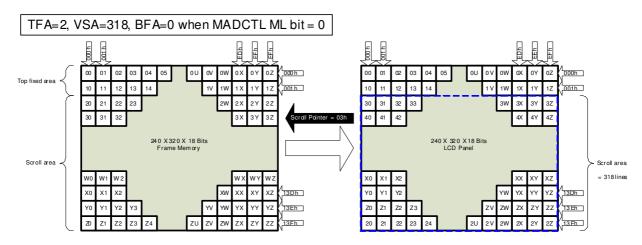


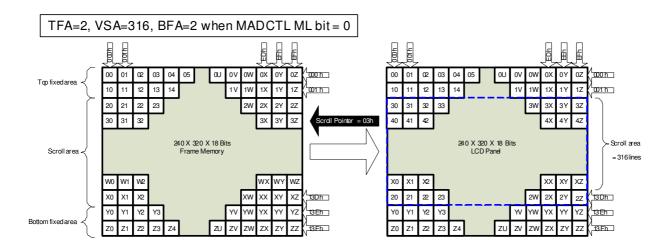


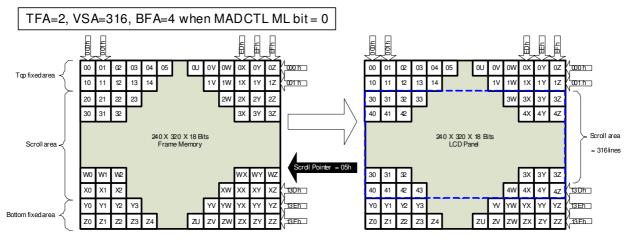
9.2.2. Vertical Scroll Mode

There is a vertical scrolling mode, which is determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

The Vertical Scroll Mode function is explained by these examples in the following.







Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.





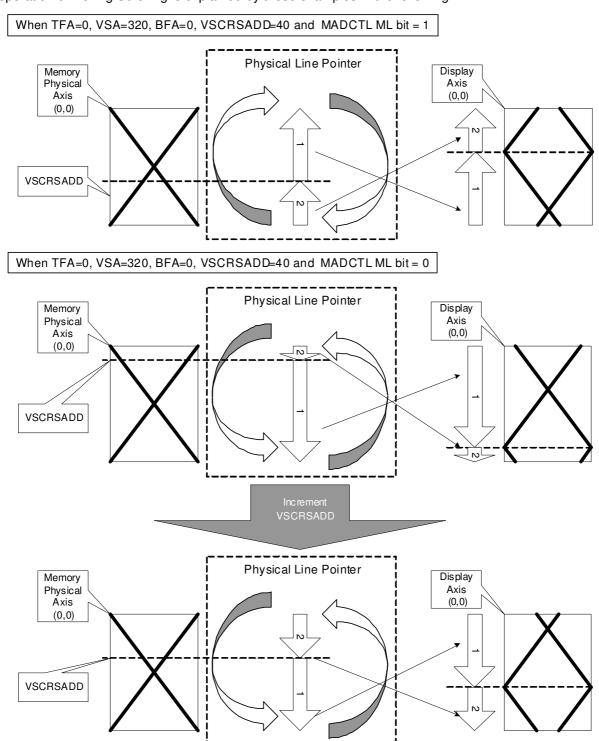
9.2.3. Vertical Scroll Example

9.2.4. Case1: TFA+VSA+BFA < 320

This setting is prohibited, unless unexpected picture will be shown.

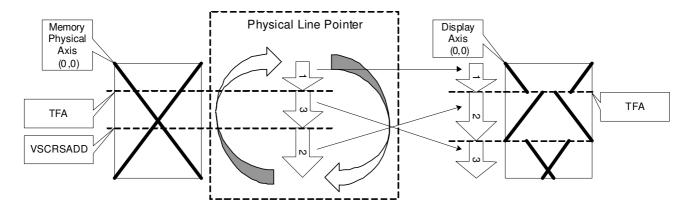
9.2.5. Case2: TFA+VSA+BFA = 320 (Rolling Scrolling)

The operation of Rolling Scrolling is explained by these examples in the following.

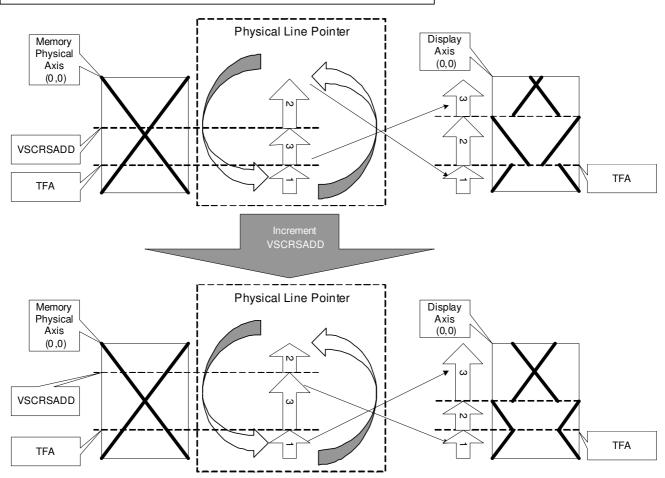




When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



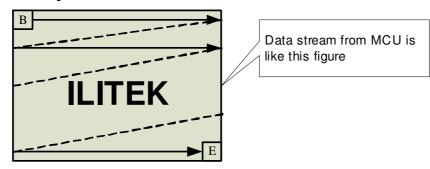
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



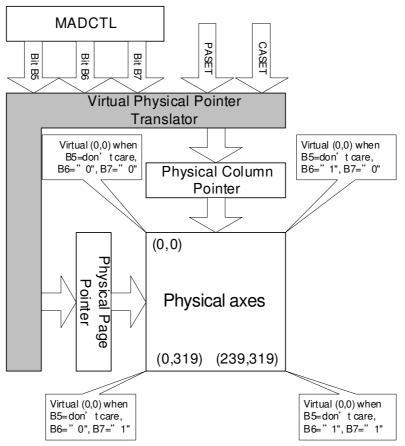




9.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, Bits B5, B6, and B7 as described below.



B5	B6	B7	CASET			PASET		
0	0	0	Direct to Physical Column F	Pointer	Direct to Physical Page Pointer			
0	0	1	Direct to Physical Column F	Pointer	Direct to (319-Physical Page Pointer)			
0	1	0	Direct to (239-Physical Col	umn Pointer)	Direct to Phy	sical Page Pointer		
0	1	1	Direct to (239-Physical Col	umn Pointer)	Direct to (319	P-Physical Page Pointer)		
1	0	0	Direct to Physical Page Poi	inter	Direct to Physical Column Pointer			
1	0	1	Direct to (319-Physical Pag	je Pointer)	Direct to Physical Column Pointer			
1	1	0	Direct to Physical Page Poi	inter	Direct to (239-Physical Column Pointer)			
1	1	1	Direct to (319-Physical Pag	je Pointer)	Direct to (239-Physical Column Pointer)			
		Col	ndition	Column	Counter	Page counter		
Whe	n RAMW	'R/RAMF	RD command is accepted	Return to "Sta	art column"	Return to "Start Page"		
	Comple	ete Pixel	Read/Write action	Increment by	1	No change		
The (Column v	/alues is	large than "End Column"	Return to "Start column"		Increment by 1		
The	e Page c	ounter is	large than "End Page"	Return to "Sta	Return to "Start Page"			





Note:

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data	N P	IADCT aramete	'R er	Image in the Memory	Luciani da Dairea (Terres Marrana)
Direction	MV	MX	MY	(MPU)	Image in the Driver (Frame Memory)
Normal	0	0	0	B	Memory(0,0) B Counter(0,0)
Y-Mirror	0	0	1	B	Memory(0.0) E Counter(0.0)
X-Mirror	0	1	0	B	Memory(0,0) B Counter(0,0)
X-Mirror Y-Mirror	0	1	1	B	Memory(0,0) E Counter(0,0)
X-Y Exchange	1	0	0	B	Memor(0,0) B Counter(0,0)
X-Y Exchange Y-Mirror	1	0	1	B	Memory(0,0) E
XY Exchange X-Mirror	1	1	0	B	Memory(0,0) B Counter(0,0)
XY Exchange XY-Mirror	1	1	1	B	Memory(0,0) E Counter(0,0)





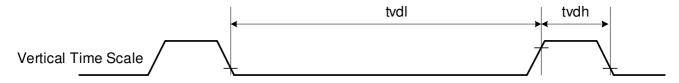
10. Tearing Effect Output

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

10.1. Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

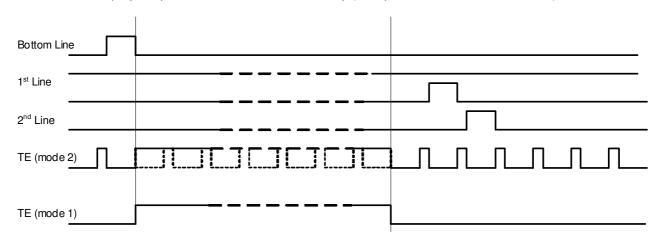
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 320 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

thdl = The LCD display is updated from the Frame Memory (except Invisible Line - see above).



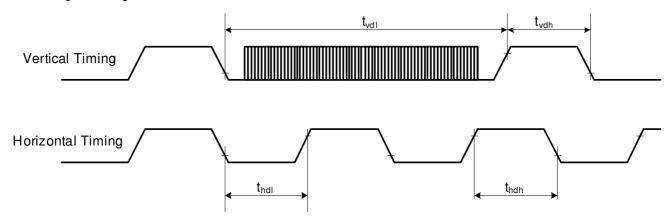
Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.





10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

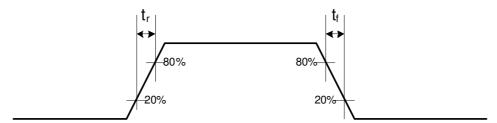


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration				ms	
$t_{\rm vdh}$	Vertical timing high duration	1000			us	
t _{hdl}	Horizontal timing low duration				us	
t _{hdh}	Horizontal timing high duration		-1	500	us	

Note:

- 1. The timings in Table as above apply when MADCTL B4=0 and B4=1
- 2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.





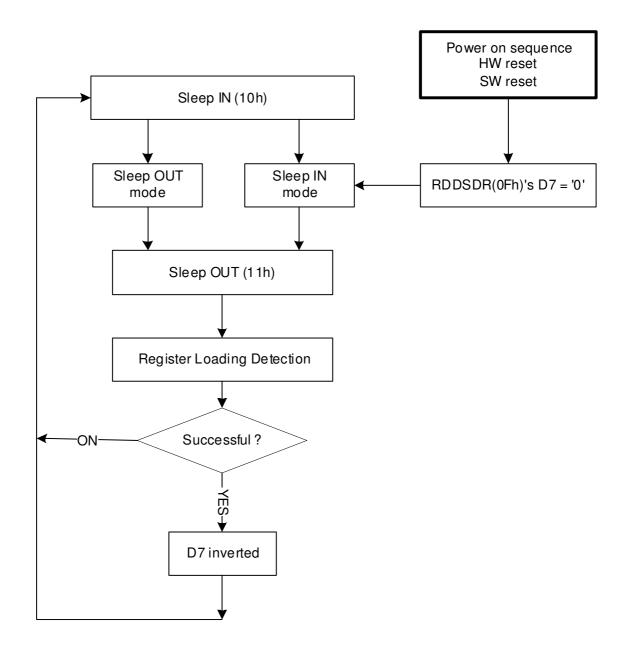
11. Sleep Out – Command and Self-Diagnostic Functions of the Display Module

11.1. Register loading Detection

Sleep Out-command (Command "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EV Memory(or similar device) to registers of the display controller is working properly.

If the register loading detection is successfully, there is inverted (= increased by 1) a bit, which is defined in command "Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D7). If it is failure, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:





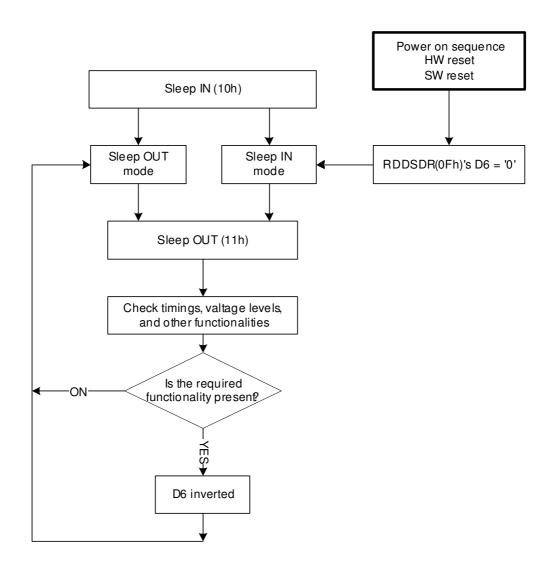


11.2. Functionality Detection

Sleep Out-command (Command "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In -mode to Sleep Out -mode, before there is possible to check if User's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out -command is sent in Sleep Out -mode.





12. Power ON/OFF Sequence

VDDI and VCI can be applied in any order.

VCI and VDDI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDDI must be powered down minimum 120msec after RESX has been released.

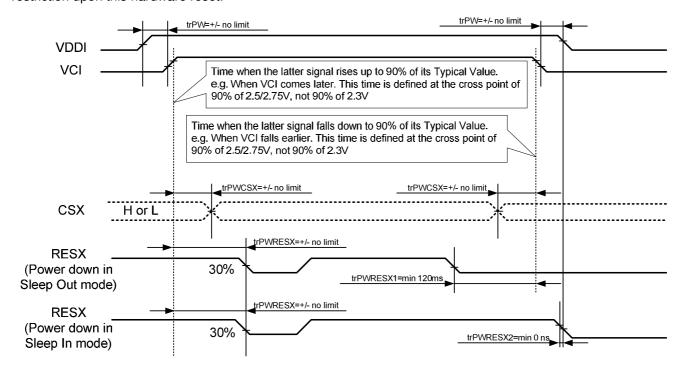
During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

- Note 1: There will be no damage to the display module if the power sequences are not met.
- Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
- Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
- Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode trPWRESX2 is applied to RESX falling in the Sleep In Mode

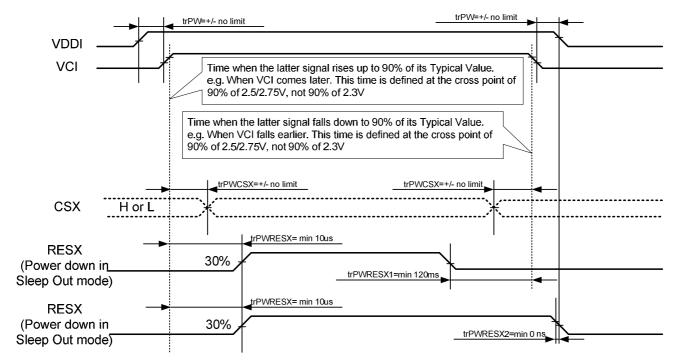
Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.





12.2. Case 2 – RESX line is held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and VDDI have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.





12.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9341 will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until "Power On Sequence" actives.





13. Power Level Definition

13.1. Power Levels

7 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

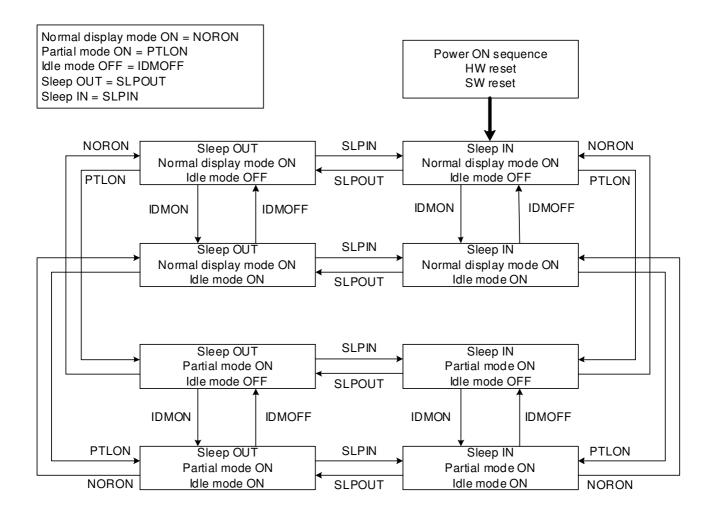
- 1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
 - In this mode, the display is able to show maximum 262,144 colors.
- 2. Partial Mode On, Idle Mode Off, Sleep Out.
 - In this mode part of the display is used with maximum 262,144 colors.
- 3. Normal Mode On (full display), Idle Mode On, Sleep Out.
 - In this mode, the full display area is used but with 8 colors.
- 4. Partial Mode On, Idle Mode On, Sleep Out.
 - In this mode, part of the display is used but with 8 colors.
- 5. Sleep In Mode.
 - In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
- 6. Power Off Mode.
 - In this mode, both VCI and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands.





13.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.





14. Gamma Curves Selection

ILI9341 provide one gamma curve Gamma2.2. The gamma curve can be selected by the GC0 settings.

14.1. Gamma Default Values (for NW type LC)

	י יטי, כ		ypc L	
Doto	VCOM		Voltage	Lliada
Data	VCOM :		VCOM =	
_	Gamma	2.2	Gamma	2.2
1	V0P V1P	4.084	V0N V1N	0.277
2	V1P V2P	4.015	V1N V2N	0.346
		3.843		0.482
3	V3P	3.681	V3N V4N	0.629
5	V4P V5P	3.518	V4N V5N	0.776 0.924
	VSF V6P	3.445	V6N	
7		3.371		1.071
8	V7P V8P	3.285	V7N V8N	1.157 1.242
9	V9P	3.128	V9N	1.314
10	V10P	3.056 2.985	V10N	1.385 1.456
11	V11P V12P	2.965	V11N V12N	
				1.513
13	V13P	2.871	V13N	1.570
14	V14P	2.802	V14N	1.619
15	V15P	2.733	V15N	1.668
16	V16P	2.674	V16N	1.710
17	V17P	2.615	V17N	1.753
18	V18P	2.557	V18N	1.795
19	V19P	2.508	V19N	1.830
20	V20P	2.458	V20N	1.865
21	V21P	2.425	V21N	1.899
22	V22P	2.391	V22N	1.932
23	V23P	2.357	V23N	1.966
24	V24P	2.323	V24N	2.000
25	V25P	2.289	V25N	2.034
26	V26P	2.256	V26N	2.068
27	V27P	2.222	V27N	2.102
28	V28P	2.193	V28N	2.129
29	V29P	2.165	V29N	2.155
30	V30P	2.136	V30N	2.182
31	V31P	2.108	V31N	2.208
32	V32P	2.080	V32N	2.235
33	V33P	2.051	V33N	2.262
34	V34P	2.023	V34N	2.288
35	V35P	1.994	V35N	2.315
36	V36P	1.966	V36N	2.342
37	V37P	1.942	V37N	2.368
38	V38P	1.917	V38N	2.395
39	V39P	1.893	V39N	2.421
40	V40P	1.869	V40N	2.448
41	V41P	1.845	V41N	2.475
42	V42P	1.820	V42N	2.501
43	V43P	1.796	V43N	2.528
44	V44P	1.776	V44N	2.549
45	V45P	1.755	V45N	2.571
46	V46P	1.730	V46N	2.597
47	V47P	1.706	V47N	2.623
48	V48P	1.681	V48N	2.649
49	V49P	1.653	V49N	2.679
50	V50P	1.624	V50N	2.710
51	V51P	1.598	V51N	2.735
52	V52P	1.573	V52N	2.761
53	V53P	1.541	V53N	2.793
54	V54P	1.508	V54N	2.825
55	V55P	1.476	V55N	2.857
56	V56P	1.438	V56N	2.895
57	V57P	1.400	V57N	2.933
58	V58P	1.359	V58N	2.982
59	V59P	1.319	V59N	3.031
60	V60P	1.246	V60N	3.109
61	V61P	1.173	V61N	3.186
62	V62P	1.070	V62N	3.289
63	V63P	0.279	V63N	4.083

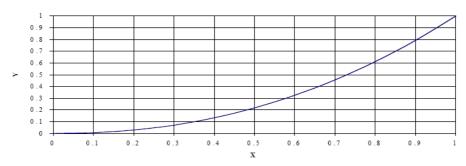




14.2. Gamma Curves

14.2.1. Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$



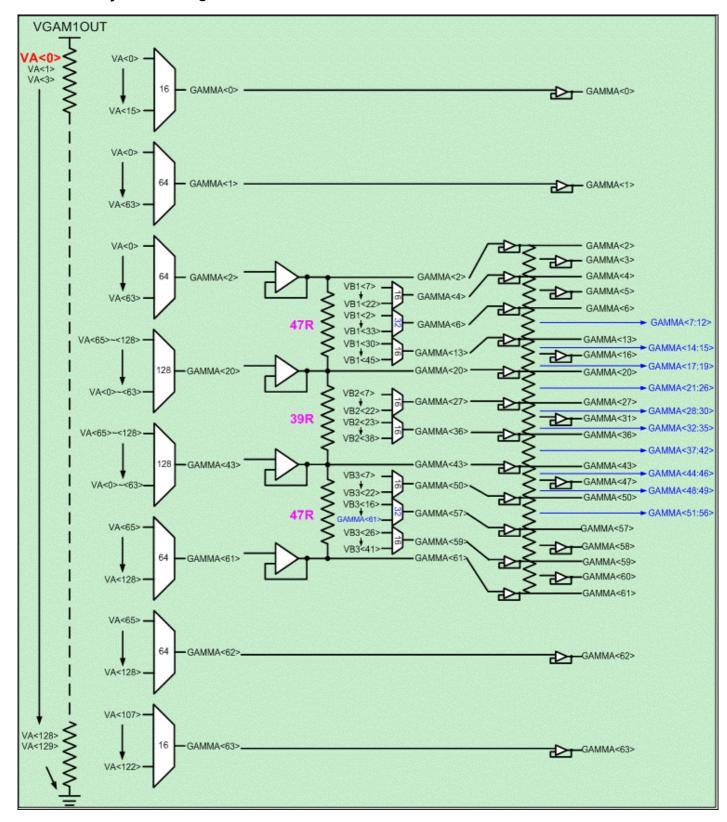






14.3. Gamma Curves

14.3.1. Grayscale Voltage Generation







14.3.2. Positive Gamma Correction

Gamma	Value "X"	Formula
Level VP0	in Formula VP0[3:0]	A/DEC4 \/CC*/430D \/*D\/430D
VP1	VP0[3.0] VP1[5:0]	(VREG1-VGS)*(130R-X*R)/130R (VREG1-VGS)*(130R-X*R)/130R
VP2	VP2[5:0]	(VREG1-VGS)*(130R-X*R)/130R
VP3	—	(VP2-VP4)*35R/(35R*2)+VP4
VP4	VP4[3:0]	(VP2-VP20)*(47R-X*R-7R)/47R+VP20
VP5		(VP4-VP6)*35R/(35R*2)+VP6
VP6	VP6[4:0]	(VP2-VP20)*(47R-X*R-2R)/47R+VP20
VP7	_	(VP6-VP13)*(12R+10R*3+8R*2)/(12R*2+10R*3+8R*2)+VP13
VP8	_	(VP6-VP13)*(10R*3+8R*2)/(12R*2+10R*3+8R*2)+VP13
VP9		(VP6-VP13)*(10R*2+8R*2)/(12R*2+10R*3+8R*2)+VP13
VP10		(VP6-VP13)*(10R+8R*2)/(12R*2+10R*3+8R*2)+VP13
VP11	_	(VP6-VP13)*(8R*2)/(12R*2+10R*3+8R*2)+VP13
VP12	_	(VP6-VP13)*8R/(12R*2+10R*3+8R*2)+VP13
VP13	VP13[3:0]	(VP2-VP20)*(47R-X*R-30R)/47R+VP20
VP14		(VP13-VP20)*(14R+12R*3+10R*2)/(14R*2+12R*3+10R*2)+VP20
VP15		(VP13-VP20)*(12R*3+10R*2)/(14R*2+12R*3+10R*2)+VP20
VP16		(VP13-VP20)*(12R*2+10R*2)/(14R*2+12R*3+10R*2)+VP20
VP17		(VP13-VP20)*(12R+10R*2)/(14R*2+12R*3+10R*2)+VP20
VP18		(VP13-VP20)*(10R*2)/(14R*2+12R*3+10R*2)+VP20
VP19		(VP13-VP20)*10R/(14R*2+12R*3+10R*2)+VP20
VP20	VP20[6:0]	<pre><64 (VREG1-VGS)*(130R-X*R)/130R >=64 (VREG1-VGS)*(130R-X*R-1R)/130R</pre>
VP21	<u></u>	(
VP21		(VP20-VP27)*(12R*6)/(12R*7)+VP27
VP23	<u> </u>	(VP20-VP27)*(12R*5)/(12R*7)+VP27 (VP20-VP27)*(12R*4)/(12R*7)+VP27
VP24		(VP20-VP27) (12R 4)/(12R 7)+VP27 (VP20-VP27)*(12R*3)/(12R*7)+VP27
VP25		(VP20-VP27) (12R 3)(12R 7)+VP27 (VP20-VP27)*(12R*2)/(12R*7)+VP27
VP26		(VP20-VP27) (12R 2) (12R 7)+VP27 (VP20-VP27)*12R/(12R*7)+VP27
VP27	VP27[3:0]	(VP20-VP43)*(39R-X*R-7R)/39R+VP43
VP28	— —	(VP27-VP36)*(8R*8)/(8R*9)+VP36
VP29	_	(VP27-VP36)*(8R*7)/(8R*9)+VP36
VP30	_	(VP27-VP36)*(8R*6)/(8R*9)+VP36
VP31	_	(VP27-VP36)*(8R*5)/(8R*9)+VP36
VP32	_	(VP27-VP36)*(8R*4)/(8R*9)+VP36
VP33	_	(VP27-VP36)*(8R*3)/(8R*9)+VP36
VP34	_	(VP27-VP36)*(8R*2)/(8R*9)+VP36
VP35	_	(VP27-VP36)*8R/(8R*9)+VP36
VP36	VP36[3:0]	(VP20-VP43)*(39R-X*R-23R)/39R+VP43
VP37	_	(VP36-VP43)*(12R*6)/(12R*7)+VP43
VP38		(VP36-VP43)*(12R*5)/(12R*7)+VP43
VP39	_	(VP36-VP43)*(12R*4)/(12R*7)+VP43
VP40		(VP36-VP43)*(12R*3)/(12R*7)+VP43
VP41		(VP36-VP43)*(12R*2)/(12R*7)+VP43
VP42		(VP36-VP43)*12R/(12R*7)+VP43
VP43	VP43[6:0]	<64 (VREG1-VGS)*(130R-X*R)/130R
VP44		>=64 (VREG1-VGS)*(130R-X*R-1R)/130R
VP45		(VP43-VP50)*(14R*2+12R*3+10R)/(14R*2+12R*3+10R*2)+VP50 (VP43-VP50)*(14R*2+12R*3)/(14R*2+12R*3+10R*2)+VP50
VP46		(VP43-VP50)*(14R*2+12R*3)*(14R*2+12R*3+10R*2)+VP50
VP47		(VP43-VP50)*(14R*2+12R)/(14R*2+12R*3+10R*2)+VP50
VP48		(VP43-VP50)*(14R*2+12R);(14R*2+12R*3+10R*2)+VP50
VP49	_	(VP43-VP50)*14R/(14R*2+12R*3+10R*2)+VP50
VP50	VP50[3:0]	(VP43-VP61)*(47R-X*R-7R)/47R+VP61
VP51	—	(VP50-VP57)*(12R*2+10R*3+8R)/(12R*2+10R*3+8R*2)+VP57
VP52	_	(VP50-VP57)*(12R*2+10R*3)/(12R*2+10R*3+8R*2)+VP57
VP53	_	(VP50-VP57)*(12R*2+10R*2)/(12R*2+10R*3+8R*2)+VP57
VP54	_	(VP50-VP57)*(12R*2+10R)/(12R*2+10R*3+8R*2)+VP57
VP55	_	(VP50-VP57)*(12R*2)/(12R*2+10R*3+8R*2)+VP57
VP56	_	(VP50-VP57)*12R/(12R*2+10R*3+8R*2)+VP57
VP57	VP57[4:0]	(VP43-VP61)*(47R-X*R-16R)/47R+VP61
VP58		(VP57-VP59)*35R/(35R*2)+VP59
VP59	VP59[3:0]	(VP43-VP61)*(47R-X*R-26R)/47R+VP61
VP60		(VP59-VP61)*35R/(35R*2)+VP61
VP61	VP61[5:0]	(VREG1-VGS)*(65R-X*R)/130R
VP62	VP62[5:0]	(VREG1-VGS)*(65R-X*R)/130R
VP63	VP63[3:0]	(VREG1-VGS)*(23R-X*R)/130R





14.3.3. Negative Gamma Correction

Gamma	Value "X"	Formula
Level VN63	in Formula VN63[3:0]	(VREG1-VGS)*(130R-X*R)/130R
VN62	VN62[5:0]	(VREG1-VGS)*(130R-X*R)/130R
VN61	VN61[5:0]	(VREG1-VGS)*(130R-X*R)/130R
VN60	— — — — — — — — — — — — — — — — — — —	(VN61-VN59)*35R/(35R*2)+VN59
VN59 VN58	VN59[3:0]	(VN61-VN43)*(47R-X*R-7R)/47R+VN43 (VN59-VN57)*35R/(35R*2)+VN57
VN57	VN57[4:0]	(VN61-VN43)*(47R-X*R-2R)/47R+VN43
VN56	—	(VN57-VN50)*(12R+10R*3+8R*2)/(12R*2+10R*3+8R*2)+VN50
VN55	_	(VN57-VN50)*(10R*3+8R*2)/(12R*2+10R*3+8R*2)+VN50
VN54	_	(VN57-VN50)*(10R*2+8R*2)/(12R*2+10R*3+8R*2)+VN50
VN53		(VN57-VN50)*(10R+8R*2)/(12R*2+10R*3+8R*2)+VN50
VN52	_	(VN57-VN50)*(8R*2)/(12R*2+10R*3+8R*2)+VN50
VN51 VN50		(VN57-VN50)*8R/(12R*2+10R*3+8R*2)+VN50
VN49	VN50[3:0] —	(VN61-VN43)*(47R-X*R-30R)/47R+VN43 (VN50-VN43)*(14R+12R*3+10R*2)/(14R*2+12R*3+10R*2)+VN43
VN48	_	(VN50-VN43)*(12R*3+10R*2)/(14R*2+12R*3+10R*2)+VN43
VN47	_	(VN50-VN43)*(12R*2+10R*2)/(14R*2+12R*3+10R*2)+VN43
VN46		(VN50-VN43)*(12R+10R*2)/(14R*2+12R*3+10R*2)+VN43
VN45		(VN50-VN43)*(10R*2)/(14R*2+12R*3+10R*2)+VN43
VN44		(VN50-VN43)*10R/(14R*2+12R*3+10R*2)+VN43
VN43	VN43[6:0]	<64 (VREG1-VGS)*(130R-X*R)/130R
VN42		>=64 (VREG1-VGS)*(130R-X*R-1R)/130R
VN41		(VN43-VN36)*(12R*6)/(12R*7)+VN36 (VN43-VN36)*(12R*5)/(12R*7)+VN36
VN40		(VN43-VN36)*(12R*4)/(12R*7)+VN36
VN39	_	(VN43-VN36)*(12R*3)/(12R*7)+VN36
VN38	_	(VN43-VN36)*(12R*2)/(12R*7)+VN36
VN37	_	(VN43-VN36)*12R/(12R*7)+VN36
VN36	VN36[3:0]	(VN43-VN20)*(39R-X*R-7R)/39R+VN20
VN35	_	(VN36-VN27)*(8R*8)/(8R*9)+VN27
VN34		(VN36-VN27)*(8R*7)/(8R*9)+VN27
VN33		(VN36-VN27)*(8R*6)/(8R*9)+VN27
VN32 VN31		(VN36-VN27)*(8R*5)/(8R*9)+VN27
VN30		(VN36-VN27)*(8R*4)/(8R*9)+VN27 (VN36-VN27)*(8R*3)/(8R*9)+VN27
VN29	_	(VN36-VN27)*(8R*2)/(8R*9)+VN27
VN28	_	(VN36-VN27)*8R/(8R*9)+VN27
VN27	VN27[3:0]	(VN43-VN20)*(39R-X*R-23R)/39R+VN20
VN26	_	(VN27-VN20)*(12R*6)/(12R*7)+VN20
VN25		(VN27-VN20)*(12R*5)/(12R*7)+VN20
VN24	_	(VN27-VN20)*(12R*4)/(12R*7)+VN20
VN23	_	(VN27-VN20)*(12R*3)/(12R*7)+VN20
VN22 VN21		(VN27-VN20)*(12R*2)/(12R*7)+VN20
	_	(VN27-VN20)*12R/(12R*7)+VN20 <64 (VREG1-VGS)*(130R-X*R)/130R
VN20	VN20[6:0]	>=64 (VREG1-VGS)*(130R-X*R-1R)/130R
VN19	_	(VN20-VN13)*(14R*2+12R*3+10R)/(14R*2+12R*3+10R*2)+VN13
VN18	_	(VN20-VN13)*(14R*2+12R*3)/(14R*2+12R*3+10R*2)+VN13
VN17		(VN20-VN13)*(14R*2+12R*2)/(14R*2+12R*3+10R*2)+VN13
VN16		(VN20-VN13)*(14R*2+12R)/(14R*2+12R*3+10R*2)+VN13
VN15 VN14		(VN20-VN13)*(14R*2)/(14R*2+12R*3+10R*2)+VN13
VN13	VN13[3:0]	(VN20-VN13)*14R/(14R*2+12R*3+10R*2)+VN13 (VN20-VN2)*(47R-X*R-7R)/47R+VN2
VN12	— —	(VN13-VN6)*(12R*2+10R*3+8R)/(12R*2+10R*3+8R*2)+VN6
VN11	_	(VN13-VN6)*(12R*2+10R*3)/(12R*2+10R*3+8R*2)+VN6
VN10	_	(VN13-VN6)*(12R*2+10R*2)/(12R*2+10R*3+8R*2)+VN6
VN9	_	(VN13-VN6)*(12R*2+10R)/(12R*2+10R*3+8R*2)+VN6
VN8		(VN13-VN6)*(12R*2)/(12R*2+10R*3+8R*2)+VN6
VN7	<u> </u>	(VN13-VN6)*12R/(12R*2+10R*3+8R*2)+VN6
VN6 VN5	VN6[4:0]	(VN20-VN2)*(47R-X*R-16R)/47R+VN2
VN4	— VN4[3:0]	(VN6-VN4)*35R/(35R*2)+VN4 (VN20-VN2)*(47R-X*R-26R)/47R+VN2
VN3	VIN→[S.U] —	(VN4-VN2)*35R/(35R*2)+VN2
VN2	VN2[5:0]	(VREG1-VGS)*(65R-X*R)/130R
VN1	VN1[5:0]	(VREG1-VGS)*(65R-X*R)/130R
VN0	VN0[3:0]	(VREG1-VGS)*(23R-X*R)/130R





15. **Reset**

15.1. Registers

The registers that are initialized are listed as below:

	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Repair data	No Change
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display	Off	Off	Off
ldle	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	00EF h	00EF h	If MADCTL's B5=0:00EF h If MADCTL's B5=1:013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	013F h	013F h	If MADCTL's B5 = 0:013F h If MADCTL's B5=1:00EF h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	013F h	013F h	013F h
Memory Data Access Control	00 h	00 h	No Change
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	No Change
RDDCOLMOD	06 h	06 h	06 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.

Note 2: After Powered-On Reset finishes within 10µs after both VCI & VDDI are applied.

Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.





15.2. Output Pins, I/O Pins

	After Power ON	After Hardware Reset	After Software Reset	
TE line	Low	Low	Low	
D[17:0] (output driver)	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)	

Note 1: There will be no output from D [17:0] during Power ON/OFF sequence, hardware reset and software reset.

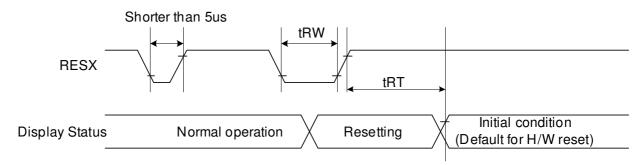
15.3. Input Pins

	During Power ON Process	r ÖN Power Hardware Soft		After Software Reset	During Power OFF Process
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D[17:0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid





15.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tDT Poset sensel			5 (note 1,5)	mS
	tRT	Reset cancel		120 (note 1,6,7)	mS

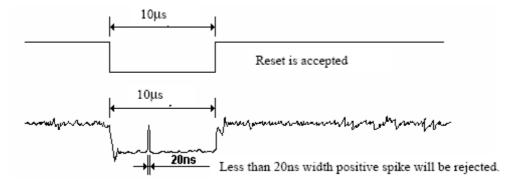
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action		
Shorter than 5us	Reset Rejected		
Longer than 10us	Reset		
Between 5us and 10us	Reset starts		

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



- Note 5: When Reset applied during Sleep In Mode.
- Note 6: When Reset applied during Sleep Out Mode.
- Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

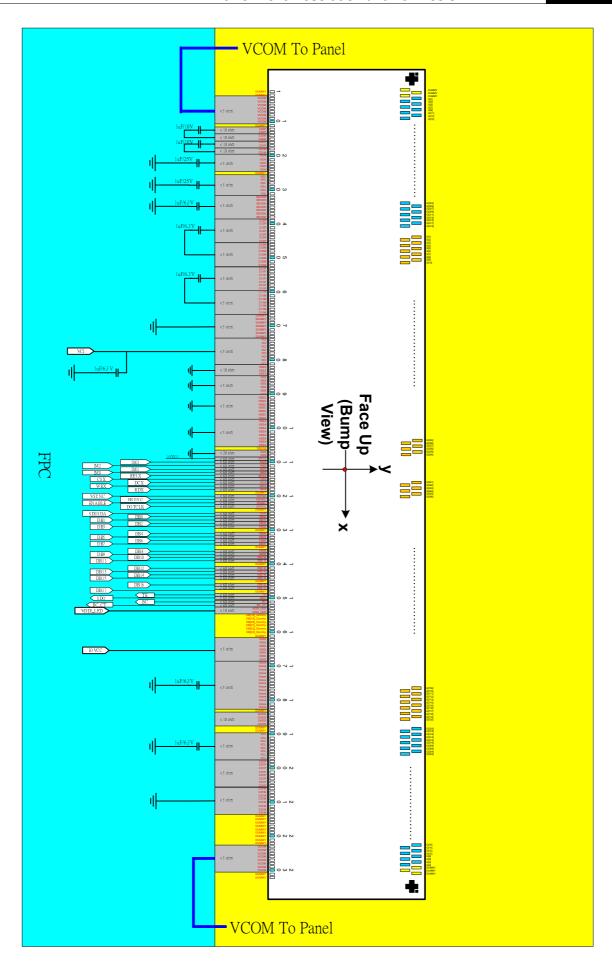






16. Configuration of Power Supply Circuit









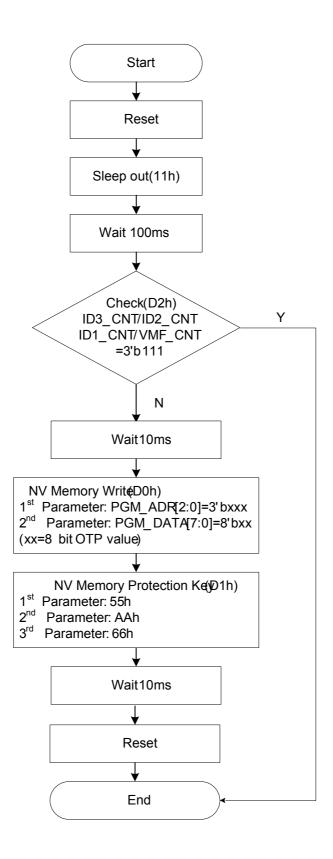
The Following tables shows specifications of external elements connected to the ILI9341's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 µF (B characteristics)	6.3V	DDVDH ,VCL,C11P/M,C12P/M,Vcore,VCI
	10V	C21P/M,C22P/M
	25V	VGL, VGH





17. NV Memory Programming Flow









18. Electrical Characteristics

18.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9341 is used out of the absolute maximum ratings, ILI9341 may be permanently damaged. To use ILI9341 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9341 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.6
Supply voltage (Logic)	VDDI	V	-0.3 ~ +4.6
Supply voltage (Digital)	VCORE	V	-0.3 ~ + <mark>2.0</mark>
Driver supply voltage	VGH-VGL	V	-0.3 ~ +32.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	Topr	$^{\circ}\!\mathbb{C}$	-40 ~ +85
Storage temperature	Tstg	$^{\circ}$	-55 ~ +110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.





18.2 DC Characteristics

18.2.1 General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Тур.	Max.	Note
Power and Operation V	oltage						
Analog Operating Voltage	VCI	٧	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	٧	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	٧	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	ī	-10.0	-	-5.0	Note3
Driver Supply Voltage	-	V	VGH-VGL	15		28	Note3
Current consumption during standby mode	I _{ST}	μΑ	VCI=2.8V , Ta=25 ℃	-	-	100	-
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	٧	-	VSS	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	٧	IOL=1.0mA	VSS	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	1	-	-	1	Note1,2,3
Logic Low Level input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or VSS	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5	-	0.0	Note3
VCOM Amplitude Voltage	VCOMA	V	VCOMH-VCOML	4.0	-	5.5	Note3
Source Driver							
Source Output Range	Vsout	V	-	0.1	-	DDVDH-0.1	Note4
Gamma Reference Voltage	GVDD	V	-	3.0	-	5.0	Note3
Output Deviation Voltage (Source	Vdev	mV	Sout>=4.2V Sout<=0.8V	-	-	20	Note4
Output channel)			4.2V>Sout>0.8V	-	-	15	-
Output Offset Voltage	VOFSET	mV	-	-	-	35	Note7
Booster Operation	_						
1 st Booster (VCIx2) Voltage	DDVDH	V	-	4.95 (Note 5)	-	5.8 (Note 6)	Note3
1 st Booster (VCIx2 Drop Voltage	VCIx2 drop	%	loading=1mA	-	-	5	Note3
Liner Range	Vliner	V	-	0.2	-	DDVDH-0.2	





Note 1: VDDI=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage) \mathcal{C} .

Note2: Please supply digital VDDI voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1, IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

Note5: VCI=2.6V Note6: VCI=3.3V

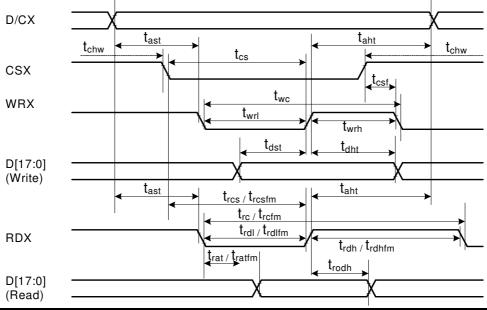
Note7: The Max. Value is between with Note 4 measure point and Gamma setting value





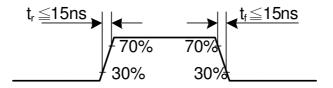
18.3 AC Characteristics

18.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)



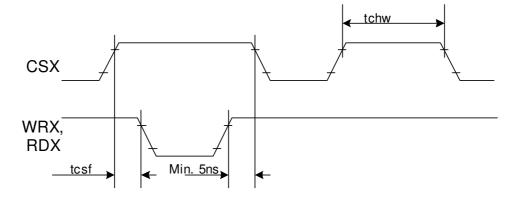
Signal	Symbol	Parameter	min	max	Unit	Description
DCX tast		Address setup time	0	-	ns	
DCX	taht	Address hold time (Write/Read)	0	-	ns	
	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
CSX	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
	twc	Write cycle	66	-	ns	
WRX	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
	trcfm	Read Cycle (FM)	450	-	ns	
RDX (FM)	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
	trc	Read cycle (ID)	160	-	ns	
RDX (ID)	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[47.0]	tdst	Write data setup time	10	-	ns	
D[17:0],	tdht	Write data hold time	10	-	ns	For movimum CL 20nF
D[15:0], D[8:0],	trat	Read access time	-	40	ns	For maximum CL=30pF For minimum CL=8pF
D[8:0], D[7:0]	tratfm	Read access time	-	340	ns	I of millimum GL=opr
D[7.0]	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V



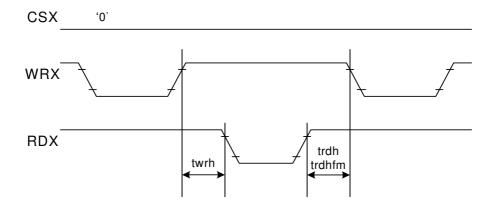


CSX timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

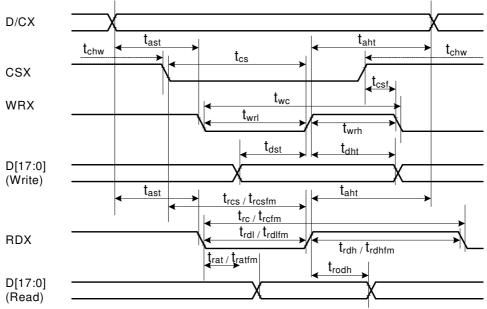
Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

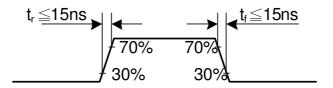






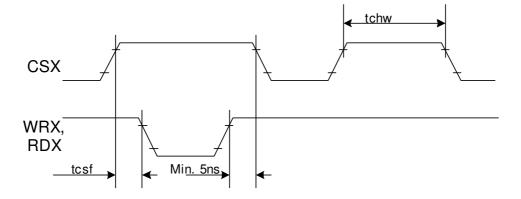
Signal	Symbo	Parameter	min	max	Unit	Description
DCV	tast	Address setup time	0	-	ns	For maximum CL=30pF For minimum CL=8pF
DCX	taht	Address hold time (Write/Read)	Setup time			
	tchw	CSX "H" pulse width	0	-	ns	For maximum CL=30pF
	tast Address setup time 0 - ns taht Address hold time (Write/Read) 0 - ns tchw CSX "H" pulse width 0 - ns trcs Chip Select setup time (Read ID) 45 - ns trcsfm Chip Select setup time (Read FM) 355 - ns tcsf Chip Select Wait time (Write/Read) 10 - ns twc Write cycle 66 - ns twrl Write Control pulse H duration 15 - ns trcfm Read Cycle (FM) 450 - ns trcfm Read Cycle (FM) 450 - ns trdlfm Read Control H duration (FM) 90 - ns trdlfm Read Control pulse H duration 90 - ns trdl Read Control pulse H duration 90 - ns trdl Read Control pulse H duration 90 - ns trdl Read Control pulse H duration 90 - ns trdl Read Control pulse L duration 90 - ns trdl Read Control pulse Read Control 90 - ns trdl Read Control pulse Read Control 90 - ns Tormin 90 - ns Tormin 90 - 90 - 90 - 90 - 90 - 90 - 90 - 90					
CSX	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
WRX twc Write cycle twrh Write Control pulse H durat	Chip Select Wait time (Write/Read)	10	-	ns		
	twc	Write cycle	66	-	ns	
WRX	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
	trcfm	Address setup time Address hold time (Write/Read) CSX "H" pulse width Chip Select setup time (Write) Chip Select setup time (Read ID) Chip Select setup time (Read ID) Chip Select setup time (Read FM) Chip Select setup time (Read FM) Chip Select wait time (Write/Read) Chip Select Wait time (Write/Read) Write cycle 66 ns Write Control pulse H duration Fread Cycle (FM) Read Cycle (FM) Read Control L duration (FM) Read Control L duration (FM) Read Cycle (ID) Read Control pulse H duration Read Control pulse H duration Read Control pulse H duration Read Control pulse H duration Read Control pulse H duration Read Control pulse H duration Read Control pulse H duration Read Control pulse L duration Read Control pulse L duration Read Control pulse L duration Read Control pulse L duration Read Control pulse L duration Read Control pulse L duration Read Control pulse L duration Read Control pulse L duration Read Control pulse L duration Read Control pulse L duration Read access time - 40 ns For maximum For minimum Control pulse Control				
RDX (FM)	Tast	ns				
	trdlfm	Address hold time (Write/Read) CSX "H" pulse width Chip Select setup time (Write) Chip Select setup time (Read ID) Chip Select setup time (Read ID) Chip Select setup time (Read FM) Chip Select Wait time (Write/Read) Write cycle Chip Select Wait time (Write/Read) Write Control pulse H duration Write Control pulse L duration Read Cycle (FM) Read Cycle (FM) Read Control H duration (FM) Read Control L duration (FM) Read Cycle (ID) Read Control pulse H duration Read Control pulse H duration Write data setup time Write data setup time To ns Write data hold time Read access time				
	trc	Read cycle (ID)		-	ns ns ns ns ns ns ns ns ns ns ns ns ns n	
RDX (ID)	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[47.0]	tdst	Write data setup time	10	-	ns	
D[17:0],	tdht	Write data hold time	10	-	ns	For maximum CL 2055
	trat	Read access time	-	40	ns	·
	tratfm	Read access time	-	340	ns	For minimum CL=opF
D[17:9]	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.



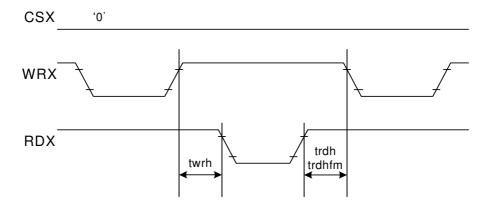


CSX timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

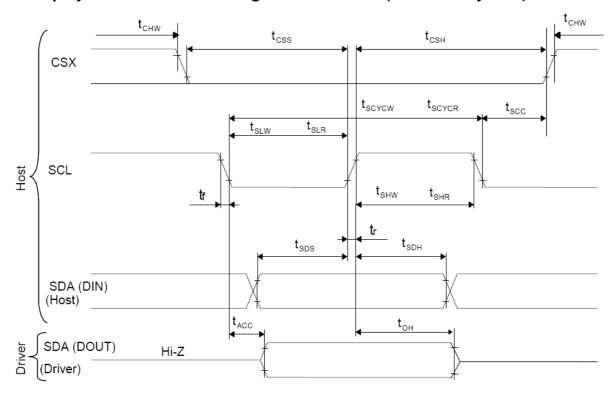


Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.



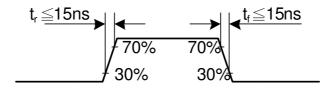


18.3.3 Display Serial Interface Timing Characteristics (3-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
SCL	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
SOL	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI	tsds	Data setup time (Write)	30	-	ns	
(Input)	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO	tacc	Access time (Read)	10	-	ns	
(Output)	toh	Output disable time (Read)	10	50	ns	
	tscc	SCL-CSX	20	-	ns	
CSX	tchw	CSX "H" Pulse Width	40	-	ns	
USA	tcss	CSX-SCL Time	60	-	ns	
	tcsh	COA-OCL TITLE	65	-	ns	

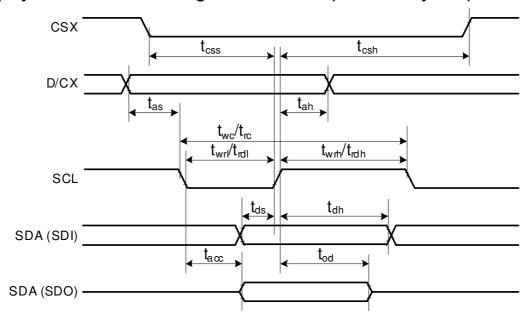
Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V





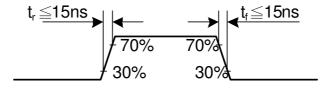


18.3.4 Display Serial Interface Timing Characteristics (4-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description	
CCV	tcss	Chip select time (Write)	40	-	ns		
CSX							
	CSX tcss Chip select time (Write) tcsh Chip select hold time (Read) twc Serial clock cycle (Write) twrh SCL "H" pulse width (Write) trc Serial clock cycle (Read) trdh SCL "H" pulse width (Read) trdh SCL "H" pulse width (Read) trdl SCL "L" pulse width (Read) trdl SCL "L" pulse width (Read)	Serial clock cycle (Write)	100	-	ns		
	twrh	SCL "H" pulse width (Write)	40	-	ns		
801	twrl	SCL "L" pulse width (Write)	40	-	ns		
SCL	trc	Serial clock cycle (Read) 150 - ns					
	trdh	SCL "H" pulse width (Read)	60	-	ns		
	trdl	SCL "L" pulse width (Read)	60	-	ns		
D/CV	tas	D/CX setup time	10	-			
D/GX	tah	D/CX hold time (Write / Read)	10	-			
SDA / SDI	tds	Data setup time (Write)	30	-	ns		
(Input)	tdh	Data hold time (Write)	30	-	ns		
SDA / SDO	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF	
(Output)	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF	

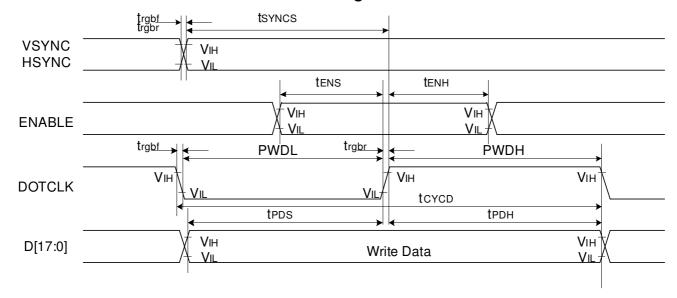
Note: $Ta = 25 \, ^{\circ}$ C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V





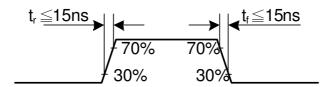


18.3.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC /	tsyncs	VSYNC/HSYNC setup time	15	-	ns	
HSYNC	tsynch	VSYNC/HSYNC hold time	SYNC/HSYNC setup time			
DE	t _{ENS}	DE setup time		-	ns	
DE	t _{ENH}	tens DE setup time 15 tenh DE hold time 15 tpos Data setup time 15 tpdh Data hold time 15 PWDH DOTCLK high-level period 15 PWDL DOTCLK low-level period 15 tcycd DOTCLK cycle time 100 dor, trgbf DOTCLK,HSYNC,VSYNC rise/fall time - dsyncs VSYNC/HSYNC setup time 15 dsynch VSYNC/HSYNC hold time 15 tens DE setup time 15 tens DE hold time 15	-	ns		
D[17:0]	t _{POS}	Data setup time	15	-	ns	18/16-bit bus RGB
D[17.0]	t _{PDH}	Data hold time	15	-	ns	interface mode
	PWDH	DOTCLK high-level period	15	-	ns	
DOTCLK	PWDL	DOTCLK low-level period	15	-	ns	
DOTOLK	t _{CYCD}	DOTCLK cycle time	cycle time 100 - ns		ns	
	t _{rgbr} , t _{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC /	tsyncs	VSYNC/HSYNC setup time	15	-	ns	
HSYNC	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	t _{ENS}	DE setup time	15	-	ns	
DE	t _{ENH}	DE hold time	15	-	ns	
D[17:0]	t _{POS}	Data setup time	15	-	ns	6-bit bus RGB
D[17:0]	t _{PDH}	Data hold time	15	-	ns	interface mode
	PWDH	DOTCLK high-level pulse period	15	-	ns	
DOTCLK	PWDL	DOTCLK low-level pulse period	15	-	ns	
DOTCLK	t _{CYCD}	DOTCLK cycle time	100	-	ns	
	t _{rgbr} , t _{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V







19 Revision History

Version No.	Date	Page	Description
V1.00	2010/10/12	All	New Created.
V1.01	2010/10/12	179	Update charge pump ratio
V1.02	2010/12/17	35,195~200	Add description of extend register command
V1.03	2010/12/20	196	Modify description of pumping
V1.04	2010/12/24	All	Update extend register and OTP flow
V1.05	2011/01/05	All	Update extend register
V1.06	2011/01/20	16,230	No.75 pad location, DC Characteristics
V1.07	2011/02/24	199,226,227	Modify register, external element.
V1.08	2011/03/04	179,196,227,228	Analog supply voltage naming, external element, DDVDH Max, Modify C1h,CFh
			default setting
V1.09	2011/03/15	9,159,197,199,226	Update clock timing, IC Configuration, E8h, EDh
V1.10	2011/04/15	226	Update for general FPC application



Application Notes

Version: Preliminary V0.7

Date: Mar. 22th 2011

ILI TECHNOLOGY CORP.

8F, No.38, Taiyuan St., Jhubei City, Hsinchu County 302, Taiwan, R.O.C Tel.886-3-5600099; Fax.886-3-5600055 http://www.ilitek.com



1.	LGD 2.6" PANEL	3
1.1	FPC Application Circuit	3
1.2	LG 2.8" INITIAL CODE	4
2.1	BOE 2.0_2.4_3.14 FPC APPLICATION CIRCUIT	8
2.2	BOE 2.0" Initial Code	9
2.3	BOE 2.4" Initial Code	12
2.3	BOE 2.4" INITIAL CODE	15
3.	TM 2.2" 2.4" PANEL	20
3.1	FPC Application Circuit	20
3.2	TM2.4 INCH INITIAL CODE	21
3.3	TM2.8 INCH INITIAL CODE	25
4.1	HSD2.8 INCH INITIAL CODE	29

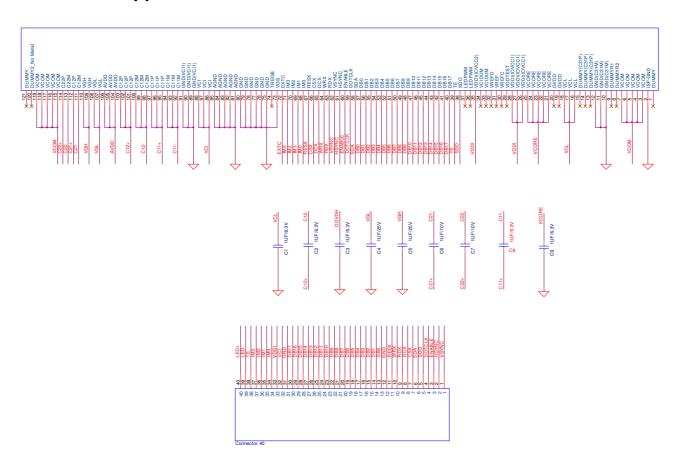
REVISION HISTORY





1. LGD 2.6/2.8 Panel

1.1 FPC Application Circuit







1.2 LG 2.8" Initial Code

```
void ILI9341 LG2.8 Initial(void)
{
// VCI=2.8V
//******* Reset LCD Driver *********//
LCD_nRESET = 1;
delayms(1);
                                   // Delay 1ms
LCD nRESET = 0;
delayms(10);
                                   // Delay 10ms // This delay time is necessary
LCD nRESET = 1;
delayms(120);
                                   // Delay 120 ms
//******* Start Initial Sequence ********//
LCD ILI9341 CMD(0xCB);
                         //功耗控制A
LCD_ILI9341_ Parameter (0x39);
LCD ILI9341 Parameter (0x2C);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x34); //内核电压控制
LCD_ILI9341_ Parameter (0x02); //DDVDH控制
                          //功耗控制B
LCD ILI9341 CMD(0xCF);
LCD ILI9341 Parameter (0x00);
LCD JLI9341_ Parameter (0XC1); //Power控制
LCD_ILI9341_ Parameter (0X30);
LCD_ILI9341_CMD(0xE8); //驱动时序控制A
LCD_ILI9341_ Parameter (0x85); //栅极驱动器的非重叠时序控制
LCD ILI9341 Parameter (0x00); //EQ时序控制
LCD_ILI9341_ Parameter (0x78); //预充电时间控制
LCD_ILI9341_CMD(0xEA); //驱动时序控制B
LCD_ILI9341_ Parameter (0x00); //栅极驱动器时序控制
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0xED); //电源序列控制
LCD_ILI9341_ Parameter (0x64); //软启动控制
LCD_ILI9341_ Parameter (0x03); //电源序列控制
LCD_ILI9341_ Parameter (0X12); //电源序列控制
LCD_ILI9341_ Parameter (0X81) //DDVDH增强模式
```





LCD_ILI9341_CMD(0xF7); //泵比控制 LCD_ILI9341_ Parameter (0x20); //比率控制

LCD_ILI9341_CMD(0xC0); //Power control //功耗控制1 LCD_ILI9341_ Parameter (0x1b); //VRH[5:0] //设置GVDD电平

LCD_ILI9341_CMD(0xC1); //Power control //功耗控制2

LCD_ILI9341_ Parameter (0x10); //SAP[2:0];BT[3:0] //设置用于升压电路的因子

LCD_ILI9341_CMD(0xC5); //VCM control //VCOM控制1

LCD_ILI9341_ Parameter (0x2d); //设置VCOMH电压 LCD_ILI9341 Parameter (0x33); //设置VCOML电压

//LCD ILI9341 CMD(0xC7); //VCM control2 //VCOM控制2

//LCD_ILI9341_ Parameter (0xCf); //设置VCOM偏移电压

LCD_ILI9341_CMD(0x36); // Memory Access Control //存储器访问控制

LCD_ILI9341_ Parameter (0x48); //该指令定义帧存储器的读写扫描方向

LCD_ILI9341_CMD(0xB1); //(正常模式/全色模式下)帧速率控制

LCD_ILI9341_ Parameter (0x00); //内部时钟分频设置,00时表示不分频

LCD_ILI9341_ Parameter (0x1d); //RTNA设置,用于设置1H(行)的时间

LCD_ILI9341_CMD(0xB6); // Display Function Control //显示功能设置

LCD_ILI9341_ Parameter (0x0A); //设置在没显示区域的扫描格式, 0A表示间隔扫描

LCD_ILI9341_ Parameter (0x02); //设置源极、栅极驱动器的移动方向和扫描周期

LCD_ILI9341_CMD(0xF2); // 3Gamma Function Disable //使能3G

LCD ILI9341 Parameter (0x00); //01使能3G,00不使能

LCD_ILI9341_CMD(0x26); //Gamma curve selected //伽马设置

LCD_ILI9341_ Parameter (0x01); //选择伽马曲线1

LCD ILI9341 CMD(0xE0); //Set Gamma //正极伽马校准

LCD_ILI9341_ Parameter (0x0F);

LCD_ILI9341_ Parameter (0x3a);

LCD_ILI9341_ Parameter (0x36);

LCD_ILI9341_ Parameter (0x0b);





```
LCD ILI9341 Parameter (0x0d);
LCD_ILI9341_ Parameter (0x06);
LCD_ILI9341_ Parameter (0x4c);
LCD_ILI9341_ Parameter (0x91);
LCD_ILI9341_ Parameter (0x31);
LCD_ILI9341_ Parameter (0x08);
LCD_ILI9341_ Parameter (0x10);
LCD_ILI9341_ Parameter (0x04);
LCD_ILI9341_ Parameter (0x11);
LCD_ILI9341_ Parameter (0x0c);
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 CMD(0XE1);
                                      //Set Gamma //负极伽马校准
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x06);
LCD ILI9341 Parameter (0x0a);
LCD_ILI9341_ Parameter (0x05);
LCD_ILI9341_ Parameter (0x12);
LCD_ILI9341_ Parameter (0x09);
LCD_ILI9341_ Parameter (0x2c);
LCD_ILI9341_ Parameter (0x92);
LCD_ILI9341_ Parameter (0x3f);
LCD_ILI9341_ Parameter (0x08);
LCD_ILI9341_ Parameter (0x0e);
LCD_ILI9341_ Parameter (0x0b);
LCD_ILI9341_ Parameter (0x2e);
LCD_ILI9341_ Parameter (0x33);
LCD_ILI9341_ Parameter (0x0F);
LCD ILI9341 CMD(0x11);
                                      //Exit Sleep //退出睡眠模式
Delayms(120);
LCD_ILI9341_CMD(0x29);
                                      //Display on //开显示
}
```

V0.6





```
void LCD_Enter Sleep_ILI9341(void)
{
LCD_ILI9341_CMD(0x28);  // Display off
Delayms(20);
LCD_ILI9341_CMD(0x10);  // Enter Sleep mode
}

void LCD_Exit Sleep_ILI9341(void)
{
LCD_ILI9341_CMD(0x11);  // Sleep out
Delayms(120);
LCD_ILI9341_CMD(0x29);  // Display on
}
```

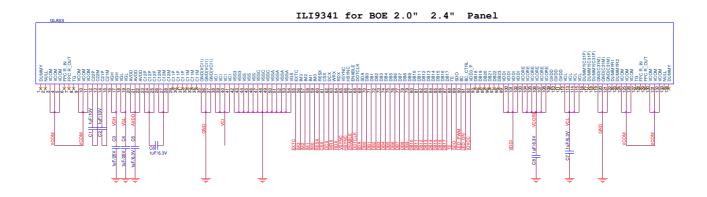
V0.6





2. BOE 2.0" 2.4"3.14 Panel

2.1 FPC Application Circuit









2.2 BOE 2.0" Initial Code

```
void ILI9341_BOE2.0_Initial(void)
{
// VCI=2.8V
//************ Reset LCD Driver **********//
LCD_nRESET = 1;
delayms(1);
                                      // Delay 1ms
LCD_nRESET = 0;
                                      // Delay 10ms // This delay time is necessary
delayms(10);
LCD_nRESET = 1;
delayms(120);
                                      // Delay 120 ms
//******* Start Initial Sequence *******//
LCD_ILI9341_CMD(0xCF);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x81);
LCD_ILI9341_ Parameter (0X30);
LCD_ILI9341_CMD(0xED);
LCD_ILI9341_ Parameter (0x64);
LCD_ILI9341_ Parameter (0x03);
LCD_ILI9341_ Parameter (0X12);
LCD_ILI9341_ Parameter (0X81);
LCD_ILI9341_CMD(0xE8);
LCD_ILI9341_ Parameter (0x85);
LCD_ILI9341_ Parameter (0x10);
LCD_ILI9341_ Parameter (0x78);
LCD_ILI9341_CMD(0xCB);
LCD_ILI9341_ Parameter (0x39);
LCD_ILI9341_ Parameter (0x2C);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x34);
LCD_ILI9341_ Parameter (0x02);
LCD_ILI9341_CMD(0xF7);
LCD_ILI9341_ Parameter (0x20);
```

V0.6





```
LCD_ILI9341_CMD(0xEA);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0xB1);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x1B);
LCD_ILI9341_CMD(0xB6);
                                      // Display Function Control
LCD_ILI9341_ Parameter (0x0A);
LCD_ILI9341_ Parameter (0xA2);
LCD_ILI9341_CMD(0xC0);
                                      //Power control
LCD_ILI9341_ Parameter (0x21);
                                      //VRH[5:0]
LCD_ILI9341_CMD(0xC1);
                                      //Power control
LCD_ILI9341_ Parameter (0x11);
                                      //SAP[2:0];BT[3:0]
                                      //VCM control
LCD_ILI9341_CMD(0xC5);
LCD_ILI9341_ Parameter (0x3F);
LCD_ILI9341_ Parameter (0x3C);
LCD_ILI9341_CMD(0xC7);
                                      //VCM control2
LCD_ILI9341_ Parameter (0Xab);
LCD_ILI9341_CMD(0x36);
                                      // Memory Access Control
LCD_ILI9341_ Parameter (0x48);
LCD ILI9341 CMD(0xF2);
                                      // 3Gamma Function Disable
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 CMD(0x26);
                                      //Gamma curve selected
LCD_ILI9341_ Parameter (0x01);
LCD_ILI9341_CMD(0xE0);
                                      //Set Gamma
LCD_ILI9341_ Parameter (0x0F);
LCD_ILI9341_ Parameter (0x27);
LCD_ILI9341_ Parameter (0x25);
```





```
LCD ILI9341 Parameter (0x0a);
LCD_ILI9341_ Parameter (0x0E);
LCD_ILI9341_ Parameter (0x09);
LCD_ILI9341_ Parameter (0x56);
LCD_ILI9341_ Parameter (0X98);
LCD_ILI9341_ Parameter (0x49);
LCD_ILI9341_ Parameter (0x07);
LCD_ILI9341_ Parameter (0x10);
LCD_ILI9341_ Parameter (0x03);
LCD_ILI9341_ Parameter (0x31);
LCD_ILI9341_ Parameter (0x30);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0XE1);
                                       //Set Gamma
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 Parameter (0x18);
LCD_ILI9341_ Parameter (0x1a);
LCD_ILI9341_ Parameter (0x05);
LCD_ILI9341_ Parameter (0x11);
LCD_ILI9341_ Parameter (0x06);
LCD_ILI9341_ Parameter (0x29);
LCD_ILI9341_ Parameter (0x67);
LCD_ILI9341_ Parameter (0x36);
LCD_ILI9341_ Parameter (0x08);
LCD_ILI9341_ Parameter (0x0f);
LCD_ILI9341_ Parameter (0x0c);
LCD_ILI9341_ Parameter (0x0e);
LCD_ILI9341_ Parameter (0x0f);
LCD_ILI9341_ Parameter (0x0f);
LCD_ILI9341_CMD(0x11);
                                       //Exit Sleep
Delayms(120);
LCD_ILI9341_CMD(0x29);
                                       //Display on
}
```







2.3 BOE 2.4" Initial Code

```
void ILI9341_BOE2.4_Initial(void)
{
// VCI=2.8V
//************ Reset LCD Driver **********//
LCD_nRESET = 1;
delayms(1);
                                      // Delay 1ms
LCD_nRESET = 0;
                                      // Delay 10ms // This delay time is necessary
delayms(10);
LCD_nRESET = 1;
delayms(120);
                                      // Delay 120 ms
//******* Start Initial Sequence *******//
LCD_ILI9341_CMD(0xCF);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x81);
LCD_ILI9341_ Parameter (0X30);
LCD_ILI9341_CMD(0xED);
LCD_ILI9341_ Parameter (0x64);
LCD_ILI9341_ Parameter (0x03);
LCD_ILI9341_ Parameter (0X12);
LCD_ILI9341_ Parameter (0X81);
LCD_ILI9341_CMD(0xE8);
LCD_ILI9341_ Parameter (0x85);
LCD_ILI9341_ Parameter (0x10);
LCD_ILI9341_ Parameter (0x78);
LCD_ILI9341_CMD(0xCB);
LCD_ILI9341_ Parameter (0x39);
LCD_ILI9341_ Parameter (0x2C);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x34);
LCD_ILI9341_ Parameter (0x02);
LCD_ILI9341_CMD(0xF7);
LCD_ILI9341_ Parameter (0x20);
```





```
LCD_ILI9341_CMD(0xEA);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0xB1);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x1B);
LCD_ILI9341_CMD(0xB6);
                                      // Display Function Control
LCD_ILI9341_ Parameter (0x0A);
LCD_ILI9341_ Parameter (0xA2);
LCD_ILI9341_CMD(0xC0);
                                      //Power control
LCD_ILI9341_ Parameter (0x21);
                                      //VRH[5:0]
LCD_ILI9341_CMD(0xC1);
                                      //Power control
LCD_ILI9341_ Parameter (0x11);
                                      //SAP[2:0];BT[3:0]
                                      //VCM control
LCD_ILI9341_CMD(0xC5);
LCD_ILI9341_ Parameter (0x3F);
LCD_ILI9341_ Parameter (0x3C);
LCD_ILI9341_CMD(0xC7);
                                      //VCM control2
LCD_ILI9341_ Parameter (0Xb5);
LCD_ILI9341_CMD(0x36);
                                      // Memory Access Control
LCD_ILI9341_ Parameter (0x48);
LCD ILI9341 CMD(0xF2);
                                      // 3Gamma Function Disable
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 CMD(0x26);
                                      //Gamma curve selected
LCD_ILI9341_ Parameter (0x01);
LCD_ILI9341_CMD(0xE0);
                                      //Set Gamma
LCD_ILI9341_ Parameter (0x0F);
LCD_ILI9341_ Parameter (0x26);
LCD_ILI9341_ Parameter (0x24);
```





```
LCD ILI9341 Parameter (0x0B);
LCD_ILI9341_ Parameter (0x0E);
LCD_ILI9341_ Parameter (0x09);
LCD ILI9341 Parameter (0x54);
LCD_ILI9341_ Parameter (0XA8);
LCD_ILI9341_ Parameter (0x46);
LCD_ILI9341_ Parameter (0x0C);
LCD_ILI9341_ Parameter (0x17);
LCD_ILI9341_ Parameter (0x09);
LCD_ILI9341_ Parameter (0x0F);
LCD_ILI9341_ Parameter (0x07);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0XE1);
                                       //Set Gamma
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 Parameter (0x19);
LCD_ILI9341_ Parameter (0x1B);
LCD_ILI9341_ Parameter (0x04);
LCD_ILI9341_ Parameter (0x10);
LCD_ILI9341_ Parameter (0x07);
LCD_ILI9341_ Parameter (0x2A);
LCD_ILI9341_ Parameter (0x47);
LCD_ILI9341_ Parameter (0x39);
LCD_ILI9341_ Parameter (0x03);
LCD_ILI9341_ Parameter (0x06);
LCD_ILI9341_ Parameter (0x06);
LCD_ILI9341_ Parameter (0x30);
LCD_ILI9341_ Parameter (0x38);
LCD_ILI9341_ Parameter (0x0F);
LCD_ILI9341_CMD(0x11);
                                      //Exit Sleep
Delayms(120);
LCD_ILI9341_CMD(0x29);
                                       //Display on
}
```





```
void LCD_Enter Sleep_ILI9341(void)
{
LCD_ILI9341_CMD(0x28);  // Display off
delayms(20);
LCD_ILI9341_CMD(0x10);  // Enter Sleep mode
}

void LCD_Exit Sleep _ILI9341(void)
{
LCD_ILI9341_CMD(0x11);  // Sleep out
Delayms(120);
LCD_ILI9341_CMD(0x29);  // Display on
}
```

V0.6





2.4 BOE 3.14" Initial Code

```
void ILI9341_BOE3.14_Initial(void)
{
// VCI=2.8V
//************ Reset LCD Driver **********//
LCD_nRESET = 1;
delayms(1);
                                      // Delay 1ms
LCD_nRESET = 0;
                                      // Delay 10ms // This delay time is necessary
delayms(10);
LCD_nRESET = 1;
delayms(120);
                                      // Delay 120 ms
//******* Start Initial Sequence *******//
LCD_ILI9341_CMD(0xCF);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0xc1);
LCD_ILI9341_ Parameter (0X30);
LCD_ILI9341_CMD(0xED);
LCD_ILI9341_ Parameter (0x64);
LCD_ILI9341_ Parameter (0x03);
LCD_ILI9341_ Parameter (0X12);
LCD_ILI9341_ Parameter (0X81);
LCD_ILI9341_CMD(0xE8);
LCD_ILI9341_ Parameter (0x85);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x78);
LCD_ILI9341_CMD(0xCB);
LCD_ILI9341_ Parameter (0x39);
LCD_ILI9341_ Parameter (0x2C);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x34);
LCD_ILI9341_ Parameter (0x02);
LCD_ILI9341_CMD(0xF7);
LCD_ILI9341_ Parameter (0x20);
```





```
LCD_ILI9341_CMD(0xEA);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0xB1);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x16);
LCD_ILI9341_CMD(0xB6);
                                      // Display Function Control
LCD_ILI9341_ Parameter (0x0A);
LCD_ILI9341_ Parameter (0xA2);
LCD_ILI9341_CMD(0xC0);
                                      //Power control
LCD_ILI9341_ Parameter (0x10);
                                      //VRH[5:0]
LCD_ILI9341_CMD(0xC1);
                                      //Power control
LCD_ILI9341_ Parameter (0x10);
                                      //SAP[2:0];BT[3:0]
                                      //VCM control
LCD_ILI9341_CMD(0xC5);
LCD_ILI9341_ Parameter (0x30);
LCD_ILI9341_ Parameter (0x50);
LCD_ILI9341_CMD(0xC7);
                                      //VCM control2
LCD_ILI9341_ Parameter (0XA4);
LCD_ILI9341_CMD(0x36);
                                      // Memory Access Control
LCD_ILI9341_ Parameter (0x08);
LCD ILI9341 CMD(0xF2);
                                      // 3Gamma Function Disable
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 CMD(0x26);
                                      //Gamma curve selected
LCD_ILI9341_ Parameter (0x01);
LCD_ILI9341_CMD(0xE0);
                                      //Set Gamma
LCD_ILI9341_ Parameter (0x0F);
LCD_ILI9341_ Parameter (0x29);
LCD_ILI9341_ Parameter (0x24);
```





```
LCD ILI9341 Parameter (0x0c);
LCD_ILI9341_ Parameter (0x0e);
LCD_ILI9341_ Parameter (0x09);
LCD_ILI9341_ Parameter (0x4e);
LCD_ILI9341_ Parameter (0X78);
LCD_ILI9341_ Parameter (0x3C);
LCD_ILI9341_ Parameter (0x09);
LCD_ILI9341_ Parameter (0x13);
LCD_ILI9341_ Parameter (0x05);
LCD_ILI9341_ Parameter (0x17);
LCD_ILI9341_ Parameter (0x11);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0XE1);
                                       //Set Gamma
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 Parameter (0x16);
LCD_ILI9341_ Parameter (0x1b);
LCD_ILI9341_ Parameter (0x04);
LCD_ILI9341_ Parameter (0x11);
LCD_ILI9341_ Parameter (0x07);
LCD_ILI9341_ Parameter (0x31);
LCD_ILI9341_ Parameter (0x33);
LCD_ILI9341_ Parameter (0x42);
LCD_ILI9341_ Parameter (0x05);
LCD_ILI9341_ Parameter (0x0C);
LCD_ILI9341_ Parameter (0x0A);
LCD_ILI9341_ Parameter (0x28);
LCD_ILI9341_ Parameter (0x2f);
LCD_ILI9341_ Parameter (0x0F);
LCD_ILI9341_CMD(0x11);
                                      //Exit Sleep
Delayms(120);
LCD_ILI9341_CMD(0x29);
                                       //Display on
}
```





```
void LCD_Enter Sleep_ILI9341(void)
{
LCD_ILI9341_CMD(0x28);  // Display off
delayms(20);
LCD_ILI9341_CMD(0x10);  // Enter Sleep mode
}

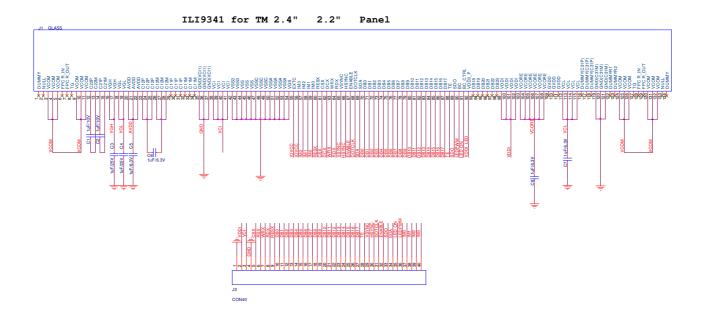
void LCD_Exit Sleep _ILI9341(void)
{
LCD_ILI9341_CMD(0x11);  // Sleep out
Delayms(120);
LCD_ILI9341_CMD(0x29);  // Display on
}
```





3. TM 2.2" 2.4" Panel

3.1 FPC Application Circuit



V0.6







3.2 Tianma 2.4" Initial Code

LCD_ILI9341_ Parameter (0x20);

```
void ILI9341_Tianma2.4_Initial(void)
// VCI=2.8V
//******* Reset LCD Driver *********//
LCD nRESET = 1;
delayms(1);
                                      // Delay 1ms
LCD nRESET = 0;
delayms(10);
                                      // Delay 10ms // This delay time is necessary
LCD_nRESET = 1;
delayms(120);
                                      // Delay 120 ms
//******* Start Initial Sequence ********//
LCD_ILI9341_CMD(0xCF);
LCD ILI9341 Parameter (0x00);
LCD_ILI9341_ Parameter (0x81);
LCD_ILI9341_ Parameter (0X30);
LCD_ILI9341_CMD(0xED);
LCD ILI9341 Parameter (0x64);
LCD_ILI9341_ Parameter (0x03);
LCD_ILI9341_ Parameter (0X12);
LCD ILI9341 Parameter (0X81);
LCD ILI9341 CMD(0xE8);
LCD ILI9341 Parameter (0x85);
LCD_ILI9341_ Parameter (0x10);
LCD_ILI9341_ Parameter (0x7A);
LCD ILI9341 CMD(0xCB);
LCD_ILI9341_ Parameter (0x39);
LCD_ILI9341_ Parameter (0x2C);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x34);
LCD_ILI9341_ Parameter (0x02);
LCD ILI9341 CMD(0xF7);
```





```
LCD_ILI9341_CMD(0xEA);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0xC0);
                                      //Power control
LCD_ILI9341_ Parameter (0x21);
                                      //VRH[5:0]
LCD_ILI9341_CMD(0xC1);
                                      //Power control
LCD_ILI9341_ Parameter (0x11);
                                      //SAP[2:0];BT[3:0]
LCD_ILI9341_CMD(0xC5);
                                      //VCM control
LCD ILI9341 Parameter (0x3F);
LCD_ILI9341_ Parameter (0x3C);
LCD_ILI9341_CMD(0xC7);
                                      //VCM control2
LCD_ILI9341_ Parameter (0Xa7);
LCD_ILI9341_CMD(0x36);
                                      // Memory Access Control
LCD_ILI9341_ Parameter (0x48);
LCD_ILI9341_CMD(0xB1);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x1B);
LCD_ILI9341_CMD(0xB6);
                                      // Display Function Control
LCD_ILI9341_ Parameter (0x0A);
LCD_ILI9341_ Parameter (0xA2);
LCD ILI9341 CMD(0xF2);
                                      // 3Gamma Function Disable
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 CMD(0x26);
                                      //Gamma curve selected
LCD_ILI9341_ Parameter (0x01);
LCD_ILI9341_CMD(0xE0);
                                      //Set Gamma
LCD_ILI9341_ Parameter (0x0F);
LCD_ILI9341_ Parameter (0x23);
LCD_ILI9341_ Parameter (0x1F);
```





```
LCD ILI9341 Parameter (0x0B);
LCD_ILI9341_ Parameter (0x0E);
LCD_ILI9341_ Parameter (0x08);
LCD ILI9341 Parameter (0x4B);
LCD_ILI9341_ Parameter (0XA8);
LCD_ILI9341_ Parameter (0x3B);
LCD_ILI9341_ Parameter (0x0A);
LCD_ILI9341_ Parameter (0x14);
LCD_ILI9341_ Parameter (0x06);
LCD_ILI9341_ Parameter (0x10);
LCD_ILI9341_ Parameter (0x09);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0XE1);
                                      //Set Gamma
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 Parameter (0x1C);
LCD_ILI9341_ Parameter (0x20);
LCD_ILI9341_ Parameter (0x04);
LCD_ILI9341_ Parameter (0x10);
LCD_ILI9341_ Parameter (0x08);
LCD_ILI9341_ Parameter (0x34);
LCD_ILI9341_ Parameter (0x47);
LCD_ILI9341_ Parameter (0x44);
LCD_ILI9341_ Parameter (0x05);
LCD_ILI9341_ Parameter (0x0B);
LCD_ILI9341_ Parameter (0x09);
LCD_ILI9341_ Parameter (0x2F);
LCD_ILI9341_ Parameter (0x36);
LCD_ILI9341_ Parameter (0x0F);
LCD_ILI9341_CMD(0x11);
                                      //Exit Sleep
Delayms(120);
LCD_ILI9341_CMD(0x29);
                                      //Display on
}
```





```
void LCD_Enter Sleep_ILI9341(void)
{
LCD_ILI9341_CMD(0x28);  // Display off
delayms(20);
LCD_ILI9341_CMD(0x10);  // Enter Sleep mode
}

void LCD_Exit Sleep _ILI9341(void)
{
LCD_ILI9341_CMD(0x11);  // Sleep out
Delayms(120);
LCD_ILI9341_CMD(0x29);  // Display on
```







3.2 Tianma 2.8" Initial Code

LCD_ILI9341_ Parameter (0x20);

```
void ILI9341_Tianma2.8_Initial(void)
// VCI=2.8V
//******* Reset LCD Driver *********//
LCD nRESET = 1;
delayms(1);
                                      // Delay 1ms
LCD nRESET = 0;
delayms(10);
                                      // Delay 10ms // This delay time is necessary
LCD_nRESET = 1;
delayms(120);
                                      // Delay 120 ms
//******* Start Initial Sequence ********//
LCD_ILI9341_CMD(0xCF);
LCD ILI9341 Parameter (0x00);
LCD_ILI9341_ Parameter (0x83);
LCD_ILI9341_ Parameter (0X30);
LCD_ILI9341_CMD(0xED);
LCD ILI9341 Parameter (0x64);
LCD_ILI9341_ Parameter (0x03);
LCD_ILI9341_ Parameter (0X12);
LCD ILI9341 Parameter (0X81);
LCD ILI9341 CMD(0xE8);
LCD ILI9341 Parameter (0x85);
LCD_ILI9341_ Parameter (0x01);
LCD_ILI9341_ Parameter (0x79);
LCD ILI9341 CMD(0xCB);
LCD_ILI9341_ Parameter (0x39);
LCD_ILI9341_ Parameter (0x2C);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x34);
LCD_ILI9341_ Parameter (0x02);
LCD ILI9341 CMD(0xF7);
```





```
LCD_ILI9341_CMD(0xEA);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0xC0);
                                      //Power control
LCD_ILI9341_ Parameter (0x1D);
                                      //VRH[5:0]
LCD_ILI9341_CMD(0xC1);
                                      //Power control
LCD_ILI9341_ Parameter (0x11);
                                      //SAP[2:0];BT[3:0]
LCD_ILI9341_CMD(0xC5);
                                      //VCM control
LCD ILI9341 Parameter (0x33);
LCD_ILI9341_ Parameter (0x34);
LCD_ILI9341_CMD(0xC7);
                                      //VCM control2
LCD_ILI9341_ Parameter (0Xbe);
LCD_ILI9341_CMD(0x36);
                                      // Memory Access Control
LCD_ILI9341_ Parameter (0x08);
LCD_ILI9341_CMD(0xB1);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x1B);
LCD_ILI9341_CMD(0xB6);
                                      // Display Function Control
LCD_ILI9341_ Parameter (0x0A);
LCD_ILI9341_ Parameter (0xA2);
LCD ILI9341 CMD(0xF2);
                                      // 3Gamma Function Disable
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 CMD(0x26);
                                      //Gamma curve selected
LCD_ILI9341_ Parameter (0x01);
LCD_ILI9341_CMD(0xE0);
                                      //Set Gamma
LCD_ILI9341_ Parameter (0x0F);
LCD_ILI9341_ Parameter (0x23);
LCD_ILI9341_ Parameter (0x1F);
```





```
LCD ILI9341 Parameter (0x09);
LCD_ILI9341_ Parameter (0x0f);
LCD_ILI9341_ Parameter (0x08);
LCD_ILI9341_ Parameter (0x4B);
LCD_ILI9341_ Parameter (0Xf2);
LCD_ILI9341_ Parameter (0x38);
LCD_ILI9341_ Parameter (0x09);
LCD_ILI9341_ Parameter (0x13);
LCD_ILI9341_ Parameter (0x03);
LCD_ILI9341_ Parameter (0x12);
LCD_ILI9341_ Parameter (0x07);
LCD_ILI9341_ Parameter (0x04);
LCD_ILI9341_CMD(0XE1);
                                       //Set Gamma
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 Parameter (0x1d);
LCD_ILI9341_ Parameter (0x20);
LCD_ILI9341_ Parameter (0x02);
LCD_ILI9341_ Parameter (0x11);
LCD_ILI9341_ Parameter (0x07);
LCD_ILI9341_ Parameter (0x34);
LCD_ILI9341_ Parameter (0x81);
LCD_ILI9341_ Parameter (0x46);
LCD_ILI9341_ Parameter (0x06);
LCD_ILI9341_ Parameter (0x0e);
LCD_ILI9341_ Parameter (0x0c);
LCD_ILI9341_ Parameter (0x32);
LCD_ILI9341_ Parameter (0x38);
LCD_ILI9341_ Parameter (0x0F);
}
```





```
void LCD_Enter Sleep_ILI9341(void)
{
LCD_ILI9341_CMD(0x28);  // Display off
delayms(20);
LCD_ILI9341_CMD(0x10);  // Enter Sleep mode
}

void LCD_Exit Sleep _ILI9341(void)
{
LCD_ILI9341_CMD(0x11);  // Sleep out
Delayms(120);
LCD_ILI9341_CMD(0x29);  // Display on
```





4.1 HSD 2.8" Initial Code

LCD_ILI9341_ Parameter (0x20);

```
void ILI9341_HSD2.8_Initial(void)
// VCI=2.8V
//******* Reset LCD Driver *********//
LCD nRESET = 1;
delayms(1);
                                      // Delay 1ms
LCD nRESET = 0;
delayms(10);
                                      // Delay 10ms // This delay time is necessary
LCD_nRESET = 1;
delayms(120);
                                      // Delay 120 ms
//******* Start Initial Sequence ********//
LCD_ILI9341_CMD(0xCF);
LCD ILI9341 Parameter (0x00);
LCD_ILI9341_ Parameter (0xC1);
LCD_ILI9341_ Parameter (0X30);
LCD_ILI9341_CMD(0xED);
LCD ILI9341 Parameter (0x64);
LCD_ILI9341_ Parameter (0x03);
LCD_ILI9341_ Parameter (0X12);
LCD ILI9341 Parameter (0X81);
LCD ILI9341 CMD(0xE8);
LCD ILI9341 Parameter (0x85);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x7A);
LCD ILI9341 CMD(0xCB);
LCD_ILI9341_ Parameter (0x39);
LCD_ILI9341_ Parameter (0x2C);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x34);
LCD_ILI9341_ Parameter (0x02);
LCD ILI9341 CMD(0xF7);
```





```
LCD_ILI9341_CMD(0xEA);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0xC0);
                                      //Power control
LCD_ILI9341_ Parameter (0x21);
                                      //VRH[5:0]
LCD_ILI9341_CMD(0xC1);
                                      //Power control
LCD_ILI9341_ Parameter (0x11);
                                      //SAP[2:0];BT[3:0]
LCD_ILI9341_CMD(0xC5);
                                      //VCM control
LCD ILI9341 Parameter (0x31);
LCD_ILI9341_ Parameter (0x3C);
LCD_ILI9341_CMD(0xC7);
                                      //VCM control2
LCD_ILI9341_ Parameter (0X9f);
LCD_ILI9341_CMD(0x36);
                                      // Memory Access Control
LCD_ILI9341_ Parameter (0x08);
LCD_ILI9341_CMD(0xB1);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_ Parameter (0x1B);
LCD_ILI9341_CMD(0xB6);
                                      // Display Function Control
LCD_ILI9341_ Parameter (0x0A);
LCD_ILI9341_ Parameter (0xA2);
LCD ILI9341 CMD(0xF2);
                                      // 3Gamma Function Disable
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 CMD(0x26);
                                      //Gamma curve selected
LCD_ILI9341_ Parameter (0x01);
LCD_ILI9341_CMD(0xE0);
                                      //Set Gamma
LCD_ILI9341_ Parameter (0x0F);
LCD_ILI9341_ Parameter (0x20);
LCD_ILI9341_ Parameter (0x1d);
```





```
LCD ILI9341 Parameter (0x0b);
LCD_ILI9341_ Parameter (0x10);
LCD_ILI9341_ Parameter (0x0a);
LCD_ILI9341_ Parameter (0x49);
LCD_ILI9341_ Parameter (0Xa9);
LCD_ILI9341_ Parameter (0x3b);
LCD_ILI9341_ Parameter (0x0a);
LCD_ILI9341_ Parameter (0x15);
LCD_ILI9341_ Parameter (0x06);
LCD_ILI9341_ Parameter (0x0c);
LCD_ILI9341_ Parameter (0x06);
LCD_ILI9341_ Parameter (0x00);
LCD_ILI9341_CMD(0XE1);
                                       //Set Gamma
LCD_ILI9341_ Parameter (0x00);
LCD ILI9341 Parameter (0x1f);
LCD_ILI9341_ Parameter (0x22);
LCD_ILI9341_ Parameter (0x04);
LCD_ILI9341_ Parameter (0x0f);
LCD_ILI9341_ Parameter (0x05);
LCD_ILI9341_ Parameter (0x36);
LCD_ILI9341_ Parameter (0x46);
LCD_ILI9341_ Parameter (0x46);
LCD_ILI9341_ Parameter (0x05);
LCD_ILI9341_ Parameter (0x0b);
LCD_ILI9341_ Parameter (0x09);
LCD_ILI9341_ Parameter (0x33);
LCD_ILI9341_ Parameter (0x39);
LCD_ILI9341_ Parameter (0x0F);
}
```





V0.6

```
void LCD_Enter Sleep_ILI9341(void)
{
LCD_ILI9341_CMD(0x28);  // Display off
delayms(20);
LCD_ILI9341_CMD(0x10);  // Enter Sleep mode
}

void LCD_Exit Sleep _ILI9341(void)
{
LCD_ILI9341_CMD(0x11);  // Sleep out
Delayms(120);
LCD_ILI9341_CMD(0x29);  // Display on
```





Revision History

Revision History

Version No.	Date	Page	Description
V01	2010/09/14	All	New Creation
V02	2010/10/26	All	Modified VCI1 → GND · C31M → GND
			Add BOE2.0" BOE2.4" LG2.6" initial code
V03	2010/12/20	All	Remove command EF
V0.4	2011/02/20	ALL	Add 1uF capacitor in Vcore pad
V0.5	2011/03/08	ALL	Add Tianma initial code and modify LG/BOE initial code
V0.6	2011/03/11	ALL	Modify TM 2.4 and BOE initial code
V0.7	2011/03/22	ALL	Add LG 2.8 TM2.8 BOE 3.14 HSD 2.8 initial code