PIC24F16KM204 FAMILY

PIC24F16KM204 Family
Silicon Errata and Data Sheet Clarification

The PIC24F16KM204 family devices that you have received conform functionally to the current Device Data Sheet (DS30003030**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24F16KM204 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on Page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24F16KM204 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A0	A1			A0	A1
PIC24FV16KM204	551Fh	0000h	0001h	PIC24F16KM204	551Eh	0000h	0001h
PIC24FV08KM204	5517h			PIC24F08KM204	5516h		
PIC24FV16KM104	550Fh			PIC24F16KM104	550Eh		
PIC24FV16KM202	551Bh			PIC24F16KM202	551Ah		
PIC24FV08KM202	5513h			PIC24F08KM202	5512h		
PIC24FV16KM102	550Bh			PIC24F16KM102	550Ah		
PIC24FV08KM102	5503h			PIC24F08KM102	5502h		
PIC24FV08KM101	5501h			PIC24F08KM101	5500h		

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FXXKMXXX/KLXXX Flash Programming Specifications"* (DS30625) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A0	A1
A/D Converter	—	1.	Excessive current consumption under certain conditions.	X	X
A/D Converter	—	2.	Device Reset when sampling upper guardband input.	X	X
MCCP and SCCP	Triggered Operation	3.	TRSET bit does not function in retrigger operations.	X	X
MCCP and SCCP	Compare Mode	4.	Extra compare event in One-Shot mode under certain conditions.	X	X
MCCP and SCCP	Compare Mode	5.	Output compare synchronization does not occur correctly for the first event.	X	X
MCCP and SCCP	Compare Mode	6.	Special Event Trigger postscaler does not work.	X	X
MCCP and SCCP	—	7.	Unexpected 32-bit timer rollover under certain conditions.	X	X
Op Amp	—	8.	Op amp output and digital output drivers may cause bus conflict.	X	X
Reset	BOR	9.	Unexpected BOR events when BOR is disabled in Sleep mode.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: A/D Converter

When low-power operation is enabled (LPEN bit is set), the module may still consume high current (approximately 90 µA) when the device is in Sleep mode and after the conversion is completed.

Work around

After conversions in Sleep mode are complete, wake the device and disable the module.

Affected Silicon Revisions

A0	A1						
X	X						

2. Module: A/D Converter

Sampling and converting the upper V_{DD} guardband rail input (AD1CHS<12:8> = 11100) may cause a device Reset. This can occur without regard to any other operating conditions.

Work around

Do not use the upper guardband input.

Affected Silicon Revisions

A0	A1						
X	X						

3. Module: MCCP and SCCP

In retrigger operation, setting the TRSET bit (CCPxSTATL<6>) may not properly cause a retrigger event. All other available trigger sources will cause a retrigger event as described.

Work around

If the TRSET bit must be used for retrigger operation, set the TRCLR bit (CCPxSTATL<5>) prior to setting the TRSET bit.

Affected Silicon Revisions

A0	A1						
X	X						

4. Module: MCCP and SCCP

In One-Shot Output Compare mode, an additional compare event may occur, causing an extra toggling of the OCx pin and an additional interrupt event. This occurs whenever the value of CCPxRA is 0000h, and after the trigger has been cleared and the CCPxTMR is reset.

Work around

A non-zero value of CCPxRA (e.g., 0001h) prevents the additional compare event.

Affected Silicon Revisions

A0	A1						
X	X						

5. Module: MCCP and SCCP

Output compare synchronization of the OCx pin to the module's selected time base (enabled when OENSYNC (CCPxCON2H<15>) = 1) may prevent output on the pin on the first time base period after enabling the module. After the first period, OCx pin events will appear correctly.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

6. Module: MCCP and SCCP

When the Special Event Trigger output is selected (CCPxCON1H = 1), the interrupt postscaler setting, selected by CCPxCON1H<11:8>, has no effect. A Special Event Trigger will output on each compare match event.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

7. Module: MCCP and SCCP

The MCCP module may rollover at an incorrect time when all of the following conditions are met:

- The module is configured in 32-bit operation (T32 (CCPxCON1L<5>) = 1)
- The CCPxTMRH and CCPxPRH registers are initialized with the same value
- The CCPxTMRL register is initialized with a value higher than CCPxPRL
- The module is configured for a timer match with no external synchronization source (SYNC<4:0> (CCPxCON1H<4:0>) = 00000)

With the module configured this way, the MCCP module will clear the CCPxTMRH/L register pair and generate a timer rollover interrupt when CCPxTMRL rolls over from FFFFh to 0000h, regardless of the value of CCPxTMRH. The expected behavior would be to roll over only after reaching the expected timer rollover value of FFFFFFFFh.

For example, if the module is initialized with the following settings:

- CCPxTMRH = CCPxPRH = 1000h
- CCPxPRL = 0000h
- CCPxTMRL = 0001h

When the module is enabled, it will run until CCPxTMR = 1000FFFFh, then roll over to zero and generate an MCCP timer rollover interrupt.

Work around

None.

Affected Silicon Revisions

A0	A1						
X	X						

8. Module: Op Amp

When op amp modules are enabled, a bus conflict between the module's analog driver and the digital I/O driver may result, causing an unexpected voltage level and high-current consumption.

This is only seen when the TRISx bit associated with the OAxOUT pin is cleared. This results in the digital output driver being enabled and conflicting with the op amp's analog output driver.

Work around

When using an op amp module, ensure that the TRISx bit associated with the OAxOUT pin is set as an input (TRISx = 1) to disable the digital output driver.

Affected Silicon Revisions

A0	A1						
X	X						

9. Module: Reset

Under certain conditions, the device may improperly perform a Brown-out Reset upon wake-up from a Sleep mode. This has been observed under two conditions:

1. When the BOR is disabled in Sleep mode, BOREN<1:0> (FPOR<1:0>) = 10, a BOR may occur when the device wakes from Sleep, regardless of the supply voltage.
2. When the BOR is configured for software control (BOREN<1:0> = 01), the device enters and wakes from Sleep normally while the BOR is disabled in software, SBOREN (RCON<13>) = 0. However, if the BOR was disabled prior to entering Sleep mode and is subsequently enabled after waking from Sleep, a BOR may occur regardless of the supply voltage.

BOR functions normally when it is always enabled or disabled (BOREN<1:0> = 11 or 00).

Work around

Do not use Sleep mode when BOREN<1:0> = 10. If the BOR is to operate under software control, always enable the HLVD module, HLVDEN (HLVDCON<15>) = 1, before enabling the BOR in software (SBOREN = 1). This procedure activates the internal band gap reference and assures its stability for the BOR circuit.

Affected Silicon Revisions

A0	A1						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30003030**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Memory Organization

In Table 4-25: A/D Register Map, and in Register 19-6: AD1CHITH, Register 19-8: AD1CSSH and Register 19-10 AD1CTMENH, respectively, it is incorrectly noted that bits 3 and 4 are not implemented on 20-pin devices. These bits are implemented on 20-pin parts, and instead, this note should apply to bits 1 and 2.

2. Module: Electrical Characteristics

Table 27-17: Operational Amplifier Specifications has had the Input Offset Voltage Max value and Common-Mode Input Voltage Range Max value updated, as shown below in **bold**.

TABLE 27-17: OPERATIONAL AMPLIFIER SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Comments
	VIOFF	Input Offset Voltage	—	±2	**±50**	mV	
	VICM	Common-Mode Input Voltage Range	AVSS	—	**AVDD – 850**	**mV**	

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3. Module: 12-Bit A/D Converter with Threshold Detect

The Note 2 references in Register 19-6: AD1CHITH moved from CHH19 and CHH20 to CHH17 and CHH18. The Table Footnote 2 now reads “The CHH<18:17> bits are not implemented in 20-pin devices”.

The Note 2 references in Register 19-8: AD1CSSH moved from CSS19 and CSS20 to CSS17 and CSS18. The Table Footnote 2 now reads “The CSS<18:17> bits are not implemented in 20-pin devices”.

The Note 2 reference in Register 19-10: AD1CTMENH moved from CTMEN19 and CTMEN20 to CTMEN17 and CTMEN18. The Table Footnote 2 now reads “The CTMEN<18:17> bits are not implemented in 20-pin devices.”

4. Module: Timer1

The first sentence in the Timer1 introduction has changed to the following:

The Timer1 module is a 16-bit timer which operates as a free-running, interval timer/counter.

5. Module: Capture/Compare/PWM/Timer (MCCP and SCCP)

In Register 13-1: CCPxCON1L, corrections have been made, as shown below in **bold**.

CLKSEL<2:0>: CCPx Time Base Clock Select bits(1)

111 = External TCKIA input
110 = External TCKIB input
101 = CLC1
100 = Reserved
011 = LPRC (31 kHz source)
010 = Secondary Oscillator
001 = Reserved
000 = **Peripheral Clock (TCY)**

6. Module: Special Features

In Register 25-6: FPOR, corrections have been made, as shown below in **bold**.

BORV<1:0>: Brown-out Reset **Voltage Level** bits(3)

7. Module: Master Synchronous Serial Port (MSSP)

In Register 14-3: SSPxCON1, corrections have been made, as shown below in **bold**.

SSPM<3:0>: Master Synchronous Serial Port Mode Select bits(3)

1010 = SPI Master mode, Clock = FOSC/(2 * ([SSPxADD] + 1))
0101 = SPI Slave mode, Clock = SCKx pin; SSx pin control is disabled, SSx can be used as an I/O pin
0100 = SPI Slave mode, Clock = SCKx pin; SSx pin control is enabled
0011 = Reserved
0010 = SPI Master mode, Clock = FOSC/32
0001 = SPI Master mode, Clock = FOSC/8
0000 = SPI Master mode, Clock = FOSC/2

8. Module: Real-Time Clock and Calendar (RTCC)

The FRM referenced for the RTCC module in **Section 16.0 "Real-Time Clock and Calendar (RTCC)"** has been corrected. The note with the correct reference is shown below in **bold**.

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the Real-Time Clock and Calendar, refer to the *"PIC24F Family Reference Manual"*, **"RTCC with External Power Control" (DS39745)**.

9. Module: Configurable Logic Cell

In Register 17-4: CLCxGLSL, the following corrections have been made, as shown below in **bold**.

bit 15 G2D4T: Gate 2 Data Source 4 True Enable bit
1 = **The Data Source 4 signal is enabled for Gate 2**
0 = **The Data Source 4 signal is disabled for Gate 2**

bit 14 G2D4N: Gate 2 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2

bit 13 G2D3T: Gate 2 Data Source 3 True Enable bit
1 = **The Data Source 3 signal is enabled for Gate 2**
0 = **The Data Source 3 signal is disabled for Gate 2**

bit 12 G2D3N: Gate 2 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2

bit 11 G2D2T: Gate 2 Data Source 2 True Enable bit
1 = **The Data Source 2 signal is enabled for Gate 2**
0 = **The Data Source 2 signal is disabled for Gate 2**

bit 10 G2D2N: Gate 2 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2

bit 9 G2D1T: Gate 2 Data Source 1 True Enable bit
1 = **The Data Source 1 signal is enabled for Gate 2**
0 = **The Data Source 1 signal is disabled for Gate 2**

bit 8 G2D1N: Gate 2 Data Source 1 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 7 G1D4T: Gate 1 Data Source 4 True Enable bit
1 = **The Data Source 4 signal is enabled for Gate 1**
0 = **The Data Source 4 signal is disabled for Gate 1**

bit 6 G1D4N: Gate 1 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1

bit 5 G1D3T: Gate 1 Data Source 3 True Enable bit
1 = **The Data Source 3 signal is enabled for Gate 1**
0 = **The Data Source 3 signal is disabled for Gate 1**

bit 4 G1D3N: Gate 1 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 1
0 = The Data Source 3 inverted signal is disabled for Gate 1

bit 3 G1D2T: Gate 1 Data Source 2 True Enable bit
1 = **The Data Source 2 signal is enabled for Gate 1**
0 = **The Data Source 2 signal is disabled for Gate 1**

bit 2 G1D2N: Gate 1 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 1
0 = The Data Source 2 inverted signal is disabled for Gate 1

bit 1 G1D1T: Gate 1 Data Source 1 True Enable bit
1 = **The Data Source 1 signal is enabled for Gate 1**
0 = **The Data Source 1 signal is disabled for Gate 1**

bit 0 G1D1N: Gate 1 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 1
0 = The Data Source 1 inverted signal is disabled for Gate 1

10. Module: Electrical Characteristics

in Table 27-22: Internal RC Oscillator Accuracy, the following note has been added for the LPRC:

3: In High-Power/High-Accuracy mode, the Configuration bit, LPRCSEL = 1.

11. Module: Capture/Compare/PWM/Timer (MCCP and SCCP)

In **Section 13.2 "General Purpose Timer",** the text has been updated to omit the sentence below:

The secondary timer uses CCPxTMRH and CCPxPRH. It is intended to be used only as a periodic interrupt source for scheduling CPU events. It does not generate an Output Sync/ Trigger signal like the primary time base.

~~In Dual Timer mode, the Secondary Timer Period register, CCPxPRH, generates the MCCP Compare Event.~~

12. Module: Capture/Compare/PWM/Timer (MCCP and SCCP)

The following changes have been made to Register 19-1: AD1CON1, as shown below in **bold**.

SSRC<3:0>: Sample Clock Source Select bits
1111 = Reserved
•
•
•
1101 = Reserved
1100 = CLC2 event ends sampling and starts conversion
1011 = SCCP4 Capture/Compare Event or Timer (CCP4IF/CCT4IF) ends sampling and starts conversion
1010 = MCCP3 Capture/Compare Event or Timer (CCP3IF/CCT3IF) ends sampling and starts conversion
1001 = MCCP2 Capture/Compare Event or Timer (CCP2IF/CCT2IF) ends sampling and starts conversion
1000 = CLC1 event ends sampling and starts conversion
0111 = Internal counter ends sampling and starts conversion (auto-convert)
0110 = TMR1 Sleep mode Trigger event ends sampling and starts conversion(1)
0101 = TMR1 event ends sampling and starts conversion
0100 = CTMU event ends sampling and starts conversion
0011 = SCCP5 Capture/Compare Event or Timer (CCP5IF/CCT5IF) ends sampling and starts conversion
0010 = MCCP1 Capture/Compare Event or Timer (CCP1IF/CCT1IF) ends sampling and starts conversion
0001 = INT0 event ends sampling and starts conversion
0000 = Clearing the Sample bit ends sampling and starts conversion

13. Module: Pin Diagrams

The pin diagram for the 20-Pin QFN has been removed from the Pin Diagram section.

14. Module: Electrical Characteristics

Thermal Packaging Characteristics for 20-Pin QFN have been removed from Table 27-2.

15. Module: Packaging Information

Package Marking Information and Package Details for 20-pin QFN have been removed.

16. Module: Electrical Characteristics

In Table 27-4, the HLVD Voltage on VDD Transition Min and Max values have been updated, as shown below in **bold**.

TABLE 27-4: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions:	1.8V to 3.6V (PIC24F16KM204) 2.0V to 5.5V (PIC24FV16KM204)						
Operating temperature	-40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended						
Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0000(2)	—	—	**2**	V	
			HLVDL<3:0> = 0001	**1.84**	—	**2.23**	V	
			HLVDL<3:0> = 0010	**2.05**	—	**2.45**	V	
			HLVDL<3:0> = 0011	**2.21**	—	**2.63**	V	
			HLVDL<3:0> = 0100	**2.31**	—	**2.72**	V	
			HLVDL<3:0> = 0101	**2.51**	—	**2.94**	V	
			HLVDL<3:0> = 0110	**2.76**	—	**3.2**	V	
			HLVDL<3:0> = 0111	**2.91**	—	**3.35**	V	
			HLVDL<3:0> = 1000	**3.05**	—	**3.51**	V	
			HLVDL<3:0> = 1001	**3.23**	—	**3.69**(1)	V	
			HLVDL<3:0> = 1010(1)	**3.42**	—	**3.89**	V	
			HLVDL<3:0> = 1011(1)	**3.58**	—	**4.11**	V	
			HLVDL<3:0> = 1100(1)	**3.87**	—	**4.36**	V	
			HLVDL<3:0> = 1101(1)	**4.14**	—	**4.65**	V	
			HLVDL<3:0> = 1110(1)	**4.45**	—	**4.97**	V	

Note 1: These trip points should not be used on PIC24FXXKMXXX devices.
2: This trip point should not be used on PIC24FVXXKMXXX devices.

17. Module: Comparator Module

The bit locations in Register 22-1 for CREF1 and CREF0 have been corrected as shown below in **bold**.

REGISTER 22-1: CMxCON: COMPARATOR x CONTROL REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R-0
CON	COE	CPOL	CLPWR	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	**U-0**	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0	**CREF1**	**CREF0**	**—**	—	CCH1	CCH0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 5-4 CREF<1:0>: Comparator x Reference Select bits (non-inverting input)
11 = Non-inverting input connects to the DAC2 output
10 = Non-inverting input connects to the DAC1 output
01 = Non-inverting input connects to the internal CVREF voltage
00 = Non-inverting input connects to the CxINA pin

bit **3**-2 Unimplemented: Read as '0'

bit 1-0 CCH<1:0>: Comparator x Channel Select bits
11 = Inverting input of the comparator connects to BGBUF1
10 = Inverting input of the comparator connects to the CxIND pin
01 = Inverting input of the comparator connects to the CxINC pin
00 = Inverting input of the comparator connects to the CxINB pin

18. Module: Capture/Compare/PWM/Timer Modules (MCCP AND SCCP)

The reset value for OCAEN in Register 13-4 has been changed from R/W-0 to R/W-1 as shown in **bold** below.

REGISTER 13-4: CCPxCON2H: CCPx CONTROL 2 HIGH REGISTERS

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	**R/W-1**
OENSYNC	—	OCFEN(1)	OCEEN(1)	OCDEN(1)	OCCEN(1)	OCBEN(1)	OCAEN
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ICGSM1	ICGSM0	—	AUXOUT1	AUXOUT0	ICS2	ICS1	ICS0
bit 7							bit 0

19. Module: Capture/Compare/PWM/Timer Modules (MCCP AND SCCP)

The values of SYNC<4:0> for CLC1 and CLC2 in Table 13-6 have been updated as shown in **bold** below.

TABLE 13-6: SYNCHRONIZATION SOURCES

SYNC<4:0>	Synchronization Source
01100 to **01111**	Unused
10000	CLC1 Output(1)
10001	CLC2 Output(1)
10010 to 11010	Unused

Note 1: These sources are only available when the source module is being used in a Synchronous mode.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (2/2013)

Initial release of this document; issued for Revision A0. Includes silicon issues 1-2 (A/D Converter) and 3-6 (MCCP and SCCP).

Rev B Document (9/2013)

Adds silicon issues 7 (MCCP and SCCP) and 8 (Op Amp) to Silicon Revision A0.

Adds data sheet clarification 1 (Memory Organization).

Rev C Document (3/2014)

Adds data sheet clarifications 2 (Electrical Characteristics), 3 (12-Bit A/D Converter with Threshold Detect) and 4 (Timer1).

Rev D Document (3/2015)

Adds silicon issue 9 (Reset) and data sheet clarifications 5 (Capture/Compare/PWM/Timer, MCCP and SCCP), 6 (Special Features), 7 (Master Synchronous Serial Port, MSSP), 8 (Real-Time Clock and Calendar, RTCC), 9 (Configurable Logic Cell), 10 (Electrical Characteristics) and 11-12 (Capture/Compare/PWM/Timer, MCCP and SCCP).

Rev E Document (7/2015)

Adds data sheet clarifications 13 (Pin Diagrams), 14 (Electrical Characteristics) and 15 (Packaging Information).

Rev F Document (1/2016)

Adds new silicon revision ID#: A1.

Rev G Document (7/2016)

Adds data sheet clarification 16 (Electrical Characteristics).

Rev H Document (8/2017)

Updates data sheet clarifications 5 (Capture/Compare/PWM/Timer (MCCP and SCCP)) and 16 (Electrical Characteristics), and adds data sheet clarifications 17 (Comparator Module), 18 (Capture/Compare/PWM/Timer (MCCP and SCCP)) and 19 (Capture/Compare/PWM/Timer (MCCP and SCCP)).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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