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## RTCC with Timestamp

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### HIGHLIGHTS

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# dsPIC33/PIC24 Family Reference Manual

## 1.0 INTRODUCTION

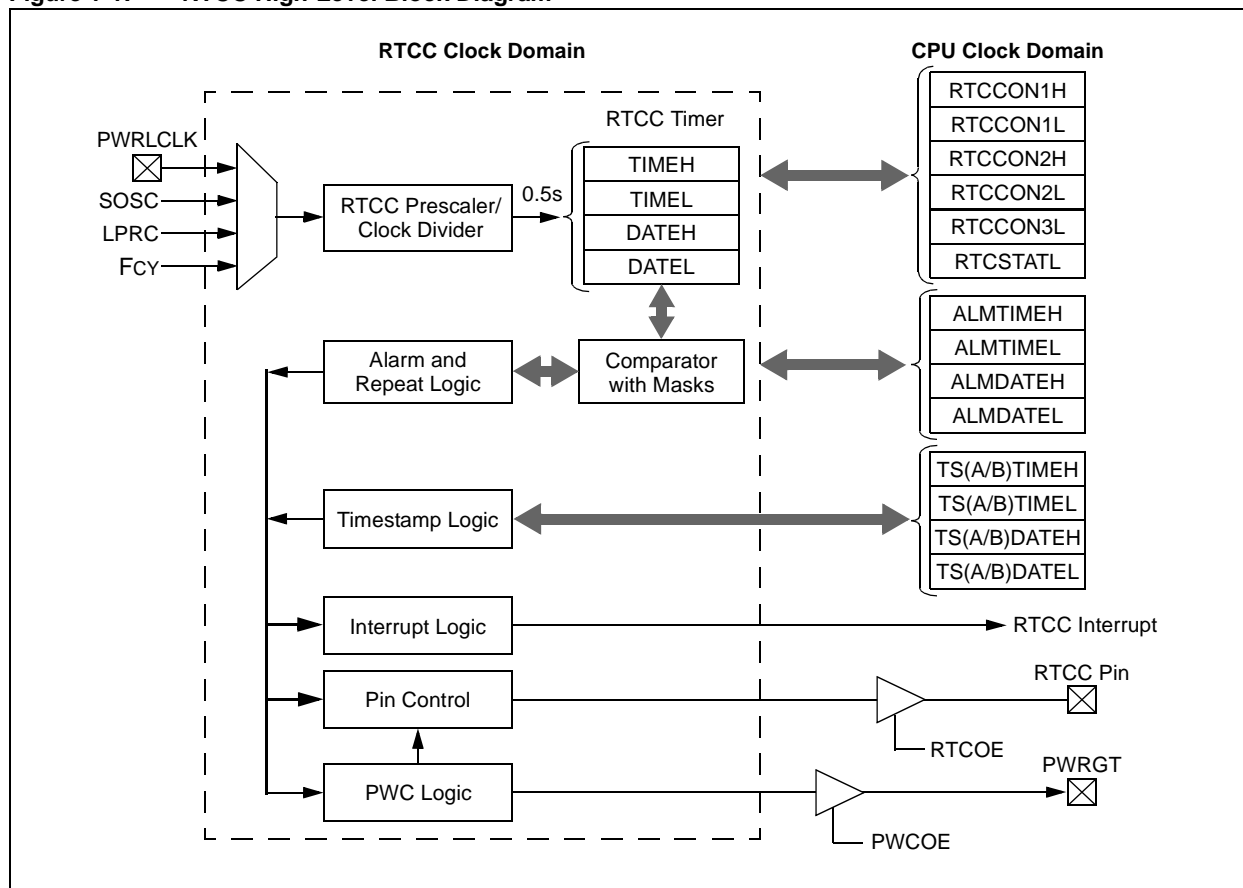
The Real-Time Clock and Calendar (RTCC) hardware module is intended for applications where accurate time must be maintained for extended periods of time with minimum to no intervention from the CPU. The module is optimized for low-power usage in order to provide extended battery lifetime while keeping track of time.

Key features of this module include:

- Time (Hours, Minutes and Seconds) in 24-Hour (Military Time) Format
- Calendar (Weekday, Date, Month and Year)
  - Year Range from 2000 to 2099 with Automatic Leap Year Correction
- Alarm with Configurable Mask and Repeat Options
- BCD Format for Compact Firmware
- Optimized for Low-Power Operation
- Multiple Clock Input Options, Including 32.768 kHz Crystal and Power Line
- User Calibration Within 2 ppm When Using 32 kHz Source
- Interrupt on Alarm and Timestamp Events
- Timestamp Feature for Date and Time Capture from Multiple Trigger Events
- User-Configurable Power Control with Dedicated Output Pin to Periodically Wake External Devices

The RTCC module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099. The hours are available in 24-hour format. The clock provides a granularity of one second with half second visibility to the user.

Figure 1-1: RTCC High-Level Block Diagram



## 2.0 REGISTERS

The RTCC module uses a total of 22 registers, which are organized into four categories.

### 2.1 Control and Status Registers

RTCCON1L ([Register 2-1](#)) is the main control register for the RTCC. Power control features, pin control and timestamping are controlled through this register.

RTCCON1H ([Register 2-2](#)) controls alarm functionality, including alarm mask configuration and alarm repeat.

RTCCON2L ([Register 2-3](#)) controls the RTCC prescalers; it is used to configure the prescaler to generate the 0.5s signal used to drive the timer. It also controls calibration functions.

RTCCON2H ([Register 2-4](#)) contains the value of DIV<15:0>, the 16-bit coarse clock divider; the value stored here is used by the RTCC prescaler to generate a nominal 0.5s timer signal.

RTCCON3L ([Register 2-5](#)) controls the Sampling and Stability windows for the power control functionality.

RTCSTATL ([Register 2-6](#)) contains the event flag status bits for timestamps, calibration and timer synchronization.

### 2.2 Time and Date Registers

Four registers are used to store current time and date information in BCD format:

- TIMEH ([Register 2-7](#)) holds the current time hours and minutes value.
- TIMEL ([Register 2-8](#)) holds the current time seconds value.
- DATEH ([Register 2-9](#)) holds the current year and month value.
- DATEL ([Register 2-10](#)) holds the current date and weekday value.

### 2.3 Alarm Registers

Four registers are used to store the alarm value time and date value. They are formatted identically to the Time and Date registers.

- ALMTIMEH (see [Register 2-7](#) for format)
- ALMTIMEL (see [Register 2-8](#) for format)
- ALMDATEH (see [Register 2-9](#) for format)
- ALMDATEL (see [Register 2-10](#) for format)

### 2.4 Timestamp Registers

Each of the timestamps (Timestamp A and Timestamp B) have a set of four Time and Date registers associated with them. They are normally 16-bit Data registers; when timestamp data is stored in them, they assume the data formatting associated with the corresponding Time and Date registers.

- TSATIMEH and TSBTIMEH (see [Register 2-7](#) for format)
- TSATIMEL and TSBTIMEL (see [Register 2-8](#) for format)
- TSADATEH and TSBDATEH (see [Register 2-9](#) for format)
- TSADATEL and TSBDATEL (see [Register 2-10](#) for format)

## 2.5 RTCC Register Write Lock

To prevent spurious changes to the Time Control or Time Value registers, the WRLOCK bit (RTCCON1L<11>) must be cleared first. By default, WRLOCK is cleared on any device Reset. It is recommended that WRLOCK be set after the Date and Time registers are properly initialized, and the RTCEN bit (RTCCON1L<15>) has been set.

Any attempt to write to the RTCEN bit, the RTCCON2 registers, or the Date or Time registers, will be ignored as long as WRLOCK = 1. Alarm, power control and timestamping features may be changed regardless of the state of WRLOCK.

Clearing the WRLOCK bit requires an unlock sequence, writing two bytes consecutively to the NVMKEY register. A sample assembly sequence is shown in [Example 2-1](#). If WRLOCK is already clear, it can be set (= 1) without using the unlock sequence.

### Example 2-1: Clearing the WRLOCK Bit

```
DISI    #6
MOV     #NVMKEY,W1          ; Refer to specific device data sheet. Register
                               ; used for unlock sequence is device-specific.
MOV     #0x55, W2
MOV     W2, [W1]
MOV     #0xAA, W3
MOV     W3, [W1]
BCLR    RTCCON1L,#WRLOCK
```

**Note:** To avoid accidental writes to the timer, it is recommended that the WRLOCK bit be kept set at any other time. For the WRLOCK bit to be cleared, there is only one instruction cycle time window allowed between the 55h/AA sequence and the clearing of WRLOCK; therefore, it is recommended to use the code example in [Example 2-1](#).

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## 2.6 RTCC Control Registers

**Register 2-1: RTCCON1L: RTCC Control 1 Low Register**

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
RTCEN	—	—	—	WRLOCK	PWCEN	PWCPOL	PWCOE
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
RTCOE	OUTSEL2	OUTSEL1	OUTSEL0	—	—	TSBEN	TSAEN
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15      **RTCEN:** RTCC Enable bit  
1 = RTCC is enabled and counts from selected clock source  
0 = RTCC module is disabled
- bit 14-12    **Unimplemented:** Read as '0'
- bit 11      **WRLOCK:** RTCC Registers Write Lock Bit  
1 = Registers associated with accurate timekeeping are locked  
0 = Registers associated with accurate timekeeping may be written by user
- bit 10      **PWCEN:** Power Control Enable bit  
1 = Power control is enabled  
0 = Power control is disabled
- bit 9        **PWCPOL:** Power Control Polarity bit  
1 = Power control output is active-high  
0 = Power control output is active-low
- bit 8        **PWCOE:** Power Control Output Enable bit  
1 = Power control output pin is enabled  
0 = Power control output pin is disabled
- bit 7        **RTCOE:** RTCC Output Enable bit  
1 = RTCC clock output is enabled; signal selected by OUTSEL<2:0> is presented on the RTCC pin  
0 = RTCC clock output is disabled
- bit 6-4      **OUTSEL<2:0>:** RTCC Signal Output Selection bits  
11x = Unused  
101 = Timestamp B event  
100 = Timestamp A event  
011 = Power control output (PWRGT function on RTCC pin)  
010 = RTCC input clock source  
001 = Seconds clock  
000 = Alarm event
- bit 3-2      **Unimplemented:** Read as '0'
- bit 1        **TSBEN:** Timestamp Source B Enable bit  
1 = Timestamp Source B signal generates a timestamp event  
0 = Timestamp Source B signal is disabled
- bit 0        **TSAEN:** Timestamp Source A Enable bit  
1 = Timestamp Source A signal will generate a timestamp event  
0 = Timestamp Source A signal is disabled

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**Register 2-2: RTCCON1H: RTCC Control 1 High Register**

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ALRMEN	CHIME	—	—	AMASK3	AMASK2	AMASK1	AMASK0
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALMRPT7 <sup>(1)</sup>	ALMRPT6 <sup>(1)</sup>	ALMRPT5 <sup>(1)</sup>	ALMRPT4 <sup>(1)</sup>	ALMRPT3 <sup>(1)</sup>	ALMRPT2 <sup>(1)</sup>	ALMRPT1 <sup>(1)</sup>	ALMRPT0 <sup>(1)</sup>
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **ALRMEN:** Alarm Enable bit

1 = Alarm is enabled

0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit

1 = Chime is enabled; ALMRPT<7:0> bits are allowed to underflow from '00' to 'FF'

0 = Chime is disabled; ALMRPT<7:0> bits stop once they reach '00'

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits

11xx = Reserved, do not use

101x = Reserved, do not use

1001 = Once a year (or once every 4 years when configured for February 29th)

1000 = Once a month

0111 = Once a week

0110 = Once a day

0101 = Every hour

0100 = Every 10 minutes

0011 = Every minute

0010 = Every 10 seconds

0001 = Every second

0000 = Every half second

bit 7-0 **ALMRPT<7:0>:** Alarm Repeat Counter Value bits<sup>(1)</sup>

11111111 = Alarm will repeat 255 more times

11111110 = Alarm will repeat 254 more times

...

00000010 = Alarm will repeat 2 more times

00000001 = Alarm will repeat 1 more time

00000000 = Alarm will not repeat

**Note 1:** The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

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**Register 2-3: RTCCON2L: RTCC Control 2 Low Register**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
FDIV4	FDIV3	FDIV2	FDIV1	FDIV0	—	—	—
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
PWCPS1	PWCPS0	PS1	PS0	—	—	CLKSEL1	CLKSEL0
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **FDIV<4:0>**: Fractional Clock Divide bits

11111 = Clock period increases by 31 RTCC input clock cycles every 16 seconds

11101 = Clock period increases by 30 RTCC input clock cycles every 16 seconds

...

00010 = Clock period increases by 2 RTCC input clock cycles every 16 seconds

00001 = Clock period increases by 1 RTCC input clock cycle every 16 seconds

00000 = No fractional clock division

bit 10-8 **Unimplemented**: Read as '0'

bit 7-6 **PWCPS<1:0>**: Power Control Prescale Select bits

11 = 1:256

10 = 1:64

01 = 1:16

00 = 1:1

bit 5-4 **PS<1:0>**: Prescale Select bits

11 = 1:256

10 = 1:64

01 = 1:16

00 = 1:1

bit 3-2 **Unimplemented**: Read as '0'

bit 1-0 **CLKSEL<1:0>**: Clock Select bits

11 = Peripheral clock (FCY)

10 = PWRLCLK input pin

01 = LPRC

00 = SOSOC

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## Register 2-4: RTCCON2H: RTCC Control 2 High Register

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
DIV<15:8>							
bit 15							
bit 8							

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
DIV<7:0>							
bit 7							
bit 0							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0

**DIV<15:0>**: Clock Divide bits

Sets the period of the clock divider counter; value should cause a nominal 1/2 second underflow.

## Register 2-5: RTCCON3L: RTCC Control 3 Low Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCSAMP7	PWCSAMP6	PWCSAMP5	PWCSAMP4	PWCSAMP3	PWCSAMP2	PWCSAMP1	PWCSAMP0
bit 15							
bit 8							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCSTAB7	PWCSTAB6	PWCSTAB5	PWCSTAB4	PWCSTAB3	PWCSTAB2	PWCSTAB1	PWCSTAB0
bit 7							
bit 0							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8

**PWCSAMP<7:0>**: Power Control Sample Time Window bits

11111111 = Sample input is always allowed (not gated)

11111110 = Sample Time window is 254 TPWC

...

00000010 = Sample Time window is 2 TPWC

00000001 = Sample Time window is 1 TPWC

00000000 = Sample input is always gated

bit 7-0

**PWCSTAB<7:0>**: Power Control Stability Time bits

11111111 = Stability Time window is 255 TPWC

11111110 = Stability Time window is 254 TPWC

...

00000010 = Stability Time window is 2 TPWC

00000001 = Stability Time window is 1 TPWC

00000000 = No Stability Time window



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**Register 2-6: RTCSTATL: RTCC Status Low Register**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

R-0, HSC	U-0	R/C-0, HSC	R/W-0, HSC	R/W-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
CPLCK	—	ALMEVT	TSBEVT <sup>(1)</sup>	TSAEVT <sup>(1)</sup>	SYNC	ALMSYNC	HALFSEC
bit 7						bit 0	

<b>Legend:</b>	C = Clearable Only bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CPLCK:** Calibration PLL Lock Status bit

1 = External calibration PLL is locked; 1 second clock output is valid

0 = External calibration PLL is not locked

bit 6 **Unimplemented:** Read as '0'

bit 5 **ALMEVT:** Alarm Event bit

1 = An alarm event has occurred

0 = An alarm event has not occurred

bit 4 **TSBEVT:** Timestamp B Event bit<sup>(1)</sup>

1 = A Timestamp B event has occurred

0 = A Timestamp B event has not occurred

bit 3 **TSAEVT:** Timestamp A Event bit<sup>(1)</sup>

1 = A Timestamp A event has occurred

0 = A Timestamp A event has not occurred

bit 2 **SYNC:** Synchronization Status bit

1 = Time registers may change during software read

0 = Time registers may be read safely

bit 1 **ALMSYNC:** Alarm Synchronization status bit

1 = Alarm registers (ALMTIME/H and ALMDATE/H) and RTCCON1H should not be modified; ALRMEN and ALMRPT<7:0> bits may change during software read

0 = Alarm registers and Alarm Control registers may be modified safely

bit 0 **HALFSEC:** Half Second Status bit

1 = Second half of 1 second period

0 = First half of 1 second period

**Note 1:** Software may write a '1' to this bit to initiate a timestamp event; the event capture is not valid until the bit reads as '1'.

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## 2.7 Time/Alarm/Timestamp Registers

**Register 2-7: TIMEH/ALMTIMEH/TSATIMEH/TSBTIMEH: Upper Time (Hour/Minute) Registers<sup>(1)</sup>**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **HRTEN<1:0>:** Binary Coded Decimal Value of Hours bits (10-digit)  
Contains a value from 0 to 2.

bit 11-8 **HRONE<3:0>:** Binary Coded Decimal Value of Hours bits (1-digit)  
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes bits (10-digit)  
Contains a value from 0 to 5.

bit 3-0 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes bits (1-digit)  
Contains a value from 0 to 9.

**Note 1:** A write to this register is only allowed when RTCWREN = 1.

**Register 2-8: TIMEL/ALMTIMEL/TSATIMEL/TSBTIMEL: Lower Time (Seconds) Registers<sup>(1)</sup>**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SECTEN<2:0>:** Binary Coded Decimal Value of seconds bits (10-digit)  
Contains a value from 0 to 5.

bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of seconds bits (1-digit)  
Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** A write to this register is only allowed when RTCWREN = 1.

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**Register 2-9: DATEH/ALMDATEH/TSADATEH/TSBDATEH: Upper Date (Month/Year) Registers**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	MHTTEN	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-12     **YRTEN<3:0>**: Binary Coded Decimal Value of Years bits (10-digit)
- bit 11-8     **YRONE<3:0>**: Binary Coded Decimal Value of Years bits (1-digit)
- bit 7-5     **Unimplemented**: Read as '0'
- bit 4     **MHTTEN**: Binary Coded Decimal Value of Months bits (10-digit)  
Contains a value from 0 or 1.
- bit 3-0     **MTHONE<3:0>**: Binary Coded Decimal Value of Months bits (1-digit)  
Contains a value from 0 to 9.

**Register 2-10: DATEL/ALMDATEL/TSADATEL/TSBDATEL: Lower Date (Day/Date) Registers**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-0
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-14     **Unimplemented**: Read as '0'
- bit 13-12     **DAYTEN<1:0>**: Binary Coded Decimal Value of Days bits (10-digit)  
Contains a value from 0 to 3.
- bit 11-8     **DAYONE<3:0>**: Binary Coded Decimal Value of Days bits (1-digit)  
Contains a value from 0 to 9.
- bit 7-3     **Unimplemented**: Read as '0'
- bit 2-0     **WDAY<2:0>**: Binary Coded Decimal Value of Weekdays bits (1-digit)  
Contains a value from 0 to 6.

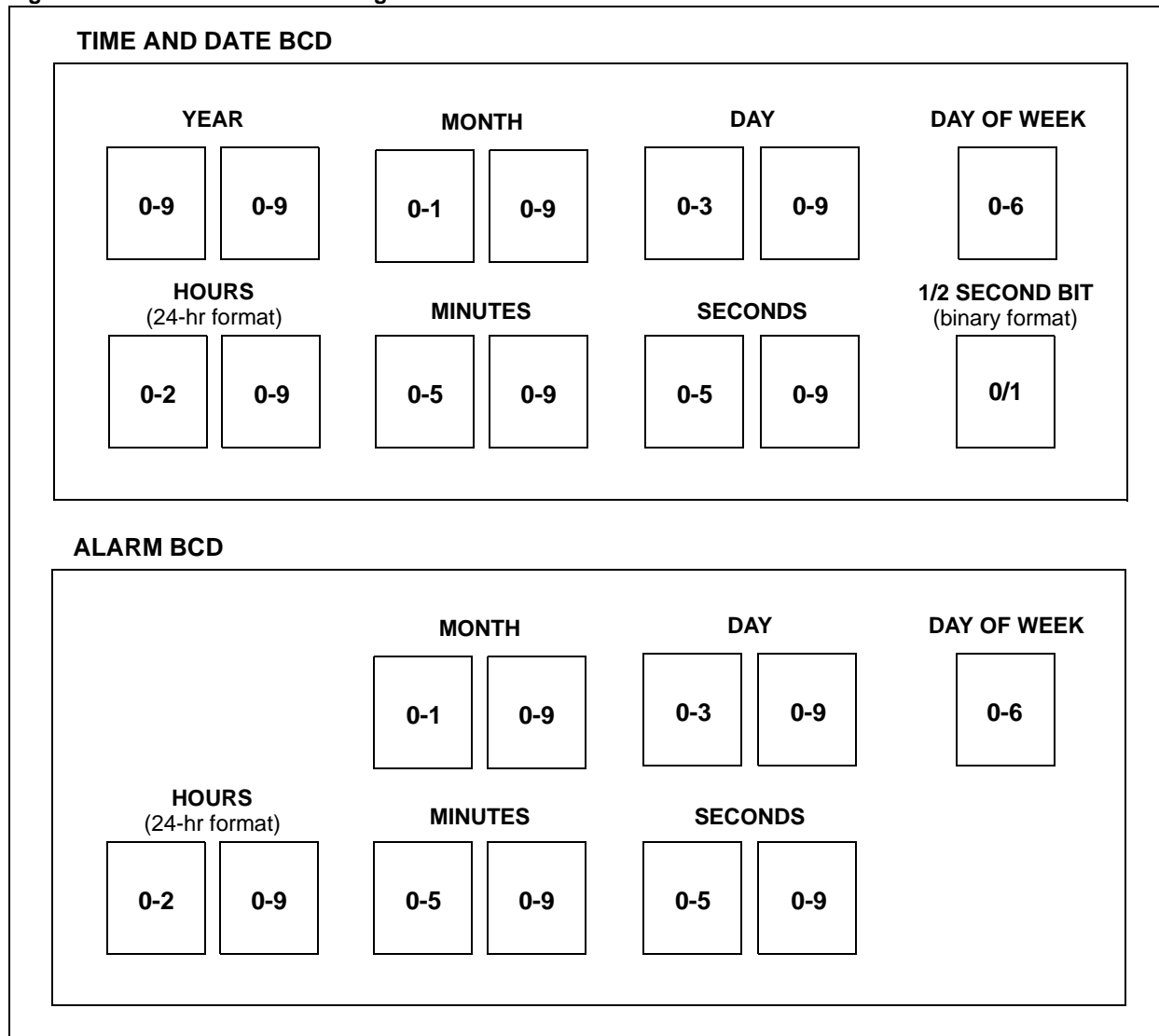
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## 3.0 OPERATION

### 3.1 Register Interface

The register interface for the RTCC and alarm values is implemented using natural Binary Coded Decimal (BCD) format. This simplifies the firmware, when using the module, as each of the digit values is contained within its own 4-bit value (see [Figure 3-1](#)).

Figure 3-1: Timer and Alarm Digit Format



### 3.2 General Functionality

All Timer registers containing a time value of seconds or greater are writable. The user can configure the time by writing the desired year, month and day to the DATEL and DATEH registers; and the hour, minutes and seconds to the TIMEL and TIMEH registers. The timer will then use the newly written values and proceed with the count from the desired starting point. The RTCC module is enabled by setting the RTCEN bit (RTCCON1L<15>). If enabled while adjusting these registers, the timer will still continue to increment.

The user has visibility to the half second field of the counter, HALFSEC (RTCSTATL<0>). This value is read-only, and can only be reset by writing to SECONE<3:0> (TIMEL<11:8>).

## 3.3 Synchronization

Because the CPU and the RTCC operate in different clock domains, care must be taken when reading and writing the RTCC registers. The user is responsible to assure that when  $RTCEN = 1$ , the updated registers will not be incremented at the same time. This can be accomplished in several ways:

- Checking the SYNC bit ( $RTCSTATL<2>$ );
- Checking the preceding digits from which a carry can occur; or
- Updating the registers immediately following the seconds pulse (or alarm interrupt).

The SYNC bit indicates a time window during which the RTCC Clock Domain registers can be safely read and written without concern about a rollover. When  $SYNC = 0$ , the registers can be safely accessed by the CPU. Whether  $SYNC = 1$  or  $0$ , the user should employ a firmware solution to assure that the data read did not fall on a rollover boundary, resulting in an invalid or partial read. This firmware solution would consist of reading each register twice and then comparing the two values. If the two values match, then a rollover did not occur.

## 3.4 Digit Carry Rules

Certain timer values are affected when there is a rollover:

- Time of Day: from 23:59:59 to 00:00:00 with a carry to the day field
- Day of Week: from 6 to 0 with no carry (refer to [Table 3-1](#) for values)
- Day (DAYONEx and DAYTENx fields together): from 28, 29, 30 or 31, with a carry to the month field (refer to [Table 3-2](#) for the schedule)
- Month (MTHONEx and MHTEN fields together): from 12/31 to 01/01 with a carry to the year field
- Year Carry: from 99 to 00; this also surpasses the use of the RTCC

**Table 3-1: Day of Week Schedule**

Day of Week	WDAY Value
Sunday	0
Monday	1
Tuesday	2
Wednesday	3
Thursday	4
Friday	5
Saturday	6

**Table 3-2: Day to Month Rollover Schedule**

Month	Maximum Day Field	Month	Maximum Day Field
01 (January)	31	07 (July)	31
02 (February)	28 or 29 <sup>(1)</sup>	08 (August)	31
03 (March)	31	09 (September)	30
04 (April)	30	10 (October)	31
05 (May)	31	11 (November)	30
06 (June)	30	12 (December)	31

**Note 1:** See [Section 3.4.1 “Leap Year”](#) for details.

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As the module uses BCD format, the carry to the upper BCD digit occurs at a count of 10 and not a count of 16 for these fields:

- SEC
- MIN
- HR
- WDAY
- DAY
- MON

## 3.4.1 LEAP YEAR

Since the year range on the RTCC module is 2000 to 2099, the leap year calculation is determined by any year, divisible by 4, in the above range. The only month to be affected in a leap year is February. The month of February will have 29 days in a leap year, while any other year, it will have 28 days.

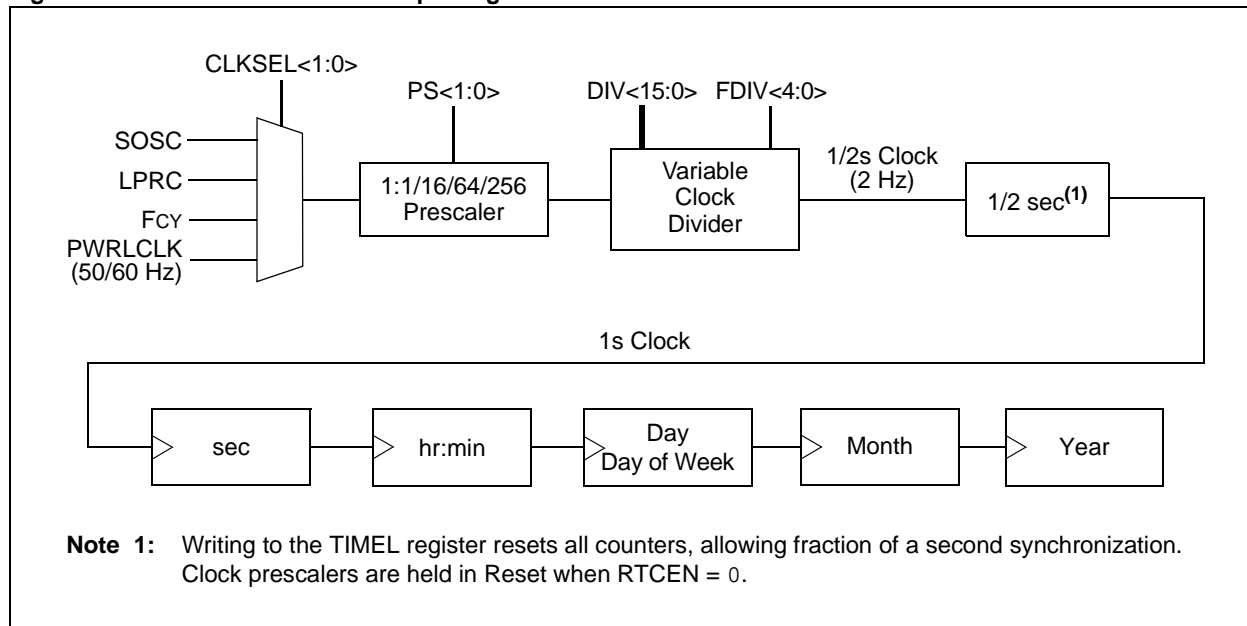
## 3.5 Clock Source

The RTCC clock source is selected with the CLKSEL<1:0> bits (RTCCON2L<1:0>). It is designed to operate from any one of four clock sources:

- The crystal-controlled 32.768 kHz Secondary Oscillator (SOSC)
- The Internal Low-Power RC 31 kHz Oscillator (LPRC)
- The microcontroller peripheral clock, operating at the instruction frequency (FCY)
- The PWRLCLK pin input, generally derived from the local mains frequency (50/60 Hz)

Each option provides users with choices of application component count and accuracy over time. The Secondary Oscillator (SOSC) provides the highest accuracy and lowest power consumption option. When used as the source, calibration of the crystal can be accomplished through this module yielding an error of 3 seconds or less per month. See [Section 3.6 “Clock Calibration”](#) for further details.

**Figure 3-2: Clock Source Multiplexing and Divider Chain**



## 3.5.1 CLOCK DIVIDER

The RTCC timer must be provided with a 1/2 second (2 Hz) clock source. This is done by selecting appropriate values for the clock prescaler and the variable clock divider.

The clock prescaler divides the input clock by one of four fixed ratios. It is controlled by the PS<1:0> bits (RTCCON2L<5:4>). Divider options are 1:1, 1:16, 1:64 and 1:256.

The variable coarse clock divider further divides the clock input from the prescaler. It provides the entire range of integer divisor options, from 1:1 to 1:32,768. It is controlled by the DIV<15:0> bits field (RTCCON2H<15:0>).

The clock divider also has a fine divider, controlled by the FDIV<4:0> bits. This permits fine frequency adjustments to the timer output. This is discussed in [Section 3.6 “Clock Calibration”](#).

Selection of a particular clock input with the CLKSELx bits does not automatically select an appropriate prescaler or clock divider option. It is the user's responsibility to configure the prescaler and divider correctly to provide a 2 Hz signal to the timer. [Table 3-3](#) lists the most common combinations for typical clock sources. [Equation 3-1](#) shows how to calculate the prescaler and DIVx values for any input frequency.

**Table 3-3: Clock Divider vs. Input Frequency (Nominal Clock Frequencies)**

Input Frequency	Prescaler	DIV<15:0>	FDIV<4:0>
32,768 kHz	1:1	3FFF	00000
60 Hz	1:1	1D	00000
50 Hz	1:1	18	00000
16 MHz	1:256	7A11	00000

**Equation 3-1: RTCC Clock Frequency Divider Output Frequency**

$$F_{OUT} = \frac{1}{2} \cdot \left[ \frac{F_{IN}}{\text{Prescale} \cdot (\text{DIV}<15:0> + 1) + \frac{\text{FDIV}<4:0>}{32}} \right]$$

Where:

$$\text{DIV}<15:0> = \frac{F_{IN}}{2 \cdot \text{PRESCALE}} - 1$$

and  $\text{FDIV}<4:0>$  is the fractional remainder of  $\text{DIV}<15:0>$ , multiplied by 32

## 3.5.2 SECONDARY OSCILLATOR (SOSC) ENABLE

If the RTCC is configured to use the Secondary Oscillator, it will automatically be enabled when the RTCC is enabled. The SOSCEN bit (OSCCON<1>) does not need to be set. For more information on the Secondary Oscillator, refer to the “Oscillator Configuration” chapter of the device data sheet.

## 3.5.3 LOW-POWER RC OSCILLATOR ENABLE

If the RTCC is configured to be clocked by LPRC, the LPRC will automatically be enabled. Refer to the “Oscillator Configuration” chapter of the device data sheet for more information on the LPRC.

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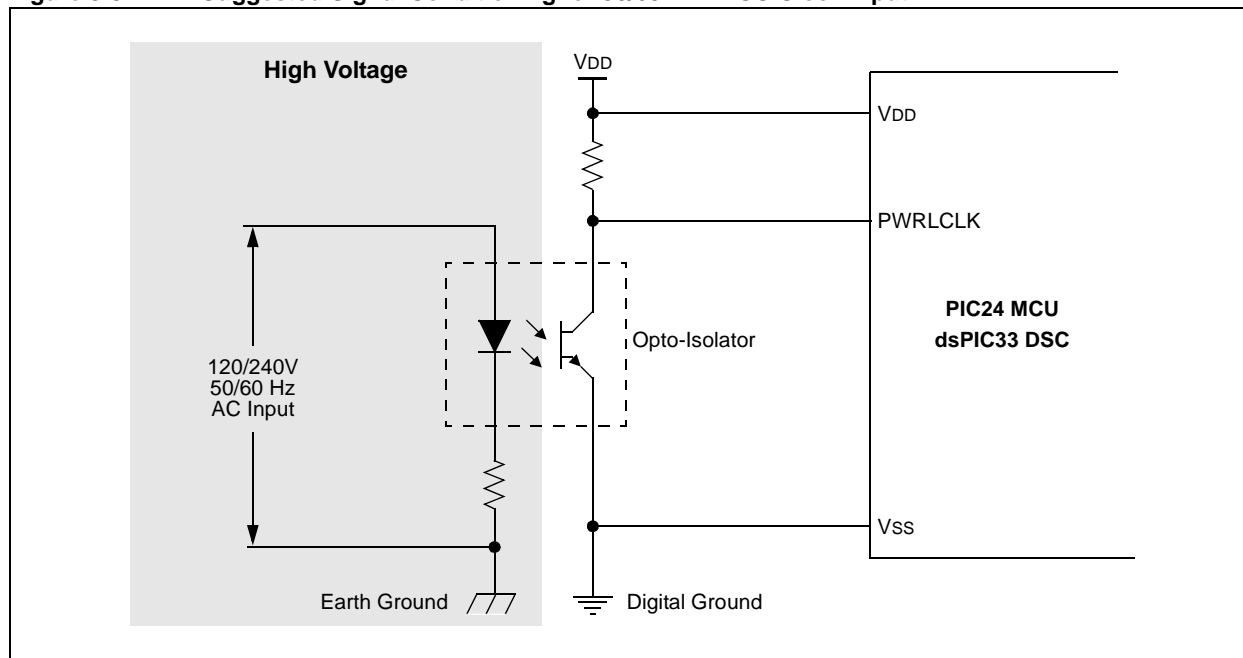
## 3.5.4 CLOCK SOURCE FROM POWER LINE (50/60 HZ SIGNAL)

It is possible to use the power mains as an external clock source for the RTCC. The module can use either 50 or 60 Hz AC, to accommodate local power in most locations throughout the world.

Line voltage cannot be used directly to provide the clock reference. For safety reasons, the line voltage must be properly isolated from the digital portion of the application. Failure to properly design the circuitry that interfaces mains voltage to the microcontroller may result in a fatal shock.

Figure 3-3 shows a suggested signal conditioning circuit for such a clock source.

**Figure 3-3: Suggested Signal Conditioning for 50/60 Hz RTCC Clock Input**



## 3.6 Clock Calibration

In addition to the 16-bit coarse divider ( $DIV<15:0>$ ), the variable clock divider also uses a fine clock frequency divisor to make small trim adjustments to the nominal 0.5s timer signal. This fine divider,  $FDIV<4:0>$  ( $RTCCON2L<15:11>$ ), acts as the fractional part of a 21-bit clock divider when used with  $DIV<15:0>$ .

The fine divider operates on the variable clock divider output every 1/2 second, optionally omitting a clock cycle. This effectively stretches the period set by the period counter by one clock cycle. When  $FDIV<4:0> = 01h$ , it takes 16 seconds to remove a clock cycle and see any effect on the output. The maximum effect is when  $FDIV<4:0> = 31$  (decimal), which represents 31 clock cycles removed over 16 seconds. When  $FDIV<4:0> = 0$ , the clock period is not affected by the fine divider.

Deviation from the desired input frequency is adjusted by changing the values of  $DIVx$  and  $FDIVx$  accordingly, as calculated by Equation 3-1. A faster than desired oscillator generally requires increases to the value of  $FDIVx$  for small changes, or decreases to the value of  $DIVx$  for large changes. On the other hand, a slow oscillator requires decreases to the value of  $FDIVx$ , or increases to the value of  $DIVx$ . Table 3-4 shows the effect of changing  $DIVx$  and  $FDIVx$ ; Example 3-1 demonstrates the calculation of  $FDIVx$  in these cases.



# RTCC with Timestamp

The fine clock divider is optimized to provide an adjustment error of less than 2 ppm when operating from a crystal-controlled 32.768 kHz oscillator. Even so, it is effective for fine-tuning the timer signal frequency, regardless of the clock input.

**Note:** Before calibration, the user must determine the error of the crystal. This should be done using another timer resource on the device or an external timing reference. It is the user's responsibility to include in the error value the initial error of the crystal, drift due to temperature and drift due to crystal aging.

**Table 3-4: Clock Divider vs. Input Frequency (Showing Fine-Tuning Options)**

Input Frequency	Prescaler	DIV<15:0>	FDIV<4:0>
32,767.9 kHz <sup>(1)</sup>	1:1	3FFE	1E
32,768.0 kHz	1:1	3FFF	00
32,768.3 kHz <sup>(1)</sup>	1:1	3FFF	05
59.9 Hz <sup>(1)</sup>	1:1	1C	1E
60 Hz	1:1	1D	00
60.1 Hz <sup>(1)</sup>	1:1	1D	02

**Note 1:** These selections are provided to demonstrate settings for a clock source slightly faster or slower than the desired output frequency.

**Example 3-1: Clock Divider Calculation (with FDIV<4:0>)**

$F_{IN} = 32767.8 \text{ Hz}$  (Oscillator running slow)  
Prescaler = 1:1  
Divide Ratio =  $32767.8/2 - 1 = 16382.9$   
Therefore,  $DIV<15:0> = 16382$  and  $FDIV<4:0> = 32(0.9) = 29$

## 3.7 RTCC Pin

The RTCC pin can be configured by the OUTSEL<2:0> bits (RTCCON1L<6:4>) to present any one of several outputs:

- One second clock pulse
- A direct pass-through of the RTCC input clock source
- Alarm signal (see [Section 4.0 “Alarm”](#) for details)
- Power control pin, in addition to or as an alternative to the PWRGT pin (see [Section 5.0 “Power Control”](#) for details)
- Timestamp events (see [Section 6.0 “Timestamping”](#) for details)

When used as an output, the RTCC Output Enable bit, RTCOE (RTCCON1L<7>), must also be set.

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## 4.0 ALARM

The RTCC alarm includes these features:

- Configurable from half second to one year
- One-time alarm and repeat alarm options available

### 4.1 Configuring the Alarm

The alarm feature is enabled by setting the ALRMEN bit (RTCCON1H<15>). This bit is cleared by hardware when an alarm is issued, but is not cleared if the CHIME bit (RTCCON1H<14>) = 1, or if ALMRPT<7:0> (RTCCON1H<7:0>) has any value other than 00h.

The interval selection of the alarm is configured through the AMASK<3:0> bits (RTCCON1H<11:8>). These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur. Figure 4-1 shows the available alarm mask options.

**Note:** Changing any of the control bits, other than RTCOE, ALMRPT<7:0> and CHIME, while the alarm is enabled (ALRMEN = 1), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, change the timer and alarm values only while the alarm is disabled (ALRMEN = 0). It is recommended that these bits be changed when ALMSYNC = 0.

Figure 4-1: Alarm Mask Settings

Alarm Mask Setting AMASK<3:0>	Day of the Week	Month	Day	Hours	Minutes	Seconds
0000 – Every half second	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>
0001 – Every second	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>
0010 – Every 10 seconds	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> s
0011 – Every minute	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> s
0100 – Every 10 minutes	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> m	<input type="checkbox"/> s
0101 – Every hour	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> m	<input type="checkbox"/> s
0110 – Every day	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> h	<input type="checkbox"/> h	<input type="checkbox"/> s
0111 – Every week	<input type="checkbox"/> d	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> h	<input type="checkbox"/> h	<input type="checkbox"/> s
1000 – Every month	<input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> d	<input type="checkbox"/> h	<input type="checkbox"/> h	<input type="checkbox"/> s
1001 – Every year <sup>(1)</sup>	<input type="checkbox"/>	<input type="checkbox"/> m	<input type="checkbox"/> d	<input type="checkbox"/> h	<input type="checkbox"/> h	<input type="checkbox"/> s

**Note 1:** Annually, except when configured for February 29.

## 4.2 Alarm Repeat and Chime

The alarm can also be configured to repeat based on a preconfigured interval. The amount of times this occurs once the alarm is enabled is determined by the ALMRPT<7:0> bits. The alarm can be repeated up to 255 times. When ALMRPT<7:0> = 00h and CHIME = 0, the repeat function is disabled and only a single alarm will occur.

After each alarm is issued, the ALMRPT<7:0> bits are decremented by one. Once the bit field has reached '00', the alarm will be issued one last time, after which, the ALRMEN bit is cleared automatically and the alarm is turned off.

Indefinite repetition of the alarm can occur if the CHIME bit = 1. Instead of the alarm being disabled when the ALMRPT<7:0> bits reach 00h, the value of the bit field rolls over to FFh and continues to count down indefinitely.

## 4.3 Alarm Interrupt

An interrupt is generated at every alarm event. When an event occurs, the ALMEVT bit (RTCSTATL<5>) is set. This allows the application to distinguish an alarm interrupt from other interrupt events, if necessary. The application should clear ALMEVT after an RTCC interrupt in order to distinguish additional alarm events (or other interrupts if they are enabled).

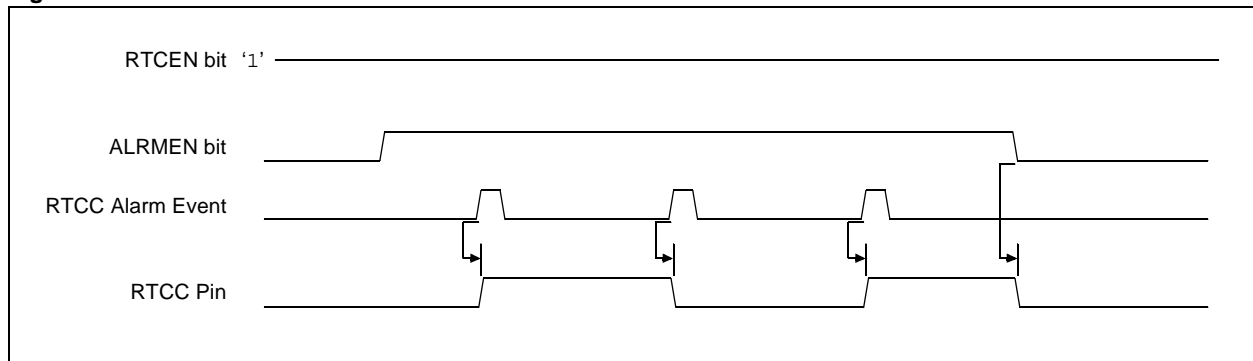
## 4.4 Alarm Output

In addition to the alarm interrupt, an alarm pulse output is provided that operates at half the frequency of the alarm. This output is completely synchronous to the RTCC clock and can be used as a trigger clock to other peripherals. This output is available on the RTCC pin. The output pulse is a clock with a 50% duty cycle and a frequency half that of the alarm event (see [Figure 4-2](#)).

The alarm output pulse is presented on the RTCC pin whenever the OUTSEL<2:0> bits (RTCCON1L<6:4>) = 000. The RTCC Output Enable bit, RTCOE (RTCCON1L<7>), must also be set.

**Note:** When the timer value reaches that of the Alarm registers, one period of the RTCC clock will elapse before the alarm interrupt is set. As a result, the application will see the timer value at the alarm value before the interrupt has occurred.

**Figure 4-2: Timer Pulse Generation**



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## 5.0 POWER CONTROL

The RTCC includes a power control feature that allows the device to periodically wake up an external device, wait for the device to be stable before sampling wake-up events from that device and then shut down the external device. This can be done completely autonomously by the RTCC without the need to wake from the current lower power mode (Sleep, Deep Sleep, etc.).

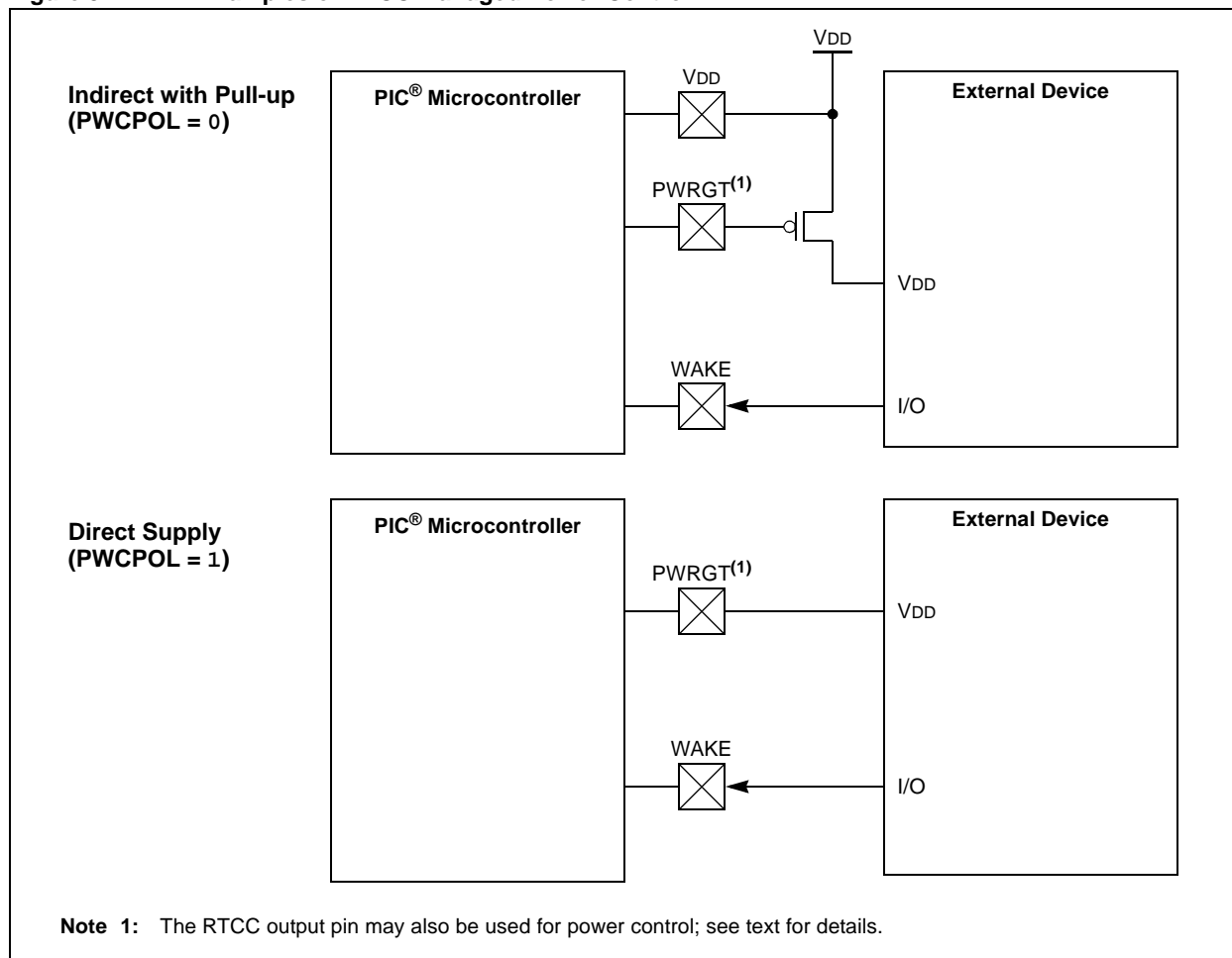
The power control feature uses the PWRGT output pin; the RTCC output pin may also be used with PWRGT, or as an alternative. (Select devices may only use the RTCC pin for power control. Refer to the device data sheet for more information.) Two possible control circuits for this feature are shown in Figure 5-1. The WAKE pin in both examples represents an input that would wake up the device in the desired circumstances (e.g., INT0 in Deep Sleep, any enabled interrupt in Sleep, etc.).

The top of the figure illustrates a situation in which the external device requires more current than the I/O pin can reliably generate. Note that the power control polarity is active-low in order to provide the external device power at the correct times.

A more straightforward approach is shown in the bottom of the figure. For external devices, whose current consumption is within the range an I/O pin can provide (approximately 20 mA), the device can be powered directly via the PWRGT or RTCC pin. If the device requires a stabilizing capacitor on VDD, this method could result in a significant current load. To use this layout, the capacitor would have to be very small (0.01  $\mu\text{F}$ ) or allowances for a greater time to reach operating stability may be required (see Section 5.2 “Power Control Operation” for more information).

To determine the best power control configuration for any given application, refer to the data sheets for both the Microchip device and the external device.

Figure 5-1: Examples of RTCC Managed Power Control



## 5.1 Initialization

To enable power control:

- The RTCC must be enabled (RTCEN (RTCCON1L<15>) = 1)
- Power control must be enabled (PWCEN (RTCCON1L<10>) = 1)
- The PWRGT and/or RTCC pins must be enabled for power control:
  - For PWRGT, the pin must be enabled (PWCEN (RTCCON1L<10>) = 1)
  - For RTCC, the pin must be enabled (RTCOE (RTCCON1L<7>) = 1) and configured for power control (RTCCON1L<6:4> = 011)

In addition, set the CHIME bit (RTCCON1H<14>) to enable the PWC periodicity.

The polarity of the PWC control signal on both pins is selected using the PWCPOL bit (RTCCON1L<9>). Active-low or active-high may be used with the appropriate external switch to turn on or off the power to one or more external devices. The active-low setting may also be used in conjunction with an open-drain setting on the PWRGT or RTCC pads, in order to drive the GND or Vss pin(s) of the external device directly (with the appropriate external VDD pull-up device), without the need for external switches.

## 5.2 Power Control Operation

When the RTCC and PWC are enabled and running, the PWC logic generates a control output and a sample gate output. The control output is driven out on either the PWRGT pin or the RTCC pin, and is used to power up or down the external device.

Once the control output is asserted, the Stability window begins. During this interval, the external device is given enough time to power-up and provide a stable output. When the output is (theoretically) stable, the Sample window begins. In this interval, the RTCC monitors for the wake-up signal from the external device. Typically, a sample gate is used to mask out one or more wake-up signals from the external device.

Finally, both the Stability and Sample windows close after the expiration of the Sample window, and the external device is powered down.

### 5.2.1 STABILITY AND SAMPLE WINDOWS

The Stability and Sample windows are defined in terms of the RTCC clock source, the PWC prescaler, and the PWCSTABx and PWCSAMPx bits field in the RTCCON3L register (RTCCON3L<15:8> and <7:0>, respectively).

The clock source selected for the RTCC is also used for the PWC clock source. A dedicated prescaler, controlled by the PWCPx<1:0> bits (RTCCON2L<7:6>), divides the RTCC clock input. Divider options of 1:1, 1:16, 1:64 or 1:256 are available. The clock and prescaler selections determine the base value of the PWC clock period. The 8-bit magnitude of PWCSTABx and PWCSAMPx allows for a Stability/Sample window size of 0 to 255 clock periods. [Table 5-1](#) shows the size of the windows for common RTCC clock and prescaler options.

Certain values for PWCSTABx and PWCSAMPx have specific control meanings in determining power control operations. If either field is 00h, the corresponding window is inactive. In addition, if the PWCSTABx field is FFh, the Stability window remains active continuously, even if power control is disabled.

**Table 5-1: Stability and Sample Windows for Common Clock Sources**

Clock Source	PWCPx<1:0>	PWCSTAB<7:0> Range	PWCSAMP<7:0> Range
SOSC (32.768 kHz)	11 (1:256)	0 ms-2s	0 ms-2s
LPRC (31 kHz)	11 (1:256)	0 ms-2.1s	0 ms-2.1s
Power Line (50 Hz)	00 (1:1)	0 ms-5.12s	0 ms-5.12s
Power Line (60 Hz)		0 ms-4.25s	0 ms-4.25s

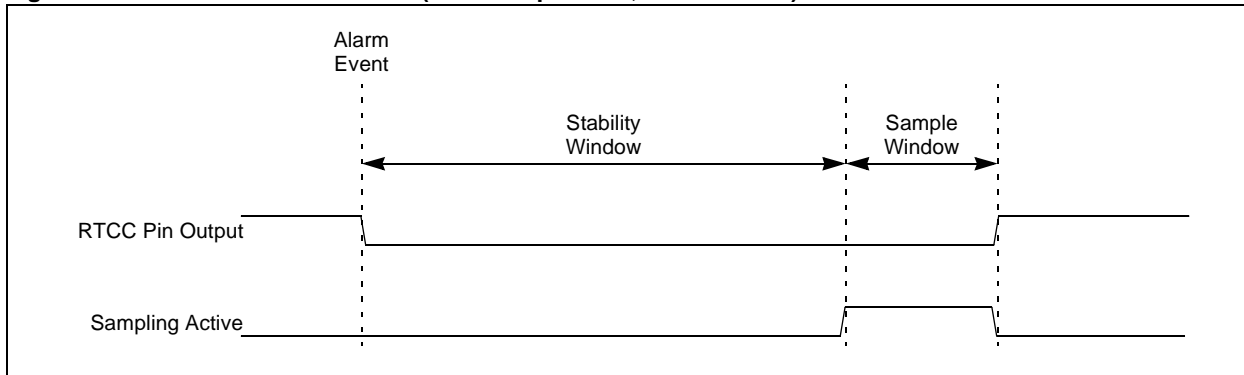
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## 5.2.2 MODES OF OPERATION

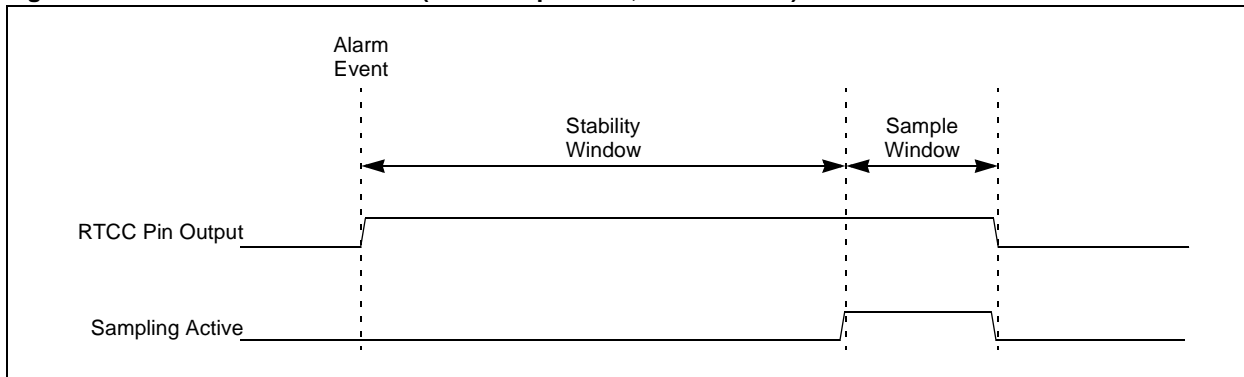
### 5.2.2.1 Normal Operation (Stability and Sample Windows Active)

When PWCSTABx is not 0 and PWCSAMPx is any value except 0 or 255, the PWC is configured for the normal mode of operation. In this mode, the external wake-up interrupt should be connected to the external device, controlled by the PWC power enable. [Figure 5-2](#) shows operation with inverted (active-low) operation; [Figure 5-3](#) shows normal (active-high) operation.

**Figure 5-2: Power Control Timer (Normal Operation, PWCPOL = 0)**



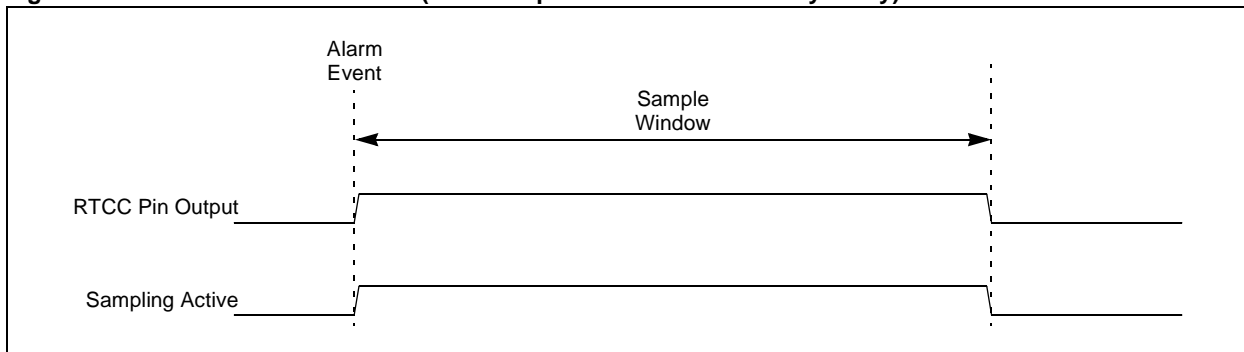
**Figure 5-3: Power Control Timer (Normal Operation, PWCPOL = 1)**



### 5.2.2.2 Normal Operation without Stability Delay (Stability Window Inactive)

When PWCSTABx is 0 and PWCSAMPx is any value except 0 or 255, the PWC is configured for the normal mode of operation with no stability time, as shown in [Figure 5-4](#). This mode is recommended when the external device, controlled by the PWC power enable, requires no time between when power is applied and when its wake-up or interrupt output is valid. Although a valid option, this case is considered to be unlikely.

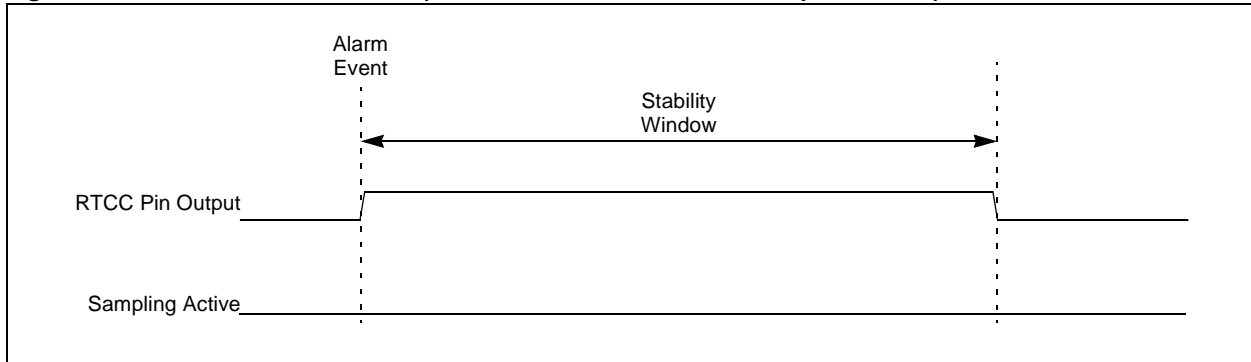
**Figure 5-4: Power Control Timer (Normal Operation without Stability Delay)**



## 5.2.2.3 Power Control without Sampling (Sample Window Inactive)

When PWCSTABx is any value but 0 and PWCSAMPx is 0, the PWC is configured for power control only. No wake-up or interrupt sampling occurs, as shown in [Figure 5-5](#). This mode is generally not used.

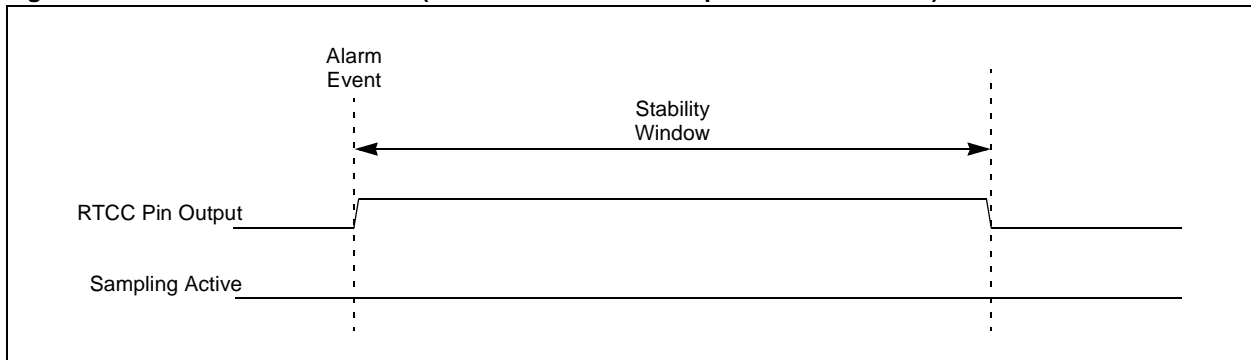
**Figure 5-5: Power Control Timer (Power Control with Inactive Sample Window)**



## 5.2.2.4 Power Control without Sampling (Sample Window Unused)

When PWCSTABx is any value but 0 and PWCSAMPx is 255, the PWC is configured for power control only. The Sample window, although always active, is not used. This is shown in [Figure 5-6](#). This mode should be used when the external device, controlled by the PWC power enable, does not drive a wake-up or interrupt input directly. In this case, the sampling of external interrupts is disabled and the external interrupt may be driven by any source.

**Figure 5-6: Power Control Timer (Power Control with Sample Window Unused)**



## 5.2.2.5 PWC Disabled

When PWCEN is cleared ( $RTCPWC<15> = 0$ ), the PWCSTABx and PWCSAMPx fields have no effect. In this case, the sampling of external interrupts is disabled; the external interrupt may be driven by any source.

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## 6.0 TIMESTAMPING

The RTCC provides up to two sets of Timestamp registers that are used to capture the Time and Date register values when an external input signal is received. The RTCC has a timestamp event input assigned to each of set of Timestamp registers, Timestamp A and Timestamp B (TSATIMEL/H, TSADATEL/H, etc). Timestamp event sources are device dependent; please see the device data sheet for further details.

Because the Timestamp registers are all essentially “blank” 16-bit registers (i.e., all bits are implemented and do not have special Reset conditions), these registers may also be used as backup RAM during Deep Sleep and VBAT modes if the RTCC is configured for VBAT operation.

### 6.1 Operation

Each event input is enabled for timestamping using the TSAEN and TSBEN bits (RTCCON1L<1:0>). If a bit is clear, the event input for the corresponding set of Timestamp registers is disabled. User software may then use the TSxTIMEL/H and TSxDATEL/H register pairs for data storage.

When TSxEN = 1, the timestamp source is enabled. When a timestamp event is detected, the present time and date values are stored in the respective TSxTIMEL/H and TSxDATEL/H registers. The TSxEVT status bit becomes set and an RTCC interrupt occurs. The TSxTIMEL/H and TSxDATEL/H registers become read-only when TSxEN = 1. A new timestamp capture event cannot occur until the TSxEVT bit is cleared in software. The edge sensitivity of the timestamp event depends on the source; see the device data sheet for more information.

The data stored in TSxTIMEL/H and TSxDATEL/H is maintained throughout all Resets, except for POR and BOR.

### 6.2 Manual Timestamping

The present time and date can be captured in software by writing a ‘1’ to the TSxEVT bit. This does not immediately set the TSxEVT bit, but initiates a timestamp capture. When the capture is completed, the TSxEVT bit becomes set. The application must poll the TSxEVT bit to determine when the capture has completed.

After the Timestamp registers have been read, clear the TSxEVT bit to allow further hardware or software timestamp capture events.

## 7.0 INTERRUPTS

The RTCC generates a single, top-level interrupt flag, RTCCIF. This interrupt can be triggered by either a timestamp event (TSA or TSB) or by an RTCC alarm event. Setting the RTCCIE bit allows a device-level interrupt to be generated.

If the source of the interrupt is required, the application may poll the appropriate bits in the RTCSTATL register (TSAEVT, TSBEVT or ALMEVT, respectively) to see which event has occurred.



## 8.0 RESETS

### 8.1 Device Reset

When a device Reset, other than POR or BOR occurs, the RTCC will continue to operate if it was already enabled. The Alarm Date and Time registers will need to be reloaded.

### 8.2 Power-on Reset (POR)

The RTCCON registers, and the Time and Date registers are reset on a POR or BOR. Once the device exits the POR state, the time is reset to 12 midnight (00:00:00) on Saturday, January 1st, 2000; the correct time and date will need to be written to these registers.

The timer prescaler values can only be reset by writing to the TIMEL register. No device Reset can affect the prescalers.

## 9.0 OPERATION IN POWER-SAVING MODES

### 9.1 Idle Mode

Idle mode does not affect the operation of the timer or alarm.

### 9.2 Sleep Modes

The timer and alarm continue to operate while in Sleep mode, including Deep Sleep mode. The operation of the alarm is not affected by Sleep, as an alarm event can always wake up the CPU.

### 9.3 VBAT Mode

In devices that include VBAT power-saving features, the RTCC is capable of continued operation during this mode. While the alarm still functions, it will not wake the device.

The RTCBAT Configuration bit controls this feature. By default (RTCBAT = 1), continued RTCC operation in VBAT mode is enabled.

While in VBAT mode, the RTCC clock source selected by the CLKSEL<1:0> bits remains active. Users should remember to include the incremental current consumption required for the clock source when calculating a power budget for VBAT operation.

## 10.0 PERIPHERAL MODULE DISABLE (PMD) REGISTER

The Peripheral Module Disable (PMD) registers provide a method to disable the RTCC module by stopping all clock sources supplied to that module. When a peripheral is disabled via the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral will also be disabled, so writes to those registers will have no effect and read values will be invalid. The RTCC will only be enabled if the RTCCMD bit in the PMDx register is cleared.

## 11.0 REGISTER MAPS

A summary of the registers associated with the RTCC with Timestamp module is provided in [Table 11-1](#).

**Table 11-1: RTCC with Timestamp Register Map**

Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RTCCON1L	RTCON	—	—	—	WRLOCK	PWCEN	PWCPOL	PWCOE	RTCOE	OUTSEL2	OUTSEL1	OUTSEL0	—	—	TSBEN	TSAEN	0000
RTCCON1H	ALRMEN	CHIME	—	—	AMASK3	AMASK2	AMASK1	AMASK0	ALMRPT7	ALMRPT6	ALMRPT5	ALMRPT4	ALMRPT3	ALMRPT2	ALMRPT1	ALMRPT0	0000
RTCCON2L	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0	—	—	—	PWCPS1	PWCPS0	PS1	PS0	—	—	CLKSEL1	CLKSEL0	8000
RTCCON2H	RTCC Coarse Clock Divider (DIV<15:0>)																3FFF
RTCCON3L	PWCSAMP7	PWCSAMP6	PWCSAMP5	PWCSAMP4	PWCSAMP3	PWCSAMP2	PWCSAMP1	PWCSAMP0	PWCSTAB7	PWCSTAB6	PWCSTAB5	PWCSATB4	PWCSTAB3	PWCSTB2	PWCSTAB1	PWCSTAB0	0000
RTCSTATL	—	—	—	—	—	—	—	—	CPLK	—	ALMEVT	TSBEVT	TSAEVT	SYNC	ALMSYNC	HALFSEC	0000
RTCSTATH	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
TIMEL	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	—	—	—	—	—	—	—	—	0000
TIMEH	—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	0000
DATEL	—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0	—	—	—	—	—	WDAY2	WDAY1	WDAY0	0106
DATEH	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0	—	—	—	MTHTEN	MTHONE3	MTHONE2	MTHONE1	MTHONE0	0001
ALMTIMEL	—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0	—	—	—	—	—	—	—	—	0000
ALMTIMEH	—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0	0000
ALMDATEL	—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0	—	—	—	—	—	WDAY2	WDAY1	WDAY0	0106
ALMDATEH	YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0	—	—	—	MTHTEN	MTHONE3	MTHONE2	MTHONE1	MTHONE0	0001
TSATIMEL	Timestamp A Time Register Low (TSATIMEL<15:0>)																0000
TSATIMEH	Timestamp A Time Register High (TSATIMEH<15:0>)																0000
TSADATEL	Timestamp A Date Register Low (TSADATEL<15:0>)																0000
TSADATEH	Timestamp A Date Register High (TSADATEH<15:0>)																0000
TSBTIMEL	Timestamp B Time Register Low (TSBTIMEL<15:0>)																0000
TSBTIMEH	Timestamp B Time Register High (TSBTIMEH<15:0>)																0000
TSBDATEL	Timestamp B Date Register Low (TSBDATEL<15:0>)																0000
TSBDATEH	Timestamp B Date Register High (TSBDATEH<15:0>)																0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## 12.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33 or PIC24 device families, but the concepts are pertinent and could be used with modification and possible limitations.

The current application notes related to the RTCC with Timestamp module are:

Title	Application Note #
No related application notes at this time.	

# dsPIC33/PIC24 Family Reference Manual

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## 13.0 REVISION HISTORY

### Revision A (October 2014)

This is the initial released revision of this document.

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**Note the following details of the code protection feature on Microchip devices:**

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