RF CMOS Comes of Age

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***Abstract*—All-CMOS radio transceivers and systems-on-a-chip are rapidly making inroads into a wireless market that for years was dominated by bipolar and BiCMOS solutions. It is not a matter of replacing bipolar transistors in known circuit topologies with FETs; the wave of RF CMOS brings with it new architectures and unprecedented levels of integration. What are its origins? What is the commercial impact? How will RF CMOS evolve in the future? This paper offers a retrospective and a perspective.**

I. Introduction

RADIO-FREQUENCY (RF) integrated circuits in CMOS are developing a strong presence in the commercial world. For applications such as wireless LAN and Bluetooth, they are dominant, and in areas such as GSM cellular transceivers and GPS receivers, they are making inroads. This paper offers a brief retrospective on how RF circuits and systems in CMOS have evolved to their current state of the art, followed by a perspective of what the future might hold for RF systems-on-a-chip in CMOS. It seems appropriate today, roughly ten years after the first publications reporting RF circuits in CMOS, to document the key developments and first reports of the circuit techniques and architectural innovations that are today in widespread use. There are many more publications in this area than the selected list of references at the end of the paper may suggest, and in most cases the first reports listed here were often followed by more detailed journal publications by the same authors.

II. The Beginnings

In a few instances, universities justifiably take credit for conceiving some important techniques used in microelectronics. Chief among them must be the switched-capacitor concept and the accompanying CMOS analog circuits developed in the mid-1970s, which gave rise to mixed-signal microelectronics as we know it today. Another is the use of CMOS for RF, which also sprang out of university research in the mid-1990s.

The first phase of RF-CMOS research consisted mainly of the discovery of MOS-appropriate circuit techniques for various standalone circuit building blocks. This was followed by their refinement and final assembly into prototype wireless receivers and transmitters. Meanwhile in industry, then busily engaged in a race to grab a share of the expanding market for cellular handsets, seasoned practitioners, many with microwave training, were busy developing products in the way they knew best: by combining silicon bipolar and even GaAs ICs, at small scales of integration, with many discrete elements, such as filters, resonators, striplines, and so on, to assemble radios on boards. Tried and true radio architectures mitigated risk in meeting the demanding specifications of cellular handsets. Pressures of short time to market left little room for high-risk innovation.

Exempt from these pressures, universities could experiment relatively freely. Research into RF CMOS was prompted by the bold assumption that in the not-too-distant future, radios would come to resemble the complex mixed-signal CMOS ICs such as wireline modems that had revolutionized baseband communications. Agencies such as DARPA and some far-sighted companies accepted this vision as sufficiently futuristic to fund good-sized groups of students.

It was interesting to witness in those early days the unavoidable clash between the seasoned radio designers in industry steeped in discrete bipolar circuits, five-transistor MMICs, transmission lines, Smith Charts, discrete filters, and the heterodyne receiver, and the free-wheeling university types charged with schemes for on-chip image rejection, integrated spiral inductors, monolithic low-noise amplifiers and oscillators in CMOS, and single-chip direct conversion receivers [1], often designed in a style drawn from low-frequency circuits but operating at 1 or 2 GHz. Many good things would emerge from this heady brew and influence the design of commercial radio ICs.

III. University Research

A. Circuits and Devices

The first reported CMOS RF amplifier was hidden in a publication on a method to fabricate an integrated spiral inductor [2]. This is because the only way to obtain gain at 900 MHz in the then-current 2-μm-long CMOS technology was by inductively tuning the transistor capacitance, in effect transforming the intrinsic low-pass frequency response to bandpass. However, to do so at a moderate current required a rather large inductance, which, furthermore, had to be constructed on-chip to avoid the large parasitic capacitance of pads, package, and board traces entailed with an off-chip inductor. Conventional wisdom held that a large spiral is incompatible with the heavily doped silicon substrate. Textbooks from the 1960s and 1970s on IC design contained grim warnings such as: "Inductors with practical values of inductance and Q are by far the most difficult components to fabricate by integrated circuit techniques ... it seems likely that any necessary inductance will be placed external to the monolithic circuit" [3] and "It is almost impossible to fabricate inductors of any reasonable value of inductance in integrated circuits ... as the size of the spiral increases, so does the resistance of the metal pattern. The silicon wafer also contributes eddy current losses ... if it is at all possible, one avoids the use of inductors" [4].

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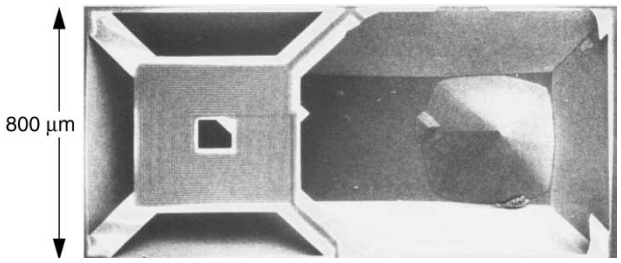


Fig. 1. A suspended spiral inductor of about 100 nH on a heavily doped CMOS substrate. This element enabled the first RF CMOS circuits at 900 MHz.

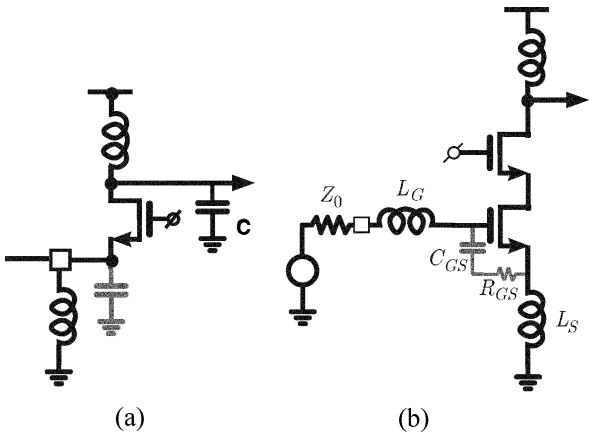


Fig. 2. Low-noise amplifier styles commonly used in CMOS. (a) Common-gate circuit, robust against parasitics, moderate noise figure. (b) Common-source circuit, lowest noise figure.

One of the main differentiating claims of GaAs IC technology (indeed, later to become its main differentiating claim) was that high quality monolithic inductors can be built on a semi-insulating substrate. The paper [2] showed that by removing the heavily doped CMOS substrate under a spiral with a wet selective etch, the self-capacitance of a 100-nH spiral and the associated eddy current losses fall to almost zero (Fig. 1). Thus, a 2-μm CMOS differential pair using two of these inductors as loads could deliver a tuned gain of 20 dB at the then extremely high frequency of 900 MHz.

Refinements in the design of matched impedance, low-noise tuned amplifiers would soon follow (Fig. 2) [5], [6]. The common-gate low-noise amplifier proved to be an easy one to use, giving robust input impedance match to 50 Ω across a relatively wide band of frequencies; however, its noise figure was limited to 2.2 dB. For lower noise, which would be ultimately limited by fundamental losses such as inversion layer resistance, the common-source amplifier with inductor degeneration was better suited.

The suspended inductor would only be used for a short while longer as better inductors became available through improved layout techniques [7], such as the differential spiral [8], and by the appearance of a new generation of CMOS substrates (as described later). However, the use of MEMs techniques in suspending the inductor to solve an RF circuit problem would trigger work by others that would develop into a subfield all of its own: RF-MEMs [9].

Next, let us turn to the mixer, a circuit that is central to wireless devices. In the world of bipolar circuits, the double-balanced current-commutating mixer reigned as king. Although the passive mixers based on FETs as analog switches was natural to CMOS [10], the first CMOS mixer operating at RF [11] was based on a classic CMOS switched-capacitor bottom-plate sampling track-and-hold circuit (Fig. 3). In track mode, the broadband passive *RC* circuit comprising a FET switch and capacitor can follow a modulated carrier voltage waveform at 900 MHz, and by clocking the tracking capacitor into hold mode at a rate of at least the twice the *modulation* bandwidth, the discrete-time analog output represents the desired channel and the other preselected channels surrounding it downconverted to a low frequency. As this modulation bandwidth is a small fraction of the desired channel's carrier frequency, the operational amplifier (opamp) is clocked at a modest rate of only a few to tens of megahertz. The downconversion action can be understood in terms of aliasing. Subsampling a signal at a rate lower than Nyquist results in aliasing, and the aliased spectrum closest to dc contains the sampled channels downconverted to dc. The theory underpinning the sampling of bandpass waveforms had been set out a few years prior [12]. It was noted that a wideband tracking circuit will also follow white noise generated by circuits after the preselect filter occupying the band from dc to the track-mode cutoff frequency, and that after aliasing the mean-square power in the wideband noise would accumulate into the subsampled Nyquist band. This raises the spectral density of noise accompanying the downconverted signal, penalizing mixer noise figure. For these reasons this approach would be soon replaced by a CMOS version of the bipolar current-commutating mixer which does not alias input noise. Meanwhile, the idea of mixing by subsampling would live on in bandpass delta-sigma A/D converters (ADCs) for IF signal processing [13]. Also, it will appear once again at the end of this paper, this time as part of a more sensible anti-aliasing arrangement.

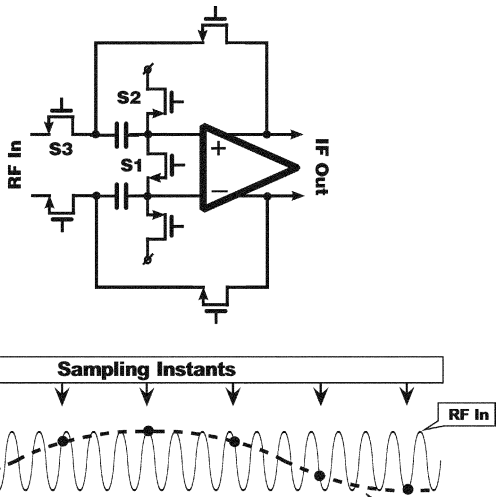


Fig. 3. CMOS sample-and-hold circuit which acts as a downconversion mixer by subsampling the modulated RF waveform at its input.

Inspired by prevailing practice in mixed-signal integrated circuits, RF-CMOS circuits almost always used differential topologies to reject as common-mode the noise digital circuits would generate when eventually they would inhabit the same substrate as the radio (this would not happen for several years). A differential *LC* oscillator circuit was therefore a

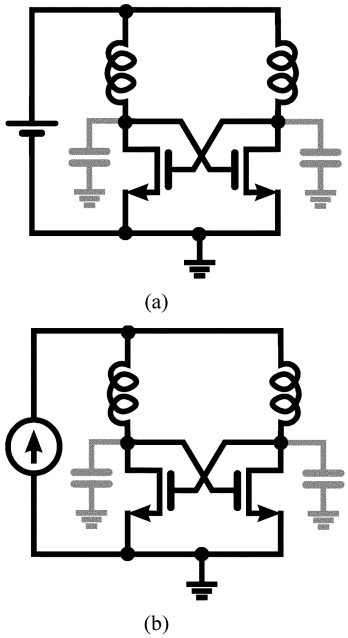


Fig. 4. Two styles of CMOS differential *LC* oscillator: (a) constant voltage biased and (b) constant current biased.

natural choice (Fig. 4); the first implementation was tuned with bondwire inductors [14], the next with on-chip spirals [15]. The phase noise of early integrated CMOS voltage-controlled oscillators (VCOs) was not very impressive when compared with the then-dominant discrete transistor oscillators using high-Q off-chip resonators. CMOS oscillators also suffer from upconversion of their large flicker noise into phase noise sidebands, whose spectral density at small frequency offsets (typically less than 100 kHz) from the carrier frequency rises at a rate higher by 10 dB/decade. This was reason enough at first for CMOS oscillators to be much maligned, although in truth upconverted flicker noise seldom handicapped the local oscillator (LO) in digital cellular handsets such as GSM; usually it was more difficult to meet specifications on far-away phase noise, which was limited by ever-present white noise and low quality factor of the resonator. CMOS researchers, intent on integrating the resonator on the oscillator circuit, started to investigate the various losses associated with on-chip spiral inductors which limit resonator Q. It was apparent that spirals realized with customary aluminum metallization, which is usually thinner than 1 μm to enable planarization of middle layers of interconnect, introduces too large a series resistance. To lower this loss, foundries were persuaded to make available a thick metal film at the uppermost layer of the metal stack, where planarization is not required. Inductors also suffer from eddy current losses in the substrate. In heavily doped substrates at high frequencies, this loss can easily overtake the loss due to series resistance. Traditionally, CMOS substrates were doped heavily to avoid latchup, but with the realization that substrate loss can seriously handicap inductor Q [16], a new generation of RF-friendly lightly doped CMOS substrates became available, with surprisingly little added risk of latchup. As power dissipated by eddy currents varies as V^2/R, this loss is lower in high resistivity substrates, but now power

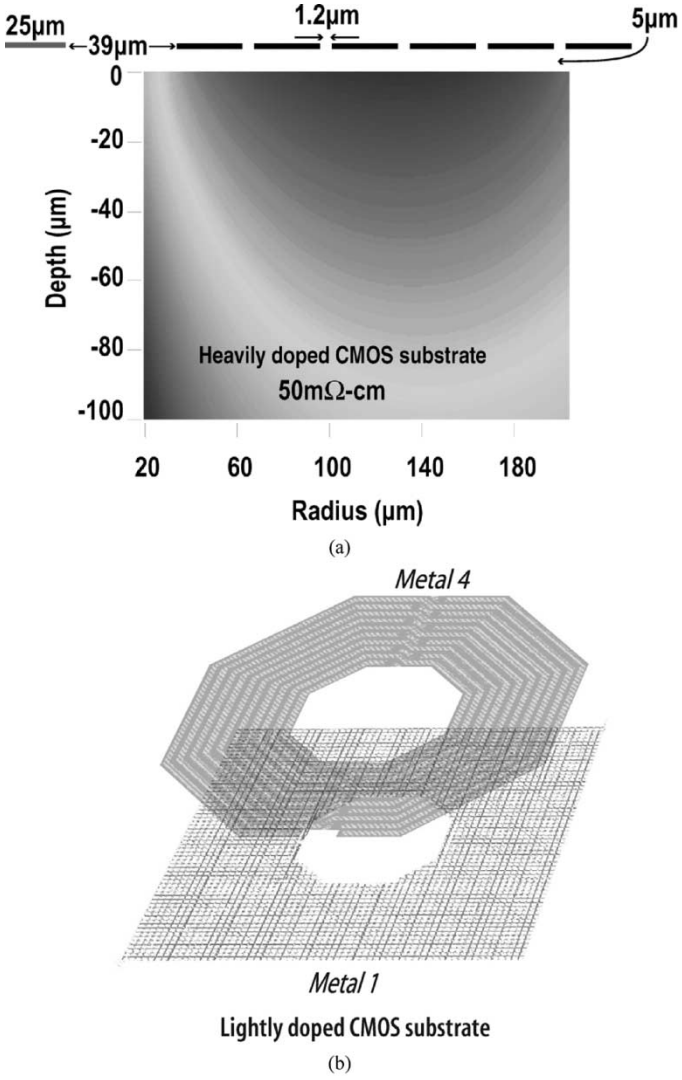


Fig. 5. Losses associated with spiral inductors on different types of CMOS substrates. (a) Power dissipation in heavily doped substrates caused by eddy currents. (b) Metal 1 segmented shield mitigates loss due to displacement currents in lightly doped substrates.

loss due to displacement currents that is proportional to I^2R poses a greater threat to inductor Q. However, displacement currents can be shielded from the substrate (although there is no practical way compatible with silicon technology to shield magnetic fields from penetrating the substrate). The shield consists of placing a segmented conductive surface connected to ground between the spiral and the substrate, which may be realized in a lower level of metal or in polysilicon (Fig. 5) [17]. Its segmented geometry blocks eddy current loops from flowing in the plane of the shield.

On a parallel front, the push for integrated VCOs to meet cellular specifications prompted progress on the analysis and simulation of oscillator phase noise. Although a search for phase noise mechanisms had drawn much attention over the years, no compact, comprehensive, and credible theory or simulation method had yet emerged that would lead to circuit techniques to lower phase noise. Three important developments would breathe new life into this well-worn topic: an impulse-response-based numerical strategy for the prediction of phase

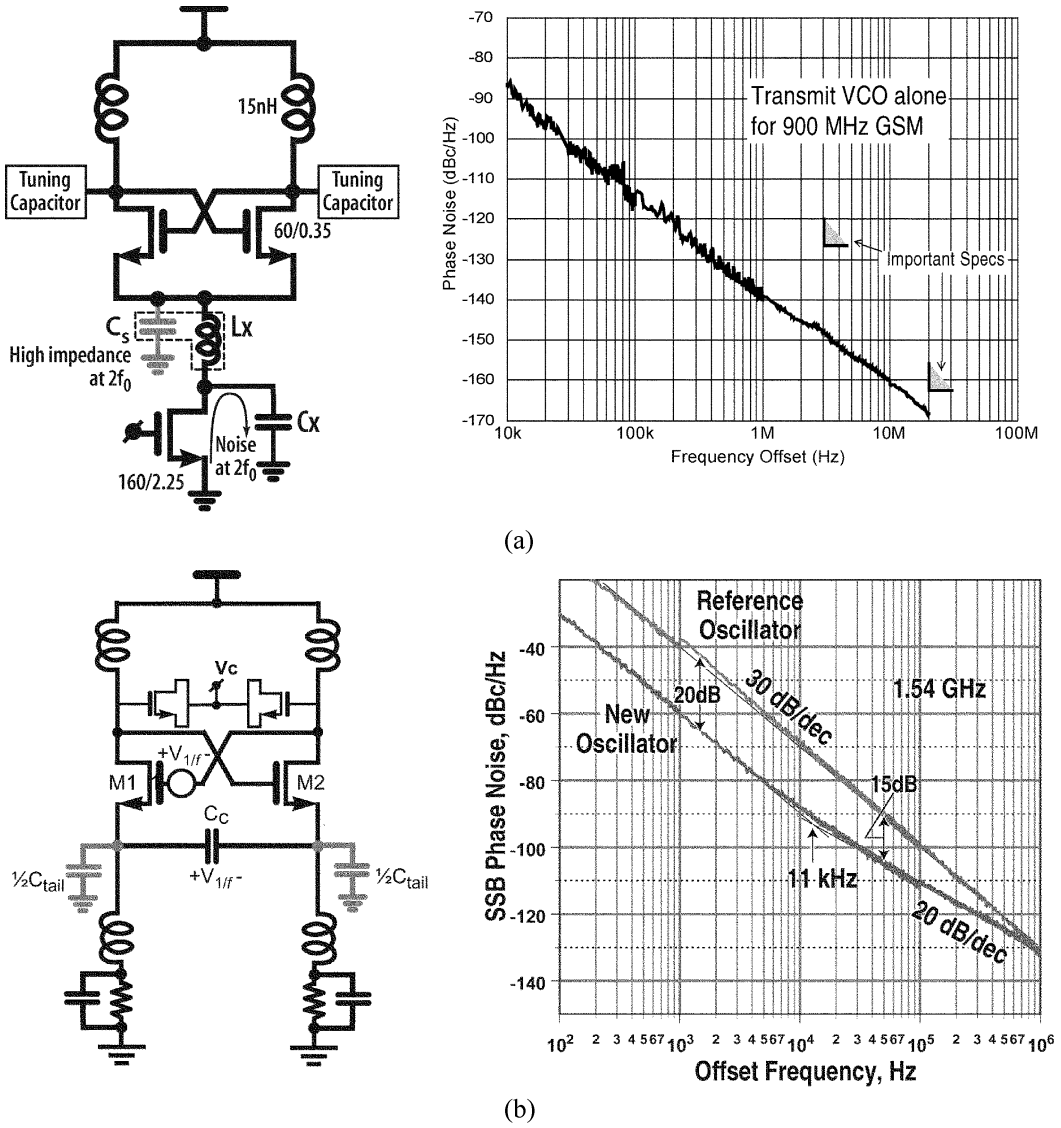


Fig. 6. Circuit techniques that lower VCO phase noise. (a) Filtering of tail current white noise at the second harmonic essentially eliminates that contribution to phase noise. Prototype circuit satisfies phase noise for GSM TX VCO. (b) Decoupling the sources of the differential pair with a capacitor eliminates the second harmonic of voltage there, suppressing flicker noise upconversion. Prototype circuits satisfies close-in phase noise of PDC receiver.

noise, which offered some qualitative insights [18]; the appearance of the PNOISE SIMULATION function in SPECTRE-RF [19], which allowed for a fast and exact simulation of phase noise in any oscillator; and the pinpointing of the physical mechanisms responsible for phase noise in the differential oscillator [20]. This last has led to circuit techniques that can substantially lower far-away phase noise [21] and reliably suppress the upconversion of flicker noise (Fig. 6) [22]. Combining these circuit techniques with the insights gained into lowering loss in on-chip spiral inductors has finally enabled CMOS oscillators biased at a few milliamperes to meet, on the one hand, the very low phase noise required at 20-MHz offset in GSM transmitters, and on the other hand, the low close-in phase noise at 50-kHz offset in PDC cellular receivers.

Some unique advantages of CMOS oscillators were soon recognized: one is that MOSFETs can sustain oscillation amplitudes of $2V_{\rm DD}$ without forward-biasing a junction or necessarily jeopardizing reliability; the other, that varactors that are themselves MOSFETs [23] can absorb this large amplitude without malfunction. As the oscillator phase noise is inversely proportional to the square of the amplitude, the large oscillation in steady-state compared to the bipolar case largely accounts for why CMOS oscillators are able to do well with on-chip resonators (inductors) of moderate Q. Indeed, this is good enough reason to even sway the committed bipolar circuit designer, who when working in a BiCMOS technology will often opt to use a CMOS circuit for the oscillator.

The MOSFET used as a switch enables another important idea, namely, discrete frequency tuning with switched reactive elements [24], usually capacitors (Fig. 7). This "band switching" technique, as it is now popularly known, has proved to be very useful in extending the frequency tuning range sufficiently to encompass process-induced spreads of as large as $\pm 20\%$ in the on-chip capacitance without compromising phase noise. It is now a standard technique in commercial RF-CMOS ICs.

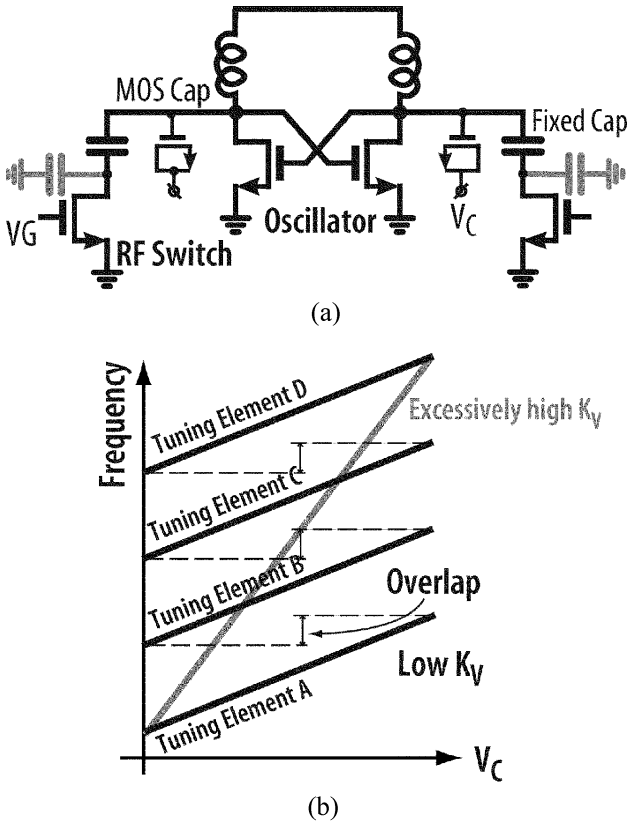


Fig. 7. Adding switch-selectable frequency tuning to a continuously tunable VCO. With a binary weighted array of tuning capacitors, a family of uniformly spaced tuning curves may be obtained to cover a large frequency range, without suffering excessive VCO sensitivity to the analog control voltage.

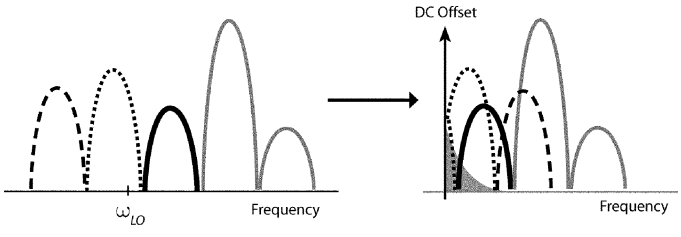


Fig. 8. Principle of low-IF receiver. The desired channel downconverts to a center frequency away from zero, so as to circumvent dc offset and flicker noise. The image is a nearby channel.

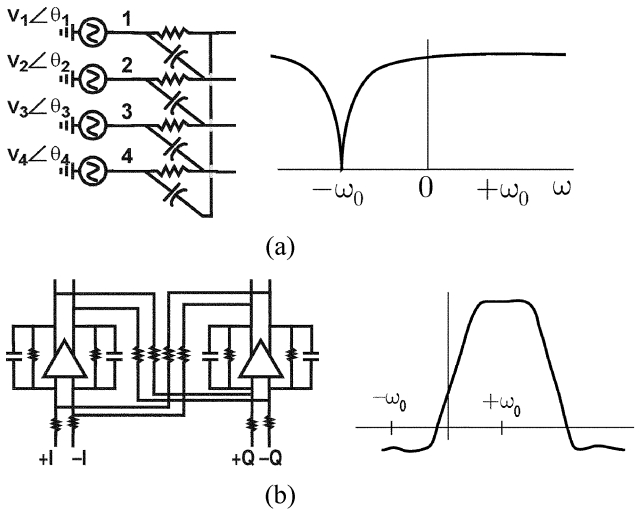


Fig. 9. Analog Hilbert filters to suppress image channels after downconversion mixer. (a) Passive polyphase filter positions a null at center of image channel. (b) Active polyphase filter passes desired channel, and suppresses adjacent and image channels in its stopband.

The wireless receiver uses two types of filter: one to reject the image channel that is an outcome of mixing, and the other to isolate the channel of interest from surrounding unwanted channels. Any active filter used in a wireless receiver must be very linear [25], otherwise intermodulation distortion between large unwanted channels in the stopband can create frequencies that will land in the filter passband. Negative feedback is a powerful way to linearize filter circuits [26], but to lower power consumption the filter poles (that is, its passband) must also lie at low frequencies. This implies that after downconversion the desired channel must lie at a low frequency, that is, at some low or zero intermediate frequency (IF).

B. Receivers, Transmitters, and Transceivers

As an alternative to zero IF, low-IF receivers became of interest because active circuits still consume the least possible power in amplifying and filtering the signal at low frequencies, yet the signal of interest can be situated away in frequency from dc offsets as well as the region of high flicker noise spectral density; but now there is the burden of rejecting an image that lies close in frequency of the desired channel (Fig. 8). Prior to downconversion this would require an RF or other high-frequency filter with such a sharp transition band that the filter is unrealistic; therefore, the only practical option is to suppress the image in a Hilbert filter *after* mixing [27]. This is a type of filter that responds differently to the positive and negative frequencies where the desired signal and image, respectively, will lie after downconversion. The push to receivers with low IF led to the rediscovery of a simple analog Hilbert filter, the passive *RC* polyphase filter [28], which can be easily realized in CMOS with only resistors and capacitors. Better yet, the two functions of suppressing the image and suppressing the adjacent channels can be rolled into one in a complex active channel-select Hilbert filter, which is synthesized with a frequency shifting transform on a low-pass active filter prototype (Fig. 9) [29]. It must be mentioned that the Hilbert filter can be implemented in the digital domain as well if the two quadrature channels are digitized separately.

When, for various practical reasons, a dual downconversion receiver must be used, the Weaver architecture can reject the image at the first IF, followed by a Hilbert filter at the second IF. Although the concept is old, it requires six mixers and became practical only with the high integration possible in CMOS [28], [30], [31].

CMOS implementations of baseband functions open new possibilities of digital functionality that might otherwise be out of the question. The main thrust so far is in replacing on-chip active channel-select filters at low IF or baseband with filtering and automatic gain control (AGC) using digital circuits that consume a small fraction of the area. The channel of interest located at some reasonable IF, assuming that the image has been rejected by some (analog) means, may be directly digitized by a bandpass delta-sigma converter [32], [33]. This approach is

very well suited to the job at hand, because the converter shapes quantization noise so that its spectral density is lowest in the desired channel, but rises in the adjacent channels that will later be filtered out. A sufficiently high oversampling rate guarantees that adjacent channels do not alias on to the desired channel. Depending on the modulation, a signal-to-noise ratio of 6 to 20 dB may be sufficient for demodulation with acceptably low bit-error rate (BER), and the surplus dynamic range afforded by the full-scale to quantization noise ratio after conversion can be used, in effect, for digital AGC. Polyphase Hilbert filter implementations of the delta-sigma converter reject the image internally [34], enabling receivers that translate directly to digital low-IF. The image-reject bandpass sigma-delta ADC is an important step toward digital receivers; the last section of this paper discusses more general prospects for the future.

To a lesser degree than in the receiver, work in CMOS implementations has also influenced the modern transmitter. For linear modulations, the I–Q or Cartesian upconversion transmitter is widespread. Two DACs driven by complex outputs from a digital baseband can synthesize an arbitrary modulation centered at 0 Hz, and two mixers driven by quadrature phases of an LO can upconvert this to the required carrier frequency without creating an image sideband. These functions are all readily integrated. Although the "CMOS philosophy" may drive one toward also integrating a high power amplifier (PA) [35], this is not a good idea for two reasons; power amplifiers in conventional CMOS are seldom as efficient as in boutique technologies optimized for low parasitics and high f_T, and worse yet, on-chip parasitic coupling can cause the high power modulated output of the PA to pull the frequency of the unmodulated on-chip oscillator, with devastating consequences. At least in the foreseeable future, RF systems-on-a-chip will work best when the high power amplifier is off the chip, although PAs with modest output powers have been shown to coexist reasonably.

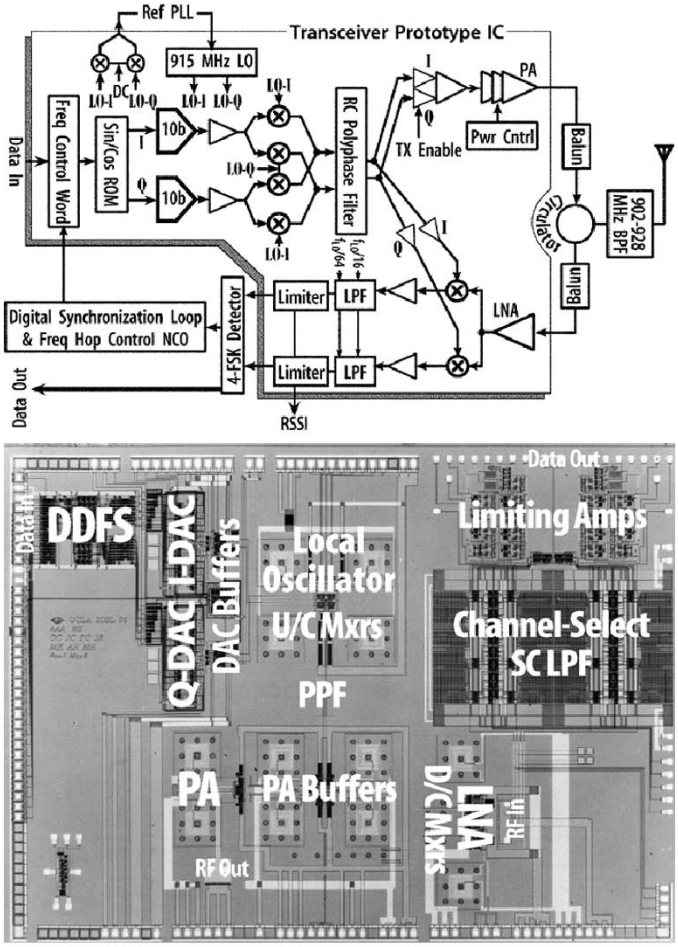


Fig. 10. First fully integrated RF-CMOS transceiver, designed for FHSS data communications in the 900-MHz ISM band. This showed the feasibility of sensitive receiver circuits sharing the same substrate as high-speed logic (the direct digital frequency synthesizer).

In Cartesian transmitters for constant envelope waveforms such as in GSM, gain imbalance or quadrature phase error in the upconverter induces parasitic amplitude modulation. After suffering nonlinearity in the saturated PA, this unintended AM creates intermodulation distortion that will violates adjacent channels. The easiest way to lower this effect in a given PA is to back off its bias from saturation. This improves linearity but worsens efficiency. This problem can be largely avoided by driving a saturated PA with the phase-modulated output of a VCO which is guaranteed to be constant envelope. A pure phase-modulating transmitter may be realized by embedding the VCO in an offset phase-locked loop (PLL) [36], where a conventional I–Q Cartesian upconverter first creates an approximately constant envelope waveform at some IF, and then a PLL with a mixer in feedback translates this to RF; the phase-modulated RF VCO in the loop then drives the nonlinear PA. This transmitter needs three mixers and two local oscillators. Another approach which does away with the mixers and needs only one VCO is a digital-to-phase/frequency converter: a high-resolution fractional-N PLL where a sigma-delta noise-shaping quantizer controls the instantaneous divide modulus to lower the spurious tones associated with time-varying division [37]. The modulation is applied as a stream of digital words to the quantizer input, and controls the instantaneous VCO phase. The constant envelope phase modulated waveform suffers none of the adverse effects associated with the nonlinear power amplifier, and yet benefits from its high efficiency. With determined effort the only remaining analog components, the phase detector and loop filter (aside from the VCO, which in some ways is only a generator of zero crossings), can also be done away with and replaced by digital phase estimation and frequency control [38].

For high bandwidth efficiency, the new generation of cellular and WLAN systems use modulations with strongly varying envelopes such as quadrature amplitude modulation (QAM) and multilevel phase shift keying (PSK). Some promising ways are now being explored to transmit these waveforms using high-efficiency saturated power amplifiers. One such method is polar modulation, where the baseband modulated signal is separated into AM and PM components. The closed-loop wideband digital-to-phase modulator described above controls the VCO, and baseband AM, which determines the envelope of the modulated RF, controls either the supply voltage of the nonlinear PA through a dc–dc converter or its power control terminal. The main challenge is in making sure that the phase and amplitude modulations, which travel in two completely different signal flow paths, arrive at the PA simultaneously to reconstruct the desired waveform without distortion. Tropian has in-

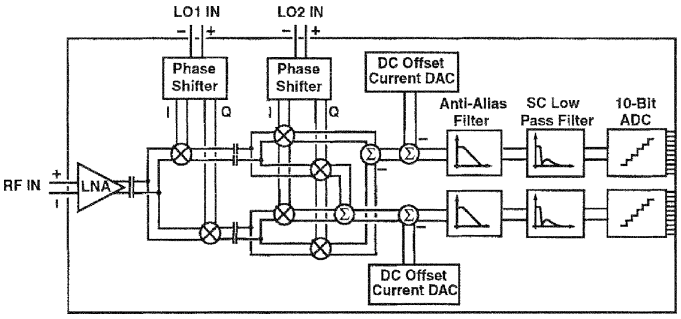


Fig. 11. Receiver for cordless applications with dual conversion Weaver broadband image-reject architecture. Image rejected in digital baseband.

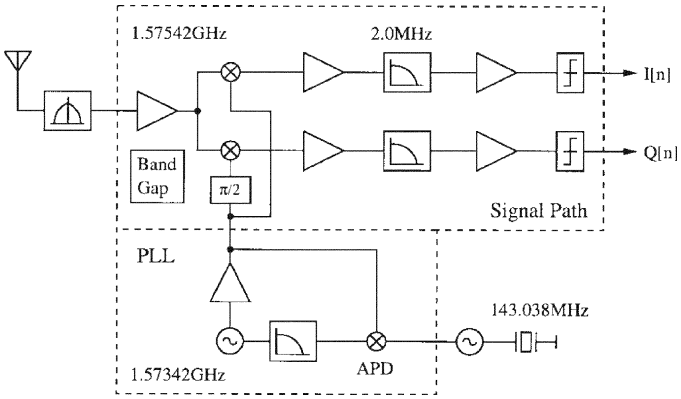


Fig. 12. GPS receiver with single conversion to 2-MHz low IF. Image is rejected in later baseband sections.

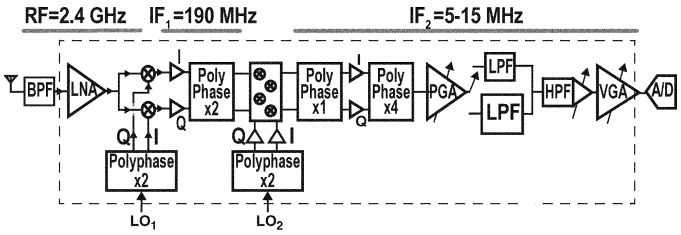


Fig. 13. Dual conversion Weaver image-reject receiver for wideband wireless LAN. All image rejection on-chip with analog circuits.

troduced such a polar modulator for EDGE signaling in GSM channels [39]. The phase modulator is implemented in CMOS, as is the switching power supply controller. Extensive calibration is used to equalize the delays between these two paths. Another promising method is to decompose envelope modulation into the sum of two constant envelope waveforms, amplify them separately in efficient nonlinear power amplifiers, and combine them at the output [40], [41]. Hampered in the past by the difficulty of decomposition in real time, with fast DSP this is becoming more practical as in the power amplifier offerings by IceFyre. Losses in power combining remain a problem.

The amplifiers, mixers, and oscillators described thus far were used to realize a single-chip transceiver (Fig. 10) [42] based on a 1-μm CMOS direct-conversion receiver for frequency-hopped spread-spectrum communication in the 900-MHz ISM band. This prototype system would evolve into later standards-driven WLAN systems. They were also put to

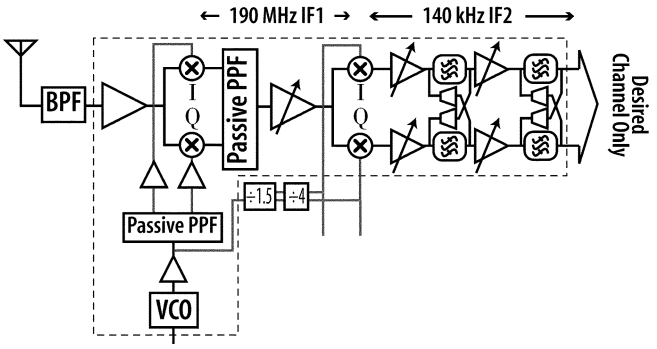


Fig. 14. Dual conversion to low-IF receiver for 900-MHz GSM with on-chip image rejection.

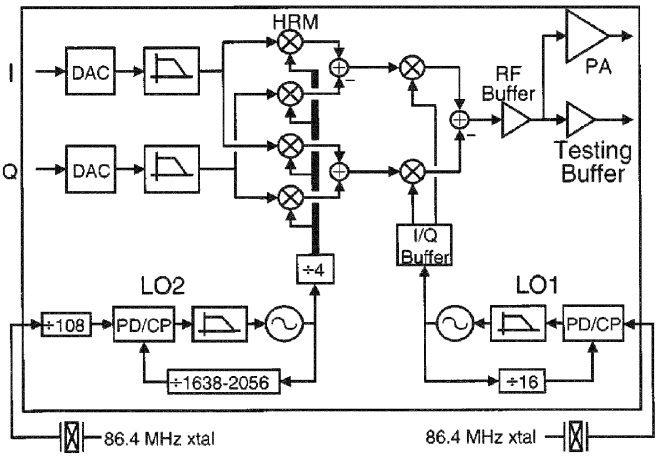


Fig. 15. DCS-1800 transmitter with dual Cartesian upconversion using harmonic-reject mixers to suppress spurious outputs. On-chip high power amplifier.

use in a 1.8-GHz integrated receiver for cordless telephony using the broadband image-reject Weaver architecture to zero IF (Fig. 11) [30], a 0.5-μm CMOS GPS receiver tuned to 1.5 GHz based on single conversion to a low IF of 2 MHz (Fig. 12) [43], a 0.6-μm CMOS implementation of a QAM receiver operating in the 2.4 GHz ISM band for high-data-rate WLAN (Fig. 13) [44], and a 0.35-μm CMOS receiver for 900 MHz GSM based on dual conversion to a low IF of 120 kHz (Fig. 14) [45]. Dual conversion would prove to be an important principle to lower the effect of flicker noise in CMOS mixers when the signal of interest lies at low IF. Other all-CMOS integrated wireless devices include a GSM transceiver that bases an unusual frequency plan around high-quality off-chip filters and inductors [46], an approach that runs counter to the CMOS philosophy of high levels of integration but results in impressive performance at low power. Many interesting variants are possible when the IF is fully customized by rejecting the image on-chip, such as a dual-band receiver that centers the first LO between bands and then selects either the upper or the lower sideband after second downconversion to zero IF [47]. A single conversion to low-IF all-CMOS transceiver for 1.8-GHz DCS (GSM-like) has been described [48], as well as a dual conversion to zero IF receiver tuned to 5 GHz that uses injection-locked frequency dividers in the frequency synthesizer to operate at this high frequency [49].

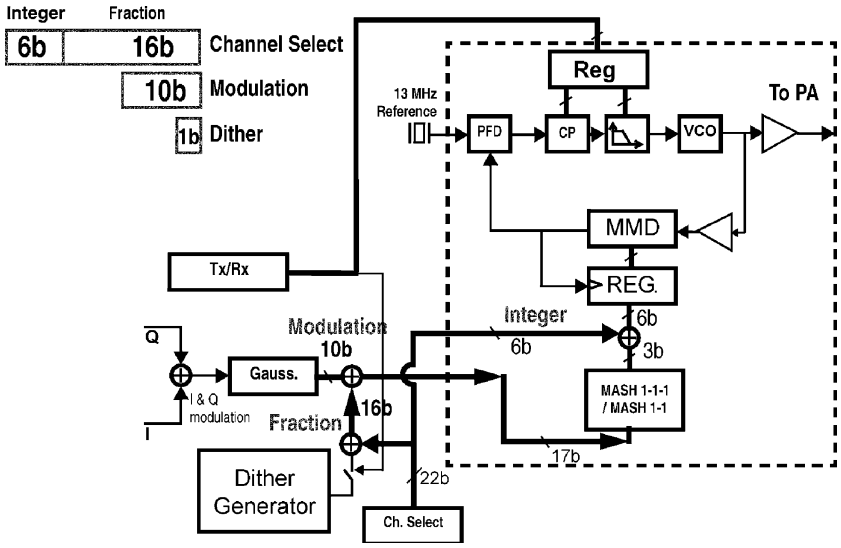


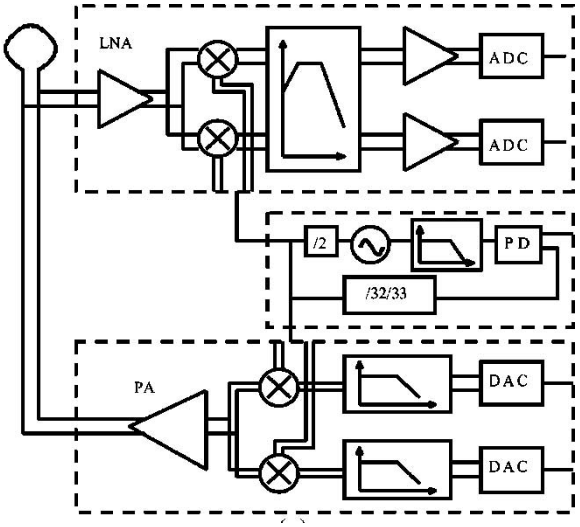
Fig. 16. Fractional-N PLL-based 900-MHz GSM modulator and frequency synthesizer with constant-envelope output.

Important CMOS transmitters described so far include a Cartesian transmitter for 1.8-GHz DCS (Fig. 15) [50] and a 0.35-μm CMOS transmitter for GSM in the 900-MHz band, based on delta-sigma fractional-N frequency synthesizer which exploits the constant envelope nature of GSM modulation (Fig. 16) [51].

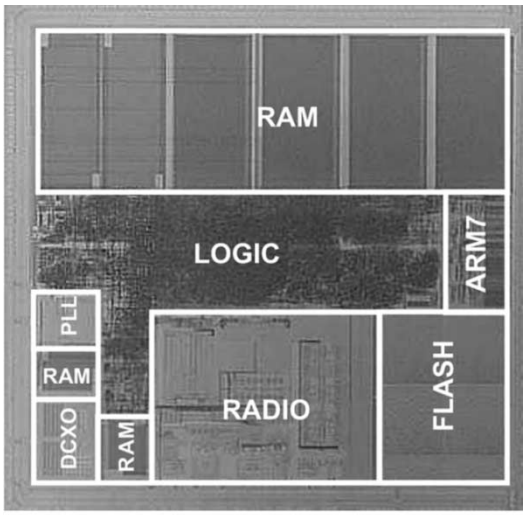
Notwithstanding the considerable efforts of university researchers in the developments described so far, these RF ICs served only as proof of concept. However, they would pave the way for a new generation of commercial products.

IV. Commercialization

Bipolar RF ICs dominated in cellular mobile handsets for many years, because there was little incentive, and mainly risk, in switching to CMOS. The spur for commercialization of CMOS wireless transceivers came with new markets for Bluetooth and the IEEE 802.11 WLANs, whose economics were entirely different than those of cellular handsets. No longer would service providers subsidize the electronics; the cost of WLAN chipsets would determine the street price of WLAN PC cards and plug-ins, and therefore the lower the price the better. With this commoditization came the familiar pressures for high levels of integration, smaller bills of material (BOM), and to as much a degree as possible, the elimination of off-chip discrete components that add to assembly and test costs. The trend was clear: these radios must be CMOS systems-on-a-chip (SOC). It also helped that the radio specifications of some of these standards were relatively relaxed. Indeed, because circuit designers had participated in the definition process, this was the first generation of wireless systems that could be called "silicon-friendly." For instance, the Bluetooth system [52] specifies a receiver with modest in-band image suppression, a relatively large permitted noise figure, and moderate linearity, which more or less spells out implementation as a fully integrated low-IF receiver. Ironically, it is the complex baseband DSP responsible for protocol processing and modulation/demodulation that costs twice as much [53].



(a)



(b)

Fig. 17. First CMOS mixed RF-analog-digital wireless system on a chip, a Bluetooth transceiver from Alcatel. The radio block diagram shows a low-IF receiver and a Cartesian transmitter.

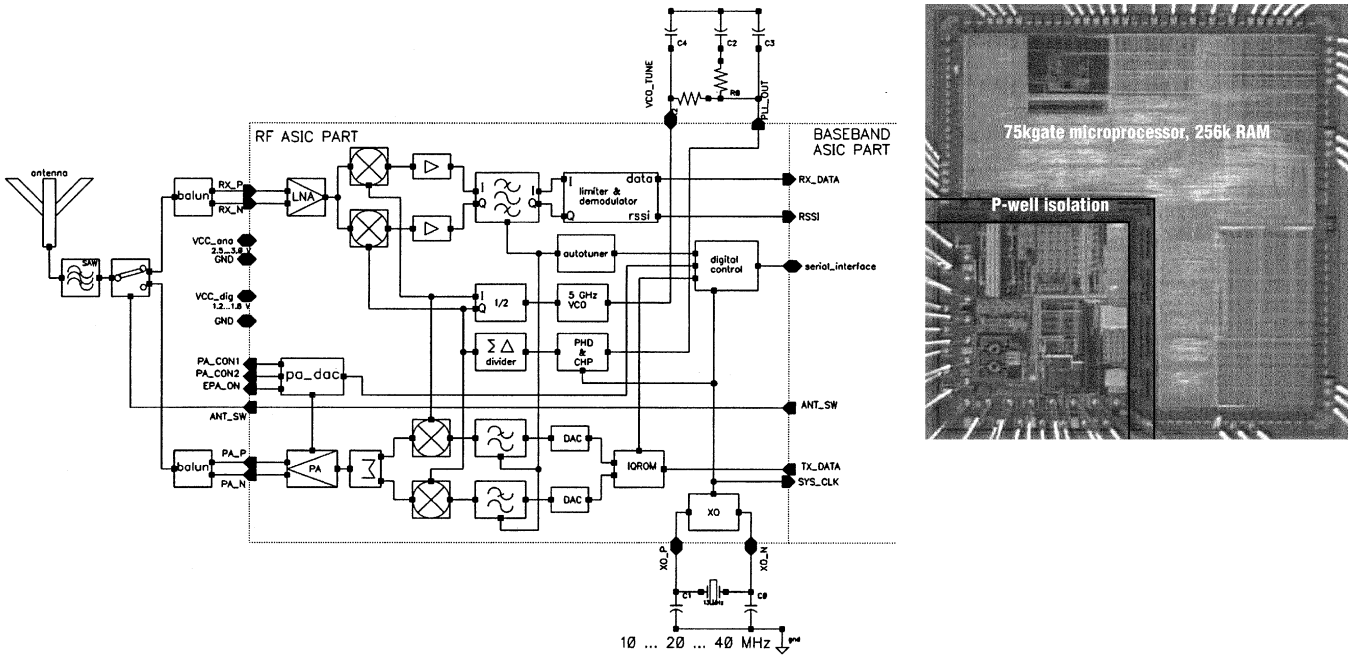


Fig. 18. Bluetooth transceiver from Ericsson. The receiver uses a low-IF with analog Hilbert filter, and is complemented with a Cartesian transmitter. A large p-well on the transceiver chip isolates the radio from the microprocessor and memory.

The first wave of commercial 2.4-GHz CMOS Bluetooth radio transceivers were announced at ISSCC 2001. The Alcatel Bluetooth transceiver [54] was the first to integrate on the same substrate as the radio significant digital functions, namely a baseband processor, an ARM processor, flash memory, and RAM (Fig. 17). This heralded a new generation of wireless SOCs. The receiver was based on a 1-MHz low-IF using an analog complex channel-select filter for post-mixer image rejection. The Broadcom Bluetooth transceiver [55] used a 2-MHz IF. The local oscillator on both transceivers is fully integrated, and the transmitter is based on Cartesian upconversion. On-chip CMOS PAs deliver a nominal output power of 1 mW, and if this is insufficient for communication they can serve as preamplifiers to drive an off-chip high PA. At the ISSCC 2002, Ericsson presented its all-CMOS Bluetooth transceiver, also using a 2-MHz IF, Hilbert-type channel-select filter, and Cartesian transmitter [56]. This chip integrates a 75 Kgate microprocessor and 256 kb RAM. There are two notable items of interest in this chip (Fig. 18). First, to lower the active chip area of the radio portion, there is only one on-chip inductor which is used in the local oscillator. The amplifiers in the RF front-end are wideband, with resistor loads. Second, the prominent p-well grounded guard ring separating the digital circuits from the sensitive analog radio clearly plays a key role in isolating substrate crosstalk from the former to the latter. At the ISSCC 2003, Toshiba presented a similar Bluetooth SOC.

National Semiconductor has developed an all-CMOS 1.9-GHz transceiver for DECT (Digital European Cordless Telephony) in 0.25-μm CMOS [57]. As DECT is in many ways a precursor to Bluetooth, it is not surprising that this should follow close on the commercial RF-CMOS Bluetooth transceivers. The receiver downconverts the 1.2-MHz-wide DECT channel to 864-kHz IF for FM demodulation; on the transmit side, data modulates the VCO in open-loop mode, aided by a calibration scheme that uses variable varactor bias and switchable capacitors.

Other commodity radios have also converged on all-CMOS solutions. To serve the growing market for GPS-aided positioning, Valence Semiconductor developed an all-CMOS GPS receiver that uses a low IF of 1 MHz [58], where the image falls within the extended GPS band, and requires only modest suppression by a complex channel-select filter. Sony has presented a slightly different low-IF receiver SOC, which integrates the baseband processor on the same substrate in 0.18-μm CMOS [59]. The receiver for GPS must be considerably more sensitive than for Bluetooth, so accurate modeling of crosstalk between the large logic blocks and the radio section through the common substrate is paramount. The new generation of substrate modeling CAD tools plays an important role in the development of such an SOC, and in this case has led to the strategic placement of two guard rings surrounding the RF and IF stages of the sensitive receiver front-end.

Next, let us turn to wireless LAN. The new generation of radio transceivers is almost exclusively in CMOS. There are good reasons why this is so. The large bandwidth of each received channel makes it relatively simple to use a direct conversion receiver, because an analog or digital notch filter at dc can suppress offset and flicker noise with little adverse effect on demodulation resulting from the sacrifice of a small percentage of the useful signal spectrum [53]. The requirements on linearity and LO phase noise are also relaxed compared to cellular receivers. Single-chip transceivers have been presented for IEEE 802.11b WLAN in the 2.4-GHz ISM band [60] and IEEE 802.11a WLAN in the 5-GHz NII band [61], [62], some capable of dual-mode operation. So far, the baseband chip is separate in all cases. These publications also show that today's

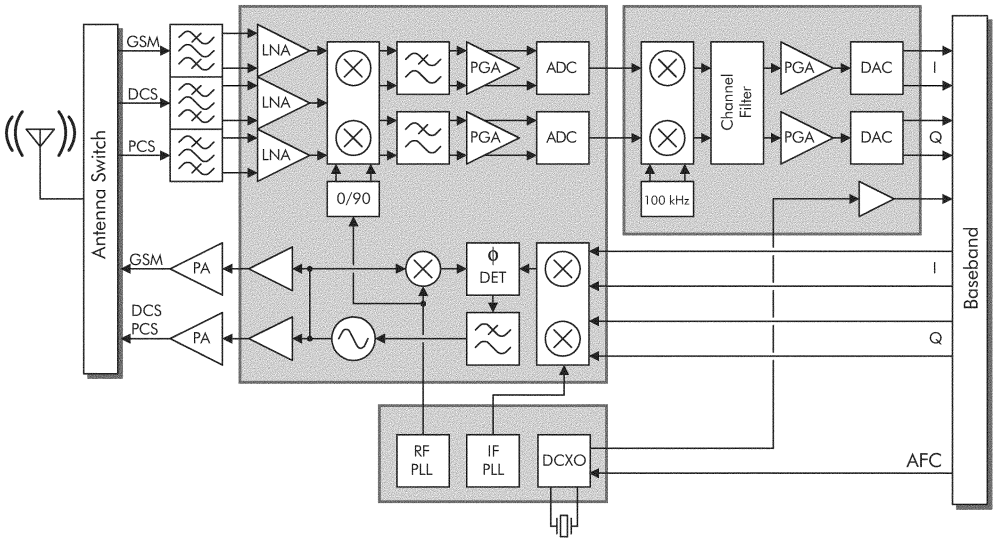


Fig. 19. CMOS GSM multimode transceiver chipset from Silicon Labs. The low-IF receiver digitizes the downconverted signal for digital filtering, then reconverts to a standard analog interface for use with various baseband processors. The transmitter is an offset PLL. The frequency synthesizer is on a separate chip to avoid crosstalk from the digital circuits.

widely available 0.18-μm CMOS is sufficient to give production-quality 5-GHz radios. Once again, these new standards require a simpler analog radio than in cellular applications, but the digital baseband becomes more complex.

By far the most successful RF-CMOS commercial product to date is Silicon Labs' GSM transceiver chipset. The transmitter, like all other contemporary ones for GSM, uses an offset-PLL phase modulator. However, bucking the trend toward direct-conversion receivers in bipolar IC implementations, the CMOS receiver uses a low IF of 100 kHz, where the image is the adjacent channel which, in the worst case, need only be rejected by about 30 dB. The large dc offset and flicker noise associated with CMOS does not encroach on the narrow 200-kHz-wide GSM channel of interest. Exploiting CMOS mixed-signal capability, after downconversion and coarse analog filtering the channel of interest and adjacent channels are digitized with high resolution at this low IF, mixed to zero IF in the digital domain whereupon a high-order and programmable digital FIR filter isolates the channel of interest. To interface with legacy third-party baseband chips that require quadrature analog inputs, the wanted channel is converted back to analog at the output pins. The complete transceiver is divided into three separate chips: the analog transceiver, the digital baseband receive filter, and the frequency synthesizer which integrates the VCO and its resonator (Fig. 19). This partitioning isolates the sensitive frequency synthesizer from noise generated in the digital circuits. For the first time, a commercial solution to the demanding needs of cellular telephony uses ideas that so far had only been explored by university researchers: low IF, which in the case of GSM was shown to offer clear advantages over zero IF in the analog sections [27], [63], and high levels of integration which fully exploit the on-chip digitally activated correction enabled by analog switches in CMOS. Lingering doubts about the fitness of CMOS radios for mass production because they might suffer from large process spreads and marginal RF performance were put to rest when it is realized that by mid-2003, 30 million of these transceivers had been inserted into GSM cell phones.

V. The Future

So far, this paper has described the evolution and subsequent commercialization of CMOS radios-on-a-chip founded on what may be termed classic analog techniques; that is, circuit topologies and transceiver architectures whose lineage is traceable to radio electronics dating back to vacuum tubes. Now we must ask: What of the future?

In particular, will this approach to circuit and transceiver design survive as CMOS technology scales down? While the higher transistor f_T will certainly be welcome, the lower supply voltage poses serious problems. For one, it will impair any RF or baseband analog circuit's ability to handle large unwanted signals, and for another, in the local oscillator the lower steady-state amplitude will worsen phase noise quadratically. Today these problems are deferred by realizing critical analog circuits with thick-oxide FETs, which are, in effect, devices belonging to an older generation. However, in the future these thick-oxide FETs will themselves scale down, until they can no longer sustain the constant signal dynamic range that the application requires. It is fair to say that in CMOS at channel lengths of 90 nm or less, analog circuits will no longer be able to handle waveforms with large dynamic range without a disproportionate rise in power consumption, at which point it is wiser to spend the available power budget on an ADC with adequate dynamic range and bandwidth, and process the waveforms from then onwards in a dense digital signal flow with adequate wordlength.

This means that the received waveform should be digitized as early on as possible. In the limit, this would mean an ADC at the antenna with sufficiently high conversion rate and dynamic range to capture the weak desired signal and all the strong unwanted signals passing the antenna preselect filter. A literal im-

plementation requires a heroic ADC sampling and digitizing at rates exceeding twice the highest RF of interest [64], which is well out of reach in the next several years. A more careful look at the problem shows that this literal interpretation is grossly excessive for the problem at hand, because it requires the digitizing an array of channels of wildly varying strengths when we are only interested in one, very likely weak, bandpass channel. We are constrained in our thinking by our experience with single-channel baseband receivers, where a low-pass antialias filter blocks out-of-band signals and noise, requiring the ADC to deal only with the signal of interest and its in-band noise.

The correct way to extend this to RF requires that adjacent channels and wideband noise be suppressed prior to sampling the waveform [12]. This is exactly how digital receivers in basestations work [65]. The entire band of interest is block-downconverted to a convenient IF, where a surfacce acoustic wave (SAW) bandpass filter passes all the channels in the band. An ADC digitizes the entire band, and from then on all channels are processed in the digital domain. The SAW filter acts like a bandpass antialias filter.

The situation in the mobile handset is different. First, there is no need to receive all the channels in a band simultaneously: only one channel is of interest. Second, the SAW filter must be eliminated, because it adds to the BOM and it is customized to one band, and cannot service the multiple bands and modes that a modern handset is required to support [53]. Therefore, what is required is a programmable method to realize finite-impulse response (FIR)-like filtering to narrow in on a band of interest and suppress aliases internally *before* sampling (Fig. 20). A synthesized clock frequency can direct this mostly digital receiver to narrow in on any band within a large frequency range, and any reasonable channel bandwidth.

Texas Instruments has developed a mainly digital Bluetooth transceiver of this type, which also integrates a baseband processor on the same substrate as a sampled-data radio front-end in 0.13-μm CMOS [66]. The front-end uses mainly passive switched capacitor circuits and single FET transconductors, which operate well at low supply voltages. The sole on-chip inductor is in the oscillator. It is claimed that this approach will finally make practical the very low-cost SOC that had been envisioned originally for Bluetooth as a wireless replacement for cables.

If this approach is a glimpse of the next paradigm for CMOS radios, the RF SOC will now resemble, in every way, the same mixed-signal baseband ICs that had inspired the very first forays into RF CMOS.

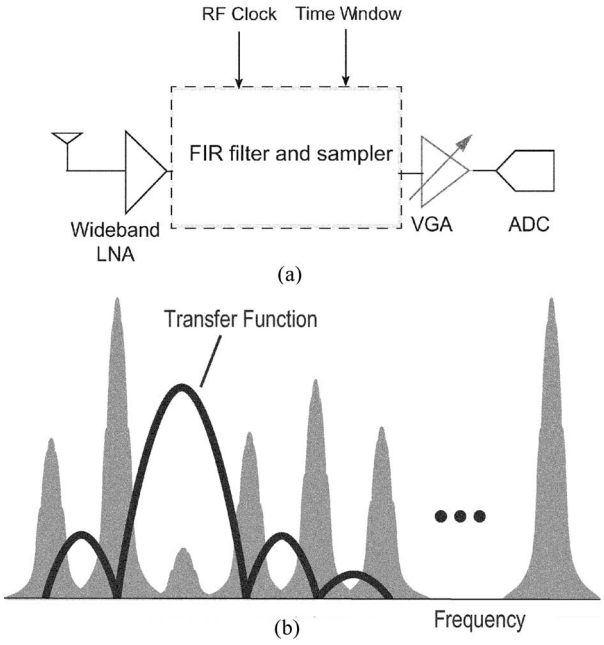


Fig. 20. Possible front-end for a software-definable wireless receiver. The functions enclosed in the dashed box narrow in on a carrier frequency and a channel bandwidth, while suppressing adjacent channels. The input to the optional VGA is a series of discrete-time samples at baseband (or at low IF), which are digitized by the ADC.

VI. Conclusion

This paper recounts the emergence of RF circuits and transceiver architectures from university research, and their appearance in commercial products in recent years. We may categorize the history of RF electronics into two main epochs: the first epoch spanning the dawn of vacuum-tube electronics until the 1950s, driven by the worldwide market for receivers for broadcast radio and television, and the needs of military communication during World War II, a time when electronics was synonymous with radio frequency circuits; then a relative decline when RF circuits disappeared from electronics curricula and became a black art with only a few practitioners, while baseband data communications drove the microelectronics revolution; and then the second epoch, starting in the early 1990s with the digital cellular telephone and continuing today. It is in this second epoch that the CMOS mixed-signal philosophy and technique that developed in the intervening years was applied to radio transceivers. The next epoch, it seems, will leave behind the analog-centric circuits and architectures that are beginning to mature today, and convert radios (the RF front-end as well as the baseband) into software-controlled, largely digital devices. We are poised at its threshold.

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