CMPT 295

Assignment 4: CPU CIRCUIT
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1. Documentation File Index:
    a.a4solns.pdf: Solution to assignment questions
    b. circuit.pdf: CPU Circuit with CM component

2. Complete the following table, listing all the μ-instructions and their corresponding control words that this CPU is capable of performing.

#	INSTRUCTIONS	CONTROL WORDS				
		CI	Ib	Ia	s0	oe
1	A ← DATA INPUT	0	0	1	1	0
2	B ← DATA INPUT	0	1	0	1	0
3	B ← A+B / DATA OUTPUT ← A+B	0	1	0	0	0
4	B ← A+B+1 / DATA OUTPUT ← A+B+1	1	1	0	0	0
5	A ← A+B	0	0	1	0	0
6	A ← A+B+1	1	0	1	0	0
7	A,B ← DATA INPUT	0	1	1	1	0
8	A,B ← A+B	0	1	1	0	0
9	A,B ← A+B+1	1	1	1	0	0
10	DATA OUTPUT = B	0	0	0	0	0
11	DATA OUTPUT = Z (HIGH IMPEDENCE)	0	0	0	0	1

3. Express the behaviour of the CM component as a function selection table.

~Cl	cm	Function
0	0	Data Output = Does not change
0	1	Data Output = Complement data input
1	0	Data Output = 0
1	1	Data Output = 0

6. Extend your table in (2) to include the control inputs of CM and to include any additional μ-instructions that ae now possible with this enhancement.

#	INSTRUCTIONS	CONTROL WORDS							
		CI	Ib	Ia	s0	X	oe	cm	cl
12	A ← COMPLEMENT DATA INPUT / ~A	0	0	1	1	0	0	1	0
13	B ← COMPLEMENT DATA INPUT / ~B	0	1	0	1	0	0	1	0
14	A ← COMPLEMENT DATA INPUT+1 / ~A+1	1	0	1	1	0	0	1	0
15	B ← COMPLEMENT DATA INPUT +1 / ~B+1	1	1	0	1	0	0	1	0
16	A,B ← COMPLEMENT DATA INPUT / ~A+~B	0	1	1	1	0	0	1	0
17	A,B ← COMPLEMENT DATA INPUT+1 / ~A+~B+1	1	1	1	1	0	0	1	0
18	A ← 0 (WITHOUT DATA INPUT)	0	0	1	1	0	0	0	1
	A ← 0 (WITHOUT DATA INPUT)	0	0	1	1	0	0	1	1
19	B ← 0 (WITHOUT DATA INPUT)	0	1	0	1	0	0	0	1
	B ← 0 (WITHOUT DATA INPUT)	0	1	0	1	0	0	1	1
20	A,B ← 0 (WITHOUT DATA INPUT)	0	1	1	1	0	0	0	1
	A,B ← 0 (WITHOUT DATA INPUT)	0	1	1	1	0	0	1	1

7. For each of the following proposed assembly language instructions from a hypothetical instruction set architecture, provide a sequence of μ-instructions that, when executed will perform the desired instruction.

				CONTROL WORDS							
	OPR	OPND	SEMANTICS	Cl	lb	la	s0	X	oe	cm	cl
A)	CLR	A	A ← 0	0	0	1	1	0	0	0	1
B)	INC	B	B ← B+1	0	0	1	1	0	0	0	1
				1	1	0	0	0	0	0	0
C)	SHL1	A	A ← A << 1	0	1	0	1	0	0	0	1
				0	1	0	0	0	0	0	0
				0	0	1	0	0	0	0	0
D)	SET	B	B ← 1	0	1	1	1	0	0	0	1
				1	1	0	0	0	0	0	0
E)	DECB	DATA INPUT	B ← B – DATA INPUT	0	0	1	1	0	0	1	0
				1	1	0	0	0	0	0	0