TÉCNICO LISBOA

Lab 4: Audio Amplifier

Circuit Theory and Electronics Fundamentals
Master's programme in Engineering Physics, Técnico, University of Lisbon

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1 Introduction

The main objective of this laboratory assignment is to design an audio amplifier. This circuit should be able to amplify $10\ mV$ of alternating current at a wide range of frequencies. To this purpose, three types of components will be employed: resistors, capacitors and transistors.

The secondary goal is to achieve the best performance at the lowest cost. This is quantified by maximizing the following function:

$$M = \frac{voltageGain \cdot bandwidth}{cost \cdot lowerCutoffFrequency} \tag{1}$$

$$cost = cost\ of\ resistors + cost\ of\ capacitors + cost\ of\ transistors$$
$$cost\ of\ resistors = 1MU/k\Omega$$
$$cost\ of\ capacitors = 1MU/\mu F$$
$$cost\ of\ transistors = 0.1MU/transistor$$

In Section 2, the amplifier is presented and its behaviour is studied using a simulation. This is followed by a theoretical analysis of the circuit, in Section 3. Both are compared in the final section, Section 4. Here, M is also presented, allowing for some considerations to be made about the circuit designed. The simulation was run by using **Ngspice** and the theoretical calculations were performed with **Octave**.

2 Simulation Analysis

The basic template for an amplifier is as follows:

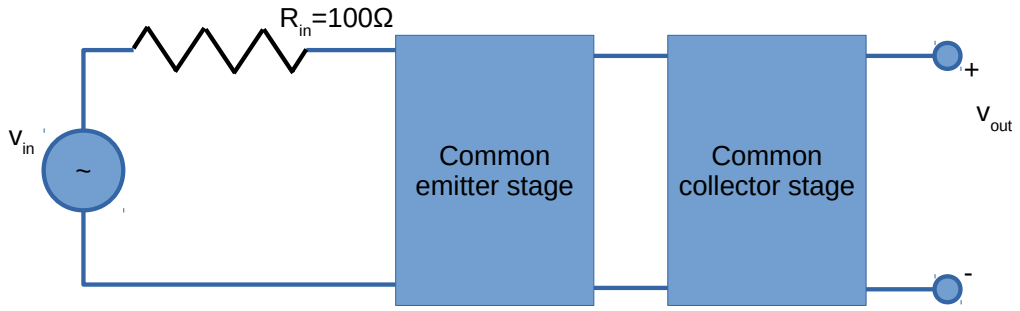

Figure 1: Template

2.1 Common emitter stage

The purpose of the common emitter amplifier is to amplify the signal with linear DC gain. To this purpose the following circuit can be employed:

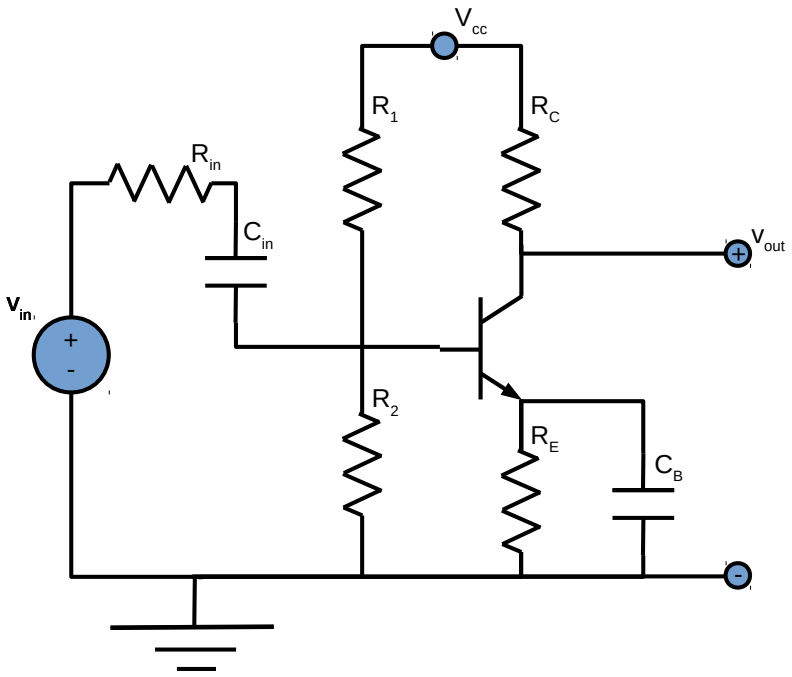

Figure 2: Common emitter stage

2.2 Common collector stage

The purpose of the common collector amplifier is to supply enough current to the load. To this purpose the following circuit can be employed:

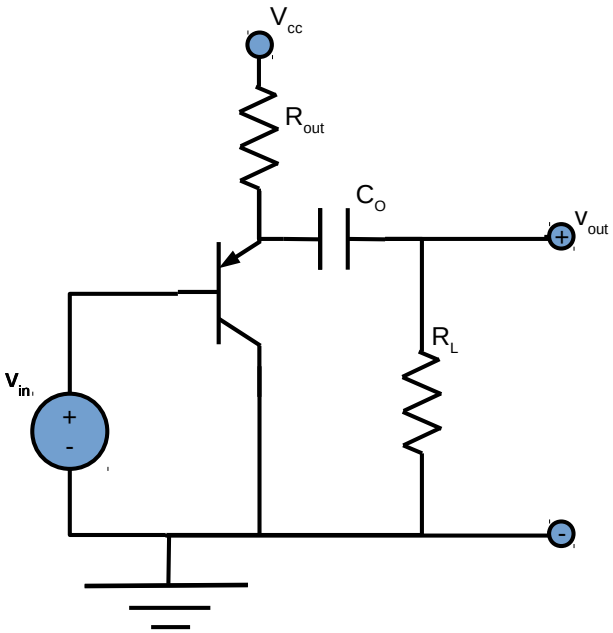

Figure 3: Common collector stage

2.3 Final result

Combining these two circuits, a very good amplifier can be designed:

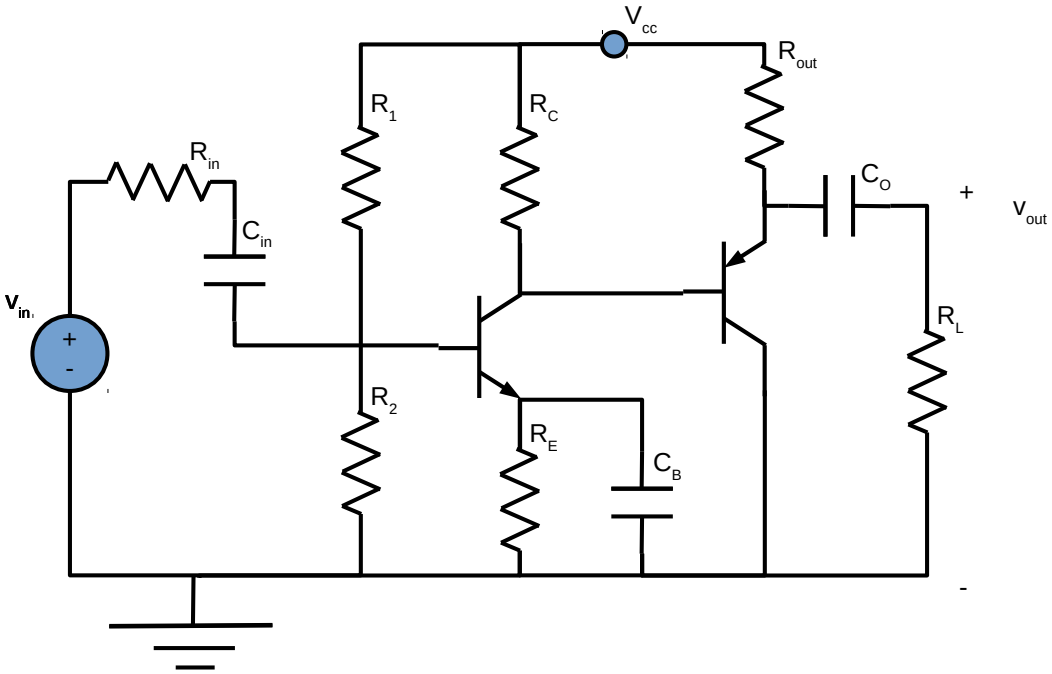

Figure 4: Amplifier

By a lengthy process of trial and error, attempting to maximize the merit figure, while also keeping the input impedance high and the output impedance low, gave us the following parameters:

Parameter	Value
$R_1(k\Omega)$	220.0
$R_2(k\Omega)$	42.0
$R_c(k\Omega)$	1.0
$R_e(k\Omega)$	0.02
$R_{out}(k\Omega)$	0.2
$C_i(\mu F)$	55.0
$C_b(\mu F)$	780.0
$C_o(\mu F)$	570.0

Table 1: Parameters

Input	0.8717151+i-0.162514
Output	-36.8764+i1266.19

Table 2: Impedances (10^3)

Name	**Value**
vcc (V)	1.200000e+01
in (V)	0.000000e+00
in2 (V)	0.000000e+00
base (V)	8.092567e-01
coll (V)	6.386599e+00
emit (V)	1.154112e-01
emit2 (V)	7.127663e+00
out (V)	0.000000e+00
rin (A)	0.000000e+00
r1 (A)	5.086702e-05
r2 (A)	1.926802e-05
rc (A)	5.613401e-03
re (A)	5.770558e-03
rl (A)	0.000000e+00
rout (A)	-2.43617e-02
cin (A)	0.000000e+00
cb (A)	0.000000e+00
co (A)	0.000000e+00
vb1 (A)	3.159900e-05
ve1 (A)	5.770558e-03
vc1 (A)	5.738959e-03
ve2 (A)	2.436168e-02

Table 3: Simulation results OP

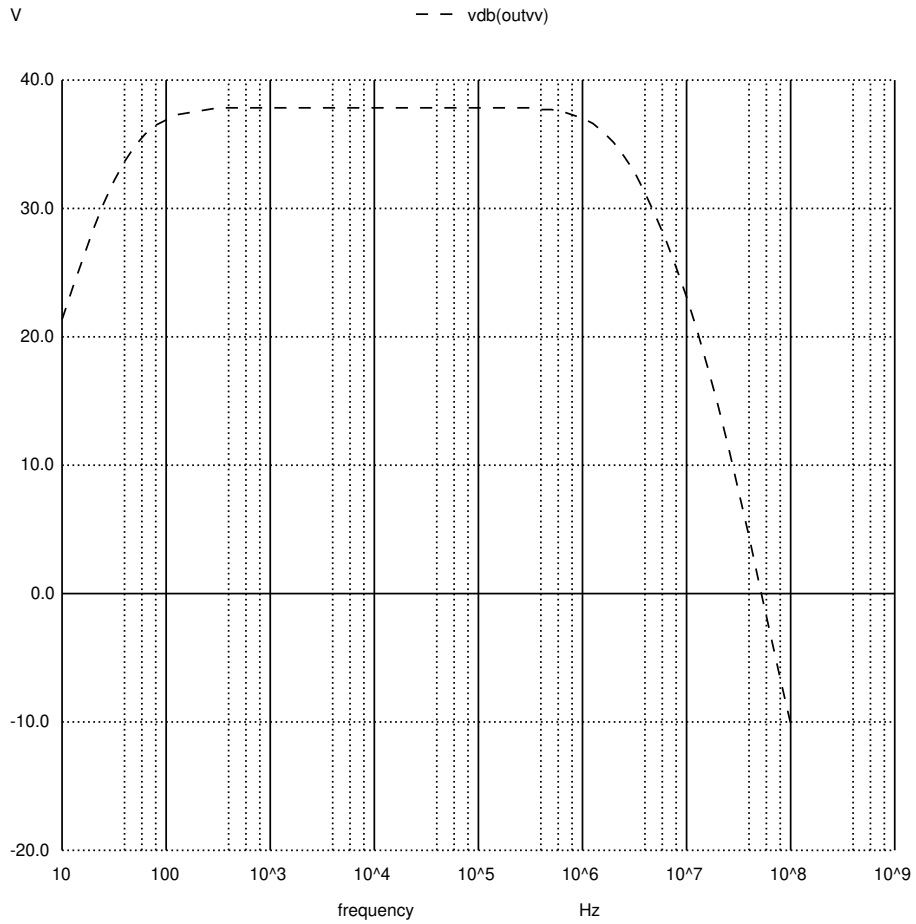

Figure 5: Voltage gain

Voltage gain	78.27066073399706
Lower cutoff frequency	50.0412
Bandwidth	2142211.9588

Table 4: Voltage gain, lower cutoff frequency and bandwidth

Afterwards, we also designed a second circuit, with only merit maximisation in mind:

Parameter	Value
$R_1(k\Omega)$	204.0
$R_2(k\Omega)$	42.0
$R_c(k\Omega)$	2.7
$R_e(k\Omega)$	0.3
$R_{out}(k\Omega)$	0.32
$C_i(\mu F)$	64.0
$C_b(\mu F)$	790.0
$C_o(\mu F)$	578.0

Table 5: Parameters

Input	1.539177+i-0.472487
Output	0.01623532+i0.001019533

Table 6: Impedances (10^3)

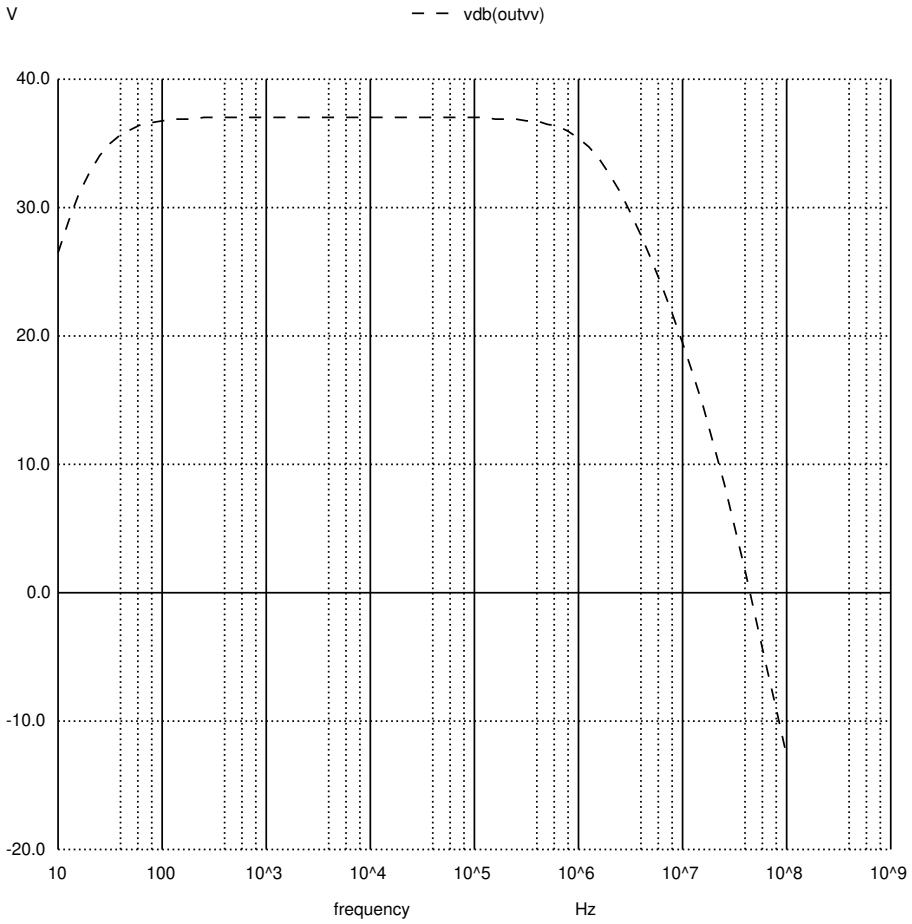

Figure 6: Voltage gain

Voltage gain	70.84847392695694
Lower cutoff frequency	25.1392
Bandwidth	1497536.8608

Table 7: Voltage gain, lower cutoff frequency and bandwidth

As one can see, a bigger merit also resulted in a lower cutoff frequency. The gain became slighly smaller. As the goal would be for te lower cutoff frequency to be below $20Hz$ there is still some room for improvement. The input resistor (real part of the impedance) is also bigger, but unfortunately so is the output one, which would result in more dissipated power.

3 Theoretical Analysis

To study the circuit in figure 4, it was first performed an operating point analysis, OP, as it was explained in classes. In this DC analysis (the source is like a short-circuit), the capacitors have infinite impedance, so they behave like an open circuit. The fact that capacitor C_O behaves like an open circuit implies that the DC final output voltage is equal to 0 V, like the DC initial voltage. Bearing this in mind, the capacitors and R_{in} can be removed from the OP analysis. Using a Thévenin's equivalent for the bias circuit makes the OP analysis quite simple. Considering first the common emitter, with the mesh analysis it is possible to observe that:

$$-V_{eq} + R_{eq}I_B + V_{BEON} + R_E I_E = 0 \tag{2}$$

In the equation above, I_B is the base current and I_E is the emitter current of the considered transistor. V_{BEON} was estimated to be $0.7\ V$. By using the equation $I_E = (1+\beta_F)I_B$ (3), the following is obtained:

$$I_B = \frac{V_{eq} - V_{BEON}}{R_{eq} + (1+\beta_F)R_E} \tag{4}$$

With other transistor equation that gives the collector current, $I_C = \beta_F I_B$ (5), it is possible to compute all DC voltages and currents in the common emitter circuit. The output voltage of this stage will simply be $V_{O1} = V_{CC} - R_C I_C$ (6).

The common collector stage is simple to analyse. The mesh analysis gives that:

$$V_{O1} - V_{cc} + R_{out}I_E + V_{EBON} = 0 \iff I_E = \frac{V_{CC} - V_{EBON} - V_{O1}}{R_E} \tag{7}$$

Using the already mentioned equations for the transistor (and Ohm's Law) it is then possible to calculate all the voltages and currents of the circuit. Finally, it can be observed in table 8 the results obtained for the OP analysis of the circuit in figure 4.

Name	Value
V_{cc} (V)	12.000000
V_{eq} (V)	1.923664
V_{B1} (V)	0.813168
V_{C1} (V)	6.373079
V_{E1} (V)	0.113168
V_{E2} (V)	7.073079
I_{B1} (mA)	0.031488
I_{R1} (mA)	0.005048
I_{R2} (mA)	0.026440
I_{C1} (mA)	5.626921
I_{E1} (mA)	5.658409
I_{E2} (mA)	24.634607
I_{B2} (mA)	0.107905
I_{C2} (mA)	24.526702

Table 8: Theoretical results OP

This OP analysis is very important to compute the parameters necessary to perform the incremental analysis.

As derived in classes, the gain for the common emitter is equal to:

$$A_v = -\frac{g_m}{\frac{1}{ro} + \frac{1}{R_C}} \frac{1}{(\frac{1}{r_\pi} + \frac{1}{R_{eq}})(R_{in} + \frac{1}{\frac{1}{r_\pi} + \frac{1}{R_{eq}}})} \tag{8}$$

The common emitter input impedance is the parallel of R_{eq} and r_π and its output impedance is the parallel of r_o and R_C. Using **Octave**, the following results were obtained for the common emitter:

Gain	-184.501997
Input Impedance	776.470759
Output Impedance	925.299996

Table 9: Gain and impedances - Common emitter

As desired, the input impedance is bigger than R_{in}, however it would be better if the input impedance was bigger. The gain is negative because the common emitter is designed in a way that inverts the amplitude. However, this is not problematic, because the human ear is not affected by this inversion, what matters is the absolute value of the gain.

The gain for the common collector is easy to compute using the conductances:

$$A_v = \frac{g_\pi + g_m}{g_\pi + g_m + g_o + g_{out}} \tag{9}$$

The input and output impedances are calculated using the following equations:

$$Z_I = \frac{g_\pi + g_m + g_o + g_{out}}{(g_o + g_{out})g_\pi} \tag{10}$$

$$Z_O = \frac{1}{g_\pi + g_m + g_o + g_{out}} \tag{11}$$

The following results were obtained:

Gain	0.994290
Input Impedance	40572.222216
Output Impedance	1.009037

Table 10: Gain and impedances - Common collector

By observing the two last tables we can conclude that the two stages can be connected without significant signal loss, because the output impedance of the common emitter is small when compared with the input impedance of the common collector. It is also worth referring that the output impedance of the common collector is, as desired, smaller than the load resistance, considered to be 8Ω.

The gain and impedances obtained for the complete circuit are presented in table 11. The input impedance is equal to the input impedance of the common emitter, Z_{O1}. The gain and the output impedance are calculated with these equations, where the parameters with index 1 correspond to the common emitter and the parameters with index 2 correspond to the common collector:

$$A_v = \frac{\frac{1}{r_{\pi 2} + Z_{O1}} + \frac{g_{m2} r_{\pi 2}}{r_{\pi 2} + Z_{O1}}}{\frac{1}{r_{\pi 2} + Z_{O1}} + \frac{1}{R_{out}} + \frac{1}{r_{o2}} + \frac{g_{m2} r_{\pi 2}}{r_{\pi 2} + Z_{O1}}} A_{v1} \tag{12}$$

$$Z_O = \frac{1}{\frac{g_{m2} r_{\pi 2}}{r_{\pi 2} + Z_{O1}} + g_{o2} + g_{out} + \frac{1}{r_{\pi 2} + Z_{O1}}} \tag{13}$$

Gain	-179.357924
Input Impedance	776.470759
Output Impedance	4.926537

Table 11: Gain and impedances - Complete circuit

Incremental analysis allowed also to make a graph of the frequency response. However, with the model studied in classes for the transistor in incremental analysis, the frequency response stabilized until infinity, instead of going down eventually like it happens in the simulation.

Ngspice uses a quite complex model for the transistor, with lots of parameters, including capacitances. To try to have a theoretical frequency response more similar to the one provided by **Ngspice**, the following model was considered for the transistor, where two capacitors were added to the original model.

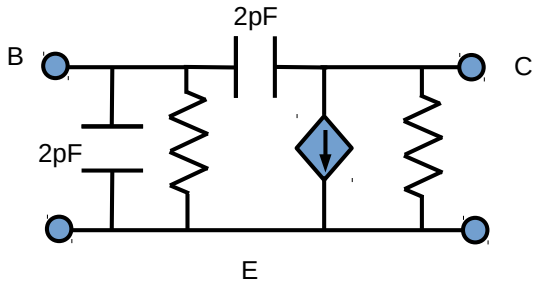

Figure 7: Transistor incremental model

With the model presented, the following graph was obtained for the frequency response.

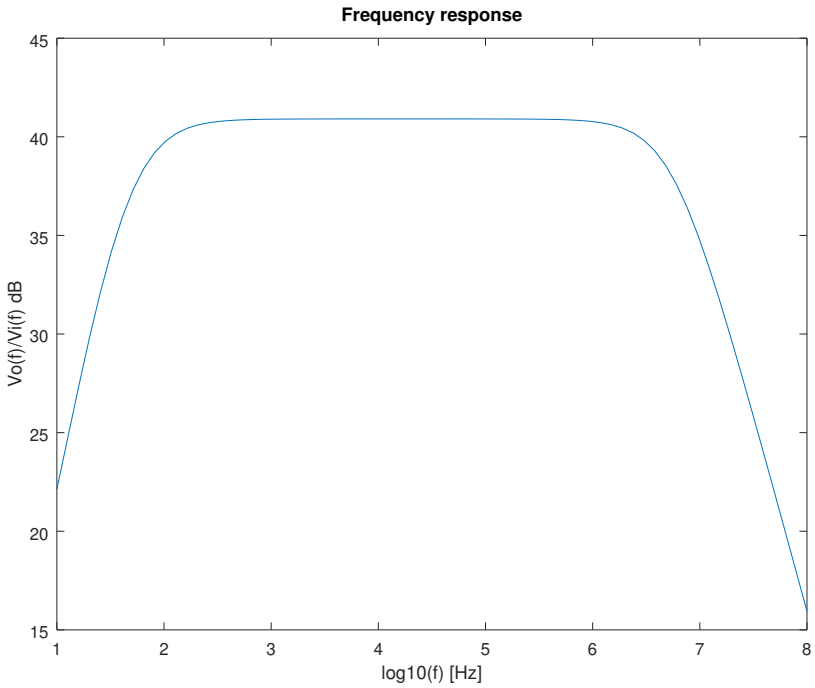

Figure 8: Theoretical frequency response

4 Conclusion

This laboratory assignment had as the main objective the construction and analysis of an audio amplifier. The chosen design is present in figure 4. The goal was to maximise the voltage gain and the bandwidth at which the circuit operates at "full capacity", while minimising the cost and the lower cutoff frequency, preferably to less than $20\ Hz$, the lower limit of the audible range.

We designed two circuits, as explained in 2, with two objectives in mind. By analysing the results obtained, we conclude that we were able to achieve a good result in either of the circuits designed, with high gain and low cost. Unfortunately we were not able to lessen the lower cutoff limit any more without lessening the merit. We also tried to lessen the output impedance, but this was not possible for the same reason.

The merit figure of our first circuit is: 2008 . For our second circuit, it's 2510 .

V	V_t	V_s	$\lvert V_t - V_s \rvert$	$Error(\%)$
V_{B1} (V)	0.813168	0.8092567	0.004	0.5
V_{C1} (V)	6.373079	6.386599	0.02	0.3
V_{E1} (V)	0.113168	0.1154112	0.003	2
V_{E2} (V)	7.073079	7.127663	0.06	0.8
I_{B1} (V)	3.1488e-05	3.1599e-05	0.0000002	0.4
I_{R1} (V)	5.048e-06	5.086702e-05	0.00005	100
I_{R2} (V)	2.644e-05	1.926802e-05	0.000008	40
I_{C1} (V)	0.005626921	0.005738959	0.0002	2
I_{E1} (V)	0.005658409	0.005770558	0.0002	2
I_{E2} (V)	0.024634607	0.02436168	0.0003	2

Table 12: Theoretical values (V_t) and Simulation values (V_s) of the operating point analysis (table produced with **Python**) - The absolute deviation and error presented here are rounded up to one significant digit, for ease of interpretation.

Some deviations between the simulation and theoretical results were expected, due to the different model used by **Ngspice** for transistors. In the theoretical analysis, we used very simple models. These deviations can be observed not only in table 12, but also by comparing figures 5 and 8 and the gains and impedances computed.

All in all, the objectives were met. With more time and a lengthier study, better results could be obtained, and other solutions implemented.