**BYOC course**

**Homework exercise #1**

**An example project**

**Part2**

1. **Homework 1 report**

Your homework assignment is made the report detailed in sections 3.1-3.3 and of a zip file of your entire project – as described in section 3.4 below.

1. **Compilation**
   1. Fill up the following table showing the compilation errors you found

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| No. | Compilation error message | filename | Line no. | What was the error | What was the fix |
| 1 | When condition 'o' is not of type std\_ulogic. | mux\_2to1.vhd | 22 | The letter ‘o’ was defined instead of ‘0’ (zero) | Changing the letter ‘o’ to ‘0’ (zero) |
| 2 | = can not have such operands in this context. | counter\_6bits.vhd | 23 | The if’s literal was illegal since it was comparing “1” instead of ‘1’ | Changing from a value “1” to logical on ‘1’ |
| 3 | Choice 0111 duplicated in select. | decoder\_7seg.vhd | 42 | There was a duplicate condition in the selection (‘0111’ repeated itself) | Replacing line #41’s condition from ‘0111’ to ‘0110’ to create a full binary sequence from 0 to F |
| 4 | An index or element of the formal port cntr\_out of counter\_6bits is missing in instantiation. | p4\_top.vhd | 117 | According to the design we suppose to output 6 bits from the 6bits counter, 4 LSB digits to encode digit value and 2 MSB to encode the digit number. The code was incorrect since it configured 7 bits (5 LSB and 2 MSB) instead of 6 bits | Changing digital\_val to be 4 LSB bits from cntr\_out (3 downto 0) and digital\_no to be the 2 MSBs(5 downto 4) |
| 5 | Width mismatch. Expected width 2, Actual width is 4 for dimension 1 of anodes\_out. | p4\_top.vhd | 133 | In\_no received the value from anodes\_out instead of digit\_no | Changing the input value of in\_no to digit\_no. |
| 6 | Width mismatch. Expected width 4, Actual width is 2 for dimension 1 of digit\_no. | p4\_top.vhd | 134 | Out\_lines sent the value to digit\_no instead of anodes\_out | Changing the output value of out\_lines to anodes\_out |
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1. **Simulation**

Use may use the Xilinx ISIM or the Modelsim student edition simulator.

After running the simulation you should:

* 1. Save the format of signals you want to monitor on the simulator screen
  2. Run the simulation and show the problem you find by printing the screen and attaching it to this doc file.
  3. Fix the problem. Explain the source of the problem, and show simulation of the corrected result.
  4. Use the following format for this:

|  |
| --- |
| Problem description: |
| An incorrect output was selected by the outputs of 2to4 decoder, resulting in an incorrect display of the digits(the 2nd left one was on twice and ahead of time). |
| Simulation picture before fixing: |
| as can be seen, the right digit does not change to the 2nd right one. (1110 → 1011 instead of 1101) |
| Fix description |
| The order of the binary values was restored in order to correctly move from the rightmost digit to the leftmost one. |
| Simulation picture after fix: |
|  |

If more than a single fix step was used, duplicate the above format and show the 2nd, 3rd, 4th,… fix as well.

1. **ISE compilation & testing on Nexyxs2 board**

In this stage you are required to keep the BIT files of all of your trials. Call them p4\_v1.bit, p4\_v2.bit, p4\_v3.bit etc. Read again the description of the project in section 1.a of part1 of the report and verify that your design complies with that description (if you want a good grade). Then fill up the following table showing other errors you found in this step.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| No. | Error symptom | filename | Line no. | What was the error | What was the fix |
| 2 | The incorrect segments were lit when the counter digits were displayed due to incorrect wiring. | **p4\_toplevel.ucf** | 11,13 | Incorrect assignment of the 7 segment output within each digit.  (fix the ucf to correctly wire the components accordingly) | The segments were correctly set according to the board’s pinout and the numbering provided.(switch H14 with G14) |
| 3 | Incorrect digit display order when completing each hex. Cycle. | **p4\_toplevel.ucf** | 1,2 | The anodes were incorrectly assigned resulting in incorrect display order. | Correct anode assignment according to the boards pinout was made. (switch H17 with F17) |
| 4 | Pushbutton was incorrectly assigned | **p4\_toplevel.ucf** | 21 | The left instead of the right most button was assigned | The correct button was assigned according to the board’s description.(H13→B18) |
| 5 | The counter is automatically incremented twice the required speed | Ck\_divider.vhd | 32 | The clock divider rate was set twice the required speed (instead of 1.5hz, it is set to exactly half).  Since the frequency of the clock has to be multiplied by 2^25 and in the original code it is divided by 2^24, the cycle is twice as fast. | Clock Rate of FPGA CPU: 5 Mhz divider clock segments (required) : 2^25. (and not 2^24, in the original erroneous code)  CK\_out freq = CK\_in freq / 2^25 5 \* 1000 / 2^25 = 0. 000149 = ~0.00015s→ 1.5Hz  → ~0.67s |
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1. **Submission instructions**

You should submit a single zip file called **HW1.zip** including this report and the Simulation and implementation projects. It should have four directories/folders. The first is called **Src**, the 2nd is called **Sim** the third is called **ISE** and the last one is called **Docs**. Those will include:

* **Src** – here you put all of the \*.vhd sources, (including the TB and the ucf files), used for simulation and implementation
* **Sim** – here you should have all of the Simulation project files created by the simulator you used (ISIM or Modelsim)
* **ISE** – here you should have all of the Implementation project files created by Xilinx ISE SW in the laqb
* **Docs** – Here you put your report. The first few lines in the report will have your ID numbers (names are optional). You should submit is in Microsoft Word file format to allow addition of remarks by the grader.

**Enjoy the homework**