STM32 Interrupt Service Routine Priority

From RapidSTM32

Three parameters are used to configure STM32 Interrupt Service Routine Priority.

- NVIC_PriorityGroup
- NVIC_IRQChannelPreemptionPriority
- NVIC_IRQChannelSubPriority

The relationship and availability between each parameter are summarized in the following table.

NVIC_PriorityGroup	NVIC_IRQChannelPreemptionPriority	NVIC_IRQChannelSubPriority
0	0	0-15
1	0-1	0-7
2	0-3	0-3
3	0-7	0-1
4	0-15	0

STM32 Interrupt Service Routine is based on Nested Vectored Interrupt Controller (NVIC) and supports nesting (stacking) of interrupts, allowing an interrupt to be serviced earlier by exerting higher priority. The followings summarize important points.

1. The lower the number the higher the priority.
2. NVIC_PriorityGroup has the highest priority. All other interrupts with lower NVIC_PriorityGroup that occur after are put in a stack (queue).
3. NVIC_IRQChannelPreemptionPriority is used to determine if an interrupt that occurs after can overtake previous interrupt that is being serviced.
4. NVIC_IRQChannelSubPriority is used to determine priority if two interrupts occur at the same time. (If NVIC_IRQChannelSubPriority is not determined, the position in the NVIC table is used to determine the priority.)

To aids understanding we will use an example to illustrate the concept and usage of these parameters.

Example 1

EXTI1 is NVIC_PriorityGroup0 and NVIC_IRQChannelSubPriority15 TIM2 is NVIC_PriorityGroup0 and NVIC_IRQChannelSubPriority0 ADC3 is NVIC_PriorityGroup1

EXTI1 and TIM2 is NVIC_IRQChannelPreemptionPriority0 by default.

If EXTI1 interrupt is being serviced and TIM2 interrupt occurs, TIM2 interrupt is put in a queue. This is because EXTI1 and TIM2 has the same NVIC_IRQChannelPreemptionPriority level, so TIM2 can not take over and put EXTI1 interrupt in pending state.

If EXTI1 and TIM2 interrupts occur at the same time, EXTI1 interrupt will be put in

a queue and TIM2 will be serviced first, because TIM2 has higher NVIC_IRQChannelSubPriority.

If EXTI1 interrupt is being serviced and ADC3 interrupt occurs, ADC3 interrupt will have to wait since EXTI1 interrupt has higher NVIC_PriorityGroup priority.

Example 2

EXTI1 is NVIC_PriorityGroup4 and NVIC_IRQChannelPreemptionPriority15 TIM2 is NVIC_PriorityGroup4 and NVIC_IRQChannelPreemptionPriority0 ADC3 is NVIC_PriorityGroup1

If EXTI1 interrupt is being serviced and TIM2 interrupt occurs, EXTI1 interrupt is paused and put in a queue and TIM2 is serviced. This is because EXTI1 and TIM2 has the same NVIC_PriorityGroup4 level, and TIM2 has a higher NVIC_IRQChannelPreemptionPriority level.

If TIM2 interrupt is being serviced and ADC3 interrupt occurs, TIM2 interrupt is paused and put in a queue and ADC3 interrupt is serviced. This is because ADC3 has a higher NVIC_PriorityGroup level.

The above examples are intended as preliminary guidelines only. For more detailed in formation, consult relevant technical documents.

Category: Interrupt