

A

U\_POWER  
POWER.SchDoc

U\_CLOCK\_GENERATOR  
CLOCK\_GENERATOR.SchDoc

B

U\_CONNECTIONS  
CONNECTIONS.SchDoc

U\_FPGA  
FPGA.SchDoc

U\_STM32  
STM32.SchDoc

U\_AUDIO\_CODEC  
AUDIO CODEC.SchDoc

C

U\_DAC  
DAC.SchDoc

U\_ADC  
ADC.SchDoc

D

Title **MOTHERBOARD**

Size: A4 Number:2 Revision:1.9

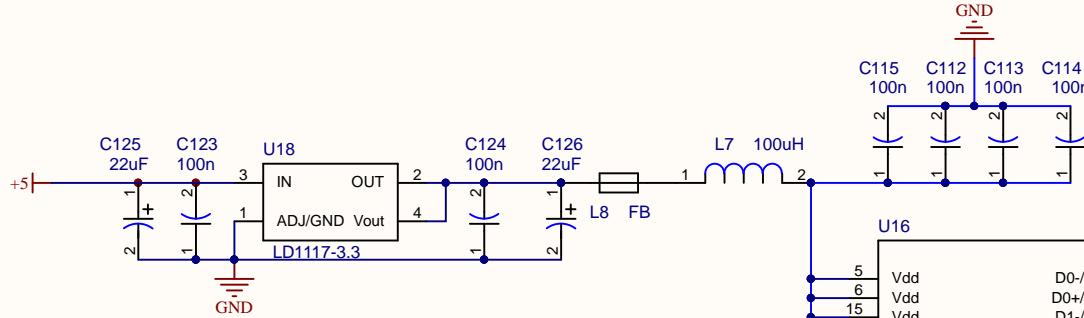
Date: 15.07.2020 Time: 20:01:45 Sheet 2 of 18

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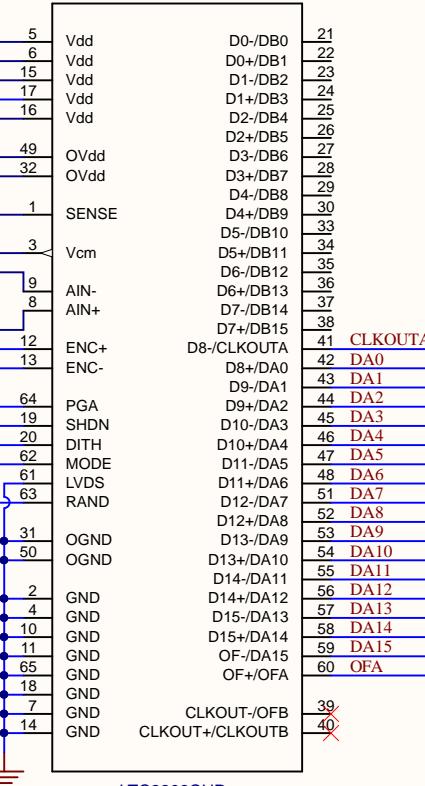
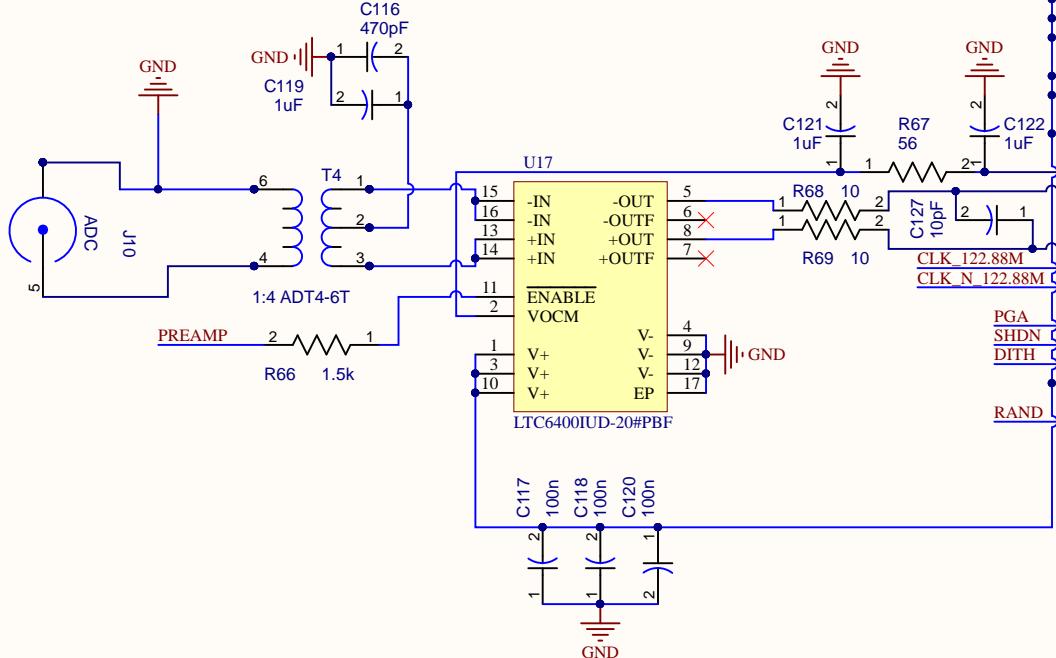
A

A



B

B

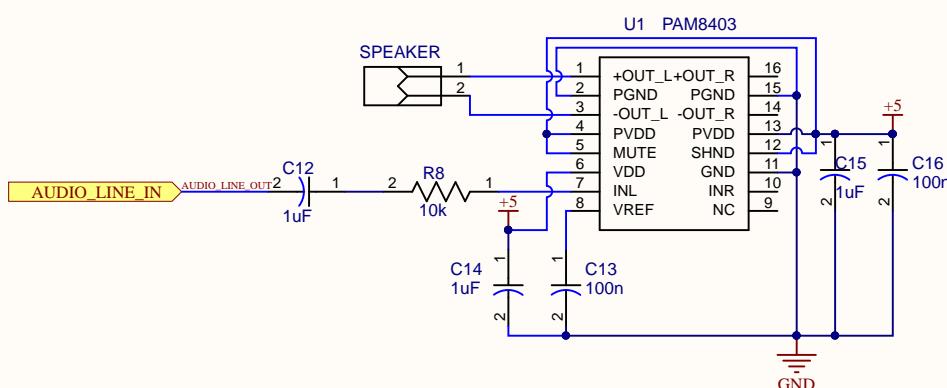
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Size: A4 Number:3 Revision:1.9

Date: 15.07.2020 Time: 20:01:46 Sheet 3 of 18

File: D:\Dropbox\Develop\Projects\UA3REO\Scheme\EXPERIMENTAL\MOTHERBOARD\ADC.SchDoc

**Altium**



Title <b>AF AMP</b>			* UA3REO
Size: A4	Number:4	Revision:1.9	BH8CGJ
Date: 15.07.2020	Time: 20:01:46	Sheet 4 of 18	*
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A

A

B

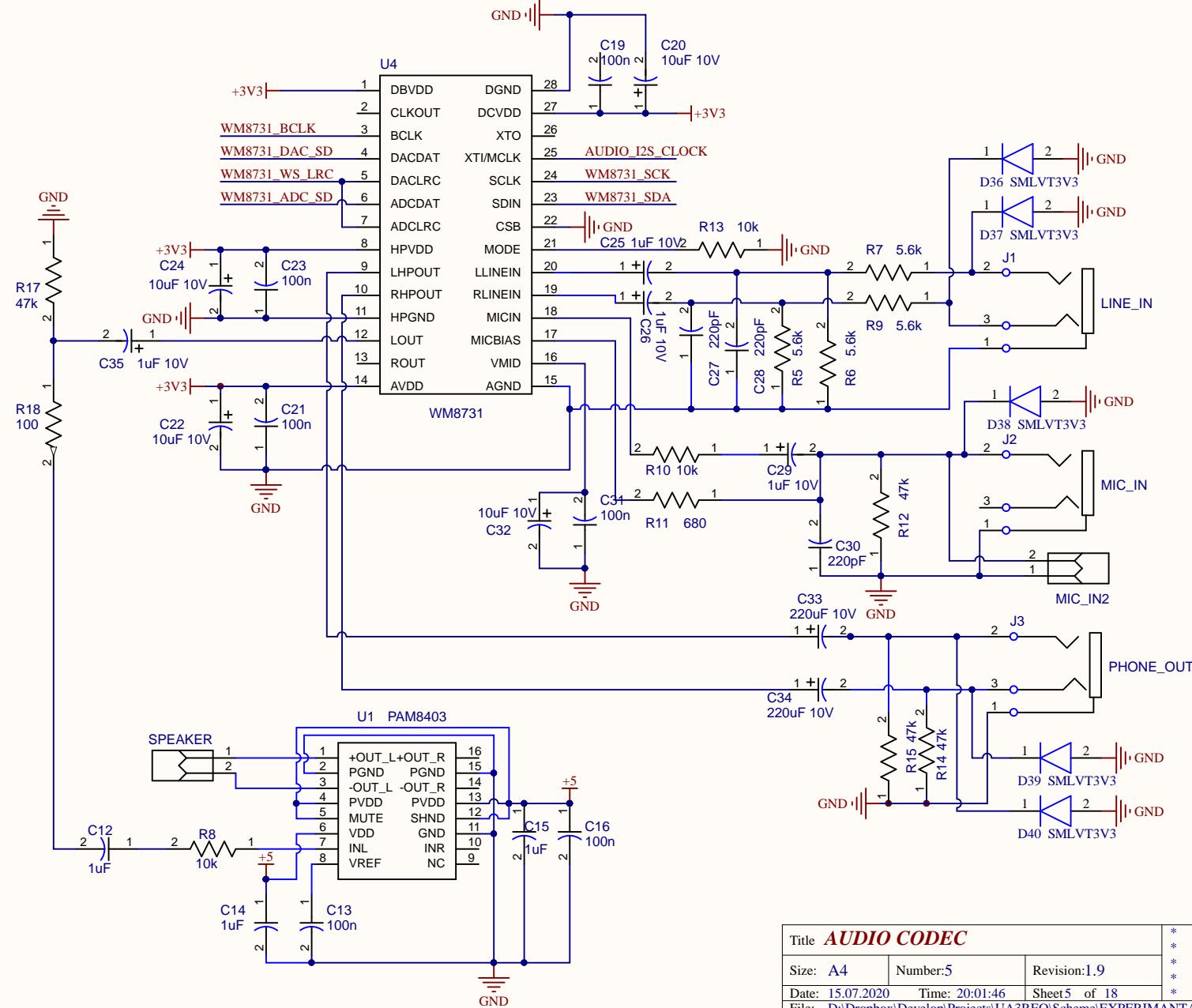
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C

C

D

D

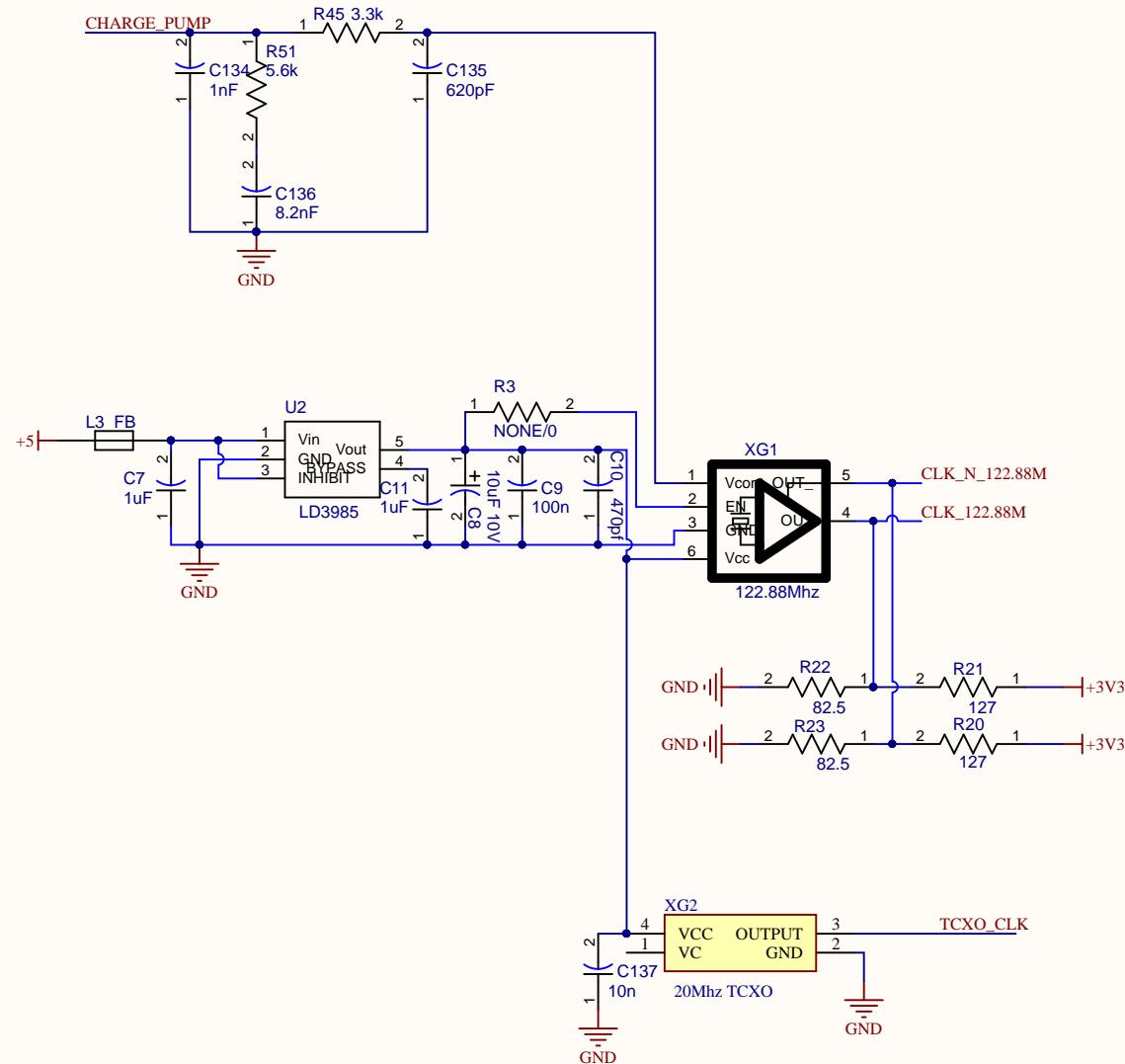
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Size: A4 Number:5 Revision:1.9

Date: 15.07.2020 Time: 20:01:46 Sheet 5 of 18

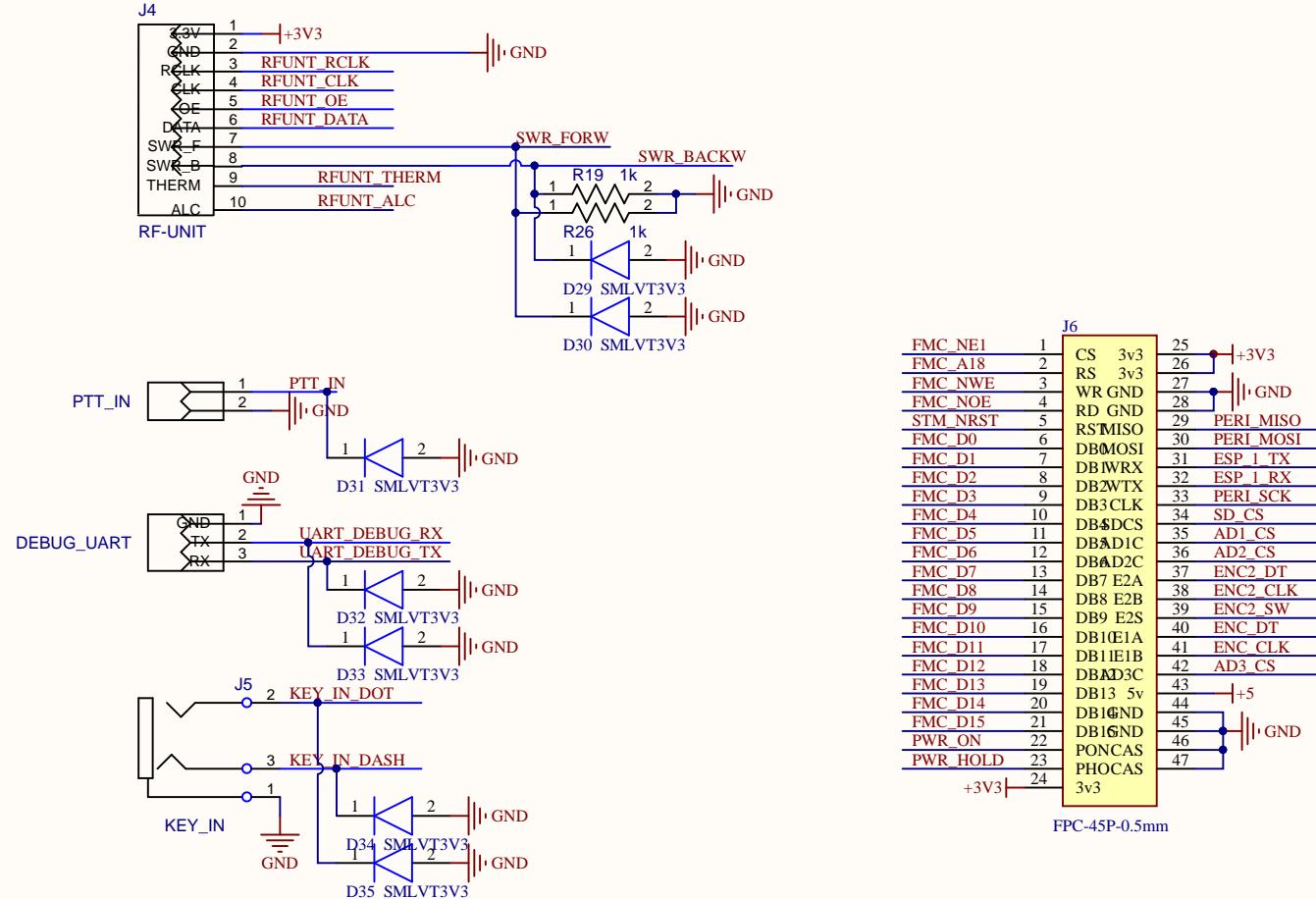
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**Altium**



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Date: 15.07.2020 Time: 20:01:46  
File: D:\Dropbox\Develop\Projects\UA3R\

**Altium**

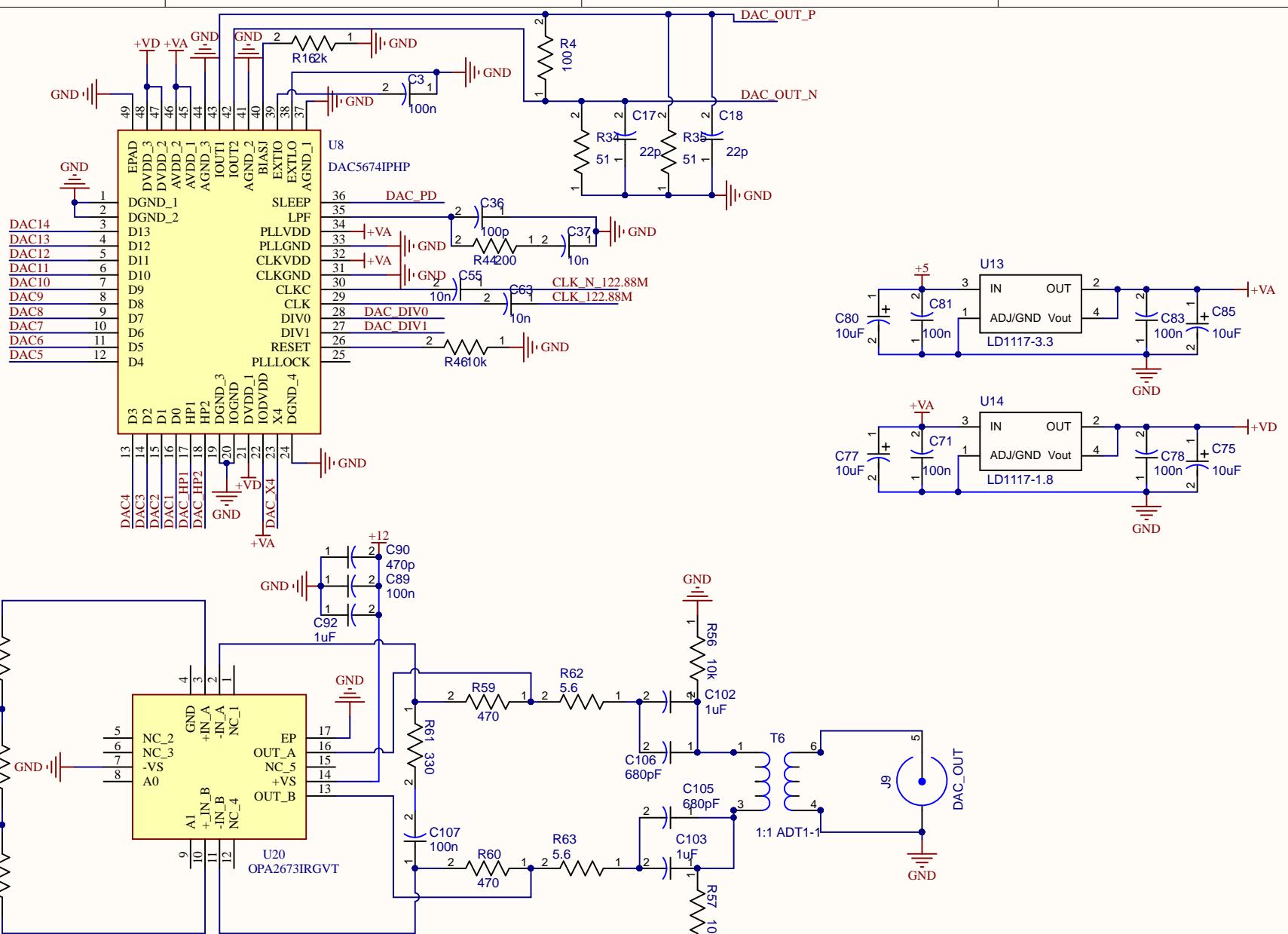
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Size: A4 Number: 7 Revision: 1.9

Date: 15.07.2020 Time: 20:01:46 Sheet 7 of 18

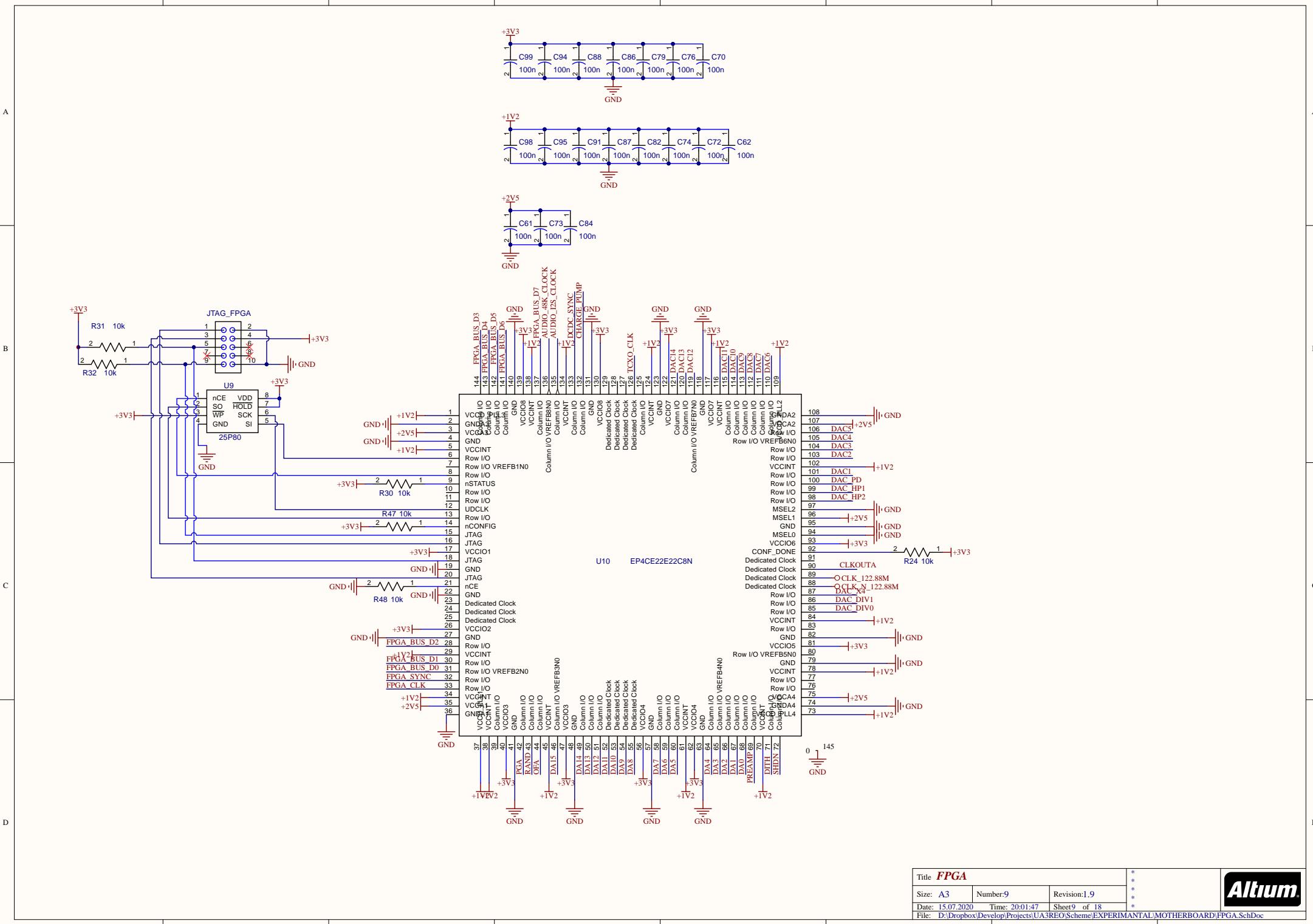
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**Altium**



Title <b>DAC</b>		
Size: A4	Number: 8	Revision: 1.9
Date: 15.07.2020	Time: 20:01:46	Sheet 8 of 18
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**Altium**

**Title *FPGA***

Size: A3

Number: 9

Revision: 1.9

Date: 15.07.2020

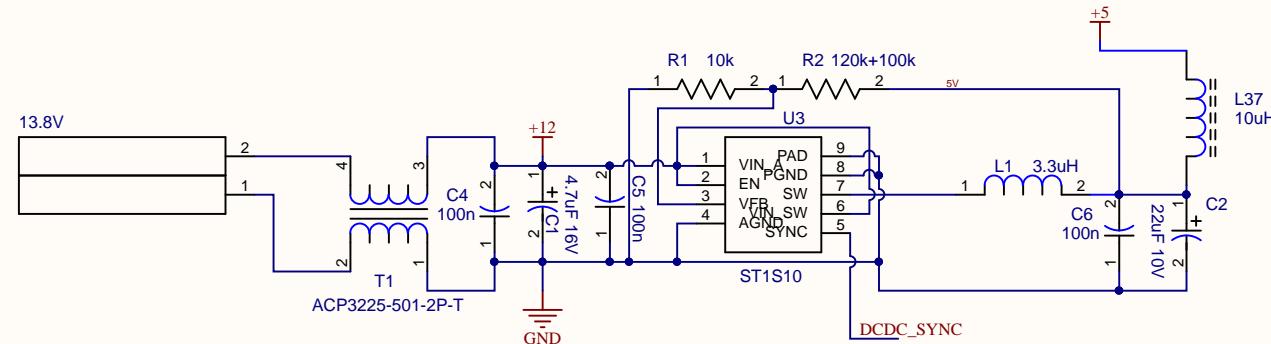
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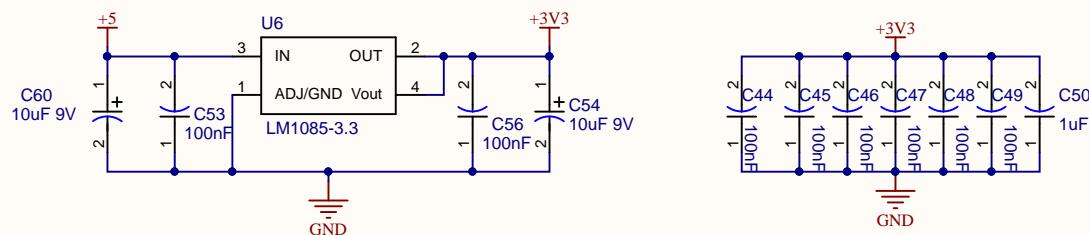
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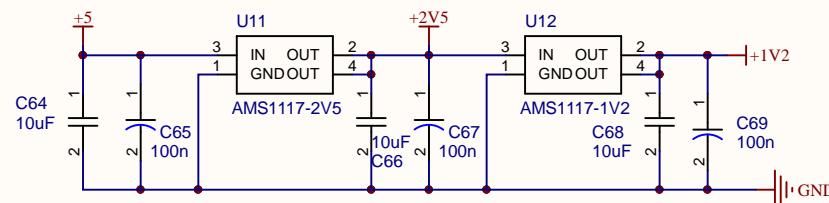
A



B



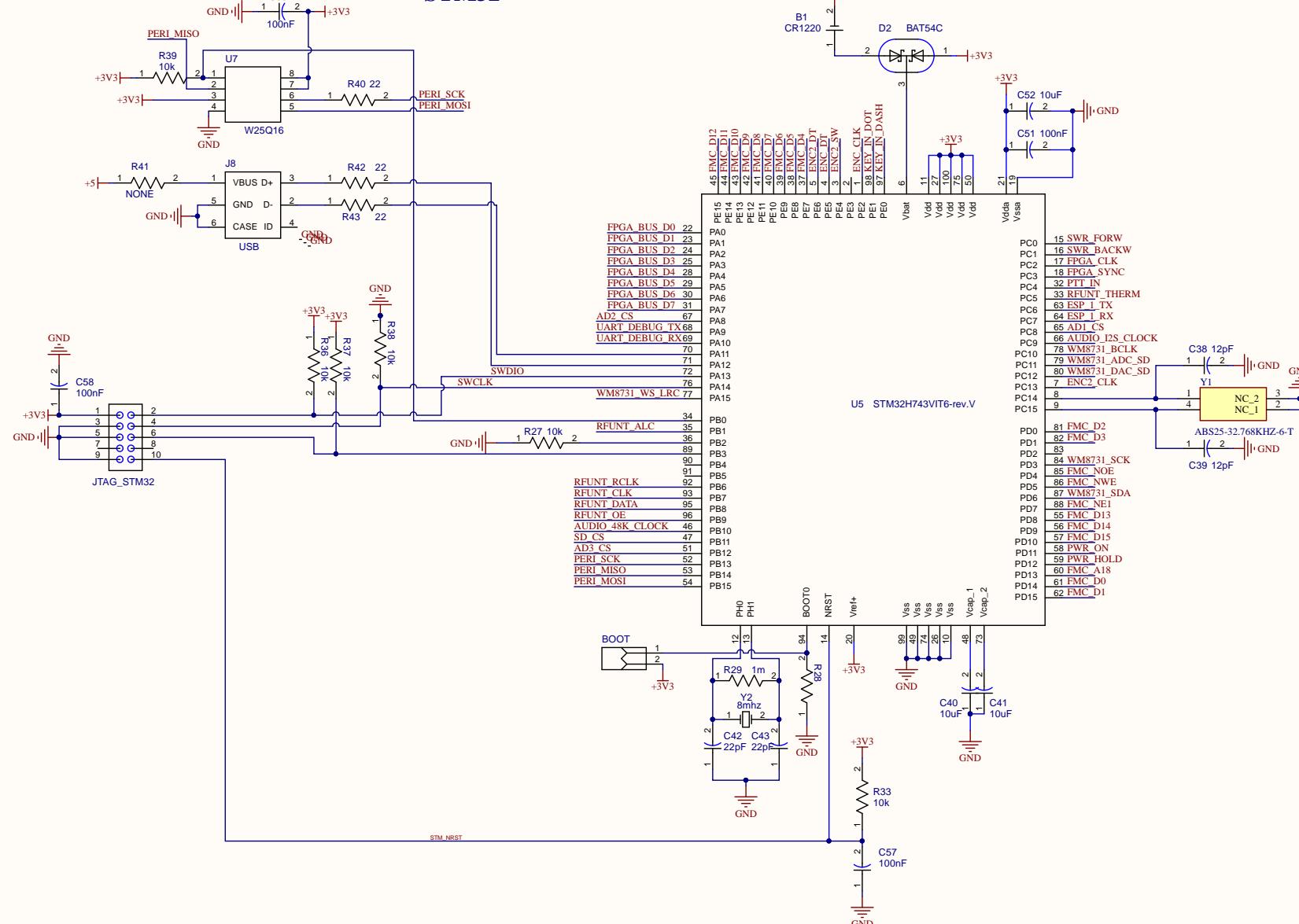
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Title **POWER**

Size: A4	Number: 10	Revision: 1.9
Date: 15.07.2020	Time: 20:01:47	Sheet 10 of 18
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# STM32



A

A

B

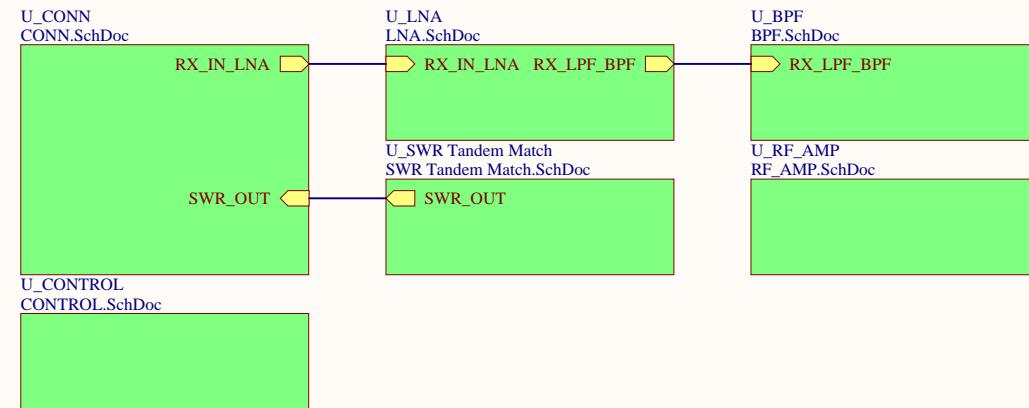
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C

C

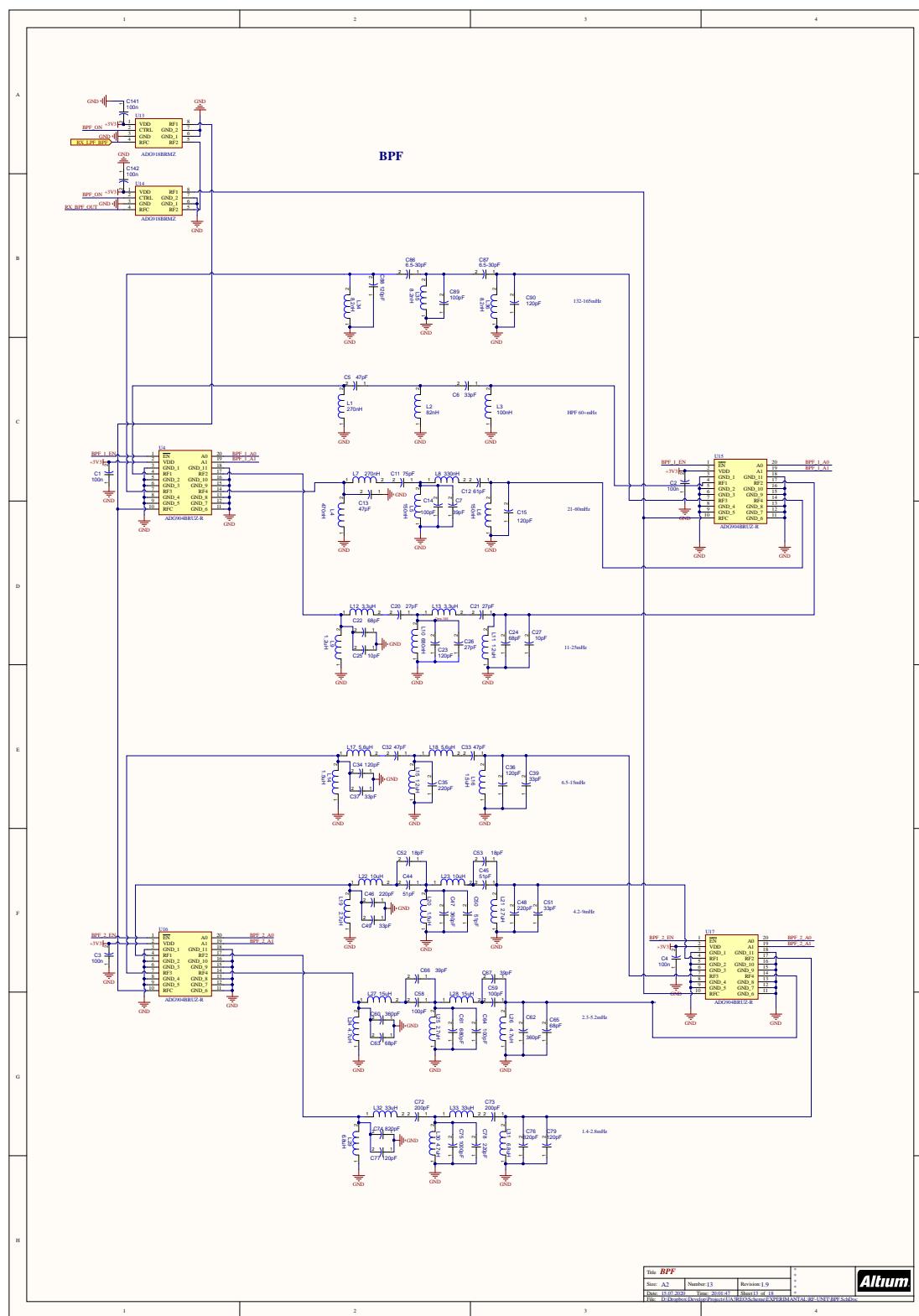
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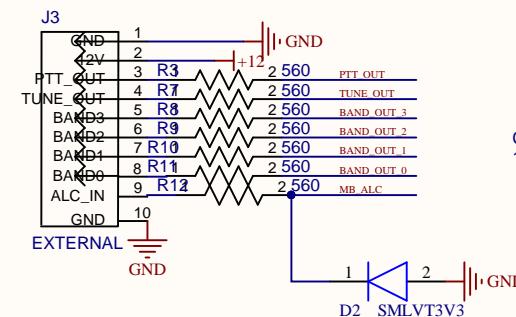
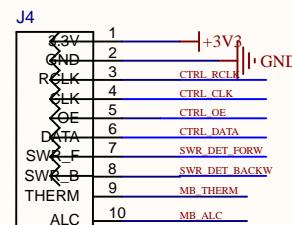
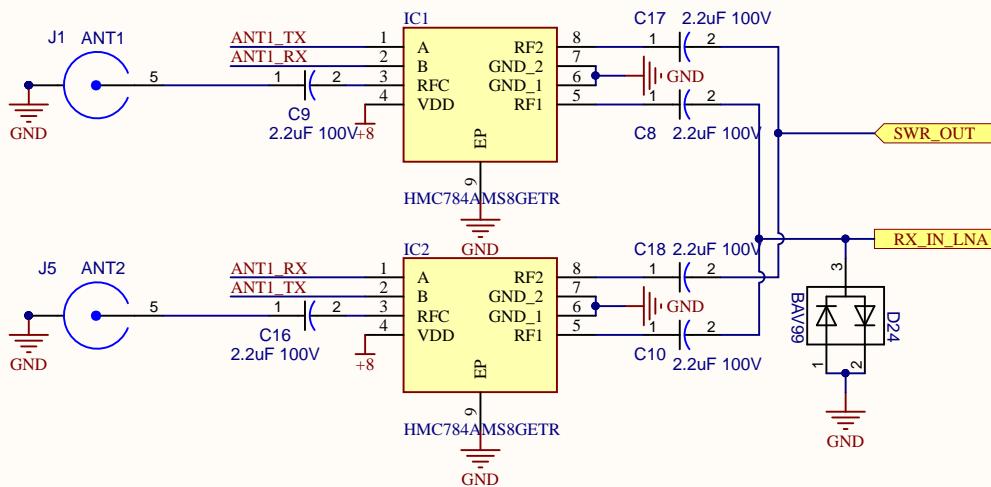


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Date: 15.07.2020	Time: 20:01:47	Sheet 12 of 18	*
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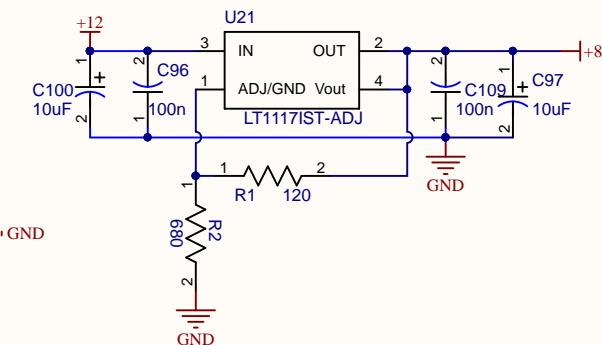
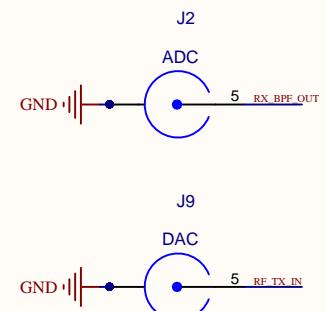
**Altium**



## TXRX\_COMUTATOR



## CONN



Title **CONN**

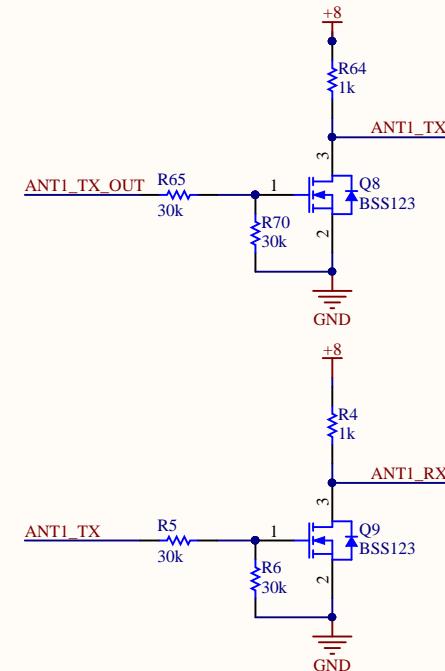
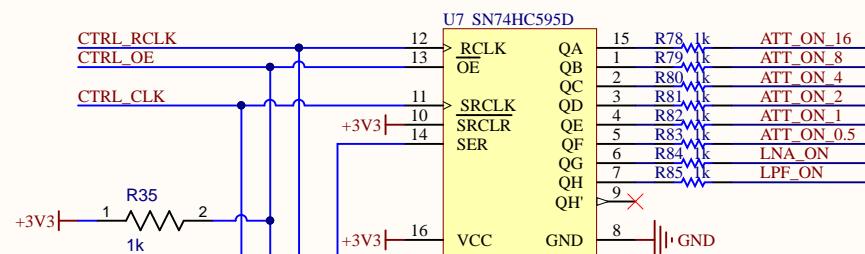
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Date: 15.07.2020 Time: 20:01:48 Sheet 14 of 18

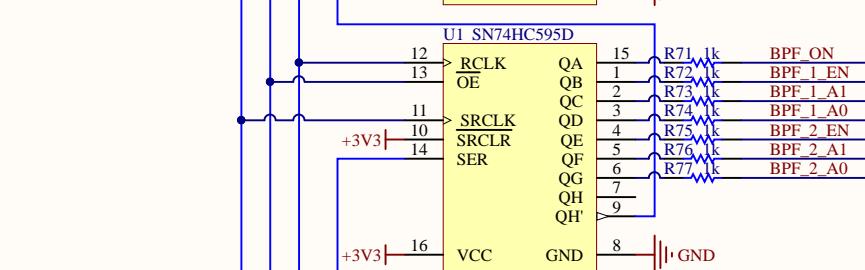
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**Altium**

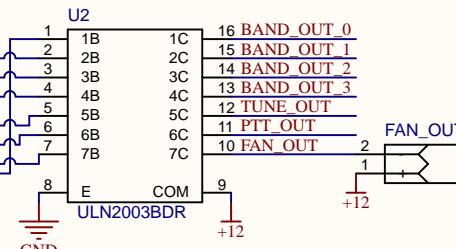
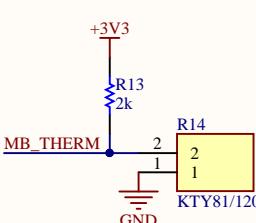
A



B

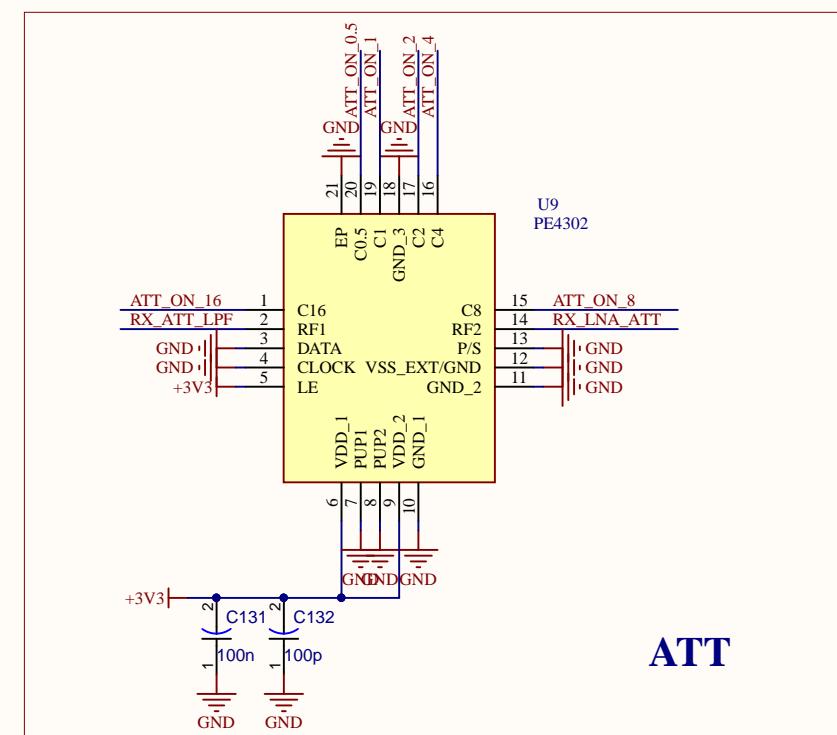
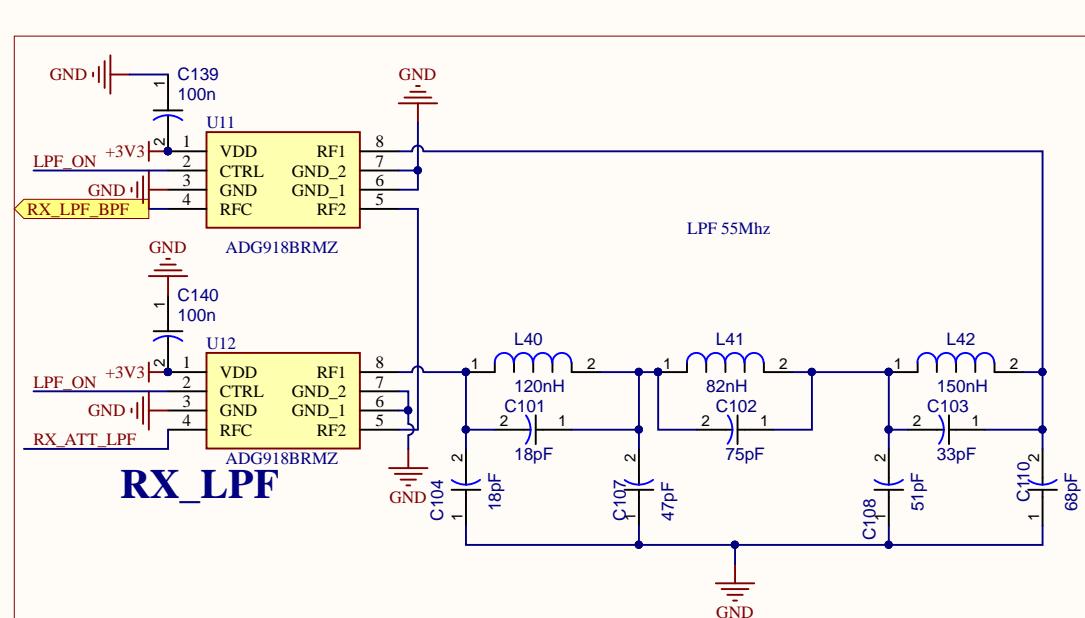
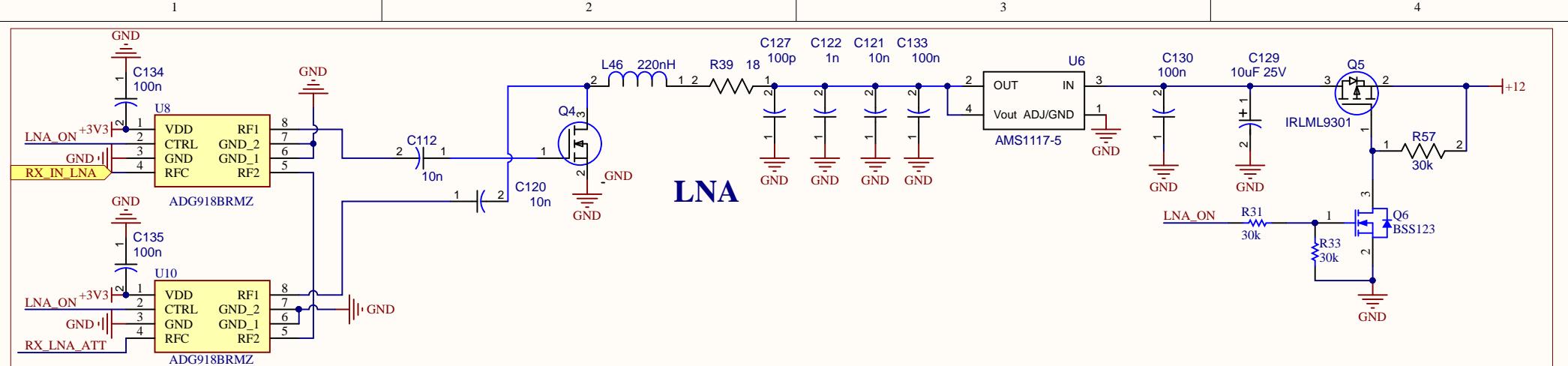


C

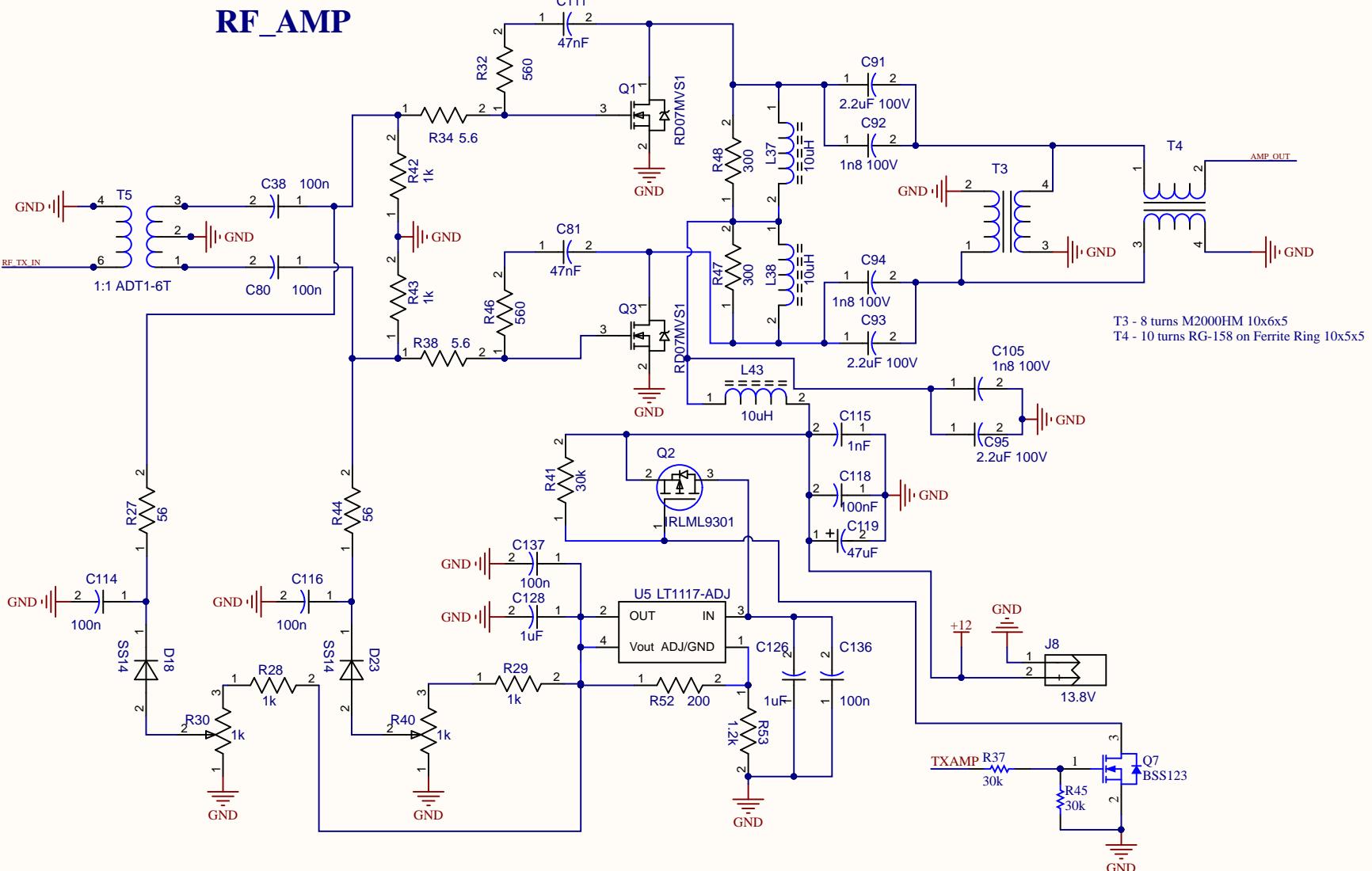


D

Title **CONTROL**Size: **A4** Number: **15** Revision: **1.9**Date: **15.07.2020** Time: **20:01:48** Sheet **15** of **18**File: **D:\Dropbox\Develop\Projects\UA3REO\Scheme\EXPERIMENTAL\RF-UNIT\CONTROL.SchDoc****Altium**



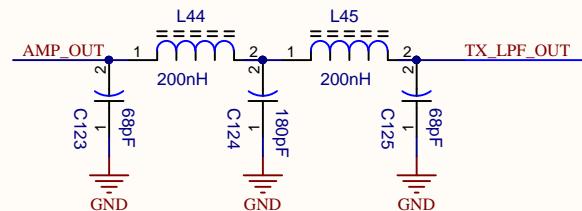
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Size: A4	Number: 16	Revision: 1.9	*	*
Date: 15.07.2020	Time: 20:01:48	Sheet 16 of 18	*	*
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Title: <b><i>RF_AMP</i></b>	*		
Size: A4	Number:17		*
Revision:1.9			*
Date: 15.07.2020	Time: 20:01:48		*
Sheet 17 of 18			
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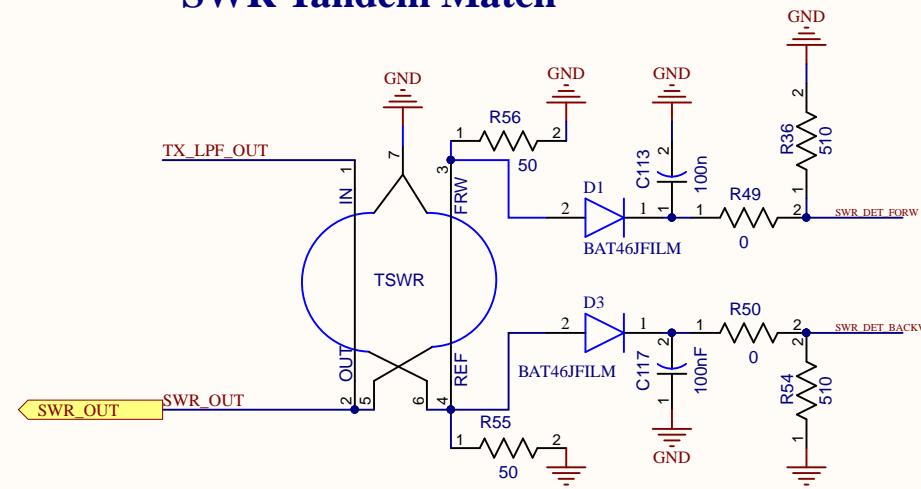
## TX\_LPF

LPF 60Mhz



Катушки намотаны проводом 0.5мм на оправке диаметром 5мм, 7 витков

## SWR Tandem Match



2 провода 0.9мм пропущено через бинокль

по диагонали пропущено и намотано по 5 витков 0.5мм

Title ***SWR Tandem Match***

Size: A4	Number: 18	Revision: 1.9
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