Name: Dopor Date: 14.Jan	ase tick (V) your campus: (DEHRADUN/BHIMTAL/HALDWANI) akon. Ahanma. Univ.Roll No2992014 Student ID2004. 12022 Course:BCA Branch: Sem.: .03 Section: ne:COA	
Que 1 (1)	Dinet SC < 0 Imitialize Dequence counter < 0	
		Jotch Wteste
	AR CPC To	Sittle
	IR - M[AR], PC-PC+1 T1	
	T ₂	(15) Derode
	Decode opcode in TR(12-14), AR ← TR(0-11), I ← IR =1 (Register/IO) \ =0 (Memory Reference)	(15) Datour
	02	maiaioh
=1 (1/0)	I =0 (register) D7 Indirect (1) I = 0 (Direct)	
	T3 T3 T3 T3 T3	Execution
I/O	Reference SC=0 AR=MLARJ T4	<u> </u>
Inatru.		
L SC ← O	Instruction sc ← 0	
Flaucha	pt for Instruction Cycle	
iamos E	to al appentially 7 sotops.	
(1) altant	SC-0 @ To: AR-PC. @ Docorle the importantion operate & Decision & Exerction	& umcre.PC
	of may amaly up ant tat early alt air elys mit	orot-run
0	i sonorg at robra, ni novabitudo ach retugman	
what		
yetch	Harma	
decode	Signature of S	tudent
execute		
1		

	Sheet for Online Examination Jan	
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Date: 14 700 Cours	M. Univ.Roll No. 2092014 St e:BCA Branch: Se	udent ID 200.41249
Subject Name: COA	Subject Code:	TOC-203 Page No
		VII A CONTROL OF THE PROPERTY
Queaz (a) dilleponre.	lectureum Marhimo language am	d Dommbly Lamanage .
Machimo Lamanaga: Th	is low level programming de	amarian habish in tanpromite
O O O	On and to The South	de la company de
10 contact under a tr	Op and so. It is the low	many language worker
As and direction to	marble to machine in form	of high and lon hopodio-
rapporting ranguage	· dovaminal tandarde la voo	meushore in lootuseen of
	low level machine Jananaa	momind losed daid loman
danguages. donom	amonna Alon Juniona	MICA LITERA MIMISORA
el alortmus brown	it not full statements to	anastructura aasaaxa
	U	
# Language Jamaura	munorut bhn at magard op	100.000
Memory Address	Mnomanica	Commont
2000	LDA 2050	
2003	MOV H.AC	AC ← [2050]
2004		H ← AC
	1DA 2051	AC ← [205]]
2007	ADD H	AC ← AC+H
2008	Mov L,AC	1-AC
2009	MUT AC 00	AC€00
200B	ADC AC	AC. + AC + CORRY
200 C	MOV H.AC	H←AC
200D	SHLD 3050	H → 3051, L → 3050
2010		3030
2010	HLT	
I've used HI pair to	ton at rebra ni aretains	let go of rapry loit
and use carry in	the result.	0 0 1
And the mamour	locations are not suppose	d Lama
to les social	some was two suppose	Signature of Student
to be exact.		Signature of Student

Name: Dopponko Date:14.Jam	Dhama Univ.Ro . Course:B.C.A	Il No. 209 2014 Student ID. 20041299 Branch: Sem.: .03 Section: Subject Code: T.BC-303 Page No
LDA A ADDR	some to add to $AC \leftarrow A$ $AC \leftarrow AC + B$ $A \leftarrow AC$	two numbers would be:

Signature of Student

Please tick (V) your campus: (DEHRADUN/BHIMTAL/HALDWANI) Name: Deeponkan Rhammuniv Roll No 2092014 Student ID . 20041299 Date: 14 Jam. Course:BCA
Subject Name:CO.A
Ques 3 (a) Addressing Modes - Tres are different usus in which torations on the property of in an instruction of the property
different types of addressing modes are:
1) Implicit / Implied iddoesaing Made - no memory reference, and data
2 - Charle in provided, like CMA, INCA
(3) Immediate Addressing Mode > doto colle is given with the instruction instead of some address eg ADD 5 [M ADD 5]
3 Direct Addressing Made -> mode Loit, (M=0), Effective Address is given
and the openend on ADDA AC = AC + [A]
3 Indirect Addressing Marle -> mode let (M=1), orderes mohore effective address
LEXII + AC + AC + LEXII
Lie atored is given na oponomid, eg. ADD X, AC ← AC+ L[X]) Beginter Addressing Mode > register is given no the approved, meass.
Effective address= Register lastest addressing mode. ADDR, AC←AC+ERJ
6) Register Indirect Actorisming Made - approand hour orders of register sholding
Effertuseradaress, uses momory reference.
Felative Addressing Mode - use displacement addressing with respect
10 the program counter, eg. PA = PC + X [address] ⊕PC → operand 8) Indexed Addressing Made → word while donling water with someonce
Indexed Addressing Made > word while dealing water with sequence data like apprays, schoping under EA (Expertise Add.) = [X]+[R]
Comptent 2 Register to i
Base Addressing Mode - [Maprode base register balue]
EA = content of Base Register + value
duto Increment/Decrement addressing modes? a constant value stored in register is incremented
was decremented from repersand to get effective signature of Student
Address
$r\Lambda = + \lceil R \rceil$

Name: Deponker Oborna Univ.Roll No2022014 Student ID 20041229 Date:14. Jam Course:BCA Branch: Sem.: .D.3 Section:	
Subject Name:	
(1) Imput Output Interface - Imput output Interface is used as a the	momenti momenti
Link which helps in transferring the information between the	<u></u>
IO Interface IO Interface	
Monitor other divides (ii) Imput Output Processor is a sprinkly	<u></u>
Deput compart Processor - Impart compart of the memory alogorations and intermediate of the memory alogorations. It inche as an impart of the memory alogorations. It inche as an impart of the memory	toplace
Idersice 1 dersice 2 I Johns	
(iii) Direct Memory Access - Direct Memory Access (DMA) is in feature of computer systems that allows restain has	duarea
DMA cam be used for copying, moving data in momory and oth similar tasks. Perspherals Data I handshake Signature of Student CPU handslake I Memory DMA Controller	CPU.
common bus	

Please tick (V) your campus: (DEHRADUN/BHIMTAL/HALDWAND) Name: Depart on Ohanna Univ Roll No. 2092014 Student ID. 20041299 Date: 14 Jam Course: BCA Branch: BCA Sem.: 3 Section: Subject Name:
Que 5 (a) Memory Nevernichy is an embancement in computer system
Design and organization to organize the momory such
that it can minimize the access time. The memory shourarchy
do developed based on a program lockations know as
dorality of referencea. CPU Registers 10000
Loot per unit increasing cache Memory (SRAMA) Lovel 1
Dynamic RAM -> Main Memory D(RAMS) 101102
Jastness Magnetic Diska (Disk Alonge) Lovel 3
0 0
- capacity, more necess time Louel lower Livels - Processor Registers
This memory heironchy is divided D/ cache > 4 livels
unto two main types: 2/Main Memore > DRAM
(1) Extermal Momany / Decompany
Memory - comprise magnetic 4/ Nearline storage (Testinger)
Whore pripresses observed dilling of office &
2) Internal Memory Primary Memory > It comprises of main memory
cache and CPU registers It comprises of main momony
supporte al Momon Haranday
characteratica of Memory Heirarchy (i) capacity → alolal valume almomory
(i) capacity → global volume of momory, increases at tower levels (h, 9) (ii) Access Time > I/O time period, uncreases at higher town levels where memory is
(11) Access Time > I/O time period, uncreases at
higher the down levels where memory is form
Mollium Signature of Student
(iii) cost per let > coat occurred to store one let, increases toward lower
levels, hence CPU registers are very arranging