Address Sequencing :→

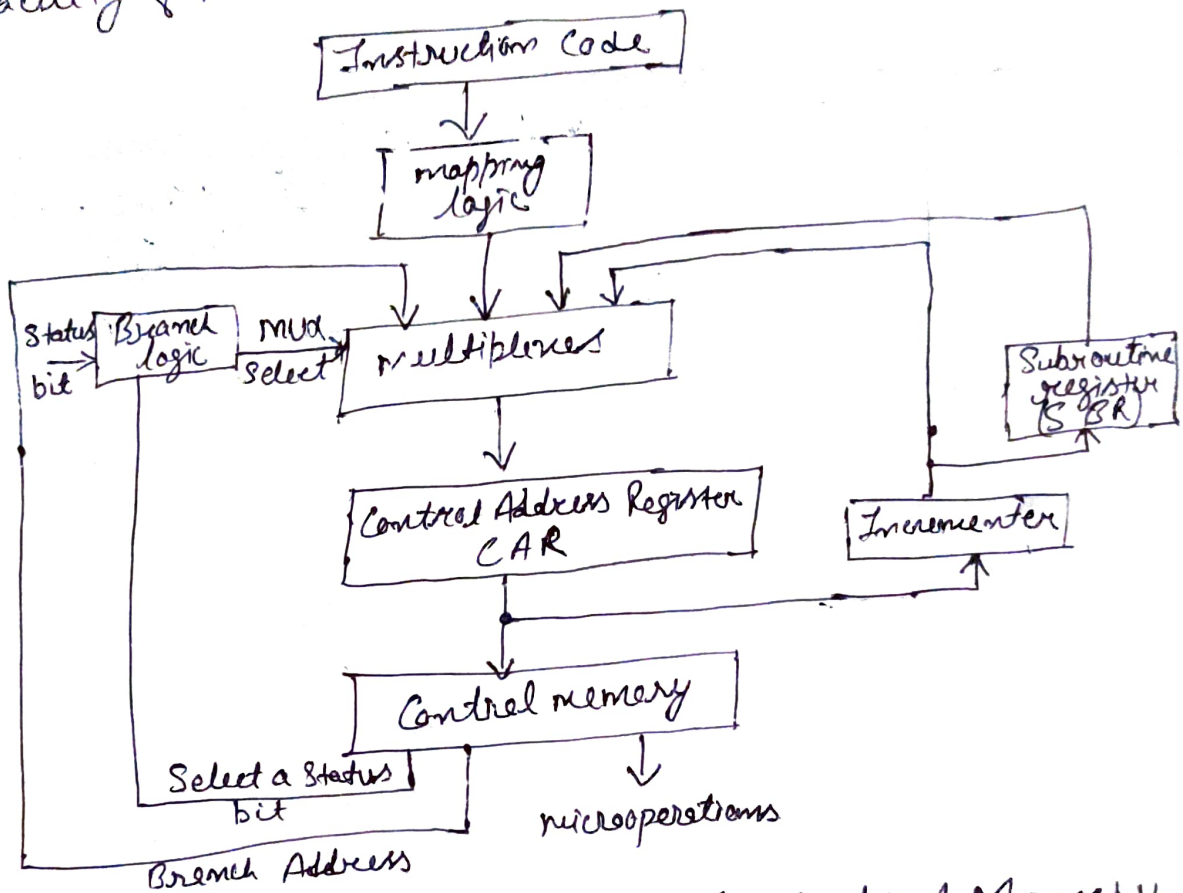
* Each instruction has its own microprogram routine stored in a given fixed location in the control memory to generate micro operations that execute the instructions.
* The hardware that controls the address sequencing of the control memory must be capable of sequencing the micro-instructions within a sub-routine and also be able to branch from one routine to another.
* An initial address that is the address of the first micro-instruction that activates the instruction fetch routine is loaded into the CAR, when the power is turned ON in the computer.
* The fetch routine in the sequence by incrementing the control address register to the rest of its micro-instructions. At the end of the fetch routine, the instruction is in the instruction register of the computer.
* The control memory must next go to the routine that determines the effective address of the operand which can be reached through branch micro-operation based on the bits of the instruction. when the effective address computation routine is completed. The address of the operand is available in the Memory Address register.
* The next step is to generate micro-operations that execute the instruction fetched from the memory. The micro-operations step to be generated in the processor registers depends on the operational code part of the instruction.

The address capability sequences required in the control memory are:-

(a) Incrementing the CAR
(b) Unconditional branch or conditional branch, depending on the status bit conditions.
(c) A mapping from the instruction code bits of the instructions to an address for the control memory, where the micro-program routine is located in the memory.

(mapping procedure is such, that transforms the instruction code to control memory address)

(d). facility for Subroutine call & return.



Selection of Address for Control Memory

The diagram shows four different paths from which the CAR receives the address.

1). The incrementer increments the content of the control address register by 1 to select the next microoperation in sequence.

2). Branching is achieved by specifying the branch address in one of the field of micro-operation.

3). Conditional branching is obtained by using a part of the micro-instruction to select the specific status bit.

4). An external address is transferred into the control memory via mapping logic circuit.

5). The return address for a subroutine is stored in a special register called Sub-routine register (SBR). for storing the return address during a SBR call and restoring the address during a SBR return.

Microprogram Example :→

To Generate the microcode for the Control memory is called microprogramming and is a Process Similar to conventional machine language Programming. To appreciate this Process, we study here a simple digital Computer.

Computer Configuration :→ The Basic digital Computer Consist of two memory unit :-

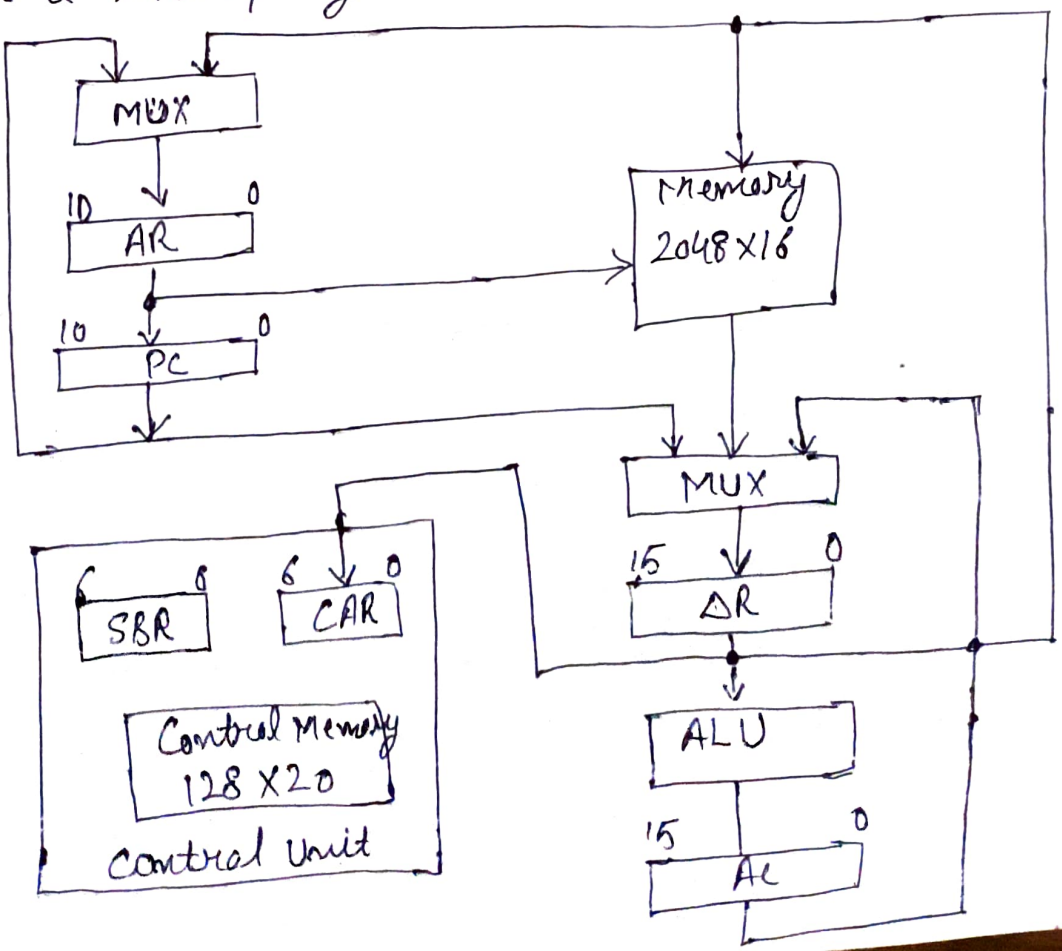
(a) Main Memory for storing instructions and data.

(b) Control Memory for storing the microprogram.

*. Four Registers PC (Program Counter), address register AR, data register DR, and accumulator register AC, are associated with Processor unit.

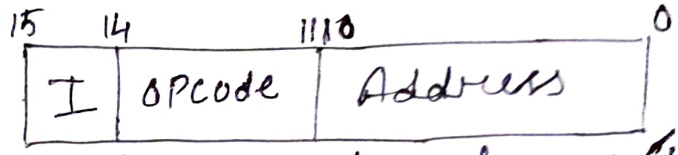
* Two registers CAR (control address register) and SBR Subroutine register are associated with Control Unit.

*. The Control memory and its registers are organized as a microprogrammed Control unit.

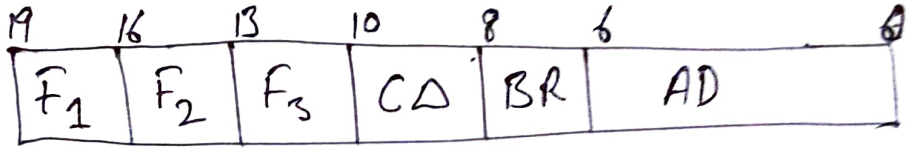


* DR can receive information from AC, PC or memory.
* AR can receive information from PC or DR. PC can receive information only from AR.
* The arithmetic, logic, and shift unit performs micro-operations with data from AC and DR and places the result in AC.

Computer Instructions:-



(a) Instruction format (16-bits)



F_1, F_2, F_3 : Microoperation fields
CD : Condition for branching
BR : Branch field
AD : Address field.

(b) Microinstruction code format (20-bits)

Symbols and Binary Code for Microinstruction fields:-

F_i	Microoperation	Symbol
000	None	NOPE (No operation)
001	AC ← AC + DR	ADD
010	AC ← 0	CLRAC (Clear AC)
011	AC ← AC + 1	INC AC (Increment AC)
100	AC ← DR	DRTAC (DR copy to AC)
101	AR ← DR (0-10)	DRTAR (DR copy to AR)
110	AR ← PC	PCTAR (PC copy to AR)
111	M[AR] ← DR	WRITE