4.19.4 DDR4 DIMM Label

1 Scope

The following labels shall be applied to all DDR4 memory modules to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggg, are to be omitted when not needed.

2 DDR4 DIMM Label Format for DRAM-only module types

ggg**GB** phe**Rx**ff **PC4**s**-**wwwwaa**-**mccd**-**bb

Where:

ggg**GB** = Module total capacity, in gigabytes, for primary bus (ECC not counted)
1GB, 2GB, 4GB, etc. (no space between digits and units)

phe**R** = Number of package ranks of memory per DIMM and number of logical ranks per package rank.

p =
1 = 1 package rank of SDRAMs per DIMM
2 = 2 package ranks of SDRAMs per DIMM
3 = 3 package ranks of SDRAMs per DIMM
4 = 4 package ranks of SDRAMs per DIMM

h = blank for monolithic DRAMs (SDP), else for modules using stacked DRAM:
h = DRAM package type
D = Dual die multi-load DRAM stack (DDP)
Q = Quad die multi-load DRAM stack (QDP)
S = Single load DRAM stacking (3DS)

e = blank for SDP, DDP, or QDP, else for modules using 3DS stacks, logical ranks per package rank
2 = 2 logical ranks in each package rank
4 = 4 logical ranks in each package rank
8 = 8 logical ranks in each package rank

R = rank(s)

xff = Device organization (data bit width) of SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
x16 = x16 organization

s = SDRAM operational scaling
blank = DDR4
E = DDR4E with operational scaling

wwww = Module speed in Mb/s/data pin
1600
1866
2133
2400
2666

2933
3200

aa = SDRAM speed grade

aa = Speed grade, i.e., J, K, L, etc. (See JESD79-4 and 3DS Addendum specifications for details)
Examples:

DDR4 Monolithic Components				
Letter	Speed Grade	CAS Latency	tRCD in nCK	tRP in nCK
J	All	10	10	10
K	All	11	11	11
L	All	12	12	12
M	All	13	13	13
N	All	14	14	14
P	All	15	15	15
R	All	16	16	16
T	All	17	17	17
U	All	18	18	18
V	All	19	19	19
W	All	20	20	20
Y	All	21	21	21
AA	All	22	22	22
AC	All	24	24	24

DDR4 3DS Stacked Single-Load Components				
Letter	Speed Grade	CAS Latency	tRCD in nCK	tRP in nCK
J	All	12	11	10
K	All	13	12	11
L	All	14	13	12
M	All	15	14	13
N	All	16	15	14
P	2133P-3DS2A	17	15	15
P	2133P-D 3DS2A	17	15	15
P	2133P-3DS3A	18	15	15
P	2400P-3DS3B	18	16	15
R	All	20	16	16
T	2400T-3DS2A	19	17	17

DDR4 3DS Stacked Single-Load Components (Cont'd)				
Letter	Speed Grade	CAS Latency	tRCD in nCK	tRP in nCK
T	2666T-3DS3A	20	17	17
U	2400U-3DS2A	20	18	18
U	2400U-3DS4A	22	18	18
U	2400U-D 3DS4A	22	18	18
V	All	22	19	19
W	All	24	20	20
AA	All	26	22	22
AC	All	28	24	24

m = Module Type
- A = Unbuffered 16-bit Small Outline DIMM ("16b-SO-DIMM"), x16 data bus (*placeholder*)
- B = Unbuffered 32-bit Small Outline DIMM ("32b-SO-DIMM"), x32 data bus (*placeholder*)
- C = Registered 72-bit Small Outline DIMM ("72b-SO-RDIMM"), x64 primary + 8 bit ECC module data bus (*placeholder*)
- E = Unbuffered DIMM ("UDIMM"), x64 primary + 8 bit ECC module data bus
- L = Load Reduced DIMM ("LRDIMM"), x64 primary + 8 bit ECC module data bus
- N = Mini registered DIMM ("Mini-RDIMM"), x64 primary + 8 bit ECC module data bus
- R = Registered DIMM ("RDIMM"), x64 primary + 8 bit ECC module data bus
- S = Small Outline DIMM ("SO-DIMM"), no ECC (x64 bit module data bus)
- T = Unbuffered 72-bit Small Outline DIMM ("72b-SO-DIMM"), x64 primary + 8 bit ECC module data bus
- U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
- W = Mini unbuffered DIMM ("Mini-UDIMM"), x64 primary + 8 bit ECC module data bus

cc = Reference design file used for this design (if applicable)
- A = Reference design for raw card 'A' is used for this assembly
- B = Reference design for raw card 'B' is used for this assembly
- AC = Reference design for raw card 'AC' is used for this assembly
- ZZ = None of the JEDEC standard reference designs were used for this assembly

d = Revision number of the reference design used (see table below)
- 0~9 = Production release revisions
- A~K = Pre-production releases (new method -- preferred)
- P = Pre-release or Engineering sample (for legacy modules; new modules should use A~K)
- Z = To be used when field cc = ZZ

bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM

As modules are developed in JEDEC, samples of pre-standard approval designs are often distributed for evaluation. Legacy DIMM labels allowed for a single pre-production indicator 'P' in the d field, and determining the specific board revision required reading the module SPD. This is replaced in newer modules with using the first letter in the cc field to indicate which raw card revision the pre-production module represents. For pre-production modules, a letter is used in the 'd' field in place of the target

production level:

Production Levels		
DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
A	0	Raw card revision 0
B	1	Raw card revision 1
C	2	Raw card revision 2
D	3	Raw card revision 3
E	4	Raw card revision 4
F	5	Raw card revision 5
G	6	Raw card revision 6
H	7	Raw card revision 7
J	8	Raw card revision 8
K	9	Raw card revision 9
P	-	Legacy pre-production indicator; production revision documented in module SPD
Z	Z	Non-standard design

Legacy DIMM labels allowed for a single pre-production indicator in the d field, and determining the specific board revision required reading the module SPD. This is replaced in newer modules with using the first character in the cc field to indicate which raw card revision the pre-production module represents.

Pre-Production Example: A hypothetical release cycle of a raw card F, for example, may proceed like this:

ccd = FA Pre-production sample of raw card F0

ccd = F0 Production F0 module

ccd = FB Pre-production sample of raw card F1

ccd = F1 Production F1 module

Examples:

16GB 2Rx4 PC4-2133N-RA2-11

16 GB DDR4 RDIMM (72 bit data bus)
2 package ranks per DIMM
using SDP DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade N: CAS Latency = 14
Raw card reference design file A revision 2 used for the assembly
DDR4 SPD revision 1.1

16GB 2DRx4 PC4-2133N-RJ0-10

16 GB DDR4 RDIMM (72 bit data bus)

2 package ranks per DIMM
using DDP multi-load stacked DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade N: CAS Latency = 14
Raw card reference design file J revision 0 used for the assembly
DDR4 SPD revision 1.0

16GB 1S2Rx4 PC4-2133N-RF1-10
16 GB DDR4 VLP RDIMM (72 bit data bus)
1 package rank per DIMM
with 2 logical ranks per package rank
using 2H 3DS single-load stacked DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade N: CAS Latency = 14
Raw card reference design file F revision 1 used for the assembly
DDR4 SPD revision 1.0

32GB 2DRx8 PC4-2400U-UZZZ-11
32 GB DDR4 UDIMM (64 bit data bus)
2 package ranks per DIMM
using DDP multi-load stacked DDR4 SDRAMs
x8 data organization per SDRAM
DDR4-2400 performance
Speed grade U: CAS Latency = 18
Non-JEDEC standard design used for the assembly
DDR4 SPD revision 1.1

16GB 1S4Rx4 PC4-2133R-LZZZ-10
16 GB DDR4 LRDIMM
1 package rank per DIMM
with 4 logical ranks per package rank
using 4H 3DS single-load stacked DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade R: CAS Latency = 16
Non-JEDEC design used for the assembly
DDR4 SPD revision 1.0

16GB 1S2Rx4 PC4-2133N-RFC-10
16 GB DDR4 VLP RDIMM (72 bit data bus)
1 package rank per DIMM
with 2 logical ranks per package rank
using 2H 3DS single-load stacked DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade N: CAS Latency = 14
Pre-production engineering sample of raw card reference design file F revision 2 used for the assembly
DDR4 SPD revision 1.0

32GB 2DRx8 PC4E-2400U-UZZZ-11
32 GB DDR4E UDIMM (64 bit data bus)
2 package ranks per DIMM
using DDP multi-load stacked DDR4 SDRAMs

x8 data organization per SDRAM
DDR4E-2400 performance with operational scaling
Speed grade U: CAS Latency = 18
Non-JEDEC standard design used for the assembly
DDR4 SPD revision 1.1

16GB 1S4Rx4 PC4E-2133R-LZZZ-10
16 GB DDR4E LRDIMM
1 package rank per DIMM
with 4 logical ranks per package rank
using 4H 3DS single-load stacked DDR4 SDRAMs
x4 data organization per SDRAM
DDR4E-2133 performance with operational scaling
Speed grade R: CAS Latency = 16
Non-JEDEC design used for the assembly
DDR4 SPD revision 1.0

3 DDR4 DIMM Label Format for Hybrid memory module types

"System accessible memory" refers to media that is available for use by the system. For NVDIMM-N this refers to the DRAM capacity. For NVDIMM-H, this refers to the usable Flash capacity. For NVDIMM-P, this refers to the guaranteed Host accessible volatile or non-volatile capacity.

Hybrid modules appear to the system with a "base module type" compatible interface. For example, an NVDIMM-N may be constructed with an RDIMM-style interface or an LRDIMM-style interface. What specific functions the module provides are described in an "Hybrid Media Type" field ('n'), essentially a functional overlay on the base module type.

DDR4 DIMM labels for Hybrid memory modules contain four required sections: a module type section, a technical detail section, a serial number section, and a machine-readable section. The first three sections are recommended in order on the label, but the 4th section, machine readable, may be placed anywhere it fits on the label.

Legacy hybrid memory module labels required the technical detail section only.

3.1 Module Type Section

DDR4 dimm_type

Where:

dimm_type = one of:

NVUDIMM-N			
NVRDIMM-N	NVRDIMM-H	NVRDIMM-P	NVRDIMM-PL
NVLRDIMM-N	NVLRDIMM-H	NVLRDIMM-P	NVLRDIMM-PL

3.2 Technical Detail Section

ggg**GB** phe**Rx**ff **N**nn**4**s-wwwwaa-mccd-bb

Where:

ggg = Module total capacity, in gigabytes, for system accessible DRAM on primary bus (ECC not

counted)
ggg: natural numbers

GB = Gigabytes of module capacity; may be **TB** for terabytes

phe**R** = Number of package ranks of memory per DIMM and number of logical ranks per package rank.

p =
1 = 1 package rank of SDRAMs per DIMM
2 = 2 package ranks of SDRAMs per DIMM
3 = 3 package ranks of SDRAMs per DIMM
4 = 4 package ranks of SDRAMs per DIMM

h = blank for monolithic DRAMs (SDP), else for modules using stacked DRAM:

h = DRAM package type
D = Dual die multi-load DRAM stack (DDP)
Q = Quad die multi-load DRAM stack (QDP)
S = Single load DRAM stacking (3DS)

e = blank for SDP, DDP, or QDP, else for modules using 3DS stacks, logical ranks per package rank

2 = 2 logical ranks in each package rank
4 = 4 logical ranks in each package rank
8 = 8 logical ranks in each package rank

R = rank(s)

xff = Device organization (data bit width) of SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
x16 = x16 organization

N = NVDIMM

nn = NVDIMM type
N = persistent DRAM using NAND flash
H = NAND flash accessed as a block cached, byte addressable device
P = transactional credit based device
PL = transactional credit based device, lightweight protocol

s = SDRAM operational scaling
blank = DDR4
E = DDR4E with operational scaling

wwww = Module speed in Mb/s/data pin
1600
1866
2133
2400
2666
2933
3200

aa = SDRAM speed grade
aa = Speed grade, i.e., J, K, L, etc.

Examples:

DDR4 Monolithic Components				
Letter	Speed Grade	CAS (SEND) Latency	tRCD in nCK	tRP in nCK
J	All	10	10	10
K	All	11	11	11
L	All	12	12	12
M	All	13	13	13
N	All	14	14	14
P	All	15	15	15
R	All	16	16	16
T	All	17	17	17
U	All	18	18	18
V	All	19	19	19
W	All	20	20	20
Y	All	21	21	21
AA	All	22	22	22
AC	All	24	24	24
Note: For NVDIMM-P and NVDIMM-PL, SEND latency is defined; tRCD and tRP are not				

DDR4 3DS Stacked Single-Load Components				
Letter	Speed Grade	CAS (SEND) Latency	tRCD in nCK	tRP in nCK
J	All	12	11	10
K	All	13	12	11
L	All	14	13	12
M	All	15	14	13
N	All	16	15	14
P	2133P-3DS2A	17	15	15
P	2133P-D 3DS2A	17	15	15
P	2133P-3DS3A	18	15	15
P	2400P-3DS3B	18	16	15
R	All	20	16	16
T	2400T-3DS2A	19	17	17
T	2666T-3DS3A	20	17	17

DDR4 3DS Stacked Single-Load Components (Cont'd)				
Letter	Speed Grade	CAS (SEND) Latency	tRCD in nCK	tRP in nCK
U	2400U-3DS2A	20	18	18
U	2400U-3DS4A	22	18	18
U	2400U-D 3DS4A	22	18	18
V	All	22	19	19
W	All	24	20	20
AA	All	26	22	22
AC	All	28	24	24
Note: For NVDIMM-P and NVDIMM-PL, SEND latency is defined; tRCD and tRP are not				

m = Base Module Type
- A = Unbuffered 16-bit Small Outline DIMM ("16b-SO-DIMM"), x16 data bus (*placeholder*)
- B = Unbuffered 32-bit Small Outline DIMM ("32b-SO-DIMM"), x32 data bus (*placeholder*)
- C = Registered 72-bit Small Outline DIMM ("72b-SO-RDIMM"), x64 primary + 8 bit ECC module data bus (*placeholder*)
- E = Unbuffered DIMM ("UDIMM"), x64 primary + 8 bit ECC module data bus
- L = Load Reduced DIMM ("LRDIMM"), x64 primary + 8 bit ECC module data bus
- N = Mini registered DIMM ("Mini-RDIMM"), x64 primary + 8 bit ECC module data bus
- R = Registered DIMM ("RDIMM"), x64 primary + 8 bit ECC module data bus
- S = Small Outline DIMM ("SO-DIMM"), no ECC (x64 bit module data bus)
- T = Unbuffered 72-bit Small Outline DIMM ("72b-SO-DIMM"), x64 primary + 8 bit ECC module data bus
- U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
- W = Mini unbuffered DIMM ("Mini-UDIMM"), x64 primary + 8 bit ECC module data bus

cc = Reference design file used for this design (if applicable)
- A = Reference design for raw card 'A' is used for this assembly
- B = Reference design for raw card 'B' is used for this assembly
- AC = Reference design for raw card 'AC' is used for this assembly
- ZZ = None of the JEDEC standard reference designs were used for this assembly

d = Revision number of the reference design used (see table below)
- 0~9 = Production release revisions
- A~K = Pre-production releases (new method -- preferred)
- P = Pre-release or Engineering sample (for legacy modules; new modules should use A~K)
- Z = To be used when field cc = ZZ

bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM

As modules are developed in JEDEC, samples of pre-standard approval designs are often distributed for evaluation. Legacy DIMM labels allowed for a single pre-production indicator 'P' in the d field, and determining the specific board revision required reading the module SPD. This is replaced in newer modules with using the first letter in the cc field to indicate which raw card revision the pre-production module represents. For pre-production modules, a letter is used in the 'd' field in place of the target production level

:

Production Levels		
DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
A	0	Raw card revision 0
B	1	Raw card revision 1
C	2	Raw card revision 2
D	3	Raw card revision 3
E	4	Raw card revision 4
F	5	Raw card revision 5
G	6	Raw card revision 6
H	7	Raw card revision 7
J	8	Raw card revision 8
K	9	Raw card revision 9
P	-	Legacy pre-production indicator; production revision documented in module SPD
Z	Z	Non-standard design

Legacy DIMM labels allowed for a single pre-production indicator in the d field, and determining the specific board revision required reading the module SPD. This is replaced in newer modules with using the first character in the cc field to indicate which raw card revision the pre-production module represents.

Pre-Production Example: A hypothetical release cycle of a raw card F, for example, may proceed like this:

ccd = FA Pre-production sample of raw card F0

ccd = F0 Production F0 module

ccd = FB Pre-production sample of raw card F1

ccd = F1 Production F1 module

3.3 Serial Number Section

SN:serialnumber

Where:

serialnumber = unique module serial number per ACPI specification; see uefi.org/acpi for details
<vid><mfgloc><mfgdate><serial> (Format %02x%02x%02x%02x%02x%02x%02x%02x%02x%02x)
where

<vid> = DIMM Vendor ID, 4 characters (SPD bytes 320, 321)
<mfgloc> = Manufacturing location, 2 characters (SPD byte 322)
<mfgdate> = Manufacturing date, 2 characters for year (SPD byte 323),
2 characters for week (SPD byte 324)
<serial> = Unique serial number assigned by manufacturer, 8 characters (SPD bytes 325~328)

3.4 Part Number Section

PN:partnumber

Where:

partnumber = module part number (SPD bytes 329~348)

3.5 Physical Presence Security Identifier Section

PSID:psid

Where:

psid = Physical Presence Security ID, exactly 32 printable characters
as defined by the Trusted Computing Group Storage Opal SSC Feature Set: PSID specification; see trustedcomputinggroup.org for details

This field is required for hybrid modules that incorporate self-encryption to allow data recovery.

3.6 Machine Readable Section

2d_barcode

Where:

2d_barcode follows DataMatrix ECC 200; see ISO/IEC 16022 for details; characters coded per ISO 8859-1

The size of the DataMatrix is not specified, but must contain sufficient data encoding space for at least the following textual information:

(L)technicaldetails(S)serialnumber(P)partnumber or

(L)technicaldetails(S)serialnumber(P)partnumber(K)psid for modules supporting self-encryption

Where:

technicaldetails, serialnumber, partnumber, and psid are as defined in the above specification sections.

The serialnumber field is exactly 18 characters long.

The partnumber field must include all 20 characters from SPD bytes 329~348 including leading or trailing space characters.

The psid field, when included, is exactly 32 characters long.

No whitespace characters (space, newline, etc.) are permitted in the barcode in the required JEDEC fields except as described above for the partnumber field.

Other fields are permitted in the machine readable 2D barcode, and each section must start with (x) where x is a single section delineation character. Upper case characters (A-Z) in section delineation are reserved for JEDEC definition, lower case characters (a-z) may be used for supplier specific information.

Delineated sections of the barcode may be in any order.

Examples:

DDR4 NVRDIMM-N
16GB 2Rx4 NN4-2133N-RA2-12
SN:802C26160112345678
PN:MTA12ASF2G72PA-4H4A0

16 GB DDR4 SDRAM with no system accessible Flash
DDR4 RDIMM-compatible interface NVDIMM-N
2 package ranks per DIMM
using SDP DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-2133 performance
Speed grade N: CAS Latency = 14
Raw card reference design file A revision 2 used for the assembly
DDR4 SPD revision 1.2
Manufacturer code 80 2C
Manufacturing location 26 (vendor specific)
Manufacturing date 2016 week 01
Unique product serial number 12345678
Part number MTA12ASF2G72PA-4H4A0
No PSID key
Barcode text
(L)16GB 2Rx4 NN4-2133N-RA2-12(S)802C-1601-26-12345678(P)MTA12ASF2G72PA-4H4A0

DDR4 NVLRDIMM-H
1TB 1Rx4 NH4-1866M-LB1-12
SN:078501171678123456
PN:DTINF4-1TF18Z2A

1 TB NAND Flash-only, no system accessible DRAM
DDR4 LRDIMM-compatible interface NVDIMM-H
Appears as 1 package rank per DIMM
of SDP DDR4 SDRAMs
x4 data organization per SDRAM
DDR4-1866 performance
Speed grade M: CAS Latency = 12
Raw card reference design file B revision 1 used for the assembly
DDR4 SPD revision 1.2
Manufacturer code 07 85
Manufacturing location 01 (vendor specific)
Manufacturing date 2017 week 16

Unique product serial number 78123456
Part number DTINF4-1TF18Z2A
No PSID key
Barcode text
(L)1TB 1Rx4 NH4-1866M-LB1-12(S)0785-01-1716-78123456(P)DTINF4-1TF18Z2A*(+5 spaces)*

DDR4 NVRDIMM-P
16GB 1Rx4 NP4-2133N-RA2-12
SN:80CE03172256781234
PN:XIT16G32GPR4A1

16 GB mounted as a transactional oriented device
DDR4 RDIMM-compatible interface NVDIMM-P
1 chip select signal used
x4 data organization
DDR4-2133 performance
Speed grade N: SEND Latency = 14
Raw card reference design file A revision 2 used for the assembly
DDR4 SPD revision 1.2
Manufacturer code 80 CE
Manufacturing location 03 (vendor specific)
Manufacturing date 2017 week 22
Unique product serial number 56781234
Part number XIT16G32GPR4A1
No PSID key
Barcode text
(L)16GB 1Rx4 NP4-2133N-RA2-12(S)80CE-03-1722-56781234(P)XIT16G32GPR4A1