JEDEC
STANDARD

DDR5 RDIMM Standard Annex C

JESD305-R8-RCC
Version 1.0

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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(From JEDEC Board Ballet JCB-21-35, formulated under the cognizance of the JC-45.1 Subcommittee on registered DRAM modules, item 2273.12.)

1   Scope

This standard, JESD305-R8-RCC, DDR5 Registered Dual Inline Memory Module with 8-bit ECC (EC8 RDIMM) Raw Card C Annex, defines the design detail of x4, 1 Package Rank DDR5 RDIMM with 8-bit ECC. The common feature of DDR5 RDIMM, such as the connector pinout, can be found in the JESD305, DDR5 Load Reduced (LRDIMM) and Registered Dual Inline Memory Module (RDIMM) Common Standard.

2   DDR5 Registered DIMM Design File

Table 1 — DDR5 Registered DIMM Design File

Raw card	Applicable Design File	Applicable BOM
C0	PC5-RDIMM_RC_C0_R100_20210702.brd	PC5-RDIMM_RC_C0_R100_20210702_BOM.xlsx
NOTE 1	"Reference" design file updates will be released as needed. This DIMM standard will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.	

3   Module Configuration

Table 2 — Module Configuration

SDRAM					DIMM											
Die Density	Die Organi-zation	Pack-age Type	# of Logical Ranks [1,2] per PKG. Rank		# of PKG. Rank 1,2 per DIMM	# of Logical Ranks [1,2] per DIMM		# of SDRAM Die per DIMM		Capacity per DIMM (GB)		DIMM organization		# of Address Bits Row/Col	MO-329 Variation
			Min.	Max.		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
16Gb	4G x 4	SDP	-	-	1	1	1	20	20	32	32	4Gx80	4Gx80	16/11	AAxx
		3DS	2	8	1	2	8	40	160	64	256	8Gx80	32Gx80		
24Gb	6G x 4	SDP	-	-	1	1	1	20	20	48	48	6Gx80	6Gx80	17/11	AAxx
		3DS	2	8	1	2	8	40	160	96	384	12Gx80	48Gx80		

NOTE 1   When populated with single die package (SDP), package ranks per DIMM = 1.
NOTE 2   When populated with single load stacked packages (3DS), logical ranks per package rank = 2-8. Logical ranks per DIMM = 2-8.

4   SDRAM Configuration

Table 3 — SDRAM Configuration

Raw Card	Supported DRAM Outline (Width x Length) max. (mm)	# of Bank Groups/ Banks in a Group	SDRAM Package Type	Package Type	MO-210 Variation
C0	10.1 x 11.1	8/4	82 Ball FBGA	SDP, 2H/4H/8H 3DS	AN
NOTE 1 SDP is a single die per package. 2H/4H/8H denotes number of dies stacked using 3DS stacking.					

5   Supported Speeds

Table 4 — Supported Speeds

Raw Card	Speed	PC5-4400	PC5-4800	PC5-5600	PC5-6400	Notes
C0	DDR5	Y	Y			1,2
NOTE 1 X denotes supported speed grades. NOTE 2 Y denotes newly supported speed grades.						

6   Design Deviations

Table 5 — Design Deviations

None.

7   General Layout
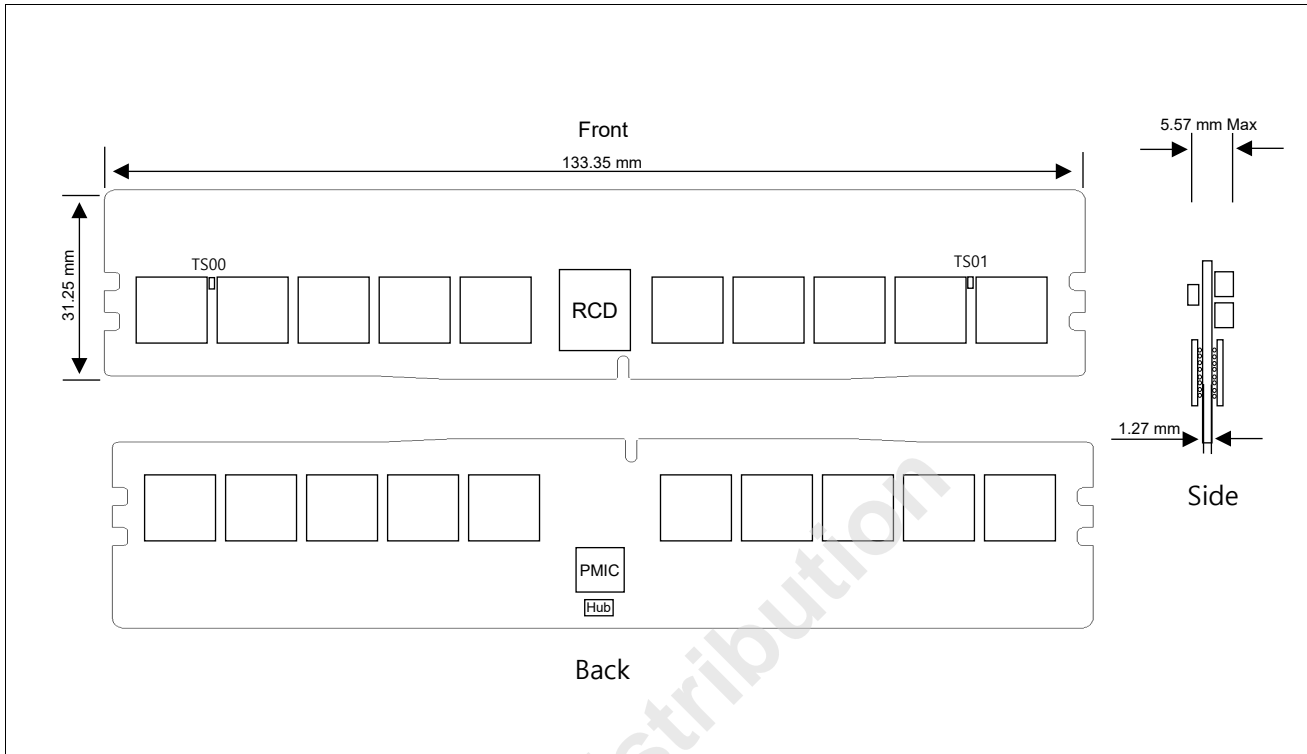
Figure 1 — General Layout

8   Functional Block Diagram

DCA [06:00] _A — QACA [13:00] _A -> CA [13:00]: SDRAMs D [10:01]

DCS0_A_n — QACS0_A -> CS_n: SDRAMs D [05:01]
QBCS0_A -> CS_n: SDRAMs D [10:06]

DCS1_A_n

DCA [06:00] _B — QACA [13:00] _B -> CA [13:00]: SDRAMs D [20:11]

DCS0_B_n — QACS0_B -> CS_n: SDRAMs D [15:11]
QBCS0_B -> CS_n: SDRAMs D [20:16]

DCS1_B_n

Register

DCK_t / DCK_c — QACK_A_t -> CK_t: SDRAMs D [05:01]   / QACK_A_c -> CK_c: SDRAMs D [05:01]

QCCK_A_t -> CK_t: SDRAMs D [10:06]   / QCCK_A_c -> CK_c: SDRAMs D [10:06]

QACK_B_t -> CK_t: SDRAMs D [15:11]   / QACK_B_c -> CK_c: SDRAMs D [15:11]

QCCK_B_t -> CK_t: SDRAMs D [20:16]   / QCCK_B_c -> CK_c: SDRAMs D [20:16]

QLBD — DLBD_A -> LBDQ: SDRAMs D [10:01]
DLBD_B -> LBDQ: SDRAMs D [20:11]

QLBS — DLBS_A -> LBDQS: SDRAMs D [10:01]
DLBS_B -> LBDQS: SDRAMs D [20:11]

DRST_n — QRT_A_n -> RESET_n: SDRAMs D [10:01]
QRT_B_n -> RESET_n: SDRAMs D [20:11]

ALERT_n — DERROR_IN_A_n -> ALERT_n: SDRAMs D [10:01]
DERROR_IN_B_n -> ALERT_n: SDRAMs D [20:11]

Front   TS00   D01 D02 D03 D04 D05   RCD   D11 D12 D13 D14 TS01 D15

Back   D06 D07 D08 D09 D10   D16 D17 D18 D19 D20

PMIC
SPD/HUB

Address, Control and Clock lines

NOTE 1 Unless otherwise noted resistors are 15 Ω ± 5%

Figure 2 — X80 DIMM, Populated as One Package Rank of x4 DDR5 SDRAMs (Part 1 of 4)

8 **Functional Block Diagram (cont'd)**

Figure 3 — X80 DIMM, Populated as One Package Rank of x4 DDR5 SDRAMs (Part 2 of 4)

8   Functional Block Diagram (cont'd)

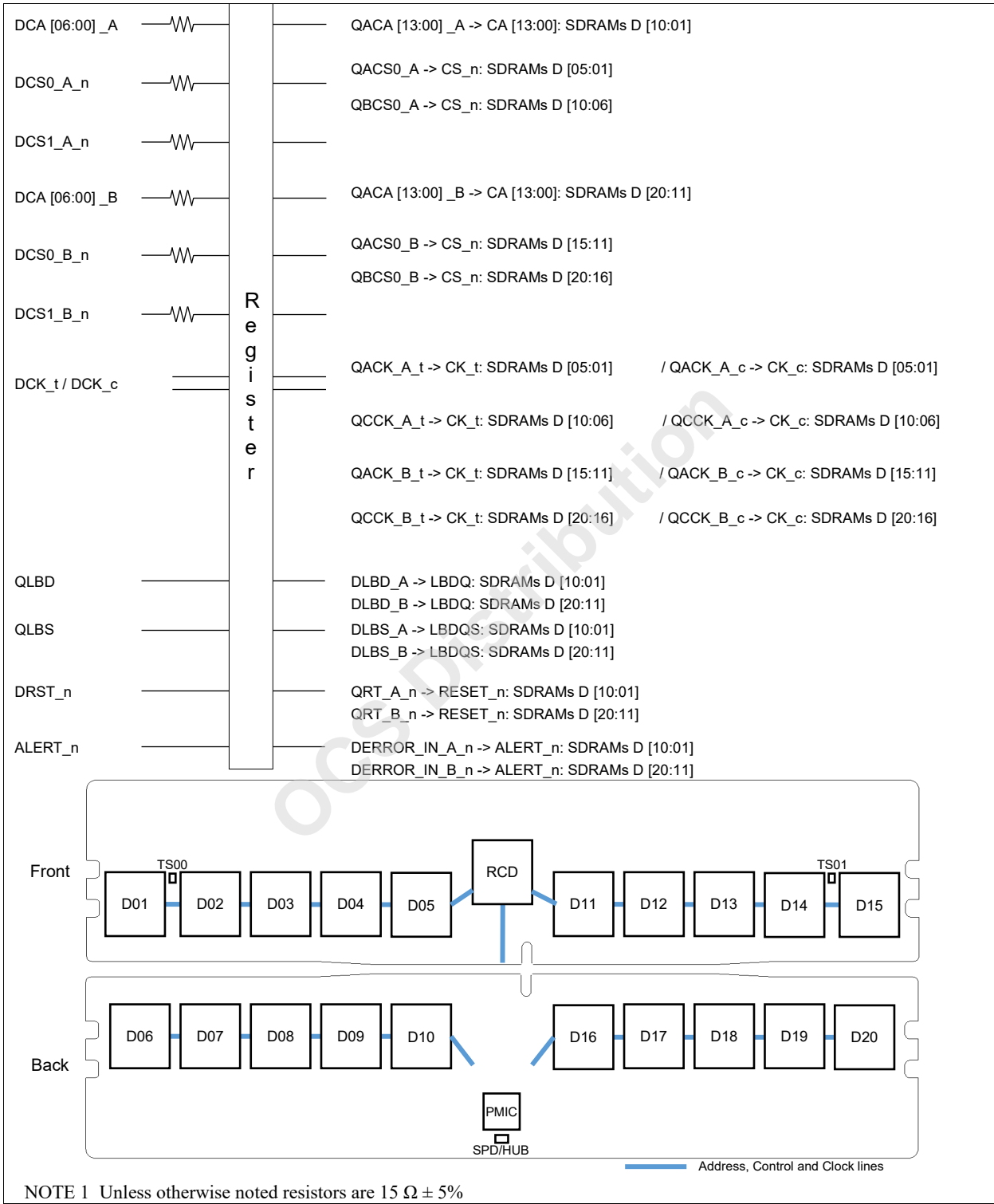**Figure 4 — X80 DIMM, Populated as One Package Rank of x4 DDR5 SDRAMs (Part 3 of 4)**

8   Functional Block Diagram (cont'd)
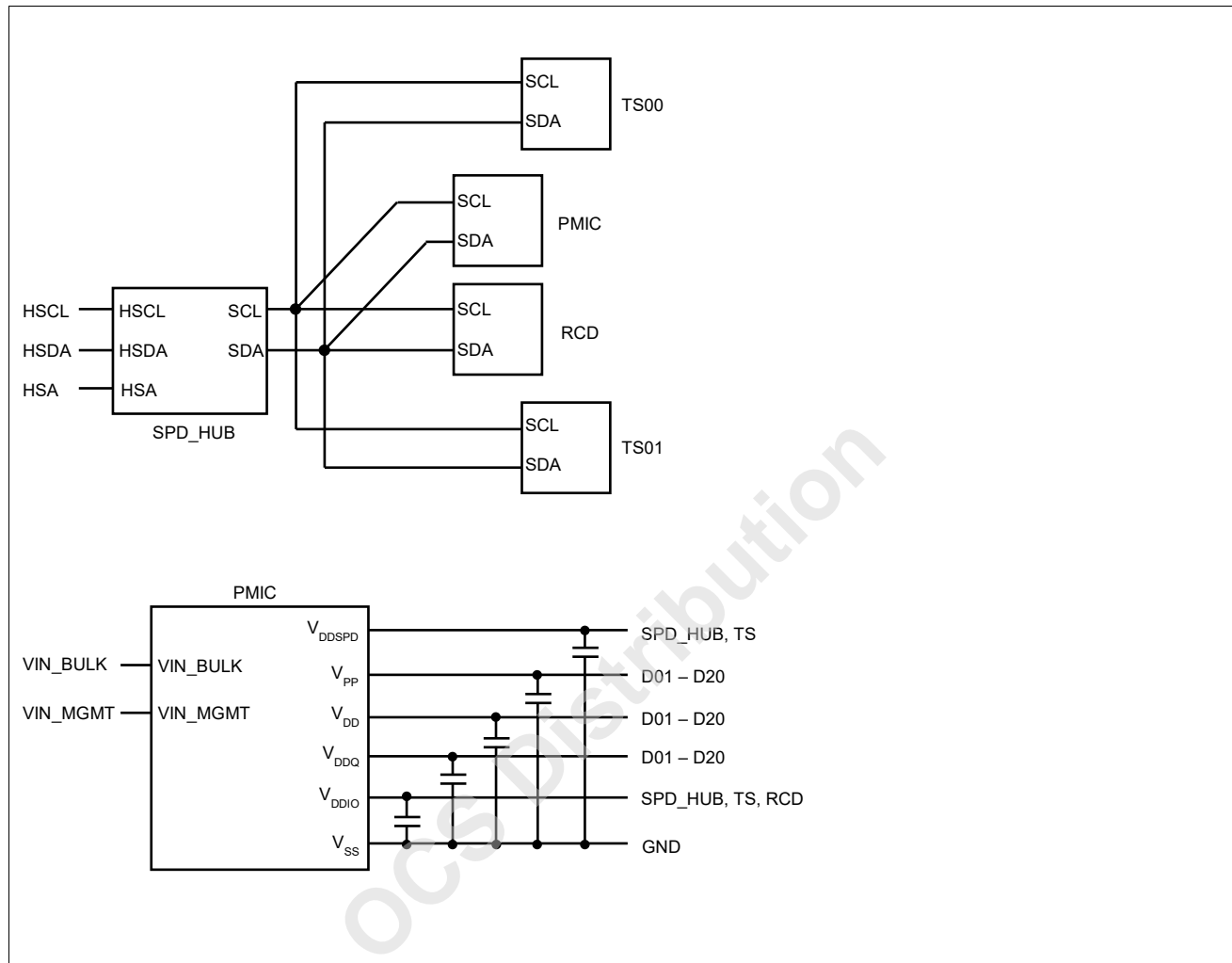
Figure 5 — X80 DIMM, Populated as One Package Rank of x4 DDR5 SDRAMs (Part 4 of 4)

9   SMBus Net Structures

Table 6 — SMBus Net Structures

Signal	Etch Length (mm)			
HSCL	89.3			
HSDA	90.7			
HSA	86.2			
	Hub to PMIC	Hub to RCD	Hub to TS00	Hub to TS01
LSCL	8.1	16.4	63.7	63.7
LSDA	6.7	18.1	65.8	65.8

NOTE 1   Gold Finger to Hub is to be 105 mm or less.
NOTE 2   Hub to PMIC is to be 10 mm or less.
NOTE 3   Hub to RCD is to be 25 mm or less.
NOTE 4   Hub to TS0 is to be 80 mm or less.
NOTE 5   Hub to TS1 is to be 80 mm or less.

10   Clock Input Net Structure
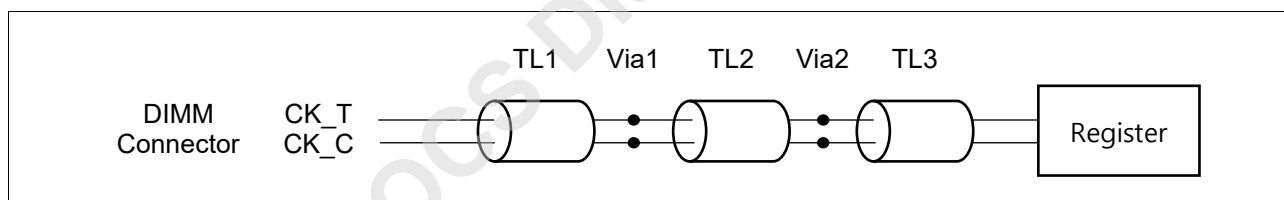
Figure 6 — Net Structure Routing for Register Clock Input

Table 7 — Clock Lengths for Register Input Net Structures

Raw Card	Signal	TL0(MS)	Via1	TL1(SL)	Via2	TL2(MS)	Compensated Total Length
C0	CK_T	1.8	0.1	5.2	1.0	0.5	8.4
	CK_C	1.8	0.1	5.2	1.0	0.5	8.4

NOTE 1   All distances are given in mm.
NOTE 2   Compensated Total = TL1/1.1 + Via1 + TL2 + Via2 + TL3/1.1.
NOTE 3   Total Length must be kept within a tolerance of $\pm$ 1.0 mm. The segment lengths are not required to be met .

11   Register Clock Output Net Structure
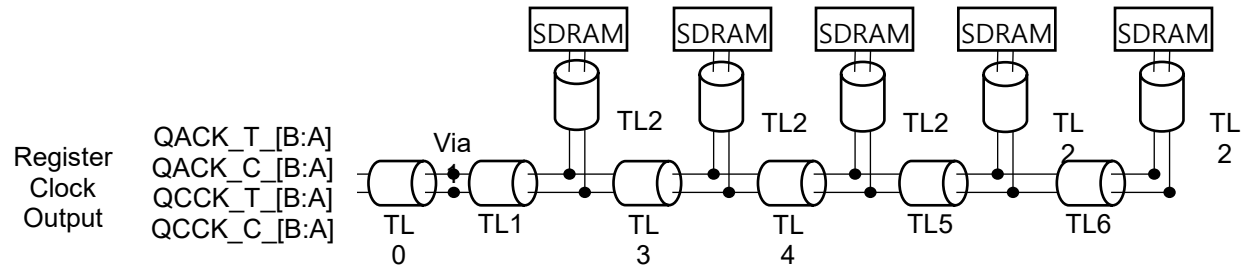
**Figure 7 — Net Structure Routing for Register Clock Output to SDRAM Load
QACK_C_[B:A], QACK_T_[B:A], QCCK_C_[B:A], and QCCK_T_[B:A]**

Table 8 — Trace Lengths for Register Clock Output to SDRAM Load Net Structures

Raw Card	Signal	TL0 (MSL)	Via1	TL1 (SL)	Comp 1st DRAM	TL3 (SL)	TL4 (SL)	TL5 (SL)	TL6 (SL)	Comp 5th DRAM	TL2 (MSL)
C0	QACK_T_A, QACK_C_A	0.5	0.1	19.2	19.7	18.6	18.6	19.6	18.6	95.1	0.6
	QCCK_T_A, QCCK_C_A	0.5	1.0	18.3	19.7	18.6	18.6	19.6	18.6	95.1	0.6
	QACK_T_B, QACK_C_B	0.5	1.0	17.4	18.8	18.6	18.6	19.6	18.6	94.2	0.6
	QCCK_T_B QCCK_C_B	0.5	0.1	18.3	18.8	18.6	18.6	19.6	18.6	94.2	0.6

NOTE 1   All distances are given in mm.
NOTE 2   Compensation 1st DRAM = TL0/1.1 + Via1 + TL1.
NOTE 3   Compensation 5th DRAM = TL0/1.1 + Via1 + TL1 + TL3 + TL4 + TL5 + TL6.
NOTE 4   Clock routing length may be adjusted as needed.

12   Data Net Structure – DQ, CB, DQS_t, and DQS_c

Figure 8 — Net Structure Routing for DQ, CB, DQS_t, and DQS_c

Table 9 — R/C C0 – Trace Lengths for DQ[31:00]_A, CB[07:00]_A, DQS[09:00]_t_A, and DQS[09:00]_c_A

DQ / Strobes	TL0 (MS)		TL1 (MS)		Via 1		TL2 (SL)		Via 2		TL3 (MS)		Comp Total Length	R1 (Ω)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQ[03:00]_A	2.8	2.8	0.6	1.5	0.1	1.0	5.5	5.7	0.1	0.1	0.6	0.6	10.3	15±5%
DQS00_t_A, DQS00_c_A	3.0	3.0	1.4	1.4	0.4	0.4	6.6	6.6	0.4	0.4	1.2	1.2	12.7	15±5%
DQ[07:04]_A	2.8	2.8	0.6	1.4	0.1	1.0	9.3	9.5	0.1	0.1	0.6	0.6	14.1	15±5%
DQS05_t_A, DQS05_c_A	3.0	3.0	0.7	0.7	0.7	0.7	8.2	8.3	0.7	0.7	1.2	1.2	14.1	15±5%
DQ[11:08]_A	2.8	2.8	0.6	1.5	0.1	1.0	5.0	5.2	0.1	0.1	0.6	0.6	9.8	15±5%
DQS01_t_A, DQS01_c_A	3.0	3.0	1.4	1.4	0.4	0.4	4.8	4.9	0.4	0.4	1.2	1.2	10.9	15±5%
DQ[15:12]_A	2.8	2.8	0.6	1.4	0.1	1.0	8.0	8.2	0.1	0.1	0.6	0.6	12.9	15±5%
DQS06_t_A, DQS06_c_A	3.0	3.0	0.7	0.7	0.7	0.7	7.1	7.1	0.7	0.7	1.2	1.2	13.0	15±5%
DQ[19:16]_A	2.8	2.8	0.6	1.5	0.1	1.0	6.1	6.3	0.1	0.1	0.6	0.6	10.9	15±5%
DQS02_t_A, DQS02_c_A	3.0	3.0	1.4	1.4	0.4	0.4	4.4	4.4	0.4	0.4	1.2	1.2	10.4	15±5%
DQ[23:20]_A	2.8	2.8	0.6	1.4	0.1	1.0	7.0	7.2	0.1	0.1	0.6	0.6	11.8	15±5%
DQS07_t_A, DQS07_c_A	3.0	3.0	0.7	0.7	0.7	0.7	6.3	6.3	0.7	0.7	1.2	1.2	12.2	15±5%
DQ[27:24]_A	2.8	2.8	0.6	1.4	0.1	1.0	6.5	7.6	0.1	0.1	0.6	0.6	12.0	15±5%
DQS03_t_A, DQS03_c_A	3.0	3.0	0.7	0.7	0.4	0.4	6.4	6.4	0.4	0.4	1.2	1.2	11.8	15±5%
DQ[31:28]_A	2.8	2.8	0.6	1.4	0.1	1.0	5.2	5.4	0.1	0.1	0.6	0.6	10.0	15±5%
DQS08_t_A, DQS08_c_A	3.0	3.0	1.4	1.4	0.7	0.7	4.3	4.4	0.7	0.7	1.2	1.2	10.9	15±5%
CB[03:00]_A	2.8	2.8	0.6	1.4	0.1	1.0	8.1	9.3	0.1	0.1	0.6	0.6	13.6	15±5%
DQS04_t_A, DQS04_c_A	3.0	3.0	0.7	0.7	0.4	0.4	8.0	8.0	0.4	0.4	1.2	1.2	13.5	15±5%
CB[07:04]_A	2.8	2.8	0.7	1.4	0.1	1.0	5.4	5.6	0.1	0.1	0.6	0.6	10.2	15±5%
DQS09_t_A, DQS09_c_A	3.0	3.0	1.4	1.4	0.7	0.6	6.3	6.3	0.7	0.7	1.2	1.2	12.8	15±5%

NOTE 1   All distances are given in mm. R1 value should not be changed.
NOTE 2   Compensated Total Length, TL0/1.1 + TL1/1.1 + Via1 + TL2 + Via2 + TL3/1.1, must be kept within a tolerance of ± 1.0 mm. The segment lengths are not required to be met.

12   Data Net Structure – DQ, CB, DQS_t, and DQS_c (cont'd)
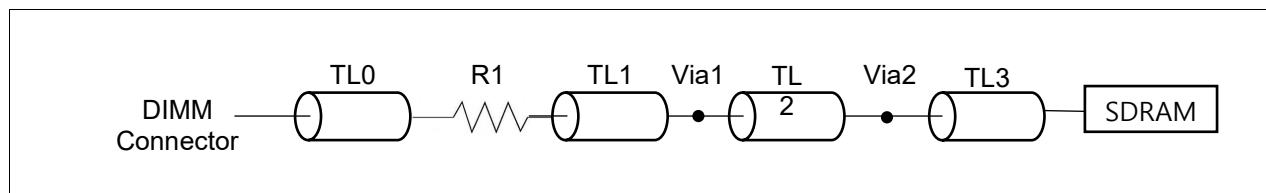
Table 10 — R/C C0 – Trace Lengths for DQ[31:00]_B, CB[07:00]_B, DQS[09:00]_t_B, and DQS[09:00]_c_B

DQ / Strobes	TL0 (MS)		TL1 (MS)		Via 1		TL2 (SL)		Via 2		TL3 (MS)		Comp Total Length	R1 (Ω)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQ[03:00]_B	2.8	2.8	0.7	1.4	0.1	1.0	5.4	6.7	1.0	1.0	0.6	0.6	11.8	15±5%
DQS00_t_B, DQS00_c_B	3.0	3.0	0.7	0.7	0.4	0.4	9.0	9.0	0.7	0.7	1.2	1.2	14.6	15±5%
DQ[07:04]_B	2.8	2.8	0.7	1.4	0.1	1.0	11.7	12.8	1.0	1.0	0.6	0.6	18.1	15±5%
DQS05_t_B, DQS05_c_B	3.0	3.0	1.5	1.5	0.7	0.7	10.9	10.9	0.4	0.4	1.2	1.2	17.3	15±5%
DQ[11:08]_B	2.8	2.8	0.6	1.4	0.1	1.0	5.5	5.7	1.0	1.0	0.6	0.6	11.2	15±5%
DQS01_t_B, DQS01_c_B	3.0	3.0	0.7	0.7	0.4	0.4	7.9	7.9	0.7	0.7	1.2	1.2	13.5	15±5%
DQ[15:12]_B	2.8	2.8	0.6	1.6	0.1	1.0	9.2	10.6	1.0	1.0	0.6	0.6	15.7	15±5%
DQS06_t_B, DQS06_c_B	3.0	3.0	1.4	1.4	0.7	0.7	7.5	7.5	0.4	0.4	1.2	1.2	13.9	15±5%
DQ[19:16]_B	2.8	2.8	0.6	1.4	0.1	1.0	4.6	4.7	1.0	1.0	0.6	0.6	10.2	15±5%
DQS02_t_B, DQS02_c_B	3.0	3.0	0.7	0.7	0.4	0.4	6.1	6.1	0.7	0.7	1.2	1.2	11.7	15±5%
DQ[23:20]_B	2.8	2.8	0.6	1.5	0.1	1.0	8.5	8.7	1.0	1.0	0.6	0.6	14.2	15±5%
DQS07_t_B, DQS07_c_B	3.0	3.0	1.4	1.4	0.7	0.7	5.7	5.7	0.4	0.4	1.2	1.2	12.0	15±5%
DQ[27:24]_B	2.8	2.8	0.6	1.4	0.1	1.0	6.2	6.4	1.0	1.0	0.6	0.6	11.9	15±5%
DQS03_t_B, DQS03_c_B	3.0	3.0	0.7	0.7	0.4	0.4	4.8	4.8	0.7	0.7	1.2	1.2	10.4	15±5%
DQ[31:28]_B	2.8	2.8	0.6	1.5	0.1	1.0	6.7	6.8	1.0	1.0	0.6	0.6	12.3	15±5%
DQS08_t_B, DQS08_c_B	3.0	3.0	1.4	1.4	0.7	0.7	4.1	4.1	0.4	0.4	1.2	1.2	10.4	15±5%
CB[03:00]_B	2.8	2.8	0.6	1.4	0.1	1.0	13.8	13.9	1.0	1.0	0.6	0.6	19.4	15±5%
DQS04_t_B, DQS04_c_B	3.0	3.0	1.5	1.5	0.7	0.7	12.8	12.8	0.4	0.4	1.2	1.2	19.2	15±5%
CB[07:04]_B	2.8	2.8	0.6	1.5	0.1	1.0	8.7	8.8	1.0	1.0	0.6	0.6	14.3	15±5%
DQS09_t_B, DQS09_c_B	3.0	3.0	0.7	0.7	0.4	0.4	11.1	11.1	0.7	0.7	1.2	1.2	16.7	15±5%

NOTE 1   All distances are given in mm. R1 value should not be changed.
NOTE 2   Compensated Total Length, TL0/1.1 + TL1/1.1 + Via1 + TL2 + Via2 + TL3/1.1, must be kept within a tolerance of ± 1.0 mm. The segment lengths are not required to be met.

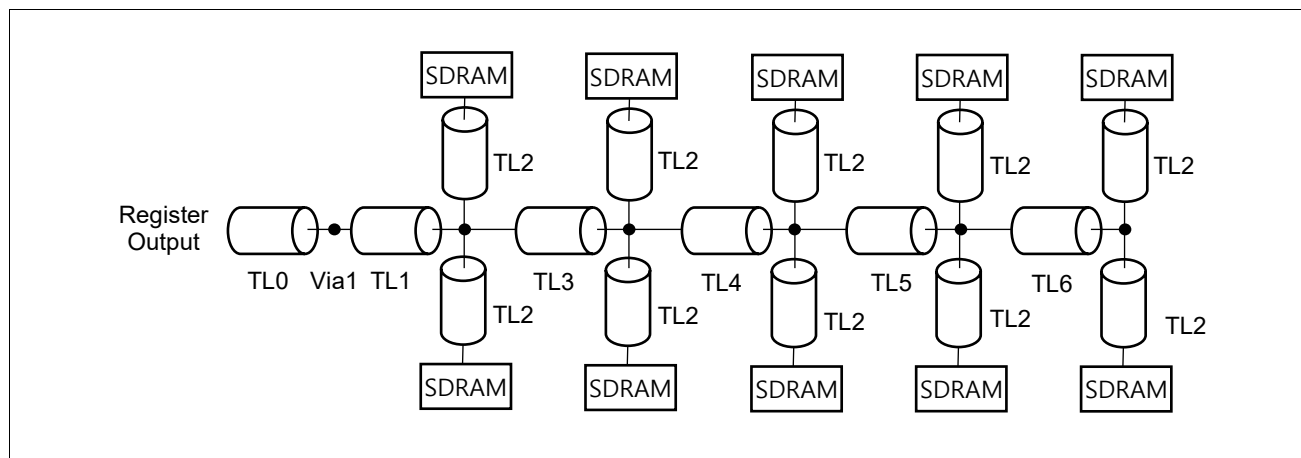**13   Post Register Address and Command Net Structure Routing**

Figure 9 — Net Structure Routing for QACA[13:00]_[B:A]

Table 11 — Trace Lengths for Post Register Address and Command Net Structures

Raw Card	Signal	TL0 (MS)	Via1	TL1 (SL)	Comp 1st DRAM	TL3 (SL)	TL4 (SL)	TL5 (SL)	TL6 (SL)	Comp 5th DRAM	TL2 (MS)
C0	Channel A CA00	0.5	1.0	14.6	16.0	12.6	12.6	12.6	12.6	66.4	0.6
	Channel B CA00	0.5	1.0	14.6	16.0	12.6	12.6	12.6	12.6	66.4	0.6

NOTE 1   All distances are given in mm.
NOTE 2   Compensation 1st DRAM = TL0/1.1 + Via1 + TL1.
NOTE 3   Compensation 5th DRAM = TL0/1.1 + Via1 + TL1 + TL3 + TL4 + TL5 + TL6.
NOTE 4   All distances can be adjusted within the below rules.
-    Address routing lengths between the DRAMs(TL3, TL4, TL5, TL6) may be adjusted by +/- 3.0 mm relative to the reference design.
-    The segment between the via and the DRAM ball(TL2) may also be changed as needed.
-    Address routing lengths between the register and the first DRAMs(TL1) may be adjusted by +/- 10 mm.

14   Post Register Control Net Structure Routing
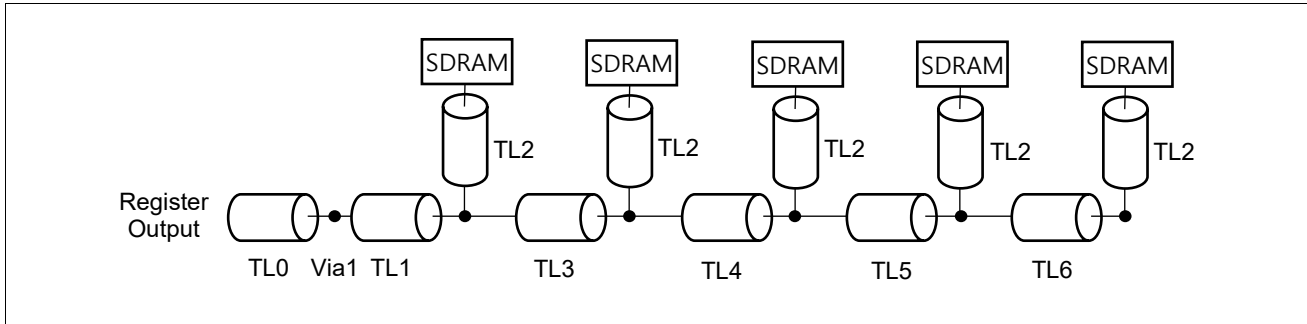
Figure 10 — Net Structure Routing for Q[B:A]CS00_[B:A]

Table 12 — Trace Lengths for Post Register Control Net Structures

Raw Card	Signal	TL0 (MS)	Via1	TL1 (SL)	Comp 1st DRAM	TL3 (SL)	TL4 (SL)	TL5 (SL)	TL6 (SL)	Comp 5th DRAM	TL2 (MS)
C0	Channel A CS00_n	0.5	1.0	16.0	17.5	16.6	16.6	15.6	15.6	81.9	0.6
	Channel B CS00_n	0.5	0.1	17.8	18.3	16.6	16.6	15.6	15.6	82.7	0.6

NOTE 1   All distances are given in mm.
NOTE 2   Compensation 1st DRAM = TL0/1.1 + Via1 + TL1.
NOTE 3   Compensation 5th DRAM = TL0/1.1 + Via1 + TL1 + TL3 + TL4 + TL5 + TL6.
NOTE 4   All distances can be adjusted within the below rules.
  -    Control routing length may be adjusted as needed to maintain timing to the clock.

15 Pre-Register Address, Command, and Parity Net Structure Routing
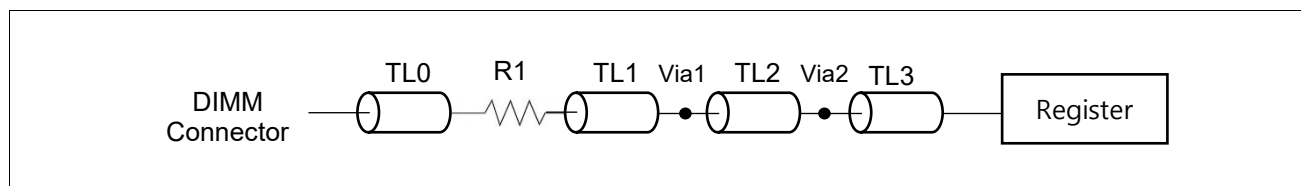

**Figure 11 — Net Structure Routing for CA[06:00]_[B:A], CS[01:00]_n_[B:A], and PAR_[B:A]**

Table 13 — Trace Lengths for Pre-Register Address, Command, and Parity Net Structures

Raw Card	Signal	TL0 (MS)		TL1 (MS)		Via1		TL2 (SL)		Via 2		TL3 (MS)		Comp. Total Length	R1 (Ω)
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
C0	CA_A PAR_A	2.9	3.1	0.6	0.8	0.1	0.1	5.0	6.0	0.1	1.0	0.5	0.9	10.0	15±5%
	CA_B PAR_B	2.8	3.2	0.7	1.0	0.1	1.0	6.0	7.3	0.1	1.0	0.5	1.0	11.5	15±5%
	CS_A	2.8	2.9	0.6	1.3	0.1	1.0	7.6	9.2	0.1	0.1	0.5	0.5	13.0	15±5%
	CS_B	2.9	3.0	0.7	0.9	0.1	0.1	9.5	10.4	0.1	1.0	0.5	0.5	14.4	15±5%

NOTE 1   All distances are given in mm. R1 value should not be changed.
NOTE 2   Compensated Total = TL0/1.1 + TL1/1.1 + Via1 + TL2 + Via2 + TL3/1.1.
NOTE 3   Total Length must be kept within a tolerance of ± 1.0 mm. The segment lengths are not required to be met.
NOTE 4   DIMM vendor allowed to adjust compensated length of nets to align Address and Chipselect within and between Ch-A and Ch-B if length for Address is ≤ 12.5 mm, and Chipselect is ≤ 15.5 mm.

16   DIMM Impedance Profile

Applies to VDD, VDDQ and VPP voltage rails for this raw card.

Frequency ranges f1, f2, f3 are defined as: f1 ≤ 2 MHz; f2 = 10 MHz; f3 = 20 MHz
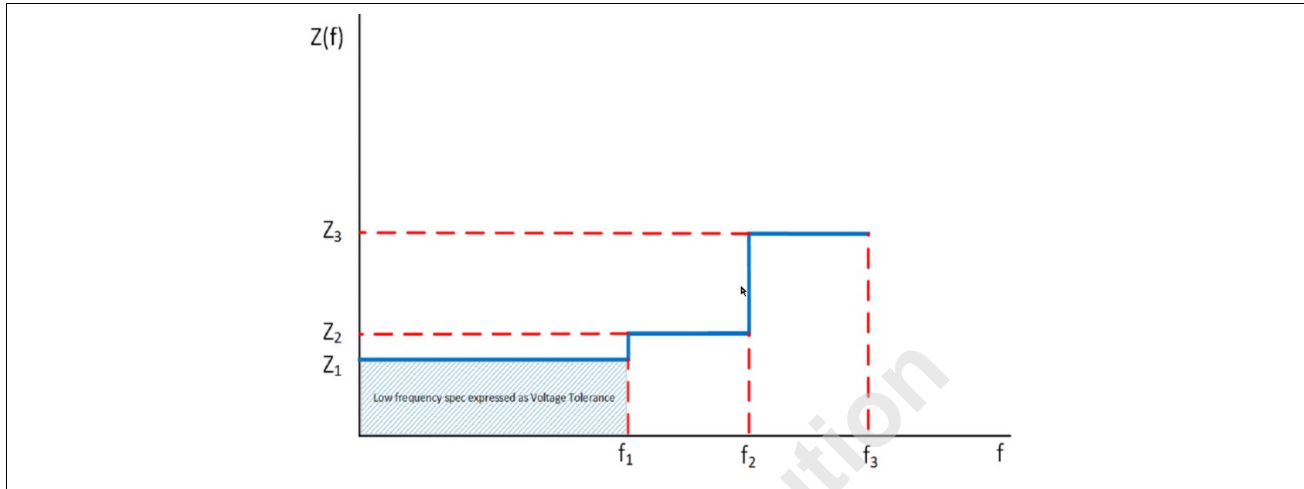
NOTE 1   Z(f) targets for each frequency range (Z_1, Z_2, Z_3).

NOTE 2 Z_x is expressed as voltage tolerance based on DRAM input supply tolerances (-3%, +6%)

Figure 12 — DIMM Impedance Profile

Table 14 — Voltage Operating Conditions

DRAM	Symbol	Voltage Spec Freq: DC to 2 MHz				Z(f) Spec Freq: 2 to 10 MHz		Z(f) Spec Freq: 10 to 20 MHz		Notes
		Min (- 3%)	Typ	Max (+ 6%)	Unit	z_{max}	Unit	z_{max}	Unit	
Core Power	VPP	1.746	1.8	1.908	V	100	mOhm	170	mOhm	
Supply Voltage	VDDQ	1.067)	1.1	1.166	V	40	mOhm	80	mOhm	
Supply Voltage	VDD	1.067	1.1	1.166	V	30	mOhm	50	mOhm	

NOTE 1   VDDQ must be less than or equal to VDD. VDD must be within 66 mV of VDDQ.
NOTE 2   AC parameters are measured separately on VDD and VDDQ.
NOTE 3   DC to 2 MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations.
NOTE 4   Z(f) is per voltage domain per DRAM device. Per DRAM BGA pin is not required.
NOTE 5   Z(f) does not include the DRAM package and silicon die.

17 RESET_n and QRST_n Net Structure Routing
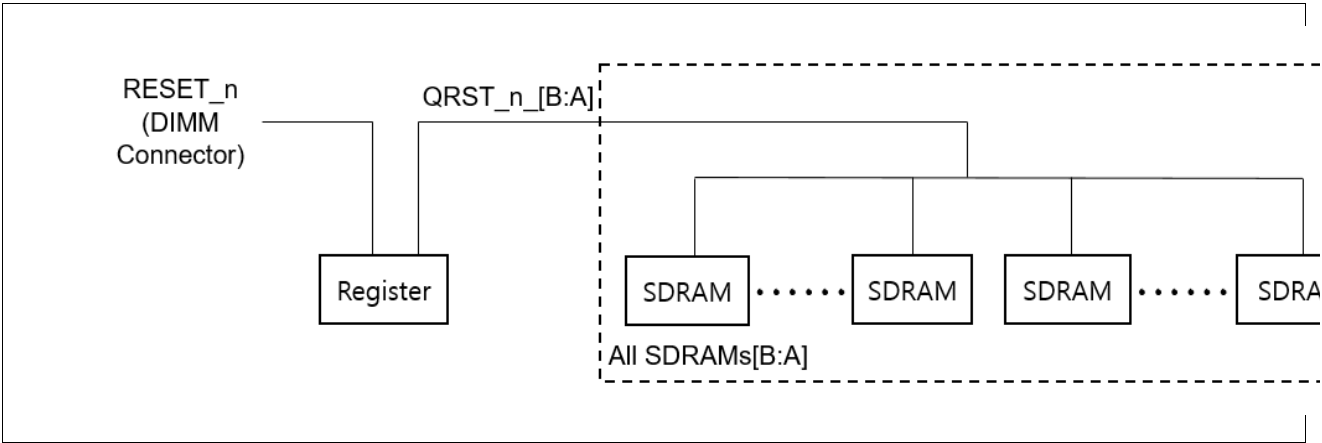
Figure 13 — Net structure Routing for RESET_n and QRST_n_[B:A]

Table 15 — Trace Lengths for RESET_n and QRST_n_[B:A] Net Structures

Raw Card	Signal	Total Net Length (mm)	Notes
C0	RESET_n	17.1	
	QRST_n (Channel A / Channel B)	74.9 / 76.0	1
NOTE 1 For QRST_n, electrical length from register to any DRAM must be less than 100 mm. This length is for reference and not required to be met.			

18 ALERT_n Output Net Structure Routing

Figure 14 — Net Structure Routing for ALERT_n

18 ALERT_n Output Net Structure Routing (cont'd)

Table 16 — Trace Lengths for ALERT_n Output Net Structures

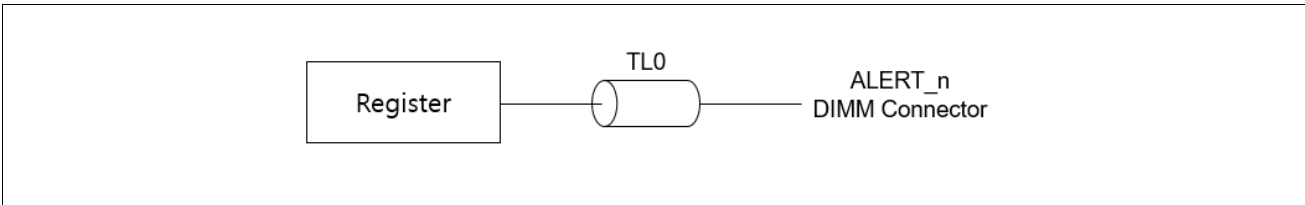| Raw Card	TL0	Notes
C0	14.1	1
NOTE 1 Only the total length of the trace is specified. This length is for reference and not required to be met.		

19 DERROR_in_n Net Structure Routing
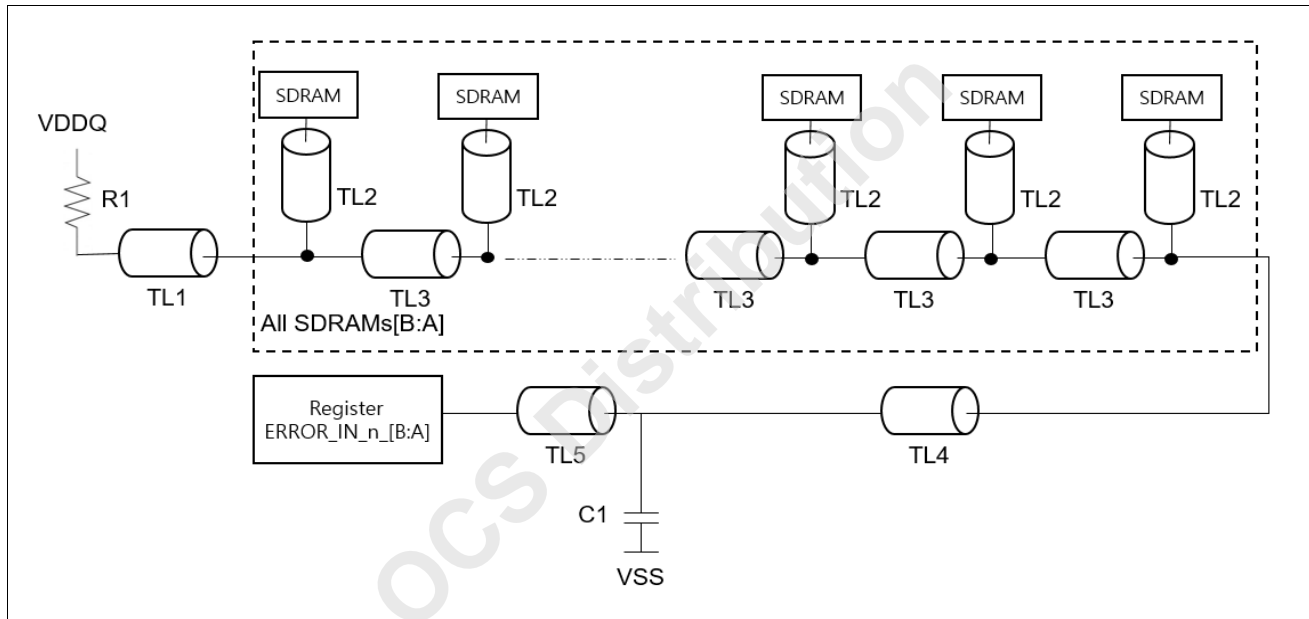
Figure 15 — Net Structure Routing for DERROR_in_n_[B:A]

Table 17 — Trace Lengths for DERROR_in_n_[B:A] Net Structures

Raw Card	TL1	TL2	TL3		Total of TL3	TL4	TL5	R1 (Ω)	C1 (pF)	Notes
			Min	Max						
C0	0.7	0.6	4.0	7.5	57.4	10.3	0.5	47±5%	10	1
NOTE 1 All distances are given in mm. All lengths are for reference and not requited to be met. Topology must be maintained. The values of R1 and C1 may be changed by DIMM manufacturer.										

20 Function Control Word Programming

The Register is configured through Register Control Words (RCW).

Some of the Control Words are module PCB design specific and must be programmed the same way for all systems. These are the Control Words that are defined in Table 18.

Table 18 — RC C0 – SPD Programming

SPD Byte	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
230	0	0	0	1	0	0	0	1	11	Module Nominal Height
231	0	0	1	0	0	0	0	1	21	Module Thickness (Front 1~2 mm / Back 2~3 mm)
232	0	0	0	0	0	0	1	0	02	Reference Raw Card Used – C0
233	1	0	0	0	0	0	0	1	81	Temperature Grade - XT, No Heat Spreader, Row-1
234	0	0	0	0	0	0	0	0	00	Module Organization – 1Rx4
235	0	0	1	1	0	0	1	0	32	2 Channels, 8 bit ECC, 32 bit Channel Bus Width
248[1]	0	0	1	0	1	0	1	0	2A	BCK_t/_c - disabled, QDCK_t/_c - disable, QCCK_t/_c - enable, QBCK_t/_c - disable, QACK_t/_c – enable
249[1]	0	0	0	0	1	0	1	0	0A	QBCS[1:0]_n output - enable, QACS[1:0]_n output - enable, Q[B:A]CA13 output driver - enable, BCS_n, BCOM[2:0] and BRST_n outputs - disable, DCS1_n input buffer and QxCS1_n outputs - enable, QBCA outputs - disable, QACA outputs – enable
250[1]	0	1	0	1	0	1	0	1	55	RCD-RW0A QCK Driver Characteristics - only QACK_t/QACK_c - enabled (14 ohm)
252[1]	0	0	0	1	0	0	0	1	11	RCD-RW0C QxCA and QxCS_n Driver Characteristics – (both) 14 ohm
254[1]	0	0	0	0	0	0	0	0	00	RCD-RW0E QCK - mod, QCA – mod, and QCS – mod, Output Slew Rate
NOTE 1 DIMM vendor has option to update these bytes to optimize product.										

21   Cross Section Recommendations

PCBs should contain solid ground plane and power plane layers as far as possible.

The PCB edge connector contacts shall be gold plated.

Any exceptions to these design rules have been identified in the front of this annex

Table 19 — PCB Fabrication

Layer	Layer Description	Single-ended Impedances		Differential Impedances		Copper (oz)	Dielectric Thickness (μm)
		Trace Width (mm)	Impedance (ohm)	Trace Width / Spacing (mm / mm)	Impedance (ohm)		
1	DQ/DQS	0.190	35±10%	0.190 / 0.10	60±10%	0.3 + Plating	
	CA/DCK/ETC	0.093	50±10%	0.093 / 0.10	81±10%		
	QCK + VDD	0.330	25±10%				
							65
2	GND + VPP					0.5	
							60
3	DQ	0.145	35±10%			0.5	
	CA/ETC	0.074	50±10%				
	QCK	0.248	25±10%	0.248 / 0.10	47±10%		
							205
4	GND					1.0	
							60
5	DQS	0.136	35±10%	0.136 / 0.10	63±10%	1.0	
	ETC + VDDQ	0.063	50±10%				
							200
6	ETC + VDD	0.063	50±10%	0.063 / 0.10	86±10%	1.0	
							60
7	VDDQ					1.0	
							205
8	DQ	0.145	35±10%			0.5	
	CA/DCK	0.074	50±10%	0.074 / 0.10	89±10%		
	QCK + VPP	0.248	25±10%	0.248 / 0.10	47±10%		
							60
9	GND					0.5	
							65
10	DQ/DQS	0.190	35±10%	0.190 / 0.10	60±10%	0.3 + Plating	
	CA/DCK/ETC	0.093	50±10%				
	QCK + VDD	0.330	25±10%				

NOTE   The recommended construction and impedance can be found in the PCB Fabrication Table. The values in the table were used in the simulations during development and in the initial DIMMs used to verify operation. Deviations should be kept to a minimum. All Differential impedances in the table are for reference only.

Section

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Standard Improvement Form **JEDEC Standard <u>JESD305-R8-RCC v1.0</u>**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC   Fax: 703.907.7583
Attn: Publications Department
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Suite 240 South
Arlington, VA 22201-2107

1.   I recommend changes to the following:

☐   Requirement, clause _____

☐   Test method number _____   Clause number _____

The referenced clause number has proven to be:

☐ Unclear   ☐ Too Rigid   ☐ In Error

☐ Other _____

2.   Recommendations for correction:

_____
_____
_____
_____

3.   Other suggestions for document improvement:

_____
_____
_____
_____

Submitted by
Name: _____   Phone: _____
Company: _____   E-mail: _____
Address: _____
City/State/Zip: _____   Date: _____