4.20.28 - 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/
PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification

DDR4 SDRAM Registered DIMM Design Specification

Revision 1.00

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1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Registered, Double Data Rate, Synchronous SDRAM Dual In-Line Memory Modules (DDR4 SDRAM RDIMMs). These DDR4 Registered DIMMs (RDIMMs) are intended for use as main memory when installed in PCs.

Reference design examples are included which provide an initial basis for DDR4 RDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666 and PC4-3200 support. All DDR4 RDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

An additional lower voltage of TBD is defined. PC4L is used to reference DIMMs capable of operation at this voltage level. The annex for each raw card will have specific entries to indicate DIMM operation at PC4 and PC4L voltage levels.

This specification follows the JEDEC standard DDR4 component specification (refer to JEDEC standard JESD79-4, at www.jedec.org).

Table 1 — DDR4 Product Family Attributes

DIMM Organization	x72 ECC	Notes
DIMM Dimensions (nominal)	133.35 mm x 31.25 mm	Refer to MO-309
	133.35 mm x 18.75 mm	Refer to MO-309
Pin Count	288	
DDR4 SDRAMs Supported	4 Gb, 8 Gb, 16 Gb	78/106-ball FBGA package for x4 and x8 devices. Refer to MO-207: variations DT-z, DW-z
Capacity	16 GB, 32 GB, 64 GB, 128 GB	
SDRAM width	x4, x8	
Serial Presence Detect, Thermal Sensor (SPD-TSE)	512 byte	TSE2004av specifications
Voltage Options	VDD: PC4 - 1.2 V ± 5%, PC4L - TBD	
	VPP: 2.5 V + 10%, - 5%	The VPP supply has VSS as its return path. VPP is a separate supply, VDDSPD.
	VDDSPD: 2.5 V ± 10%	The VDDSPD supply has VSS as its return path. VDDSPD is separate from the VPP power plane. VDDSPD is shared between the SPD-TSE and the RCD (register). The RCD only supports 2.5 V.
	12 V ± 15%	May be available on the connector but not used by RDIMMs
Interface	1.2 V signaling	

2 Environmental Requirements

288-pin Registered DDR4 SDRAM DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Table 2 — Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +55	°C	3
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
T_{STG}	Storage Temperature	-50 to +100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2

Note 1 Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
Note 2 Up to 9850 ft.
Note 3 The component maximum case temperature (T_{CASE}) shall not exceed the value specified in the DDR4 SDRAM component specification, JESD79-4.

3 Connector Pinout and Signal Description

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I^2C serial bus clock for SPD-TSE and register
BA0, BA1	Register bank select input	SDA	I^2C serial bus data line for SPD-TSE and register
BG0, BG1	Register bank group select input	SA0–SA2	I^2C slave address select for SPD-TSE and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	C0, C1 C2	Chip ID lines for SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS9_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	DM0_n-DM8_n	Data Mask
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred.
CK0_t, CK1_t	Register clock input (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clocks input (negative line of differential pair)	RFU	Reserved for future use

Note 1 Address A17 is only valid for 16 Gb x4 based SDRAMs.
Note 2 RAS_n is a multiplexed function with A16.
Note 3 CAS_n is a multiplexed function with A15.
Note 4 WE_n is a multiplexed function with A14.

Table 4 — Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT, and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, TDQS_t, and TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15, and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command being entered. Those pins are multi-function. For example, for activation with ACT_n Low, these are Addresses like A16, A15, and A14, but for non-activation command with ACT_n High, these are Command pins for Read, Write, and other commands defined in command truth table.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.

Table 4 — Input/Output Functional Description (Cont'd)

Symbol	Type	Function
DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS9_t-TDQS17_t, TDQS9_c-TDQS17_t	Input	Provides a dummy load for x8 based RDIMMs where mixed populations of X4 and x8 based RDIMMs are present.
DBI0_n-DBI8_n	Input/ Output	Provides for data bus inversion. Only possible for x8 based RDIMMs and where only x8 based RDIMMs are on a channel.
DM0_n-DM8_n	Input	Provides for masking of a byte on WRITE commands to the SDRAMs. Only possible for x8 based RDIMMs and where only x8 based RDIMMs are on a channel.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time as command & address, with CS_n LOW
ALERT_n	Output (Input)	Alert: Is multi functions, such as CRC error flag or Command and Address Parity error flag, as an Output signal. If there is an error in the CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is an error in the Command Address Parity Check, then ALERT_n goes LOW for a relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input. Using this signal or not is dependent on the system.
RFU		Reserved for Future Use: No on-DIMM electrical connection is present.
NC		No Connect: No on-DIMM electrical connection is present.
VDD[1]	Supply	Power Supply: 1.2 V ± 0.06 V
VSS	Supply	Ground
VTT	Supply	Power Supply for termination of Address, Command and Control, VDD/2.
12 V	Supply	12 V supply not used on RDIMMs.
VPP	Supply	SDRAM Activating Power Supply: 2.5 V (2.375 V min, 2.75 V max)
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD-TSE and register.
VREFCA	Supply	Reference voltage for CA

Note 1 For PC4, VDD is 1.2 V. For PC4L, VDD is TBD.

Table 5 — DDR4 288 Pin RDIMM Pin Wiring Assignments

Front Side Pin Label	Pin	Pin	Back side Pin Label
12 V, NC	1	145	12 V, NC
VSS	2	146	VREFCA
DQ4	3	147	VSS
VSS	4	148	DQ5
DQ0	5	149	VSS
VSS	6	150	DQ1
TDQS9_t, DQS9_t, DM0_n, DBI0_n, NC	7	151	VSS
TDQS9_c, DQS9_c, NC	8	152	DQS0_c
VSS	9	153	DQS0_t
DQ6	10	154	VSS
VSS	11	155	DQ7
DQ2	12	156	VSS
VSS	13	157	DQ3
DQ12	14	158	VSS
VSS	15	159	DQ13
DQ8	16	160	VSS
VSS	17	161	DQ9
TDQS10_t, DQS10_t, DM1_n, DBI1_n, NC	18	162	VSS
TDQS10_c, DQS10_c, NC	19	163	DQS1_c
VSS	20	164	DQS1_t
DQ14	21	165	VSS
VSS	22	166	DQ15
DQ10	23	167	VSS
VSS	24	168	DQ11
DQ20	25	169	VSS
VSS	26	170	DQ21
DQ16	27	171	VSS
VSS	28	172	DQ17
TDQS11_t, DQS11_t, DM2_n, DBI2_n, NC	29	173	VSS
TDQS11_c, DQS11_c, NC	30	174	DQS2_c
VSS	31	175	DQS2_t
DQ22	32	176	VSS
VSS	33	177	DQ23
DQ18	34	178	VSS
VSS	35	179	DQ19
DQ28	36	180	VSS
VSS	37	181	DQ29
DQ24	38	182	VSS
VSS	39	183	DQ25

Front Side Pin Label	Pin	Pin	Back side Pin Label
CK0_t	74	218	CK1_t
CK0_c	75	219	CK1_c
VDD	76	220	VDD
VTT	77	221	VTT
KEY			
EVENT_n	78	222	PARITY
A0	79	223	VDD
VDD	80	224	BA1
BA0	81	225	A10/AP
RAS_n/A16	82	226	VDD
VDD	83	227	RFU
CS0_n	84	228	WE_n/A14
VDD	85	229	VDD
CAS_n/A15	86	230	NC, SAVE_n
ODT0	87	231	VDD
VDD	88	232	A13
CS1_n, NC	89	233	VDD
VDD	90	234	NC, A17
ODT1, NC	91	235	NC, C2
VDD	92	236	VDD
C0, CS2_n, NC	93	237	NC, CS3_n, C1
VSS	94	238	SA2
DQ36	95	239	VSS
VSS	96	240	DQ37
DQ32	97	241	VSS
VSS	98	242	DQ33
TDQS13_t, DQS13_t, DM4_n, DBI4_n, NC	99	243	VSS
TDQS13_c, DQS13_c, NC	100	244	DQS4_c
VSS	101	245	DQS4_t
DQ38	102	246	VSS
VSS	103	247	DQ39
DQ34	104	248	VSS
VSS	105	249	DQ35
DQ44	106	250	VSS
VSS	107	251	DQ45
DQ40	108	252	VSS
VSS	109	253	DQ41
TDQS14_t, DQS14_t, DM5_n, DBI5_n, NC	110	254	VSS

Table 5 — DDR4 288 Pin RDIMM Pin Wiring Assignments

Front Side Pin Label	Pin	Pin	Back side Pin Label
TDQS12_t, DQS12_t, DM3_n, DBI3_n, NC	40	184	VSS
TDQS12_c, DQS12_c, NC	41	185	DQS3_c
VSS	42	186	DQS3_t
DQ30	43	187	VSS
VSS	44	188	DQ31
DQ26	45	189	VSS
VSS	46	190	DQ27
CB4, NC	47	191	VSS
VSS	48	192	CB5, NC
CB0, NC	49	193	VSS
VSS	50	194	CB1, NC
TDQS17_t, DQS17_t, DM8_n, DBI8_n, NC	51	195	VSS
TDQS17_c, DQS17_c, NC	52	196	DQS8_c
VSS	53	197	DQS8_t
CB6, NC	54	198	VSS
VSS	55	199	CB7, NC
CB2, NC	56	200	VSS
VSS	57	201	CB3, NC
RESET_n	58	202	VSS
VDD	59	203	CKE1, NC
CKE0	60	204	VDD
VDD	61	205	RFU
ACT_n	62	206	VDD
BG0	63	207	BG1
VDD	64	208	ALERT_n
A12/BC_n	65	209	VDD
A9	66	210	A11
VDD	67	211	A7
A8	68	212	VDD
A6	69	213	A5
VDD	70	214	A4
A3	71	215	VDD
A1	72	216	A2
VDD	73	217	VDD

Front Side Pin Label	Pin	Pin	Back side Pin Label
TDQS14_c, DQS14_c, NC	111	255	DQS5_c
VSS	112	256	DQS5_t
DQ46	113	257	VSS
VSS	114	258	DQ47
DQ42	115	259	VSS
VSS	116	260	DQ43
DQ52	117	261	VSS
VSS	118	262	DQ53
DQ48	119	263	VSS
VSS	120	264	DQ49
TDQS15_t, DQS15_t, DM6_n, DBI6_n, NC	121	265	VSS
TDQS15_c, DQS15_c, NC	122	266	DQS6_c
VSS	123	267	DQS6_t
DQ54	124	268	VSS
VSS	125	269	DQ55
DQ50	126	270	VSS
VSS	127	271	DQ51
DQ60	128	272	VSS
VSS	129	273	DQ61
DQ56	130	274	VSS
VSS	131	275	DQ57
TDQS16_t, DQS16_t, DM7_n, DBI7_n, NC	132	276	VSS
TDQS16_c, DQS16_c, NC	133	277	DQS7_c
VSS	134	278	DQS7_t
DQ62	135	279	VSS
VSS	136	280	DQ63
DQ58	137	281	VSS
VSS	138	282	DQ59
SA0	139	283	VSS
SA1	140	284	VDDSPD
SCL	141	285	SDA
VPP	142	286	VPP
VPP	143	287	VPP
RFU	144	288	VPP

Note 1 Light colored text indicates functions that are not applicable for RDIMM wiring. An example is the NC for pin 56 because RDIMMs defined by this specification will always have DIMM wiring for this pin.

4 Power Details

4.1 DIMM Voltage Requirements

The DIMM voltage requirements and the SDRAM voltage requirements are not identical. There must be some allowance for a small voltage drop across the DIMM. Table 6 defines the requirements for the Host at the DIMM socket.

Some modules have lower current requirements. Any specific module must meet the SDRAM and DDR4RCD01 voltage requirements for its worst case supply currents.

Table 6 — DDR4 RDIMM DC Operating Voltage[1,2,3] - 1.2 V operation

Symbol	Parameter	Voltage Rating (Volts)			Maximum Expected Current (AMPs)	Power State
		Minimum	Typical[4]	Maximum		
VDD	Supply Voltage	1.16	1.21	1.26	11.7	Operational
VPP	Activation Supply Voltage	2.41	2.50	2.75	3.75	Operational
VTT[5]	Termination Voltage	0.565	0.605	0.64	0.75	Operational
VTT at termination	Termination Voltage	0.95 x VDDmin[7]/2 (0.542)	-	1.05 x VDDmax[7]/2 (0.662)	0.75	Operational
VDDSPD	SPD-TSE Supply Voltage	2.41	2.5	2.75	0.75	Operational
V_12 (Optional[6])	Additional Power for non-volatile technologies	10.2	12.0	13.8	1.17	Operational
		5.8	12.0	13.8	0.7	Backup power off
		5.8	12.0	13.8	500 u	Idle power off

Note 1 20 MHz bandwidth limited measurement for all voltages in the table.
Note 2 Voltages are measured at the DIMM gold fingers.
Note 3 The SDRAM specification must be met and takes precedence over this document.
Note 4 Typical voltage is platform dependent, suggested value only.
Note 5 At the DIMM interface, VTT is the only voltage during normal operating conditions that can both source and sink current.
Note 6 If 12 volts is supplied, it must meet these requirements.
Note 7 SDRAM VDD specification range.

4.1.1 VTT Range

At the termination, Vtt must be within;

1. > 0.95 x Vddmin/2 = (0.60 V – 0.058 V) = 0.542

2. < 1.05 x Vddmax/2 = (0.60 V + 0.061 V) = 0.662

VDDmin and VDDmax refer to the SDRAM specification range.

4.1.2 Load Line

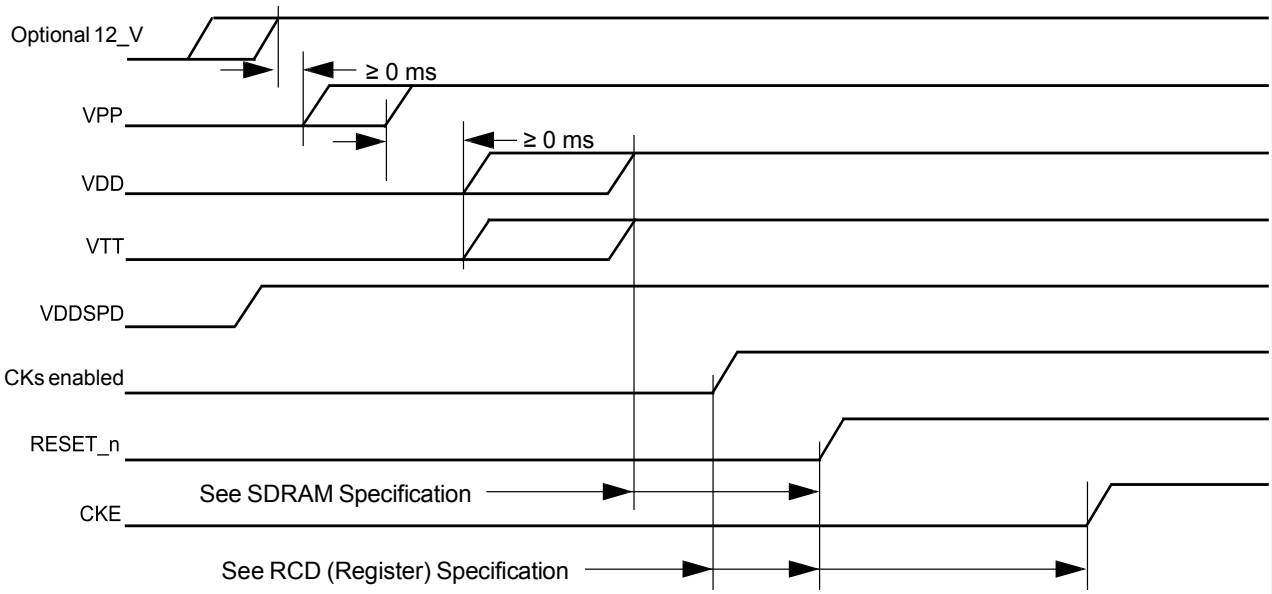
The Vdd specification can be considered a load line requirement with the specified voltage drop of 16 mV @11.7 Amps being a point on the load line. The load line can be specified as 0.016 V ≥ ZDIMM * (I_{VDD} + i_{VDD}) where ZDIMM is the DIMM power plane impedance, I_{VDD} is the DC DIMM current, and i_{VDD} is the band limited AC DIMM current.

4.2 Rules for Power-Up Sequence

VPP is the point of reference for power on sequence. There are several points of interest:

1. V_12 has to ramp with VPP or prior to VPP such that it is available as a power source on the DIMMs, which may have an on-DIMM voltage regulator.
2. VDDSPD is an independent power source that has no specific relationship to the other power sources.
3. VTT has a specific relationship to VDD: VTT=VDD/2.
4. The CK_t/CK_c input signals must be driven LOW (below the VIL(static) DDR4RCD01 parameter) throughout the VDD power ramp at least until the VDD supply voltage has settled to its final value.

Figure 1 — Graphical View of Power Sequence



Note 1 Start of ramp reference is 300 mV, as per the SDRAM specification.

4.3 12 V Power

The 12 V power source is optionally available for modules that support technologies other than homogeneously populated DRAM modules (i.e., not for UDIMMs, RDIMMs, and LRDIMMs). RDIMMs may be inserted into sockets that provide 12 V support. If support for 12 V is provided, it must meet the requirements of Sections 4.1 and 4.2.

Any module that uses 12 V must not interfere with the power sequence(s) of modules that do not support 12 V. 12 V is expected to remain valid during reduced power modes. The specific load requirements during these modes is product specific.

5 Component Details

MO-207 allows a maximum SDRAM package height of 21.0 mm. The maximum package size is not required for DDR4 RDIMMs. The larger the SDRAM package, the farther it must be placed from the edge connector and the longer the DQ bus must be. Minimizing the SDRAM package size to what is actually required improves signal integrity. Decoupling is improved if the capacitors are placed closer to the SDRAM balls.

Power delivery is improved with a reduction in width of the SDRAMs to what is actually required.

See section 6.7.3 for target SDRAM package size.

Figure 2 shows the mechanical information for the DDR4 SDRAM components. To use a smaller SDRAM component, some or all of the mechanical support balls may be omitted.

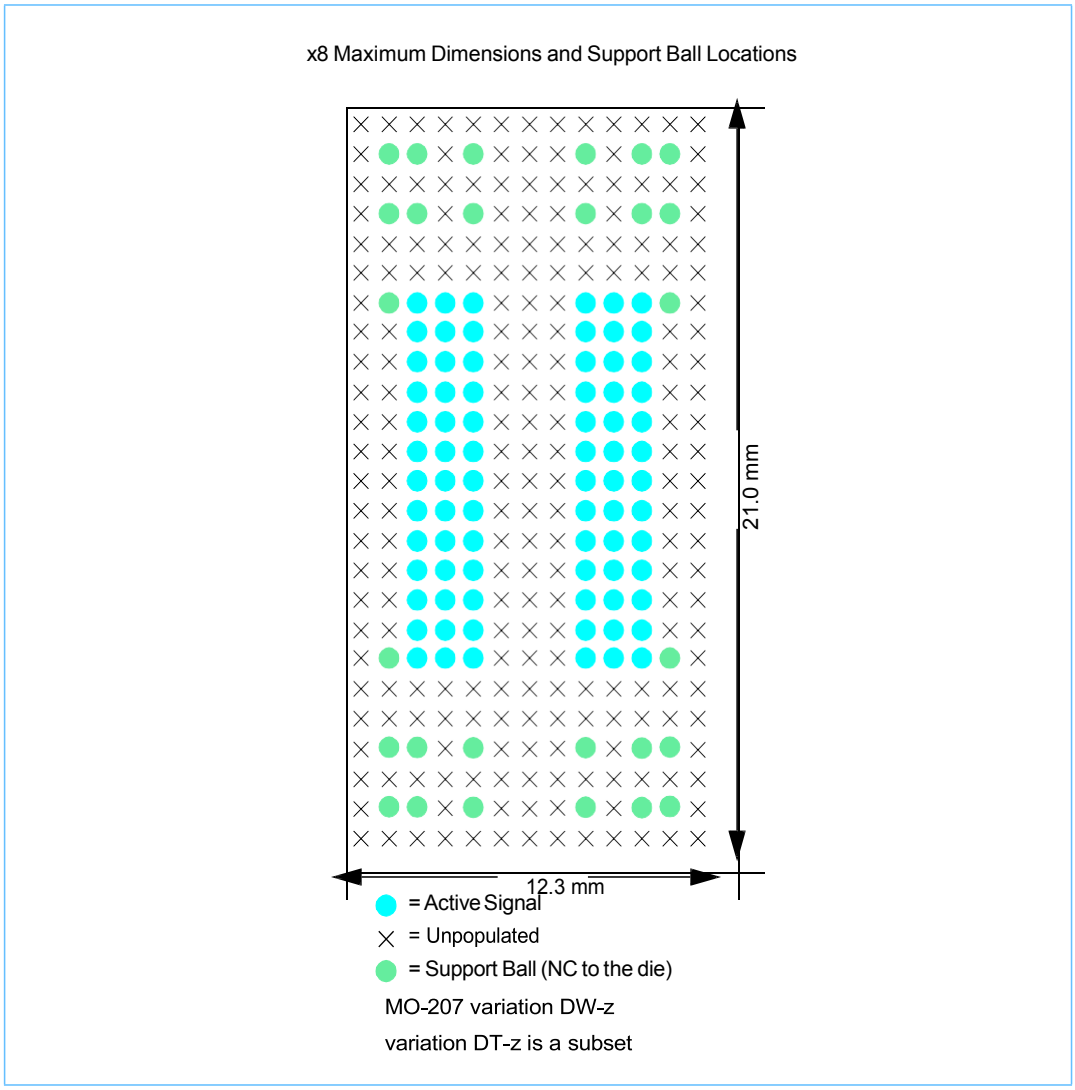


Figure 2 — DIMM Ball Patterns for DDR4 SDRAM Components

Table 7 — DDR4 x4 SDRAM DIMM Pad Array

Top view

MO-207 variation DW-z

	1	2	3	4	8	9	10	11	
A	NC[1]	NC[1]		NC[1]	NC[1]		NC[1]	NC[1]	
B									
C	NC[1]	NC[1]		NC[1]	NC[1]		NC[1]	NC[1]	
D									
E									
F	NC[1]	VDD	VSSQ	NC[2]	NC[3]	VSSQ	VSS	NC[1]	A
G		VPP	VDDQ	DQS_c	DQ1	VDDQ	ZQ		B
H		VDDQ	DQ0	DQS_t	VDD	VSS	VDDQ		C
J		VSSQ	NC[4]	DQ2	DQ3	NC[4]	VSSQ		D
K		VSS	VDDQ	NC[4]	NC[4]	VDDQ	VSS		E
L		VDD	C2, ODT1	ODT	CK_t	CK_c	VDD		F
M		VSS	C0, CKE1	CKE	CS_n	C1, CS1_n	TEN[7]		G
N		VDD	A14/WE_n	ACT_n	A15/CAS_n	A16/RAS_n	VSS		H
P		VREFCA	BG0	A10/AP	A12/BC_n	BG1	VDD		J
R		VSS	BA0	A4	A3	BA1	VSS		K
T		RESET_n	A6	A0	A1	A5	ALERT_n		L
U		VDD	A8	A2	A9	A7	VPP		M
V	NC[1]	VSS	A11	PAR[5]	A17[6]	A13	VDD	NC[1]	N
W		1	2	3	7	8	9		
Y						MO-207 variation DT-z			
AA	NC[1]	NC[1]		NC[1]	NC[1]		NC[1]	NC[1]	
AB									
AC	NC[1]	NC[1]		NC[1]	NC[1]		NC[1]	NC[1]	

Note 1 These balls are mechanical support balls for large SDRAM packages. A pad array to support MO-207 variation DT-z will not include these balls.
Note 2 TDQS_c is not valid on x4 based SDRAM components.
Note 3 DM_n, DBI_n, and TDQS_t are not valid on x4 based SDRAM components.
Note 4 DQ4, DQ5, DQ6, and DQ7 are not valid for x4 based SDRAM components.
Note 5 Parity input for address parity.
Note 6 A17 is only valid for x4 based SDRAMs of 16G bits.
Note 7 TEN is a test enable pin. It is not used on RDIMMs and should be tied low.

Table 8 — DDR4 x8 SDRAM DIMM Pad Array

Top view

MO-207 variation DW-z

	1	2	3	4	8	9	10	11	
A	NC[1]	NC[1]		NC[1]	NC[1]		NC[1]	NC[1]	
B									
C	NC[1]	NC[1]		NC[1]	NC[1]		NC[1]	NC[1]	
D									
E									
F	NC[1]	VDD	VSSQ	TDQS_c, NC[2]	TDQS_t, DBI_n, DM_n, NC[3]	VSSQ	VSS	NC[1]	A
G		VPP	VDDQ	DQS_c	DQ1	VDDQ	ZQ		B
H		VDDQ	DQ0	DQS_t	VDD	VSS	VDDQ		C
J		VSSQ	DQ4	DQ2	DQ3	DQ5	VSSQ		D
K		VSS	VDDQ	DQ6	DQ7	VDDQ	VSS		E
L		VDD	C2, ODT1	ODT	CK_t	CK_c	VDD		F
M		VSS	C0, CKE1	CKE	CS_n	C1, CS1_n	TEN[6]		G
N		VDD	A14/WE_n	ACT_n	A15/CAS_n	A16/RAS_n	VSS		H
P		VREFCA	BG0	A10/AP	A12/BC_n	BG1	VDD		J
R		VSS	BA0	A4	A3	BA1	VSS		K
T		RESET_n	A6	A0	A1	A5	ALERT_n		L
U		VDD	A8	A2	A9	A7	VPP		M
V	NC[1]	VSS	A11	PAR[4]	A17[5]	A13	VDD	NC[1]	N
W		1	2	3	7	8	9		
Y					MO-207 variation DT-z				
AA	NC[1]	NC[1]		NC[1]	NC[1]		NC[1]	NC[1]	
AB									
AC	NC[1]	NC[1]		NC[1]	NC[1]		NC[1]	NC[1]	

Note 1 These balls are mechanical support balls for large SDRAM packages. A pad array to support MO-207 variation DT-z will not include these balls.
Note 2 NC is valid for x8 based RDIMMs only when TDQS is disabled.
Note 3 NC is valid function for x8 based RDIMMs only when DM, DBI, and TDQS are disabled.
Note 4 Parity input for address parity.
Note 5 A17 is only valid for x4 based SDRAMs of 16G bits.
Note 6 TEN is a test enable pin. It is not used on RDIMMs and should be tied low.

5.1 Component Types and Placement

Components shall be positioned on the PCB to meet the minimum and maximum trace lengths required for DDR4 SDRAM signals.

Bypass capacitors for DDR4 SDRAM devices must be located near the device power pins.

5.2 Decoupling Guidelines

Table 9 — RDIMM Decoupling Capacitor Guidelines

	Guideline	Notes
VDD	Minimum of two decoupling capacitors to VSS per SDRAM	Should be placed as close as possible to the SDRAM VDD ball
	Minimum of four bulk decoupling capacitors to VSS per module	
VTT	Minimum of one decoupling capacitor to VDD per every two termination resistors or a decoupling capacitor at both ends of each resistor network	Should be placed as close as possible to the termination resistors.
	Minimum of one decoupling capacitor to VDD (located near the card edge VTT pin) or a decoupling capacitor at both ends of each resistor network	
VPP	Minimum of one decoupling capacitor to VSS per SDRAM ball	Should be placed as close as possible to the SDRAM VPP ball
	Minimum of one decoupling capacitor to VSS (located near the card edge VPP pin)	
VREFCA	Minimum of one decoupling capacitor to VDD per SDRAM	Should be placed as close as possible to the SDRAM VREFCA ball
	Minimum of one decoupling capacitor to VDD (located near the card edge VREFCA pin)	
BVREFCA	Minimum of one decoupling capacitor to VDD located near the BVREFCA pin of the register.	The capacitor is required to ensure that the power supply is stable.
QVREFCA	Minimum of one decoupling capacitor to VDD located near the QVREFCA pin of the register. Ideally, one decoupling capacitor per DRAM connected to VDD.	

Note 1 Decoupling capacitor values vary by module and may be staggered to achieve best overall impedance vs. frequency response.
Note 2 Recommended values for decoupling are 0.01 µF, 0.1 µF, and 1.0 µF.
Note 3 Recommended value for bulk decoupling is 4.7 µF.
Note 4 Depending on the SDRAM package size, all placements may not be possible.

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR4 SDRAM signals into six groups. Figure 3 illustrates the DIMM wiring. All signal groups, except DQ, implement a fly-by topology.

The signal groups are:

1. DQ and DQS signals connector to SDRAM
2. PreRegister ADD/CMD and CTRL
3. PreRegister CK
4. PostRegister ADD/CMD
5. PostRegister Control
6. PostRegister CK

The PreRegister ADD/CMD and CTRL group includes A0-A17, BA0-BA1, BG0-BG1, ACT_n, C0-C2, PAR- ITY, CSx_n, CKEx, and ODTx.

The PostRegister ADD/CMD group includes A0-A17, BA0-BA1, BG0-BG1, ACT_n, C0-C2, and PARITY. The PostRegister CTRL group includes CSx_n, CKEx, and ODTx.

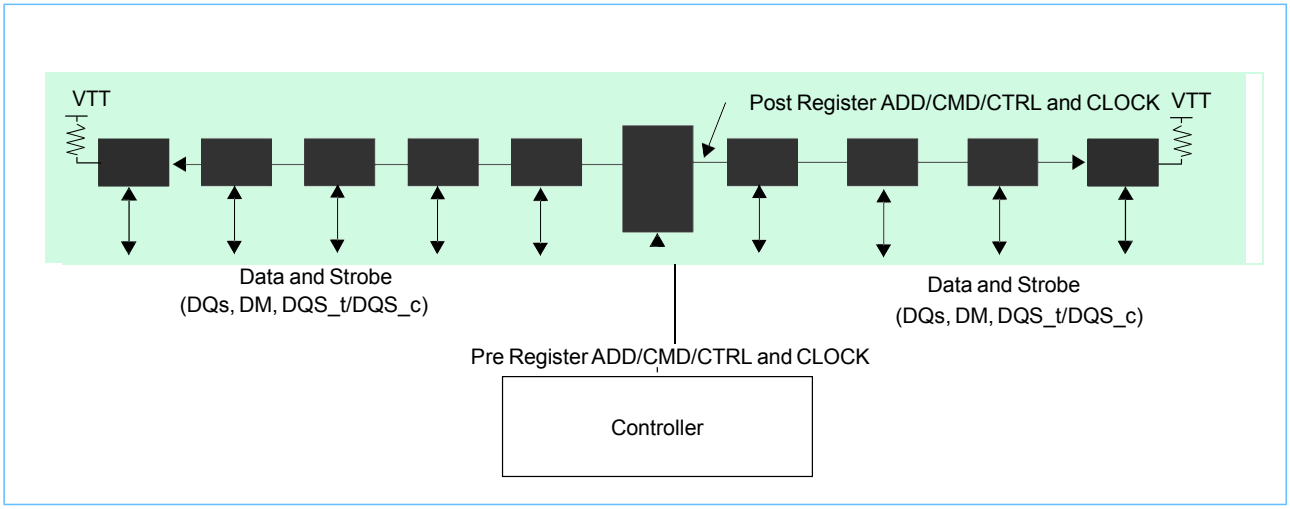


Figure 3 — Example RDIMM Topologies

6.2 General Net Structure Routing Rules

The usual design process should be followed to develop an adequate design. Simulations are typically required and timing budgets considered to verify adequate performance. Documenting line lengths alone does not ensure another design using those same line lengths will meet the intended speed. This is because there are parameters that are not documented that affect the design, such as vias, length of the via path, routing layers used, and how the actual line lengths fall within the minimum and maximum line length range. The design goal is to specify a tight range for a specific buss that has a well-controlled time relationship to the other critical signals, for example ADD/CMD to Clock.

For DDR4 the approach to documenting RDIMM timing will be primarily simulation based for buses. Small groups of signals may be documented in terms of length only. One signal in each group will be documented in terms of length. Through simulation, the other signals in the group will be adjusted such that the timing skew of

the group is less than a specified number. This number will be identified and documented for each group.

The skew number is not a goal but merely a result of the design effort that produces a module meeting the intended speed.

Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace segment length table that defines the length for a selected signal of the group.

To use simulation almost exclusively, some conditions must be defined so that the same conclusion is reached using different simulation tools. See Table 10 for a definition of the simulation environment. Any simulation conditions that differ from Table 10 must be documented in the respective annex.

Table 10 — Simulation Conditions

Group	Parameter	Condition
DQ	Motherboard Length	100 mm
	Motherboard Impedance	50 Ω
	Motherboard Configuration	One DIMM slot
	Routing Type	Stripline
	Driver	34 Ω SDRAM with SDRAM package (A different driver must be documented)
PreRegister	Motherboard Length	100 mm
	Motherboard Impedance	60 Ω
	Motherboard Configuration	One DIMM slot
	Driver	34 Ω SDRAM with SDRAM package (A different driver must be documented)
PreRegister Clock	Motherboard Length	100 mm
	Motherboard Impedance	100 Ω differential
	Motherboard Configuration	One DIMM slot
	Driver	34 Ω SDRAM with SDRAM package (A different driver must be documented)
PostRegister ADD/CMD	Driver	Register
PostRegister CTRL	Driver	Register
PostRegister CK[2]	Driver	Register

Note 1 Any deviations from these conditions must be documented in the respective annex.
Note 2 Typically, this group will be defined by length only.

6.2.1 Clock, Control, and Address/Command Groups

The DDR4 modules implement a fly-by topology for routing CK, CTRL, and ADD/CMD signal groups. Each group, CK, ADD/CMD, and CTRL, will be documented separately. This division is based on loading differences and rate differences. For the case where the loading is the same between ADD/CMD and CTRL, the CTRL group may or may not be included in the ADD/CMD group.

6.2.2 PreRegister ADD/CMD and CTRL

All signals except clock can be taken as a group, since loading and signal rate are the same across ADD/CMD, and CTRL. Clock will be documented separately, based on it having a different rate and different termination, and it being routed as a differential pair.

Simulations should be done at typical conditions. This is to be an uncoupled simulation. Crosstalk is to be

ignored. An alternating one-zero pattern should be used. Only steady state conditions should be included. To do this, remove the first several clock periods. Remove the first five cycles if uncertain. For this group, VREFCA should be used as the threshold for determine skew. Measure the time between the first and last signal crossing VREFCA. This is the skew to be documented.

Figure 4 illustrates the topology for the PreRegister ADD/CMD and CTRL. It will be used in conjunction with Table 11 to document the timing requirements for this group.

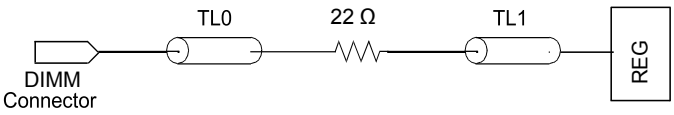


Figure 4 — Example PreRegister ADD/CMD and CTRL Diagram

.

Table 11 — Example PreRegister ADD/CMD and CTRL Definition

Signal	TL0	TL1	TL0+TL1	Timing Skew (ps)
A0	3.0	17.0	20.0	32

Note 1 Length tolerance is ± 0.8 mm.
Note 2 Signal A0 may be anywhere within this span.

6.2.3 PreRegister CK

Clock is documented separately, based on it having a different rate and different termination, and it being routed as a differential pair.

Figure 5 illustrates the topology for the PreRegister CK. It will be used in conjunction with Table 12 to define the requirements for this group. Since it is a single signal, a timing skew is not required and length alone will be used.

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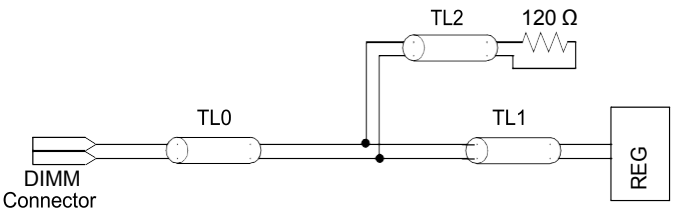

Figure 5 — Example PreRegister CK Diagram

Table 12 — Example PreRegister CK Length

Signal	TL0	TL1	TL2	TL0 + TL1
CK0_t	3.0	17.0	3.0	20.0

Note 1 Routing tolerance to be ± 0.8 mm.

Table 12 — Example PreRegister CK Length

Signal	TL0	TL1	TL2	TL0 + TL1
CK0_c	3.1	16.9	3.0	20.0

Note 1 Routing tolerance to be ± 0.8 mm.

6.2.4 PostRegister ADD/CMD

Loading differences generally require the ADD/CMD group to be treated separately form the CTRL group. If the loading for the CTRL group is the same as the ADD/CMD group, the CTRL group and the ADD/CMD group may be treated as a single group. The ADD/CMD group is further divided into a left side and a right side group. In some cases, the left side and the right side may be treated the same, but most cases will likely require these to be handled separately. Document the length of one signal in the group. Use simulation to determine the skew of the group.

Simulations should be done at typical conditions. This is to be an uncoupled simulation. Crosstalk is to be ignored. An alternating one-zero pattern should be used. Only steady state conditions should be included. To do this, remove the first several clock periods. Remove the first five cycles if uncertain. For this group, VREFCA should be used as the threshold for determining skew. Where there are multiple ranks, rank 0 will be used to define skew. All rank 0 SDRAM locations must be evaluated separately. The maximum skew for all rank 0 SDRAMs is to be the skew documented. One method is graphical, where all signals for a group at one SDRAM are plotted. Measure the time between the first and last signal crossing VREFCA. This is the skew for this DRAM. Repeat this for all rank 0 SDRAMs. The maximum is the skew to be documented.

Figure 6 illustrates the topology for the PostRegister ADD/CMD. It will be used in conjunction with Table 12 to define the requirements for this group.

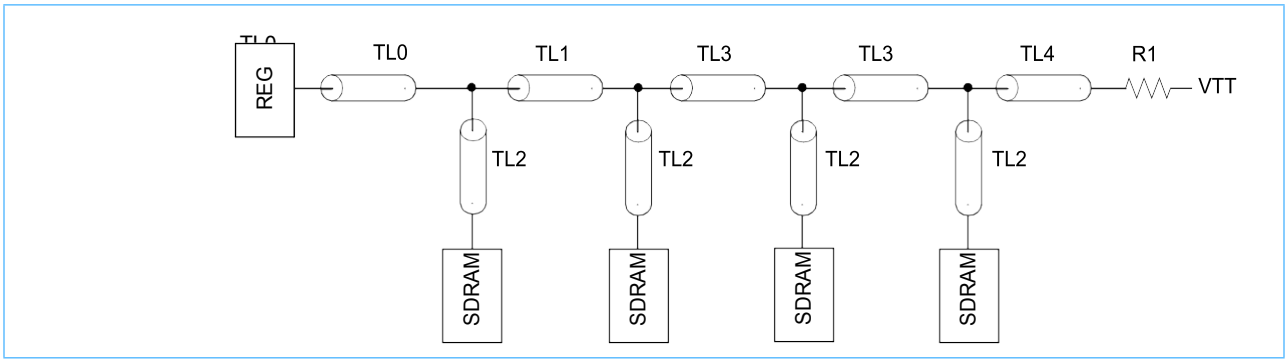

Figure 6 — Example PostRegister ADD/CMD Diagram

Table 13 — Example PostRegister ADD/CMD Definition

Signal	TL0	TL1	TL2	TL3	TL4	R1	Timing Skew (ps)
A12	21.0	15.0	3.0	14.0	10.7	39 Ω	93

Note 1 Signal A12 may be anywhere within this skew.

6.2.5 PostRegister CTRL Group

This group will use the same approach as the PostRegister ADD/CMD Group. It will typically be documented separately. Refer to the PostRegister ADD/CMD Group section for details. If the CTRL group has the same loading as the ADD/CMD group, they may be treated as one group.

6.2.6 DQ Group

This group contains the DQ signals and the respective strobes. This also includes the CB signals with the respective strobes.

There are 9 or 18 subgroups that are identified based on each strobe. Each subgroup will be called a lane. For x4 based DIMMs, each lane is a nibble. For x8 based DIMMs, each lane is a byte. The strobe for each lane will be documented using length. One net within each lane will also be documented in length. A timing skew will be documented for each lane. Table 14 depicts an example case for DQ Definition. The values in this table are fictitious. Actual values are to be determined by the reference design sponsor.

Simulations should be done at typical conditions. This is to be an uncoupled simulation. Crosstalk is to be ignored. An alternating one-zero pattern should be used. Only steady state conditions should be included. To do this, remove the first several clock periods. Remove the first five cycles if uncertain. For this group, a threshold is determined by looking at the cross point of the rising and falling edges in an eye pattern. Select a threshold that would provide the smallest skew. Where there are multiple ranks, only evaluate the timing for SDRAMs making up rank 0. Measure the time between the first and last signal crossing. This is the skew for this lane. Repeat this for each lane. The maximum skew for each lane is to be documented.

DQS is not to be included in the skew measurement. For x8 based modules, include DBI_n in the skew measurement.

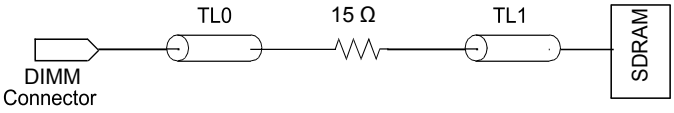

Figure 7 — Example DQ Net Structure

Table 14 — Example DQ Definition

Signal	T0	T1	T0 + T1	Bus	DQ Timing Skew[1] (ps)
DQS0_t, DQS0_c	3	15	18	-	-
DQ0	3.5	15	18.5	DQ[7:0], DBI0_n	15
DQS1_t, DQS1_c	4	17	22	-	-
DQ8	4.3	16.5	20.8	DQ[15:8], DBI1_n	18
DQS2_t, DQS2_c	3	15	18	-	-
DQ16	3.5	15	18.5	DQ[23:16], DBI2_n	16
DQS3_t, DQS3_c	3	15	18	-	-
DQ24	3.5	15	18.5	DQ[31:24], DBI3_n	12
DQS4_t, DQS4_c	3	15	18	-	-
DQ32	3.5	15	18.5	DQ[39:32], DBI4_n	9
DQS5_t, DQS5_c	3	15	18	-	-
DQ40	3.5	15	18.5	DQ[47:40], DBI5_n	18
DQS6_t, DQS6_c	3	15	18	-	-
DQ48	3.5	15	18.5	DQ[55:48], DBI6_n	14
DQS7_t, DQS7_c	3	15	18	-	-
DQ56	3.5	15	18.5	DQ[63:56], DBI7_n	17
DQS8_t, DQS8_c	3	15	18	-	-
CB0	3.5	15	18.5	CB[7:0], DBI8_n	21

Note 1 Skew excludes DQS.

6.3 Plane Referencing

Table 15 — Plane Referencing

Signals	Reference	Notes
DQ, DQS	Ground	
Address, Command, Control and VREFCA	VDD	
Clock	VDD	

6.4 Address Mirroring

DDR4 RDIMMs will use address mirroring. Where possible, SDRAMs for even ranks will be placed on the front side of the module. SDRAMs for odd ranks will be placed on the back side of the module. Wiring of the address bus will be as defined in Table 16.

Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a "load mode" operation, the specific address is required. This requires the controller to know if the rank is mirrored or not. There is a bit assignment in the SPD that indicates whether the module has been designed with the mirrored feature or not. See the DDR4 SPD-TSE specification for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the odd ranks.

Table 16 — DIMM Wiring Definition for Address Mirroring

Signal Name	SDRAM Ball Label		Comment
Connector	Even Rank	Odd Rank	
A0	A0	A0	
A1	A1	A1	
A2	A2	A2	
A3	A3	**A4**	
A4	A4	**A3**	
A5	A5	**A6**	
A6	A6	**A5**	
A7	A7	**A8**	
A8	A8	**A7**	
A9	A9	A9	
A10/AP	A10/AP	A10/AP	
A11	A11	**A13**	
A12/BC_n	A12/BC_n	A12/BC_n	
A13	A13	**A11**	
A14/WE_n	A14/WE_n	A14/WE_n	
A15/CAS_n	A15/CAS_n	A15/CAS_n	
A16/RAS_n	A16/RAS_n	A16/RAS_n	
A17	A17	A17	Only valid for x4 based DIMMs with SDRAMs components above 8 Gb.
BA0	BA0	**BA1**	
BA1	BA1	**BA0**	
BG0	BG0	**BG1**	
BG1	BG1	**BG0**	

6.5 DQ Mapping to Support CRC

For DDR4, a CRC feature has been added to support higher speeds. Generally, when using CRC, the bit order is 1:1 between the source and the destination. This is not true for DIMMs, where the bit order is somewhat random based on minimizing routing to maximize signal integrity. The CRC computation is based on a byte. For x4 based SDRAMs, the computation is truncated to 4 bits, a nibble. See DDR4 SDRAM specification JESD79-4 for a more complete explanation of how CRC is implemented. To fix the mapping issue, the host must understand the bit order at the SDRAM to map the DQ bits into the CRC generator for WRITE commands so that the SDRAM will decode the CRC correctly. The same is true for READs.

When there is more than one rank on a DIMM, the even ranks are on the front and the odd ranks are on the back. When SDRAMs are placed back to back and are of a different package rank, the DQ relationship between the even ranks and the odd ranks are fixed. To reduce the number of variations in the DQ mapping, the following rules are defined.

Rule 1: Bits within a nibble must stay together.

Rule 2: Nibbles may be swapped within a byte.

Rule 3: Definition of mapping is for rank 0 only. All even ranks have the same DQ mapping. Even rank to odd rank mapping is to swap bit 0 with 1, swap bit 2 with 3, swap bit 4 with 5, and swap bit 6 with 7.

For DIMMs that use 3DS components, the rank definition applies to package ranks. The additional die within a 3DS component are logical ranks and are part of one package rank. Another way of looking at this is that each chip select (CSx_n) used is one package rank. Where there is only one package rank, that rank may be placed on the front or the back or split between the front or back. Table 17 defines rank 0 mapping and therefore fully defines all DIMMs with one package rank.

There is one case that does not comply with Rule 3. A dual rank x4 VLP RDIMM with traditional DDP would not comply. It has 2 ranks. It uses traditional stacking so that each die in the stack is a separate package rank. The mapping of rank 0 to rank 1 is one to one and does not use the swaps as described in Rule 3 for the even versus odd ranks. This card is not defined as a reference card, so Rule 3 is valid for all reference designs defined so far.

18 bytes of the SPD are allocated for holding the DQ mapping information, one byte for each nibble of the DIMM connector. See Table 17. The table exactly specifies which DQ bits are in each nibble. The DQ Map Index refers to the specific map that is defined in Table 18.

Use of CRC is an optional feature. If a DIMM does not support CRC, values of 0x00 must fill the table. It is required that all reference designs support CRC.

Table 17 — SPD DQ Nibble Map for CRC

SPD Content - 18 bytes allocated (Example values)									
SPD Address	DQ Bits	DQ Map Index (Hex)[1]	SPD Address	DQ Bits	DQ Map Index (Hex)	SPD Address	DQ Bits	DQ Map Index (Hex)
60	DQ[0-3]	0x2B	66	DQ[24-27]	TBD	72	DQ[40-43]	TBD
61	DQ[4-7]	0x15	67	DQ[28-31]	TBD	73	DQ[44-47]	TBD
62	DQ[8-11]	0x0C	68	CB[0-3]	TBD	74	DQ[48-51]	TBD
63	DQ[12-15]	0x35	69	CB[4-7]	TBD	75	DQ[52-55]	TBD
64	DQ[16-19]	TBD	70	DQ[32-35]	TBD	76	DQ[56-59]	TBD
65	DQ[20-23]	TBD	71	DQ[36-39]	TBD	77	DQ[60-63]	TBD

Note 1 This column illustrates the values that the SPD might hold. These values are an example but do correlate with the values in the additional tables and figures.

The DQ Map table defines all possible mappings following Rule 1 and Rule 2. For x4 based DIMMs, there are 24 mappings. These are represented by DQ Map Index values 0x01 through 0x18. Offsetting by 1 allows 0x00 to be used to indicate that mapping using the table is not supported. For x8 based DIMMs, there are 48 mappings and the entire table is used. Note that the there is a gap between the left side of the table and the right side (0x19 to 0x20). These DQ Map Index values are invalid. All the values above 0x38 are invalid.

CRC is defined for x8 based components and x4 based components. For the purpose of CRC, x16 components are treated as two separate x8 components. Similarly a x32 component would be treated as four separate x8 based components. The definition for CRC can be found in the JESD79-4 specification for DDR4 SDRAMs.

Table 18 — Nibble/Byte DQ Map Patterns for CRC

DQ Map Index (Hex)	Connector - bit within nibble				DQ Map Index (Hex)	Connector - bit within nibble			
	0	1	2	3		0	1	2	3
	SDRAM bit					SDRAM bit			
0x01	0	1	2	3	0x21	4	5	6	7
0x02	0	1	3	2	0x22	4	5	7	6
0x03	0	2	1	3	0x23	4	6	5	7
0x04	0	2	3	1	0x24	4	6	7	5
0x05	0	3	1	2	0x25	4	7	5	6
0x06	0	3	2	1	0x26	4	7	6	5
0x07	1	0	2	3	0x27	5	4	6	7
0x08	1	0	3	2	0x28	5	4	7	6
0x09	1	2	0	3	0x29	5	6	4	7
0x0A	1	2	3	0	0x2A	5	6	7	4
0x0B	1	3	0	2	0x2B	5	7	4	6
0x0C	1	3	2	0	0x2C	5	7	6	4
0x0D	2	0	1	3	0x2D	6	4	5	7
0x0E	2	0	3	1	0x2E	6	4	7	5
0x0F	2	1	0	3	0x2F	6	5	4	7
0x10	2	1	3	0	0x30	6	5	7	4
0x11	2	3	0	1	0x31	6	7	4	5
0x12	2	3	1	0	0x32	6	7	5	4
0x13	3	0	1	2	0x33	7	4	5	6
0x14	3	0	2	1	0x34	7	4	6	5
0x15	3	1	0	2	0x35	7	5	4	6
0x16	3	1	2	0	0x36	7	5	6	4
0x17	3	2	0	1	0x37	7	6	4	5
0x18	3	2	1	0	0x38	7	6	5	4

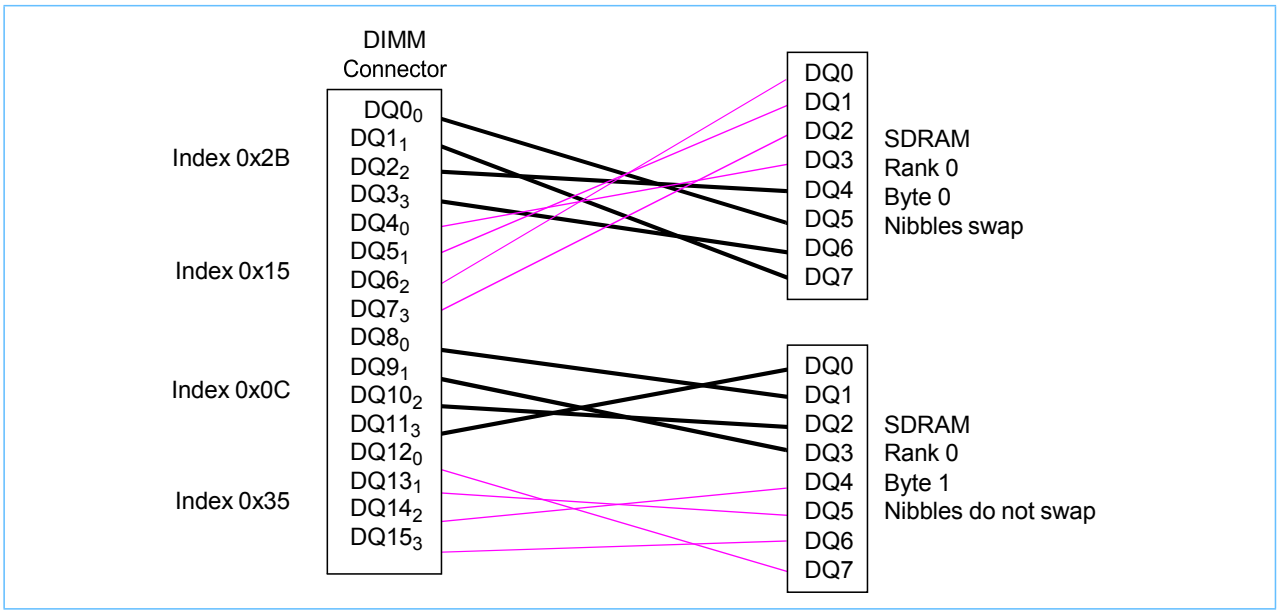

Figure 8 — Example of DQ Wiring with Mapping for CRC

Table 19 — Example of DQ Mapping for CRC

DQ bit of DIMM Connector

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
First x8 SDRAM								Second x8 SDRAM											

5	7	4	6

DQ mapping for first nibble matches index 0x2B.

0x2B would be stored in the SPD table for the first nibble.

3	1	0	2

DQ mapping of second nibble matches index 0x15.

0x15 would be stored in the SPD table for the second nibble.

1	3	2	0

0x0C for the 3rd nibble.

0x35 for the fourth nibble.

7	5	4	6

6.6 DIMM Routing Space Constraints

These are the physical rules for traces and space including keepout requirements.

Preferred rules are to be used whenever possible. Exceptional rules are only to be used when necessary. Exceptional rules when applied are to only be used in the area of the board where they are required and preferred rules used in all other areas. Where preferred rules cannot be used, it is encouraged that the most conservative rules be used up to the exceptional rules. Rules falling between preferred and exceptional are considered exceptional.

When exceptional rules are used, it must be noted in the annex for each specific raw card. It is preferred that additional details be included to identify the areas of the card that use exceptional rules.

These rules are for design of the reference card only. It is not required that these rules be met by individual manufacturers building from the reference designs.

Table 20 — Routing Space Constraints

Feature	Preferred (mm)	Exceptional (mm)	Comment
Via Size Large - Drill	0.250	0.250	
Via Size Large - Pad	0.450	0.450	
Via Size Large - Anti-pad	0.700	0.700	
Via Size Large – Solder mask	Designer preference	Designer preference	Solder mask openings are easy to change.
Via Size Small - Drill	0.200	0.200	
Via Size Small - Pad	0.400	0.400	
Via Size Small - Anti-pad	0.600	0.600	
Via Size Small – Solder mask	Designer preference	Designer preference	Solder mask openings are easy to change.
Solder mask opening (for pad)	Designer preference	Designer preference	Solder mask openings are easy to change.
Solder mask opening (cover adjacent trace)	Designer preference	Designer preference	Solder mask openings are easy to change.
Pad to pad spacing for pads of different components that are soldered down	0.250	0.200	Concern is solder bridging
Line to pad spacing	0.125	0.100	
Line to line spacing (single ended)	0.100	0.100	
Line to line spacing (differential)	0.100	0.090	
Line to shape spacing	0.200	0.125	
Shape to shape spacing	0.200	0.100	
Via to BGA pad	0.175	0.150	Copper to copper
Via to non-BGA pad	0.150	0.125	Copper to copper
Via to Via	0.200	0.150	Copper to copper
Drill wall to drill wall (nominal)	0.400		
Drill wall (nominal) to board edge (nominal)	0.500		
SDRAM (nominal) to SDRAM (nominal)	0.350	0.300	

Table 20 — Routing Space Constraints (Cont'd)

Feature	Preferred (mm)	Exceptional (mm)	Comment
SDRAM (nominal) to board edge (nominal)	0.400	0.300	
Copper to board edge (nominal)	0.300	0.250	
Component pad to board edge (nominal)	0.400	0.400	
Lower board edge to passive pad or component of less than 0.80 mm height	4.150	4.000	
Lower board edge to component body (nominal) of greater than 0.80 mm height	4.200	4.000	For RDIMMs, this is not likely required.
Minimum trace width on outer layers	0.090	0.075	Related to cross section shape
Minimum trace width on inner layers	0.075	0.075	Related to cross section shape

6.7 DIMM Physical Requirements

6.7.1 Via Size

Use of the smaller via (0.200 drill) will be typical.

6.7.2 Component Pad Sizes and Geometry

If 0201 size passive components are required, the pad size will be 0.4 mm square with a 0.2 mm space between the pads for each component.

Pads for all other components are left to the reference card designer to define. Manufacturers of these RDIMM reference designs may adjust pad sizes and geometry.

6.7.3 SDRAM Package Size

Maximum SDRAM package size affects the DQ trace length and placement of decoupling capacitors.

For DDR4 LP RDIMM reference designs with SDRAMs in a single row, a maximum package size of 11.0 mm nominal width and 13.0 mm nominal height will be used. Individual reference designs may have different requirements.

For DDR4 LP RDIMMs with 2 rows of SDRAMs and DDR4 VLP RDIMMs, the SDRAM package size will be defined by the respective reference design sponsor.

6.7.4 Clock Termination

Post register termination for differential clocks will use two resistors, one connected to each side, the true signal (_t) and the complementary signal (_c), of the differential pair. The other side of each resistor will be connected together and to a capacitor. The other side of the capacitor will be connected to the reference plane for the differential pair. This will usually be VDD. The capacitor value will be 0.01 µF.

On RDIMMs where room for 3 components for clock termination is not available, a single resistor may be used between the true signal (_t) to the complementary signal (_c). This is considered an exception and must be documented in the Design Specification Annex.

Termination on the host side will use a single 120 Ω resistor across the differential pair. The termination resistor should be located close to the register.

6.7.5 DQ Resistor

There will be a 15 Ω series resistor between the connector and SDRAMs.

6.8 RDIMM Configuration

6.8.1 Control Wiring

The following figures define the required control wiring for various reference designs. For designs not covered in the following figures, the Design Specification Annex must include this equivalent information in a clear manner.

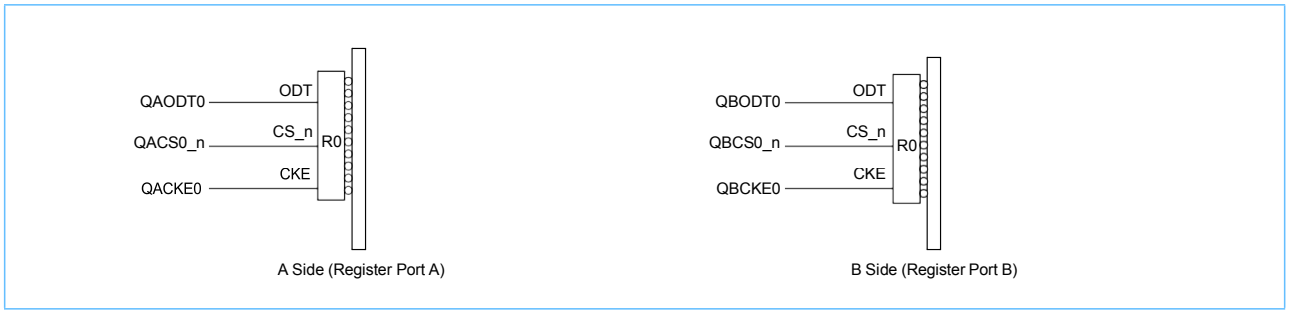

Figure 9 — DDR4 SRx8 Control Wiring

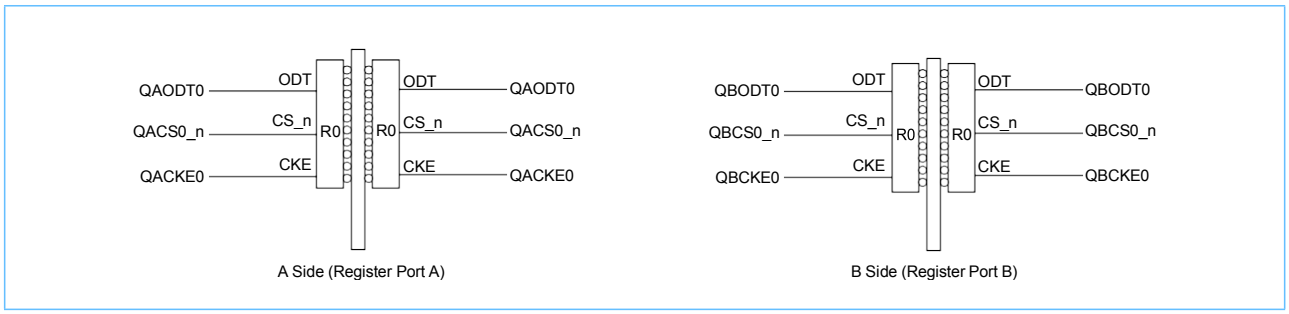

Figure 10 — DDR4 SRx4 Control Wiring

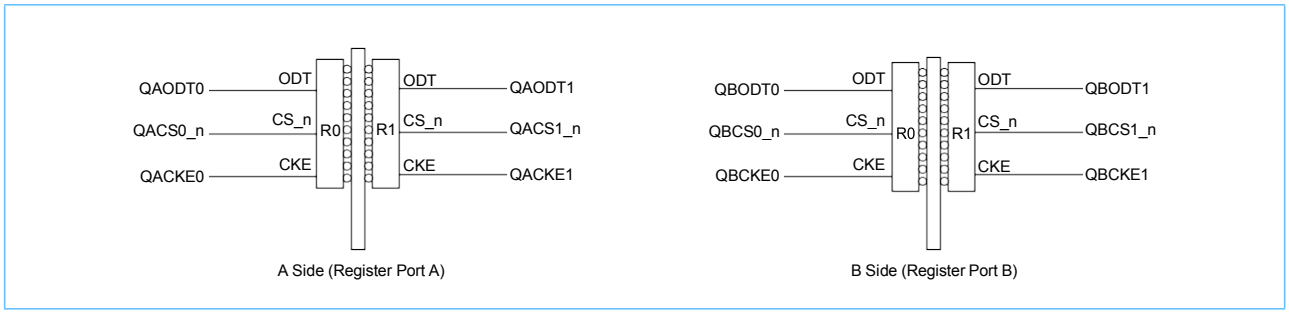

Figure 11 — DDR4 DRx8 Control Wiring

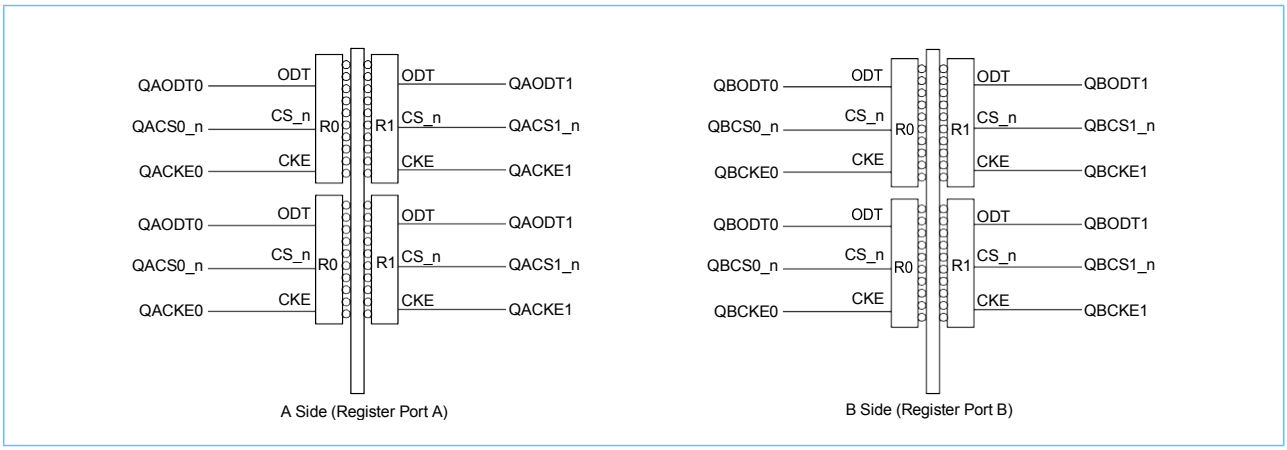

Figure 12 — DDR4 2R/4R/8R/16R (planar/3DS) Control Wiring

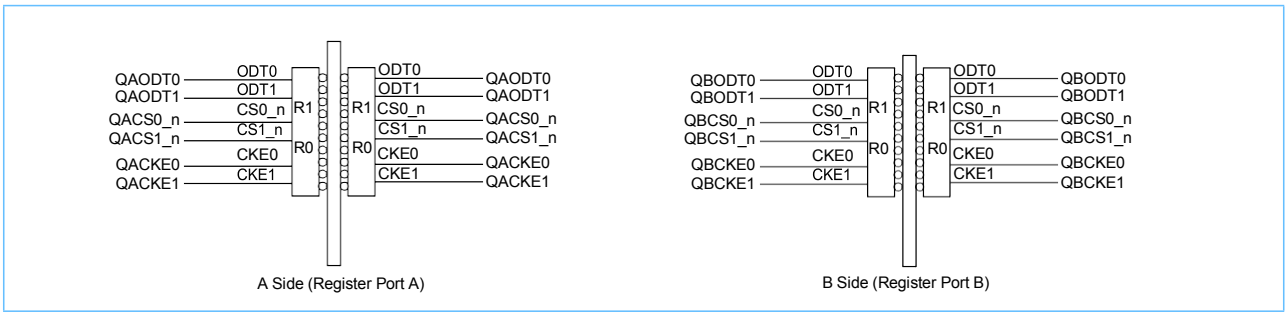

Figure 13 — DDR4 2R VLP (DDP) Control Wiring

6.8.2 AVDD Filter Circuit, Placement and Wiring

VDD and VSS via comprising a AVDD filter network should not have connection to VDD and VSS on the outer layers. On the outer layers, the vias only connect to filter components and AVSS pin of register (as depicted in Figure 14).

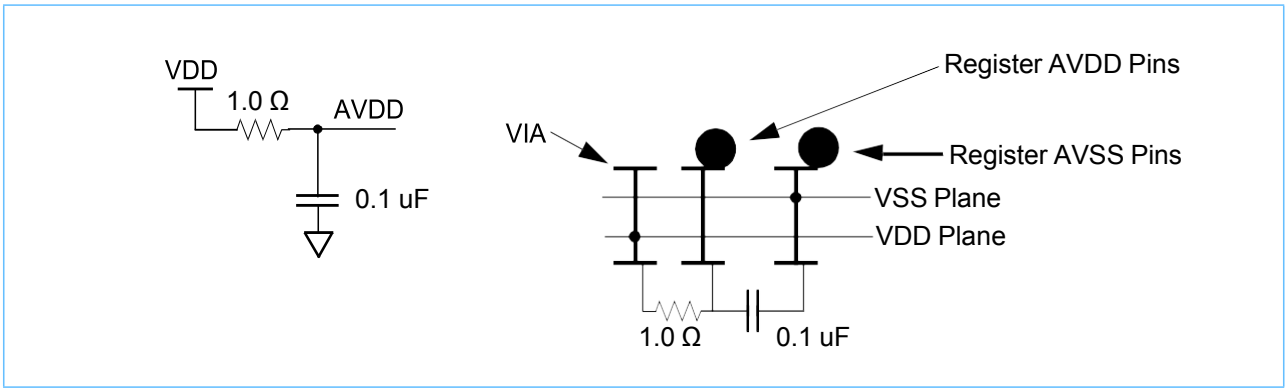

Figure 14 — AVDD Filter Circuit Wiring

6.8.3 ZQ Calibration Wiring

The DDR4RCD01 register has a ZQCAL pin. This is intended to calibrate the on die resistors for the drivers and the terminations. All RDIMMs must connect a 240 Ω ± 1% resistor from this pin of the register to ground (VSS).

The DDR4 SDRAMs have a ZQ pin. This is intended to calibrate the on die resistors for the drivers and the terminations. All RDIMMs must connect a 240 Ω ± 1% resistor from this pin of the SDRAM to ground (VSS). Each SDRAM package must have its own ZQ resistor. Sharing is not allowed.

6.8.4 ALERT_n Circuit Wiring

ALERT_n will be wired as a long fly-by connection with the register at one end. Connections will be from the ALERT_n pin of the SDRAMs to the ERROR_IN_n pin of the register. There will be a pullup resistor to VDD at the end farthest electrically from the register. There will be a filter capacitor at the register end near the register. This circuit should be simulated to verify clean signal edges. Figure 15 demonstrates typical wiring for this circuit.

The ALERT_n output of the register is connected to the ALERT_n pin of the connector.

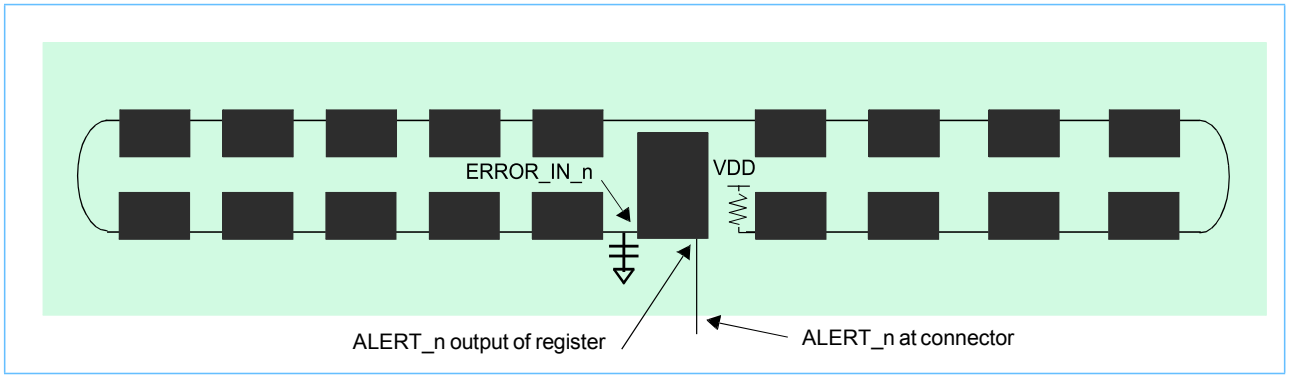

Figure 15 — Example Wiring of the ALERT_n Function

6.8.5 TEN Pin Wiring

The TEN pin is a test enable pin. This function is not used for SDRAMs mounted on RDIMMs. It must be tied low.

6.9 SPD-TSE Selection, Wiring and Placement

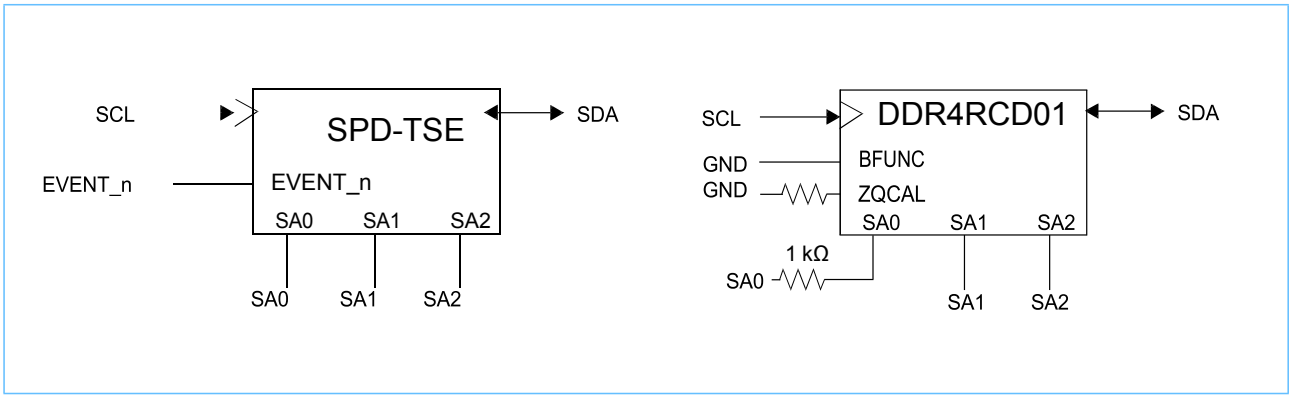

Figure 16 — Block Diagram: SPD-TSE and DDR4RCD01

SPD-TSE signals must be wired to the register. Wiring of SA0 to the register requires a series 1K Ω resistor.

RDIMMs will use a combined SPD-TSE with wiring as shown in Figure 16. Wiring for BFUNC defines the I2C address space. Wiring to ground is intended for applications that use a single register.

On low-profile, 31.25 mm DIMMs, the thermal sensor and serial presence detect footprint will be placed near the center of the DIMM.

TDFN packages are used for the thermal sensor and the serial presence detect. MO-229, variations W2030D-3, V2030D-3, and U2030D, will be referenced for the thermal sensor and serial presence detect part.

7 Serial Presence Detect

This section is included for convenience. Please refer to the DDR4 SPD specification in JESD21C, Section 4.1.

7.1 Serial Presence Detect Definition

The Serial Presence Detect function must be implemented on the DDR4 SDRAM RDIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR4 Module Serial Presence Detect Specifications. Please refer to this document for all technical specifications and requirements of the Serial Presence Detect devices.

The following is the SPD address map for all DDR4 modules. It describes where the individual lookup table entries will be held in the serial EEPROM. Consistent with the definition of DDR4 generation SPD devices which have four individual write protection blocks of 128 bytes in length each, the SPD contents are aligned with these blocks as follows:

Table 21 — SPD Address Map

Block	Range		Description
0	0-127	0x000-0x07F	Base Configuration and SDRAM Parameters
1	128-255	0x080-0x0FF	Module Specific Parameters -- See annexes for details
2	256-319	0x100-0x13F	Reserved -- must be coded as 0x00
	320-383	0x140-0x17F	Manufacturing Information
3	384-511	0x180-0x1FF	End User Programmable

Table 22 — Block 0: Base Configuration and SDRAM Parameters

Byte Number		Function Described
0	0x000	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage
1	0x001	SPD Revision
2	0x002	Key Byte / SDRAM Device Type
3	0x003	Key Byte / Module Type
4	0x004	SDRAM Density and Banks
5	0x005	SDRAM Addressing
6	0x006	SDRAM Package Type
7	0x007	SDRAM Optional Features
8	0x008	SDRAM Thermal and Refresh Options
9	0x009	Other DRAM optional features
10	0x00A	Reserved -- must be coded as 0x00
11	0x00B	Module Nominal Voltage, VDD
12	0x00C	Module Organization
13	0x00D	Module Memory Bus Width
14	0x00E	Module Thermal Sensor

Table 22 — Block 0: Base Configuration and SDRAM Parameters (Cont'd)

Byte Number		Function Described
15-16	0x00F-0x010	Reserved -- must be coded as 0x00
17	0x011	Time bases
18	0x012	SDRAM Minimum Cycle Time (t_{CKAVG}min)
19	0x013	SDRAM Maximum Cycle Time (t_{CKAVG}max)
20	0x014	CAS Latencies Supported, First Byte
21	0x015	CAS Latencies Supported, Second Byte
22	0x016	CAS Latencies Supported, Third Byte
23	0x017	CAS Latencies Supported, Fourth Byte
24	0x018	Minimum CAS Latency Time (t_{AA}min)
25	0x019	Minimum RAS to CAS Delay Time (t_{RCD}min)
26	0x01A	Minimum Row Precharge Delay Time (t_{RP}min)
27	0x01B	Upper Nibbles for tRASmin and t_{RC}min
28	0x01C	Minimum Active to Precharge Delay Time (t_{RAS}min), Least Significant Byte
29	0x01D	Minimum Active to Active/Refresh Delay Time (t_{RC}min), Least Significant Byte
30	0x01E	Minimum Refresh Recovery Delay Time (t_{RFC1}min), LSB
31	0x01F	Minimum Refresh Recovery Delay Time (t_{RFC1}min), MSB
32	0x020	Minimum Refresh Recovery Delay Time (t_{RFC2}min), LSB
33	0x021	Minimum Refresh Recovery Delay Time (t_{RFC2}min), MSB
34	0x022	Minimum Refresh Recovery Delay Time (t_{RFC4}min), LSB
35	0x023	Minimum Refresh Recovery Delay Time (t_{RFC4}min), MSB
36	0x024	Minimum Four Activate Window Time (t_{FAW}min), Most Significant Nibble
37	0x025	Minimum Four Activate Window Time (t_{FAW}min), Least Significant Byte
38	0x026	Minimum Activate to Activate Delay Time (t_{RRD_S}min), different bank group
39	0x027	Minimum Activate to Activate Delay Time (t_{RRD_L}min), same bank group
40	0x028	Minimum CAS to CAS Delay Time (t_{CCD_L}min), same as bank group
41-59	0x029-0x03B	Reserved -- must be coded as 0x00
60-77	0x03C-0x04D	Connector to SDRAM Bit Mapping
78-116	0x04E-0x074	Reserved -- must be coded as 0x00
117	0x075	Fine Offset for Minimum CAS to CAS Delay Time (t_{CCD_L}min), same bank group
118	0x076	Fine Offset for Minimum Activate to Activate Delay Time (t_{RRD_L}min), same bank group
119	0x77	Fine Offset for Minimum Activate to Activate Delay Time (t_{RRD_S}min), different bank group
120	0x078	Fine Offset for Minimum Activate to Activate/Refresh Delay Time (t_{RC}min)
121	0x079	Fine Offset for Minimum Row Precharge Delay Time (t_{RP}min)

Table 22 — Block 0: Base Configuration and SDRAM Parameters (Cont'd)

Byte Number		Function Described
122	0x07A	Fine Offset for Minimum RAS to CAS Delay Time (t_{RCD}min)
123	0x07B	Fine Offset for Minimum CAS Latency Time (t_{AA}min)
124	0x07C	Fine Offset for SDRAM Maximum Cycle Time (t_{CKAVG}max)
125	0x07D	Fine Offset for SDRAM Minimum Cycle Time (t_{CKAVG}min)
126	0x07E	CRC for Base Configuration Section, Least Significant Byte
127	0x07F	CRC for Base Configuration Section, Most Significant Byte

8 Product Label

This section is included for convenience.

The following labels shall be applied to all DDR4 memory modules to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggg, are to be omitted when not needed.

Voltage options in field 'v' describe the nominal voltage VDD of the SDRAMs and support components (excluding the SPD-TSE). Values for these voltages are 'operable' which means the device characteristics such as timing are supported at this voltage, or 'endurant' which means that the device may be powered to that voltage level without damage, however should not be used as operation is not guaranteed at the higher voltage.

DDR4 DIMM Label Format:

ggg**GB** phe**Rx**ff **PC4**v-wwwwaa-mccd-bb

Where:

ggg**GB** = Module total capacity, in gigabytes, for primary bus (ECC not counted)
1GB, 2GB, 4GB, etc. (no space between digits and units)

phe**R** = Number of package ranks of memory installed and number of logical ranks per package rank.
p =
1 = 1 package rank of SDRAMs installed
2 = 2 package ranks of SDRAMs installed
3 = 3 package ranks of SDRAMs installed
4 = 4 package ranks of SDRAMs installed
h = blank for monolithic DRAMs, else for modules using stacked DRAM:
h = DRAM package type
S = single load DRAM stacking (3DS)
D = multi-load DRAM stacking (DDP),
Q = multi-load DRAM stacking (QDP)
e = blank for SDP, DDP and QDP, else modules using 3DS stacks, logical ranks per package rank
2 = 2 logical ranks in each package rank
4 = 4 logical ranks in each package rank
8 = 8 logical ranks in each package rank
R = rank(s)

xff = Device organization (data bit width) of SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
x16 = x16 organization

v = SDRAM and support component supply voltage (VDD)
blank = 1.2 V operable
L = TBD V operable, TBD V endurant

wwww = Module speed in Mb/s/data pin
1600, 1866, 2133, 2400, 2666, 2933, 3200

aa = SDRAM speed grade
aa = Speed grade, i.e., J, K, L, etc.

m = Module Type
A = Unbuffered 16-bit Small Outline DIMM (“16b-SO-DIMM”), x16 data bus
B = Unbuffered 32-bit Small Outline DIMM (“32b-SO-DIMM”), x32 data bus
C = Registered 72-bit Small Outline DIMM ("72b-SO-RDIMM”), x64 primary + 8 bit ECC module data bus
E = Unbuffered DIMM ("UDIMM"), x64 primary + 8 bit ECC module data bus
L = Load Reduced DIMM (“LRDIMM”), x64 primary + 8 bit ECC module data bus
N = Mini registered DIMM (“Mini-RDIMM”), x64 primary + 8 bit ECC module data bus
R = Registered DIMM ("RDIMM"), x64 primary + 8 bit ECC module data bus
S = Small Outline DIMM ("SO-DIMM"), no ECC (x64 bit module data bus)
T = Unbuffered 72-bit Small Outline DIMM ("72b-SO-DIMM"), x64 primary + 8 bit ECC module data bus
U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
W = Unbuffered Mini DIMM (“Mini-UDIMM”), x64 primary + 8 bit ECC module data bus

cc = Reference design file used for this design (if applicable)
A = Reference design for raw card ’A’ is used for this assembly
B = Reference design for raw card ’B’ is used for this assembly
AC = Reference design for raw card ’AC’ is used for this assembly
ZZ = None of the JEDEC standard reference designs were used for this assembly

d = Revision number of the reference design used
0 = Initial release
1 = First revision
2 = Second revision
P = Pre-release or Engineering sample
Z = To be used when field cc = ZZ

bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM

Examples:

16GB 2Rx4 PC4-2133N-RA2-11

16 GB DDR4 RDIMM

2 package ranks per DIMM using SDP SDRAMs x4 data organization per SDRAM

1.2 V operable

DDR4-2133 performance

Speed grade N: CAS Latency = 14

Raw card reference design file A registration 2 used for the assembly DDR4 SPD revision 1.1

16GB 2S2Rx4 PC4-2133N-RB1-10

16 GB DDR4 RDIMM

2 package rank of SDRAMs using single load stacked SDRAMs

2 logical ranks per package rank of x4 data organization per SDRAM

1.2 V operable

DDR4-2133 performance

Speed grade N: CAS Latency = 14

Raw card reference design file B registration 1 used for the assembly DDR4 SPD revision 1.0

8GB 1Rx4 PC4L-2400R-RC1-10

8 GB DDR4 RDIMM

1 package rank using SDP SDRAMs x4 data organization per SDRAM TBD V operable, 1.2 V endurant DDR4L-2400 performance

Speed grade R: CAS Latency = 18

Raw card reference design file C registration 1 used for the assembly DDR4 SPD revision 1.0

8GB 1Rx8 PC4-2400U-RD0-11

8 GB DDR4 RDIMM

1 package rank per DIMM using SDP SDRAMs x8 data organization per SDRAM

1.2 V operable

DDR4-2400 performance

Speed grade U: CAS Latency = 18

Raw card reference design file D registration 0 used for the assembly DDR4 SPD revision 1.1

32GB 2DRx4 PC4-2400U-RJ0-11

32 GB DDR4 RDIMM

2 package ranks per DIMM, using DDP multi-load stacked SDRAMs x4 data organization per SDRAM

1.2 V operable

DDR4-2400 performance

Speed grade U: CAS Latency = 18

Raw card reference design file J registration 0 used for the assembly DDR4 SPD revision 1.1

9 JEDEC Process

JEDEC provides PCB reference designs for DIMM modules. The designs are divided into families one of which is Registered DIMMs (RDIMMs). Letters (A, B, C etc.) are used to define specific configurations (raw cards) of modules such as 2 rank with x4 based SDRAMs. Additional characteristics may further refine cards into specific raw card (R/C) letters. Letter assignments are arbitrary and usually chronological. There is no other association to the letter assignments.

R/Cs are reviewed and balloted by JEDEC members before being placed on the JEDEC website as reference designs. This is called registration. The initial registration is 0. A specific card may be the registration of R/C A0. Subsequent design updates to the reference design go through the same balloting process and increment the registration number from 0 to 1 or the next highest number.