writeup.md

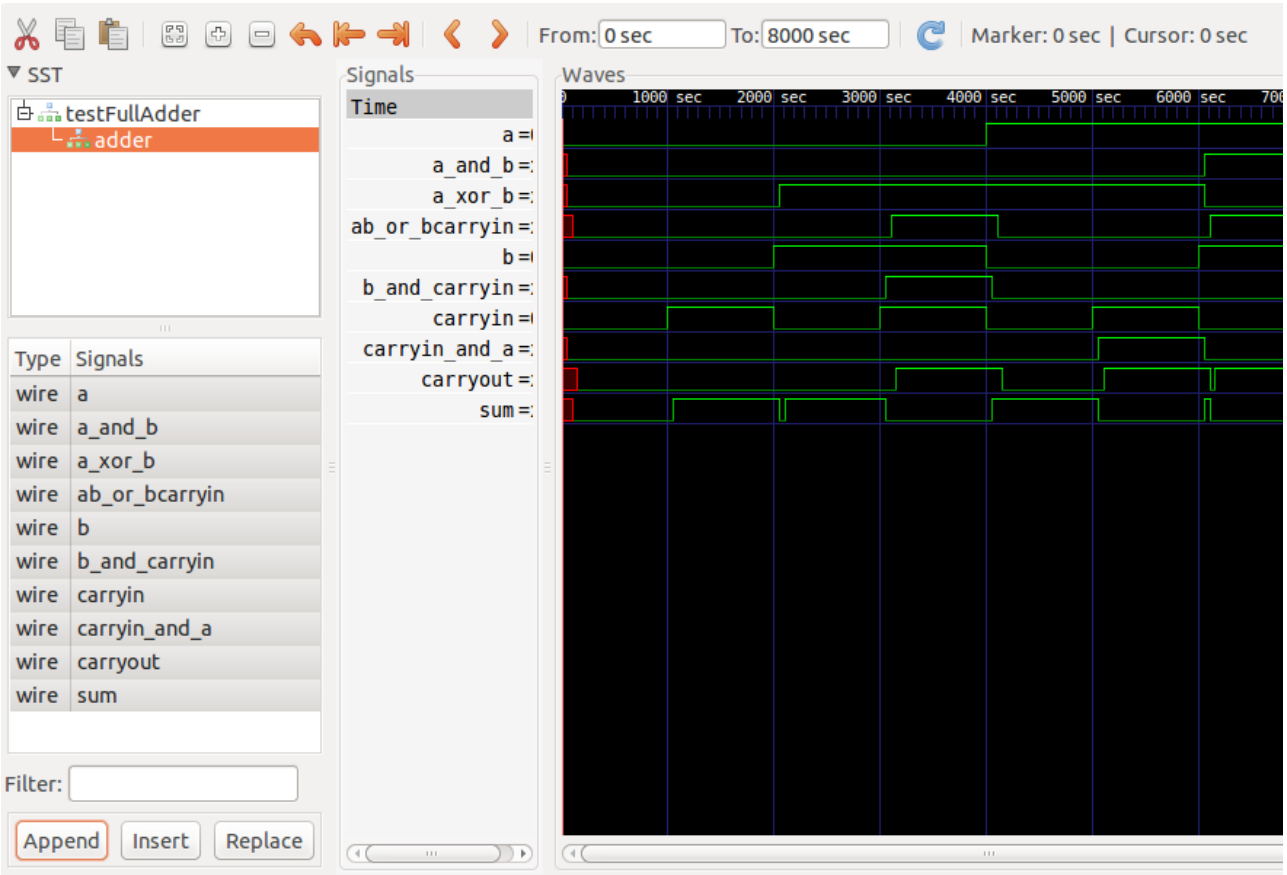
Setup

1. Compile the verilog files with `make`
2. Run the test cases using `make test`
3. Waveforms can be inspected with `gtkwave some-file.vcd`

Results

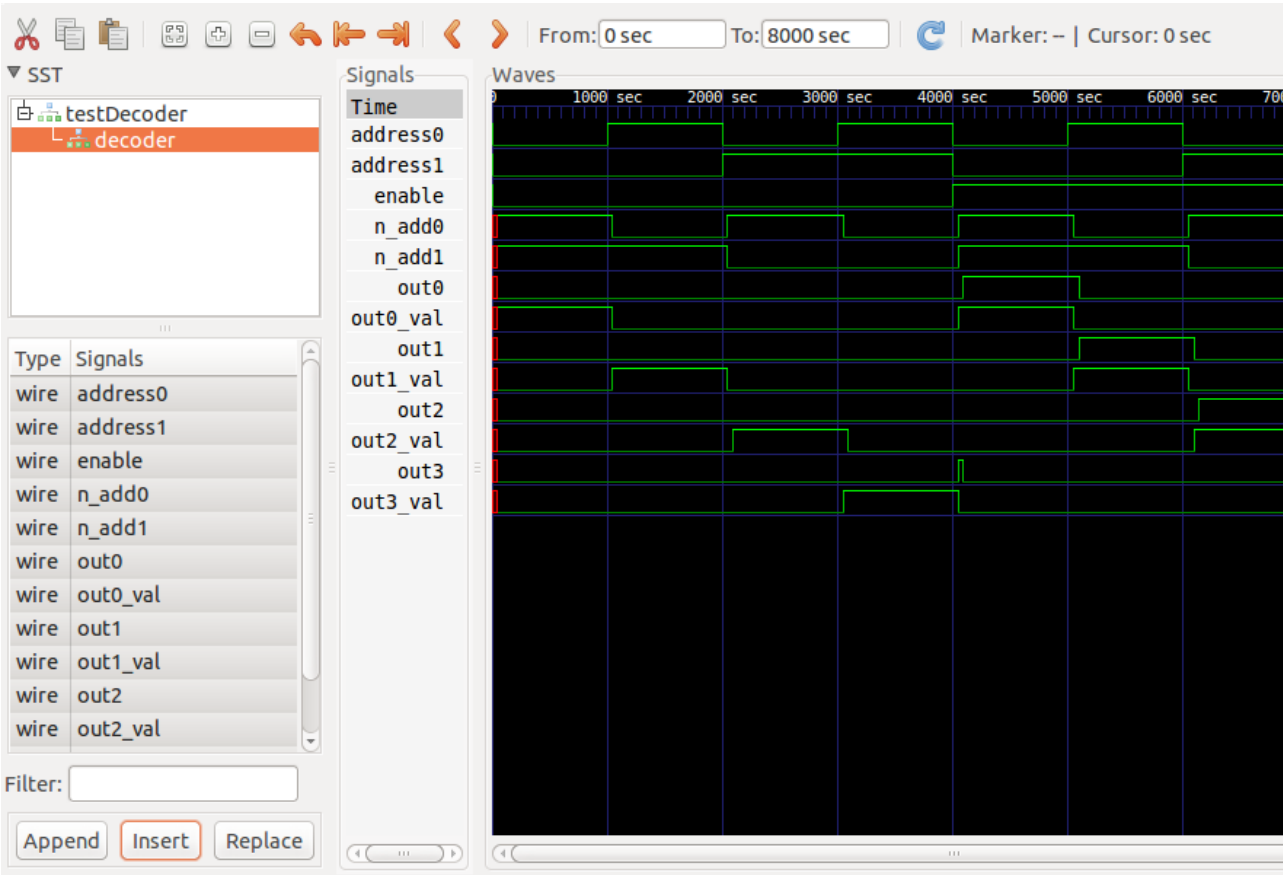
Adder

a	b	carryin	carryout	sum	Expected carryout	Expected sum
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	1	1	0	1	0
1	1	0	1	0	1	0
1	1	1	1	1	1	1



Decoder

En	A0	A1	O0	O1	O2	O3	Expected Output
0	0	0	0	0	0	0	All false
0	1	0	0	0	0	0	All false
0	0	1	0	0	0	0	All false
0	1	1	0	0	0	0	All false
1	0	0	1	0	0	0	O0 Only
1	1	0	0	1	0	0	O1 Only
1	0	1	0	0	1	0	O2 Only
1	1	1	0	0	0	1	O3 Only



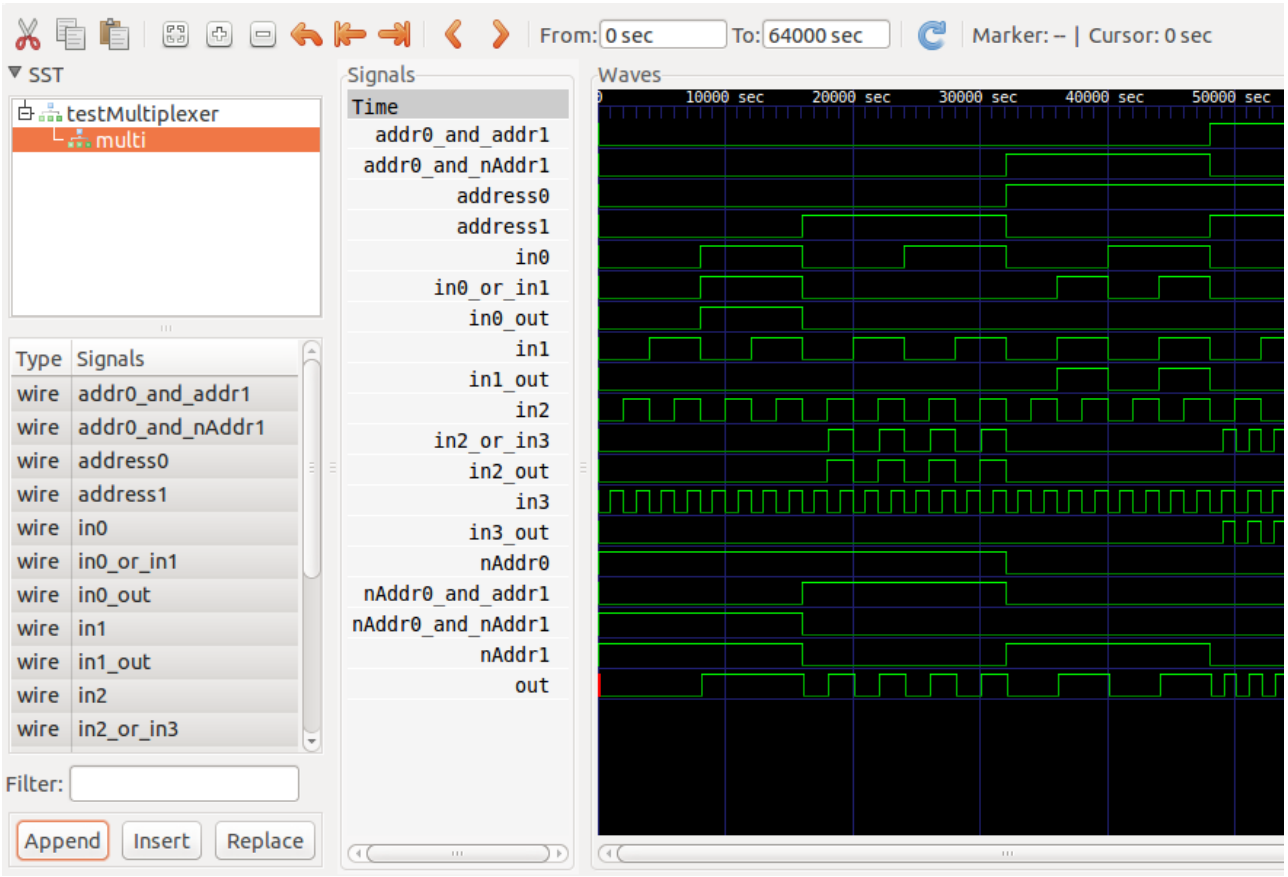
Multiplexer

address0	address1	in0	in1	in2	in3	out	Expected Output
0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0
0	0	0	0	1	1	0	0
0	0	0	1	0	0	0	0
0	0	0	1	0	1	0	0
0	0	0	1	1	0	0	0
0	0	0	1	1	1	0	0

address0	address1	in0	in1	in2	in3	out	Expected Output
0	0	1	0	0	0	1	1
0	0	1	0	0	1	1	1
0	0	1	0	1	0	1	1
0	0	1	0	1	1	1	1
0	0	1	1	0	0	1	1
0	0	1	1	0	1	1	1
0	0	1	1	1	0	1	1
0	0	1	1	1	1	1	1
0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	0	1	0	1	1
0	1	0	0	1	1	1	1
0	1	0	1	0	0	0	0
0	1	0	1	0	1	0	0
0	1	0	1	1	0	1	1
0	1	0	1	1	1	1	1
0	1	1	0	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	0	1	0	1	1
0	1	1	0	1	1	1	1
0	1	1	1	0	0	0	0

address0	address1	in0	in1	in2	in3	out	Expected Output
0	1	1	1	0	1	0	0
0	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	0	1	1	0	0
1	0	0	1	0	0	1	1
1	0	0	1	0	1	1	1
1	0	0	1	1	0	1	1
1	0	0	1	1	1	1	1
1	0	1	0	0	0	0	0
1	0	1	0	0	1	0	0
1	0	1	0	1	0	0	0
1	0	1	0	1	1	0	0
1	0	1	1	0	0	1	1
1	0	1	1	0	1	1	1
1	0	1	1	1	0	1	1
1	0	1	1	1	1	1	1
1	1	0	0	0	0	0	0
1	1	0	0	0	1	1	1

address0	address1	in0	in1	in2	in3	out	Expected Output
1	1	0	0	1	0	0	0
1	1	0	0	1	1	1	1
1	1	0	1	0	0	0	0
1	1	0	1	0	1	1	1
1	1	0	1	1	0	0	0
1	1	0	1	1	1	1	1
1	1	1	0	0	0	0	0
1	1	1	0	0	1	1	1
1	1	1	0	1	0	0	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0
1	1	1	1	0	1	1	1
1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	1


From: 0 sec
To: 64000 sec
Marker: -- | Cursor: 0 sec
SST
testMultiplexer
multi
Type
Signals
wire addr0_and_addr1
wire addr0_and_nAddr1
wire address0
wire address1
wire in0
wire in0_or_in1
wire in0_out
wire in1
wire in1_out
wire in2
wire in2_or_in3
Filter:
Append
Insert
Replace
Signals
Time
addr0_and_addr1
addr0_and_nAddr1
address0
address1
in0
in0_or_in1
in0_out
in1
in1_out
in2
in2_or_in3
in2_out
in3
in3_out
nAddr0
nAddr0_and_addr1
nAddr0_and_nAddr1
nAddr1
out
Waves
10000 sec
20000 sec
30000 sec
40000 sec
50000 sec