Koç University
College of Engineering
ELEC 491 - Design Project Proposal

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Design, Benchmark and Tapeout of Microelectronic and Spintronic Circuits

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Abstract

Artificial Intelligence (AI) continues to revolutionize various industries, yet the ever-growing computational demands of AI-driven applications present significant challenges in terms of power efficiency and processing speed. As CMOS-based microelectronics approaches fundamental physical limitations due to quantum effects, alternative technologies such as spintronic computing have emerged as promising candidates for future hardware development. This project aims to explore and compare CMOS-based and spintronic logic circuits by designing and implementing three computational units: an Arithmetic and Logic Unit (ALU), a Discrete-Time Fourier Transform (DTFT) circuit, and a Multilayer Perceptron (MLP) for MNIST classification.

For the CMOS-based implementations, the circuits will be developed in VHDL, synthesized using Vivado, and optimized based on the results of logic synthesis, static timing analysis, and power analysis. The circuits being studied within the scope of this project will then have their final GDSII layout generated using either OpenLane or Synopsys. Concurrently, the spintronic implementations will utilize MuMax3, a computational micromagnetics solver, to model equivalent designs using spintronic logic gates. The project will follow a comparative approach in analyzing the results obtained from the synthesis and static timing analysis reports generated via OpenLane/Synopsys and the impact of magnetization dynamics, spin currents, and domain wall motion on computational efficiency for the circuits realized using Mumax3.

To assess the viability of spintronic computing as a successor to CMOS, key metrics such as power consumption, latency, and area footprint will be evaluated. The study's findings, along with layout images of spintronic circuits and the GDSII mask of the CMOS circuits, will be compiled into a final report to be presented. By demonstrating the feasibility of spintronic logic in AI and digital signal processing applications, this project will contribute to ongoing research in alternative computing paradigms beyond traditional CMOS technology.

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Section 1 Introduction

1.1 *Concept*

The rapid technological advancements in the field of artificial intelligence (AI) and digital signal processing spawned an ever-growing demand and search for scalable and efficient computational systems. Despite being the backbone of current digital system architectures, CMOS based microelectronics are approaching their physical limit. Scaling down silicon-based transistors is becoming progressively more difficult because of power dissipation, leakage currents and increasing fabrication complexity at sub-nanometer technology nodes [1]. This necessitates the examination of alternative approaches to sustain improvements in performance. One promising candidate for the future of hardware design is spintronics, which leverages spin properties of electrons to enable energy-efficient and high-speed logic operations [2].

One particularly promising advancement within spintronics which we will make use of in our project is skyrmion-based logic, which utilizes the unique topological properties of magnetic skyrmions to enable energy-efficient and high-speed computation [3]. Skyrmions are nanoscale, stable at room temperature and they can be manipulated with very low energy consumption. These magnetic textures can be used in nanowires in racetrack memory architectures to produce compact and high-density logic circuits [3]. The existence of a skyrmion in a bit space of a nanotrack corresponds to a logic high whereas its absence represents a logic low [4]. By using skyrmion dynamics for information processing, it is possible to surpass the fundamental limitations of CMOS technology.

This project aims to explore the functionality of spintronic circuits as a viable alternative to CMOS-based microelectronics by designing, implementing, and benchmarking three fundamental computational circuits with both microelectronic and spintronic architectures. The circuits we will implement are as follows:

1. **Arithmetic and Logic Unit (ALU)**
2. **Discrete-Time Fourier Transform (DTFT) Circuit**
3. **Multilayer Perceptron (MLP) for MNIST Classification**

For the CMOS-based implementation, the circuits will be designed using VHDL, synthesized in Vivado, and further optimizations for power, performance, and area will be performed. Afterwards, the circuits will be designed using OpenLane or Synopsys to extend the study into real-world hardware simulation and observe the actual performance of the circuits.

Parallel to the CMOS implementation, equivalent spintronic circuits will be modeled using MuMax3, which is a software designed to generate micromagnetics simulations. The spintronic designs will be based on the RTL schematics generated in Vivado, meaning that the RTL's for microelectronics and spintronics designs will be shared, and utilize skyrmion-based logic gates from [3] to achieve improved speed, energy conservation and minimal area usage. The project will compare and analyze key performance metrics such as power consumption, latency, and silicon area for the microelectronic and spintronic implementations of the three circuits. We aim to discuss whether spintronic applications are compelling alternatives to CMOS technologies for future computing applications.

This comparative analysis will highlight the advantages and disadvantages of spintronics and microelectronics, providing valuable insights into the practicality of spintronic computing. The outcomes of the project will be CMOS-based GDSII layouts, spintronic circuit visualizations, and benchmarking data as well as the physical implementation of at least one microelectronic circuit. The results obtained from this study will contribute to ongoing research in alternative computing architectures.

By highlighting the potential of skyrmion-based logic circuits, this project aims to support the development of beyond-CMOS technologies which offer high-performance computing solutions with low energy consumption.

1.2 *Objectives*

The primary objective of this project is to explore and compare two distinct circuit design paradigms—CMOS-based microelectronics and spintronic logic circuits—through the implementation of three computational circuits: an Arithmetic and Logic Unit (ALU), a Discrete-Time Fourier Transform (DTFT) circuit, and a Multilayer Perceptron (MLP) for MNIST classification. Upon successful completion, this project will provide an in-depth understanding of the fundamental differences between spintronic and microelectronic designs, along with a comparative analysis of key performance metrics such as static timing and power consumption. This research is particularly significant given the increasing computational demands of modern software applications, particularly in artificial intelligence, and the imminent limitations of CMOS technology due to quantum effects. As conventional CMOS-based architectures approach their physical constraints, it becomes imperative to explore potential alternatives, with spintronic computing emerging as a promising candidate for future hardware development.

The tangible outcomes of this project encompass the design, implementation, and comparative analysis of CMOS-based and spintronic logic circuits. The project will begin with a literature review and software tool setup, that is planned to be completed by the end of March 2, to establish a theoretical foundation and configure the necessary computational tools for both paradigms, mainly Vivado, OpenLane, Synopsys, and Mumax3. Given the team's unfamiliarity with MuMax3 and the concept of spintronic devices in general, additional tutorial videos will be reviewed to gain a comprehensive understanding of the working principles and syntax of this open-source, finite-difference-based micromagnetic simulation package [5].

Upon successful completion of the setup and literature review, ALU, DTFT, and MLP circuits will be developed using VHDL, and their functionality will be verified through synthesis and simulation using Vivado’s built-in tools, which is expected to be completed by the Preliminary Design Review (PDR). In parallel, one team member from our group will focus on implementing equivalent circuits using spintronic logic gates and modeling them using MuMax3. Due to its relatively simpler nature, the ALU circuit is planned to be implemented first, prior to extending to the other circuits. As all three circuits will also be physically realised, another member will convert VHDL codes to Verilog via GHDL, use Openlane or Synopsys for RTL-to-GDSII flow and adjust the floorplan in accordance with the generated synthesis and static timing analysis reports. If time permits, the remaining circuits will also be physically realized via OpenLane/Synopsys and the generated synthesis and timing results from OpenLane/Synopsys will be prioritized over Vivado’s reports, as OpenLane/Synopsys provides more realistic results since the circuit is physically realized using an existing technological node.

The microelectronic and spintronic implementations for at least two of the circuits are expected to be fully completed by the Critical Design Review (CDR). While working on the final circuit, we will focus on performing a comparative analysis of CMOS and spintronic designs to assess key performance metrics such as power consumption, latency, and area footprint as it will offer insights into the viability of spintronics for common applications. The findings through this comparative analysis, images depicting the layouts of the realized spintronic circuits alongside the GDS of the submitted CMOS circuit will be included in the final report and the findings will be presented during the demo day.

Meeting the deadlines reported above and having the synthesizable VHDL codes, realizable GDSs for the circuits, the spintronic circuit layouts and a comparative analysis of the power consumption, latency and area footprint of the circuits will indicate that we have met our objectives.

1.3 *Background*

The rapid advancement of computational technologies has greatly increased the demand for efficient circuit architectures that optimize speed, energy consumption, and silicon area utilization. Traditional microelectronic circuits which are mostly based on CMOS technology have been at the core of digital systems since their introduction to the field. However, as transistor sizes are reaching their limit [1], there has been an ongoing search for alternative computing systems. One of the promising alternatives is the field of spintronics. As previously mentioned, the primary objective of this project is to explore and compare these two circuit design paradigms: CMOS-based microelectronics and spintronics. By evaluating and comparing key performance metrics such as power consumption, latency, and area utilization, this research aims to provide valuable insights into the viability of spintronics, specifically skyrmions which are to be explained in the following, as a competitive alternative to CMOS technology.

1.3.1. Microelectronics

The microelectronic circuit serves as a basis for modern computing. It provides high-performance processing opportunities. Always seeking improvement has become central to microelectronic engineers. As a result, seeking greater scalability, reduced power consumption, and increased computing efficiency has ended up with the creation of a variety of circuit topologies.

Traditional microelectronic circuits rely on Complementary Metal-Oxide-Semiconductor (CMOS) technology. Since workloads become more complex day by day, CMOS devices have been scaled for more than 30 years. Transistor delay times decrease by more than 30% per technology generation which results in a doubling of microprocessor performance every two years [6]. As a result of this advancement, modern transistor technology has now scaled down to just a few nanometers in size. Given the ongoing trend, it is expected that transistor sizes will continue to shrink further than a few nanometers. However, as the architecture scales down, challenges such as increased leakage current, short-channel effects, and reliability concerns are introduced, limiting further advancements [6]. To address these challenges, engineers have implemented techniques such as clock gating, asynchronous processing, and dynamic voltage scaling (DVS) to enhance circuit efficiency [7]. A detailed explanation of these techniques is provided below:

Clock Gating: Clock gating is a power management technique for reducing power dissipation. It removes the clock signal from the circuit that does not need any clock signal. Clock gating saves energy by minimizing the clock tree.

Asynchronous Processing: The asynchronous processing technique provides an async environment to the system for running tasks independently without any queueing or handshaking process. This approach reduces significant power dissipation by maintaining a low-power state for idle circuit components.

Dynamic Voltage Scaling: DVS is a technique to reduce the average power consumption. This is performed by reducing the switching losses of the system by changing the frequency and voltage of the system.

Performance, power efficiency, and silicon area optimization are still research challenges despite these developments. The demand for energy-efficient and high-performance computational hardware is growing. Digital signal processing, embedded systems, and artificial intelligence require more resources than other applications. High-speed computation is currently possible with contemporary microelectronic circuits. Nevertheless, they frequently have to choose between latency, power consumption, and space limitations. Addressing these trade-offs has a significant role in enabling next-generation computing architectures.

Our project aims to tackle this challenge by designing, implementing, and evaluating three fundamental circuits:

1. **Arithmetic and Logic Unit (ALU):** It is the core component of processors and is responsible for executing arithmetic/logical operations. ALU efficiency directly improves overall processor performance.
2. **Discrete-Time Fourier Transform (DTFT) Circuit:** DTFT is used in digital signal processing. They enable frequency analysis of signals. Optimizing their design can lead to real-time signal

processing improvements.

3. **Multilayer Perceptron (MLP) for MNIST Classification:** A key neural network model for image recognition. An efficient MLP with an optimized kernel implementation can enhance AI inference capabilities.

In addition to all these, we plan to design the CMOS-based circuits we designed as an ASIC design. In this process, we will use the SKY130 Process Design Kit provided by Skywater as an open-source.

SkyWater SKY130 PDK: SKY130 is an outdated 180nm-130nm hybrid technology that has been utilized for many production parts. The technology is the 8th generation SONOS technology node (130nm). However, it has become available for everyone by SkyWater Technology Foundry. In this way, anyone who wants to do ASIC design can create their design using this PDK [8].

The project will also focus on evaluating the performance of these circuits using state-of-the-art microelectronic design methodologies. We aim to provide insights into optimizing hardware performance for different application domains by systematically analyzing power consumption, computational speed, and area utilization.

1.3.2. Spintronics

Recent technological advancements emerge a growing demand for larger data storage capacity and enhanced data processing speed to accommodate the continuously increasing workload of modern computational research. As stated by Moore's law, the number of transistors on a chip is expected to double in every 2 years. In the past years, this law played a significant role in performance improvement. However, silicon-based transistors are reaching their limit in terms of size. This necessitates the investigation of alternative approaches to keep performance growing [1]. One such emerging approach is spintronics, which offers promising advancements in this domain. The central theme in spintronics is the active manipulation of spin degrees of electrons in solid-state systems [2].

What is the Spin of an Electron?

The spin angular momentum, which quantifies the degree of intrinsic rotation of a particle, is a fundamental quantum mechanical property intrinsic to every elementary particle, composite particle and quasi particle. It is expressed in terms of the reduced Planck constant ħ. Electrons possess a quantized angular momentum of half of an ħ. Therefore, if we were to project the spin angular momentum of an electron on a quantization axis, we would have two projections: + ħ/2 and - ħ/2. The spin and charge of an electron together generate a magnetic moment which is directly proportional to the spin of the electron[9].

How Can We Use Spin in Real Technological Applications?

One of the most significant technological breakthroughs which enabled the implementation of spintronics in technological application is the development of spin valves, which exploit a phenomenon known as giant magnetoresistance (GMR). A spin wall consists of 2 ferromagnets separated by an insulator [9]. The magnetization of two ferromagnets can be set as either parallel or antiparallel to each other. In the case of the parallel magnetization of the device, when electrons are injected through the device, the spin progressively aligns along the magnetization of the first ferromagnetic layer, i.e. the reference layer, and the electrons flow through the second (free) ferromagnetic layer without significant scattering *(Fig. 1, right)*. In this setup, the overall resistance of the device is considerably low [9]. In the second case of a spin-valve, in which the magnetization of the ferromagnets is antiparallel, electrons become spin-polarized by the first layer. However, due to the opposing magnetization direction of the second layer, spin-polarized electrons encounter increased scattering and resistance, making them incapable of penetrating the second ferromagnetic layer *(Fig. 1, left)*. As a result, the overall resistance of the device significantly increases. The difference of resistance between parallel and antiparallel configurations of a spin valve is called the giant magnetoresistance (GMR). The GMR mechanism has been used to sense the magnetic states of hard drives and this led to a massive improvement of the storage capacity [9].

Another significant development in the field of spintronics that has enabled real-world applications is Magnetoresistive Random-Access Memory (MRAM). Unlike traditional semiconductor-based memory technologies, which rely on charge storage, MRAM encodes information through the magnetization state of ferromagnetic layers in a spin valve. A parallel configuration of the device corresponds to a bit value of "0" whereas antiparallel configuration stands for a bit value of "1" [9], as it can also be observed in Figure 1.

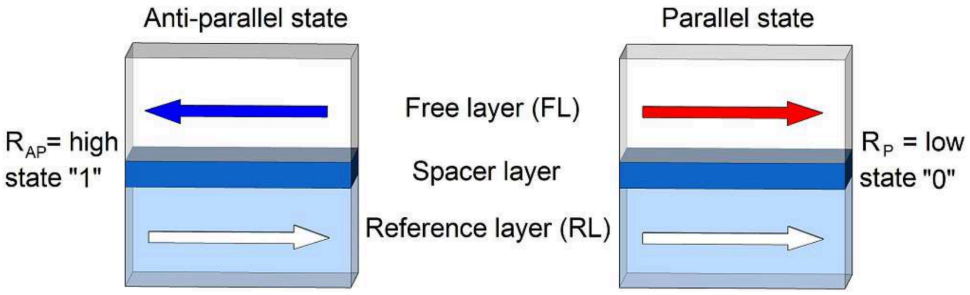

Figure 1: Schematic illustration of a spin valve in a high resistance (left) and low resistance (right) state [10]

Spin valves and MRAM contributed to crucial developments in advanced data storage and processing. However, these technologies still have limitations in terms of stability and power consumption. Manipulating spin states and changing logical bit values in traditional spin valves generally require transmissions of very large current [9], which leads to inefficiencies in energy usage. To overcome these challenges, alternative spintronic approaches have been explored. An alternative class of topological skin textures is magnetic skyrmions.

Skyrmions are nanometric magnetic textures which are capable of reaching high speed and are non-volatile at room temperature [3]. These topologies can be moved, generated, and destroyed using a current or magnetic field, which make them suitable for utilization in data storage and logic implementations [11]. Skyrmions are swirling electron spin configurations which can be observed in two different radial directions. Topological properties and different spin distributions of skyrmions are showcased in Figure 2.

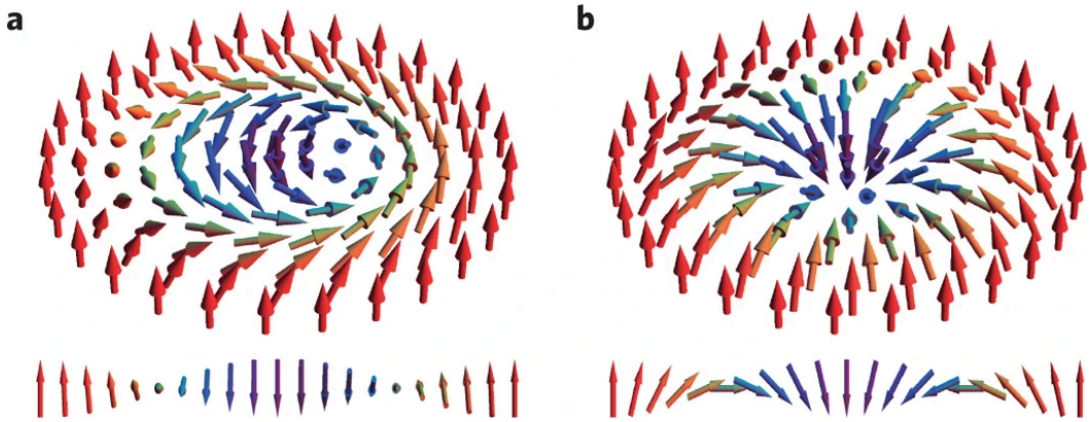

Figure 2: a) a Bloch-type skyrmion b) In a Néel-type skyrmion [12]

Skyrmions can be used in real life applications using a racetrack memory. Racetrack memory (RM) is a relatively new storage scheme in which information flows along a nanotrack. Bits in a racetrack memory are stored in subatomic "domains" between areas of magnetic charge on a nanowire [13]. Racetrack memory works by moving not the disk but rather the subatomic data domain [13]. The domains are positioned under a detector that reads binary information. A visual representation of racetrack memory and read/write operations can be seen in Figure 3. In a skyrmion-based racetrack memory (Sky-RM), binary information is encoded by a sequence of skyrmions [14]. A logic high "1" value can be obtained by placing a skyrmion on a space on the RT dedicated to a single bit whereas the absence of a skyrmion in a bit region corresponds to a logic low "0" [3].

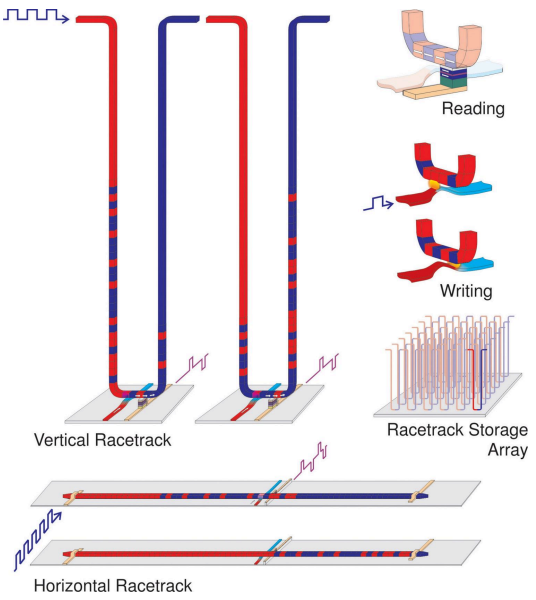

Figure 3: Racetrack Memory Design [12]

It is possible to design ferromagnetic skyrmion logic gates and circuits by analyzing and modifying skyrmion motion in nanowires under current-driven geometries. In a previous study [3], domain walls in magnetic tracks were utilized to either block or allow the propagation of a skyrmion to further regions. Thus, domain walls act as logic switches by either stopping or allowing skyrmion motion, similar to the behaviour of transistors in CMOS logic circuits. In certain regions of a circuit, a skyrmion's spin structure may get deformed due to mirror symmetry breaking, a structural asymmetry in the track. This causes conversion of incoming logic skyrmion bits into domain walls, affecting future skyrmion behaviour. These skyrmions, named as probing skyrmions, are introduced into the circuit specifically to interact with domain walls and regulate the timing of skyrmion motion. During this operation, probing skyrmions act similar to how a clock signal operates in traditional digital circuits [11].

One example logic gate application using skyrmions can be seen as displayed in Figure 4. The configuration in this figure belongs to an inverter gate. In the setup, the existence of a signal skyrmion determines the logic input and the motion of the probing skyrmion determines the output. In the case where there is a signal skyrmion and thus the input is logic high, a domain wall is generated from the signal skyrmion using current-induced magnetic domain expansion. The probing skyrmion gets blocked by the domain wall, therefore the output becomes a logic low. In the case where no domain wall gets generated (i.e. the signal skyrmion does not exist and the input is logic low), the probing skyrmion can propagate freely and yield a logic high output [4]. The inverter gate is not a universal gate in traditional logic, but for this application, we can create a NOR gate, which is universal and can be used to generate every other logic gate, by combining two inverters horizontally [3]. The track and skyrmion configuration for the NOR gate can be seen in Figure 5.

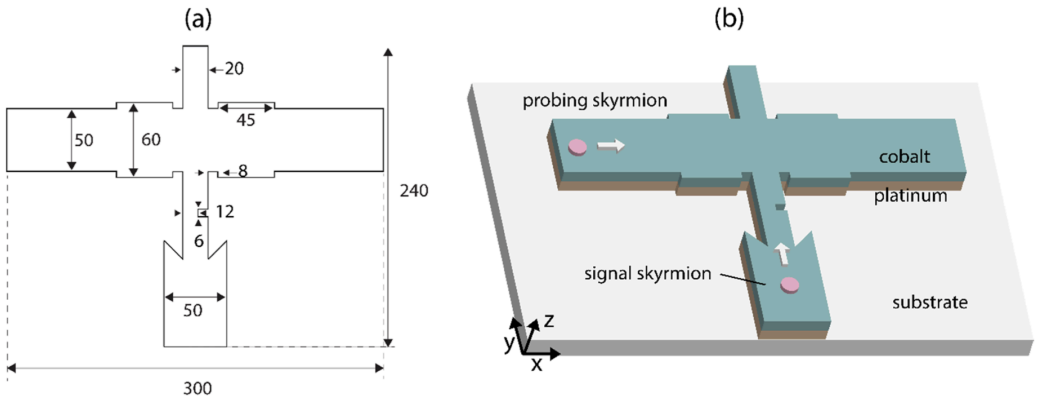

Figure 4: Schematic of the logic inverter gate and its materials: (a) dimensions of the device in nanometers and (b) a three-dimensional sketch of the device [4]

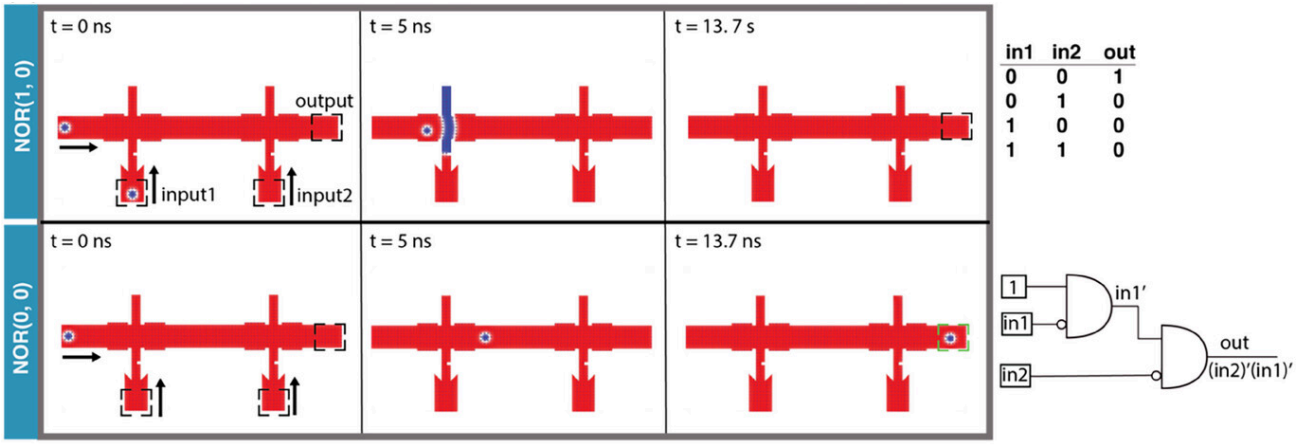

Figure 5: The NOR gate (generated by cascading two inverter gates and connecting the output of the first one to the non-inverted input of the second one) [3]

Throughout the project, we will be utilizing the "Scalable Low-Power Skyrmionic Logic Gate Library" in reference [3] as a foundation for our design and analysis. The logic circuits we will be using and simulating in MuMax3 will be dynamic magnetic systems, where magnetization evolves in response to external stimuli [4]. In order to properly conduct a performance analysis, it is mandatory to evaluate and understand the dynamic effect of these physical factors as well. The behaviours and dynamics of magnetic moments in a material medium are dictated by the Landau-Lifshitz-Gilbert (LLG) equation [4]. The formula for the LLG equation with torques transferred by current is outlined in Equation 1. In the formula, γ_{LL} stands for the gyromagnetic ratio for the LLG equation, whereas $\mathbf{B}_{\mathrm{eff}}$ is the effective magnetic field and α is the dimensionless Gilbert damping coefficient. τ_{ZL} and τ_{SI} are spin torque transfer (STT) terms for the Zhang-Li SST (for cases when the current is in-plane) and the Slonczewski STT (for cases when the current is perpendicular to plane) respectively [4].

$$\frac{d\mathbf{m}}{dt} = \gamma_{\mathrm{LL}} \frac{1}{1+\alpha^2} \left(\mathbf{m} \times \mathbf{B}_{\mathrm{eff}} + \alpha \left[\mathbf{m} \times \left(\mathbf{m} \times \mathbf{B}_{\mathrm{eff}}\right)\right]\right) + \tau_{\mathrm{ZL}} + \tau_{\mathrm{SI}}$$

Equation 1: Landau-Lifshitz-Gilbert (LLG) Equation

MuMax3 numerically solves the LLG equation using finite difference methods by utilizing the cuFFT library for calculating the magnetostatic field and the cuRAND library for generating random numbers on the GPU [15]. To advance the equation, the tool provides a number of methods with varying convergence rates [5]. The default method in MuMax3 for dynamical simulations -like our project- is the Dormand-Prince method (RK45). This method adaptively adjusts the time step to maintain the error rate as close to a predetermined value as possible [5]. This numerical approach is essential for accurately simulating skyrmion-based logic operations, which allows us to evaluate their feasibility as a replacement for conventional CMOS logic gates.

As demands for computing power keep increasing, CMOS-based microelectronics face increasing challenges due to physical limitations in transistor scaling. In our project, we aim to leverage the advantages of magnetic skyrmions to develop spintronic circuits which surpass the limitations of traditional CMOS-based logic gates. By integrating skyrmion-based logic into our design and comparing our results with the microelectronic implementations of the three circuits we chose, we aim to observe a dramatic improvement in energy efficiency, computational speed and area consumption.

Section 2 S/T methodology and associated work plan

2.1 *Methodology*

Given the multifaceted nature of this project—encompassing VHDL-based digital design, OpenLane for physical implementation, and MuMax3 for spintronic simulations—a structured approach is of utmost importance for the systematic design, implementation, and analysis of CMOS-based and spintronic circuit architectures. Due to the need for simulations and designs across different platforms, the project must be executed in parallel and divided into distinct phases, as detailed in the following sections. The evaluation of the obtained results should commence once sufficient theoretical and technical knowledge has been acquired, and these assessments should be carried out concurrently with the remaining simulations to ensure an efficient and iterative development process.

2.1.1. Literature Review and Software Tool Setup (Weeks 1-2)

An extensive literature review will be conducted to establish a strong theoretical foundation for both CMOS-based microelectronics and spintronic logic circuits. Team members will study key references on digital circuit design, magnetization dynamics, and previous research on spintronic logic gate implementation using MuMax3. Simultaneously, the necessary software tools for circuit design and simulation will be set up, including Vivado for FPGA-based synthesis, OpenLane/Synopsys for RTL-to-GDSII flow, and MuMax3 for computational micromagnetics. Given the team's lack of prior experience with MuMax3, additional tutorial resources will be reviewed to develop a comprehensive understanding of its working principles and syntax. Furthermore,as it is necessary for us to have a fundamental understanding of spintronics to effectively interpret MuMax3 simulation outputs, introductory-level spintronics courses, such as [8], will be followed. Similarly, as neither OpenLane nor Synopsys have not been previously used within the team, one project member will focus on gaining foundational knowledge and practical experience by simulating existing schematics before applying the tool to the circuit designs proposed in this study.

2.1.2. Design and Simulation of Memory Structures (Weeks 3-5)

Before implementing the DTFT and MLP in VHDL, Python scripts replicating their functionality will first be developed due to their relatively greater complexity compared to the ALU. Following this, the Python implementations will be converted to C++, serving as an intermediary step that would enable greater visibility of the underlying operations that might otherwise be abstracted by Python's high-level commands. This transition is expected to facilitate a smoother conversion to VHDL by helping us better understand the required logic at a lower level. Once the circuits are implemented in VHDL, testbenches will be developed to verify their correctness and functionality. Additionally, Vivado's built-in tools will be utilized for synthesis, generating the RTL schematic, and performing initial timing and performance analysis to assess design efficiency.

2.1.3. Control Unit and Data Path Design (Weeks 6-8)

If the lookup tables (LUTs) prove to be insufficient for storing the necessary weights, biases, for the MLP and precomputed sine and cosine values for the DTFT, we will proceed with implementing a small RAM module. The RAM module will be integrated into the datapath, allowing efficient communication between the computational units and their respective memory blocks. Additionally, a finite state machine (FSM) will be developed to handle memory read/write operations, ensuring proper sequencing of computations. Initially, this is planned to be designed in VHDL and simulated using Vivado and once the VHDL-based design is validated and optimized, the design will be transitioned to the GDSII implementation phase using OpenLane, where the datapath, memory access logic, and FSM will be further refined to suit ASIC constraints.

2.1.4. CMOS Circuit Physical Design Using OpenLane/Synopsys (Weeks 5-12)

To transition from the digital design to actual microelectronics implementation using OpenLane/Synopsys, the VHDL implementation for all three circuits will first be converted to Verilog using GHDL. A configuration file specifying the design parameters, that are to be decided by our professor, will be created to

facilitate the synthesis of the initial design. Following this, placement and routing will be carried out, and the design will be checked for any design rule violations, such as minimum spacing violations between metal layers or violations of the minimum feature size requirements for transistors.

Once the layout is finalized, the GDSII file will be verified using a layout viewer to ensure that it adheres to the fabrication requirements using SkyWater 130nm technology, although it will not be submitted due to unforeseen circumstances. This step within the project is of great significance, as OpenLane provides more accurate static timing analysis and performance reports compared to Vivado, given that it generates a physically realized design rather than a purely simulated one, hence can give more realistic insights for the comparison between two methodologies to be made.

2.1.5. Spintronic Circuit Design and Simulation (Weeks 3-13)

Since none of the team members have prior experience with spintronics, one member will first watch introductory lectures to develop a foundational understanding of spintronic principles. This will include learning how to solve the Landau-Lifshitz-Gilbert (LLG) equation for analyzing magnetization dynamics and spin current effects, as well as following MuMax3 tutorials to familiarize themselves with the tool.

In parallel, spintronic equivalents of the ALU, DTFT, and MLP circuits will be implemented using spintronic logic gates and simulated in MuMax3, a micromagnetic simulation software specifically designed for modeling magnetization processes at the nanoscale. In this approach, the RTL schematics generated via Vivado for microelectronic circuits will be utilized, meaning that both the microelectronic and spintronic designs will share the same RTL schematics. Subsequently, the standard cells within the RTL schematics will be replaced with their spintronic counterparts from the custom library developed in a previous study [3].

The ALU circuit, being the simplest and expected to have completed VHDL and OpenLane/Synopsys results, will be implemented first, followed by the more complex circuits. The gate layout, which is expected to be generated within the RTL schematics, will be replaced by spintronic equivalents of the respective circuits. Following this, the switching dynamics of the circuits will be simulated, and their feasibility will be evaluated using a verification tool for spintronic circuits that is to be decided later on.

2.1.6. Comparative Performance Analysis & Reporting (Weeks 7-13 & Week 14)

A benchmarking study will be conducted to compare the CMOS and spintronic implementations in terms of power consumption, latency, and area footprint to determine which design paradigm offers greater efficiency for specific applications. This analysis will also assess the feasibility of spintronic computing as a potential alternative to traditional CMOS-based architectures. The project will conclude with a report detailing the final CMOS and spintronic implementation choices, including design decisions and optimizations made throughout the process. Additionally, the GDSII layouts of the circuits will be included, along with the spintronic circuit layouts, simulation results and key findings from the benchmarking phase. These results will be formally presented during the demo day, where the potential of spintronic logic circuits will be showcased to demonstrate their viability as a next-generation computing solution.

2.2 *Work Package Descriptions*

Work package number	**1**	Start date or starting event:		**Week 1:** (17.02.2025)	
Work package title	**Literature Review and Software Tool Setup**				
Participant number	1	2	3		
Participant name	Damla Görgülü	İdil Görgülü	İsmet Erdem		
Weeks per participant	2	2	2		

Objectives

- Establish a strong theoretical foundation for both CMOS-based and spintronic logic circuits.
- Gain proficiency in software tools required for circuit design and simulation.
- Identify key challenges and prior research relevant to the project.

Description of work

T1.1 (w1-w2)

- Conduct a literature review on CMOS-based digital design, spintronic circuits, and relevant research papers on magnetization dynamics and spin current effects.

T1.2 (w1-w2)

- Study previous implementations of spintronic logic gates and micromagnetic simulations using MuMax3.

T1.3 (w1-w2)

- Set up and configure software tools, including Vivado (for FPGA-based synthesis), OpenLane (for RTL-to-GDSII flow), MuMax3 (for computational micromagnetics), and GHDL (for VHDL to Verilog conversion).

T1.4 (w1-w2)

- Follow introductory tutorials for MuMax3 and OpenLane to develop foundational knowledge before circuit design begins.

Deliverables

D1.1

- A document explaining basic concepts for introductory spintronics

D1.2

- A compilation of possible MLP designs for the MNIST classifier.

D1.3

- Verified installations for MuMax3, OpenLane, and Vivado.

Milestones

M1.1

- Completion of literature review and software tool setup.

Work package number	**2**	Start date or starting event:		**Week 3:** (03.03.2025)	
Work package title	**CMOS-Based Circuit Design Using VHDL**				
Participant number	1	2	3		
Participant name	Damla Görgülü	İdil Görgülü	İsmet Erdem		
Weeks per participant	3	3	3		

Objectives

- Develop and verify CMOS-based digital circuits (ALU, DTFT, MLP) in VHDL.
- Implement testbenches to ensure functionality.
- Perform synthesis, RTL schematic generation, and timing analysis using Vivado.

Description of work

T2.1 (w3)

- Experiment on different setups and based on the performance complexity trade-off decide on the number of neurons to be included in the MLP.

T2.2 (w3)

- Decide on the DTFT logic to be implemented.

T2.3 (w3-w4)

- Develop Python & C++ models for DTFT and MLP as an intermediary step.

T2.4 (w3-w5)

- Implement ALU, DTFT, and MLP in VHDL.

T2.5 (w4-w5)

- Verification using testbenches and simulation tools in Vivado.

T2.6 (w4-w5)

- Initial synthesis, timing analysis, and performance evaluation.

Deliverables

D2.1

- Functional Python and C++ implementations for DTFT, and MLP.

D2.2

- Functional VHDL implementations for ALU, DTFT, and MLP.

D2.3

- Verified simulation and synthesis reports from Vivado.

Milestones

M2.1

- Completion of Python and C++ codes describing the circuits.

M2.2

- Completion of VHDL design and verification.

M2.3

- Performance evaluation and refinement based on the generated reports before transitioning to physical design.

Work package number	**3**	Start date or starting event:		**Week 5:** (17.03.2025)	
Work package title	**CMOS Physical Design**				
Participant number	1	2	3		
Participant name	Damla Görgülü	İdil Görgülü	İsmet Erdem		
Weeks per participant	8	8	8		

Objectives

- Decide on whether to use OpenLane or Synopsys.
- Convert VHDL designs to Verilog for ASIC implementation.
- Perform floorplanning, placement, and routing in OpenLane/Synopsys.
- Prepare a final GDSII files for all circuits.

Description of work

T3.1 (w5)

- Decide on whether to use OpenLane or Synopsys.

T3.2 (w5)

- Convert VHDL files for the microelectronic circuits to Verilog using GHDL.

T3.3 (w6-w12)

- Perform placement, routing, and design rule checks in OpenLane.

T3.4 (w8-w12)

- Check the designs for Design Rule Violations and generate GDSII layouts as deliverables.

Deliverables

D3.1

- Synthesized Verilog designs.

D3.2

- Finalized GDSII layout for at least one circuit.

D3.3

- Static Timing Analysis ,Synthesis, Floorplanning, Placement, Routing Reports, Power Analysis and Final GDSII File & Signoff Reports

Milestones

M3.1

- Conversion of VHDL files to Verilog.

M3.2

- Successful completion of physical design phase.

M3.3

- Successful generation of GDSII files.

Work package number	**4**	Start date or starting event:		**Week 3:** (03.03.2025)	
Work package title	**Spintronic Circuit Design and Simulation Using MuMax3**				
Participant number	1	2	3		
Participant name	Damla Görgülü	İdil Görgülü	İsmet Erdem		
Weeks per participant	11	11	11		

Objectives

- Study spintronics and magnetization.
- Develop spintronic logic circuit equivalents of ALU, DTFT, and MLP.
- Simulate magnetization dynamics using MuMax3.
- Evaluate switching behavior and feasibility of spintronic designs.

Description of work

T4.1 (w3-w5)

- Study literature and complete introductory spintronics courses online.

T4.2 (w4-w6)

- Implement ALU using spintronic logic gates and simulate in MuMax3.

T4.3 (w6-w10)

- Develop and simulate DTFT and MLP using MuMax3.

T4.4(w9-w13)

- Analyze switching dynamics and performance using verification tools.

Deliverables

D4.1

- Simulated spintronic equivalents of ALU, DTFT, and MLP.

D4.2

- Performance analysis reports for each circuit.

Milestones

M4.1

- Finalized designs of the spintronics equivalents of ALU, DTFT and MLP circuits.

M4.2

- Performance analysis of ALU, DTFT and MLP.

Work package number	**5**	Start date or starting event:		**Week 7:** (31.03.2025)	
Work package title	**Comparative Performance Analysis & Reporting**				
Participant number	1	2	3		
Participant name	Damla Görgülü	İdil Görgülü	İsmet Erdem		
Weeks per participant	8	8	8		

Objectives

- Compare CMOS and spintronic designs in terms of power, latency, and area.
- Document key findings in a final report.
- Present results on demo day.

Description of work

T5.1 (w7-w10)

- Benchmark CMOS and spintronic circuits for key performance metrics.

T5.2 (w10-w12)

- Document comparative results and validate data.

T5.3 (w12-w14)

- Prepare a comprehensive report and presentation.

Deliverables

D5.1

- Detailed comparative analysis report.

D5.2

- Presentation slides for demo day.

Milestones

M5.1

- Completion of benchmarking study.

M5.2

- Final report and presentation delivered.

2.3 *Demonstration*

The success of the project hinges on providing a detailed comparison of speed, power consumption, and design area between the spintronic and microelectronic counterparts of all three circuits. We hypothesize that spintronic technology will outperform its microelectronic counterpart in these aspects. To ensure meaningful comparisons, parameters such as processing time, power consumption, and circuit area, that are further explained below, will be considered. Additionally, different trade-offs will be acknowledged for circuits with varying functionalities.

Process Time: Processing time is a key criterion for the performance of the circuits we will design in our project. In other words, it defines the latency of the circuit. The difference between the latency times to complete the same task will show us how much progress we have made. We will make these time measurements with the help of a simple counter logic in the CMOS circuit and with the counter in the simulation in the spintronic circuit.

Power Consumption: Power consumption has a significant role in the performance of the circuit. A circuit would have high process capability but it would need a high power supply. When a circuit needs high power you can't use it everywhere because of the power dependence. Therefore, reducing consumption is a key element for the integrated circuit (IC) design. In our project, we aim to design a more efficient spintronic-based design than an ordinary CMOS-based circuit.

Circuit Area: Larger IC area does not mean greater performance all the time. Indeed more transistors provide more process power. However, if the bus lines are very long between the system components, it would cause performance issues. Another issue is the cost of the circuit. When the design area gets larger, the resources you need to spend also increase which means cost increases. On the other hand, we need to consider the allowed design area that is a standard and provided by the chip manufacturer foundry. We believe that the spintronic-based circuit will cover less part of the allowed design boundaries to do the same task than the CMOS-based design.

Since the circuits are on a nanometer scale, the demonstration is not expected to be very human-interactive. We plan to show and compare results by using visuals from simulations and perform FPGA-based test runs. Besides, we will try our best to implement interactive UI for interactive tests and usage.

2.4 *Impact*

As planned, the implementation of Skyrmion-based logic is expected to create a significant effect on the efficiency and speed. The key impacts are listed below:

1. **Energy Efficiency and Sustainability**
    - Skyrmion-based logic offers lower switching energy consumption compared to traditional CMOS logic. In a complete design structure, it leads to a reduction in overall power consumption.
    - Making the computing power cost suitable for battery-powered and low-energy applications.
    - Reduced energy dissipation also aligns with global sustainability goals.

2. **Performance Enhancement**
    - Since skyrmion dynamics has ultra-fast switching capabilities, our proposed logic circuits are expected to outperform CMOS-based counterparts in terms of operational speed.
    - In other words, faster operations lead to improved computing performance in applications which require high speed.

3. **Scalability and Miniaturization**
    - The non-volatility and compact nature of skyrmion-based devices allows for further miniaturization beyond the scaling limits of conventional CMOS technology.
    - This advancement can enable high-density integration. Thus, it may contribute to the development of ultra-compact processors with enhanced computational power.

4. **New Computing Paradigms**
    - The development of skyrmion-based ALU, DTFT circuits, and MLP architectures will provide a basis for alternative logic families beyond CMOS.
    - These results can open a way for hybrid computing architectures that combine skyrmion-based and CMOS technologies which causes a new research area, hybrid design.

5. **Industrial and Academic Contributions**
    - Our project may provide crucial information for the semiconductor industry and academic research communities.
    - Comparative analysis of CMOS and skyrmion logic can contribute to the development of next-generation computing paradigms. Also it can influence future chip designs in AI accelerators, and neuromorphic computing.

Through these contributions, our project aims to set a new benchmark in efficient, high-speed, and scalable computing architectures. As a result, it can bridge the gap between spintronic technologies and real-world applications.

2.5 *Risk analysis*

1. **Inadequate FPGA or Chip Area**

Risk Description: We can encounter inadequate design space while realizing the CMOS-based designs.
Actions to be Taken:
- Try to implement techniques like pipelining, bit-width reduction, and hardware-sharing.
- Split the design into small parts and work on them separately.
- Switch the design to simpler.

2. **Incompatibility Issues with MuMax3 Software**

Risk Description: Since MuMax3 is a new software, it may cause unexpected and unknown errors.
Actions to be Taken:
- In order to ensure that MuMax3 supports the necessary architectures perform initial validation on each module.
- Use earlier successful circuit model scripts to complete MuMax3 circuit simulations.

3. **Limited Experimental Validation for Skyrmion Logic Performance**

Risk Description: Since the MuMax3 is a new software, its physical test environments may limit experimental validation.
Actions to be Taken:
- Confirm results using physics-based modeling then attempt to realize the hardware.
- Verify the accuracy of the simulated results by cross-referencing.

4. **Computational Complexity and Long Simulation Time**

Risk Description: Excessively long simulation times in micromagnetic circuits.
Actions to be Taken:
- Split the circuit into functional parts and only run the circuit parts that execute the skyrmion logic steps at that particular time. Assume the other parts of the circuit do not change while running the sub-section simulation of the circuit.

2.6 *Gantt Chart*

Weeks Tasks	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Literature review and software tool setup														
Design and simulation of memory structures														
Control unit and data path design														
Preparation for the Preliminary Design Review														
Integration with microprocessor controller and physical design														
Spintronic circuit design														
Preparation for the Critical Design Review (CDR)														
CMOS and spintronic circuit comparison														
Benchmarking and Reporting														

Table 1: Project Gantt Chart

Section 3 Ethical Issues

This project will stay in line with the IEEE Code of Ethics and does not have any concerns or doubts in terms of ethics. In case of the utilization of external resources, the appropriate licenses will be obtained.

Section 4 References

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